```
Running detail_route.tcl, stage 5_2_route
[INFO ORD-0030] Using 4 thread(s).
detailed_route -output_drc ./reports/nangate45/gcd/base/5_route_drc.rpt -output_maze
./results/nangate45/gcd/base/maze.log -bottom_routing_layer metal2 -top_routing_layer
metal10 -save_guide_updates -verbose 1 -drc_report_iter_step 5
[INFO DRT-0149] Reading tech and libs.

Units:                2000
Number of layers:     21
Number of macros:     135
Number of vias:       27
Number of viarulegen: 19

[INFO DRT-0150] Reading design.

Design:                   gcd
Die area:                 ( 0 0 ) ( 72760 72760 )
Number of track patterns: 20
Number of DEF vias:       0
Number of components:     669
Number of terminals:      54
Number of snets:          2
Number of nets:           692

[INFO DRT-0167] List of default vias:
  Layer via2
    default via: via2_5
  Layer via3
    default via: via3_2
  Layer via4
    default via: via4_0
  Layer via5
    default via: via5_0
  Layer via6
    default via: via6_0
  Layer via7
    default via: via7_0
  Layer via8
    default via: via8_0
  Layer via9
    default via: via9_0
[INFO DRT-0162] Library cell analysis.
[INFO DRT-0163] Instance analysis.
[INFO DRT-0164] Number of unique instances = 70.
[INFO DRT-0168] Init region query.
[INFO DRT-0024]   Complete active.
[INFO DRT-0024]   Complete Fr_VIA.
[INFO DRT-0024]   Complete metal1.
[INFO DRT-0024]   Complete via1.
[INFO DRT-0024]   Complete metal2.
```

```
[INFO DRT-0024]   Complete via2.
[INFO DRT-0024]   Complete metal3.
[INFO DRT-0024]   Complete via3.
[INFO DRT-0024]   Complete metal4.
[INFO DRT-0024]   Complete via4.
[INFO DRT-0024]   Complete metal5.
[INFO DRT-0024]   Complete via5.
[INFO DRT-0024]   Complete metal6.
[INFO DRT-0024]   Complete via6.
[INFO DRT-0024]   Complete metal7.
[INFO DRT-0024]   Complete via7.
[INFO DRT-0024]   Complete metal8.
[INFO DRT-0024]   Complete via8.
[INFO DRT-0024]   Complete metal9.
[INFO DRT-0024]   Complete via9.
[INFO DRT-0024]   Complete metal10.
[INFO DRT-0033] active shape region query size = 0.
[INFO DRT-0033] FR_VIA shape region query size = 0.
[INFO DRT-0033] metal1 shape region query size = 9624.
[INFO DRT-0033] via1 shape region query size = 75.
[INFO DRT-0033] metal2 shape region query size = 50.
[INFO DRT-0033] via2 shape region query size = 75.
[INFO DRT-0033] metal3 shape region query size = 50.
[INFO DRT-0033] via3 shape region query size = 75.
[INFO DRT-0033] metal4 shape region query size = 27.
[INFO DRT-0033] via4 shape region query size = 0.
[INFO DRT-0033] metal5 shape region query size = 28.
[INFO DRT-0033] via5 shape region query size = 0.
[INFO DRT-0033] metal6 shape region query size = 26.
[INFO DRT-0033] via6 shape region query size = 0.
[INFO DRT-0033] metal7 shape region query size = 0.
[INFO DRT-0033] via7 shape region query size = 0.
[INFO DRT-0033] metal8 shape region query size = 0.
[INFO DRT-0033] via8 shape region query size = 0.
[INFO DRT-0033] metal9 shape region query size = 0.
[INFO DRT-0033] via9 shape region query size = 0.
[INFO DRT-0033] metal10 shape region query size = 0.
[INFO DRT-0165] Start pin access.
[INFO DRT-0076]   Complete 100 pins.
[INFO DRT-0076]   Complete 200 pins.
[INFO DRT-0078]   Complete 210 pins.
[INFO DRT-0081]   Complete 66 unique inst patterns.
[INFO DRT-0084]   Complete 198 groups.
#scanned instances     = 669
#unique  instances     = 70
#stdCellGenAp          = 1761
#stdCellValidPlanarAp  = 0
#stdCellValidViaAp     = 1284
#stdCellPinNoAp        = 0
#stdCellPinCnt         = 1808
```

#instTermValidViaApCnt = 0
#macroGenAp = 0
#macroValidPlanarAp = 0
#macroValidViaAp = 0
#macroNoAp = 0
[INFO DRT-0166] Complete pin access.
[INFO DRT-0267] cpu time = 00:00:12, elapsed time = 00:00:03, memory = 97.43 (MB), peak = 97.43 (MB)

Number of guides: 4729

[INFO DRT-0169] Post process guides.
[INFO DRT-0176] GCELLGRID X 0 DO 17 STEP 4200 ;
[INFO DRT-0177] GCELLGRID Y 0 DO 17 STEP 4200 ;
[INFO DRT-0028] Complete active.
[INFO DRT-0028] Complete Fr_VIA.
[INFO DRT-0028] Complete metal1.
[INFO DRT-0028] Complete via1.
[INFO DRT-0028] Complete metal2.
[INFO DRT-0028] Complete via2.
[INFO DRT-0028] Complete metal3.
[INFO DRT-0028] Complete via3.
[INFO DRT-0028] Complete metal4.
[INFO DRT-0028] Complete via4.
[INFO DRT-0028] Complete metal5.
[INFO DRT-0028] Complete via5.
[INFO DRT-0028] Complete metal6.
[INFO DRT-0028] Complete via6.
[INFO DRT-0028] Complete metal7.
[INFO DRT-0028] Complete via7.
[INFO DRT-0028] Complete metal8.
[INFO DRT-0028] Complete via8.
[INFO DRT-0028] Complete metal9.
[INFO DRT-0028] Complete via9.
[INFO DRT-0028] Complete metal10.
[INFO DRT-0178] Init guide query.
[INFO DRT-0035] Complete active (guide).
[INFO DRT-0035] Complete Fr_VIA (guide).
[INFO DRT-0035] Complete metal1 (guide).
[INFO DRT-0035] Complete via1 (guide).
[INFO DRT-0035] Complete metal2 (guide).
[INFO DRT-0035] Complete via2 (guide).
[INFO DRT-0035] Complete metal3 (guide).
[INFO DRT-0035] Complete via3 (guide).
[INFO DRT-0035] Complete metal4 (guide).
[INFO DRT-0035] Complete via4 (guide).
[INFO DRT-0035] Complete metal5 (guide).
[INFO DRT-0035] Complete via5 (guide).
[INFO DRT-0035] Complete metal6 (guide).
[INFO DRT-0035] Complete via6 (guide).

[INFO DRT-0035] Complete metal7 (guide).
[INFO DRT-0035] Complete via7 (guide).
[INFO DRT-0035] Complete metal8 (guide).
[INFO DRT-0035] Complete via8 (guide).
[INFO DRT-0035] Complete metal9 (guide).
[INFO DRT-0035] Complete via9 (guide).
[INFO DRT-0035] Complete metal10 (guide).
[INFO DRT-0036] active guide region query size = 0.
[INFO DRT-0036] FR_VIA guide region query size = 0.
[INFO DRT-0036] metal1 guide region query size = 1544.
[INFO DRT-0036] via1 guide region query size = 0.
[INFO DRT-0036] metal2 guide region query size = 1277.
[INFO DRT-0036] via2 guide region query size = 0.
[INFO DRT-0036] metal3 guide region query size = 716.
[INFO DRT-0036] via3 guide region query size = 0.
[INFO DRT-0036] metal4 guide region query size = 137.
[INFO DRT-0036] via4 guide region query size = 0.
[INFO DRT-0036] metal5 guide region query size = 75.
[INFO DRT-0036] via5 guide region query size = 0.
[INFO DRT-0036] metal6 guide region query size = 27.
[INFO DRT-0036] via6 guide region query size = 0.
[INFO DRT-0036] metal7 guide region query size = 0.
[INFO DRT-0036] via7 guide region query size = 0.
[INFO DRT-0036] metal8 guide region query size = 0.
[INFO DRT-0036] via8 guide region query size = 0.
[INFO DRT-0036] metal9 guide region query size = 0.
[INFO DRT-0036] via9 guide region query size = 0.
[INFO DRT-0036] metal10 guide region query size = 0.
[INFO DRT-0179] Init gr pin query.
[INFO DRT-0185] Post process initialize RPin region query.
[INFO DRT-0181] Start track assignment.
[INFO DRT-0184] Done with 1441 vertical wires in 1 frboxes and 2335 horizontal wires in 1 frboxes.
[INFO DRT-0186] Done with 494 vertical wires in 1 frboxes and 544 horizontal wires in 1 frboxes.
[INFO DRT-0182] Complete track assignment.
[INFO DRT-0267] cpu time = 00:00:00, elapsed time = 00:00:00, memory = 108.22 (MB), peak = 108.22 (MB)
[INFO DRT-0187] Start routing data preparation.
[INFO DRT-0267] cpu time = 00:00:00, elapsed time = 00:00:00, memory = 108.22 (MB), peak = 108.22 (MB)
[INFO DRT-0194] Start detail routing.
[INFO DRT-0195] Start 0th optimization iteration.
    Completing 10% with 0 violations.
    elapsed time = 00:00:00, memory = 117.93 (MB).
    Completing 20% with 0 violations.
    elapsed time = 00:00:00, memory = 120.17 (MB).
    Completing 30% with 0 violations.
    elapsed time = 00:00:00, memory = 118.61 (MB).
    Completing 40% with 0 violations.

```
    elapsed time = 00:00:00, memory = 113.66 (MB).
    Completing 50% with 13 violations.
    elapsed time = 00:00:00, memory = 123.16 (MB).
    Completing 60% with 13 violations.
    elapsed time = 00:00:01, memory = 117.08 (MB).
    Completing 70% with 50 violations.
    elapsed time = 00:00:01, memory = 124.20 (MB).
    Completing 80% with 50 violations.
    elapsed time = 00:00:02, memory = 130.33 (MB).
    Completing 90% with 66 violations.
    elapsed time = 00:00:03, memory = 131.53 (MB).
    Completing 100% with 86 violations.
    elapsed time = 00:00:03, memory = 131.78 (MB).
[INFO DRT-0199]   Number of violations = 151.
Viol/Layer      metal1 metal2   via2 metal3 metal4   via4 metal5
Cut Spacing           0      0      0      0      0      1      0
Metal Spacing         3     14      0      2      0      0      0
Recheck               0     32      0     26      6      0      1
Short                 1     54      1     10      0      0      0
[INFO DRT-0267] cpu time = 00:00:05, elapsed time = 00:00:03, memory = 686.15 (MB),
peak = 686.15 (MB)
Total wire length = 4471 um.
Total wire length on LAYER metal1 = 0 um.
Total wire length on LAYER metal2 = 1770 um.
Total wire length on LAYER metal3 = 1982 um.
Total wire length on LAYER metal4 = 437 um.
Total wire length on LAYER metal5 = 223 um.
Total wire length on LAYER metal6 = 57 um.
Total wire length on LAYER metal7 = 0 um.
Total wire length on LAYER metal8 = 0 um.
Total wire length on LAYER metal9 = 0 um.
Total wire length on LAYER metal10 = 0 um.
Total number of vias = 3675.
Up-via summary (total 3675):.

---------------
 active       0
 metal1    1774
 metal2    1615
 metal3     167
 metal4      91
 metal5      28
 metal6       0
 metal7       0
 metal8       0
 metal9       0
---------------
          3675
```

```
[INFO DRT-0195] Start 1st optimization iteration.
    Completing 10% with 151 violations.
    elapsed time = 00:00:00, memory = 690.65 (MB).
    Completing 20% with 151 violations.
    elapsed time = 00:00:00, memory = 691.15 (MB).
    Completing 30% with 151 violations.
    elapsed time = 00:00:00, memory = 691.28 (MB).
    Completing 40% with 151 violations.
    elapsed time = 00:00:00, memory = 693.28 (MB).
    Completing 50% with 125 violations.
    elapsed time = 00:00:00, memory = 700.15 (MB).
    Completing 60% with 125 violations.
    elapsed time = 00:00:01, memory = 700.15 (MB).
    Completing 70% with 62 violations.
    elapsed time = 00:00:01, memory = 700.65 (MB).
    Completing 80% with 62 violations.
    elapsed time = 00:00:01, memory = 701.78 (MB).
    Completing 90% with 34 violations.
    elapsed time = 00:00:02, memory = 706.78 (MB).
    Completing 100% with 17 violations.
    elapsed time = 00:00:02, memory = 706.78 (MB).
[INFO DRT-0199]   Number of violations = 17.
Viol/Layer      metal2
Metal Spacing        2
Short               15
[INFO DRT-0267] cpu time = 00:00:04, elapsed time = 00:00:02, memory = 707.78 (MB),
peak = 707.78 (MB)
Total wire length = 4417 um.
Total wire length on LAYER metal1 = 0 um.
Total wire length on LAYER metal2 = 1744 um.
Total wire length on LAYER metal3 = 1978 um.
Total wire length on LAYER metal4 = 433 um.
Total wire length on LAYER metal5 = 202 um.
Total wire length on LAYER metal6 = 57 um.
Total wire length on LAYER metal7 = 0 um.
Total wire length on LAYER metal8 = 0 um.
Total wire length on LAYER metal9 = 0 um.
Total wire length on LAYER metal10 = 0 um.
Total number of vias = 3653.
Up-via summary (total 3653):.

---------------
 active       0
 metal1    1774
 metal2    1595
 metal3     166
 metal4      90
 metal5      28
 metal6       0
 metal7       0
```

```
 metal8       0
 metal9       0
---------------
          3653


[INFO DRT-0195] Start 2nd optimization iteration.
    Completing 10% with 17 violations.
    elapsed time = 00:00:00, memory = 707.78 (MB).
    Completing 20% with 17 violations.
    elapsed time = 00:00:00, memory = 707.78 (MB).
    Completing 30% with 16 violations.
    elapsed time = 00:00:00, memory = 707.78 (MB).
    Completing 40% with 16 violations.
    elapsed time = 00:00:00, memory = 707.78 (MB).
    Completing 50% with 16 violations.
    elapsed time = 00:00:01, memory = 707.86 (MB).
    Completing 60% with 23 violations.
    elapsed time = 00:00:01, memory = 707.86 (MB).
    Completing 70% with 23 violations.
    elapsed time = 00:00:01, memory = 709.11 (MB).
    Completing 80% with 25 violations.
    elapsed time = 00:00:01, memory = 709.11 (MB).
    Completing 90% with 25 violations.
    elapsed time = 00:00:01, memory = 717.36 (MB).
    Completing 100% with 16 violations.
    elapsed time = 00:00:02, memory = 709.25 (MB).
[INFO DRT-0199]   Number of violations = 16.
Viol/Layer      metal2 metal3
Metal Spacing        2      0
Short               10      4
[INFO DRT-0267] cpu time = 00:00:02, elapsed time = 00:00:02, memory = 709.25 (MB),
peak = 717.36 (MB)
Total wire length = 4405 um.
Total wire length on LAYER metal1 = 0 um.
Total wire length on LAYER metal2 = 1742 um.
Total wire length on LAYER metal3 = 1976 um.
Total wire length on LAYER metal4 = 431 um.
Total wire length on LAYER metal5 = 197 um.
Total wire length on LAYER metal6 = 57 um.
Total wire length on LAYER metal7 = 0 um.
Total wire length on LAYER metal8 = 0 um.
Total wire length on LAYER metal9 = 0 um.
Total wire length on LAYER metal10 = 0 um.
Total number of vias = 3632.
Up-via summary (total 3632):.

---------------
 active       0
 metal1    1774
```

```
 metal2    1577
 metal3     168
 metal4      85
 metal5      28
 metal6       0
 metal7       0
 metal8       0
 metal9       0
---------------
          3632


[INFO DRT-0195] Start 3rd optimization iteration.
    Completing 10% with 16 violations.
    elapsed time = 00:00:00, memory = 709.25 (MB).
    Completing 20% with 16 violations.
    elapsed time = 00:00:00, memory = 709.25 (MB).
    Completing 30% with 16 violations.
    elapsed time = 00:00:00, memory = 709.25 (MB).
    Completing 40% with 16 violations.
    elapsed time = 00:00:00, memory = 709.25 (MB).
    Completing 50% with 6 violations.
    elapsed time = 00:00:00, memory = 709.25 (MB).
    Completing 60% with 6 violations.
    elapsed time = 00:00:00, memory = 709.25 (MB).
    Completing 70% with 6 violations.
    elapsed time = 00:00:00, memory = 709.25 (MB).
    Completing 80% with 6 violations.
    elapsed time = 00:00:00, memory = 709.25 (MB).
    Completing 90% with 2 violations.
    elapsed time = 00:00:00, memory = 711.75 (MB).
    Completing 100% with 0 violations.
    elapsed time = 00:00:00, memory = 711.75 (MB).
[INFO DRT-0199]   Number of violations = 0.
[INFO DRT-0267] cpu time = 00:00:01, elapsed time = 00:00:00, memory = 711.75 (MB),
peak = 717.36 (MB)
Total wire length = 4409 um.
Total wire length on LAYER metal1 = 0 um.
Total wire length on LAYER metal2 = 1733 um.
Total wire length on LAYER metal3 = 1978 um.
Total wire length on LAYER metal4 = 441 um.
Total wire length on LAYER metal5 = 197 um.
Total wire length on LAYER metal6 = 57 um.
Total wire length on LAYER metal7 = 0 um.
Total wire length on LAYER metal8 = 0 um.
Total wire length on LAYER metal9 = 0 um.
Total wire length on LAYER metal10 = 0 um.
Total number of vias = 3648.
Up-via summary (total 3648):.
```

---
 active   0
 metal1   1774
 metal2   1588
 metal3   173
 metal4   85
 metal5   28
 metal6   0
 metal7   0
 metal8   0
 metal9   0

          3648

[INFO DRT-0198] Complete detail routing.
Total wire length = 4409 um.
Total wire length on LAYER metal1 = 0 um.
Total wire length on LAYER metal2 = 1733 um.
Total wire length on LAYER metal3 = 1978 um.
Total wire length on LAYER metal4 = 441 um.
Total wire length on LAYER metal5 = 197 um.
Total wire length on LAYER metal6 = 57 um.
Total wire length on LAYER metal7 = 0 um.
Total wire length on LAYER metal8 = 0 um.
Total wire length on LAYER metal9 = 0 um.
Total wire length on LAYER metal10 = 0 um.
Total number of vias = 3648.
Up-via summary (total 3648):.

---
 active   0
 metal1   1774
 metal2   1588
 metal3   173
 metal4   85
 metal5   28
 metal6   0
 metal7   0
 metal8   0
 metal9   0

          3648

[INFO DRT-0267] cpu time = 00:00:13, elapsed time = 00:00:09, memory = 711.75 (MB), peak = 717.36 (MB)

[INFO DRT-0180] Post processing.
[WARNING GRT-0246] No diode with LEF class CORE ANTENNACELL found.

Error: detail_route.tcl, 64 expected boolean value but got ""
Command exited with non-zero status 1
Elapsed time: 0:13.78[h:]min:sec. CPU time: user 27.01 sys 0.34 (198%). Peak memory: 734576KB.
make[1]: *** [Makefile:789: do-5_2_route] Error 1
make: *** [Makefile:787: results/nangate45/gcd/base/5_2_route.odb] Error 2