ADDENDUM 1 - ABSTRACT FROM PAGE 2

Joysticks/Peripherals

It is possible to connect various peripherals to the I/O Port other than joysticks. Each peripheral has its own ID Code and it is possible for the CPU to check the code to identify what is connected. Be aware that there are some Master System peripherals, which cannot be identified by this method.

S1 ID Code

The ID Code for the external ports, CTRL1, CTRL2, and EXT., which correspond to the I/O Port's DATA1, 2, 3 (PD3, PD2, PD0) are shown by a logical "or" operation. In concrete terms, setting the TH Pin to output mode and outputting either 1 or 0 as data will yield the following.

```
ID3 = (PD6 = 1) AND (PD3 OR PD2)
ID2 = (PD6 = 1) AND (PD1 OR PD0)
ID1 = (PD6 = 0) AND (PD3 OR PD2)
ID0 = (PD6 = 0) AND (PD1 OR PD0)
```

The relationship between the ID Code and the peripheral hardware is shown below.

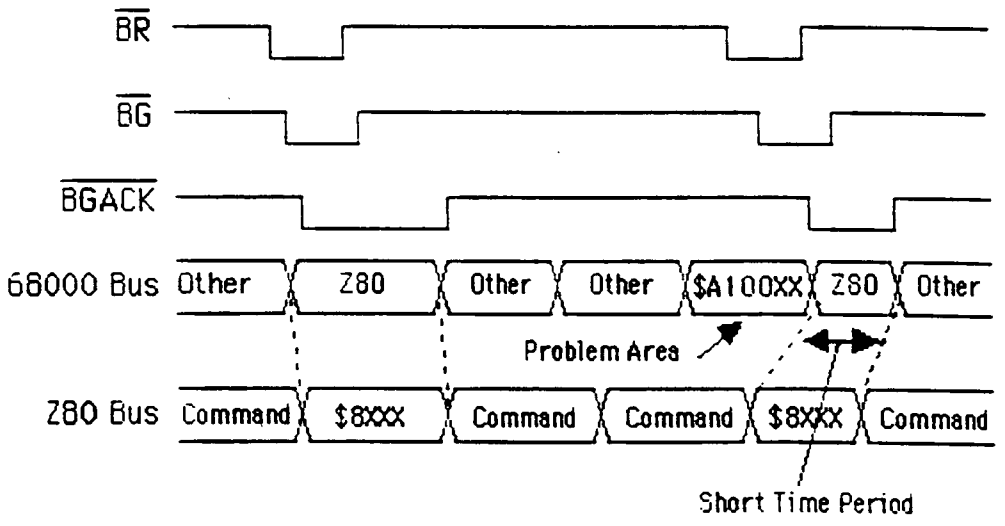
Device Name	ID3	ID2	ID1	ID0		
Old Style Joystick (2 trig):	1	1	1	1	($F)	If no joystick
Undefined:	1	1	1	0	($E)	
New Style Joystick (3 trig):	1	1	0	1	($D)	Power stick
Sega Reserved:	1	1	0	0	($C)	
Undefined:	1	0	1	1	($B)	
Sega Reserved:	1	0	1	0	($A)	
Undefined:	1	0	0	1	($9)	
Undefined:	1	0	0	0	($8)	
Undefined:	0	1	1	1	($7)	
Undefined:	0	1	1	0	($6)	
Sega Reserved:	0	1	0	1	($5)	
Undefined:	0	1	0	0	($4)	
Undefined:	0	0	1	1	($3)	
Undefined:	0	0	1	0	($2)	
Undefined:	0	0	0	1	($1)	
Sega Reserved:	0	0	0	0	($0)	

ADDENDUM 2 - NO ADDENDUM 2

ADDENDUM 3 - ABSTRACT FROM PAGE 1

1. When The Z80 Cannot Do A 68000 Bus Access

There are times when the Z80 cannot read or write good data in the 68000's addresses. If the 68000's bus cycle accesses $100XX prior to the Z80's interrupt, the bus cycle for the Z80 interrupt is shortened. When this occurs, the Z80 cannot read or write good data.



When The 68000 Is Accessing $A100XX

1. A BUSREQ is sent to the Z80. (Stops the Z80 bus access- $A11100=0100H)

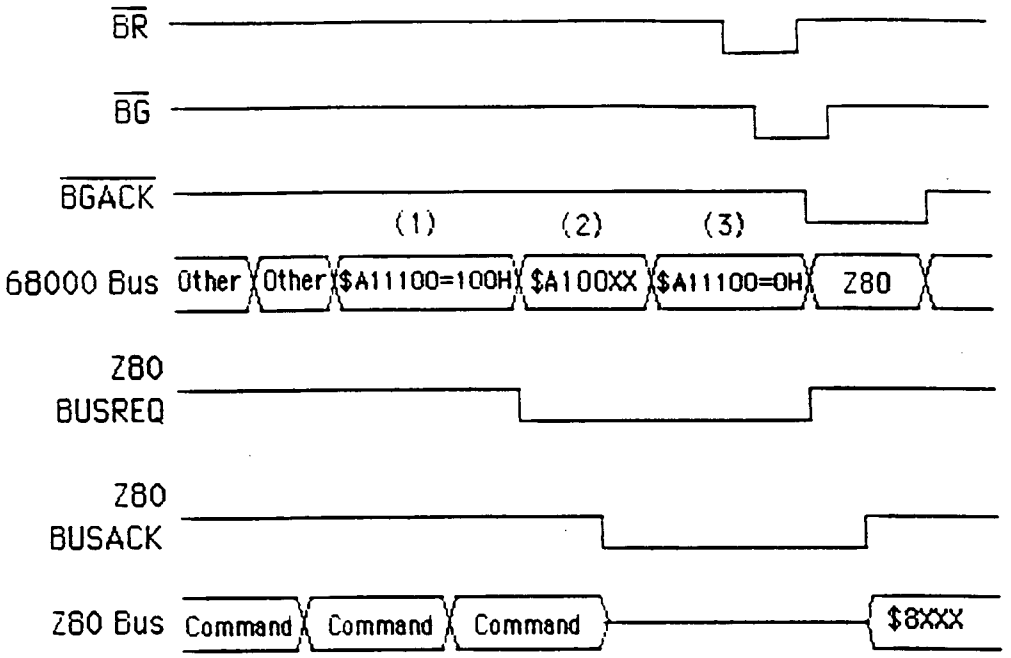
2. A100XX is accessed.

3. The BUSREQ from the Z80 is cleared. (The Z80 begins bus access- $A11100=0000H)

Change the 68000's programs to follow the steps shown above.

Miscellaneous

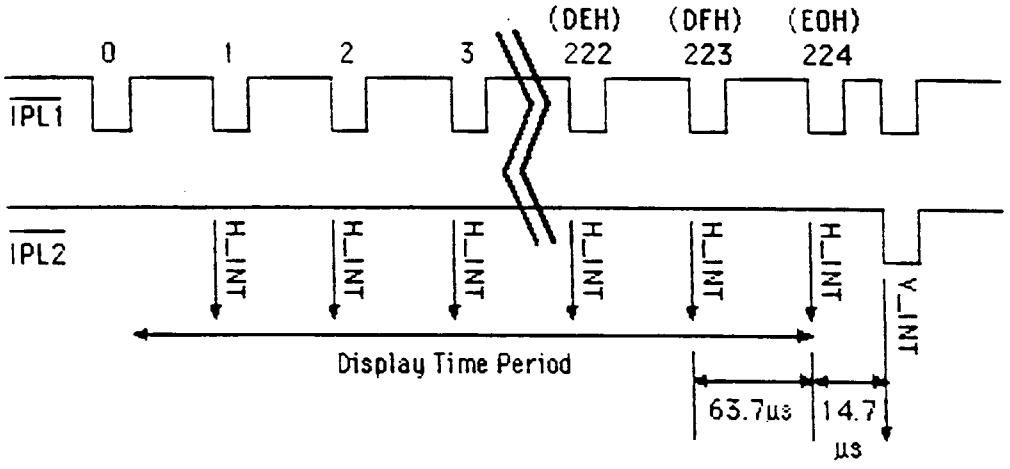
If the program structure uses something like V_INT for sync, there should be no problems as long as it is set up so that unfavorable bus access patterns are not created.


BR
BG
BGACK
(1)
(2)
(3)
68000 Bus
Other
Other
$A11100=100H
$A100XX
$A11100=0H
Z80
Z80
BUSREQ
Z80
BUSACK
Z80 Bus
Command
Command
Command
$8XXX

ADDENDUM 3 - ABSTRACT FROM PAGE 2

2. When Using H_INT And V_INT With A Genesis Program

When the VDP register #0's IE1=1 and register #10=00H,H_INT and V_INT are created with the timing scheme described below. However, a problem occurs during No.224H_INT's timing. Since the amount of time which is available before V_INT is only 14.7µs, the acceptance of the No.224H_INT means that the V_INT will miss the V_INT occurrence period. As a result, V_INT is cancelled. Moreover, when the V_INT is cancelled, the No.225H_INT occurs instead of the V_INT.



Solution A

1. Set register #0's IE1=0 before No.223H_INT ends in order to prevent No.224 from occurring.

2. Set register #0's IE1=1 before V_INT is accepted in order to make H_INT valid. (i.e., No.224 also becomes valid)

3. Process No.224H_INT.

Solution B

1. Set the 68000's SR=25XX before No.223H_INT ends in order to prevent No.224 from being processed.[1]

2. Restore the 68000's SR prior to the end of V_INT processing. (Enables No.224 processing)

3. Process No.224H_INT.

---

[1]**Warning:** When manipulating SR, make sure not to destroy the flag.

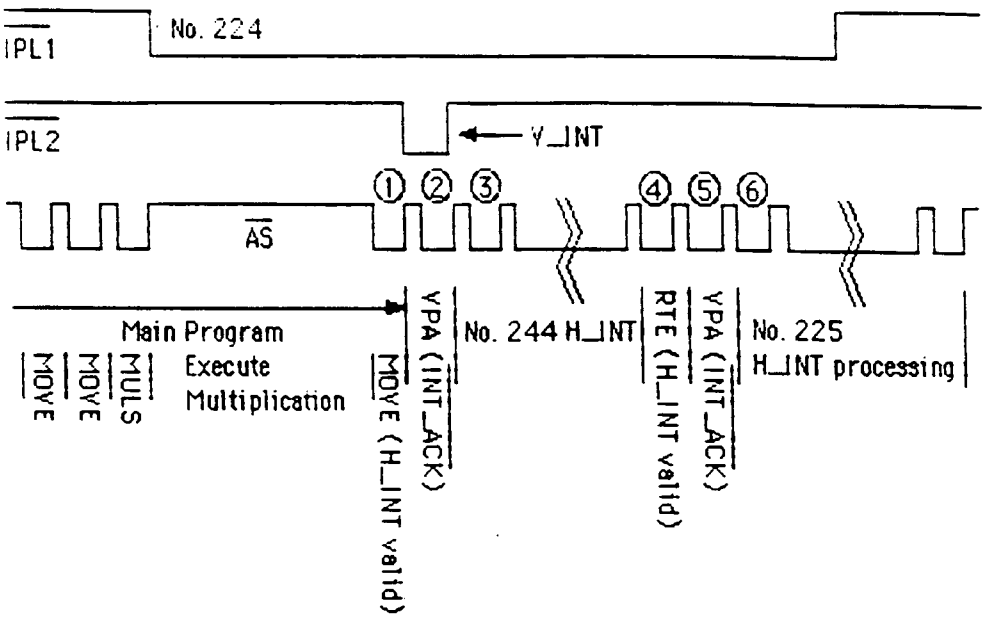


Diagram Of The Problem Caused By A Multiplication Command

1. The MOVE command given after multiplication readies the 68000 to process H_INT.

2. The 68000 creates a VPA (INT_ACK). Since the VDP (for processing No.224) does not see a VPA after H_INT occurs, H_INT is not processed. After V_INT occurs, the 68000 receives a VPA and mistakes this for V_INT processing. H_INT is stored.

3. Processing is executed since H_INT (No.224) was received in Part 1.

4. Given a RTE after processing H_INT, the 68000 readies to process H_INT again.

5. The 68000 creates a VPA (INT_ACK). The VDP (equivalent to No.225) processes the stored H_INT.

6. Receiving H_INT (No.225) in Part 4, processing occurs again.

ADDENDUM 3 - ABSTRACT FROM PAGE 4

4. The Interrupt Problem During Data Transfer

Part 2 discussed the problems encountered when using H_INT and V_INT in a program. The same kinds of problems occur during a) an INT involving H_INT data reception and b) an INT involving V_INT and data reception. (Refer back to Part 2 for details)

The "INT during data reception" does not occur in sync in relation to V_INT and H_INT; therefore, the solutions to the problem are different.

Solution In The Case of a)

During data reception, the receive flag is set at the same tine of the INT. The receive flag is cleared when the data is read by the "INT during data reception," which does not overlap with H_INT. When H_INT occurs again, it overlaps and passes as the second "INT during data reception." After this occurs, the receive flag is left in clear status.

Solve the problem by discriminating between the "INT during data reception" and the H_INT, which passes as the "INT during data reception." This can be determined by checking on the status of the receive flag.

Solution In The Case of b)

Set the mode, which prevents the occurrence of V_INT's, and then, use the VDP's V_BLK status bit to detect V-timing. Use this method to perform the same type of processing as V_INT.

Miscellaneous

It is possible to differentiate H_INT and V_INT timing by using H_BLK, V_BLK, and the HV_counter.

It is possible to distinguish between the "INT during data reception" and the "H and V that pass as the INT during data reception" by analyzing the receive flag.

Try to think of other solutions by using IE0, IE1, and IE2 settings within the VDP register.

ADDENDUM 4

1. Regarding The DMA

When using DMA's other than *FILL VRAM* and *VRAM COPY*, use the following method to program:

1) Send a bus request to the Z80.
2) Base the DMA destination address set section in RAM.
3) Rewrite the one leading word of data after the end of the DMA.

1) and 2) are used in all cases, except FILL VRAM and VRAM COPY.
3) is used for WRAM to VRAM, WRAM to COLOR RAM, and WRAM to VSRAM.

2. Compatibility With The MKIII Mode

VDP Registers #11 through #23 cannot be written over, unless bit 2 of Register #1 is not set to "1."

Reasons:

- Registers #11 through #23 are masked for MKIII mode's error trapping purposes.
- MKIII uses Registers #0 through #10.
- The Genesis mode is active when Register #1's bit 2=1.
- The registers are set to 0 on power up.

3. Warnings Regarding Use Of Back-Up RAM

- The back-up RAM data is unformatted when the cartridge (product) is shipped. Always make sure to initialize during power up. (In most cases, the back-up RAM data is cleared with $FF at the factory; however, don't count on this as a matter of fact.)
- Although this does not occur frequently, there may be occasions when the data becomes garbled. Because of this possibility, make sure to check the back-up data and perform reproduction/retrieval processing. Moreover, do not place critical data at leading and ending RAM addresses, since one word in both addresses have a high probability of becoming garbled.