I. Software Guidelines

1. When accessing the Z80 area from within the 68000's main routine, beware of the following:

1) Execute a bus request to the Z80.
2) Confirm execution.
3) An interrupt occurs.
4) A Z80 bus request is executed within the interrupt routine. (Execute for the purpose of reading the controller pad)
5) The bus request is cleared within the interrupt.
6) Return to main routine.
7) Write data to Z80 area.

In principle, the Z80 is left with the Z80 bus request in effect; however, in this example, it is cleared in Step 5).

When this occurs, the following things occur:

- The RAM of the Z80 gets damaged.
- Incorrect data is read during Z80 bank access.

A Fix For The Problem:

Disable interrupts prior to Step 1).

2. Problems During Sound Access

1) Sound output stops during the game.

Diagnosis Of The Problem:

The busy flag was read in the FM sound generator YM2612 like this (address 4001H was accessed in the Mega Drive):

(CS,RD,WR,A1,A0)=(0,0,1,0,1)

However, in the case of the YM2612, its output is not regulated according to the conditions set up above. This results in the device being read as "not busy," and as a consequence, ends up outputting sound.

A Fix For The Problem:

When the FM sound generator's busy flag is read, do not access anything else other than:

(A1,A0)=(0,0) (Mega Drive address 4000H)

3. Repeated Resets

1) The software goes out of control when resets are repeated.

Diagnosis Of The Problem:

- When the reset occurs, the CPU is reset; however, the VDP is not reset.
- When the reset occurs during DMA, the VDP continues the DMA.
- The VDP is accessed right after the reset. If this is done while the VDP is executing a DMA, then this access becomes ineffective.

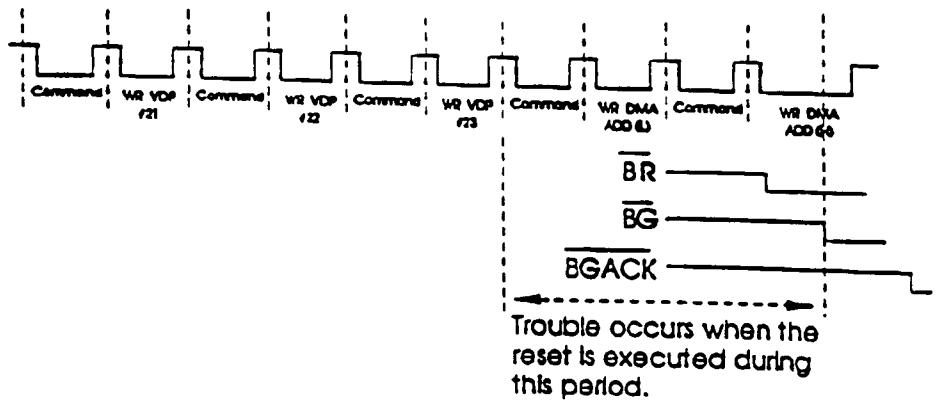
A Fix For The Problem:

Before accessing the VDP after the initialization program (ICD_BLK4), check the DMA BUSY status register. If a DMA is being executed, do not attempt to access.

2) The problem still persists even after the precautions above are taken.

Diagnosis Of The Problem:

The problem will occur when the reset takes place between the period of time when the CPU has finished setting the parameters to execute the DMA and the actual execution of the DMA itself.



A Fix For The Problem:

On top of the precautions taken in 1), as an example, make sure not to execute a DMA right after a reset.

II. Corrections To The Manual

When discussing VRAM, CRAM, VSRAM access, the manual states in Pages 22-27 that byte access is possible; however, in reality, this is false.[1] The reason for this is that after the VDP address register is set, an instruction for a CPU word access (ex. a fetch operation) causes the VDP to think during the next access that it is still a word access.

From now on, please consider the text regarding byte access in Pages 22-27 as being null and void.

Corrections to Mega Drive Addendum 6, Page 3

III. About Control Pads

Although the control pad is designed and produced so that simultaneous up/down or left/right input is impossible, there are times when simultaneous input occurs due to fatigue of the internal rubber parts or force on the pads, which exceed design specs. **Because of this, from now on, all software should have switch read routines that can process simultaneous directional input.**

Corrections to MD Manual, Page 77

IV. Bank Switching

Although the manual states that the 68000 may set the bank registers; however, in reality, this is not the case. Please execute bank switching in the Z80 from the Z80.

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[1] **Translator's Note:** The page numbers are from the original Japanese-language manual.