

**GENESIS SOFTWARE
DEVELOPMENT MANUAL**

<<COMPLEMENT>>

sega

genesisoft

**9. JUL 1991 REVISION
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REQUIRED ITEMS TO SET UP THE GENESIS

S 1 CARTRIDGE

The following data (hereafter ID) must always be entered from the address 100H.

100H	'SEGA MEGA DRIVE'	: 1
110H	'(C)SEGA 1991.MAR'	: 2
120H	'GAME NAME FOR DOMESTIC USE'	: 3
150H	'GAME NAME FOR OVERSEAS USE'	: 4
180H	'GM XXXXXXXX-XX'	: 5
18EH	\$XXXX	: 6
190H	CONTROL DATA	: 7
1A0H	\$000000,\$XXXXXX	: 8
1A8H	\$FF0000,\$FFFFFF	: 9
1B0H	EXTERNAL RAM INFORMATION	: 10
1BCH	MODEM INFORMATION	: 11
1C8H	INHIBITED TO BE USED	: 12
1FH	COUNTRY NAME	: 13

● Descriptions on the above items

1. Hardware name : 'SEGA MEGA DRIVE' or 'SEGA GENESIS'
2. A company name of four characters long or company code is entered after (C).
 (C) SEGA when made or ordered by SEGA.
 (C) T-XX(company code) when made by a third party.
3. A domestic game name is entered (shifted JIS kanji character codes can be used; however, the name should be entered with as many ASCII characters as possible).
4. A overseas game name is entered (shifted JIS kanji character codes can be used; however, the name should be entered with as many ASCII characters as possible).
5. Type of the cartridge, product number and version number.
 Cartridge type : GM for game
 AI for education
 Product number : Unique number for each game
 Version : This number should be increased when the product is upgraded.
6. Check sum (see 'check sum')
7. Information on supports for I/O

MARK III Joy Stick	: O
GENESIS Joy Stick	: J
Keyboard	: K
Serial (RS232C)	: R
Printer	: P
Tablet	: T
Track ball	: B
Paddle controller	: V
FDD	: F
CDROM	: C
Analog Joy Stick	: A

8. ROM capacity : Start address, End address
****Example**

	Start address	End address
2M :	\$000000	\$03FFFF
4M :	\$000000	\$07FFFF
8M :	\$000000	\$0FFFFFF

9. RAM capacity (fixed) from \$FF0000 to \$FFFFFF

10. External RAM information (see below)

11. Modem information (see below)

12. Inhibited to be used (filled with spaces)

13. Country name

Japan	:	J
USA	:	U
Europe	:	E

※Note※ Blank addresses must always be filled with spaces.

- The data must be entered carefully, since the ID data will be used when the product is checked.
- The ID data and the initial program must always be input during the check sample process (see '2 Initial program').

S 2 INITIAL PROGRAM

The initial program (see ICD_BLK4.PRG, in the sample program disc) must always be stored in every product, in order to set every product to the same status when the GENESIS is powered on, and to execute the hardware security process and other required processes which must be performed at the resetting.

This program must always be input as it is, starting with program start. Remember that any product cannot be released, if its initial program is modified, or if it is not input starting with program start.

S 3 INDICATION OF EXTERNAL RAM INFORMATION

1B0H : dc.b 'RA',%1x1yz000,%abcdefg
 1B4H : dc.l Start address,End address

- x : Data preservation
 - 1 ... Non-volatile ... Backup, EEPROM, etc. where data will not be destroyed even if the power is turned off.
 - 0 ... Volatile Data will be lost when the power is turned off
- yz : Data size
 - 10 Even byte (D15 to D8)
 - 11 Odd byte (D7 to D0)
 - 00 Word
 - 01 Others (EEPROMs which are serially accessed, RAMs with 4-bit data bus, etc.)
- abc : Device type
 - 000
 - 001 ... SRAM
 - 010 ... EEPROM
 - 011
 - 100
 - 101
 - 110
 - 111
- defgh : Spare which is filled with 0s.

● Start address, End address

Addresses where RAMs are installed or areas of the control ports.

● Indication examples ●

- 8k byte backup RAM cartridge
 - + SRAM backup memory
 - + Odd bytes only
 - + 8k byte capacity
 - + Addresses \$200001,\$203FFF
 - +

dc.b 'RA',%11111000,%00100000
 dc.l \$200001,\$203FFF

- EEPROM cartridge (for modem)

Since the EEPROM for modem is accessed serially, the data size fits into 'others.' Its data preservation fits into '1' since data in EEPROMs will not be destroyed when the power is turned off. The address is set to \$200001 for the control ports.

- + EEPROM memory
- + Serial access
- + 1k bit capacity (128 × 8)
- + Addresses \$200001,\$200001
- +

dc.b 'RA',%11101000,%01000000
 dc.l \$200001,\$200001

S 4

INDICATION OF ID MODEM INFORMATION

1BCH: 'MO', 'company name', 'xx,y', 'zz'

- Company name : Same as the company name or code which is entered from 110H.
- xx : Game number (if this number is the same, communication can be performed)
 - 00 TELTEL stadium
 - 01 TELTEL majong
 - 02 MEGA answer
 - 03 SEGA NET GAME
 - ⋮
- y : Version No.
- zz : Modem information
 - 00 Japan only : No microphone installed
 - 10 Japan only : Microphone installed
 - 20 Overseas only : No microphone installed
 - 30 Overseas only : Microphone installed
 - 40 Common to Japan and overseas : No microphone installed
 - 50 Common to Japan and overseas : Microphone installed
 - 60 No microphone installed for Japan;
microphone installed for overseas
 - 70 Microphone installed for Japan;
no microphone installed for overseas
 - 80
 - 90

● Indication examples ●

- ① If SEGA released a base ball game 'abcde' with a microphone, then the modem information is like this.

1BCH : 'MO', 'SEGA', '00,0', '10'

- ② After that, TOTO (third party with a company code of T-01) released the software 'xyz' with a microphone for Japan use only, which can communicate with ① abcde'. Then the modem information is like this:

1BCH : 'MO', 'T-01', '00,1', '10'

xx is common, but the version number in y is changed.
Since xx is common, the information indicates that ① and ② can communicate each other.

Note that the game number and the version number are managed by SEGA of JAPAN.

S 5 CHECK SUM

The program to examine the check sum is given below. The program starts at 0FF8000H in the RAM space.

First fill the space to be used for this game with -1 (0FFH), and then load all the programs. After this, load this program (including the check sum program), and start it at 0FF8000H. Wait a while and stop the program. The check sum value is stored in the lower word of data register 0 (d0). It is a good idea to release the break points in the memory.

The space to be used for the game must also be filled with -1 (0FFH) before the programs are stored in the ROM.

```
end_addr    equ      $1a4
org        -$8000

start:
    lea      end_addr,a0
    move.l  (a0),d1
    addq.l  #$1,d1
    movea.l #$200,a0
    sub.l   a0,d1
    asr.l   #1,d1
    move    d1,d2
    subq.w  #$1,d2
    swap   d1
    moveq   $$0,d0

?12:
    add     (a0)+,d0
    dbra   d2,?12
    dbra   d1,?12
    nop
    nop
    nop
    nop
    nop
    nop
    nop
    nop
```

```
?1e:
    nop
    nop
    bra.b  ?1e
```

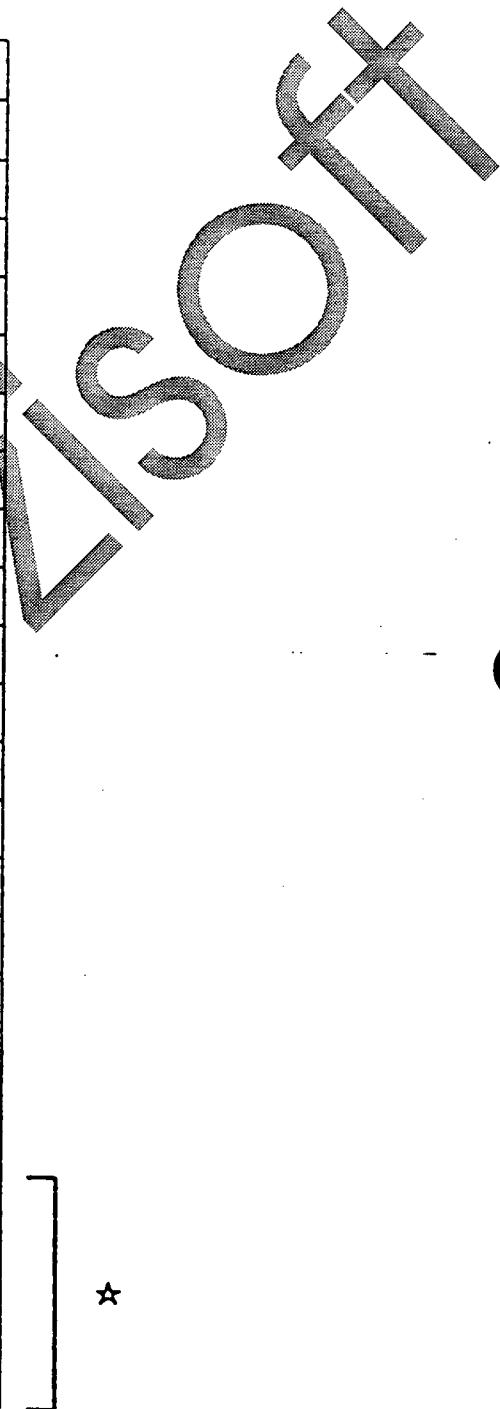
: counter

2.

VDP SETUP DATA

The followings must always be fixed.
(40-cell mode and NTSC mode)

R 0	0	0	0		0	1	0	0
1	0				0	1	0	0
2	0	0				0	0	0
3	0	0						0
4	0	0	0	0	0			
5	0							
6	0	0	0	0	0	0	0	0
7	0	0						
8	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0
10								
11	0	0	0	0	0			
12	1	0	0	0				1
13	0	0						
14	0	0	0	0	0	0	0	0
15								
16	0	0			0	0		
17	0	0						
18	0	0						
19								
20								
21								
22								
23								



* The DMA registers should be set in such a way that only the actual memory is accessed. Don't attempt to use the techniques taking advantage of image, etc.

③

SETTINGS TO PRESERVE COMPATIBILITY DURING GENESIS DEVELOPMENT

- I1 mode on the 68000 side (also applies to ER-ICE, 178 and 378)

① Cartridge in use

MA 0000000,0FFFFF=NO (No Memory is assigned for all areas)
 MA 0000000,007FFFF=US (Only required portion of the DRAM area is assigned)
 MA 0A00000,0A01FFF=US (Z80 S-RAM area)
 MA 0A04000,0A04FFF=US (FM sound source area)
 MA 0A10000,0A11FFF=US (I/O and Z80 control)
 MA 0C00000,0C00FFF=US (VDP and sound control)
 MA 0FF0000,0FFFFFF=US (work RAM area)

[Note] When the write protect function is used on the DRAM board, the following steps need to be conducted.

- STEP
1. MA 0A13000,0A13FFF=US
 2. E 0A130F0=XXXX (Setting up or releasing)
 3. MA 0A13000,0A13FFF=NO

It is easier to define a macro by conducting the above steps.

- I2 mode on the Z80 side (also applies to 178, 278 and 378)

MA 00000,0FFFF=NO (No memory is assigned for all areas)
 MA 00000,01FFF=US (Z80 SRAM area)
 MA 04000,043FF=US (Y=2612 area)
 MA 06000,063FF=US (bank register area)
 MA 07C00,07FFF=US (PSG on the VDP side)
 MA 08000,0FFFFFF=US (68000 memory area)

4.**68000 COMMANDS AND PERIPHERAL DEVICES****S 1****VDP AND 68000 COMMANDS**

The TAS command is not supported on the GENESIS. The TAS command serves to test and set up the byte operands which are assigned by the effective address fields. If this command is issued, the test is executed and completed, but the setting will be ignored and not be written.

When VRAM access is made, reading in the write mode or writing in the read mode cannot be executed.

- If an attempt is made to read in the write mode when VRAM access is performed, the VDP suspends the 68000 (the VDP will not return DTACK to the 68000).
- If an attempt is made to write in the read mode when VRAM access is performed, the address for the VRAM access is only increased, but no data is written in the VRAM.

For these reasons, the following commands cannot be used to access the VRAM.

Example: CLR command

The CLR command attempts to write 0 after reading the target memory. The VDP suspends the 68000, since the read access occurs when the write access is made to the VRAM.

**** others ****

CLR, NBCD, NEG, NEGX, NOT, Scc, TAS, (single operand commands),
 BCHG, BSET, BCLR,)bit handling commands)
 ASR, ASL, LSR, LSL, ROR, ROL, ROXR, ROXL (shift and rotate commands), ADDI, ADDQ, ANDI,
 CMPI, EORI, ORI, SUBI, SUBQ (immediate commands)
 (The above commands cannot be used to access the VRAM, since read and write operations
 are made to a single destination in these commands).

S 2 JOYSTICK AND PERIPHERAL DEVICES

In addition to the joy stick, various peripheral devices can be connected to the I/O port. Since such devices have their own ID codes, the CPU can judge which devices are connected to the I/O port by examining their ID codes. However, remember that some peripheral devices of the MARK III & MS cannot be known by this method.

◊ ID codes ◊

The ID code is expressed by the OR sum logic of DATA 1, 2 and 3, PD3, PD2, PD1 and PD0 which correspond to the external pins, CTRL1, CTRL2 and EXT in the I/O port. The OR sum value is expressed in the following way by data when 1 is output and by data when 0 is output, provided that the TH pin is set in the output mode.

$$\begin{aligned} ID3 &= (PD6 = 1) \text{ AND } (PD3 \text{ OR } PD2) \\ ID2 &= (PD6 = 1) \text{ AND } (PD1 \text{ OR } PD0) \\ ID1 &= (PD6 = 0) \text{ AND } (PD3 \text{ OR } PD2) \\ ID0 &= (PD6 = 0) \text{ AND } (PD1 \text{ OR } PD0) \end{aligned}$$

The relationships between the ID code and the peripheral device are given below.

Device name
Old joy stick (2TRIG)
Not defined
New joy stick (3TRIG)
SEGA RESERVED
Not defined
SEGA RESERVED
Not defined
Not defined
Not defined
Not defined
SEGA RESERVED
Not defined
Not defined
Not defined
Not defined
SEGA RESERVED

	ID3	ID2	ID1	ID0	
...	1	1	1	1	(\$F)
...	1	1	1	0	(\$E)
...	1	1	0	1	(\$D)
...	1	1	0	0	(\$C)
...	1	0	1	1	(\$B)
...	1	0	1	0	(\$A)
...	1	0	0	1	(\$9)
...	1	0	0	0	(\$8)
...	0	1	1	1	(\$7)
...	0	1	1	0	(\$6)
...	0	1	0	1	(\$5)
...	0	1	0	0	(\$4)
...	0	0	1	1	(\$3)
...	0	0	1	0	(\$2)
...	0	0	0	1	(\$1)
...	0	0	0	0	(\$0)

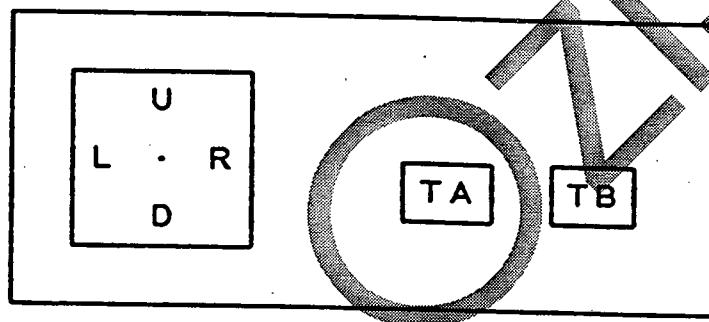
◊ Periphral devices ◊

- ID = \$F : Old joy stick

The standard joy stick of MARK III & HS contains the 4-direction switch and A and B triggers. Each switch is configured as shown below, which is set to 0 when it is pressed.

	CTRL 1	CTRL 2	EXT.
CTRL	\$A10009	\$A1000B	\$A1000D
DATA	\$A10003	\$A10005	\$A10007

	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
CTRL	0	0	0	0	0	0	0	0
DATA	*	*	TB	TA	R	L	D	U

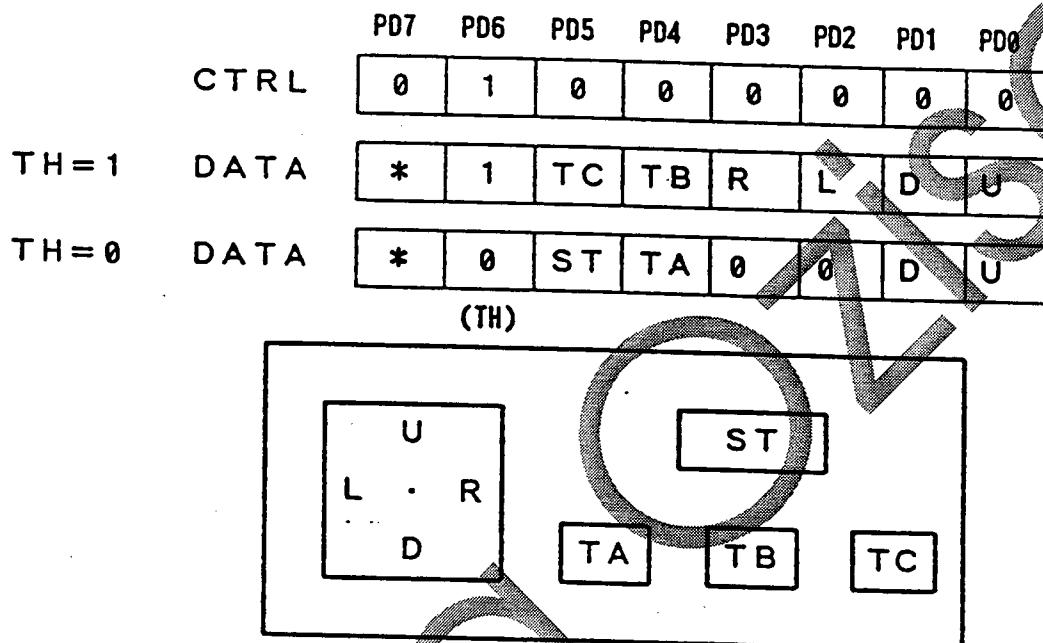


- ID = \$0 : New joy stick

The joy stick of the GENESIS contains the 4-direction switch, A, B and C triggers and Start.

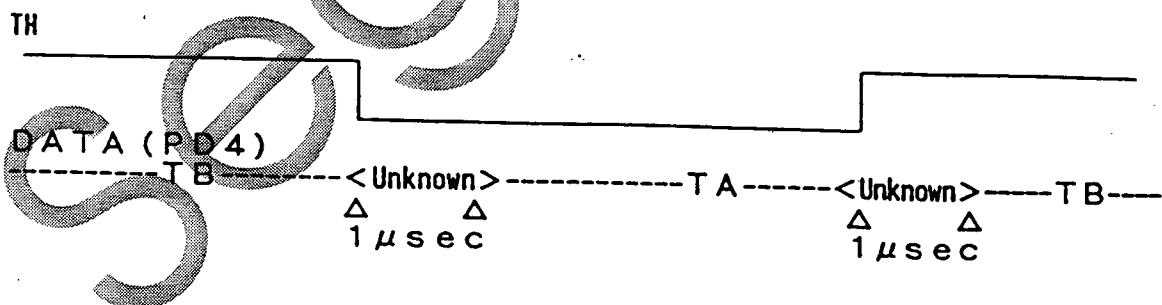
The mode can be changed by setting 0 or 1 after the TH pin is set in the output mode. Each switch is configured as shown below, which is set to 0 when it is pressed.

	CTRL 1	CTRL 2	EXT.
CTRL	\$A10009	\$A1000B	\$A1000D
DATA	\$A10003	\$A10005	\$A10007



It takes about 1μsec from the time the TH is changed until the data is fixed (corresponding to the elapse time of two NOP commands).

Example: The time difference from the time when the TH is changed until the switch value appears at PD4 of DATA.



◊ JOY PAD ◊

Player's button operations are recognized by reading data in \$A10003 and \$A10005 of the I/O addresses via CONTROL1 and CONTROL2. 7 bits of D6 to D0 in the I/O are sent to CONTROL1 and CONTROL2, but there are eight buttons. So, the D6 bit is used as the select bit, and the button operation is read in two steps.

** SAMPLE PROGRAM **

```

MOVE.B #$40,$A10009      ; Enter D5 to D0 of CONTROL1.
MOVE.B #$40,$A10003      ; D6 is set to output (select bit).
NOP                      ; 1 is output to D6 (C, B, right, left, down or up
                           ; is selected).
MOVE.B $A10003,D0        ; D5 to D0 values are read into register D0.
MOVE.B #$00,$A10003      ; 0 is output to D6 (start, A, down or up is
                           ; selected).
NOP
MOVE.B $A10003,D1        ; D5 to D0 values are read into register D1.

```

* Each button outputs 0 when it is pressed.

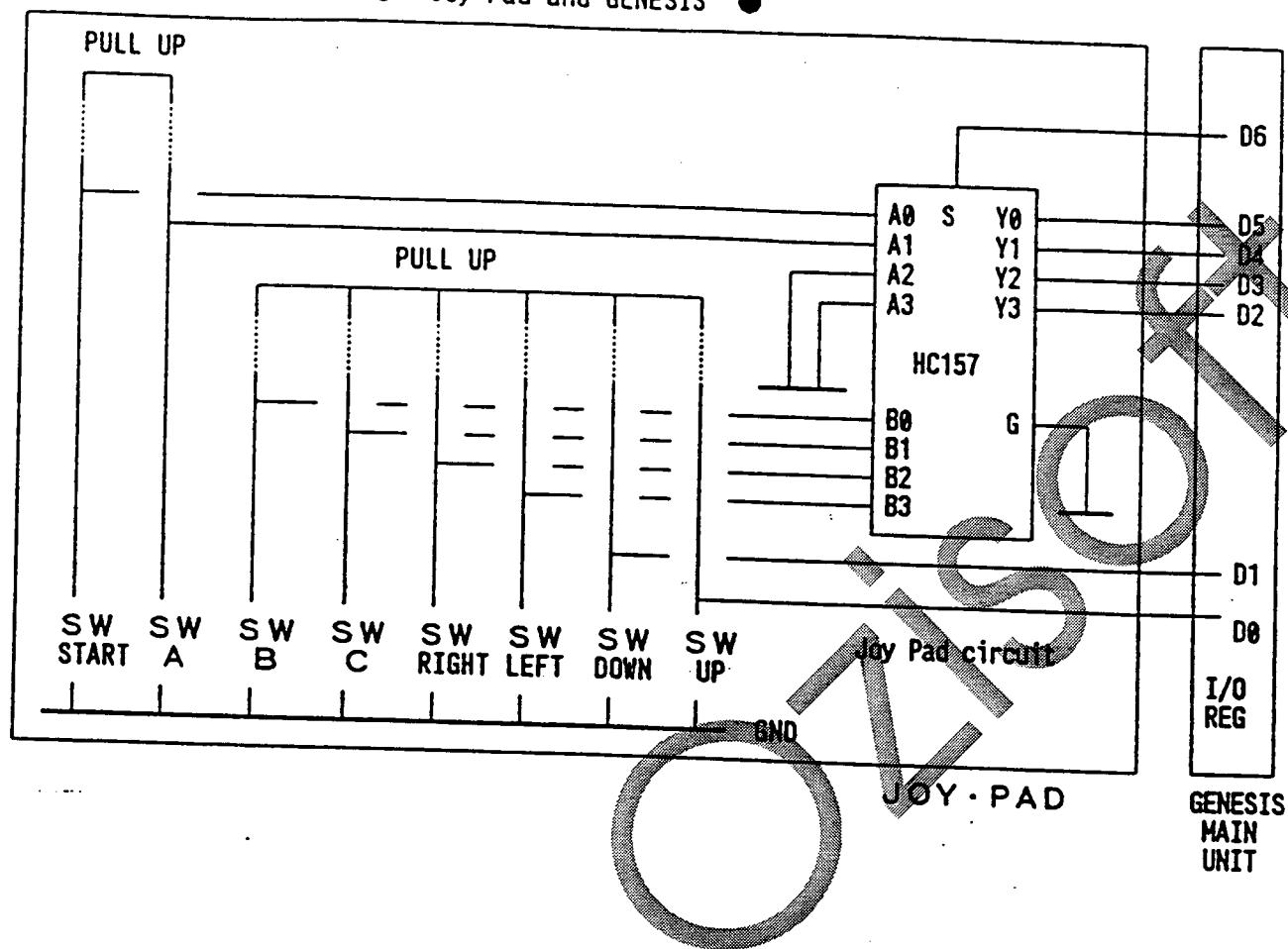
Register values after the program is executed.

DATA REG	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
REGISTER D0	0	1	C bu tt on	B bu tt on	R I G H T	L E F T	D O W N	U P
REGISTER D1	0	0	S T A R T	A bu tt on	0	0	D O W N	U P

HC 157 logic

Input		
S	G	Yx
X	1	-Z-
0	0	Ax
1	0	Bx

● Joy Pad and GENESIS ●



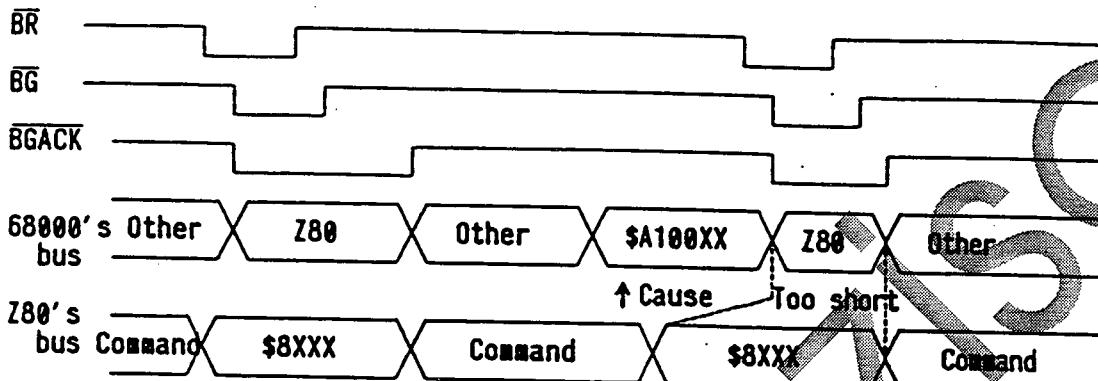
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5.

PRECAUTIONS FOR SOFTWARE DEVELOPMENT

S 1 Z80 CANNOT PROPERLY ACCESS THE BUS ON THE 68000.

When the Z80 tries to enter the bus cycles of the 68000 to read/write a specific address on the 68000, and when the access to \$A100xx is made in the 68000's bus cycle immediately before the bus cycle which the Z80 tries to enter, the cycle of the Z80's entry may become too short to read/write data properly.

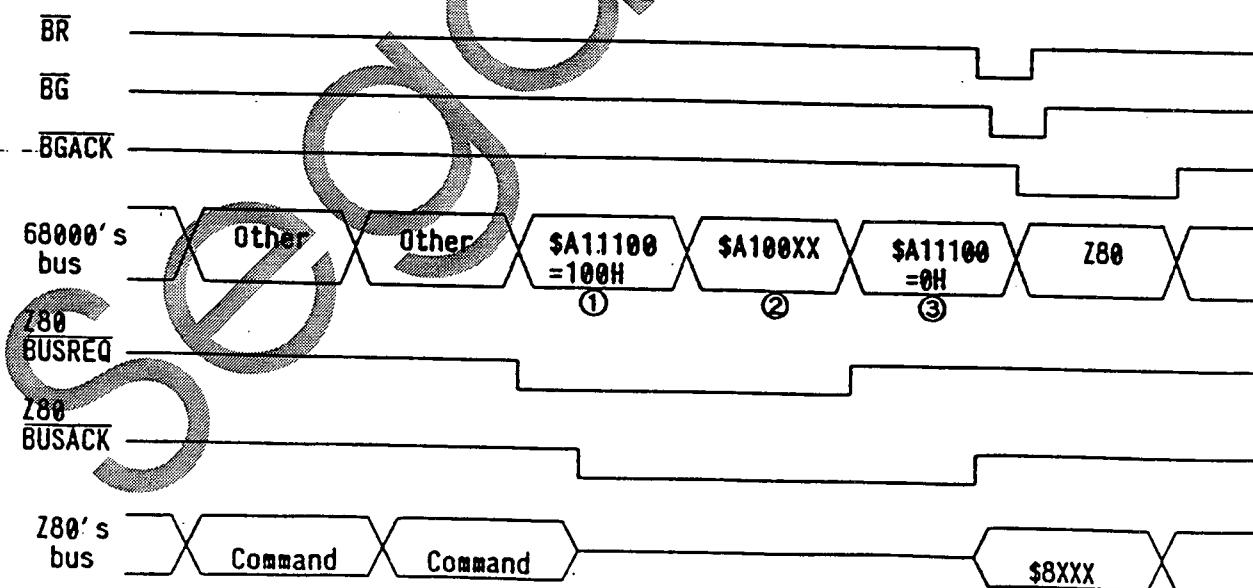


Measure... When the 68000 accesses \$A100xx,

- ① Send BUSREQ to the Z80 (suspend the Z80's bus access... \$A11100 = 0100H)
- ② Access \$A100xx.
- ③ Release the BUSREQ of the Z80 (the Z80 starts the bus access....\$A11100 = 0000H).

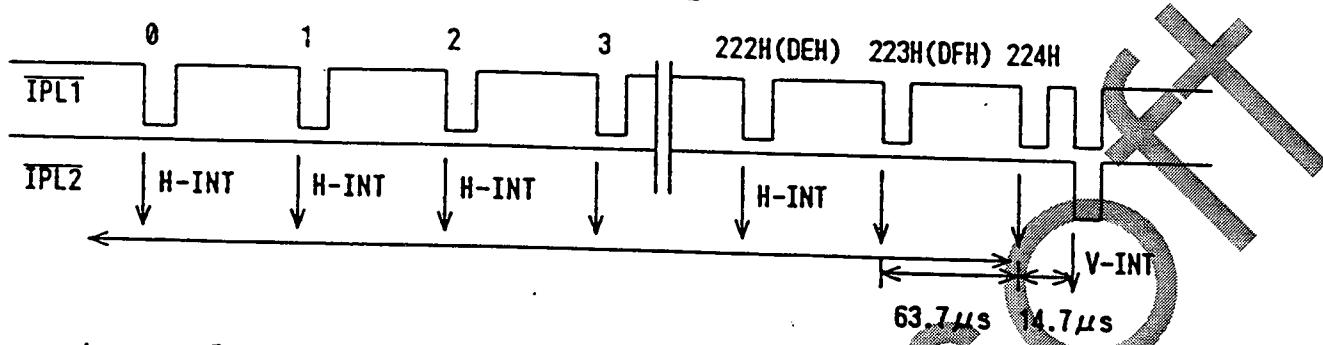
Modify the program to execute the above steps.

Note: it will be no problem if the program is designed to be synchronized with V_INT, etc. to eliminate a bad timing for the bus access.



S 2 H_INT AND V_INT ARE USED IN GENESIS PROGRAMS

- When $IE1 = 1$ and $\#10 = 00H$ are set for VDP register #0, H_INT and V_INT occur at the timings below. Care is required for the timing of H_INT at No.224, in which case, the next V_INT occurs in only $14.7\mu s$. If the receipt of H_INT at No.224 is prolonged and is canceled, H_INT occurs at No.225 instead of V_INT.



Measure A

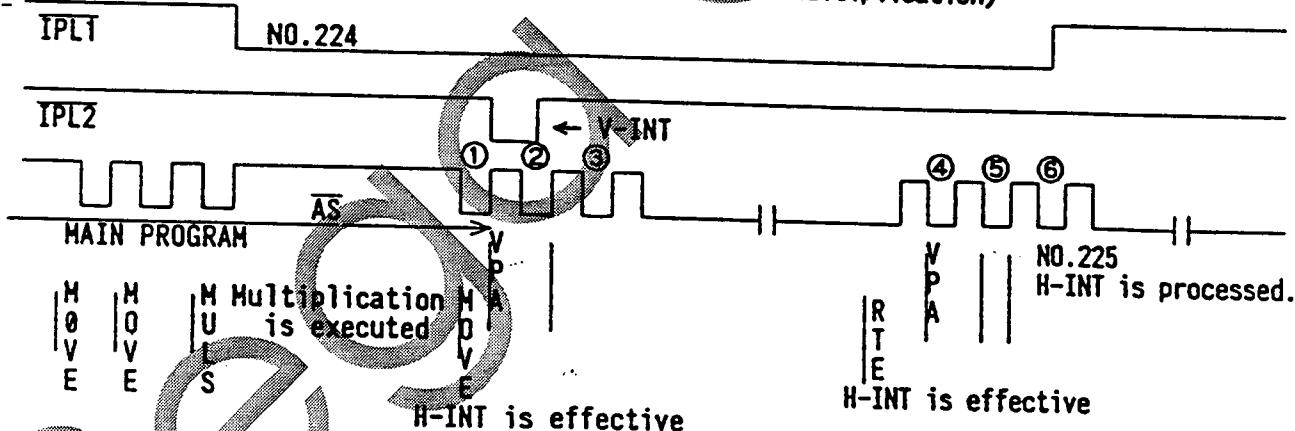
- Before H_INT at No.223 is completed, set $IE0 = 0$ for register #1 to suppress the next occurrence at No.224.
- Before the receipt of V_INT is completed, set $IE0 = 1$ for register #1 to make H_INT effective (No.224 also becomes effective).
- Receive H_INT at No.224.

Measure B

- Before H_INT at No.223 is completed, set SR = 25xx for the 68000 not to receive No.224.
- Before the receipt of V_INT is completed, return SR of the 68000 to the previous value (so that No.224 can be received).
- Receive H_INT at No.224.

*Don't give damages to the flag when you are handling SR.

- The case which was known to cause troubles (due to multiplication)



- After the multiplication, the 68000 decides to receive H_INT by means of MOVE.
- The 68000 generates VPA (INT-ACK). (No.224 is received.) The VDP cannot find the VPA after the H_INT occurrence, and so the H_INT is treated as 'un-processed.' The VPA is received after the occurrence of V_INT. This receipt is assumed that V_INT has been received and the H_INT is preserved.
- Since H_INT at No.224 was received in ①, the processing is executed.
- The 68000 decides to receive H_INT again after the H_INT is processed at the occurrence of RTE.
- The 68000 generates VPA (INT-ACK). The VDP assumes that the VPA is the preserved H_INT, and processes it (at No.225).
- H_INT (at No.225) is received in ④, and the process is executed again.

S 3**TROUBLES DUE TO INTERRUPTS DURING COMMUNICATION**

The similar troubles to 'H_INT and V_INT are used' (see section 2) occur in:

- 'H_INT and INT during data communication', and
- 'V_INT and INT during data communication'.

Since 'INT during data communication' occurs asynchronously with V_INT and H_INT, the measures differ from those described in section 2.

Measure for a)

INT and the receive flag are simultaneously set when data communication starts. The receive flag is cleared when received data is read by means of 'INT during data receipt' which does not overlap with H_INT. If it overlaps with H_INT and this H_INT is treated as the second 'INT during data receipt', the receive flag remains cleared. Hence, the proper measure should be selected by using the status of the receive flag to judge whether it is treated as 'INT during data receipt' or 'data receive INT'.

Measure for b)

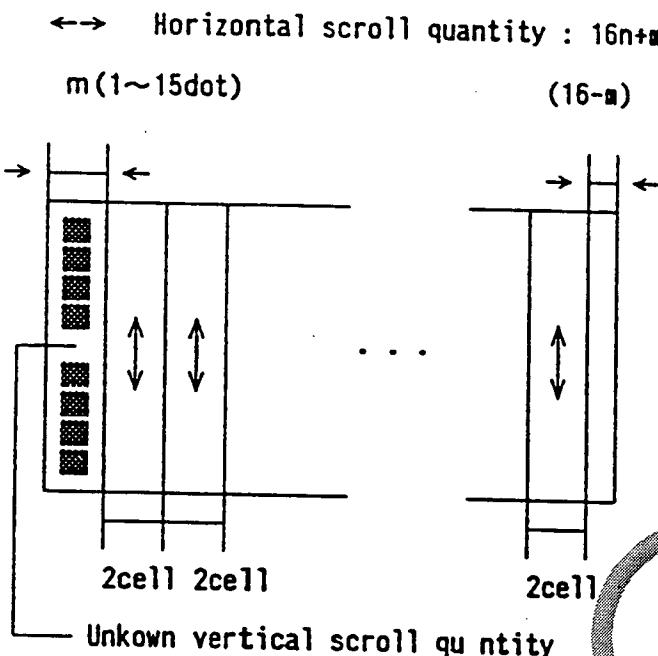
Set the mode in which V_INT does not occur and execute the same treatment as that of V_INT by detecting the V timing using the V_BLK bit for VDP status.

Others

The timing for H_INT or V_INT can be judged by using H_BLK, V_BLK, HV_counter, etc. The receive flag can be used to judge whether 'INT during data receipt' or 'INT during data receipt as which H or V is treated' occurs. Other items and measures should be judged by combining IE0, IE1 and IE2 in the VDP registers, etc.

S 4 PRECAUTIONS WHEN THE CONTROL A AND B SCREENS ARE USED

When vertical 2-cell-unit scroll and horizontal scroll are used together, remember that up to 15 dots at the left of the screen cannot be vertically scrolled if a number which is not a multiple of 16 (i.e., 1 to 15, 17 to 31, etc.) is assigned for the horizontal scroll quantity.



*When the horizontal scroll quantity = $16n+m$ ($1 \leq m \leq 15$) is set, the vertical scroll quantity becomes unknown in the left n -columns.

*Reason

When the horizontal scroll quantity = $16n+m$ ($1 \leq m \leq 15$) is set on the A or B screen, 21 words need to be secured in the RAM for the vertical scroll setting. But the actual capacity of the RAM is only 20 words.

S 5 OTHER PRECAUTIONS

● Precautions for the main program and Z80 bus requests
Care is required for the following items in the main routine on the 68000 when the Z80 area is accessed.

Main routine

- ① A bus request is sent to the Z80.
- ② An acknowledgement signal is checked.
- ③ The interrupt is achieved.
- ④ A bus request is released within INT.
(for example, for reading the control pad, etc.).
- ⑤ The bus request is released within INT.
- ⑥ Operation returns to the main routine.
- ⑦ The data is written in the Z80 area.
However, the Z80 is usually locked with a bus request, but it has been released in (5).

Hence, the following troubles may occur.

- RAMs of the Z80 may be broken.
- Wrong data may be read when a Z80 bank is accessed.

Measure

The interrupt is set to be disabled before step (1) is executed.

●Precautions for sound access

① Sound stops during game play.

★Cause and measure

When the busy flag of status data of the FM sound source (YM2612) is read,

$(CS, RD, WR, A1, A0) = (0, 0, 1, 0, 1)$

has been set (the address 4001H of the MEGA drive is accessed). However, no provisions are given to the output of the YM2612 under the above conditions. It happens that 'not busy' is set and data is successfully read.

※Measure

When the busy flag of the FM sound is read, any address other than 4000H address in the MEGA drive must not be accessed.

●When the reset button is pressed repeatedly

① Software runs away when the reset button is pressed repeatedly.

★Cause and measure

- Pressing the reset button resets the CPU, but not the VDP.
- When the reset button is pressed while DMA is performed, the VDP continues the DMA.
- If the VDP is performing DMA when the VDP is accessed immediately after resetting, this access is ignored.

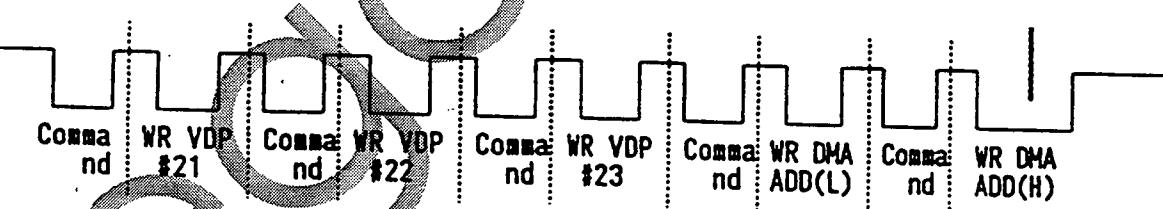
※Measure※

Before accessing the VDP after the initial program (ICD_BLK4), check 'DMA busy' in the status register. If DMA is underway, no access is made.

② The software still runs away in some cases even if the above measure is taken.

★Cause and measure

Such troubles can occur if resetting is made from the time when the parameter set for executing DMA by the CPU is terminated until the first DMA starts.



※Measure※

Although it is very rare for such troubles to occur, take the measure of ① and another appropriate measure of, for example not executing DMA immediately after reset.

BR
BG
BGACK

Trouble occurs if the system is reset during this interval.

● Notes on the control pad and read-programs

The control pad is designed and manufactured in such a way that the up and down signals or the left and right signals are entered simultaneously. However, they can rarely be entered simultaneously, when the internal rubber is aged too much or strong forces exceeding the designed tolerance level are applied. So, design the software not to accept such simultaneous signals.

● Make a revision of the Manual

Regarding the access to VRAM, SRAM, VSRAM, please disregard the statement in the manual that you can implement byte access. You can only implement word access and long-word access.

Make the changes in the manual

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6.

NOTES ON MEGA DRIVE EUROPE VERSION

S 1 PAL

●PAL

- The vertical size is increased by two cells.
- Intervals between interrupts are increased (16msec to 20msec).

●Differences in development of MEGA DRIVE software and precautions.

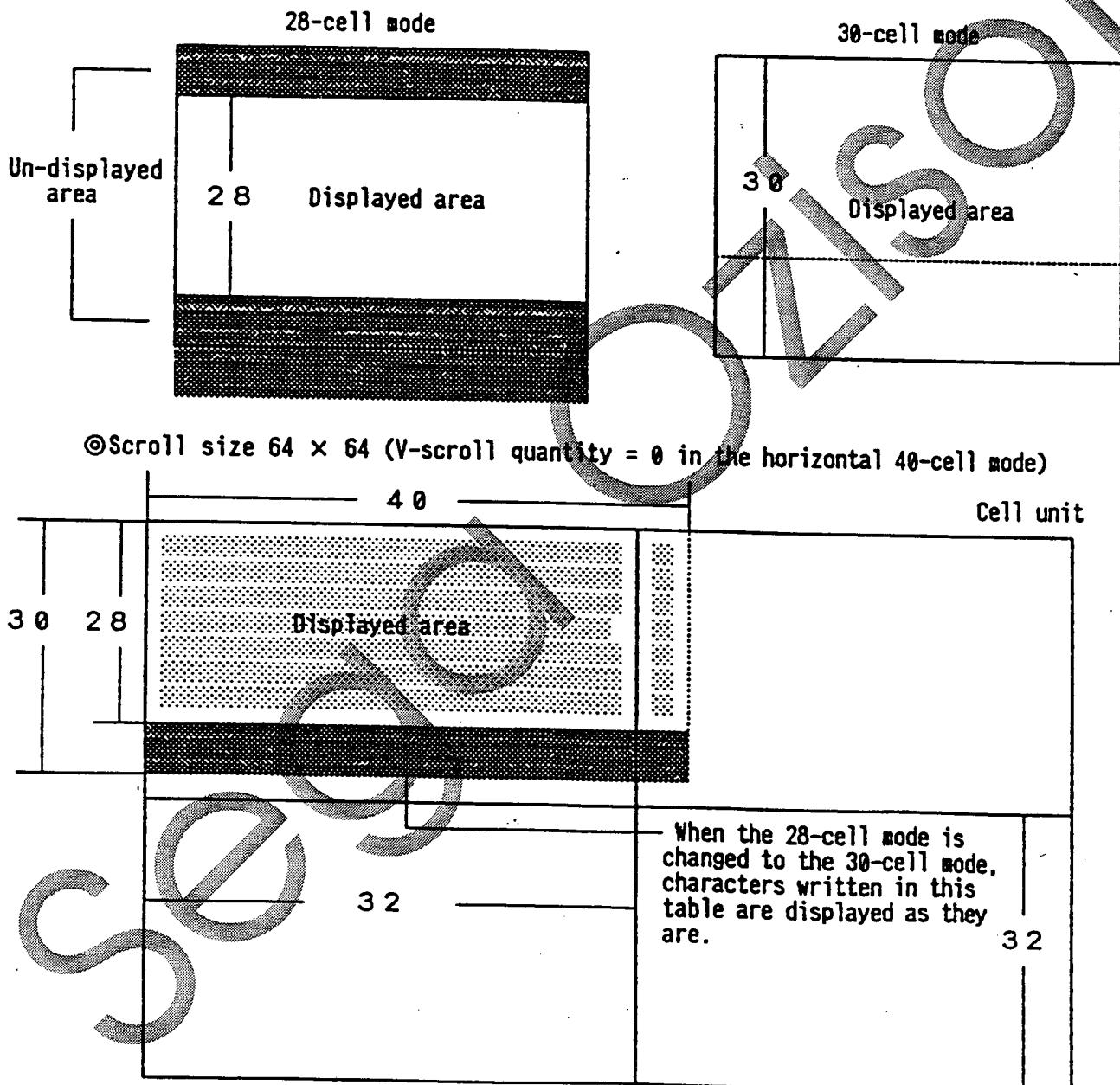
- The vertical 30-cell mode can be used.
- Since the color change appears at the bottom of the screen, wait about 3msec after entering the V-interrupt, and then change the color.
- Since every operation goes slow when synchronized in interrupts, adjust movements and rates so that motions on the screen appear naturally.
- When sounds are produced in synchronization with interrupts, the tempo needs to be increased. The PAL data table is required.
- When sounds are produced by the FM timer, no modifications for NTSC or PAL are required.

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S 2 VERTICAL 30-CELL MODE

- When the vertical 28-cell mode is changed to the vertical 30-cell mode on PAL, the 30-cell mode displays all the cells which have been displayed in the 28-cell mode and the two cells at the bottom which have not been displayed in the 28-cell modes.
- The 28-cell mode does not display one cell each at the top and the bottom; the 30-cell mode displays the entire screen.
- The V-blank period is about 5.6 msec in the 28-cell mode; it is about 4.6 msec (shorter) in the 30-cell mode (approximately same as that on NTSC).
- By developing software in awareness given to the PAL 30-cell mode, the software, which is common to NTSC and PAL and has minimized border part even in the PAL mode, can easily be developed.



When vertical scrolling is performed continuously (e.g., games played with vertical scrolling), it is believed that there will be no problem even if the 28-cell mode is changed to the 30-cell mode.

7.

NOTES ON THE BACKUP RAMs

There are two types of backp RAMs:

- Odd addresses in 200000H~203FFFFH . . 64k bits
- Odd addresses in 200000H~20FFFFH . . 256k bits

The same access methods as those for the work RAMs are used.
However, care is required for the following points.

- Data (initial values) in the backup RAMs is not known when the cartridge (product) is shipped. The initialization must always be executed when the power is turned on. (In many cases, they are cleared to \$FF when shipped from the factory, but this cannot apply for all cases.)
- Data in the backup RAMs may rarely be destroyed. For this reason, the data must always be check and reproduced. Any important data must not be stored in the first word (in the first address) and last word (in the last address), since there is a high possibility that data in these word may destroyed.

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