

CSD19506KTT 80V N-Channel NexFET™ Power MOSFET

1 Features

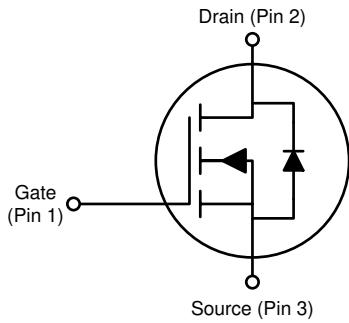
- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating
- RoHS compliant
- Halogen free
- D²PAK plastic package

2 Applications

- Secondary side synchronous rectifier
- Motor control

Description

This 80V, 2.0mΩ, D²PAK (TO-263) NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	80	V
Q_g	Gate Charge Total (10V)	120	nC
Q_{gd}	Gate Charge Gate to Drain	20	nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{V}$	2.2 mΩ
		$V_{GS} = 10\text{V}$	2.0 mΩ
$V_{GS(th)}$	Threshold Voltage	2.5	V

Ordering Information (1)

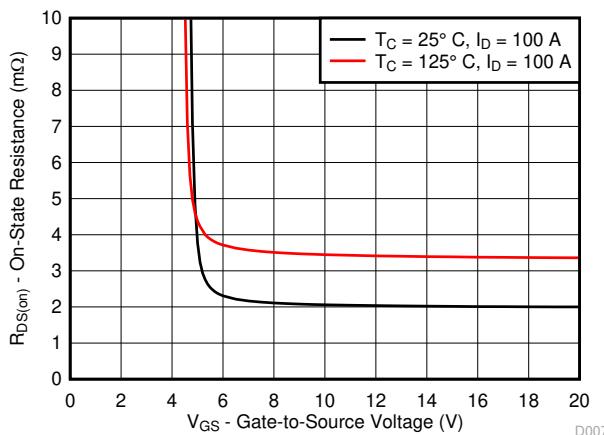
DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD19506KTT	500	13-Inch Reel	D ² PAK Plastic Package	Tape & Reel
CSD19506KTTT	50			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

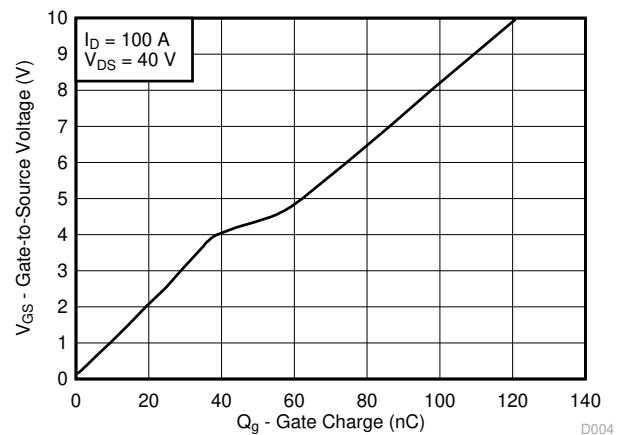
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	80	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current (Package limited)	200	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	291	
	Continuous Drain Current (Silicon limited), $T_C = 100^\circ\text{C}$	206	
I_{DM}	Pulsed Drain Current (1)	400	A
P_D	Power Dissipation	375	W
T_J , T_{stg}	Operating Junction and Storage Temperature Range	-55 to 175	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 129\text{A}$, $L = 0.1\text{mH}$, $R_G = 25\Omega$	832	mJ

(1) Max $R_{eJC} = 0.4^\circ\text{C}/\text{W}$, pulse duration $\leq 100\mu\text{s}$, duty cycle $\leq 1\%$



R_{DS(on)} vs V_{GS}



Gate Charge



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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3 Specifications

3.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS					
BV_{DSS}	Drain-to-source voltage $V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	80			V
I_{DSS}	Drain-to-source leakage current $V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 64\text{V}$			1	μA
I_{GSS}	Gate-to-source leakage current $V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = 20\text{V}$			100	nA
$V_{\text{GS}(\text{th})}$	Gate-to-source threshold voltage $V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	2.1	2.5	3.2	V
$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 6\text{V}, I_D = 100\text{A}$	2.2	2.8		$\text{m}\Omega$
	$V_{\text{GS}} = 10\text{V}, I_D = 100\text{A}$	2.0	2.3		$\text{m}\Omega$
g_{fs}	Transconductance $V_{\text{DS}} = 8\text{V}, I_D = 100\text{A}$	297			S
DYNAMIC CHARACTERISTICS					
C_{iss}	Input capacitance	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 40\text{V}, f = 1\text{MHz}$	9380	12200	pF
C_{oss}	Output capacitance		2260	2940	pF
C_{rss}	Reverse transfer capacitance		42	55	pF
R_G	Series gate resistance		1.3	2.6	Ω
Q_g	Gate charge total (10V)	$V_{\text{DS}} = 40\text{V}, I_D = 100\text{A}$	120	156	nC
Q_{gd}	Gate charge gate-to-drain		20		nC
Q_{gs}	Gate charge gate-to-source		37		nC
$Q_{\text{g}(\text{th})}$	Gate charge at V_{th}		25		nC
Q_{oss}	Output charge	$V_{\text{DS}} = 40\text{V}, V_{\text{GS}} = 0\text{V}$	345		nC
$t_{\text{d}(\text{on})}$	Turn on delay time	$V_{\text{DS}} = 40\text{V}, V_{\text{GS}} = 10\text{V}, I_{\text{DS}} = 100\text{A}, R_G = 0\Omega$	14		ns
t_r	Rise time		7		ns
$t_{\text{d}(\text{off})}$	Turn off delay time		30		ns
t_f	Fall time		5		ns
DIODE CHARACTERISTICS					
V_{SD}	Diode forward voltage	$I_{\text{SD}} = 100\text{A}, V_{\text{GS}} = 0\text{V}$	0.9	1.1	V
Q_{rr}	Reverse recovery charge	$V_{\text{DS}} = 40\text{V}, I_F = 100\text{A}, \frac{di}{dt} = 300\text{A}/\mu\text{s}$	525		nC
t_{rr}	Reverse recovery time		107		ns

3.2 Thermal Information

($T_A = 25^\circ\text{C}$ unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta,\text{JC}}$	Junction-to-case thermal resistance			0.4	$^\circ\text{C/W}$
$R_{\theta,\text{JA}}$	Junction-to-ambient thermal resistance			62	$^\circ\text{C/W}$

3.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

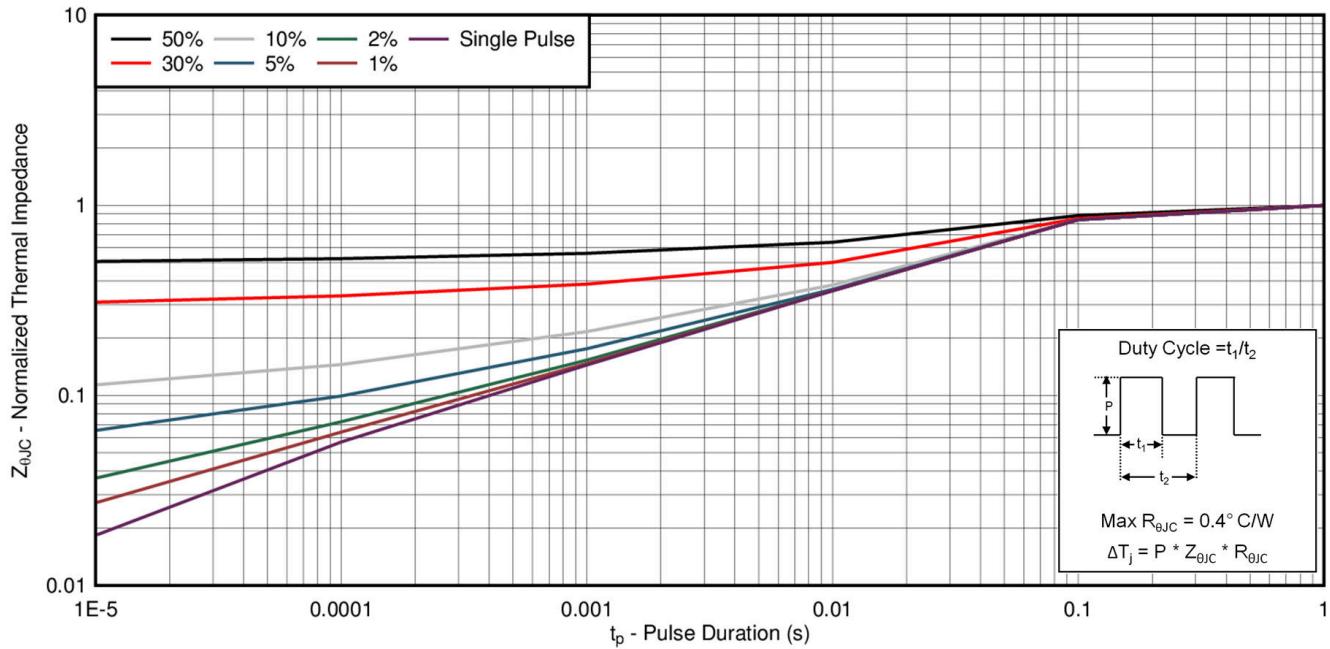


Figure 3-1. Transient Thermal Impedance

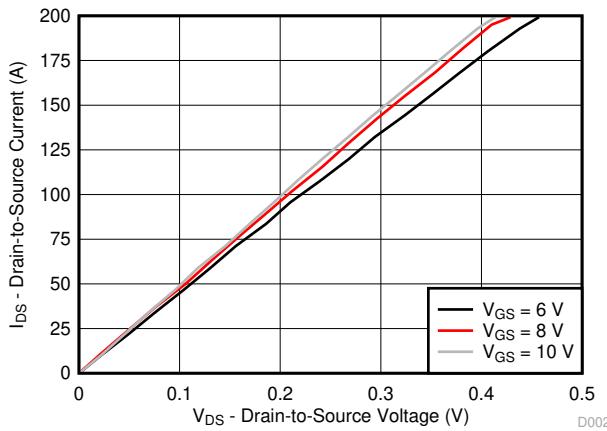


Figure 3-2. Saturation Characteristics

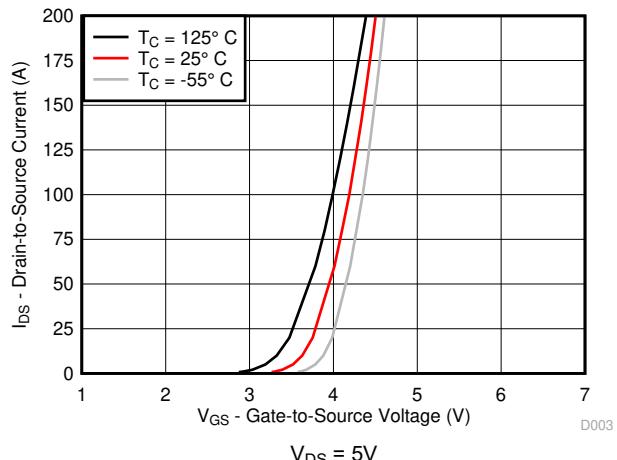


Figure 3-3. Transfer Characteristics

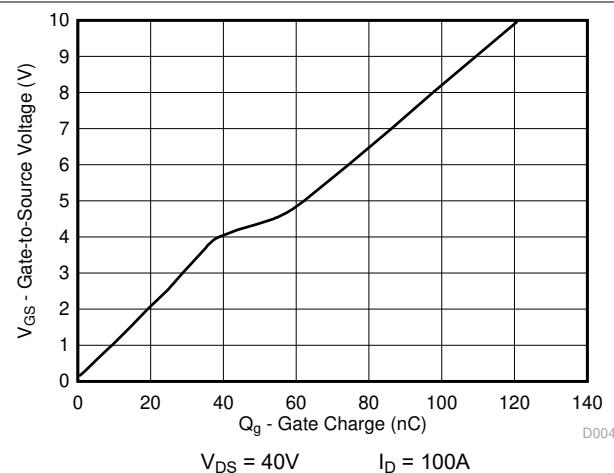


Figure 3-4. Gate Charge

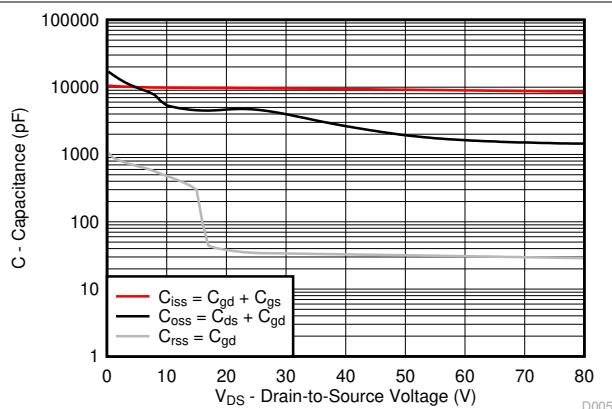


Figure 3-5. Capacitance

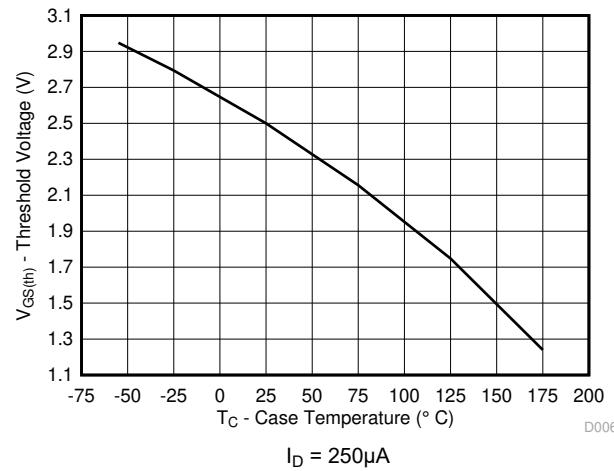


Figure 3-6. Threshold Voltage vs Temperature

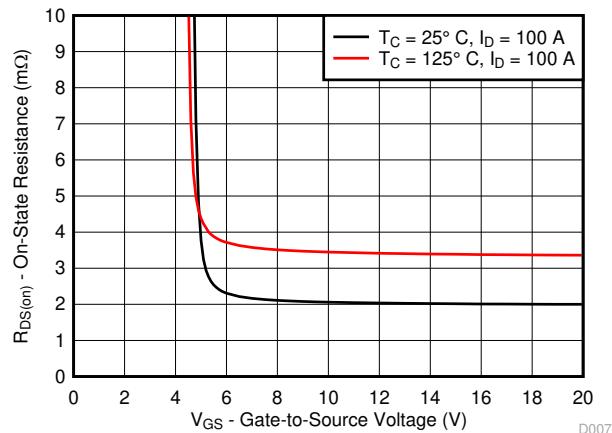


Figure 3-7. On-State Resistance vs Gate-To-Source Voltage

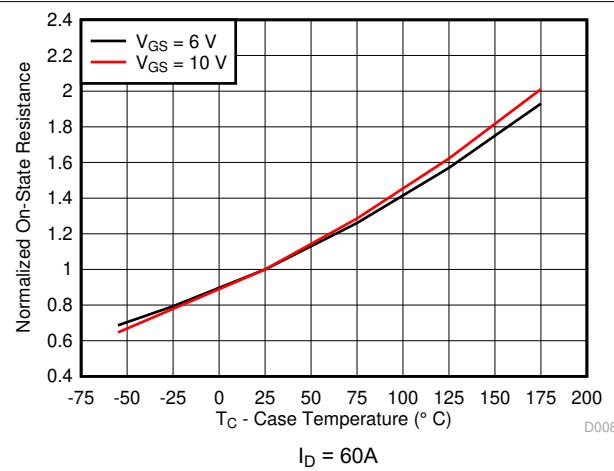


Figure 3-8. Normalized On-State Resistance vs Temperature

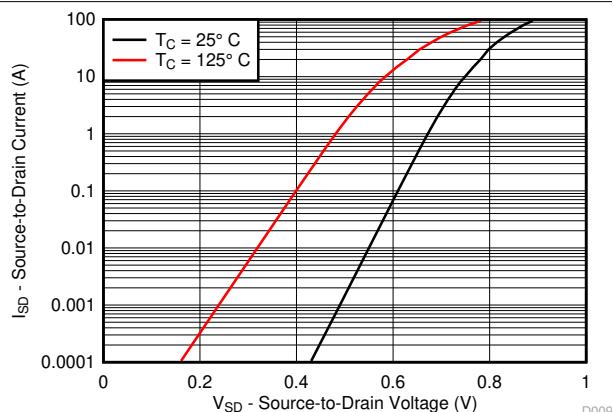
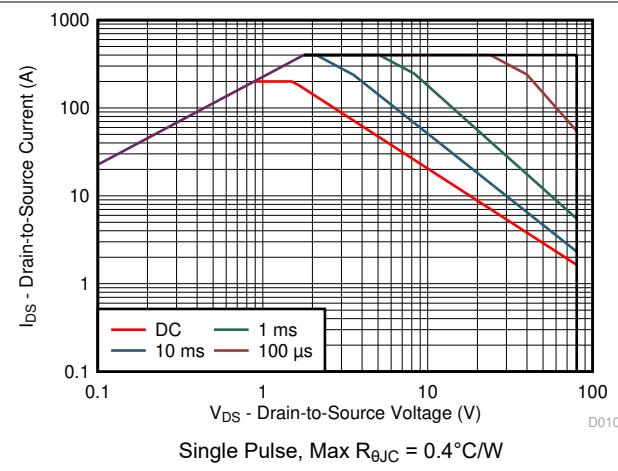
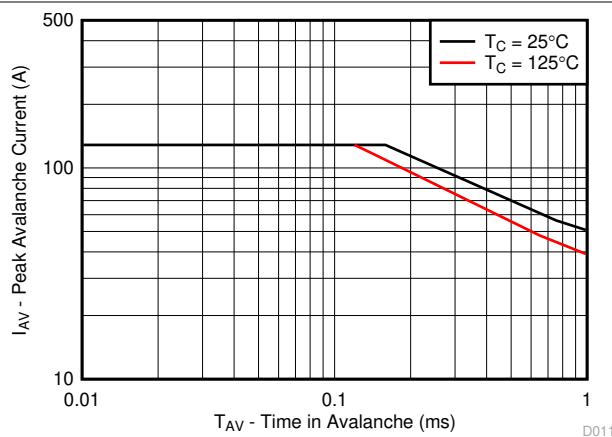
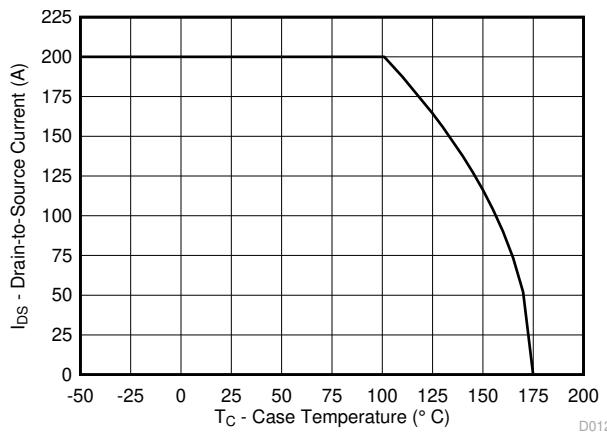


Figure 3-9. Typical Diode Forward Voltage

**Figure 3-10. Maximum Safe Operating Area****Figure 3-11. Single Pulse Unclamped Inductive Switching****Figure 3-12. Maximum Drain Current vs Temperature**

4 Device and Documentation Support

4.1 Third-Party Products Disclaimer

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4.2 Documentation Support

4.2.1 Related Documentation

4.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.5 Trademarks

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TI E2E™ are trademarks of Texas Instruments.

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4.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

Changes from Revision * (March 2016) to Revision A (June 2025)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CSD19506KTT	Active	Production	DDPAK/ TO-263 (KTT) 2	500 LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19506KTT
CSD19506KTT.B	Active	Production	DDPAK/ TO-263 (KTT) 2	500 LARGE T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19506KTT
CSD19506KTTT	Active	Production	DDPAK/ TO-263 (KTT) 2	50 SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19506KTT
CSD19506KTTT.B	Active	Production	DDPAK/ TO-263 (KTT) 2	50 SMALL T&R	ROHS Exempt	SN	Level-2-260C-1 YEAR	-55 to 175	CSD19506KTT

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

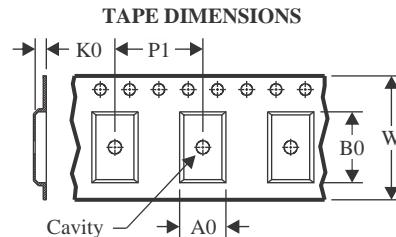
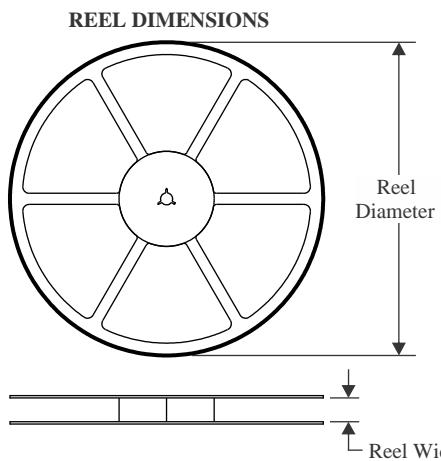
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a " ~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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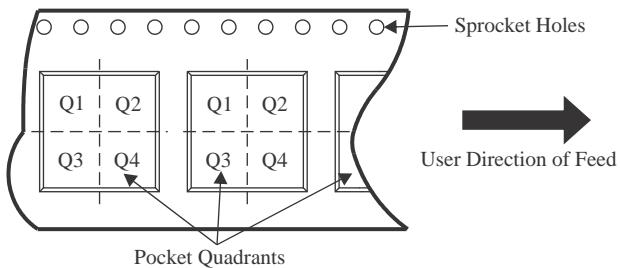
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



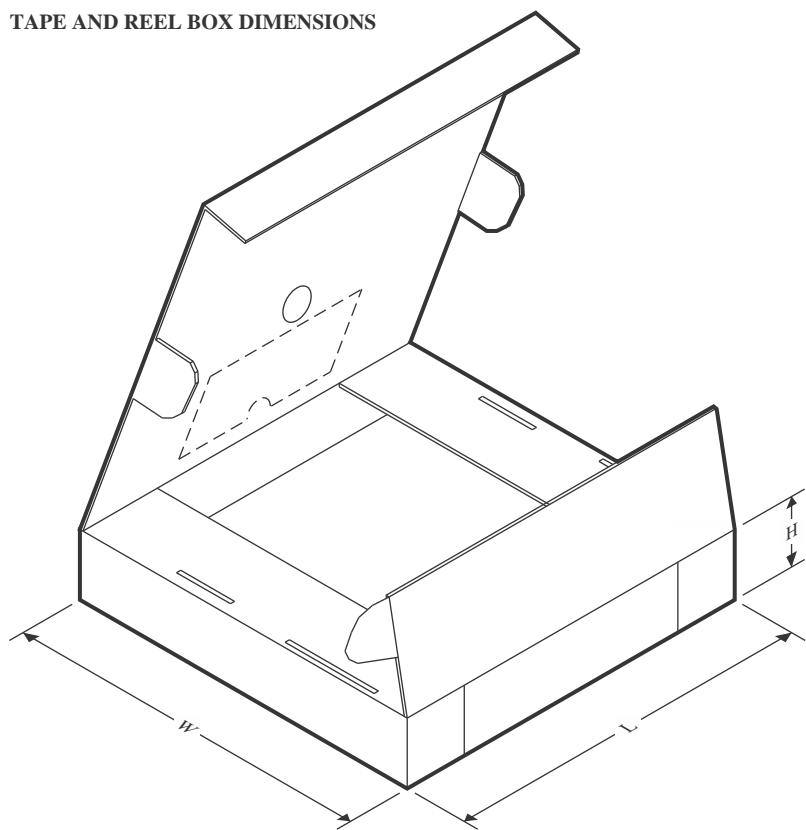
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD19506KTT	DDPAK/ TO-263	KTT	2	500	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2
CSD19506KTTT	DDPAK/ TO-263	KTT	2	50	330.0	24.4	10.8	16.3	5.11	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD19506KTT	DDPAK/TO-263	KTT	2	500	340.0	340.0	38.0
CSD19506KTTT	DDPAK/TO-263	KTT	2	50	340.0	340.0	38.0

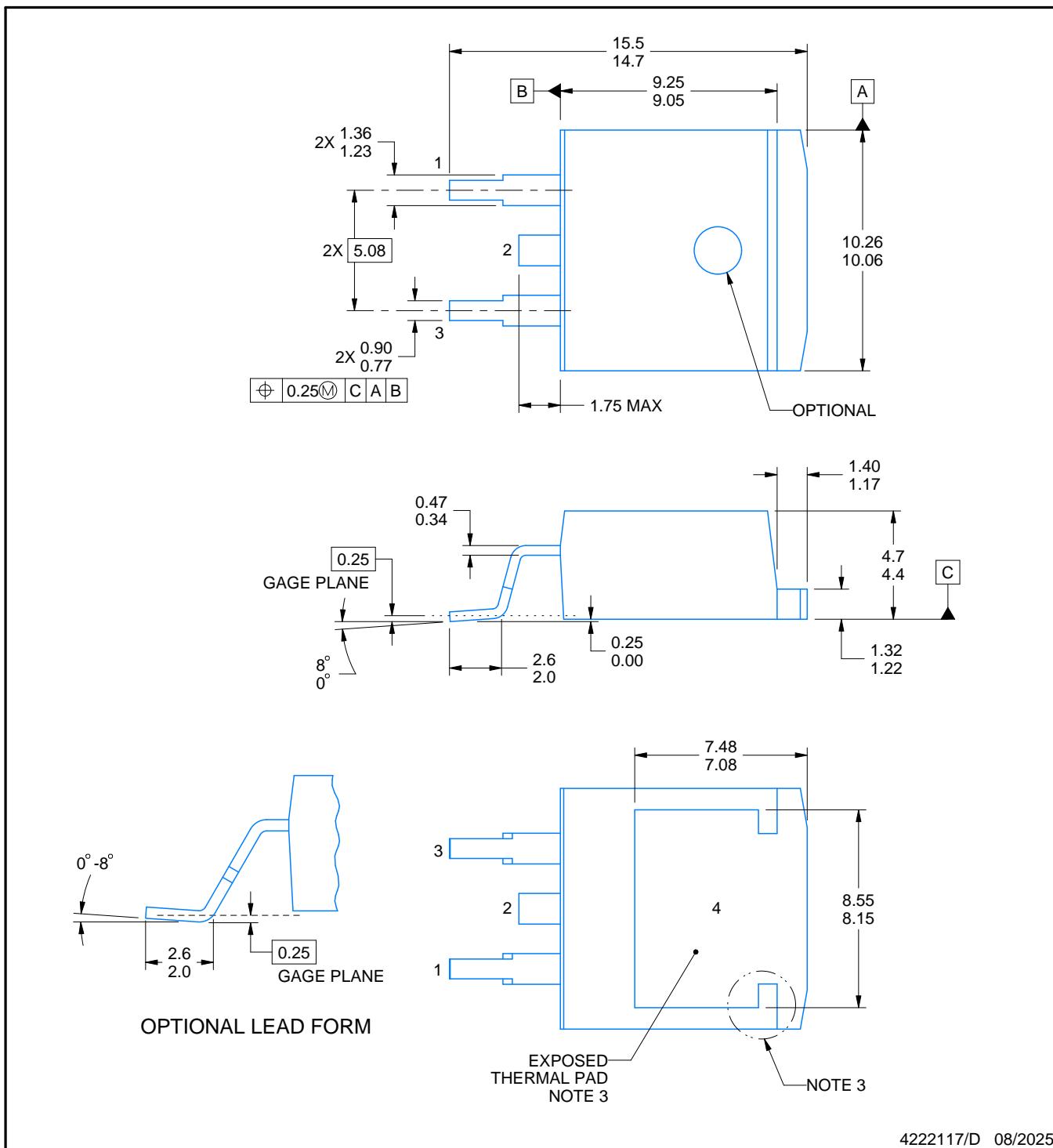
PACKAGE OUTLINE

KTT0002A



TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE



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NOTES:

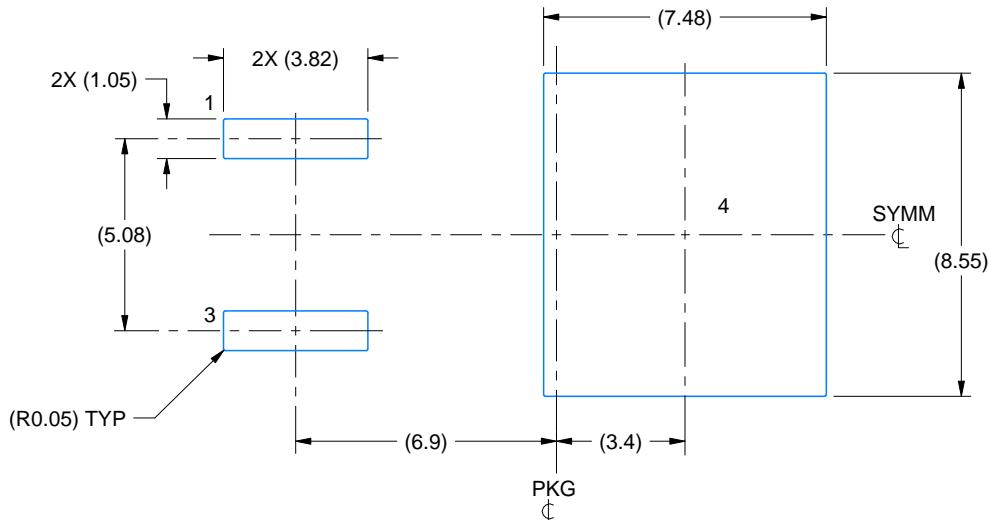
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Features may not exist and shape may vary per different assembly sites. Pin 2 and Pin 4 connected.
- Reference JEDEC registration TO-263.

EXAMPLE BOARD LAYOUT

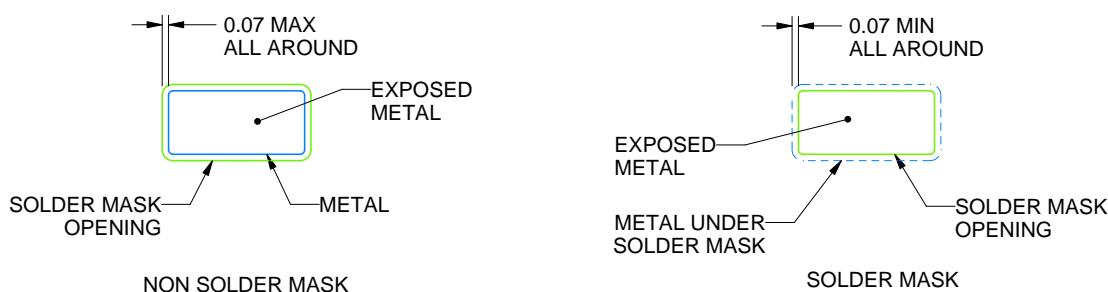
KTT0002A

TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X



SOLDER MASK DETAILS

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NOTES: (continued)

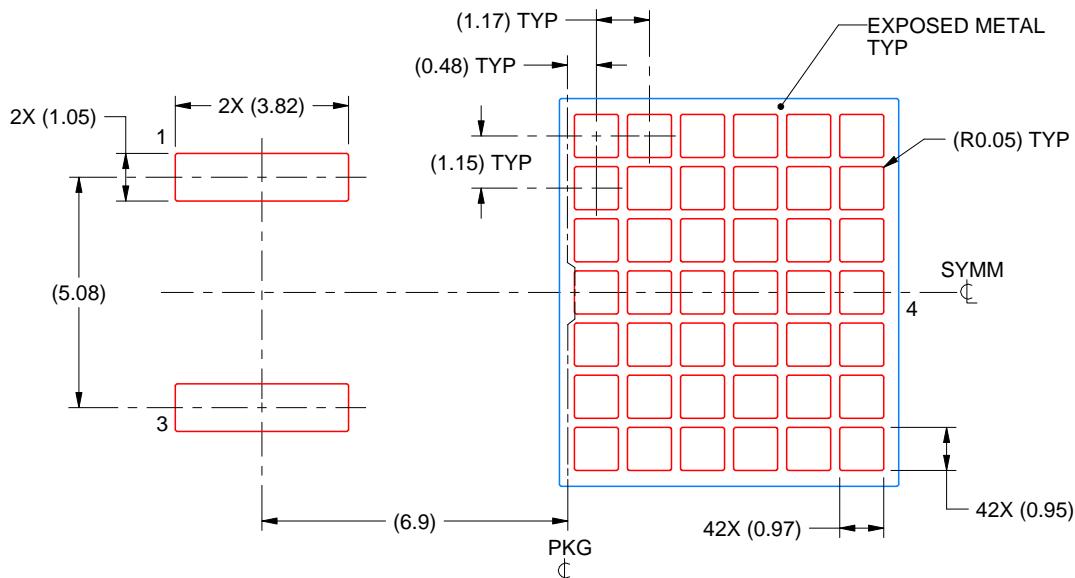
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002(www.ti.com/lit/slm002) and SLMA004 (www.ti.com/lit/slma004).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

KTT0002A

TO-263 - 4.7 mm max height

TRANSISTOR OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
60.5% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

4222117/D 08/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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