

LMP7704-SP Radiation Hardness Assured (RHA), Precision, Low Input Bias, RRIO, Wide Supply Range Amplifiers

1 Features

- QML Class V (QMLV), RHA, SMD [5962-19206](#)
- Radiation performance
 - RHA up to TID = 100 krad(Si)
 - ELDRS-free up to TID = 100 krad(Si)
 - SEL immune to LET = 85 MeV·cm²/mg
 - SEE characterized to LET = 85 MeV·cm²/mg
- Ultra-low input bias current: ±200 fA
- Input offset voltage: ±37 µV
- Unity-gain bandwidth: 2.5 MHz
- Supply voltage range: 2.7 V to 12 V
- Rail-to-rail input and output
- Military temperature range: –55°C to +125°C
- Available in 14-lead CFP with industry-standard quad amp pinout

2 Applications

- Satellite health monitoring and telemetry
- Scientific exploration payload
- Altitude and orbit control system (AOCS)
- [Satellite electrical power system \(EPS\)](#)
- [Communications payload](#)
- [Radar imaging payload](#)

3 Description

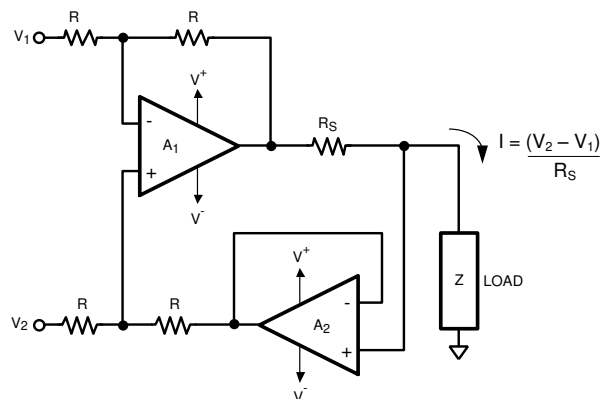
The LMP7704-SP is a precision amplifier with low input bias, low offset voltage, 2.5-MHz gain bandwidth product, and a wide supply voltage. The device is radiation hardened and operates in the military temperature range of –55°C to +125°C.

The high dc precision of this amplifier, specifically the low offset voltage of ±37 µV and ultra-low input bias of ±200 fA, make this device an excellent choice for interfacing with precision sensors with high output impedances. This amplifier can be configured for transducer, bridge, strain gauge, and transduce amplification.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
5962-1920601VXC, Flight Model (QMLV)	CFP (14)	9.73 mm x 6.47 mm
5962R1920601VXC, Flight Model (QMLV), RHA to 100-krad		
LMP7704HBH/EM, Engineering Model ⁽²⁾		

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) These units are intended for engineering evaluation only. They are processed to a noncompliant flow (that is, no burn-in, and so forth) and are tested to a temperature rating of 25°C only. These units are not suitable for qualification, production, radiation testing, or flight use. Parts are not warranted for performance over the full MIL specified temperature range of –55°C to +125°C or operating life. For more information about engineering models, see the [Texas Instruments Engineering Evaluation Units versus MIL-PRF-38535 QML Class V Processing overview](#).



Typical Application Schematic



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4 Revision History

Changes from Revision * (December 2020) to Revision A (January 2021)	Page
• Changed radiation performance <i>Features</i> bullets.....	1
• Changed pin count from (16) to (14) in <i>Device Information</i> table.....	1
• Deleted 2 redundant rows from the Pin Functions table.....	3
• Added superscripts to clarify certain values in <i>Radiation Hardened Performance</i> section.....	17

5 Pin Configuration and Functions

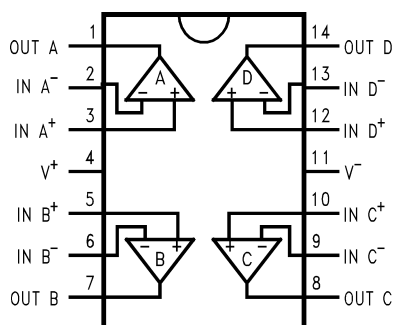


Figure 5-1. HBH Package, 14-Pin CFP, Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
IN A ⁺	3	I	Noninverting input for amplifier A
IN A ⁻	2	I	Inverting input for amplifier A
IN B ⁺	5	I	Noninverting input for amplifier B
IN B ⁻	6	I	Inverting input for amplifier B
IN C ⁺	10	I	Noninverting input for amplifier C
IN C ⁻	9	I	Inverting input for amplifier C
IN D ⁺	12	I	Noninverting input for amplifier D
IN D ⁻	13	I	Inverting input for amplifier D
OUT A	1	O	Output for amplifier A
OUT B	7	O	Output for amplifier B
OUT C	8	O	Output for amplifier C
OUT D	14	O	Output for amplifier D
V ⁺	4	P	Positive supply
V ⁻	11	P	Negative supply
LID	—	—	The metal lid is internally connected to V ⁻

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _S	Supply voltage, V _S = (V ₊) – (V _–)		13.2	V
	Voltage	Common-mode	(V _–) – 0.3	V
		Differential	(V ₊) + 0.3	
	Current		(V ₊) – (V _–) + 0.3	
			±10	mA
	Output short circuit ⁽²⁾	Continuous	Continuous	
T _A	Operating temperature	–55	150	°C
T _J	Junction temperature		150	°C
T _{STG}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _S	Supply voltage, V _S = (V ₊) – (V _–)	2.7		12	V
T _A	Specified temperature	–55		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMP7704-SP	UNIT
		HBH (CFP)	
		14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	37.5	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	20.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	21.3	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	12.9	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	21.0	°C/W
R _{θJC(bot)}	Junction-to-case(bottom) thermal resistance	10.8	N/A

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics: $V_S = 5\text{ V}$

at $T_A = +25^\circ\text{C}$, $V_S = (V+) - (V-) = 5\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage			±32	TBD	μV	
		T _A = −55°C to +125°C		TBD			
dV _{OS} /dT	Input offset voltage drift	T _A = −55°C to +125°C		±1	±5	μV/°C	
PSRR	Power-supply rejection ratio	2.7 V < V _S < 12 V		86	100	dB	
			T _A = −55°C to +125°C	82		dB	
INPUT BIAS CURRENT							
I _B	Input bias current			±0.2	TBD	pA	
		T _A = −55°C to +125°C		TBD		pA	
I _{OS}	Input offset current			±40		fA	
NOISE							
e _n	Input voltage noise density	f = 1 kHz		9		nV/√Hz	
i _n	Input current noise density	f = 100 kHz		1		fA/√Hz	
INPUT VOLTAGE							
V _{CM}	Common-mode voltage range	T _A = −55°C to +125°C		(V−) − 0.2	(V+) + 0.2	V	
CMRR	Common-mode rejection ratio	(V−) < V _{CM} < (V+)		86	130	dB	
			T _A = −55°C to +125°C	81			
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	(V−) + 0.3 V < V _{OUT} < (V+) − 0.3 V, R _L = 2 kΩ		100	119	dB	
			T _A = −55°C to +125°C	94			
		(V−) + 0.2 V < V _{OUT} < (V+) − 0.2 V, R _L = 10 kΩ		100	130		
			T _A = −55°C to +125°C	96			
FREQUENCY RESPONSE							
GBW	Gain bandwidth			TBD	2.5	MHz	
SR	Slew rate	G = 1, 4-V step	10% to 90% rising	1		V/μs	
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, R _L = 10 kΩ		0.02%			

6.5 Electrical Characteristics: $V_S = 5\text{ V}$ (continued)

at $T_A = +25^\circ\text{C}$, $V_S = (V+) - (V-) = 5\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V _O	Voltage output swing from rail	Positive rail	R _L = 2 kΩ to V _S / 2		60	120	mV
			R _L = 2 kΩ to V _S / 2, T _A = −55°C to +125°C			200	
			R _L = 10 kΩ to V _S / 2		40	60	
			R _L = 10 kΩ to V _S / 2, T _A = −55°C to +125°C			120	
		Negative rail	R _L = 2 kΩ to V _S / 2		50	120	
			R _L = 2 kΩ to V _S / 2, T _A = −55°C to +125°C			190	
			R _L = 10 kΩ to V _S / 2		30	50	
			R _L = 10 kΩ to V _S / 2, T _A = −55°C to +125°C			100	
I _{SC}	Short-circuit current	V _{OUT} = V _S / 2, V _{IN} = ±100 mV		+66 / −76		mA	
POWER SUPPLY							
I _Q	Total quiescent current	I _O = 0 A			2.9	3.7	mA
			T _A = −55°C to +125°C			4.6	

6.6 Electrical Characteristics: $V_S = 10\text{ V}$

at $T_A = +25^\circ\text{C}$, $V_S = (V+) - (V-) = 10\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage			±37		TBD	μV
		T _A = −55°C to +125°C				TBD	
dV _{OS} /dT	Input offset voltage drift	T _A = −55°C to +125°C			±1	±5	μV/°C
PSRR	Power-supply rejection ratio	2.7 V < V _S < 12 V		86	100		dB
			T _A = −55°C to +125°C	82			dB
INPUT BIAS CURRENT							
I _B	Input bias current			±0.2		TBD	pA
		T _A = −55°C to +125°C				TBD	pA
I _{OS}	Input offset current			±40			fA
NOISE							
e _n	Input voltage noise density	f = 1 kHz			9		nV/√Hz
i _n	Input current noise density	f = 100 kHz			1		fA/√Hz
INPUT VOLTAGE							
V _{CM}	Common-mode voltage range			(V−) − 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	(V−) < V _{CM} < (V+)		90	130		dB
			T _A = −55°C to +125°C	86			
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	(V−) + 0.3 V < V _{OUT} < (V+) − 0.3 V, R _L = 2 kΩ		100	121		dB
			T _A = −55°C to +125°C	94			
		(V−) + 0.2 V < V _{OUT} < (V+) − 0.2 V, R _L = 10 kΩ		100	134		
			T _A = −55°C to +125°C	97			
FREQUENCY RESPONSE							
GBW	Gain bandwidth			TBD	2.5	TBD	MHz
SR	Slew rate	G = 1, 9-V step	10% to 90% rising		1.1		V/μs
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, R _L = 10 kΩ			0.02%		

6.6 Electrical Characteristics: $V_S = 10\text{ V}$ (continued)

at $T_A = +25^\circ\text{C}$, $V_S = (V+) - (V-) = 10\text{ V}$, $V_{CM} = V_{OUT} = V_S / 2$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V _O	Voltage output swing from rail	Positive rail	R _L = 2 kΩ to V _S / 2		60	120	mV
			R _L = 2 kΩ to V _S / 2, T _A = −55°C to +125°C			200	
			R _L = 10 kΩ to V _S / 2		40	60	
			R _L = 10 kΩ to V _S / 2, T _A = −55°C to +125°C			120	
		Negative rail	R _L = 2 kΩ to V _S / 2		50	120	
			R _L = 2 kΩ to V _S / 2, T _A = −55°C to +125°C			190	
			R _L = 10 kΩ to V _S / 2		30	50	
			R _L = 10 kΩ to V _S / 2, T _A = −55°C to +125°C			100	
I _{SC}	Short-circuit current	V _{OUT} = V _S / 2, V _{IN} = ±100 mV		+86 / −84		mA	
POWER SUPPLY							
I _Q	Total quiescent current	I _O = 0 A			3.2	4.2	mA
			T _A = −55°C to +125°C			5	

6.7 Typical Characteristics

$T_A = 25^\circ\text{C}$, $V_{CM} = V_S/2$, $R_L > 10\text{ k}\Omega$ (unless otherwise noted)

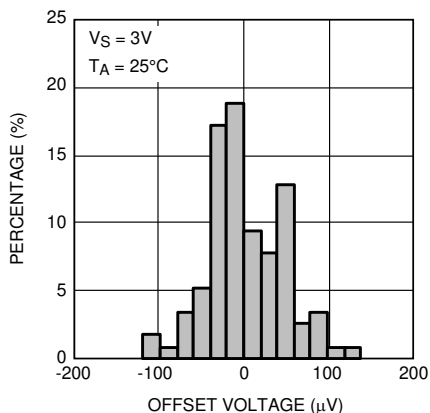


Figure 6-1. Figure 1. Offset Voltage Distribution

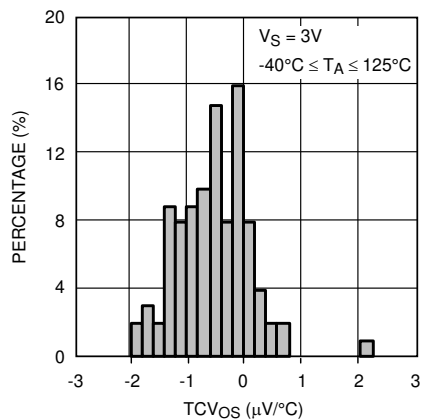


Figure 6-2. TCVOS Distribution

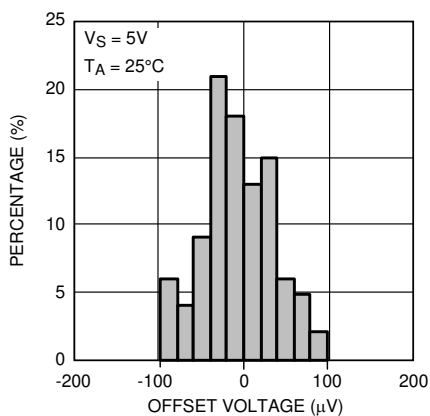


Figure 6-3. Offset Voltage Distribution

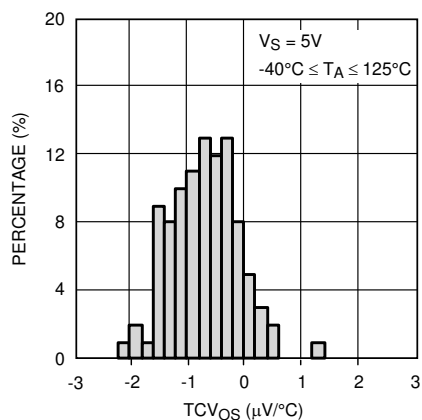


Figure 6-4. TCVOS Distribution

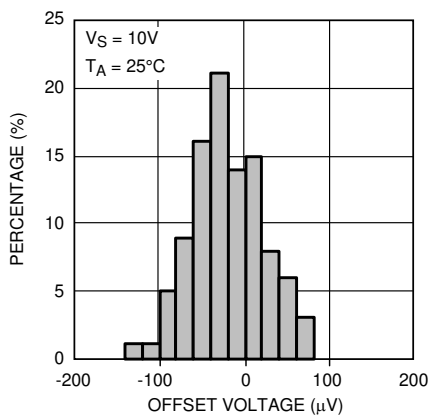


Figure 6-5. Offset Voltage Distribution

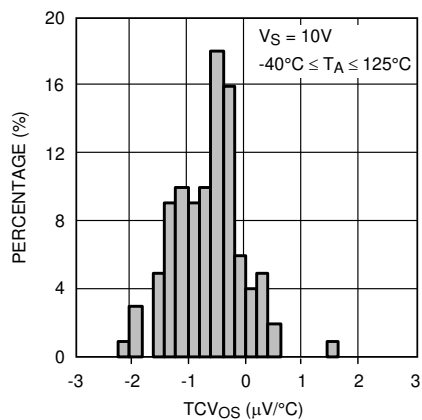


Figure 6-6. TCVOS Distribution

6.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{CM} = V_S/2$, $R_L > 10\text{ k}\Omega$ (unless otherwise noted)

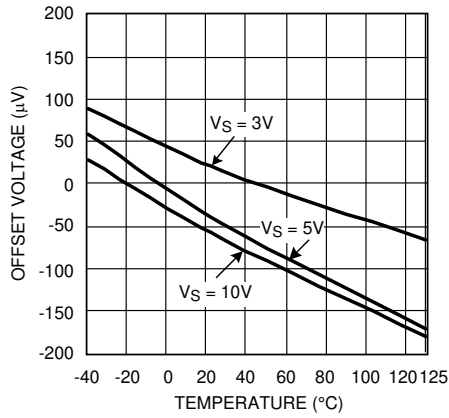


Figure 6-7. Offset Voltage vs Temperature

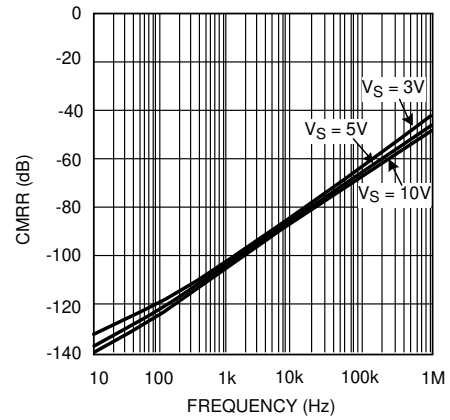


Figure 6-8. CMRR vs Frequency

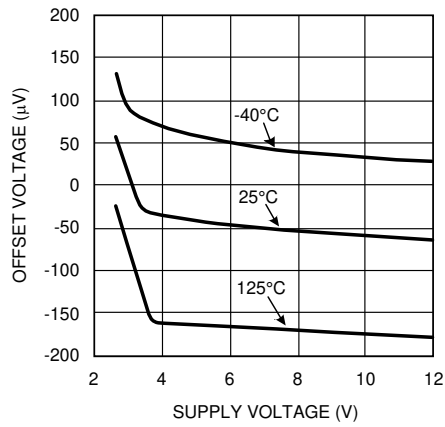


Figure 6-9. Offset Voltage vs Supply Voltage

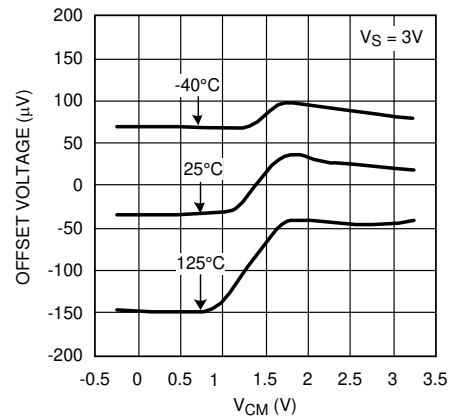


Figure 6-10. Offset Voltage vs V_{CM}

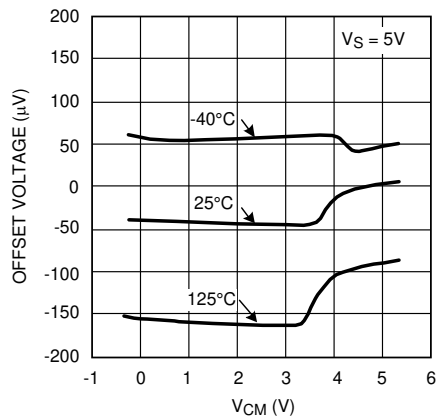


Figure 6-11. Offset Voltage vs V_{CM}

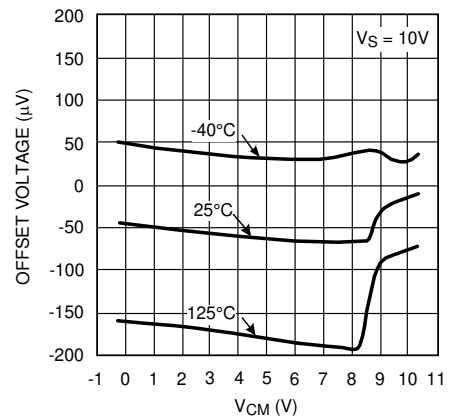


Figure 6-12. Offset Voltage vs V_{CM}

6.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{CM} = V_S/2$, $R_L > 10\text{ k}\Omega$ (unless otherwise noted)

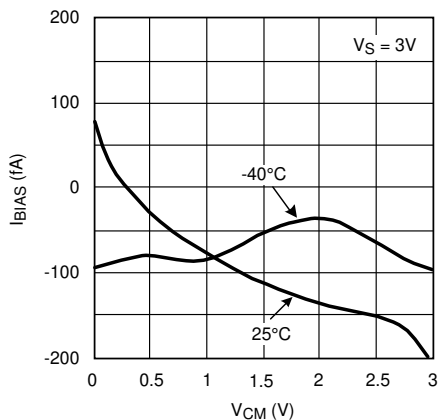


Figure 6-13. Input Bias Current vs V_{CM}

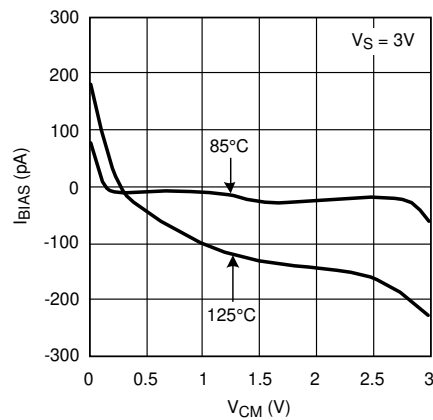


Figure 6-14. Input Bias Current vs V_{CM}

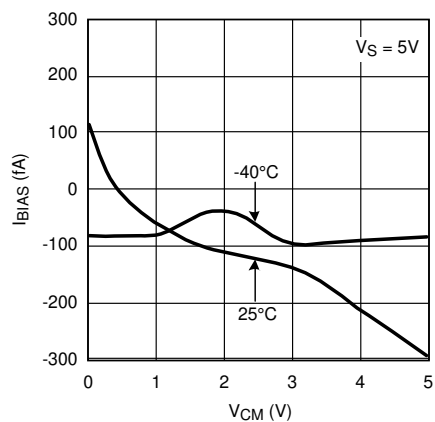


Figure 6-15. Input Bias Current vs V_{CM}

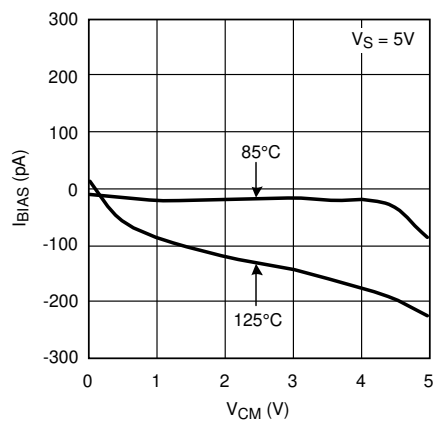


Figure 6-16. Input Bias Current vs V_{CM}

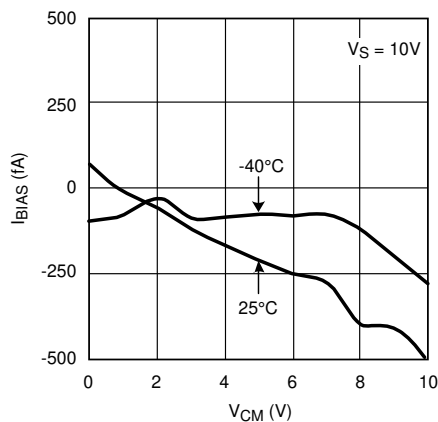


Figure 6-17. Input Bias Current vs V_{CM}

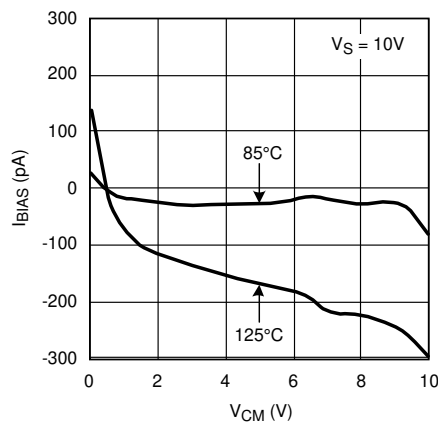


Figure 6-18. Input Bias Current vs V_{CM}

6.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{CM} = V_S/2$, $R_L > 10\text{ k}\Omega$ (unless otherwise noted)

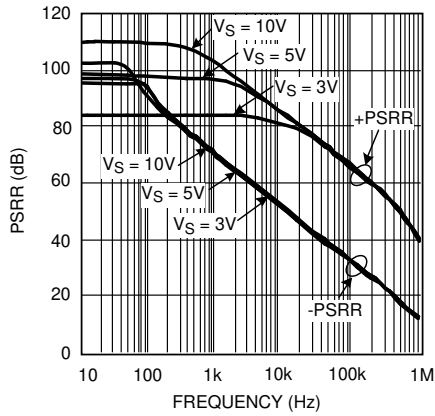


Figure 6-19. PSRR vs Frequency

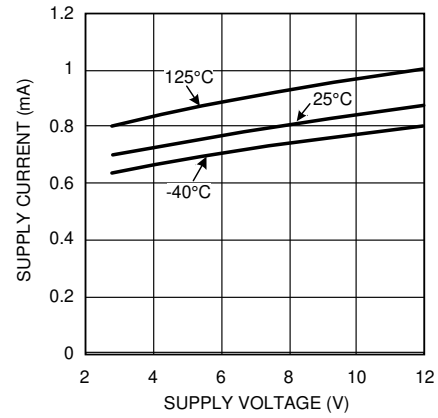


Figure 6-20. Supply Current vs Supply Voltage (Per Channel)

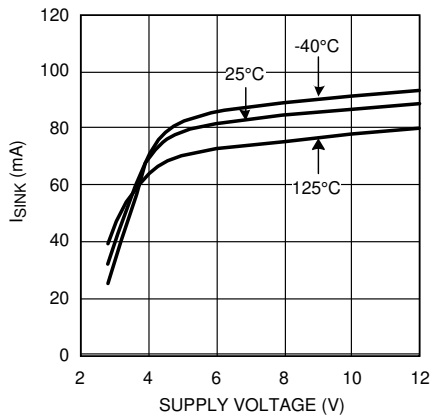


Figure 6-21. Sinking Current vs Supply Voltage

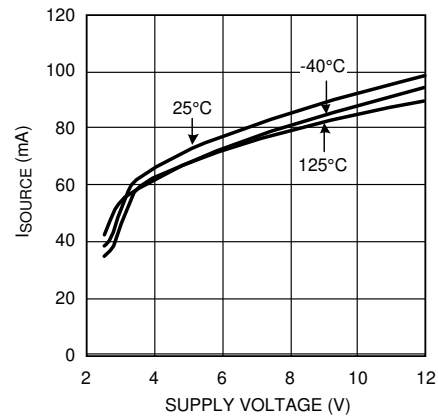


Figure 6-22. Sourcing Current vs Supply Voltage

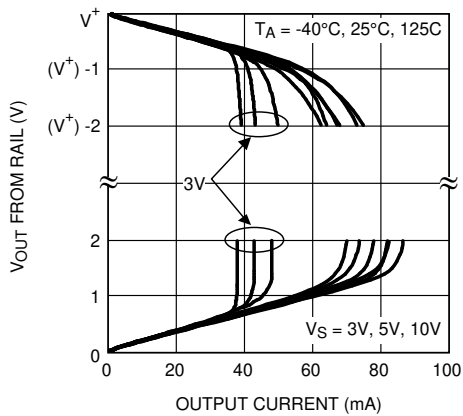


Figure 6-23. Output Voltage vs Output Current

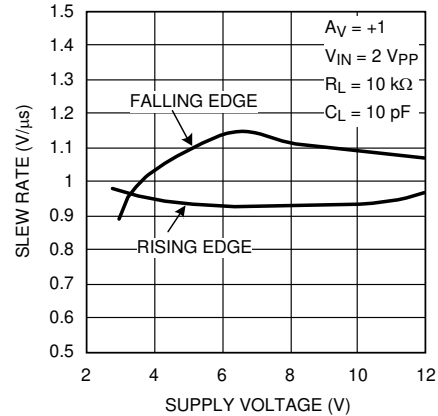


Figure 6-24. Slew Rate vs Supply Voltage

6.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{CM} = V_S/2$, $R_L > 10\text{ k}\Omega$ (unless otherwise noted)

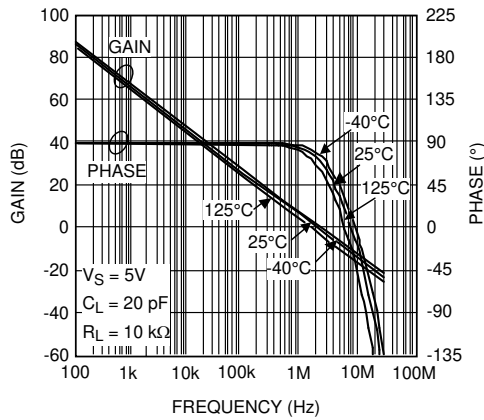


Figure 6-25. Open-Loop Frequency Response

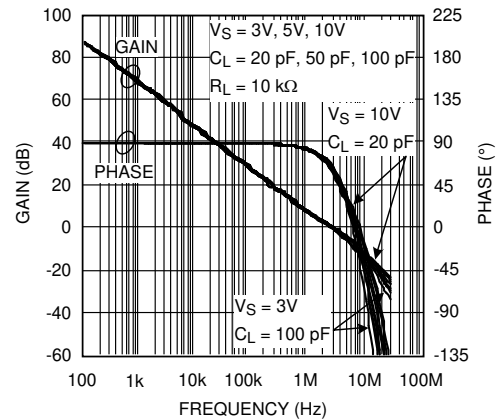


Figure 6-26. Open-Loop Frequency Response

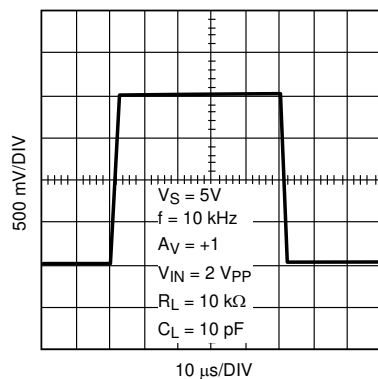


Figure 6-27. Large Signal Step Response

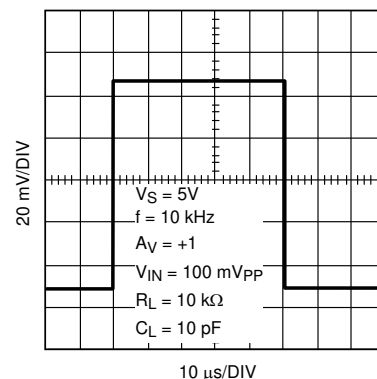


Figure 6-28. Small Signal Step Response

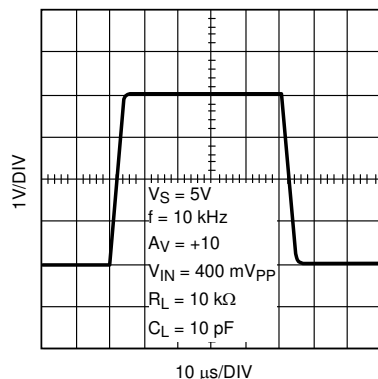


Figure 6-29. Large Signal Step Response

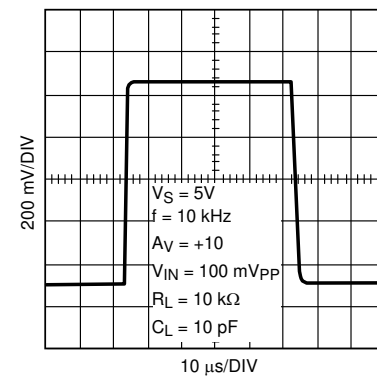


Figure 6-30. Small Signal Step Response

6.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{CM} = V_S/2$, $R_L > 10\text{ k}\Omega$ (unless otherwise noted)

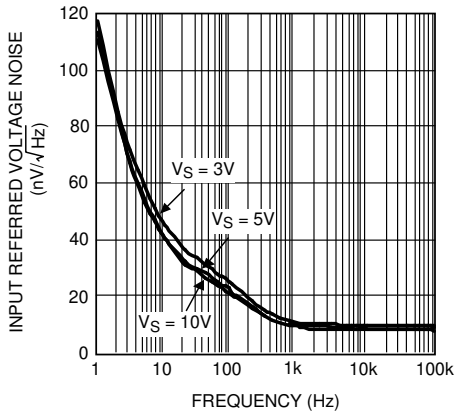


Figure 6-31. Input Voltage Noise vs Frequency

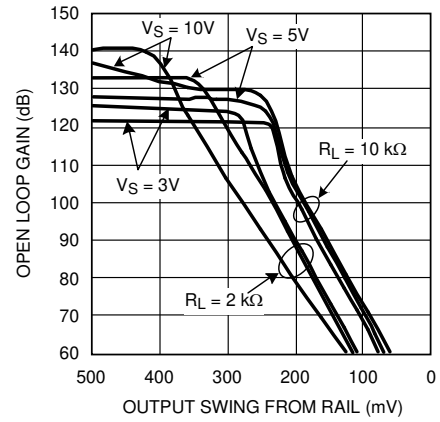


Figure 6-32. Open Loop Gain vs Output Voltage Swing

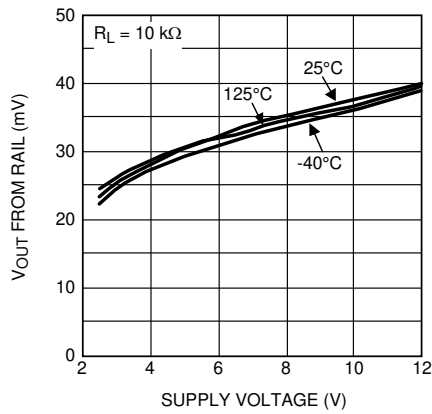


Figure 6-33. Output Swing High vs Supply Voltage

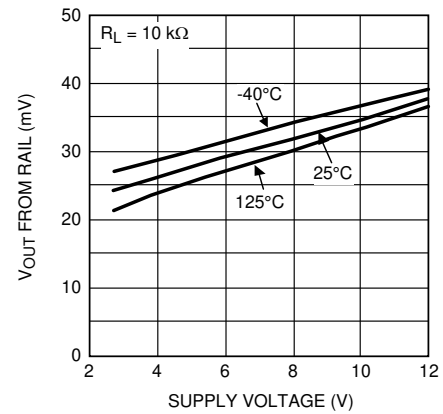


Figure 6-34. Output Swing Low vs Supply Voltage

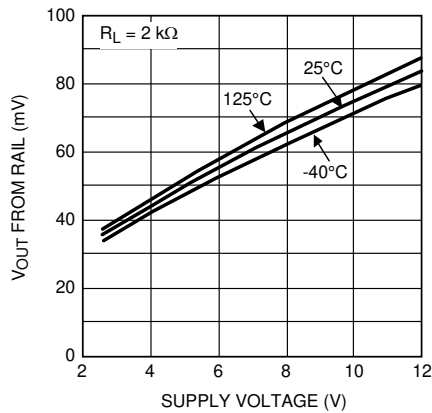


Figure 6-35. Output Swing High vs Supply Voltage

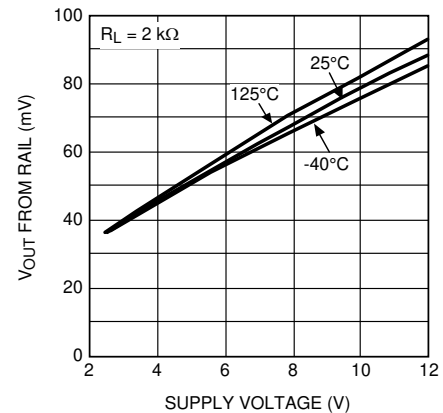


Figure 6-36. Output Swing Low vs Supply Voltage

6.7 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$, $V_{CM} = V_S/2$, $R_L > 10\text{ k}\Omega$ (unless otherwise noted)

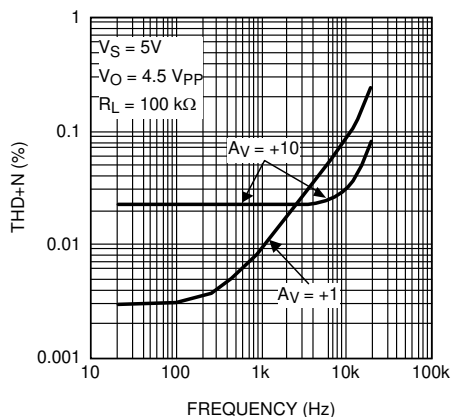


Figure 6-37. THD+N vs Frequency

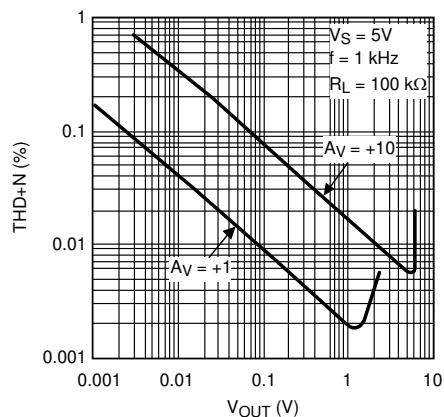


Figure 6-38. THD+N vs Output Voltage

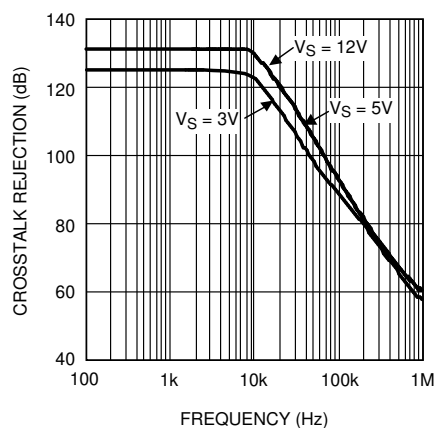


Figure 6-39. Crosstalk Rejection Ratio vs Frequency (LMP7702/LMP7704)

7 Detailed Description

7.1 Overview

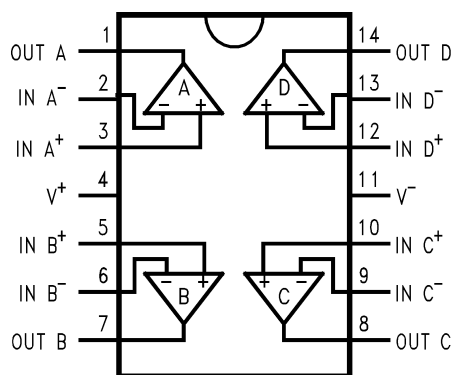
The LMP7704-SP is a radiation-hardened, quad, low offset voltage, rail-to-rail input and output precision amplifier with a CMOS input stage and wide supply voltage range of 2.7 V to 12 V. The LMP7704-SP has a very low input bias current of only ± 200 fA at room temperature.

The wide supply voltage range of 2.7 V to 12 V over the extensive temperature range of -55°C to $+125^{\circ}\text{C}$ makes the LMP7704-SP excellent choices for low-voltage precision applications with extensive temperature requirements.

The LMP7704-SP have only ± 37 μV of typical input-referred offset voltage. This minimal offset voltage allows more accurate signal detection and amplification in precision applications.

The low input bias current of only ± 200 fA along with the low input-referred voltage noise of $9 \text{ nV}/\sqrt{\text{Hz}}$ gives the LMP7704-SP superiority for use in sensor applications. Lower levels of noise from the LMP7704-SP mean better signal fidelity and a higher signal-to-noise ratio.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Radiation Hardened Performance

Total Ionizing Dose (TID)—The LMP7704-SP is a radiation-hardness-assured (RHA) QML class V (QMLV) product, and as such it has a total ionizing dose (TID) level specified in the *Device Information* table on the front page. Testing and qualification of these products is done on a wafer level according to MIL-STD-883, Test Method 1019. Radiation lot acceptance testing (RLAT) is performed at the 30-krad, 50-krad, and 100-krad TID levels.

Group E TID RLAT data are available with lot shipments as part of the QCI summary reports; for information on finding QCI summary reports, see [QML Flow, Its Importance, and Obtaining Lot Information](#).

Neutron Displacement Damage (NDD)—The LMP7704-SP was irradiated up to 1×10^{12} n/cm². A sample size of 15 units was exposed to radiation testing per MILSTD-883, Method 1017 for Neutron Irradiation.

Single-Event Effects (SEE)—One-time SEE characterization was performed according to EIA/JEDEC standard, EIA/JEDEC57 to linear energy transfer (LET) = 85 MeV·cm²/mg. During testing, no single-event latch-up (SEL) was observed.

7.3.2 Engineering Model (Devices With /EM Suffix)

Engineering evaluation or engineering model (EM) devices are available for order and are identified by the /EM in the orderable device name (see the *Ordering Information* table on the front page of the data sheet). These devices meet the performance specifications of the data sheet at room temperature only and have not received the full space production flow or testing. Engineering samples may be QCI rejects that failed tests that would not impact the performance at room temperature, such as radiation or reliability testing.

7.3.3 Capacitive Load

The LMP7704-SP can each be connected as a non-inverting unity gain follower. This configuration is the most sensitive to capacitive loading.

The combination of a capacitive load placed on the output of an amplifier along with the amplifier's output impedance creates a phase lag which in turn reduces the phase margin of the amplifier. If the phase margin is significantly reduced, the response will be either underdamped or it will oscillate.

To drive heavier capacitive loads, an isolation resistor, R_{ISO} , in [Figure 7-1](#) should be used. By using this isolation resistor, the capacitive load is isolated from the amplifier's output, and hence, the pole caused by C_L is no longer in the feedback loop. The larger the value of R_{ISO} , the more stable the output voltage will be. If values of R_{ISO} are sufficiently large, the feedback loop will be stable, independent of the value of C_L . However, larger values of R_{ISO} result in reduced output swing and reduced output current drive.

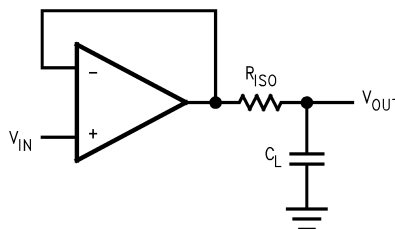


Figure 7-1. Isolating Capacitive Load

7.3.4 Input Capacitance

CMOS input stages inherently have low input bias current and higher input-referred voltage noise. The LMP7704-SP enhances this performance by having the low input bias current of only ± 200 fA, as well as, a very low input referred voltage noise of $9 \text{ nV}/\sqrt{\text{Hz}}$. To achieve these specifications, a larger input stage has been used. This larger input stage increases the input capacitance of the LMP7704-SP. The typical value of this input capacitance, C_{IN} , for the LMP7704-SP is 25 pF. The input capacitance interacts with other impedances, such as gain and feedback resistors, which are seen on the inputs of the amplifier, to form a pole. This pole has little or no effect on the output of the amplifier at low frequencies and dc conditions, but plays a bigger role as the frequency increases. At higher frequencies, the presence of this pole decreases phase margin and also causes gain peaking. To compensate for the input capacitance, care must be taken in choosing the feedback resistors. In addition to being selective in picking values for the feedback resistor, a capacitor can be added to the feedback path to increase stability.

The dc gain of the circuit shown in Figure 7-2 is simply $-R_2/R_1$.

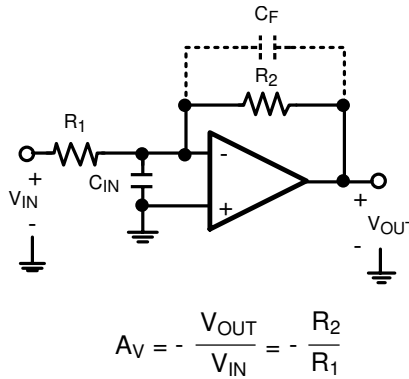


Figure 7-2. Compensating for Input Capacitance

For the time being, ignore C_F . The ac gain of the circuit in Figure 7-2 can be calculated as follows:

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}}(s) = \frac{-R_2/R_1}{\left[1 + \frac{s}{\left(\frac{A_0 R_1}{R_1 + R_2} \right)} + \frac{s^2}{\left(\frac{A_0}{C_{\text{IN}} R_2} \right)} \right]} \quad (1)$$

This equation is rearranged to find the location of the two poles:

$$P_{1,2} = \frac{-1}{2C_{\text{IN}}} \left[\frac{1}{R_1} + \frac{1}{R_2} \pm \sqrt{\left(\frac{1}{R_1} + \frac{1}{R_2} \right)^2 - \frac{4 A_0 C_{\text{IN}}}{R_2}} \right] \quad (2)$$

As shown in Equation 2, as values of R_1 and R_2 are increased, the magnitude of the poles is reduced, which in turn decreases the bandwidth of the amplifier. Whenever possible, best practice is to choose smaller feedback resistors. Figure 7-3 shows the effect of the feedback resistor on the bandwidth of the LMP7704-SP.

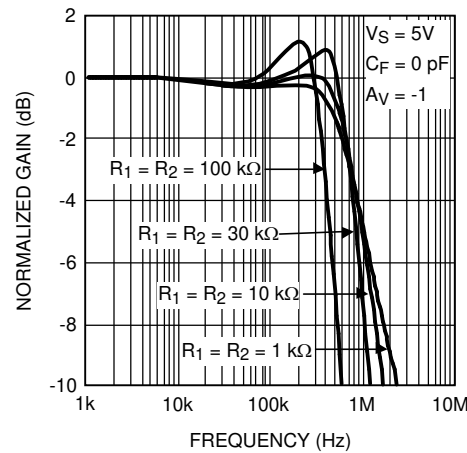


Figure 7-3. Closed-Loop Gain vs Frequency

Equation 2 has two poles. In most cases, it is the presence of pairs of poles that causes gain peaking. To eliminate this effect, the poles should be placed in Butterworth position, because poles in Butterworth position do not cause gain peaking. To achieve a Butterworth pair, the quantity under the square root in Equation 2 should be set to equal -1 . Using this fact and the relation between R_1 and R_2 , $R_2 = -A_V R_1$, the optimum value for R_1 can be found. This is shown in Equation 3. If R_1 is chosen to be larger than this optimum value, gain peaking will occur.

$$R_1 < \frac{(1 - A_V)^2}{2A_0A_VC_{IN}} \quad (3)$$

In Figure 7-2, C_F is added to compensate for input capacitance and to increase stability. Additionally, C_F reduces or eliminates the gain peaking that can be caused by having a larger feedback resistor. Figure 7-4 shows how C_F reduces gain peaking.

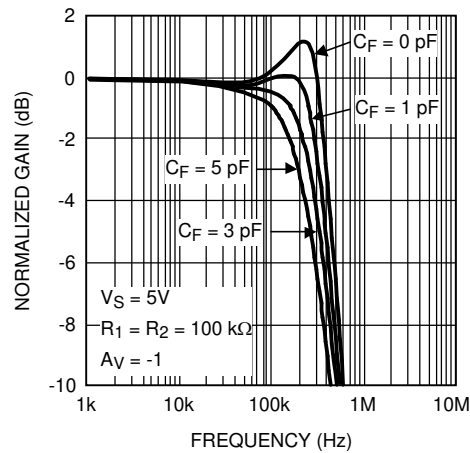


Figure 7-4. Closed-Loop Gain vs Frequency With Compensation

7.3.5 Diodes Between the Inputs

The LMP7704-SP have a set of anti-parallel diodes between the input pins, as shown in Figure 7-5. These diodes are present to protect the input stage of the amplifier. At the same time, they limit the amount of differential input voltage that is allowed on the input pins. A differential signal larger than one diode voltage drop might damage the diodes. The differential signal between the inputs needs to be limited to ± 300 mV or the input current needs to be limited to ± 10 mA.

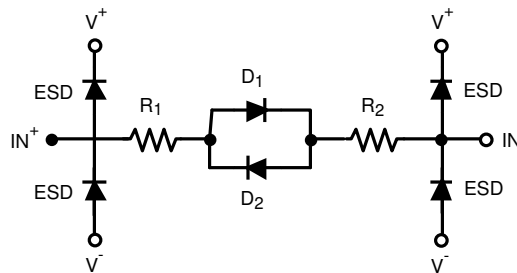


Figure 7-5. Input of LMP7704-SP

7.4 Device Functional Modes

7.4.1 Precision Current Source

The LMP7704-SP can each be used as a precision current source in many different applications. [Figure 7-6](#) shows a typical precision current source. This circuit implements a precision voltage controlled current source. Amplifier A1 is a differential amplifier that uses the voltage drop across R_S as the feedback signal. Amplifier A2 is a buffer that eliminates the error current from the load side of the R_S resistor that would flow in the feedback resistor if it were connected to the load side of the R_S resistor. In general, the circuit is stable as long as the closed loop bandwidth of amplifier A2 is greater than the closed loop bandwidth of amplifier A1. If A1 and A2 are the same type of amplifiers, then the feedback around A1 will reduce its bandwidth compared to A2.

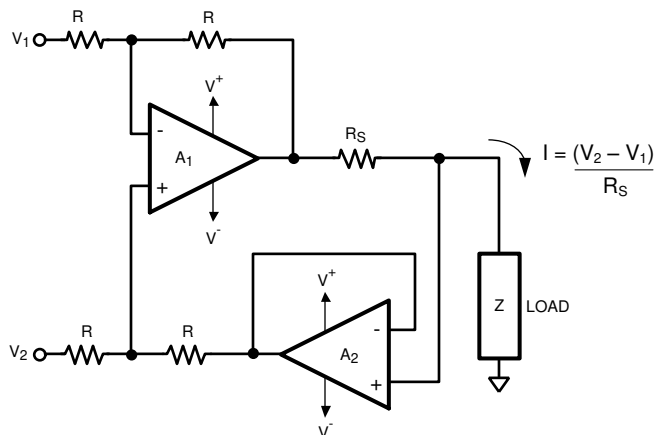


Figure 7-6. Precision Current Source

The equation for output current can be derived as shown in [Equation 4](#).

$$\frac{V_2 R}{R + R} + \frac{(V_0 - I R_S) R}{R + R} = \frac{V_1 R}{R + R} + \frac{V_0 R}{R + R} \quad (4)$$

Solving for the current I results in the [Equation 5](#).

$$I = \frac{V_2 - V_1}{R_S} \quad (5)$$

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Low Input Voltage Noise

The LMP7704-SP have the very low input voltage noise of $9 \text{ nV}/\sqrt{\text{Hz}}$. This input voltage noise can be further reduced by placing N amplifiers in parallel as shown in [Figure 8-1](#). The total voltage noise on the output of this circuit is divided by the square root of the number of amplifiers used in this parallel combination. This is because each individual amplifier acts as an independent noise source, and the average noise of independent sources is the quadrature sum of the independent sources divided by the number of sources. For N identical amplifiers, this means:

$$\begin{aligned} \text{REDUCED INPUT VOLTAGE NOISE} &= \frac{1}{N} \sqrt{e_{n1}^2 + e_{n2}^2 + \dots + e_{nN}^2} \\ &= \frac{1}{N} \sqrt{N e_n^2} = \frac{\sqrt{N}}{N} e_n \\ &= \frac{1}{\sqrt{N}} e_n \end{aligned} \tag{6}$$

[Figure 8-1](#) shows a schematic of this input voltage noise reduction circuit. Typical resistor values are:

$R_G = 10 \text{ } \Omega$, $R_F = 1 \text{ k}\Omega$, and $R_O = 1 \text{ k}\Omega$.

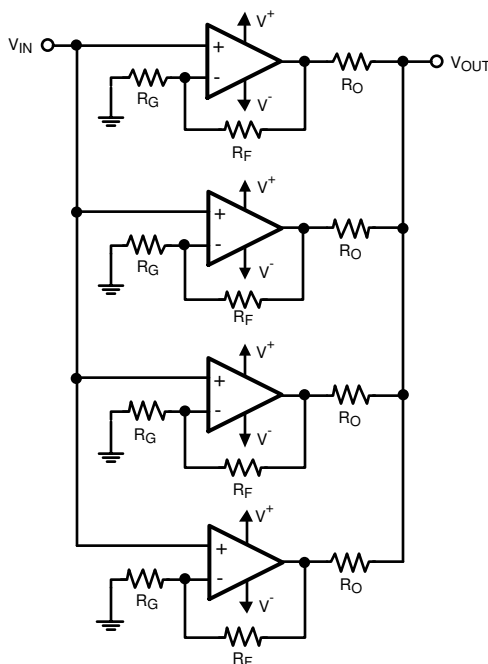


Figure 8-1. Noise Reduction Circuit

8.1.2 Total Noise Contribution

The LMP7704-SP have very low input bias current, very low input current noise, and very low input voltage noise. As a result, these amplifiers are excellent choices for circuits with high impedance sensor applications.

Figure 8-2 shows the typical input noise of the LMP7704-SP as a function of source resistance where:

- e_n denotes the input referred voltage noise.
- e_i is the voltage drop across source resistance due to input referred current noise or $e_i = R_S * i_n$.
- e_t shows the thermal noise of the source resistance.
- e_{ni} shows the total noise on the input, where:

$$e_{ni} = \sqrt{e_n^2 + e_i^2 + e_t^2}$$

The input current noise of the LMP7704-SP is so low that this noise does not become the dominant factor in the total noise unless the source resistance exceeds 300 MΩ, which is an unrealistically high value.

As is evident in Figure 8-2, at lower R_S values, total noise is dominated by the amplifier input voltage noise. After R_S is larger than a few kilo-ohms, then the dominant noise factor becomes the thermal noise of R_S . As mentioned previously, the current noise will not be the dominant noise factor for any practical application.

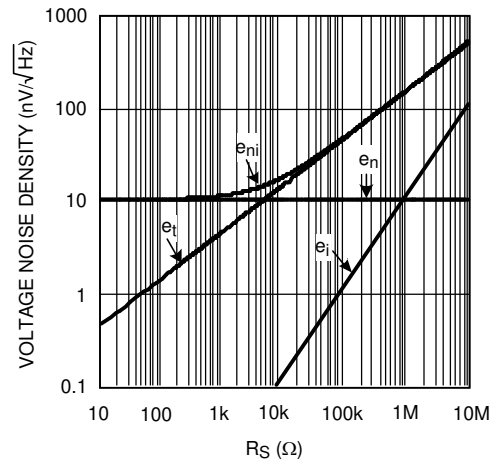


Figure 8-2. Total Input Noise

8.2 Typical Application

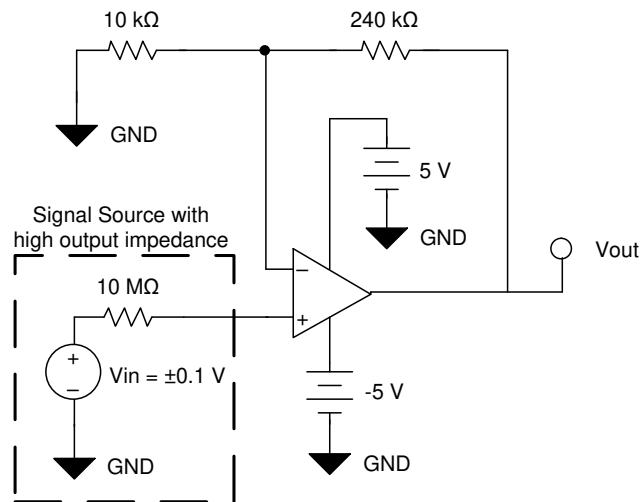


Figure 8-3. LMP7704-SP Configured for 25x Gain With High Signal Source Impedance

8.2.1 Design Requirements

Many precision, analog sensors such as temperature or pressure (bridge) sensors, require a high precision amplifier with low input bias to condition the signal before the analog-to-digital converter. The LMP7704-SP is an excellent amplifier choice for a voltage gain stage thanks to its low offset voltage, offset voltage drift and ultra-low input bias current.

8.2.2 Detailed Design Procedure

Many sensors have high source impedances that may range up to 10 MΩ. The output signal of sensors often needs to be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor output and cause a voltage drop across the source resistance, as shown in Figure 8-4, where $V_{IN+} = V_S - I_{BIAS} * R_S$.

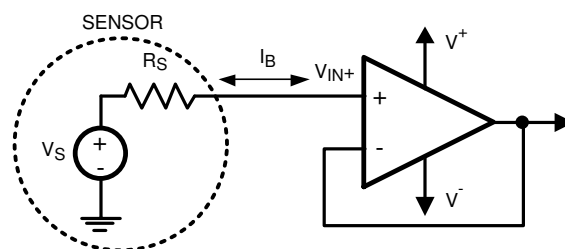


Figure 8-4. Offset Error Due to I_{BIAS}

The last term, $I_{BIAS} * R_S$, shows the voltage drop across R_S . To prevent errors introduced to the system due to this voltage, an op amp with very low input bias current must be used with high impedance sensors. An amplifier with low input bias also has low input current noise, further improving the accuracy of systems with high source resistance.

Figure 8-3 shows one channel of the LMP7704-SP configured for a gain of 10. A high source impedance is placed between the input signal and the noninverting input of the amplifier to represent the output impedance of the sensor.

With the ultra-low input bias current of the LMP7704-SP, even with a signal source that has high output impedance the system output maintains very good linearity to the ideal output voltage (that is, the output of an ideal amplifier in the same configuration) as shown in Figure 8-6.

8.2.3 Application Curves

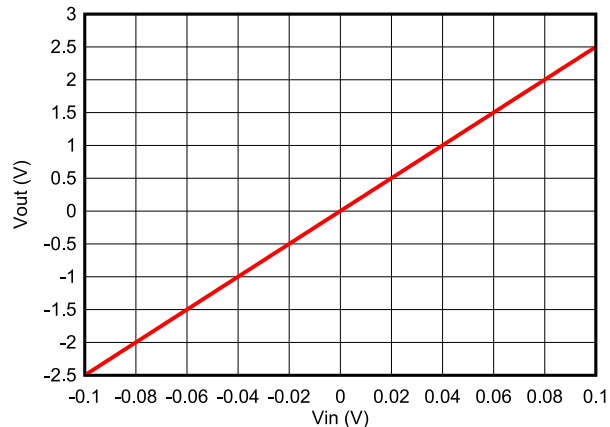


Figure 8-5. LMP7704-SP Output Voltage vs Input Voltage

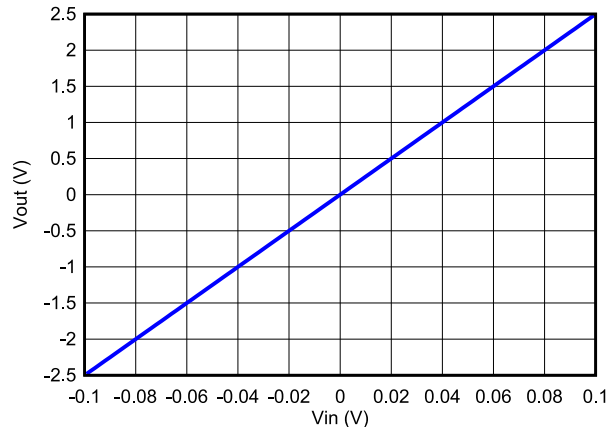


Figure 8-6. LMP7704-SP Ideal Output Voltage vs Input Voltage

9 Power Supply Recommendations

For proper operation, the power supplies must be decoupled. For supply decoupling, TI recommends placing 10-nF to 1- μ F capacitors as close as possible to the operational-amplifier power supply pins. For single supply configurations, place a capacitor between the V^+ and V^- supply pins. For dual supply configurations, place one capacitor between V^+ and ground, and place a second capacitor between V^- and ground. Bypass capacitors must have a low ESR of less than 0.1 Ω .

10 Layout

10.1 Layout Guidelines

Take care to minimize the loop area formed by the bypass capacitor connection between supply pins and ground. A ground plane underneath the device is recommended; any bypass components to ground should have a nearby via to the ground plane. The optimum bypass capacitor placement is closest to the corresponding supply pin. Use of thicker traces from the bypass capacitors to the corresponding supply pins will lower the power supply inductance and provide a more stable power supply.

The feedback components should be placed as close to the device as possible to minimize stray parasitics.

10.2 Layout Example

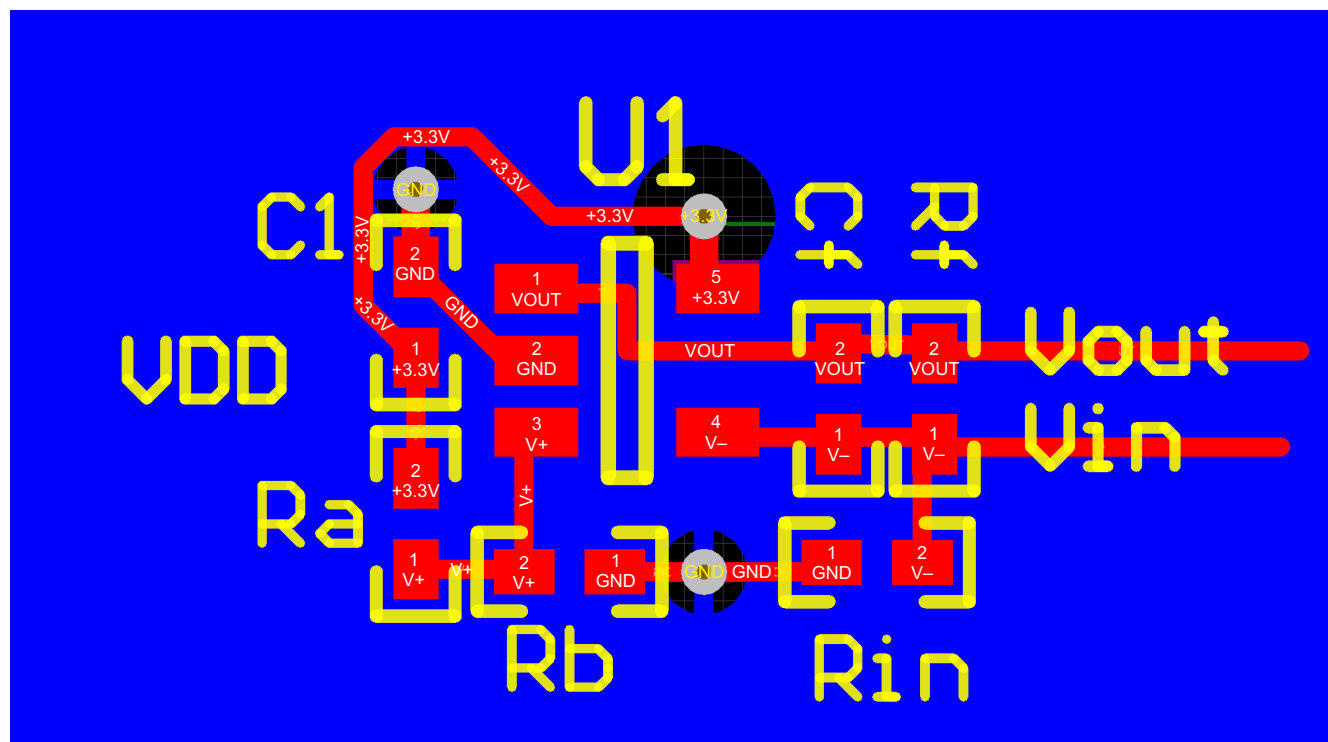


Figure 10-1. LMP7704-SP Example Layout for a Single Channel

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.3 Trademarks

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11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

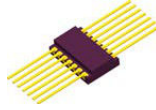
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

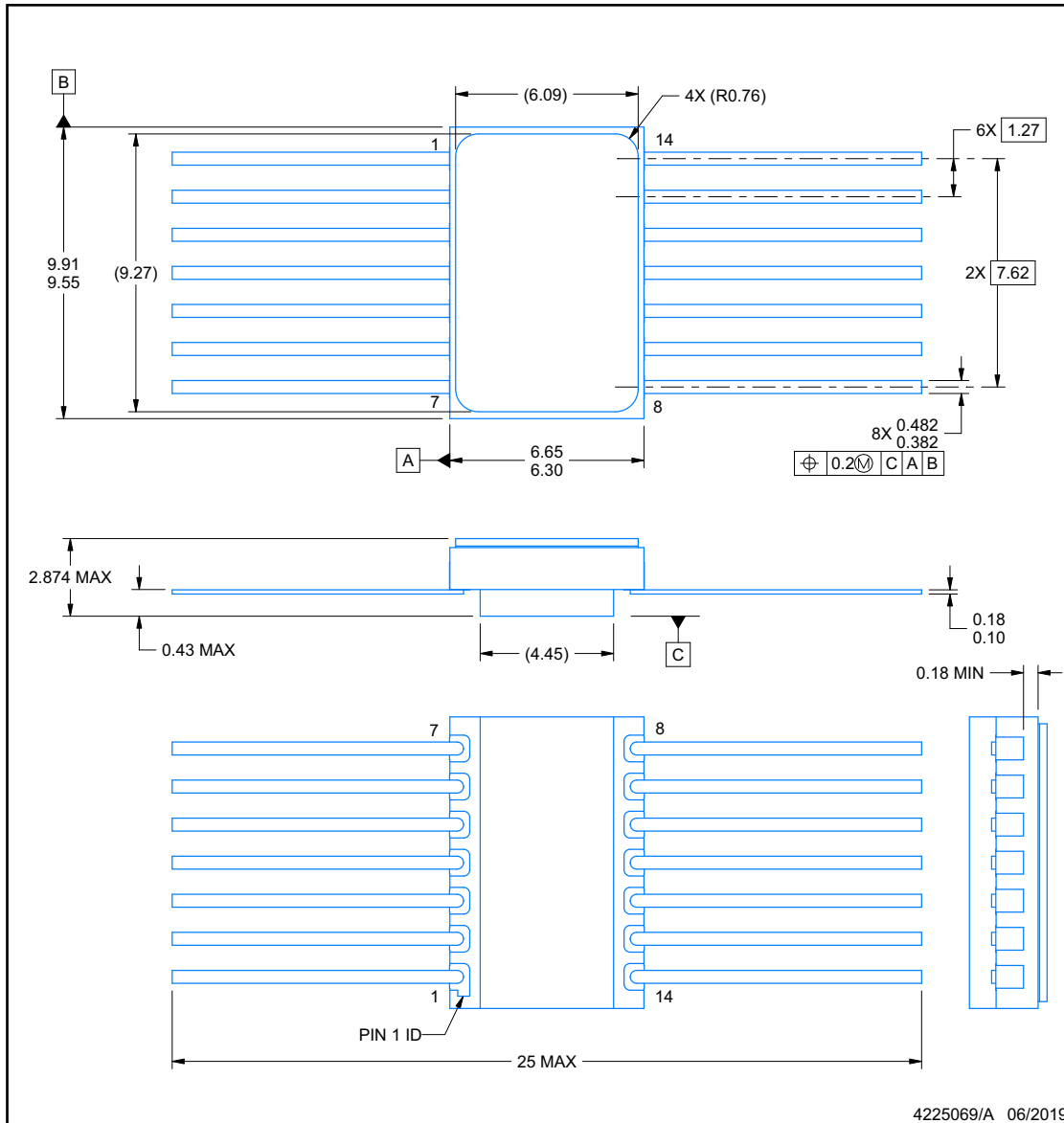
[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**HBH0014A**
PACKAGE OUTLINE
CFP - 2.874 mm max height

CERAMIC FLATPACK

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP7704HBH/EM	PREVIEW	CFP	HBH	14	1	RoHS (In work) & Green (In work)	Call TI	Call TI	-55 to 125		
PLMP7704HBH/EM	ACTIVE	CFP	HBH	14	1	RoHS (In work) & Green (In work)	Call TI	Call TI	-55 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF LMP7704-SP :

- Catalog: [LMP7704](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

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