ICS Model Questions

Computer Fundamentals

1. What are the main features of 2nd generation computers?
2. Computer Organization
   a. Draw a diagram showing the connection between the CPU and various devices and their access to memory.
   b. Describe in brief about the Von Neumann Architecture with the aid of a diagram.
   c. Explain in brief about the functions of each part listed in the von Neumann Architecture.

3. Write down short notes for following. Illustrate how they are connected to different components of a computer.
   a. Address Bus
   b. Data Bus
   c. Control Bus
4. The memory is made up of BYTES. Each BYTE can be addressed uniquely. When the address is expressed in Binary, the number of maximum BITs used to write the address specifies the total number of locations available. If **n** number of BITs are available, then the total number of locations available is $\mathbf{2^n}$.
   a. If a PC consist with 34 BIT memory, what is the memory capacity of that PC?
   b. If a PC consist with 512MB of main memory (RAM), how many bits are used to address the memory locations of that PC?

5. **Data Types**
   a. Explain different data types available to represent data in computers?
   b. Give some examples for each data type you listed.

6. **Number Representation**
   a. Explain how BCD works and limitation of it?
   b. Represent following numbers in BCD format?
      - 35
      - 49
      - 152
      - 3458

c. How many characters are possible in ASCII?
d. If the ASCII code for the letter "A" is 65, what is the ASCII Code for the letter "D"? Write the binary representation of it.
e. What are the other character codes available in ASCII?
f. What was the reason to select Unicode to represent characters?
g. Convert following IP address written in dotted decimal number to dotted binary number 126.54.24.76

7. Try to get the corresponding parity bit for the following bit patterns considering the used parity check technique.
    1. _ 0010111 (even parity)
    2. _0111011 (odd parity)
    3. _1100100 (even parity)
    4. _1111111(odd parity)
    5. _0000001 (odd parity)
    6. _0101010 (odd parity)
8. State four features of the storage devices.
9. Storage Organization.
10. Explain the hierarchy of the storages in computer and their characteristics.
11. RAM and ROM are both types of memory used by personal computers. Briefly explain these two types of memories.
12. Explain the difference between volatile and non-volatile memory.
13. Why does a personal computer need both types of memory?
14. Briefly explain the Cache Memory and Registers?
15. What is Flash Memory? Explain the characteristics of Flash memory.
16. Briefly explain the other examples of storage devices.
17. Simplify the following expressions using Boolean algebra.

    a. $A + AB$
    b. $A + A\overline{B}$
    c. $\overline{A}BC + AC$
    d. $\overline{A}B + AB\overline{C} + ABC$
    e. $AB + A\left(CD + C\overline{D}\right)$
    f. $\left(B\overline{C} + \overline{A}D\right)\left(A\overline{B} + C\overline{D}\right)$

(Question 1 is adopted from, *Computer system Architecture by Morris Mano, 3rd Edition, page 37*)

18. Use de Morgan's theorem to complement the following expressions. Do not simplify the expressions either before or after you complement them.

g. $\overline{X}\overline{Y} + XY$

h. $WX\left(\overline{Y}Z + YZ\right)$

i. $XYZ + \overline{X}\overline{Y}$

j. $WX\left(W\overline{Z} + \overline{Y}Z\right)$

k. $X\left(Y + Z\right) + \overline{X}\overline{Y}$

l. $XY + \overline{X}\overline{Y}\left(WZ + \overline{W}Z\right)$

19. Simplify the following expressions using Boolean algebra.

m. $A\overline{B}\overline{C} + \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}C$

n. $ABC + \overline{A}BC + A\overline{B}C + A\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}\overline{C}$

o. $ABC + A\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C} + A\overline{B}C + AB\overline{C} + \overline{A}\overline{B}\overline{C} + \overline{A}BC$

p. $\left(A + B + C\right)\left(A + \overline{B} + \overline{C}\right)\left(A + B + \overline{C}\right)\left(A + \overline{B} + C\right)$

(Questions 2 and 3 are adopted from, *The Principles of Computer Hardware by Alan Clements, 2nd Edition)*

20. Simplify the following Boolean expressions using K-maps.

a. $\overline{X} \cdot \overline{Y} \cdot \overline{Z} + \overline{X} \cdot \overline{Y} \cdot Z + \overline{X} \cdot Y \cdot \overline{Z} + X \cdot Y \cdot \overline{Z}$

b. $\overline{X} \cdot \overline{Y} \cdot Z + \overline{X} \cdot Y \cdot \overline{Z} + X \cdot Y \cdot \overline{Z} + X \cdot \overline{Y} \cdot Z$

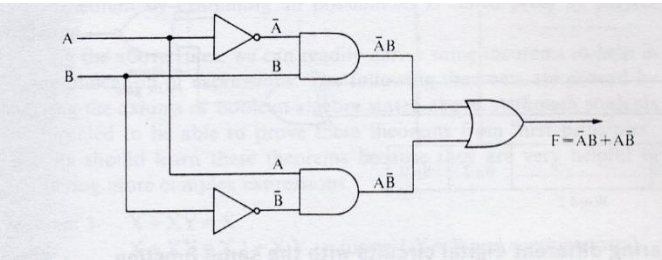
c. $\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot D + \overline{A} \cdot \overline{B} \cdot C \cdot D + \overline{A} \cdot B \cdot C \cdot \overline{D} + A \cdot B \cdot C \cdot \overline{D} + A \cdot B \cdot \overline{C} \cdot \overline{D} + A \cdot B \cdot \overline{C} \cdot D$

d. $\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot D + \overline{A} \cdot B \cdot \overline{C} \cdot D + A \cdot B \cdot \overline{C} \cdot D + A \cdot B \cdot C \cdot \overline{D} + A \cdot \overline{B} \cdot \overline{C} \cdot D + A \cdot B \cdot C \cdot D$

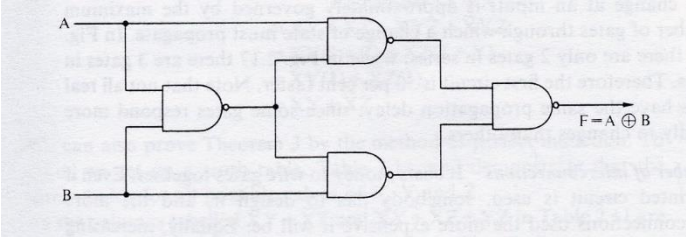
e. $\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot \overline{B} \cdot C \cdot \overline{D} + A \cdot \overline{B} \cdot C \cdot \overline{D} + A \cdot B \cdot \overline{C} \cdot \overline{D} + A \cdot B \cdot \overline{C} \cdot D$

21. Obtain the Boolean function as well as the truth table for following circuits. Using the Karnaugh Map, get the simplest sum-of-products form for the functions.

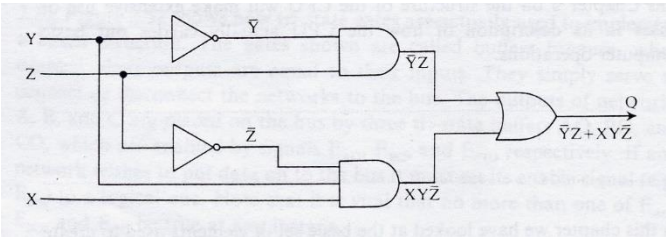
(a)



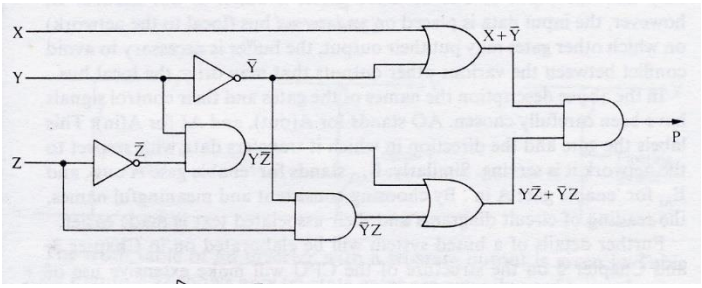
(b)



(c)



(d)



22. Using the Table in Figure 4-24 (a) in page 46 of the CF Text Book, derive the Boolean expression for the S (sum) output of the full-adder in sum-of-products form. Then by algebraic manipulation show that S can be expressed as the exclusive-OR of the three input variables.

$S = A \oplus B \oplus C$

23. Design a combinational circuit with three inputs x, y, z and three outputs A, B, C. When the binary input is 0, 1, 2 or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6 or 7, the binary output is one less than the input.

24. Show that the JK flip-flop can be converted to a D flip-flop with an inverter between the J and K inputs.

25. A sequential circuit has two D flip-flops. A and B, two inputs x and y, and one output z. The flip-flop input equations and the circuit output are as follows:

$D_A = x'y + xA$

$D_B = x'B + xA$

$z = B$

Draw the logic diagram of the circuit.

26. Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and one 2-to-4-line decoder. Use block diagrams.

27. Draw the logic diagram of a 2-to-4-line decoder with only NOR gates.

28. A logic circuit has three inputs C, B, A encoded in 4, 2, 1 natural binary form, so that a 3 bit binary number can be applied as the input. Input 'A' is used to feed the least significant bit of the number. It has a single output, F which is true if the input is divisible by 2. The circuit is used to select the number which is applied as the input, in order to use it for some other operations.

29. Implement the above circuit using a Multiplexer. First draw the block diagram of the implementation.

30. Implement the same circuit using a decoder and a OR gate.

31. Construct a 16-to-1 line Multiplexer with two 8-to-1 line Multiplexers. Use block diagrams of three Multiplexers in your design.

32. A logic circuit is needed to have a 3-to-8 line decoder for a circuit. But the designer of the circuit is not having a 3-to-8 line decoder. There are many 2-to-4 line decoders are available. Explain how a 3-to-8 line decoder can be constructed using two 2-to-4 line decoders. Use block diagrams to construct the circuit.

(Some Questions are adopted from, Computer system Architecture by Morris Mano, 3rd Edition, Chapters 1 & 2)

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