**COAL Lab # 00**

**Introductory Lab**

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**Class:** BSCS 3C1

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**Literature Review:**

In this lab we learned about the RISC-V architecture which is an open instruction set architecture (ISA) to implement CPU I microprocessor or microcontroller. hardware description language (HDL) is a specialized computer language used to describe the structure and behavior of electronic circuits, and most commonly, digital logic circuits. Verilog is one of a Hardware Description Language (HDL) used to model digital systems. VS code is an IDE (Integrated Development Environment) where Verilog designs could be written and edited.

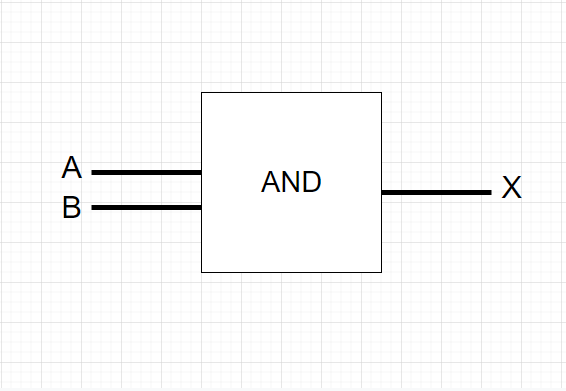
**Task:**

Implement AND gate function using Verilog.

**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **A** | **B** | **X** |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Block Diagram:**



**Boolean Equation:**

X = A.B

**Verilog Code:**

design.v

module gate(A,B,Y);

    // Declaring inputs

    input A,B;

    // Declaring output

    output Y;

    // Using gate level modeling

    and(Y,A,B);

endmodule

testBench.v

module tb();

    // declaring variables

    reg A,B;

    wire Y;

    // declaring design // dut (Design Under Test)

    gate dut (.A(A),.B(B),.Y(Y));

    initial begin

      // value change dump // variable change dump

      $dumpfile("Dump.vcd");

      $dumpvars(0);

    end

    // All input values for AND gate

    initial begin;

      A <= 1'b0;

      B <= 1'b0;

      #100

      A <= 1'b0;

      B <= 1'b1;

      #100

      A <= 1'b1;

      B <= 1'b0;

      #100

      A <= 1'b1;

      B <= 1'b1;

      #100;

      $finish;

    end;

endmodule;

**Waveforms:**

