Usman Ayub

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Summary

A Bs Electrical Engineering student with a strong foundation in embedded systems, AI for IoT, and hardware-software co-design. Passionate about digital design and system architecture, I have hands-on experience in RISC-V-based development, FPGA-based accelerators, and low-power computing. Skilled in Verilog for hardware design and verification, currently exploring Universal Verification Methodology (UVM) to enhance my proficiency in testbench development. My expertise extends to signal processing, MATLAB, and parallel/distributed processing, focusing on optimizing embedded AI solutions. Currently, I am working on my Final Year Project, designing a low-power Neural Processing Unit (NPU) for AI inference—integrating hardware design, verification, and performance optimization to enable efficient edge computing.

Education

National University of Science and Technology — Islamabad, Pakistan
Bachelor of Electrical Engineering — *Sep. 2021 – July 2025 (expected)*
CGPA: 3.61/4.0

Relevant Coursework: *Computer Architecture and Organization, Embedded Systems and Design, Digital System Design, Digital Design Verification, Parallel and Distributed Processing , Computer Vision, Discrete Signal Processing, Signals and Systems, Microprocessor Systems, Digital Logic Design, Probability & Statistics*

IQRA Academy — Abbottabad, Pakistan
Cambridge A Levels in Pre-Engineering — *2018 – 2020*
A* in Physics, A* in Mathematics, A* in Chemistry

Experience

Research Intern — June 2024 – August 2024
ChipXpert — *NUST, Islamabad*

- Conducted extensive literature reviews of state-of-the-art Neural Processing Units (NPUs) and RISC-V instruction set extensions (ISAs) to identify promising AI acceleration techniques for resource-constrained edge devices.
- Evaluated existing NPU architectures, pinpointing bottlenecks and opportunities to optimize for low-power AI inference, with a focus on minimizing memory access overhead.
- Designed and implemented a scalar core in Verilog to serve as the foundation for AI workloads, emphasizing streamlined data handling and control flow for efficient execution.
- Developed and validated Processing Elements (PEs) tailored for accelerating matrix operations commonly found in deep learning inference, employing techniques to enhance throughput.
- Translated key NPU components into synthesizable Verilog code, prioritizing functional correctness through rigorous testing and adherence to coding best practices to ensure reliable hardware implementation.
- Actively participated in weekly technical reviews, presenting research findings, proactively addressing design challenges, and iteratively refining the NPU architecture based on feedback from senior engineers.

Research Intern — Sept. 2024 – Present
System on Chip Lab, SINES, NUST — *Islamabad, Pakistan*

- Spearheading the development of a specialized AI Processing Unit (APU) to drastically improve the computational efficiency of TinyML models deployed on edge devices, focusing on novel architectural approaches.
- Pioneering the optimization of TinyML model software implementations by leveraging Parallel and Distributed Processing (PDP) methodologies, targeting significant gains in inference speed while minimizing power consumption.
- Investigating the application of mixed-precision arithmetic and truncated multiplication strategies to dramatically reduce computational complexity and overall energy footprint, contributing to ultra-low-power AI solutions.
- Creating comprehensive verification strategies and testbenches to rigorously validate APU performance under diverse operating conditions, utilizing advanced simulation tools to identify and rectify potential design flaws early in the development cycle.

- Collaborating closely with a multidisciplinary research team to integrate cutting-edge hardware acceleration techniques tailored for RISC-V-based AI workloads, facilitating seamless integration and enhanced system performance.
- Championing the refinement of hardware-software co-design strategies to maximize overall NPU performance in real-world IoT applications, emphasizing a holistic approach to system optimization.

Machine Learning and Automation Engineer July 2024 – December 2024

Team Peregrine Falcons *NUST, Islamabad*

- Conducting research on edge computing and machine learning algorithms using Jetson Nano for UAS applications.
- Developing and optimizing machine learning algorithms to support autonomous medical kit delivery in UAS competitions.
- Researching and implementing serial communication techniques between Jetson Nano and microcontrollers for efficient input/output signal handling.
- Collaborating with a multidisciplinary team to integrate AI models and hardware seamlessly, while also investigating innovative solutions to enhance system performance.

SEO Intern June 2023 – August 2023

Shadyana *Remote*

- Conducted research on the most effective SEO techniques and strategies, ensuring up-to-date and optimized practices for website enhancement.
- Quickly learned and applied SEO techniques to improve website rankings, despite having no prior experience in SEO.
- Developed and implemented effective backlink strategies, demonstrating adaptability and rapid learning in a new field.
- Worked under supervision to ensure SEO practices aligned with industry standards and best practices.

Projects

Low-Power Neural Processing Unit (NPU) on RISC-V | *Verilog, Xilinx Vivado, Python, TinyML, PDP*

- Designed a low-power NPU on RISC-V for TinyML inference on edge devices.
- Developed a functional **scalar core** and **Processing Elements (PEs)** for efficient AI computations.
- Currently working on an **AI Processing Unit (APU)** to enhance computation efficiency.
- Optimizing TinyML models using **Parallel and Distributed Processing (PDP)** for better performance.
- Integrated **RISC-V vector extensions** for accelerated deep learning on FPGAs.
- Implementing **hardware-software co-design** to streamline TinyML model execution.

Cache Memory with Cache Controller Design | *Verilog, Xilinx Vivado, Python, Digital Design*

- Designed and implemented a 4-way set-associative cache with a 32KB capacity and 64-byte block size, aimed at reducing cache misses in high-performance embedded systems.
- Developed a fully pipelined cache controller in Verilog, supporting read, write, and evict operations, and utilizing an LRU (Least Recently Used) replacement policy to optimize data retention.
- Implemented write-through and write-back strategies for handling data consistency between the cache and main memory, achieving improved data integrity.
- Synthesized and verified the cache controller design using Xilinx Vivado, ensuring timing closure and efficient FPGA resource utilization for deployment in real-time systems.

Embedded System Design: Secure Messenger | *ESP32, MQTT, WiFi, Encryption*

- Designed and implemented a secure messenger system using ESP32, MQTT protocol, and WiFi communication for encrypted message transmission.
- Developed an XOR-based encryption algorithm for securing messages during transmission, ensuring privacy and preventing unauthorized access.
- Created a two-way communication model where messages can be both sent and received securely between devices connected to the same MQTT broker.
- Utilized FreeRTOS for multitasking, enabling simultaneous management of WiFi connection, MQTT communication, and serial input handling.
- Implemented a message queue system to ensure seamless message handling and transmission, even when multiple tasks were running concurrently.

Smart Parking System | *Ultrasonic Sensors, IR Sensors, LCD, Python, EasyOCR, OpenCV*

- Designed and developed a smart parking system using ultrasonic and IR sensors to detect available parking spaces in real-time.
- Implemented an LCD display to show the status of parking spaces, such as availability and occupancy.
- Created a wireless communication interface for remote control, integrating serial communication to toggle LED indicators for parking space availability.
- Developed a dynamic algorithm for calculating parking space occupancy, utilizing sensor data to detect the distance and occupancy of parking spots.
- Implemented OCR-based image processing using EasyOCR to read and detect license plate numbers in real-time, enabling automated parking validation.
- Leveraged OpenCV for object detection and image processing, integrating live video streams and real-time parking monitoring.

Parametrized Bit-Serial RISC-V | *Verilog/VHDL, Xilinx Vivado, FPGA*

- Designed a bit-serial RISC-V core with 10 I-type and 1 M-type instructions.
- Parametrized the Arithmetic Logic Unit (ALU) to work for both 4-bit and 16-bit word lengths.
- Successfully synthesized and implemented the design on FPGA.

RISC-V Base 32 Integer Core on FPGA | *Verilog/VHDL, Xilinx Vivado, FPGA*

- Designed a single-cycle RISC-V RV32I core with a 5-stage pipeline architecture.
- Synthesized and executed Fibonacci sequence on FPGA platform.

Arrhythmia Classification Using Discrete Wavelet Transform | *MATLAB, Machine Learning*

- Preprocessed time-series ECG signals to identify heart arrhythmias.
- Applied Discrete Wavelet Transform (SYMLET 4) to detect R peaks in ECG signals.
- Trained and tested machine learning models on patient data for arrhythmia detection.

Speed Control of Induction Motor Using VFD | *MATLAB, Proteus*

- Converted AC voltage to DC using full-wave rectification circuit.
- Implemented PWM to generate square waves and control the motor speed using MOSFETs.

Smog Detection | *Arduino, Python, Google Colab*

- Developed a prototype for smog prediction in urban areas based on sensor data.
- Used MQ2, MQ4, and MQ135 sensors to monitor air quality and detect smog-related gases.
- Trained AI models to predict smog conditions for the next 10 days using real-time sensor values.

TinyML Temperature Sensor | *ATmega16, Microchip Studio, Python, C++*

- Implemented TinyML on AVR microcontroller for accurate temperature measurements.
- Deployed a machine learning model for sensor calibration, improving measurement precision.
- Enabled real-time temperature monitoring through UART communication for local and remote access.

4-Bit Number Crunching Machine | *Proteus, Logic Gates*

- Designed a 4-bit microprocessor including an ALU, data registers, and control logic unit.
- Implemented the processor using logic gates and demonstrated its functionality with Fibonacci sequence generation.

Additional Courses

CS-371 Minor in Artificial Intelligence — *NUST, Islamabad*

CS-253 Minor in Data Structures and Algorithms — *NUST, Islamabad*

Skills

Programming: Python, C/C++, Verilog, VHDL, RISC-V ASM, Assembly, HTML/CSS
Design & Simulation: Vivado, Quartus, ModelSim, MATLAB/Simulink, Proteus, LTspice, LabVIEW
Development Environments: VS Code, PyCharm, Anaconda, Microchip Studio, STM32CubeIDE, FreeRTOS
Embedded Systems: FPGA, RISC-V, STM32, Raspberry Pi, Jetson Nano, Advanced Virtual RISC uC
AI/ML Frameworks: TensorFlow, PyTorch, OpenCV, Keras, EasyOCR, Scikit-learn, NumPy, Pandas
Soft Skills: Problem-solving, Research, Teamwork, Leadership, Adaptability, Time-management

Conference Attended

Materials for Sustainable Energy & Climate Change (MatSEC) *Aug. 2023*

- Attended the International Conference on MatSEC 2023 at NUST, Pakistan, supported by the British Council.
- The conference featured keynote addresses and panel sessions by researchers from Cranfield University, UK.
- Participation aimed at exploring how my research field can contribute to the development of sustainable energy and climate change solutions.

Honors & Achievements

Currently maintaining the third highest CGPA among 45 students of NUST Electrical Engg. program in BEE-13A

3rd Position Winner of Elevator pitch competition of American Society of Mechanical Engineers, 2024

Merit Scholarship Awardee in A levels and O levels.

Bebras Mathematic Competition Winner, 2018.

Extra-Curricular Activities

Office Bearer of Nust IEEE Club (2023-2014).

Participated in the Intra-Department Cricket Championship, 2022

Interested in Swimming and gym.