

Digital Logic

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Task			Mark	Grade
Task 0 - Logic Functions			8 %	
Task 1 - Mystery Circuit			8 %	
Task 2 - Social Committee			7 %	
Task 3 - 7 segment 'bit 5'			9 %	
Task 4 - SR Latch			7 %	
Task 5 - Clocked SR Latch			7 %	
Task 6 - Clocked D Latch			7 %	
Task 7 - D Flip Flop			9 %	
Task 8 - Registers			7 %	
Task 9 - JK Flip Flop			7 %	
Task 10 - Shift Register			7 %	
Task 11 - Binary Counter			7 %	
Task 12 - Reflection			10 %	
Total			100 %	

COMP1588 Computer Systems Architectures

Laboratory #2

Digital Logic

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Abstract

This lab was all about Digital Logics. All the tasks were very long and we had to separate each task. We felt that Task 3 was the longest. Due to the reason that we had done it, but when I went over it all, I had to do it again. Due to that the map was wrong. I felt that I had to complete Task 3 again for us to get it right. We had a few mistakes that I noticed. We spent hours after the laboratories completing the tasks up to 11.

Introduction

In this report, we had several of tasks about Logic gates. We were set tasks up to 11 tasks. Each task were separated out into a group so we can complete the tasks much quicker. We had a two week period to complete.

Methods and Materials

Equipment/Material used:

- Lab Guide (Greenwich, 2016)
- DC Power Supply
- Oscilloscope
- Function Generator
- Breadboard
- Jumper Wires
- Switch Light Box
- Dual Seven Segment Display
- Oscilloscope Probe
- BNC to BNC cable
- BNC to Crocodile Clips Cable
- BNC to Probe Clips Cable
- BNC "T" Adaptor
- IDC10 Cable
- Chip sets

Software Used:

- Microsoft Office
- Crocodile Clips

Experimental Procedure

For this laboratory session, we followed a guide provided by the University of Greenwich that told us what to do step by step. All steps were followed; no extra steps were taken when doing the exercise that was based on the guide.

Results

Task 0 - Logic Gates

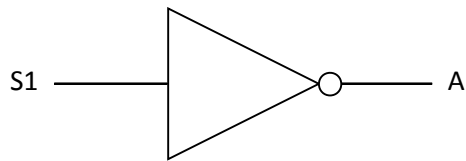
S ₁	S ₂	A	B	C	D	E	F
0	0	1	1	1	0	0	0
0	1	1	1	0	0	1	1
1	0	0	1	0	0	1	1
1	1	0	0	0	1	1	0

Table 1

S ₁	S ₂	A
0	0	1
0	1	1
1	0	0
1	1	0

Table 2

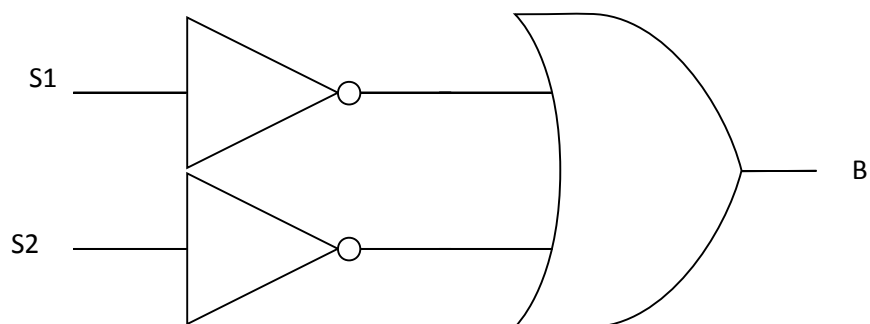
$$A = \overline{S_1}$$



S ₁	S ₂	B
0	0	1
0	1	1
1	0	1
1	1	0

Table 3

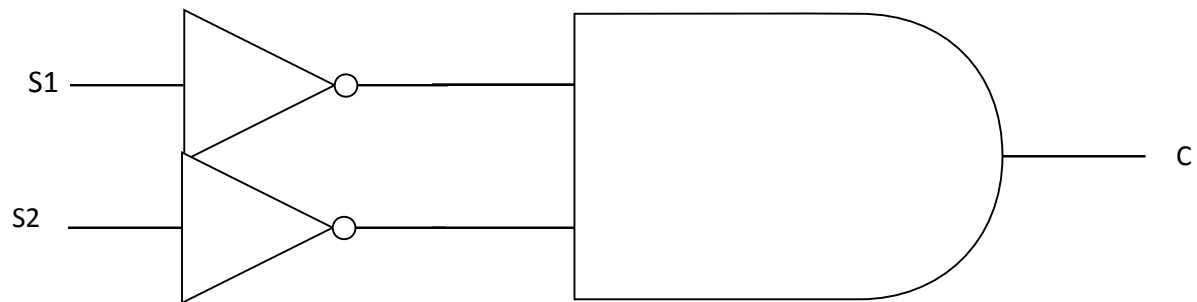
$$B = \overline{S_1} + \overline{S_2}$$



S ₁	S ₂	C
0	0	1
0	1	0
1	0	0
1	1	0

Table 4

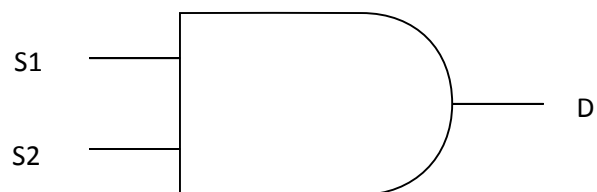
$$C = \overline{S_1} \cdot \overline{S_2}$$



S ₁	S ₂	D
0	0	0
0	1	0
1	0	0
1	1	1

Table 5

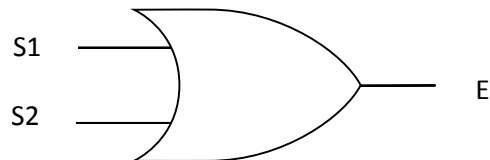
$$D = S_1 \cdot S_2$$



S ₁	S ₂	E
0	0	0
0	1	1
1	0	1
1	1	1

Table 6

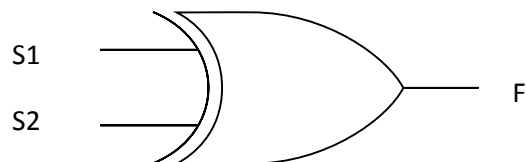
$$E = S1 + S2$$



S ₁	S ₂	F
0	0	0
0	1	1
1	0	1
1	1	0

Table 7

$$F = S1 \oplus S2$$



Task 1 - Mystery Circuit

Demonstrate the circuit's operation to the tutor, and upload to your logbook, the truth table, a description of the function of the circuit, clearly indicating the purpose the inputs and outputs. A circuit diagram of the three of the circuits connected together with the function of all inputs and outputs clearly marked - state where any unused input or outputs would be connected to within a computer. Give three examples showing the circuit's operation.

S7	S6	S5	L7	L6
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 8 – Mystery Circuit
Truth Table (Physical
Results)

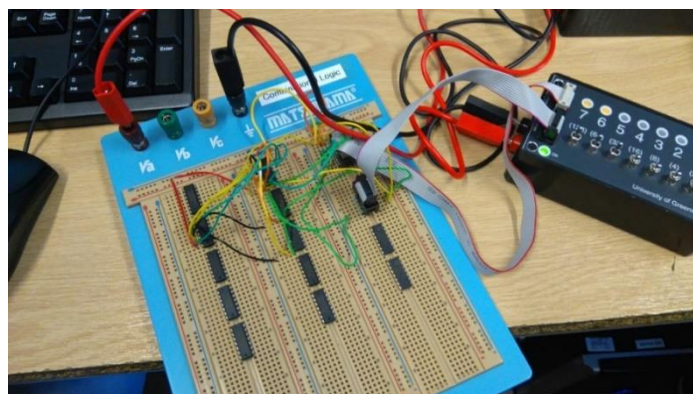


Figure 1 - Task 1 Breadboard Circuit

One member of the team constructed the circuit and Figure 1 shows how this was made. Figure 2 and 3 shows different results from the circuit made.



Figure 3 - Output from the constructed circuit

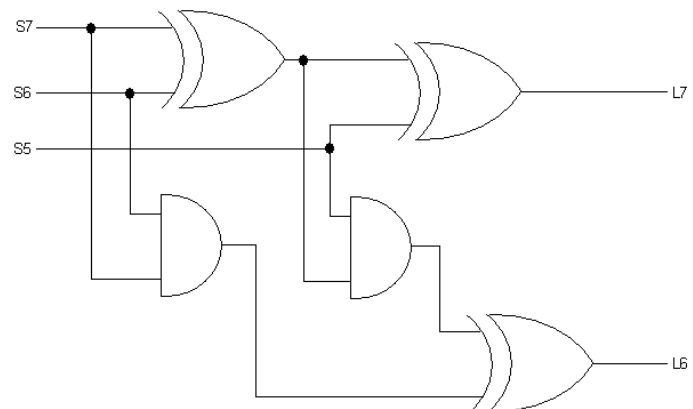


Figure 2 - Output from the constructed circuit

S7	S6	S5	L7	L6
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 9 - Mystery Circuit Truth Table (Calculated Results)

This was calculated by one member of the team and the results are shown.



S7	S6	S5	L7	L6
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 10 - Mystery Circuit Truth Table (Software Results)

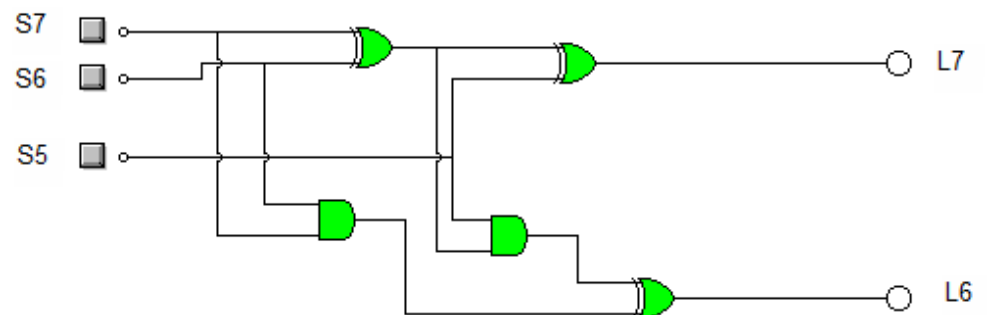
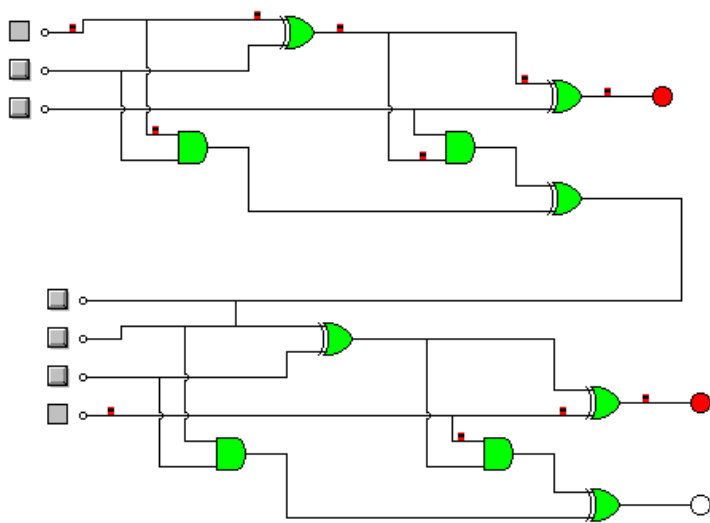


Figure 4 - Mystery Circuit Diagram Crocodile Clips

This was used on Crocodile Clip software where we the truth table shows the results of the circuit made on the software.

The circuit turns L7 on when only one switch is flicked. L6 turns on when only two switches are flicked. Finally, L7 and L6 turn on when all three are flicked.



For all three, to be connected, we need another one to be connected with each other. For example, all of them needs to be connected with each other. For the construction to be connected, we need a jumper wire connecting one to another for it to be connected with each other. This picture above shows how it is done by connecting all three circuits together. Another one would be exactly the same.

Task 2 - Social Committee

Demonstrate the circuit's operation to the tutor and upload to your logbook, the truth table, the Karnaugh map and the circuit diagram.

J	M	S	\bar{S}	J.M	$M.\bar{S}$	M+S
0	0	0	1	0	0	0
0	0	1	0	0	0	1
0	1	0	1	0	1	1
0	1	1	0	0	0	1
1	0	0	1	0	0	0
1	0	1	0	0	0	1
1	1	0	1	1	1	1
1	1	1	0	1	0	1

Table 11 - Task 2 Truth Table

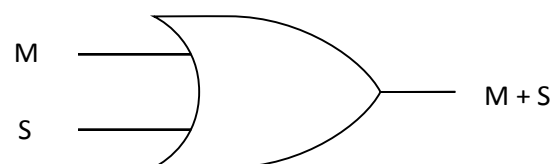
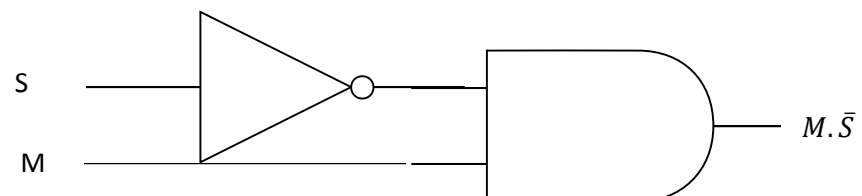
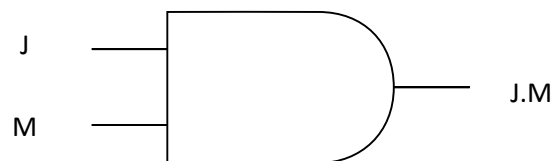
The Karnaugh Maps:

J/M	1	0
1	1	0
0	0	0

M/\bar{S}	1	0
1	1	0
0	0	0

M/S	1	0
1	1	1
0	1	0

Circuit Diagrams:



Task 3 - 7 segment 'Bit 5'

Construct the Karnaugh map for the segment controlled by 'bit 5' and implement the circuit. Connect the switch light box and the dual seven segment display to the breadboard and demonstrate the circuit's operation to the tutor. Upload the Karnaugh map and circuit diagram to your logbook.

S3	S2	S1	S0	Bit 5
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1

Table 12 - Bit 5 Truth Table

Karnaugh Map:

S3 S2 \ S1 S0	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	0	0	0	0
10	1	1	0	0

Boolean Equation:-

$$(\bar{S}1. S3. \bar{S}2) + (\bar{S}0. \bar{S}1. \bar{S}2. \bar{S}3) + (\bar{S}1. \bar{S}3.S2) + (\bar{S}3.S2.S1. \bar{S}0)$$

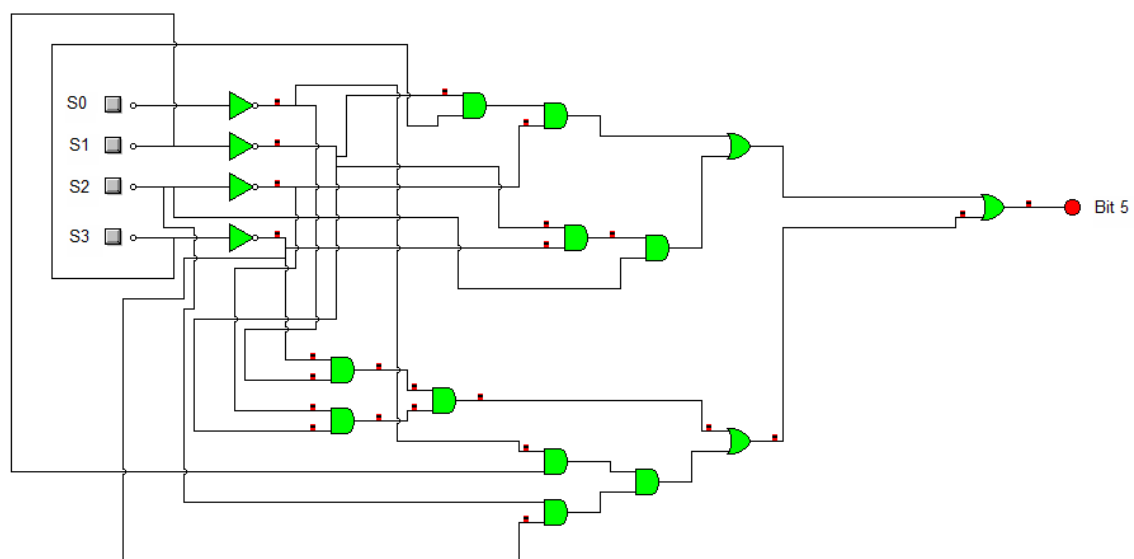


Figure 5 - Bit 5 Circuit Diagram Crocodile Clips

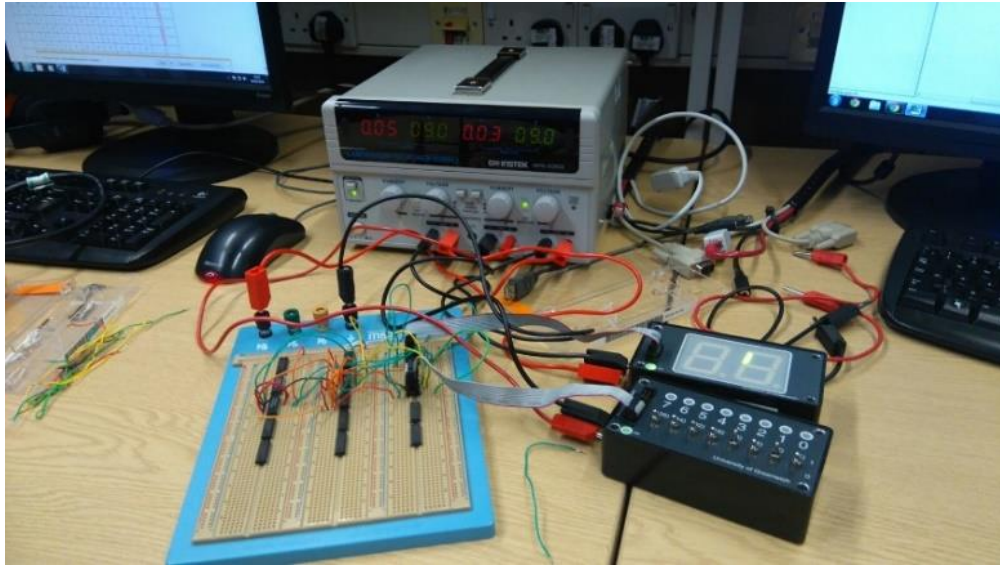


Figure 6 - Task 3 Overview

After the logic was completed, we now needed to implement this into physical form on the breadboard. The circuit that was created in crocodile clips helped us to plan where all the wires were going to go. We connected the switch output to one IDC input on the breadboard, then connected the IDC output on the dual seven segment display on the other IDC input on the breadboard. From here, I used jumper wires to create the circuit where S_0 is the 0 on the switch and the top left output on the breadboard and S_2 was the top right output on the breadboard of the IDC input and so on. After the circuit was created, we compared the results given to us in a table on the lab guide with what is displaying on the seven segment display, 0 means off, 1 means on, few pictures were taken for proof that our circuit worked as shown in Figures 6.

Task 4 - SR Latch

Upload to your logbook, the truth table and timing diagrams. State the purpose of the circuit.

S	R	Q _{n+1}
0	0	No Change
0	1	0
1	0	1
1	1	Forbidden

Table 13 - Truth Table

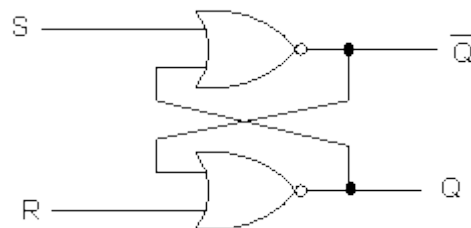


Figure 7 – SR Latch (Greenwich, 2016)

S	R	Q _{n+1}
0	0	No Change
0	1	0
1	0	1
1	1	Forbidden

Table 14 - Truth Table (Software)

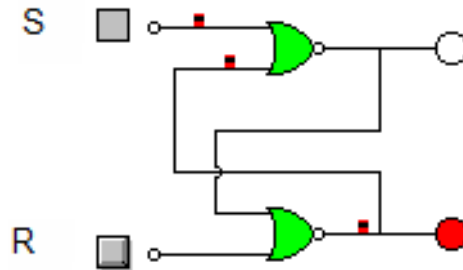


Figure 8 – SR Latch (Software)

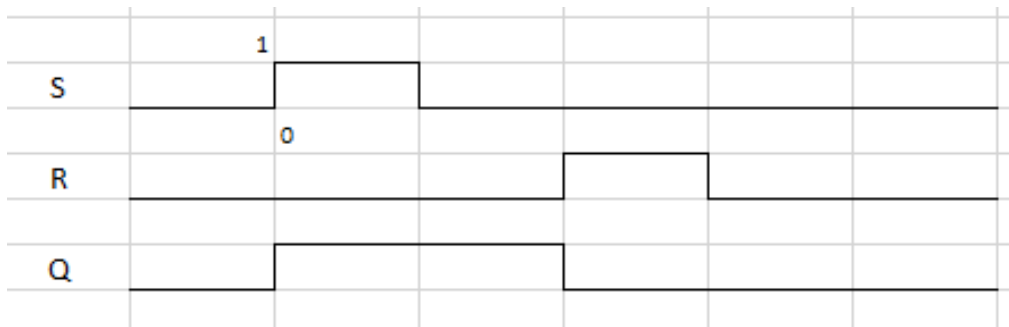


Figure 9 - Timing Diagram

The purpose of this circuit is an asynchronous device that works independently by relying on the two inputs; set and reset. This is why both of them cannot work together. They need to rely on one or other for the circuit to work.

Task 5 - Clocked SR Latch

Upload to your logbook, the truth table, timing diagram and discuss the function of the clock, identifying any advantages/disadvantages with respect to the SR latch.

Clk	S	R	Q_{n+1}
0	0	0	No Change
0	0	1	0
0	1	0	1
0	1	1	Forbidden
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	Forbidden

Table 15

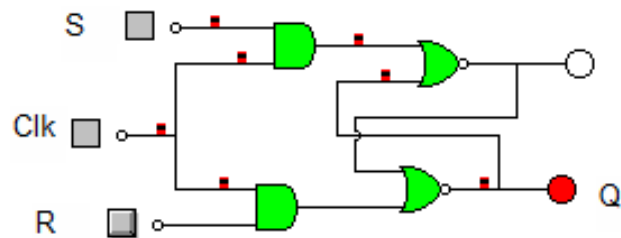


Figure 10 – Clocked SR Latch (Software)

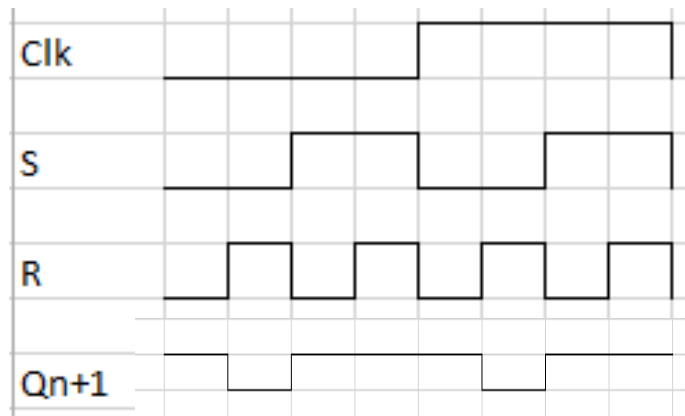


Figure 11 - Timing Diagram

This is the same with SR Latch, however it uses a clock. The purpose of the clock is to time what is coming in and going out. Whenever clock and S is on the process can continue, however if clock is off completely then a delay occurs until Clock is on. Also if clock and R is on, this will reset. Although if all 3 inputs are on, it will not do anything as it is forbidden. The problem with this circuit is that the data will keep on go through when clock is on and it will not send the data in an order.

Task 6 - Clocked D Latch

Upload to your logbook, the truth table, timing diagram and discuss any advantages/disadvantages of this circuit with respect to the clocked SR latch.

Clk	D	Q_{n+1}
0	0	No Change
0	1	1
1	0	0
1	1	Storing State

Table 16

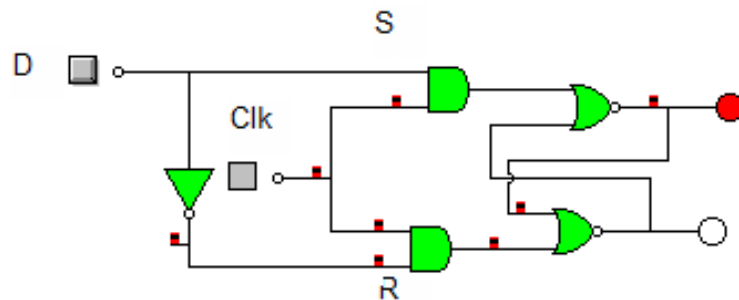


Figure 12 – Clocked D Latch (Software)

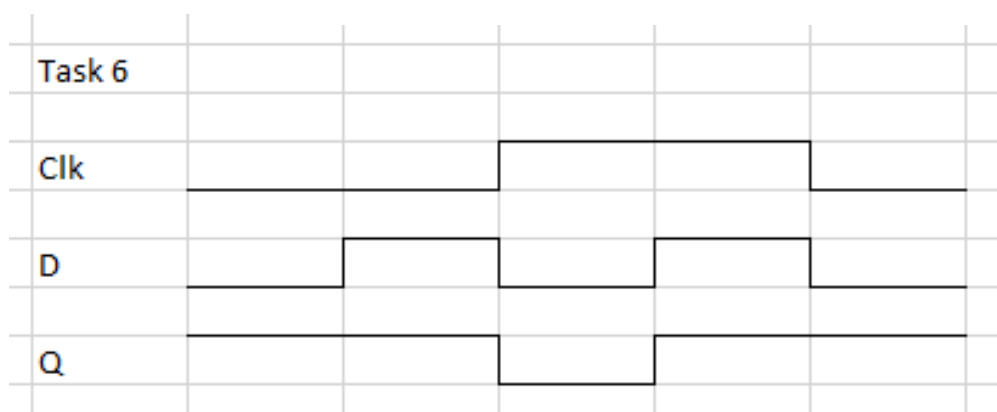


Figure 13 - Timing Diagram

Advantage

- Clocked D Latch are fast
- Clocked D Latch require less power

Disadvantage

- Less reliable due to the use of the clock
- Random results can occur

Task 7 - D Flip Flop

Upload to your logbook, the truth table and timing diagram. Apart from the preset and clear option on this device, state how this device's behaviour differs from the clocked D Latch above. With the aid of timing diagrams, discuss any advantages/disadvantage between the two.

Clk	D	Q_{n+1}
0	0	0
0	1	0
1	0	0
1	1	1

Table 17 - Truth Table

1. D-latch is a level Triggering device while D Flip Flop is an Edge triggering device.
2. The disadvantage of the D FF is its circuit size, which is about twice as large as that of a D latch. That's why, delay and power consumption in Flip flop is more as compared to D latch.
3. Latches are used as temporary buffers whereas flip flops are used as registers.

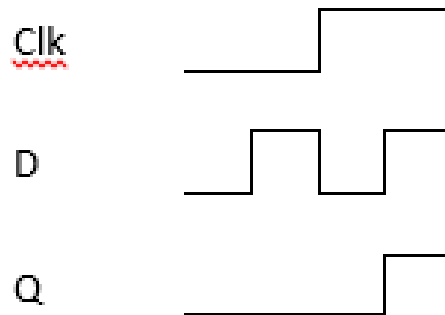


Figure 14 - Timing Diagram

Task 8 - Registers

Construct the circuit below and establish its functionality.

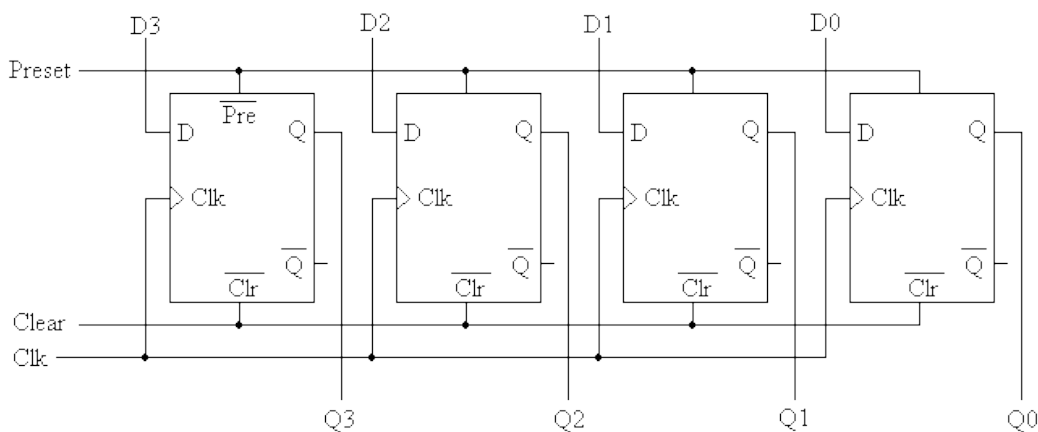


Figure 15 – Shift Register Circuit Diagram (Greenwich, 2016)

This circuit is employed and works within the CPU. This is a 4 bit registers that has four outputs with 4 inputs coming from each of the register. These registers stores temporary memory. Therefore, for it to be 4 bit, the limited capacity storage of the temporary memory will be up to 4. There are extensive lengths, but this circuits shows this.

It uses storage forms such as registers and memory. The flip flop depends on both input and output for it to work. Flip flops are connected parallel and they are opposite to a latch.

Task 9 - JK Flip Flop

Upload the truth table, timing diagram. With relation to the master slave arrangement of the circuit discuss the circuit's operation. Discuss where this circuit could be employed within a computer.

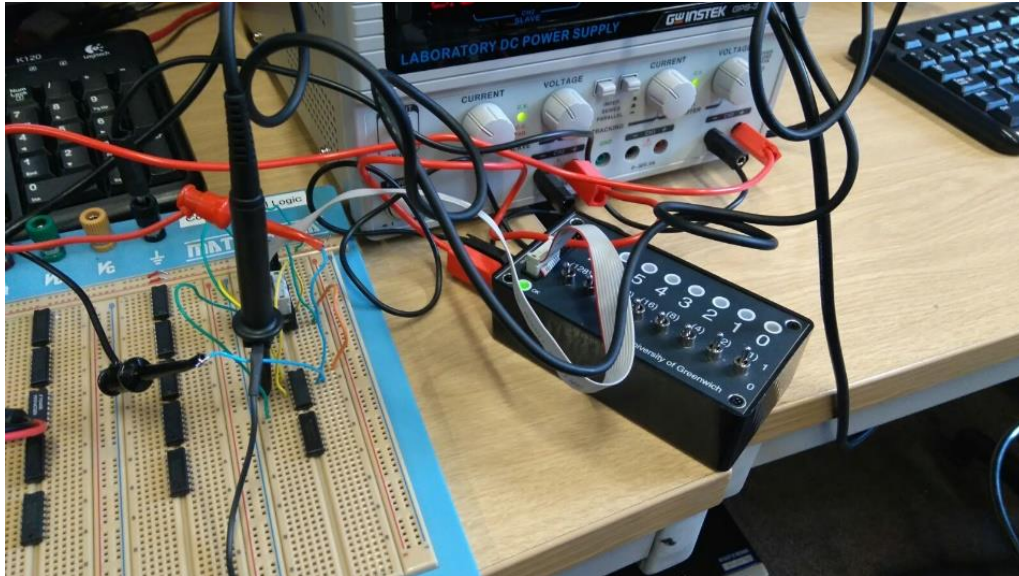


Figure 16 - Task 9 Breadboard and Switch Light Box

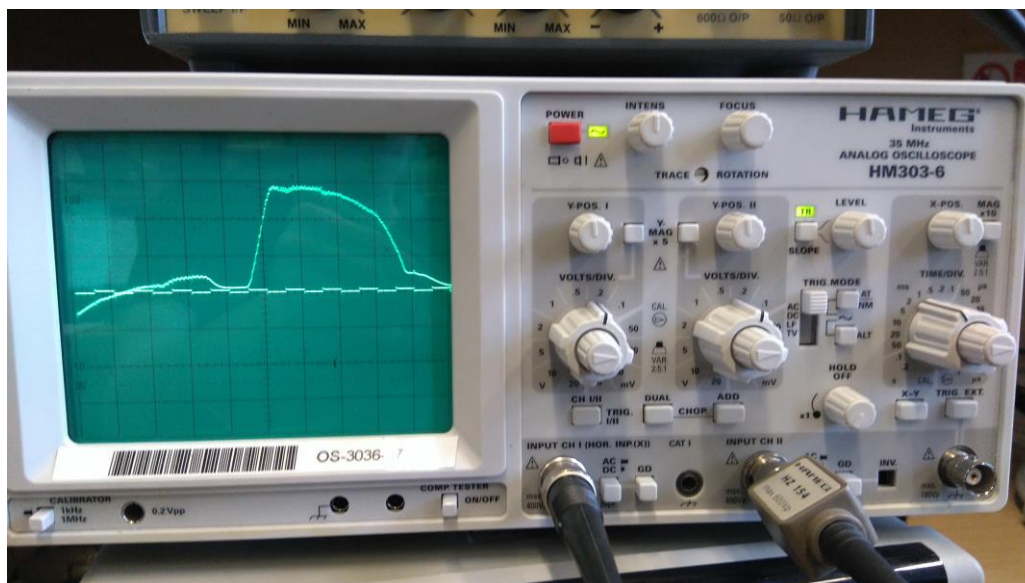


Figure 17 – Oscilloscope Display Q Output and Clock

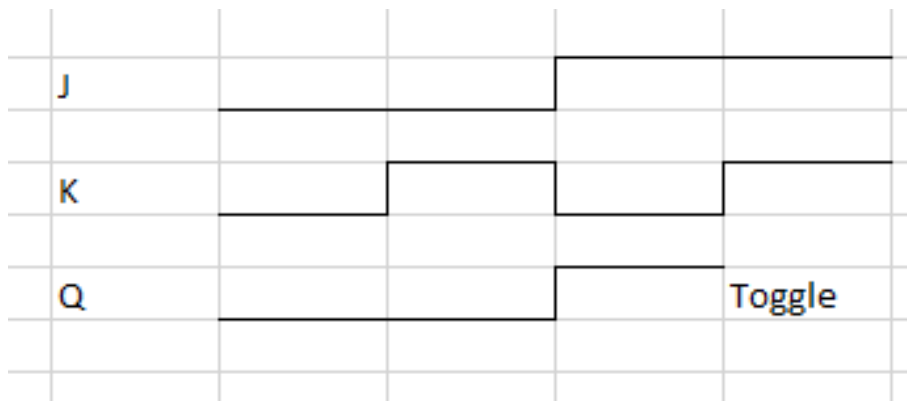


Figure 18 - Timing Diagram

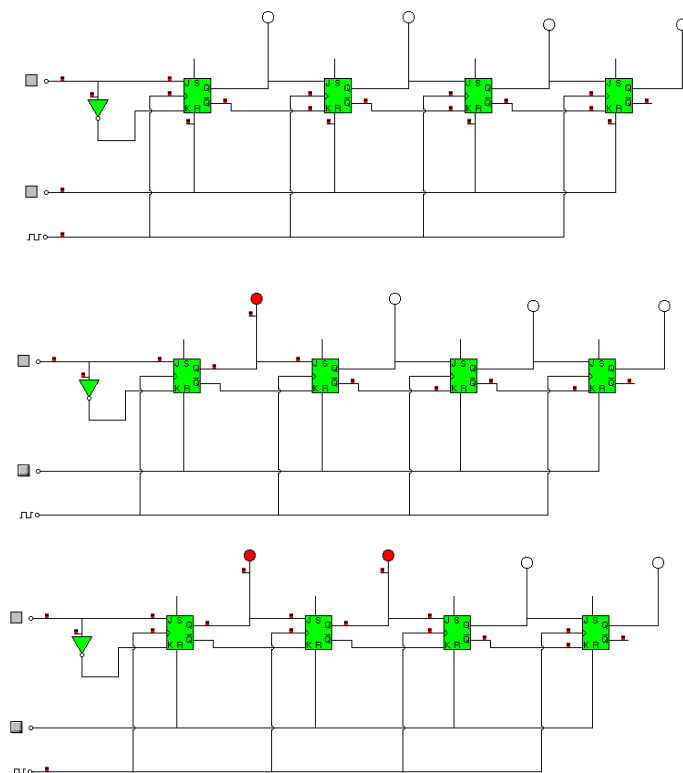
J	K	Q_{n+1}
0	0	No Change
0	1	0
1	0	1
1	1	Toggle

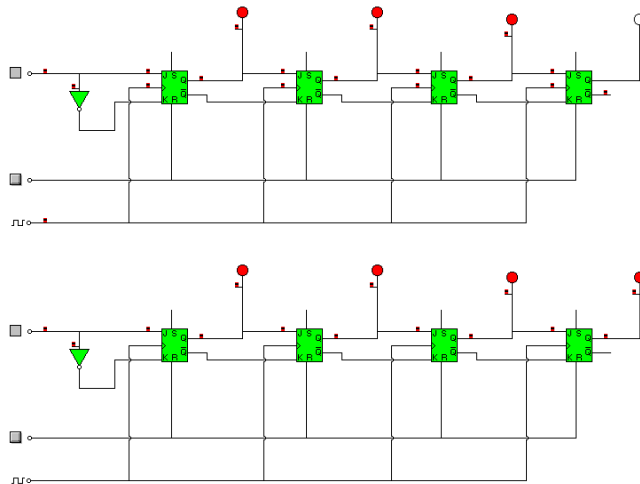
When J is set to 1, a value is stored in Q. When K is set to 1, the value in Q gets cleared so another value can get stored there. This circuit can be used as memory in a computer as it can be used as a storage device to store values such as bits.

Task 10 - Shift Register

Table 18 - Truth Table

What functions could this circuit perform? Discuss how this circuit could perform division by 2.





Shift register could be used as a circuit delay or as a converter from serial data to parallel data. Division by 2 can be done by shifting right one space and discarding the bottom bit. Shift registers are used as part of the CPU and ALU.

Task 11 - Binary Counter

Upload the timing diagram showing the relative relationship of the waveforms at Clk, Q0, Q1, Q2 and Q3. Discuss where this circuit could be employed within a computer.

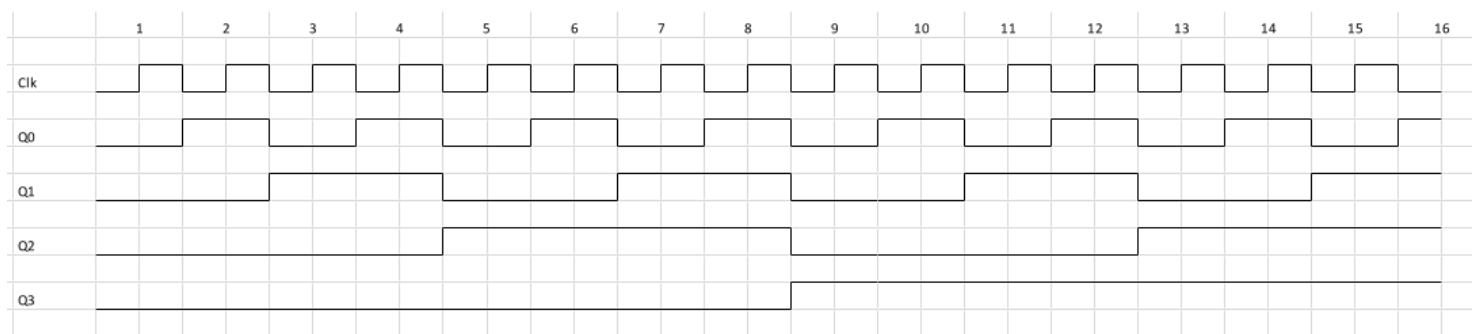


Figure 19 - Timing Diagram

The circuit can be used as a program counter in the CPU of a computer.

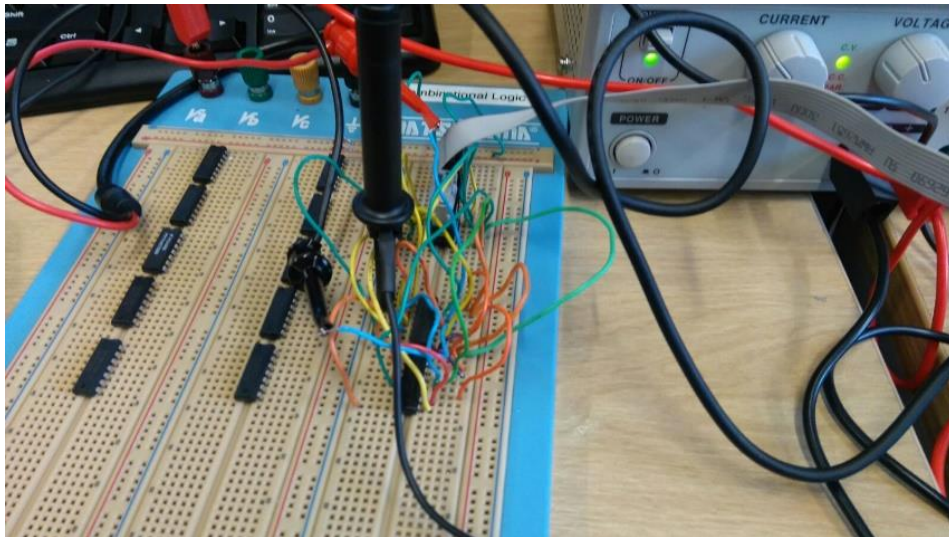


Figure 20 - Task 11 Breadboard

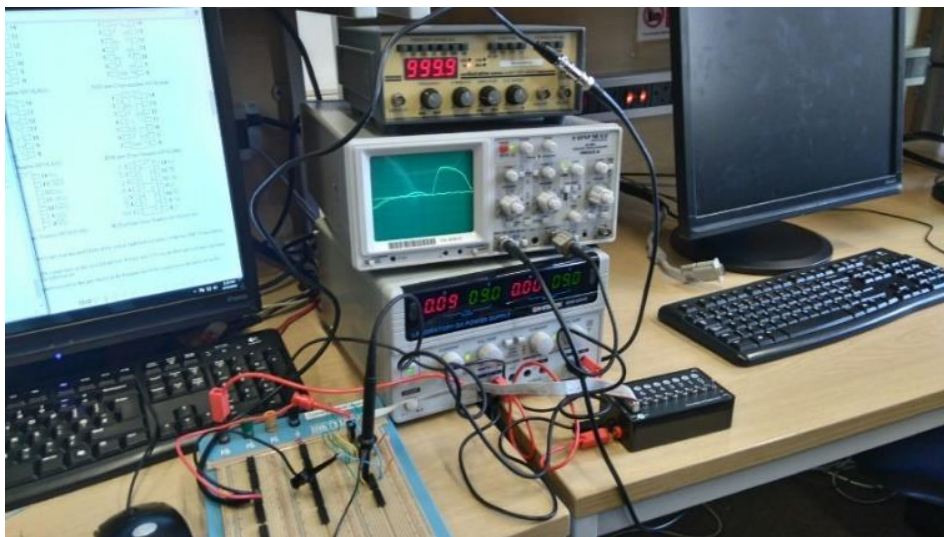


Figure 21 - Task 11 Overview

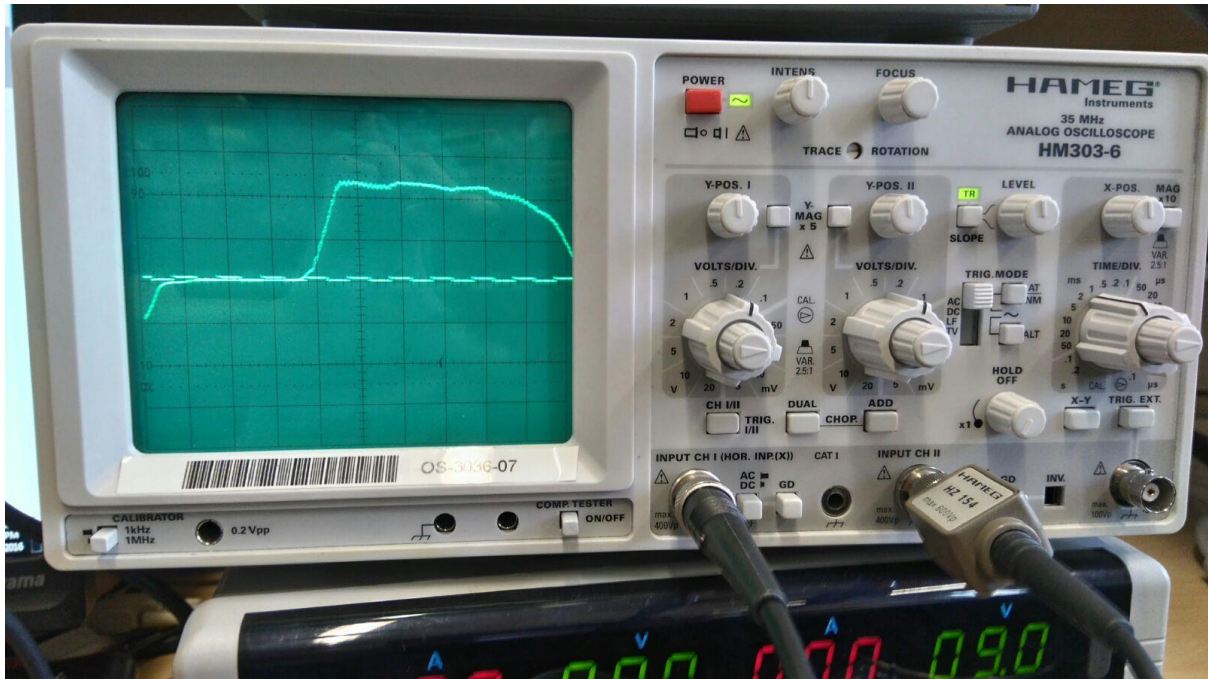


Figure 22 - Q0

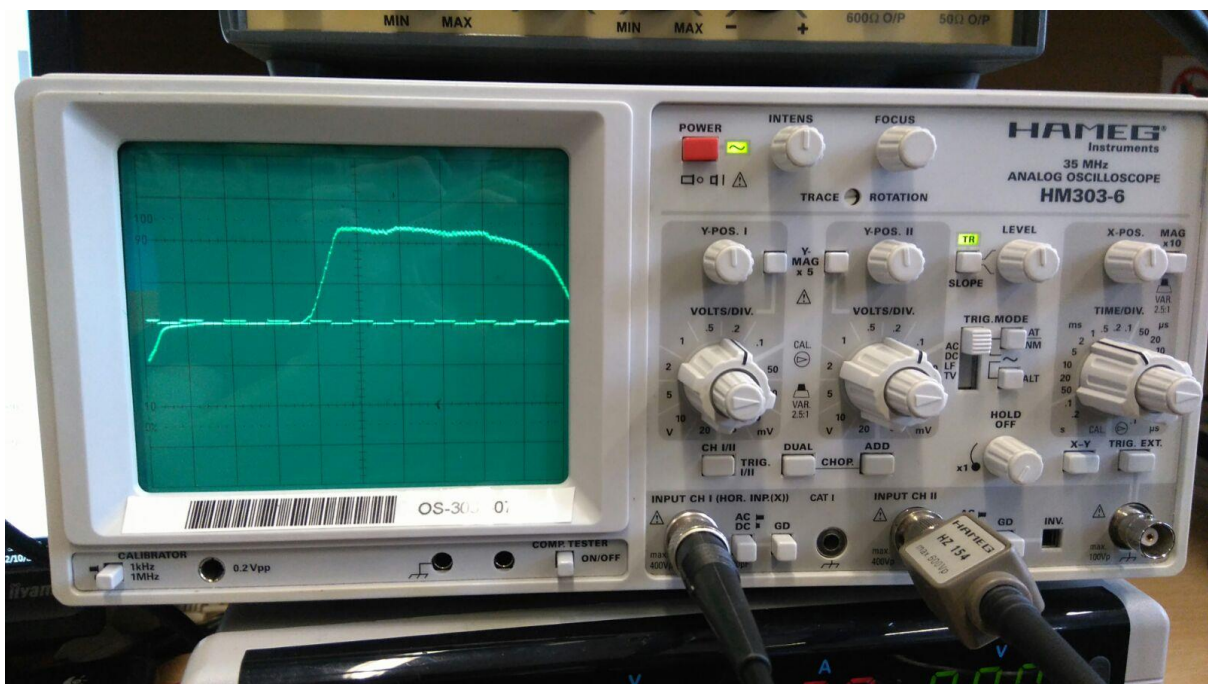


Figure 23 - Q1

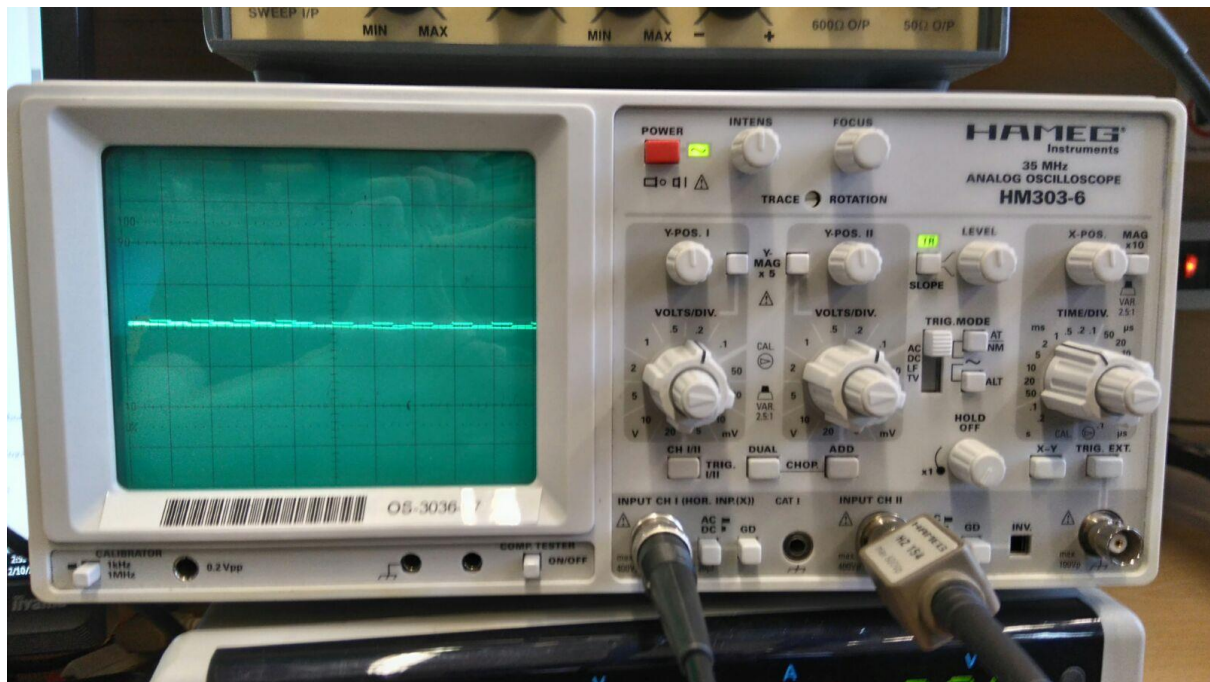


Figure 24 - Q2

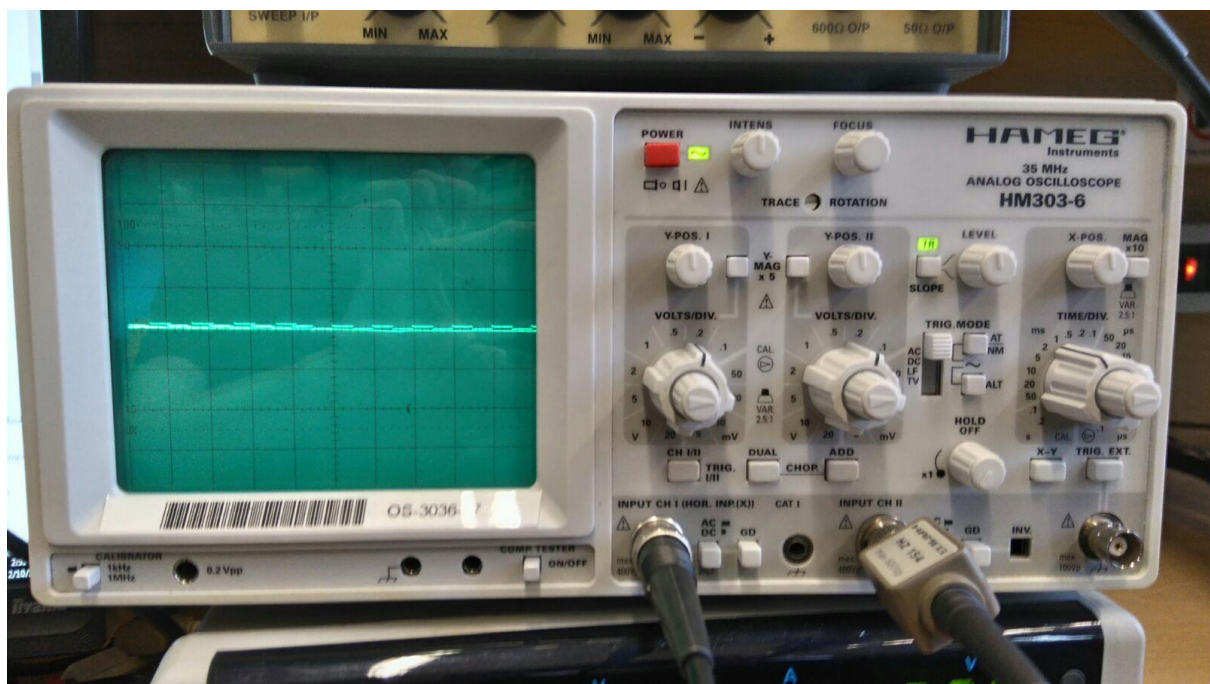


Figure 25 - Q3

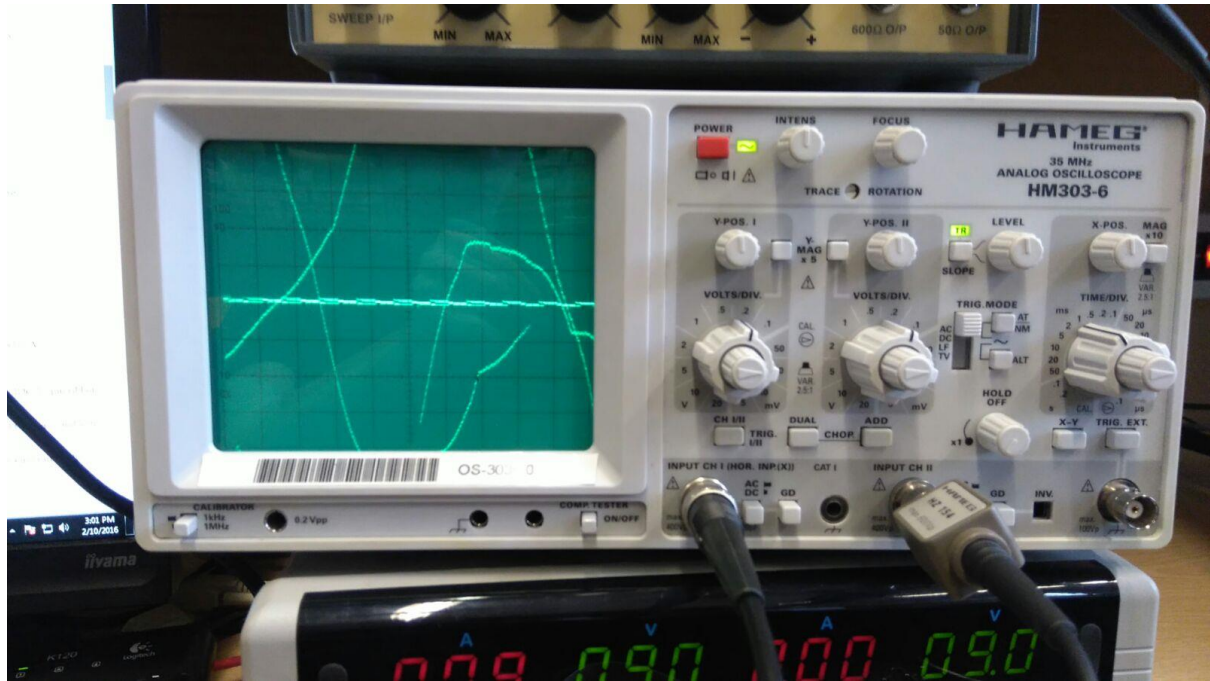


Figure 26 - Q0 Clear Switch ON

Task 12 - Reflection

By undergoing a laboratory session on logic gates, we were able to establish a basic understanding of how it all works.

For Task 0, first of all we connected DC power supply to our box with integrated circuits and we set the power supply to 9 Volts. Then we went through all possible combinations of two levers so 0011 and 0101 and we wrote down all outputs for circuits labelled A to F. After we completed this, we divided the table into smaller ones to have every integrated circuits with inputs separately so we can clearly see the Boolean formula and the logic gates. This exercise really helped us with differentiating between logic gates and showed how each logic gate looks like.

For Task 1, we were asked to demonstrate the physical built of the circuit given on a breadboard to the tutor and clearly illustrated the workings. As the truth table above on the results shows the output of the physical observation is the same as the software, calculation and crocodile clip. We tried to construct the circuit on crocodile clips software to ensure we get the right answer, which we did, to ensure we gave three examples of the circuit. We later called the tutor to ensure we did this correct and it was later confirmed we did. Once all three examples were complete, we compared notes. We later found out that each of our results were the same. This was very important to get the same results, because it would mean one of the parts we did was wrong. We found this task comfortable as we split each of the three parts to each of our group.

For Task 2, we were fairly given a real life example to produce a Karnaugh map and a truth table to understand the conclusion. We have finished truth table to show the workings and see the validity of the final answer. We backed this up with Karnaugh maps followed by the circuit diagram to indicate that all three workings lead us to the correct conclusion. We all did this as a group and we moved on to the next task.

For Task 3, we found this task the longest out of all. We had to do the Boolean equation, Karnaugh map, the physical part and the circuit diagram for this to be completed. We had completed the physical part of the task from before. However, we struggled with the Boolean equation and the Karnaugh map. This is because we read it differently. After going through the notes repeatedly, we found the mistakes that we were doing only on the map. However, once we completed the map, we had to make the Boolean equation with the circuit diagram on Crocodile Clip. We did the Boolean equation by looping together two of the nearest ones and the other two. Once this was complete, we struggled to do the circuit diagram as once we tested it; it was wrong. We did it again using the same Boolean equation and it worked. This task required in-depth hours of work to complete. We did this by taking out our own time to complete this very task.

For Task 4, we had to fill in the truth table. To do this, we recreated this on Crocodile Clip software to fill it in. We noticed that on the lecture notes, some rules occurred. We followed the rules that were given and filled the diagram. We also completed the timing diagram too.

For Task 5, we had to do the same concept of completing the truth table and timing diagram. By going to the lecture, we knew how to do the timing diagram. However, for this, we had to name the advantages and disadvantages of the SR latch. We did some research based on it and got some answers to complete this task too.

For, Task 6, it was the same concept as Task 5, however it used a Clocked D latch. We also had to complete the truth table and timing diagram. Again, by going to the lecture, we knew how to complete this task straight away. We found these tasks that had the same concept very easy as it was covered during the lecture.

For Task 7, we noticed that we did the rule of using first two zeros and the last two ones. We noticed that when both of the inputs are on, the output is only one. We found this task comfortable, because it required us only to complete the task by only filling in the truth table with the timing diagram and advantages and disadvantages. We did all these tasks as quickly as possible as we all knew that we had to complete all of them before the deadline.

For Task 8, all we had to do is discuss what the circuit did and where it was employed within the computer. This was comfortable as it was a four bit register. We had to explain what the circuit did as shown above. To improve this task, we can add the advantages and disadvantages of its uses.

For Task 9, we had to construct a JK Flip Flop circuit in crocodile clips and fill out the truth table given in the lab guide. After this, we started to connect it all together physically by using a function generator to give a clock signal and an oscilloscope to show the output of the circuit. We used the JK Flip Flop chip already given to us on the breadboard, jumper wires were used to connect it all together. The circuit on crocodile clips was compared with the results on the physical circuit which was previously connected with the lights on the switch light box and results were correct. We then output the Q signal to be displayed on the oscilloscope and then took pictures of the results which is shown in Figure 17. This task was quite simple, as we didn't have to create the JK Flip Flop ourselves, all we had to do was input the J and K input and clock to the JK Flip Flop chip on the breadboard.

For Task 10, we recreated shift register in crocodile program by adding 4 J-K Flip-Flops, a clock one input for clear and one input for data and 4 parallel outputs. Then we tested and make sure it works like it supposed to we figured out that this circuit could be used as a delay for the rest of the circuit or a serial to parallel data converter and division by 2 could be done by shifting right and discarding the bottom bit. To improve this task, we can gather a truth table out of this. This would extend this even better and interesting.

For Task 11, we had to take the previous circuit made in Task 9 and make four JK Flip Flops connected to each other where the Q is connected to the next clock and the \bar{Q} is the output to show on the oscilloscope along with the clock signal from the function generator. On the breadboard, there was two JK Flip Flop chips which made a total of four circuits. Like in Task 9, the circuit was connected with jumper wires and tested with the switch light box to see if the circuit is properly configured. After this, we then took pictures of Q0-3, outputting each signal one at a time along with the clock signal which displayed on the oscilloscope, this is shown in Figures 22 to 26. This task was just an extension to Task 9 so not much extra had to be done, it was just connecting more jumper wires accordingly to the diagram given in the guide.

Overall, I think we worked well as a team. Especially when it got really hard at the end, we all took our time to make it work. We were motivated to complete all the tasks and the positive attitude enabled us to complete the work.

Conclusion

In conclusion, we have learnt a lot of skills during this laboratory and got a lot of experience in using the breadboard, which in future, we would be really good at the next time we use it.

References

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