OR Gate:-

> Apparedus:

Bread board

· Cutter

Single core wire

Pair of Strippers

IC of OR gate

=> Objective:

→ Use IC of OR gate to perform the operation

→ Write the truth table of OR gate

=> Procedure:

-> Connect the trainer board with power supply

→ Place the corresponding IC 74LS32 on the

board

-> Connect pin 14 to +SV and 7 to GND

-> Connect pin 1 and 2 to two switches for input 3 to LED for output.

→ Give the input through switches according to the truth table and check the output.

=> Conclusion:

OR gate, generates high output when at least one input is high and even generates high output when both inputs are high

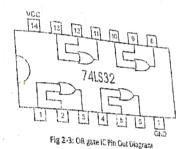


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Truth Table:

Input	Table 2-1	
A		
0	B	Output
1	1	0
	10	1

pin Configuration:



To check the operation of AND gate according to the AND's truth table, using the IC 74LS08

Theory

A Logic AND Gate is a type of digital logic gate that has an output which is normally at logic level "0" and only goes "HIGH" to a logic level "1" when ALL its inputs are at logic level "1". The output of a Logic AND Gate only returns "LOW" again when ANY of its inputs are at a logic level "0". The logic or Boolean expression given for a logic AND gate is that for Logical Multiplication which is denoted by a single dot or full stop symbol, () giving us the Boolean expression of:

A.B = Q

Equipment Required:

• - 74LS08

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AND Gate:-

Apparatus:

- Bread board
- Cutter
- Single core wire
- Paix of strippers
- IC of AND gate

- Use IC of AND gate and perform the operation.
- Write the truth table of AND gate

Procedures-

- Connect your trainer board with power supply using single cose wise
- -> Place the cossesponding IC 74LSOB on the board
- Connect pin 14 to tSV and pin 7 to GND.
- Connect pin 1 and 2 with 1st two switches for input and 3rd one with LED for output.
- -> Give the input through switches according to the truth table and check the output.

Condusion:-

AND gate, generales high output when both inputs age high otherwise the output value is low



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symbolic diagram:



Fig 2-4: And Gate Diagram

pin Configuration:

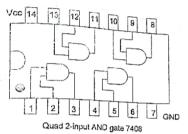


Fig 2-5: And Gate IC pinout

Truth Table:

Table 2-2

Input	18 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Output
A	В	Q
0	0	D
0		0
1	Đ	0
1	1	

To check the operation of NOT gate according to the NOT's much table, using the IC 74LS04.

The output of NOT gate is opposite to its inputs. It is also called an inverter because it inverts the input signal. It has one input and one output. All it does to invert (or complement) the

Bread board

Cutter

Pair of Strippers

Single core wire

IC of NOT gate

Use IC of NOT gate and perform the operation Write the truth table of NOT gate.

Procedure:-

Connect the trainer board with power supply.

Place the corresponding IC 74LSO4 on the board.

Connect pin +1416 with +5V and 7 with GND.

Connect pin 9 with switch and 8 with LED.

Give the input values according to the truth table

and check the output.

Conclusion:-

NOT gate, we have only one input and one output. The value of output is negation of input, if value of input is one, the value of output must be zero and



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_{Equipment} Required:

74LS04

Symbolic diagram:

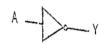
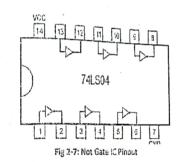


Fig 2-6: Not Gate Diagram

_{pin Configuration:}



Truth Table:

di no

Table 2-3		
laput	Output	
A	Υ	
0	11	
1	0	

To check the operation of NOR gate according to the NOR's truth table, using the IC 74LS02

It is a NOT-OR gate. It can be obtained by connecting a NOT gate in the output of an OR Theory:

gate as shown in fig. Its output is given by the Boolean equation.

$$C' = (A+B)'$$

It gives an output when it is both inputs are 0.

Bread board

Culter

Single core wire

IC of NOR gate

=> Objective:

Use IC of NOR gate and perform the operation

Write the truth table of MOR gate

Procedure:

Connect the trainer board with power supply

Place the corresponding IC 74LSO2 on the board

Connect pin 14 with +SV and 7 with GND

Connect pin 11 and 12 with two switches for input

and 13 with LED for output

Apply the combination of input and check the output

=> Conclusion:

- NOR gate, we have two inputs and one output The value of output is high, if both values of input are low otherwise, in remaining cases, the values of output must be low.

NOR gate is negation of OR



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Equipment Required: 74I.S02

symbolic diagram:

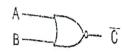


Fig 2-8: NOR Gate Diagram

pin Configuration:

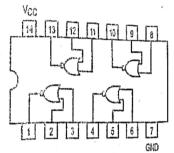


Fig 2-9: Nor Gate Diagram

Truth Table:

34.14

Table 2-4

Input	Clark Refuse	Output
A Company	B 11	C.
0	0	
-	1	
	0	0

To check the operation of NAND gute according to the NAND's truth table, using the IC 74LS00

It is in fact a NOT-AND gate. It can be obtained by connecting a NOT gate in the output of an AND gate as shown in fig. its output is given by the Boolean equation.

- Bread board
- Cutter
- Single Core wire
- IC of NAND gate

Objective:

- Use the IC of NAND gate and perform the operation white the truth table of NAND gate

Procedure:

- -> Connect the trainer board with power supply.
- Place the corresponding IC 74LSDO on the board.
- Connect pin 14 to tSV and 7 to GND.
- Connect pin 1 and 2 to two switches for input
- Give the input through switches occording to the truth table and check the output.

Conclusion:

NAND gates we have two inputs and one output. The value of output is low when both inputs are high otherwise, in remaining cases, The value of



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Q'=(A.B)'

This gate gives an output high if either A or B or both are 0.

Equipment Required: 74LS00

Symbolic diagram:



Fig 2-10: NAND Gate Diagram

_{Pin Configuration:}

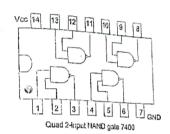


Fig 2-11: NAND Gate IC Pinout

Truth Table:

Table 2-5

Input	1.37	Output
Δ	В	Q'
0	0	1_
0	1	1
	0	11
	Ī	0_

To check the operation of KOR gate according to the KOR's truth table, using the IC 74LS86

It is the gate which gives an output I when its inputs are not same (or exclusive) and anoutput0 when its inputs are same. Its symbol is shown in fig.

Bread board

Cutter

Single core wire

IC of XOR gate

Objective:

Use IC of XOR gate and perform the operation.

Write the truth table of XOR gate

Procedure:

Connect the trainer board with power supply

Place the corresponding IC 74LS86 on the board

to LED for output.

Give the input through switches according to cheek the output.

Conclusion:

XOR gates gives an output only if inputs are dissimilar, means if and other



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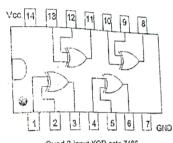
_{Equipment} Required:

74LS86

Symbolic diagram:



_{Pin Configuration:}



Quad 2-input XOR gate 7486 Fig. 2-13: XOR Gate IC Pinout

Truth Table:

Table 2-6

		Chaput
Input	T D	X
A		0
0		
0		1
		0
14-11		

Experiment NO 3

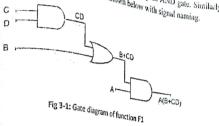
- Apparadus:
- Single core wire

- Procedure:

- Connect 7 and 14 pin of each IC to and 15V respectively through power supply. Give input C,D to AND gate and pa
- Take another input B. Apply OR operation on B
- the output of OR operation along with and perform AND operation.
- Conclusion:
 - Conclusion in given in the

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term in function is product term that is represented by an AND gate. Similarly, OR CD term in Adexail logic diagram shown below with signal naming.



- Connect the trainer board with the power supply.
- Mount the corresponding 74LSXX IC on the board
- Mount the circuit according to the diagram by consulting the corresponding gate ICs
- Apply all the combinations of inputs and observe the output on the LED.
- Fill the truth table according to your observation.
- Draw Circuit 1 in Logic works and obtain its Truth table for all possible combination.
- Draw second reduced circuit in logic works and obtain its truth table.
- Compare truth table to verify both circuits.

		lati	e 3-1	
A	B	C	.D	A(B+CD)
υ	0	0	0	. 0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
Q	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
	0	1	0	0
$-\frac{1}{1}$	0	1	1	
	1	0	0	
	1	0	1_	!
1			Λ.	1

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Experiment No 4

- Apparatus:

- Procedure:
- to expression

$$F = \overline{X}\overline{Y}\overline{Z} + \overline{X}Y\overline{Z} + XY\overline{Z} + XYZ$$

- Take a note of outputs for different inputs
- Now place ICs and single core wires for

- Cross cheek the outputs with previous outputs
- Conclusion:
 - Conclusion is shown in troth table



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Experiment#04

GATE LEVEL MINIMIZATION OF BOOLEAN FUNCTION USING POSTULATES

- The need of gate level minimization
- Understand the K-Map method

gackground Theory Gate-level minimization refers to the design task of finding an optimal gate-level implementation of squares, with each square representing one mindows of squares, with each square representing one mindows of squares. simple, States, with each square representing one min-term of the function. A K-map is a diagram pade up of squares, the user can derive alternative simple alorbraic and function. By recognizing nude up of square min-term of the function. By recognizing one min-term of the function. By recognizing pattern, the user can derive alternative simple algebraic expression for the same function.

Equipment required.

- 74LS32 NOT OR
- 74LS08
- EPAL 27
- Cutter
- Single Core Wire
- Pair of Strippers

Lab Task

Simplify the following Boolean Expression using K-Map.

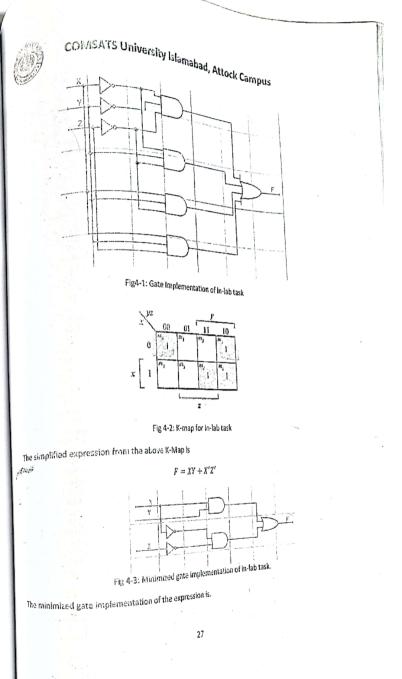
$$F = X'Y'Z' + X'YZ' + XYZ' + XYZ$$

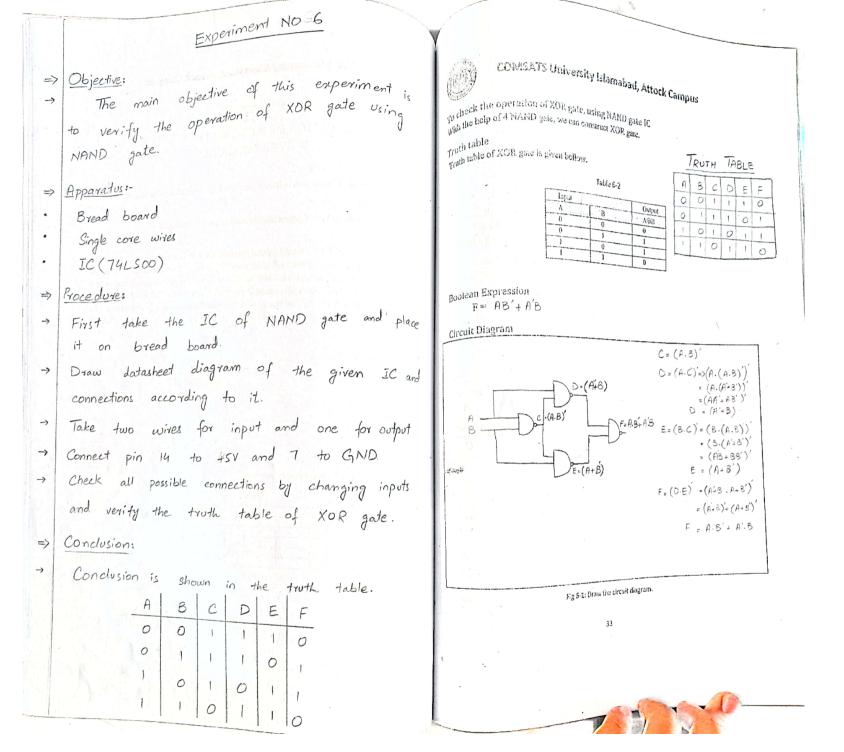
The gate implementation of the above expression is given below.

TRUTH TABLE

_								XYZ	XYZ	XYZ	
	X	Y	2	X	7	2	XYZ		0	7/2	0,1
1	5	0	0	1	1	1	11	0			1
		0	1	,	1	0	0	0	0		0
1				M G	0	1	0	70,04 (3s)	0	0	
	0		0		0		0	0	0	0	
(0		1	1		0	0	0	0	0	0
	1	0	0	0	'		0		0	D	0
	1	0	1	0	1	0	0	0	accinini.		0
-	(1	0	0	0	1	0	0	Sance of the last	0	
	1	1	1	0	0	0	0	0	0		

XY	ΧZ	XY+XZ
0	1	
0	0	0
0		
0	0	0
0	0	0
0	0	0
0	0	
	0	1.





Experiment No 7

Objective:

The main objective of this experiment is to verify the operation of half adder

- => Apparatus:
- · Bread board
- · Single core wites
- · Cutter
- · IC 74LS86 (XOR)
- · IC 742 SO8 (AND)
- => Procedure:
- → Take the ICs of AND and XOR gate
- → Install them on breadboard
- Take two wires for input and one for output for each IC
- → Make the connections of input wires of both ICs
- of both ICs
- → Check all possible connections and verify the truth table.
- => Conclusion:
- -> Conclusion is shown in the truth table.

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ph rabble in the specifications of Half-adder give above, fill in a truth table containing all phile combinations of two 1-bit inputs and the resultant values of sum and carry.

	Table 7-1			
Inputs		Outputs		
B	A	Sum		
0	0	0	Carry	
0	1	-	0 .	
1	0	+	0.	
1	1	+	0	
		10		

 $Sum, S = A \oplus B$ Carry, C = A.B

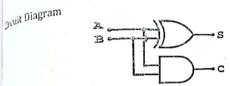


Fig 7-1: Half Adder circuit diagram

A full adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two of the input variables, denoted by x and y represent the two significant bits to be added. The third input, z, represents the earry from the previous lower two significant position. Two outputs are necessary because the arithmetic sum of three binary digits' significant position. Two outputs are necessary because the arithmetic sum of three binary digits' naive sin value from 0 to 3, and binary 2 or 3 needs two digits. The two outputs are designated by the symbols S for sum and C for carry. The binary variable S gives the value of the least significant bit of the sum.

Equipment Required:

- 74LS08 (AND)
- 74LS86 (XGR)
- 74LS32 (OR)

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Experiment No 8

=> Objective:

->

->

 \rightarrow

The main objective of this experiment is to verify the operation of full adder

Apparatus:

Bread board

Single core wires

Cutter

IC 74LS86 (XOR)

IC 74LSOB (AND)

IC 74LS32 (OR)

Procedure:

Take three ICs of XOR, AND and OR gates

Install them on bread board

Take two wires for input and one for output

for each IC

Make the connections of input wires of all IC,

Connect pin 14 to 15V and 7 to GND of all IC.

Check all possible connections and verify the

Conclusion:

Conclusion is shown in the truth table

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table ight of the specifications of Full-adder give above, fill in a truth table containing to possible combinations of two 1-bit inputs, a carry in (or a third input) and the resultant of sum and carry.

Table 8-1

Inputs	В	A	Outputs	
0	0	0	Sum	Carry
0	0	1	_ 5	0
	1	0		0
	1	1		0
	0	0	_ 0	
	0			0
<u>i</u>	1	1	0	
	1	0	0	
1	11	1	i i	1

S= A @ B @ C

C=A B + B Cin + A Cin

Circuit Diagram

Buch

