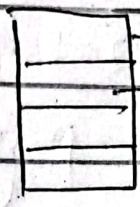
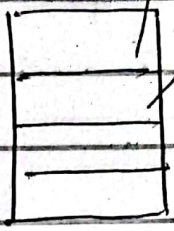
Translation Lookaside Buffer (TLB):-

Paging Concept

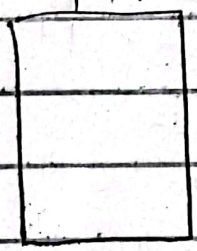
We divide process into pages



alag alag process k pages ko ly k aadkay hai main memory mai



inside the main memory, which is already divided into frames

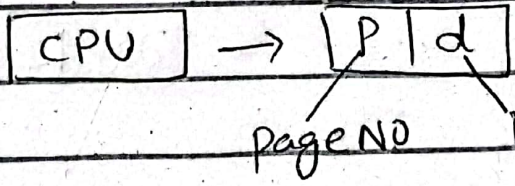


PT → physical address

Page Table.
as like as index.

Kn sa page no kis frame address pr prha hai

CPU generate logical address.



⇒ Kn sa page kis frame mai hai that is physical address.

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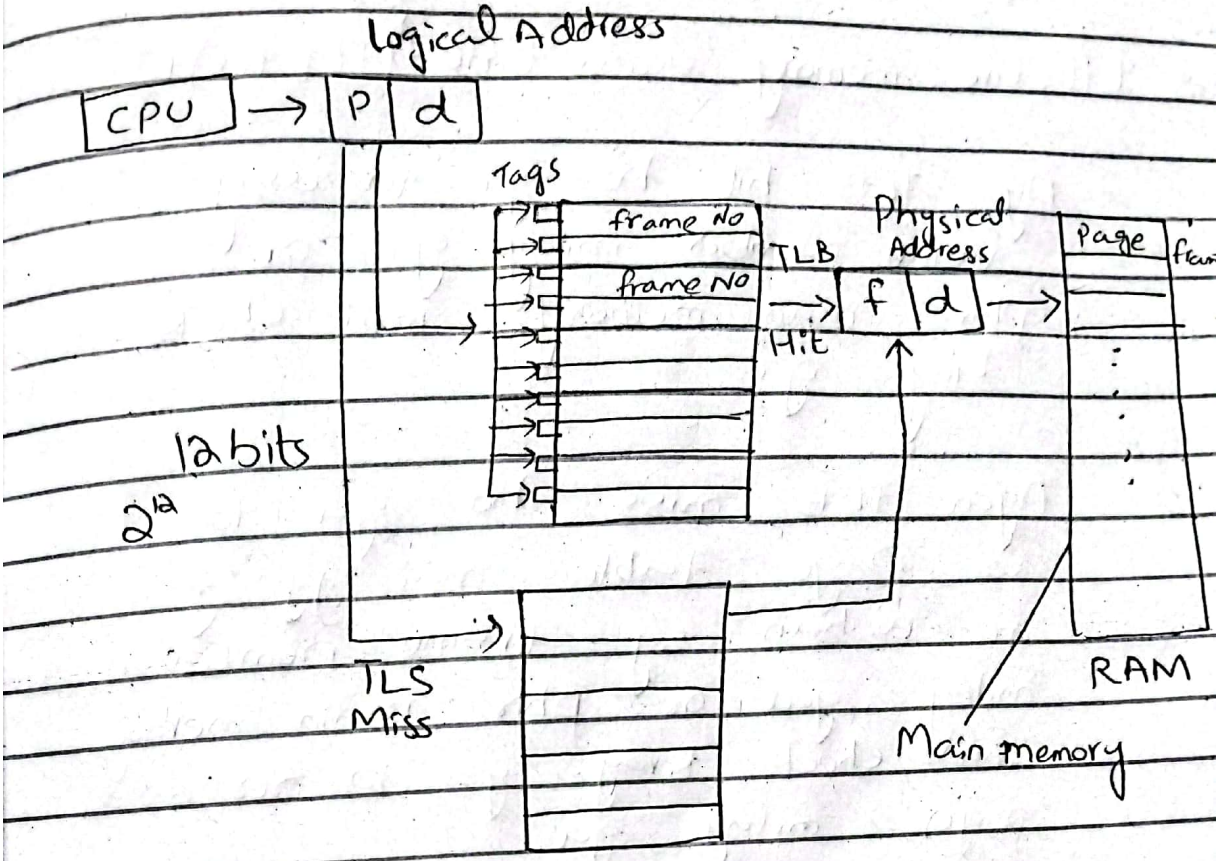
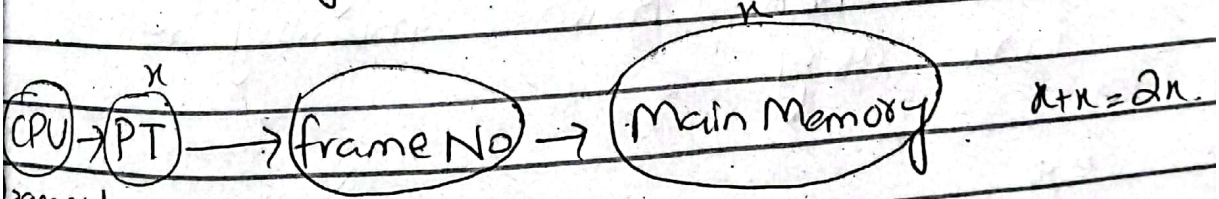


e.g; Main memory ko excess krnay ka time x hai
So how many times for accessing?
No page fault occuring



TLB faster than RAM.
↓
Buffer
↓
Cache.
frame Numbers in TLB (cache)

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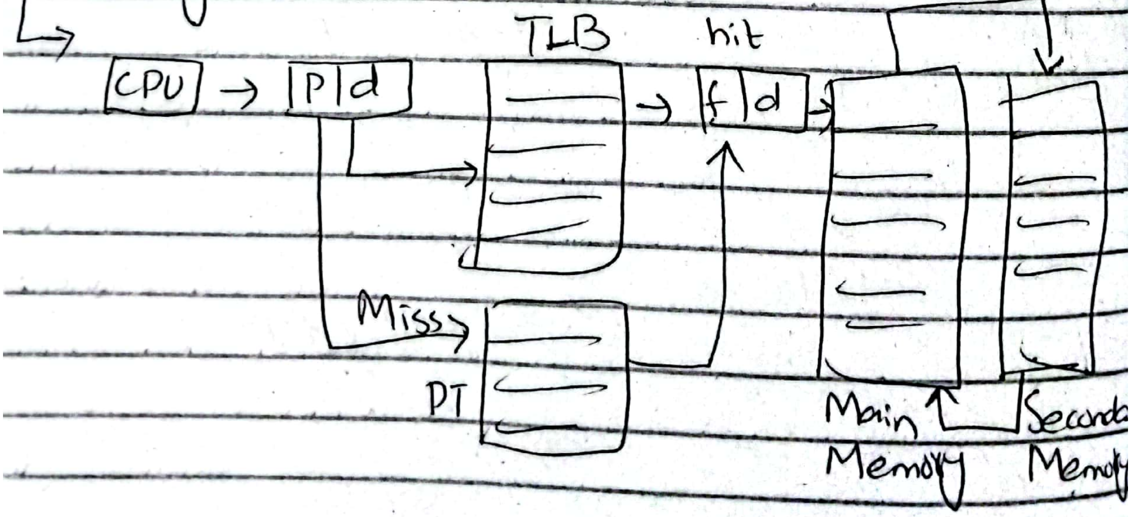
⇒ Effective memory access time = $^{Hit}(TLB + x) + ^{Miss}(TLB + x)^{k}$

Agar TLB hit ho ga to usay frame Number milay ga or phir main memory mai check kray ga.

Agar TLB miss ho ga to vo page table mai jye ga or wahan sy frame number milay ga or phir main memory mai check kray ga, to perticular page milay ga.

Page fault service time k liye philay secondary memory main jana then main memory mai lana usay.

eg.



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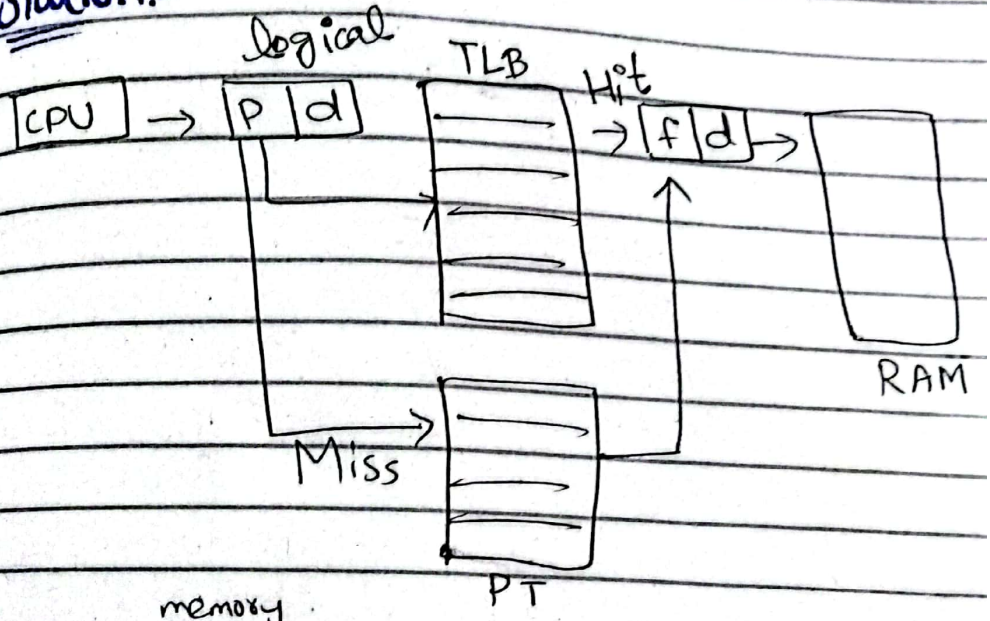
Numerical.

Question No #1.

A paging scheme using TLB. TLB access time 10 ns and main memory access time takes 50 ns. What is effective memory access time (in ns) if TLB hit ratio is 90% and there is no page fault.

Solution:-



Effective Access Time = Hit (TLB + Main Memory) + Miss (TLB + PT + Main memory)

1 - hit = Miss ⇒ 100 - hit = Miss

EAT = 90% (10 + 50) + 10% (10 + 50 + 50)

$= \frac{90}{100}(60) + \frac{10}{100}(110)$

54 + 11 ⇒ 65 ns.

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