

# Power Semiconductor Devices: Basics

Mar 18, 2019 at ICMTS

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 Kyushu Institute of Technology  
 Japan

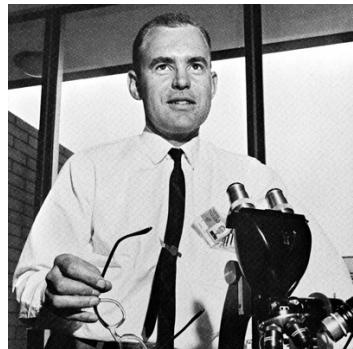
# Outline

- **Introduction**
  - History
  - Power electronics circuit
- **Power semiconductor devices**
  - Power MOSFET / Super-junction MOSFET
  - IGBT
  - Thyristors
  - Lateral devices
- **Future possibility**
- **Related technology**

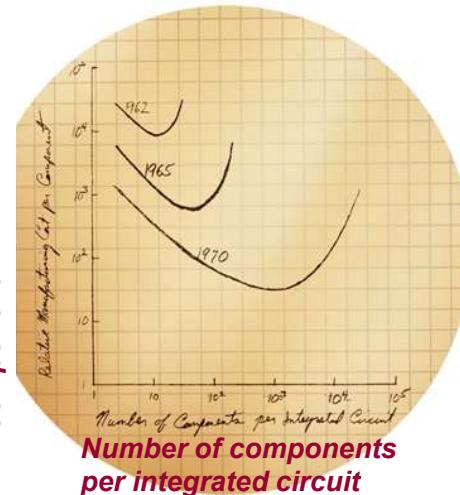
# 1965 - "Moore's Law" Silicon Engine to drive ICT



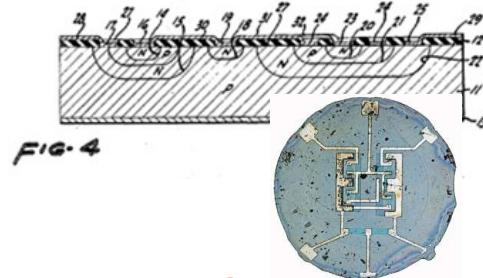
Gordon E. Moore



*Manufacturing cost per component*



Integrated circuit patent in 1959



Robert Noyce

To digital cost free => ICT for everybody

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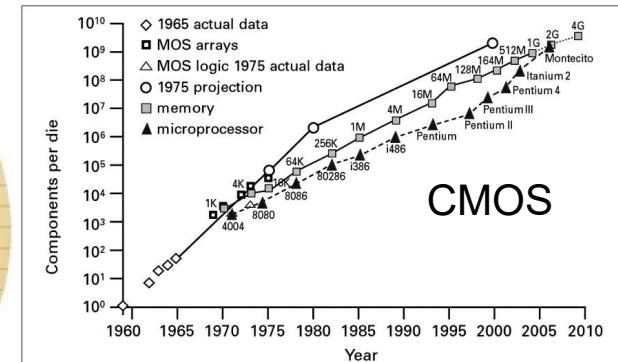
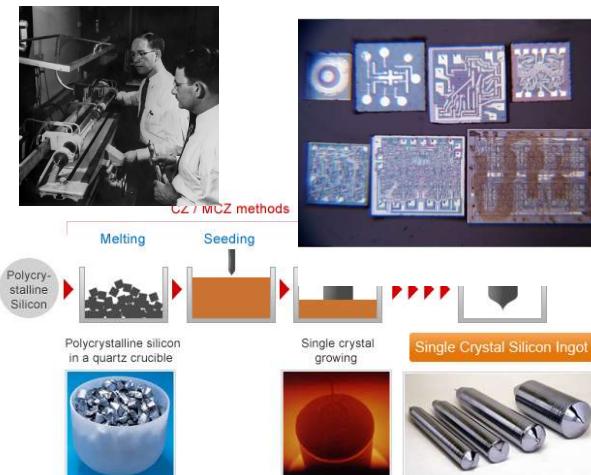


FIGURE 9. Integrated circuit complexity, actual data compared with 1975 projection. Source: Intel.



# AC power distribution system



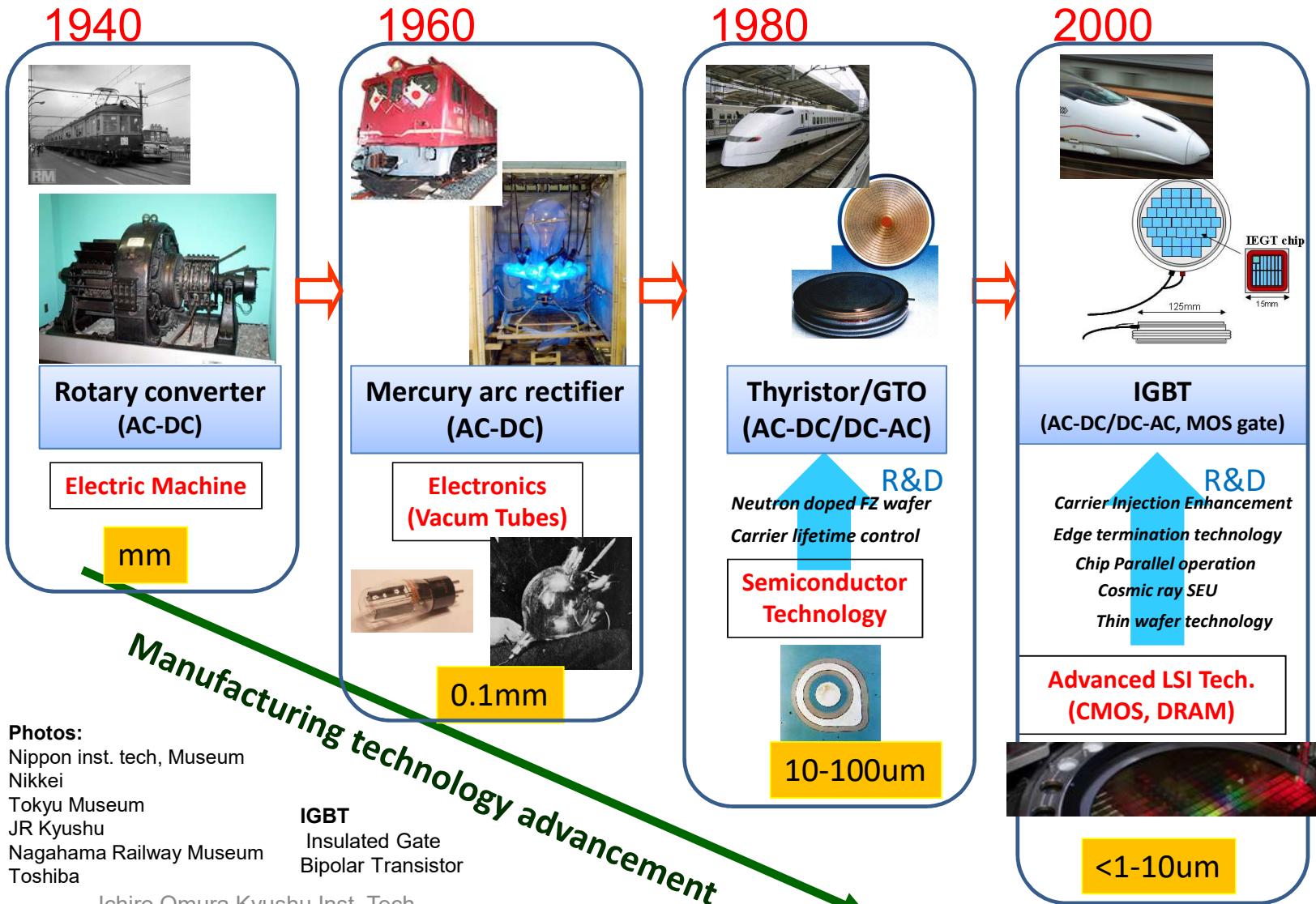
[transm.web.fc2.com](http://transm.web.fc2.com)



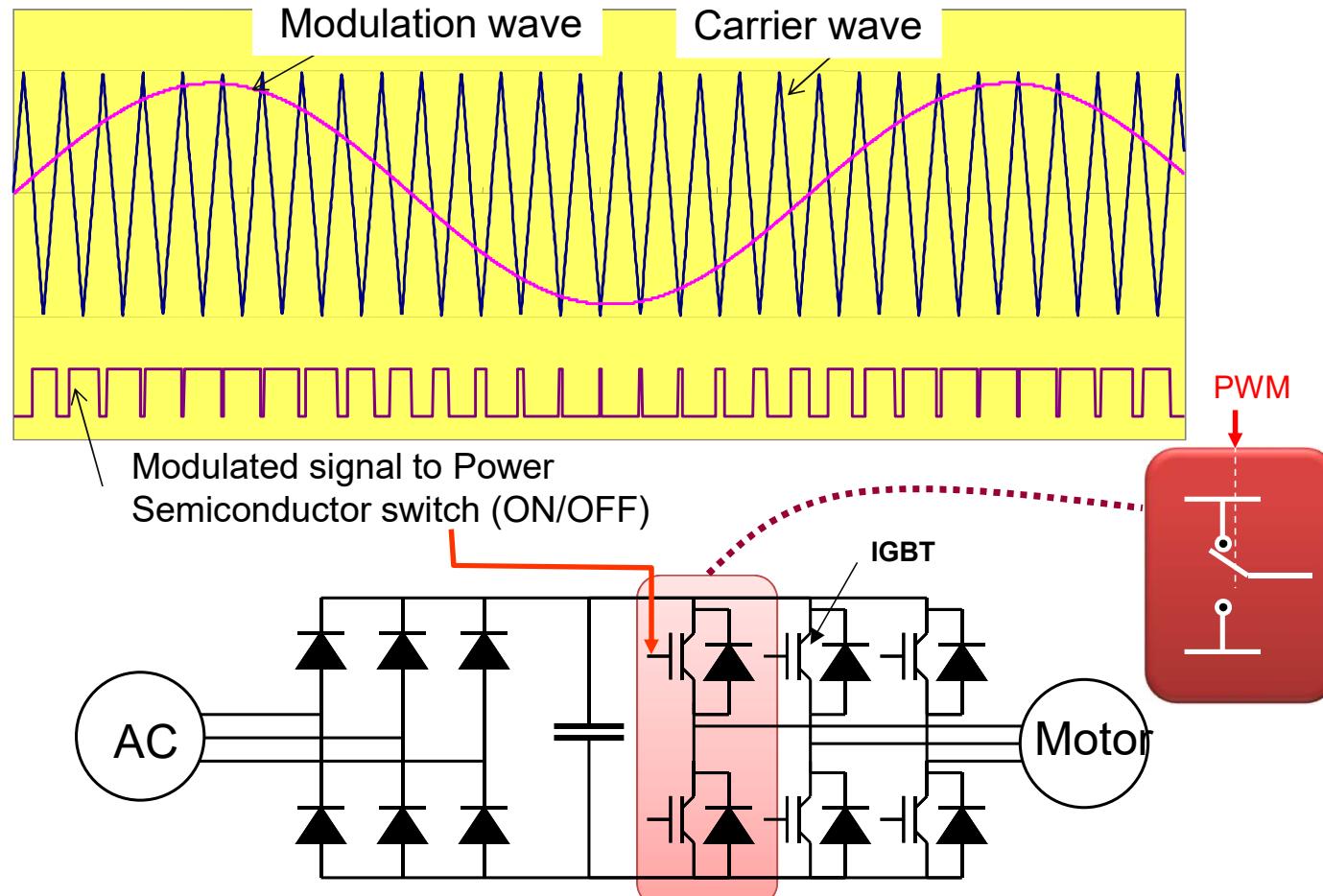
[www.cz-toshiba.com](http://www.cz-toshiba.com)

AC to AC  
Constant frequency  
No active control function

# 100 years of power device development (High voltage)

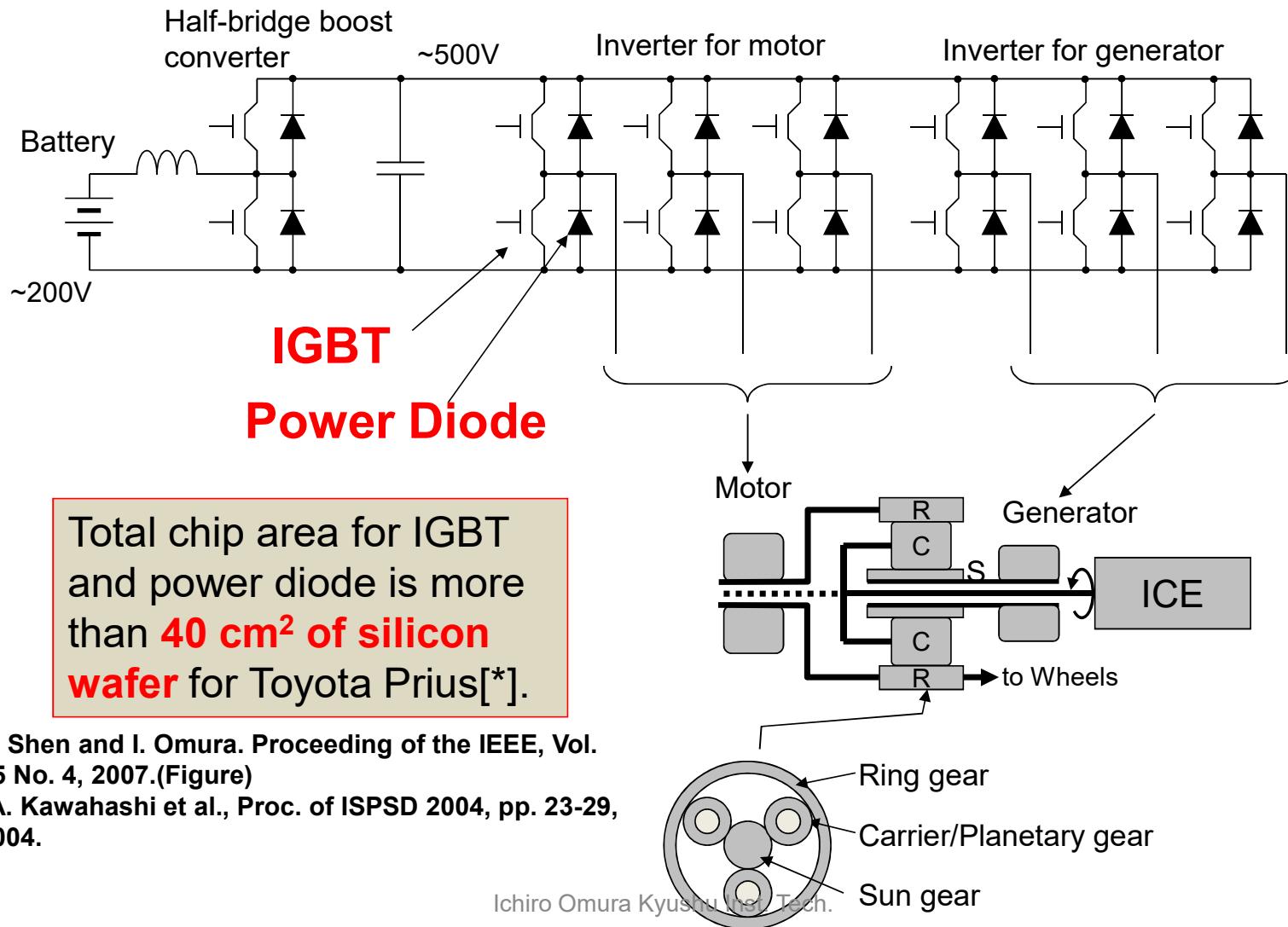


# PWM: Pulse Width Modulation



1. PWM signal control power semiconductors switch (ON / OFF)
2. Motor current follows the modulation wave

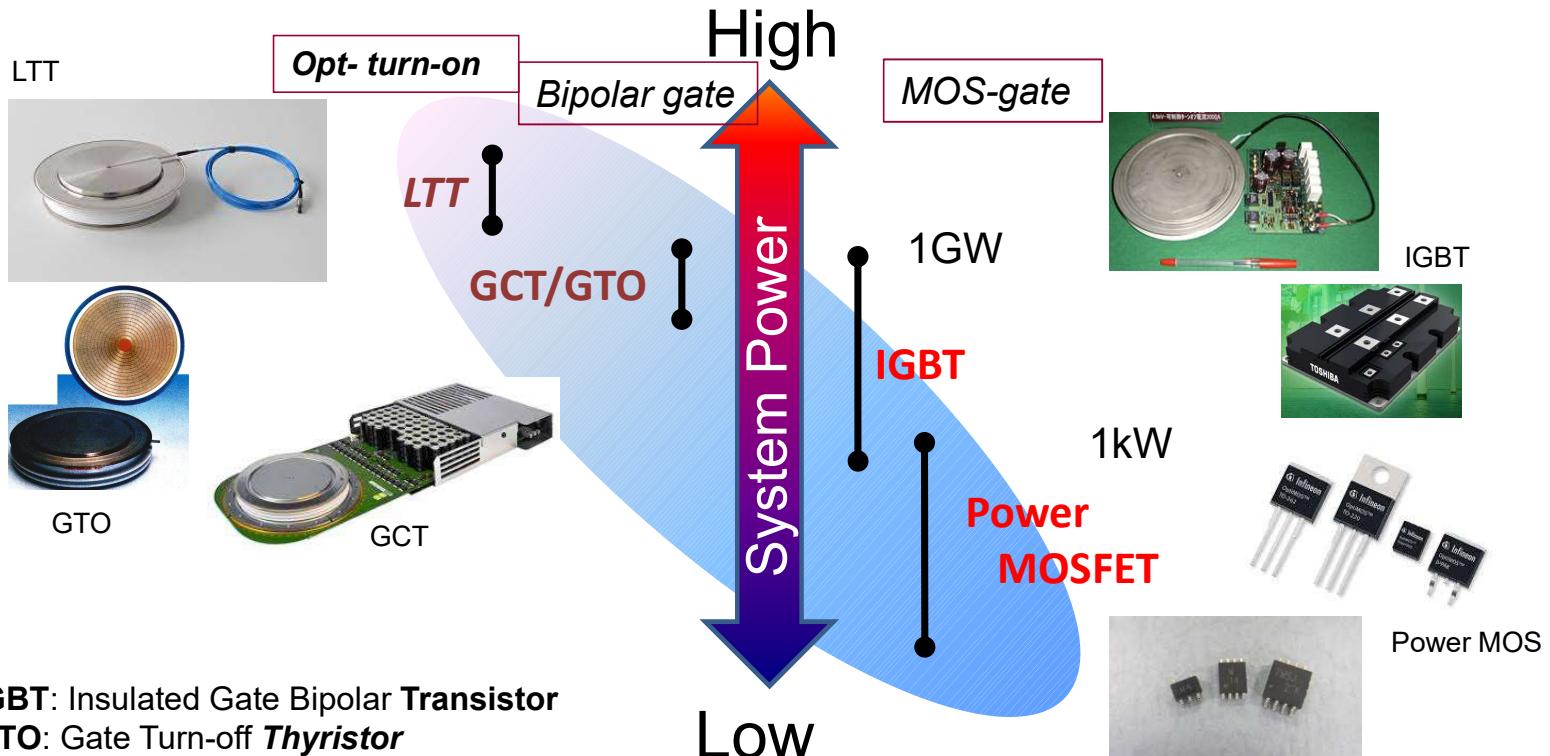
# Hybrid electric vehicle propulsion system



# Power Semiconductor Devices

# Power Semiconductor Devices

Vertical device

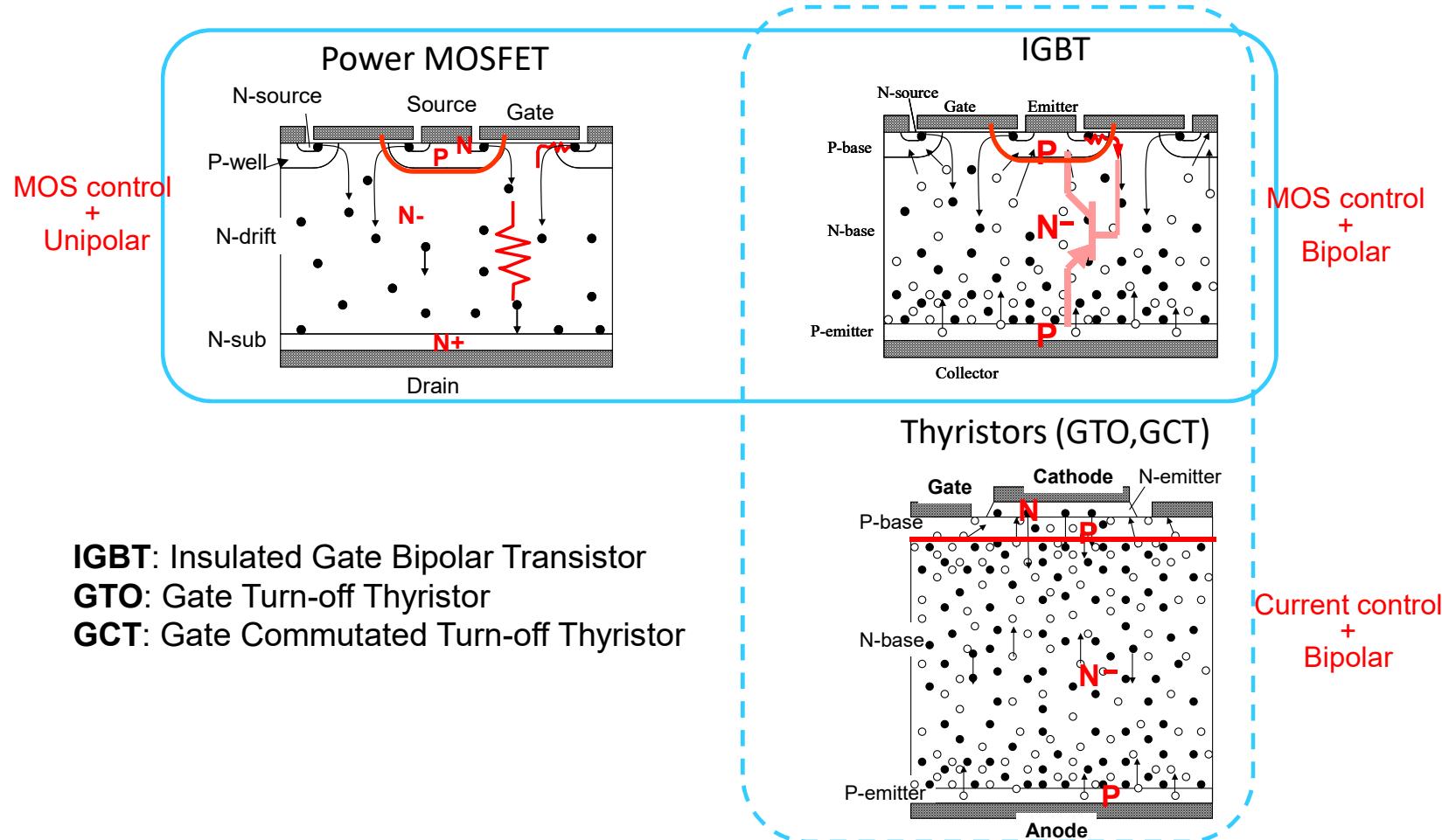


- MOS gate devices cover wide-power range.
- Bipolar gate devices cover very high power applications(>10MW).

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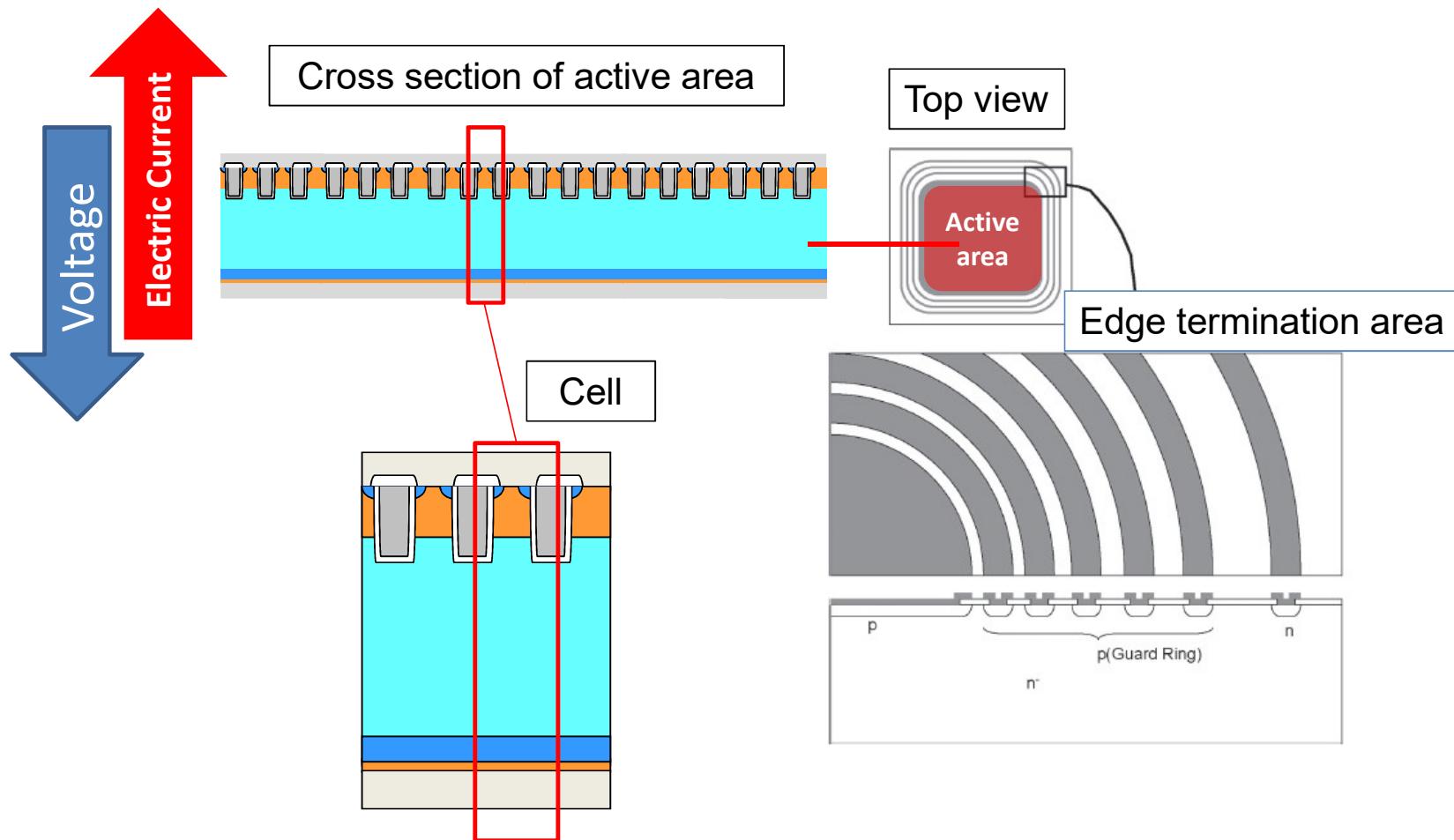
Photos:  
Infineon  
Toshiba  
ABB  
TMEIC

# Types of power semiconductors(Switch)

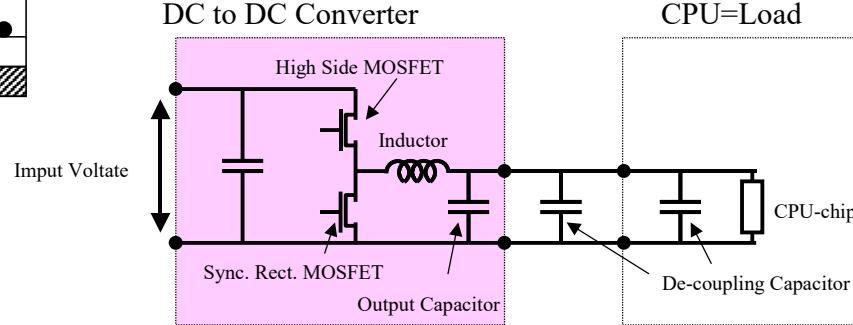
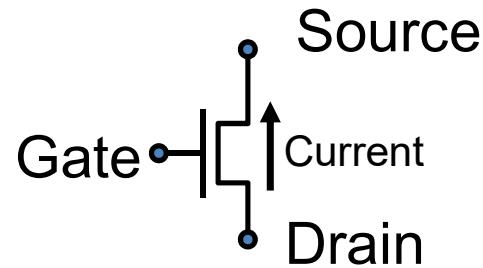
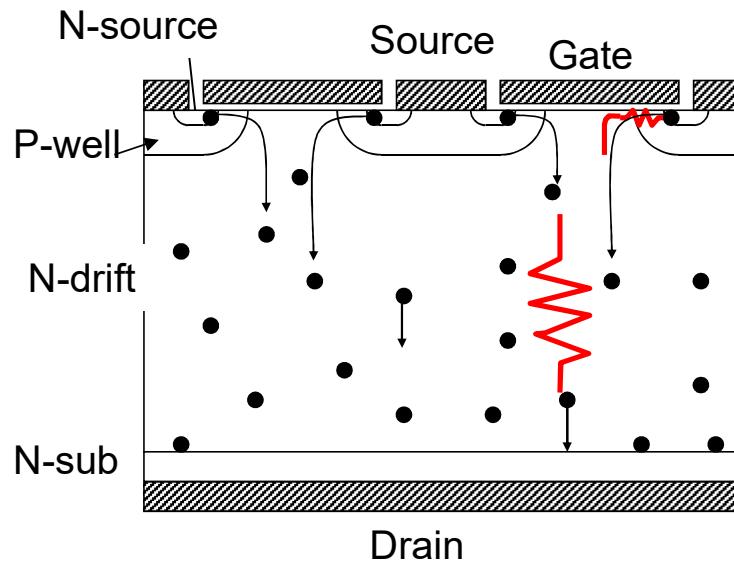


1. MOS-gate (voltage) control or bipolar gate (current) control
2. Unipolar conduction or bipolar conduction in high resistive layer( $N^-$ )

# Remark: Vertical Device Structure



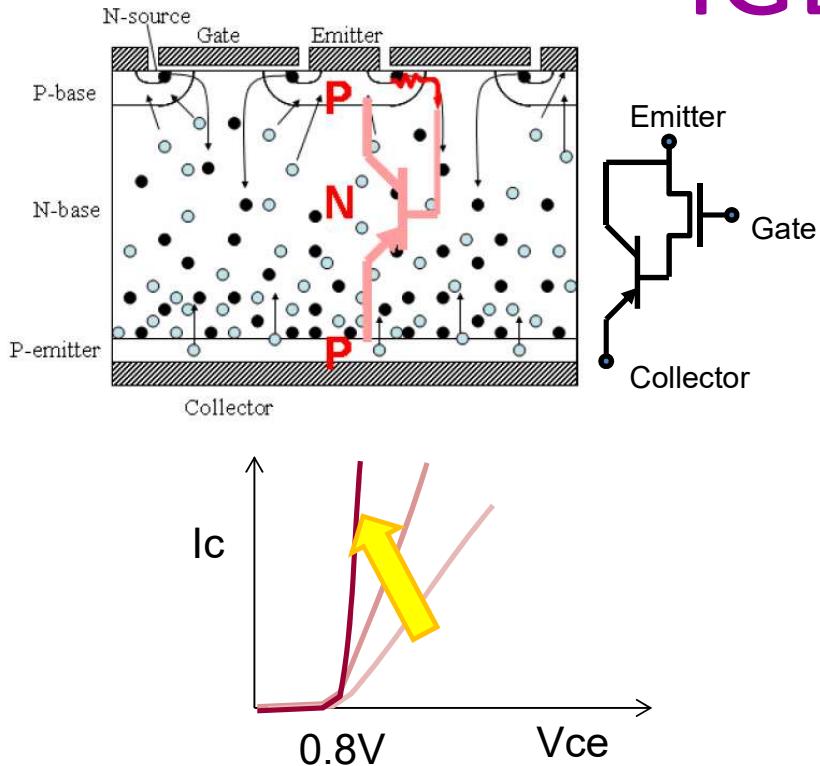
# Power MOSFET



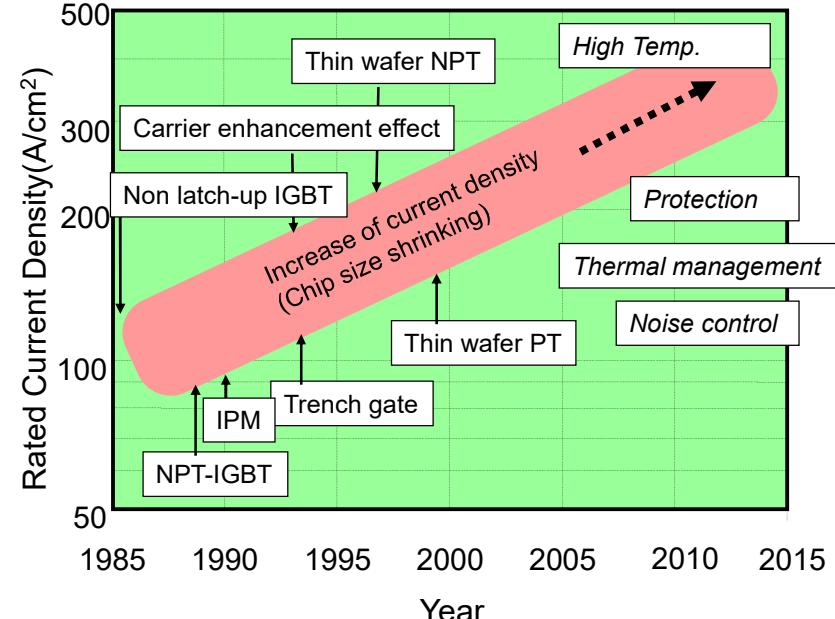
Conduction carrier..... *Electron or hole*  
 Switching control ..... *MOS-gate*  
 Switching Freq. .... *High*

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# IGBT



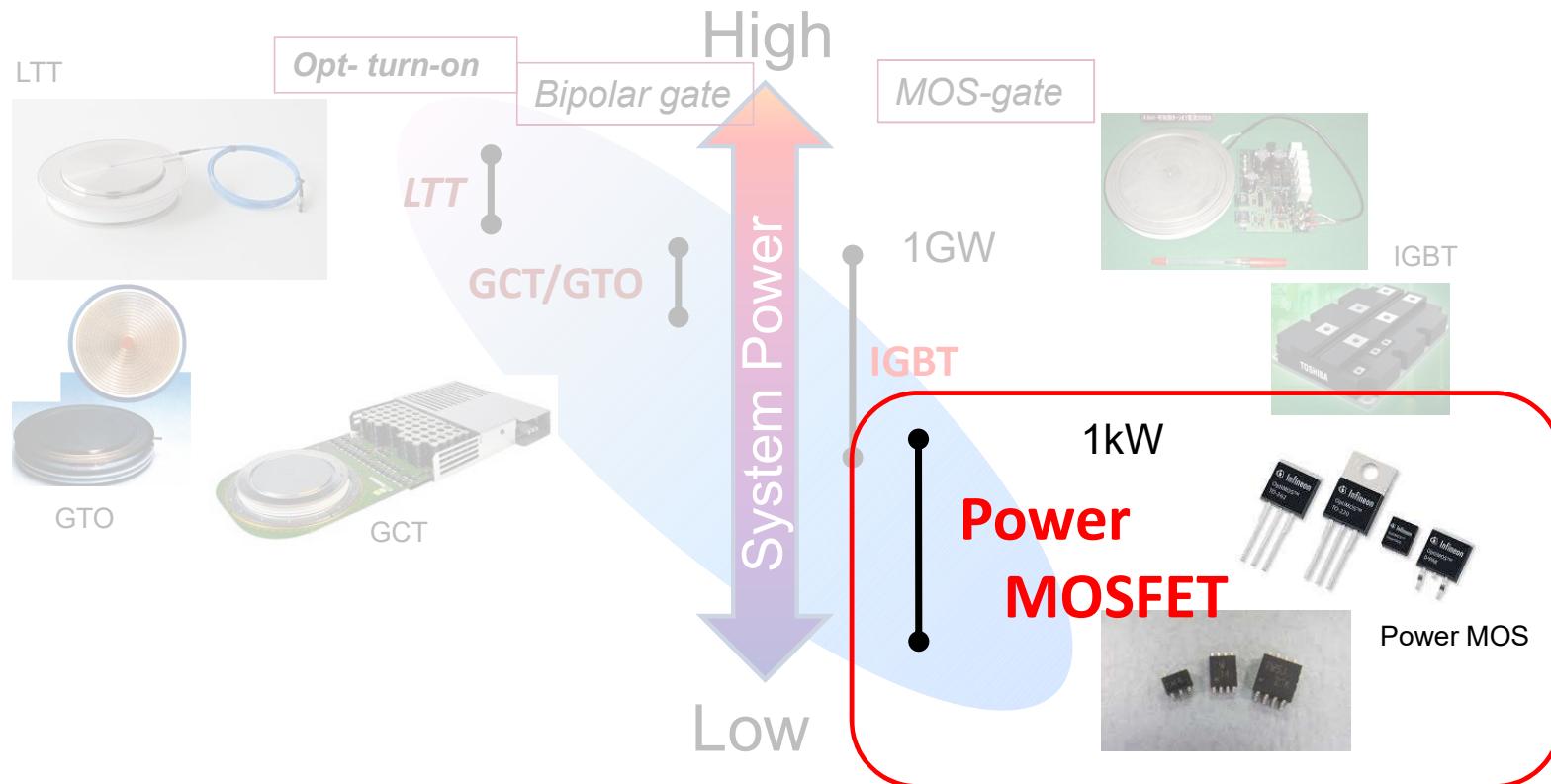
Shen, Omura, "Power Semiconductor Devices for Hybrid, Electric, and Fuel Cell Vehicles" Proc. Of the IEEE, Issue 4, 2007



1. Bipolar Transistor + MOSFET (before IE-effect)
2. High current capability
3. ~0.8V collector-emitter threshold voltage for conduction
4. Medium switching speed (15kHz for motor drive, 100kHz for ICT current supply and FPD driver )

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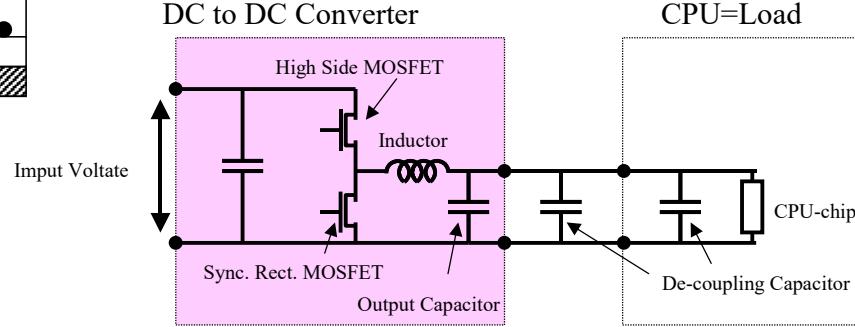
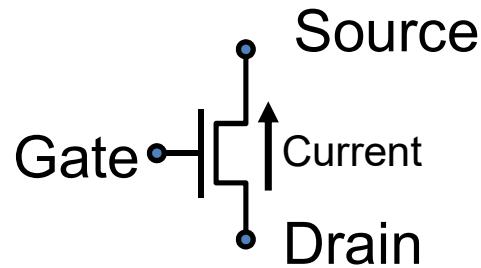
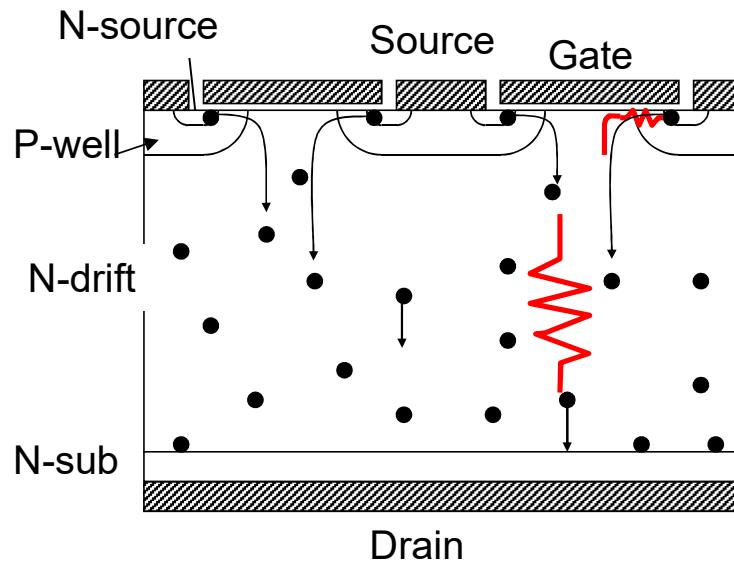
# Power MOSFET



Photos:  
Infineon  
Toshiba  
ABB  
TMEIC

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# Power MOSFET



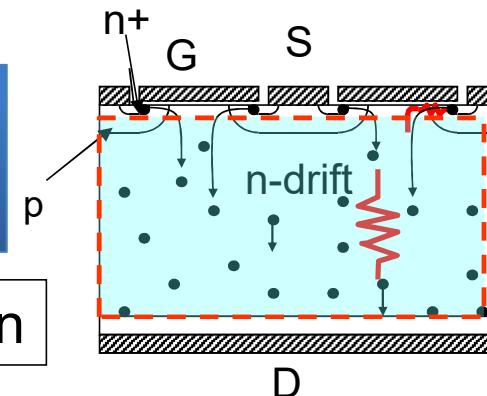
Conduction carrier..... *Electron or hole*  
Switching control ..... *MOS-gate*  
Switching Freq. .... *High*

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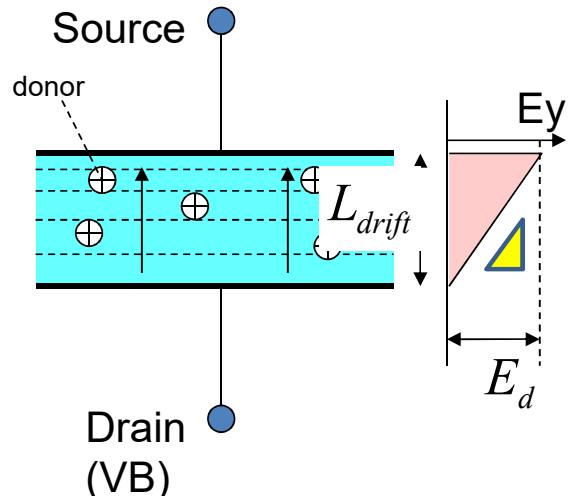
# Function of N-drift layer

**Function of N-drift layer:**

1. Voltage blocking (higher breakdown voltage)
2. Current conduction (lower resistivity)



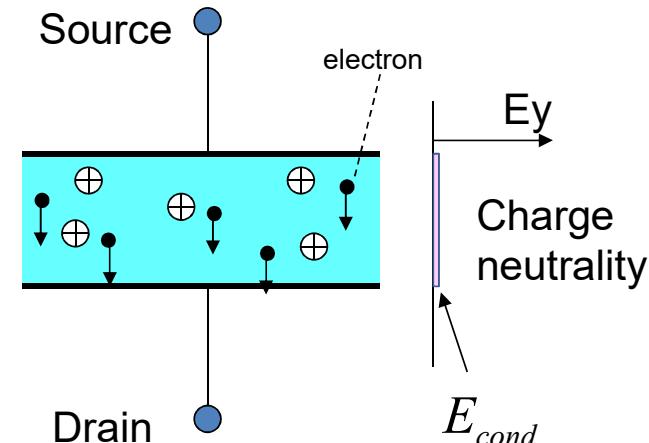
## Voltage Blocking



Blocking state (Poisson eq.)

$$qN_D = -\varepsilon \frac{dE_y}{dy} = \varepsilon \cdot \frac{E_d}{L_{drift}}$$

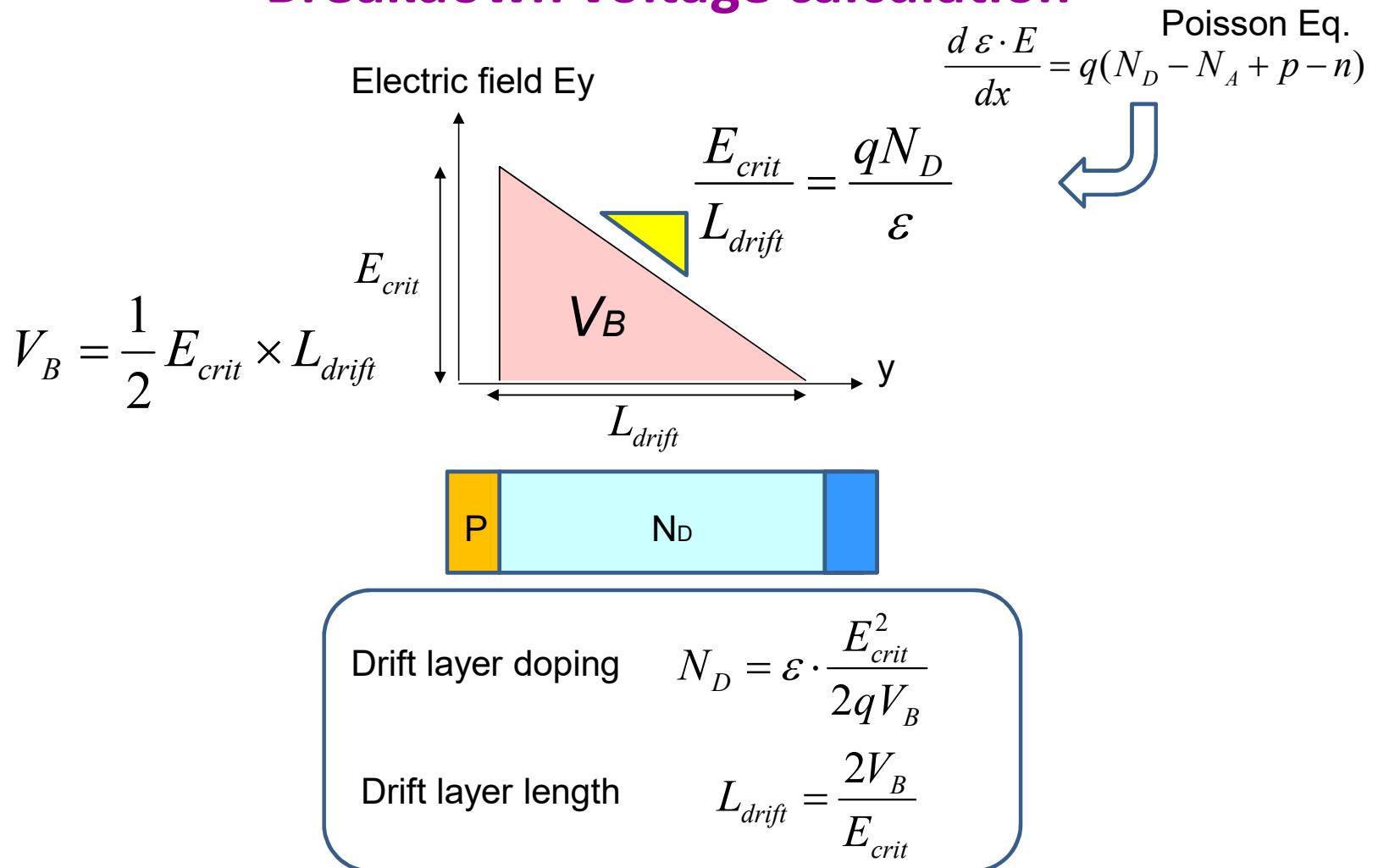
## Conduction



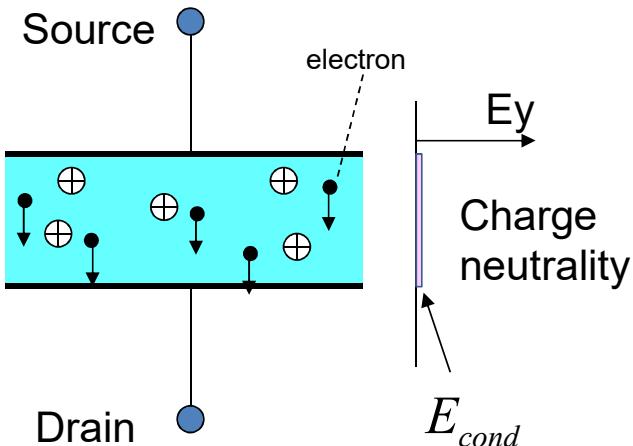
Conduction state (current eq.)

$$J_n = q\mu_n N_D E_{cond} = q\mu_n N_D \frac{V_{cond}}{L_{drift}}$$

## Breakdown voltage calculation



# Conduction resistance calculation



Conduction resistance

$$J_n = q\mu_n N_D E_{cond} = q\mu_n N_D \frac{V_{cond}}{L_{drift}}$$

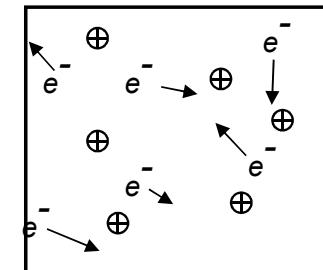
$$R_{on} A = \frac{L_{drift}}{q\mu_n N_D} \quad \text{Resistance for unit area}$$

$$\frac{d \varepsilon \cdot E}{dx} = q(N_D - N_A + p - n) \approx 0$$

↓

$n \approx N_D$

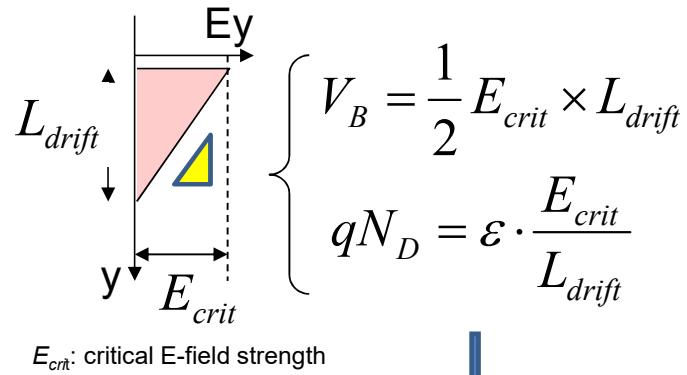
Free electron and fixed positive charge (Donor) ( $N_D$ )



## **Problem**

1. Calculate required drift length for breakdown voltage 1200V.  
( $E_{crit}=2.0E5$  V/cm)
2. Calculate donor concentration for drift layer  
( $q=1.6E-19$  C,  $\epsilon=1.0e-12$  [F/cm](silicon))
3. Calculate drift resistance (mobility of electron 1500 cm<sup>2</sup>/V-s)
4. Calculate 1~3 for 600V, 1700V,

# Drift layer doping, length and drift layer resistance



$E_{crit}$ : critical E-field strength

Drift layer doping

$$N_D = \epsilon \cdot \frac{E_{crit}^2}{2qV_B}$$

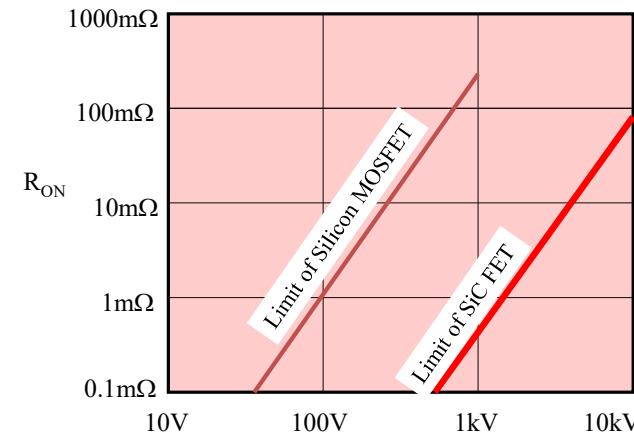
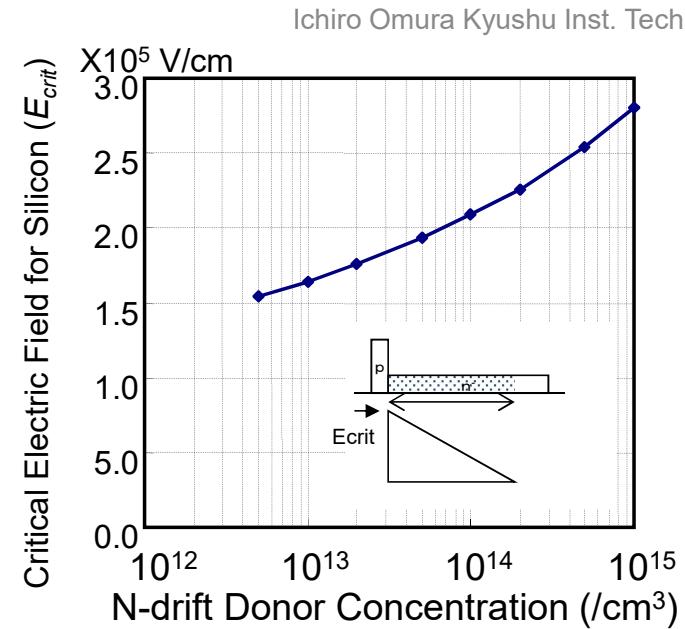
Drift layer length

$$L_{drift} = \frac{2V_B}{E_{crit}}$$

$$J_n = q\mu_n N_D \frac{V_{cond}}{L_{drift}}$$

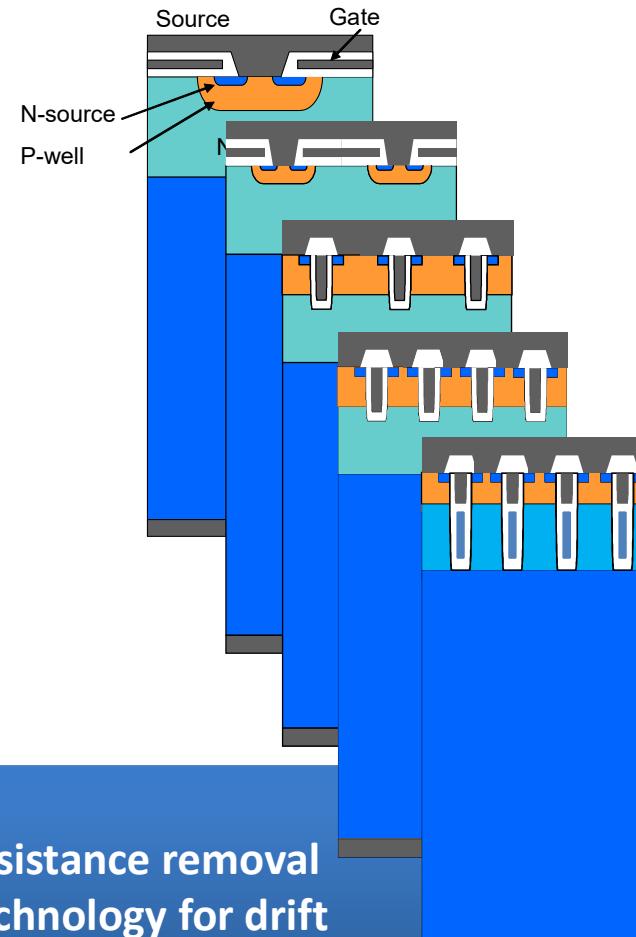
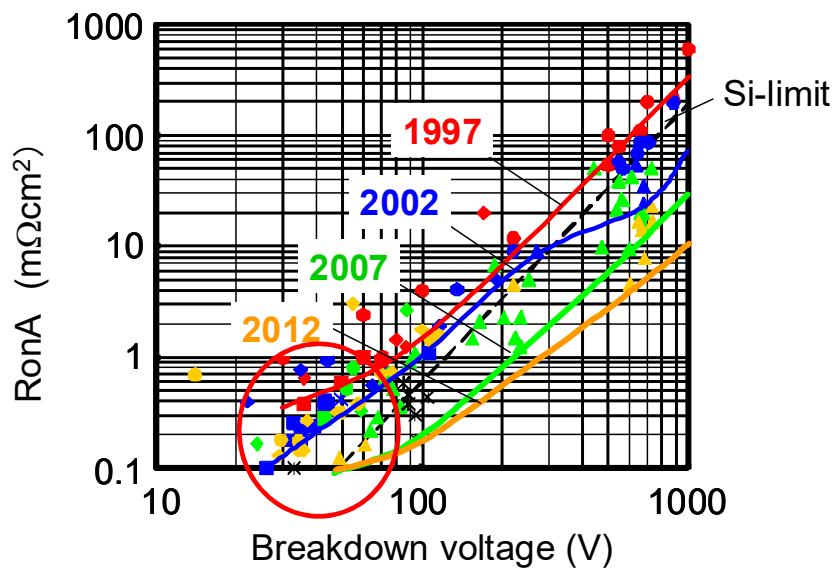
Drift layer resistance

$$R_{drift} = \frac{4V_B^2}{\mu_n \epsilon E_{crit}^3}$$



# Low Voltage MOSFET (Vertical)

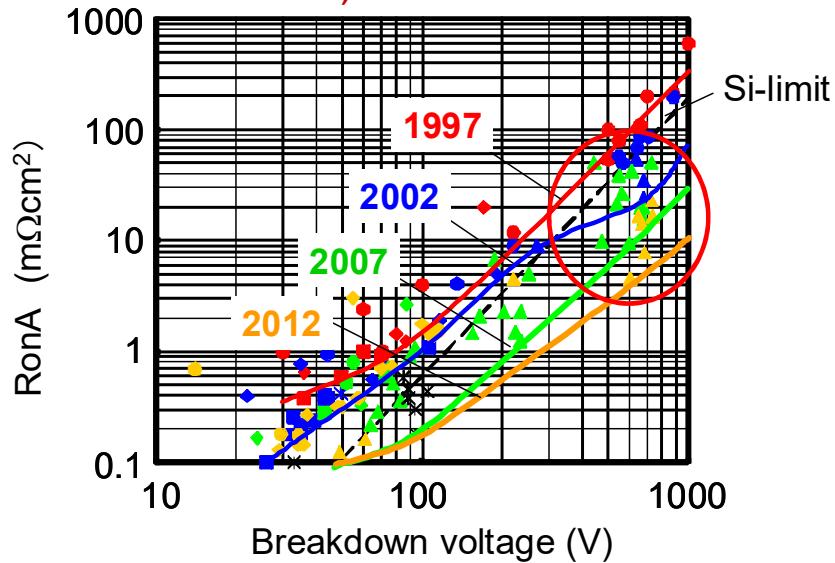
Fig from Lecture Slide by  
W. Saito, Toshiba



1. Cell size reduction for channel density
2. Trench gate for channel density and JFET resistance removal
3. Charge compensate (Vertical Field Plate) technology for drift resistance reduction.

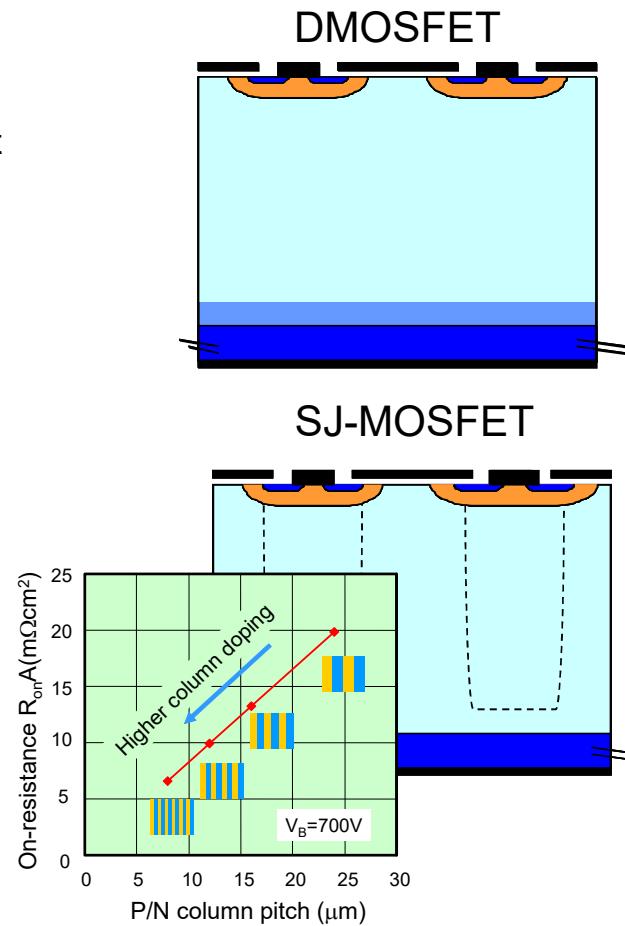
# Super Junction MOSFET

Fig from Lecture Slide by  
W. Saito, Toshiba



P/N column drift layer  
 → Easy to deplete for high impurity concentration  
 → Low Ron + High Breakdown Voltage

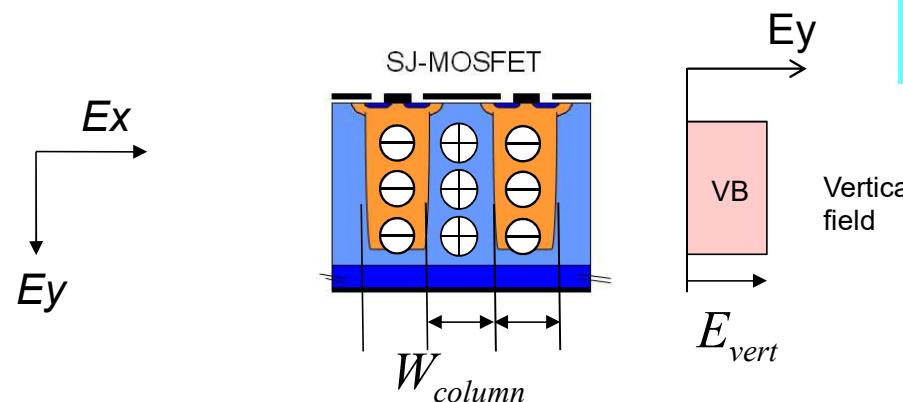
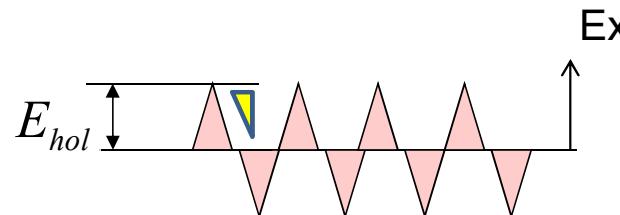
Charge compensate (Super Junction) technology  
 for drift resistance reduction.



# Electric field in Super Junction Str.

1. Horizontal field for P/N column depletion

$$qN_D = \varepsilon \frac{dE_x}{dx} = \varepsilon \cdot \frac{2E_{hol}}{W_{column}}$$

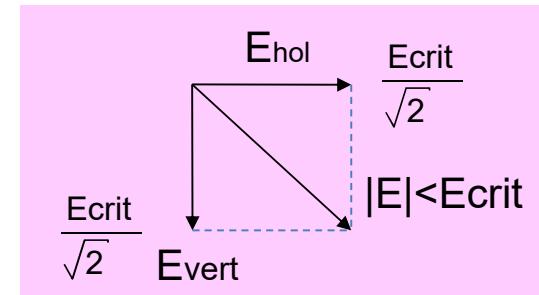
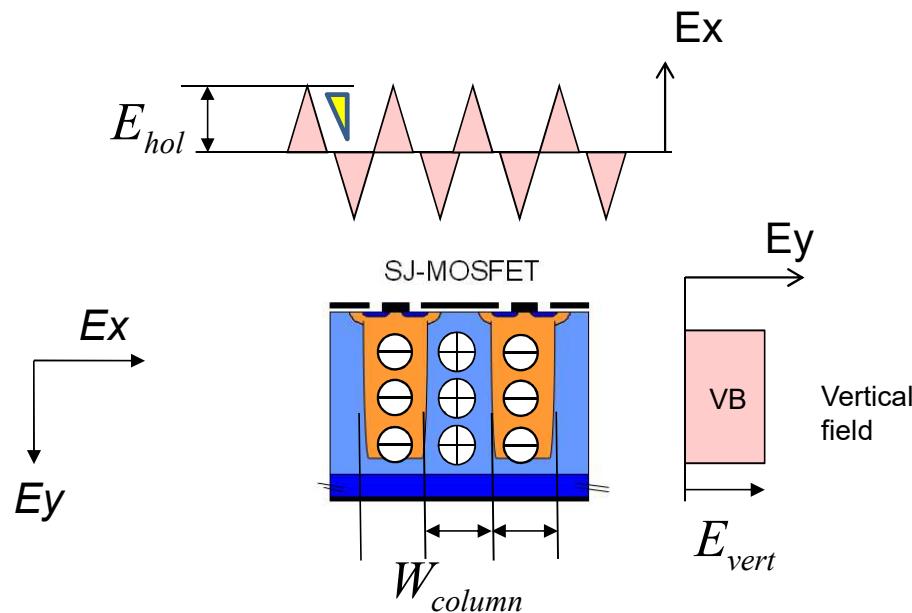


2. Vertical field for voltage blocking between drain and source

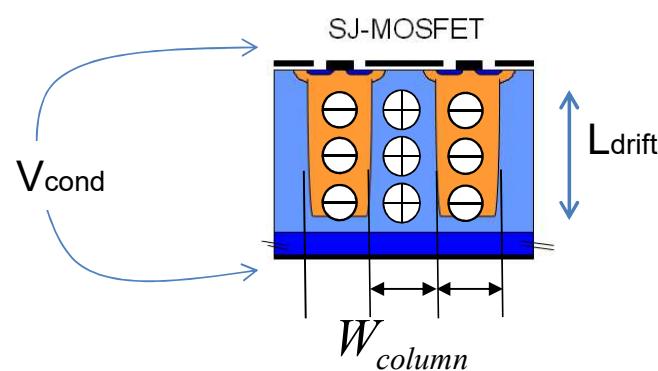
$$V_B = E_{vert} \cdot L_{drift}$$

# Electric field in Super Junction Str.

$$\left\{ \begin{array}{l} qN_D = \varepsilon \cdot \frac{2E_{hol}}{W_{column}} \\ V_B = E_{vert} \cdot L_{drift} \end{array} \right. \quad \begin{array}{l} E_{hol} \Leftarrow \frac{E_{crit}}{\sqrt{2}} \\ E_{vert} \Leftarrow \frac{E_{crit}}{\sqrt{2}} \end{array}$$



# Column doping( $N_D$ ) and conduction current



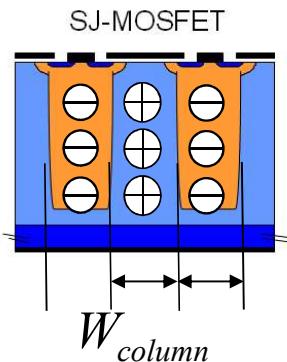
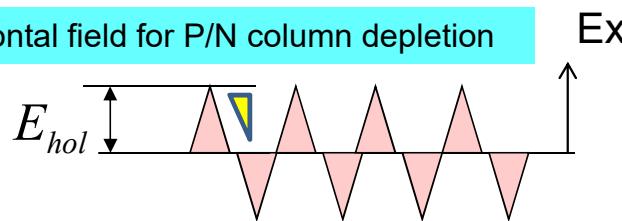
3. A half area of drift layer contribute current conduction

$$J_n = \frac{1}{2} q\mu_n N_D E_{cond} = \frac{1}{2} q\mu_n N_D \frac{V_{cond}}{L_{drift}}$$

# Column doping( $N_D$ ) and Breakdown Voltage( $V_B$ )

1. Horizontal field for P/N column depletion

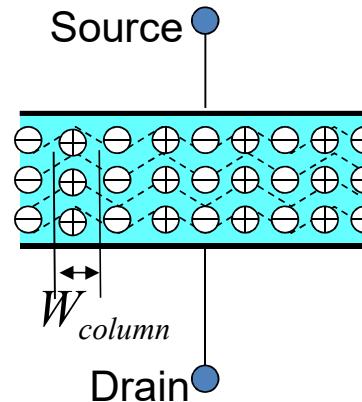
$$qN_D = \epsilon \frac{dE_x}{dx} = \epsilon \cdot \frac{2E_{hol}}{W_{column}}$$



$E_x$

3. A half area of drift layer contribute current conduction

$$J_n = \frac{1}{2} q\mu_n N_D E_{cond}$$



$$V_B = E_{vert} \cdot L_{drift}$$

2. Vertical field for voltage blocking between drain and source

Electric field in SuperJunction structure → high drift layer donor doping

1. Horizontal electric field for depletion of PN junction in narrow columns
2. Vertical electric field for sustain blocking voltage across drift layer

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## Drift layer doping, length and drift layer resistance

$$\left\{ \begin{array}{l} qN_D = \epsilon \cdot \frac{2E_{hol}}{W_{column}} \quad E_{hol} \Leftarrow \frac{E_{crit}}{\sqrt{2}} \\ V_B = E_{vert} \cdot L_{drift} \quad E_{vert} \Leftarrow \frac{E_{crit}}{\sqrt{2}} \end{array} \right.$$

Drift N-column doping

$$N_D = \epsilon \cdot \frac{\sqrt{2}E_{crit}}{qW_{column}}$$

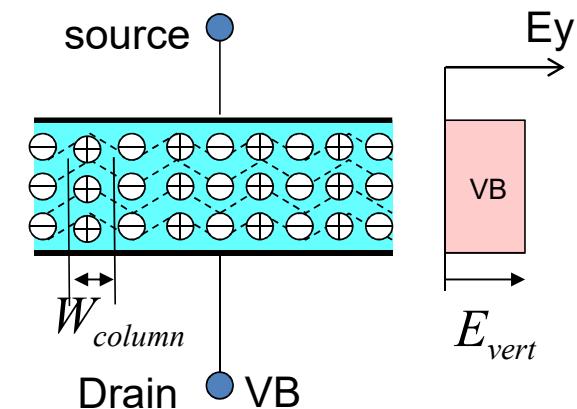
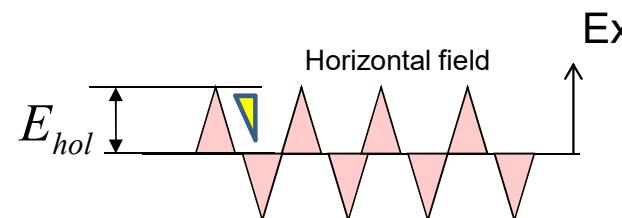
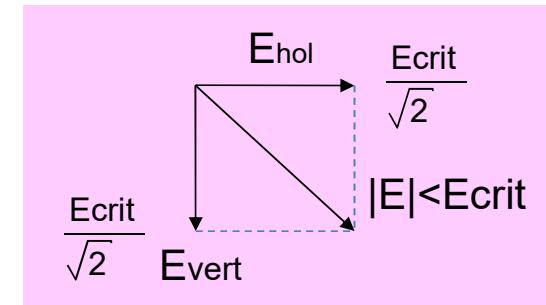
Drift layer length

$$L_{drif} = \frac{\sqrt{2} V_B}{E_{crit}}$$

$$J_n = \frac{1}{2} q \mu_n N_D E_{cond} = \frac{1}{2} q \mu_n N_D \frac{V_{cond}}{L_{drift}}$$

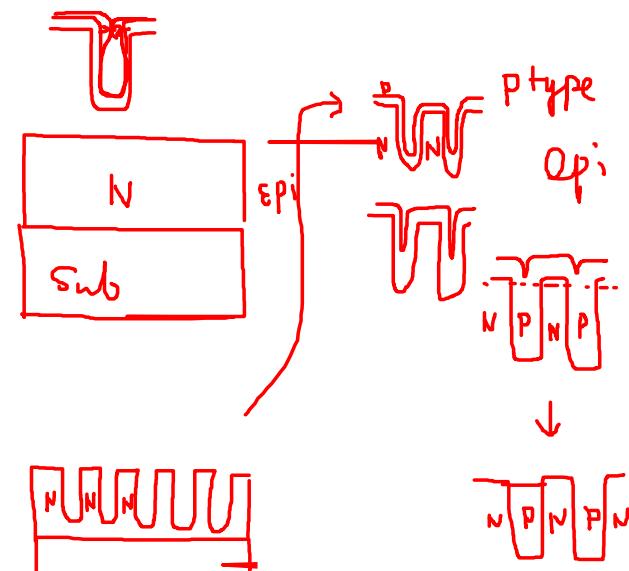
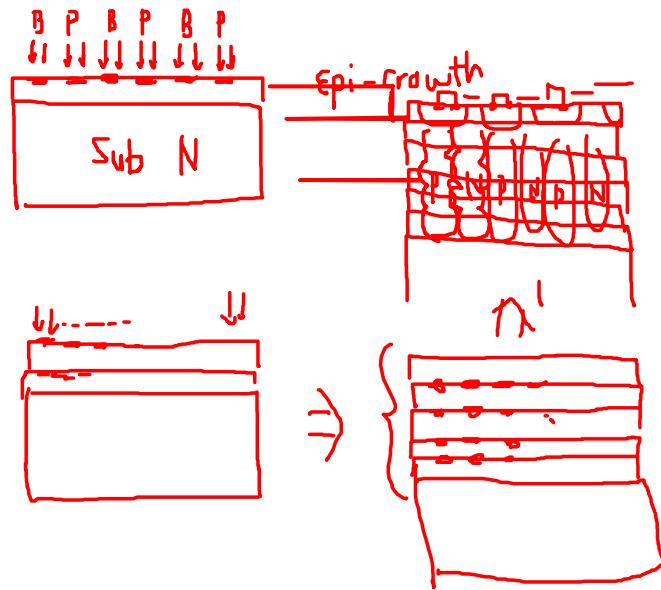
**Drift layer resistance**  $[ \Omega \text{cm}^2 ]$

$$R_{drift} = \frac{2V_B \cdot W_{column}}{\mu_n \epsilon E_{crit}^2}$$



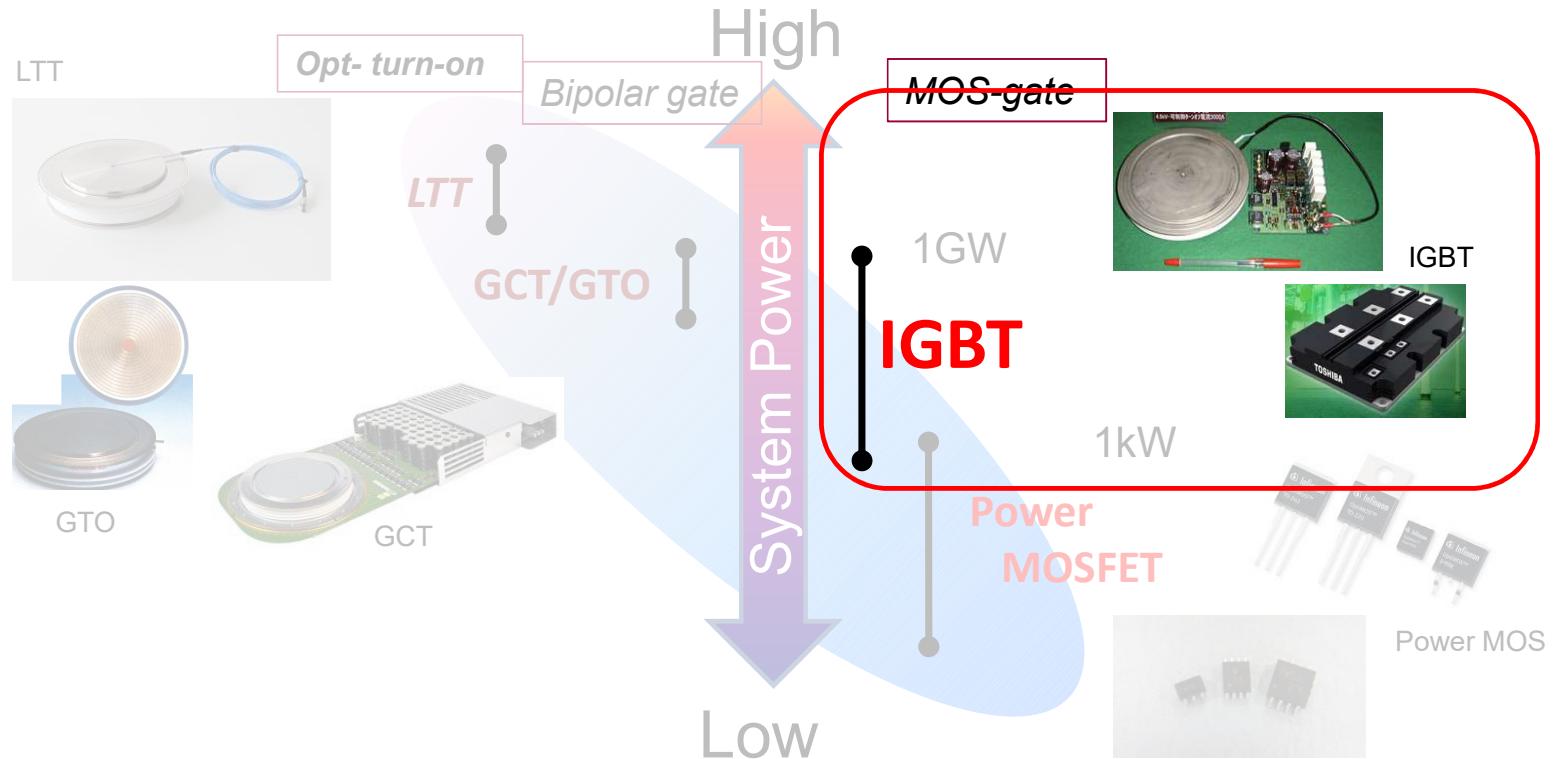
Assumption: N-column and P-column are same width

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# IGBT

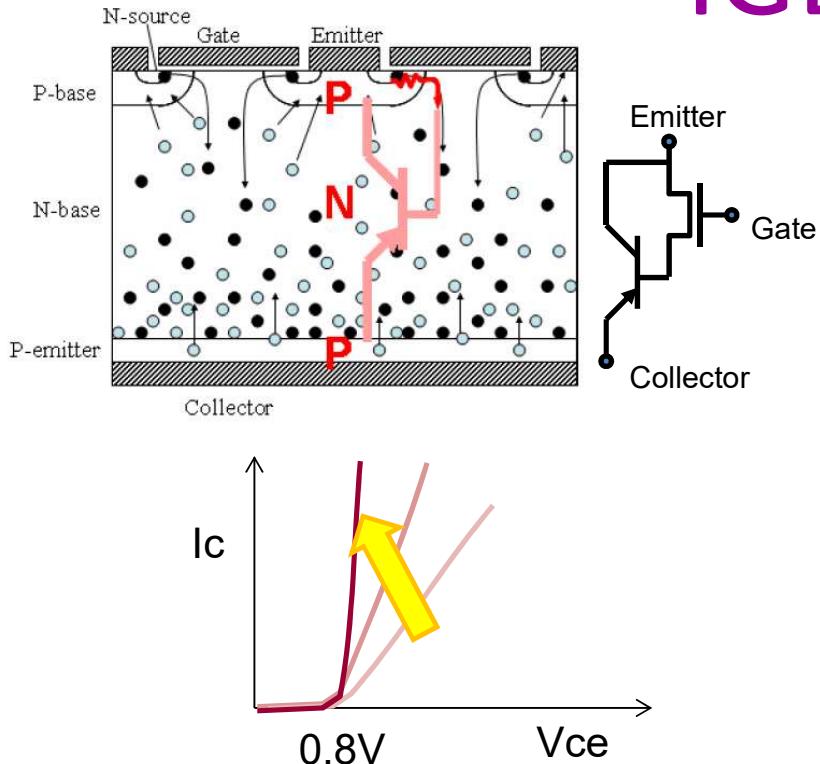
## Insulated Gate Bipolar Transistor



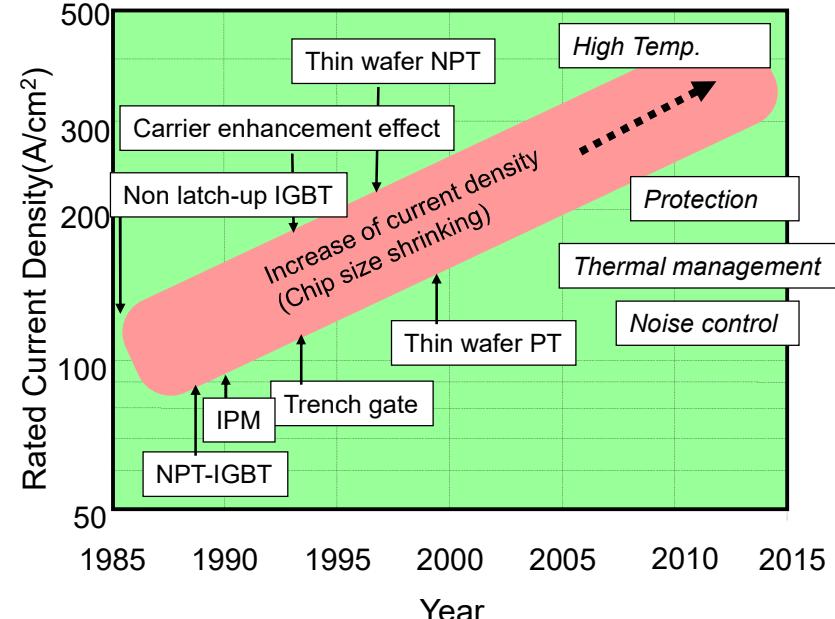
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Photos:  
Infineon  
Toshiba  
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TMEIC

# IGBT



Shen, Omura, "Power Semiconductor Devices for Hybrid, Electric, and Fuel Cell Vehicles" Proc. Of the IEEE, Issue 4, 2007

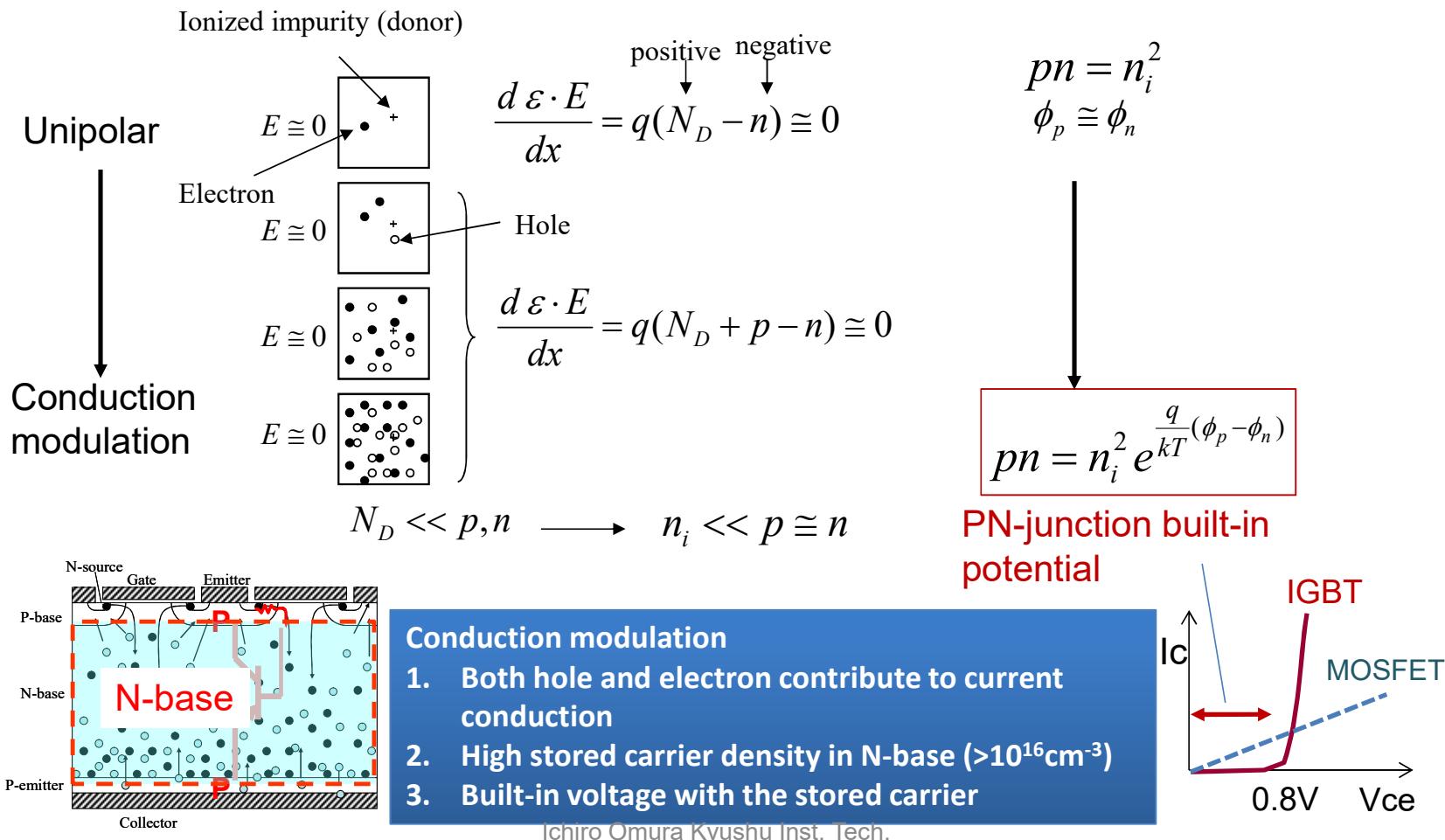


1. Bipolar Transistor + MOSFET (before IE-effect)
2. High current capability
3. ~0.8V collector-emitter threshold voltage for conduction
4. Medium switching speed (15kHz for motor drive, 100kHz for ICT current supply and FPD driver )

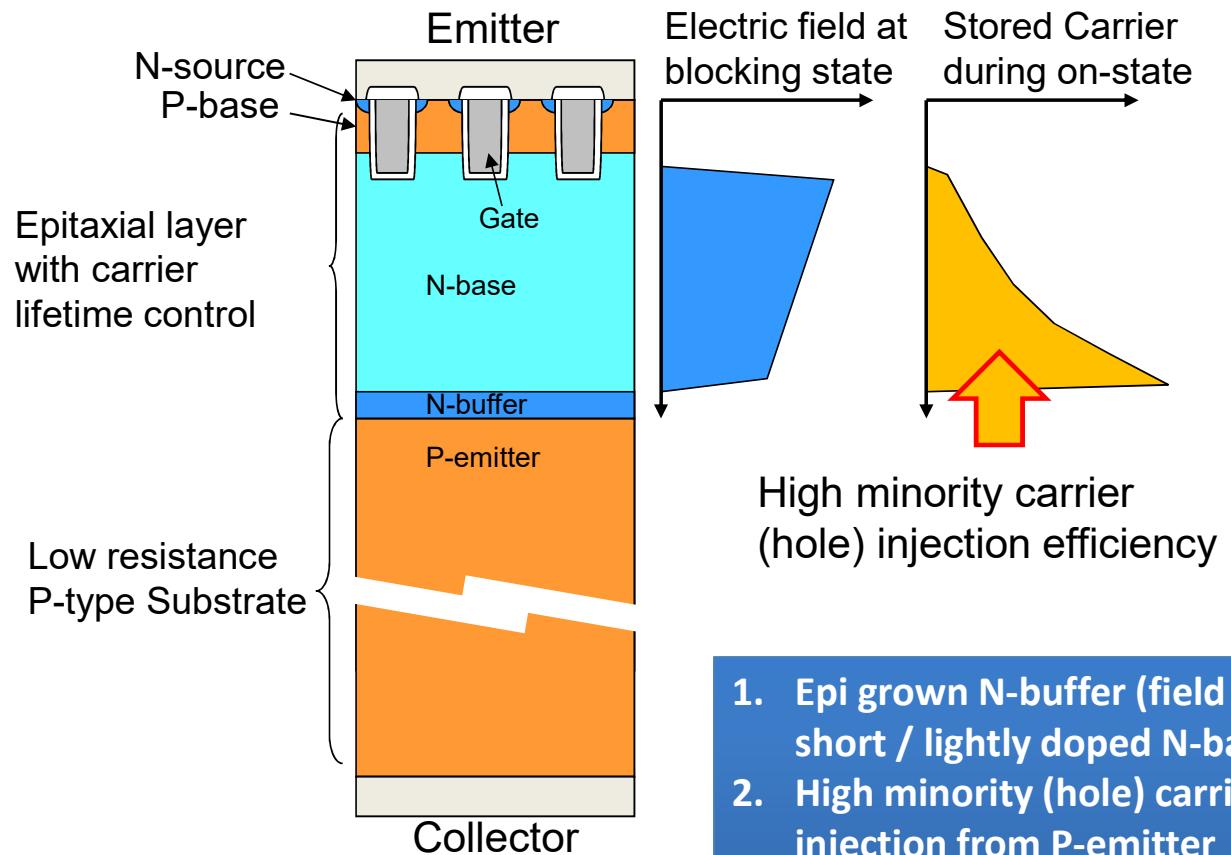
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# Operation mechanism of IGBT

## Conduction modulation in N-base

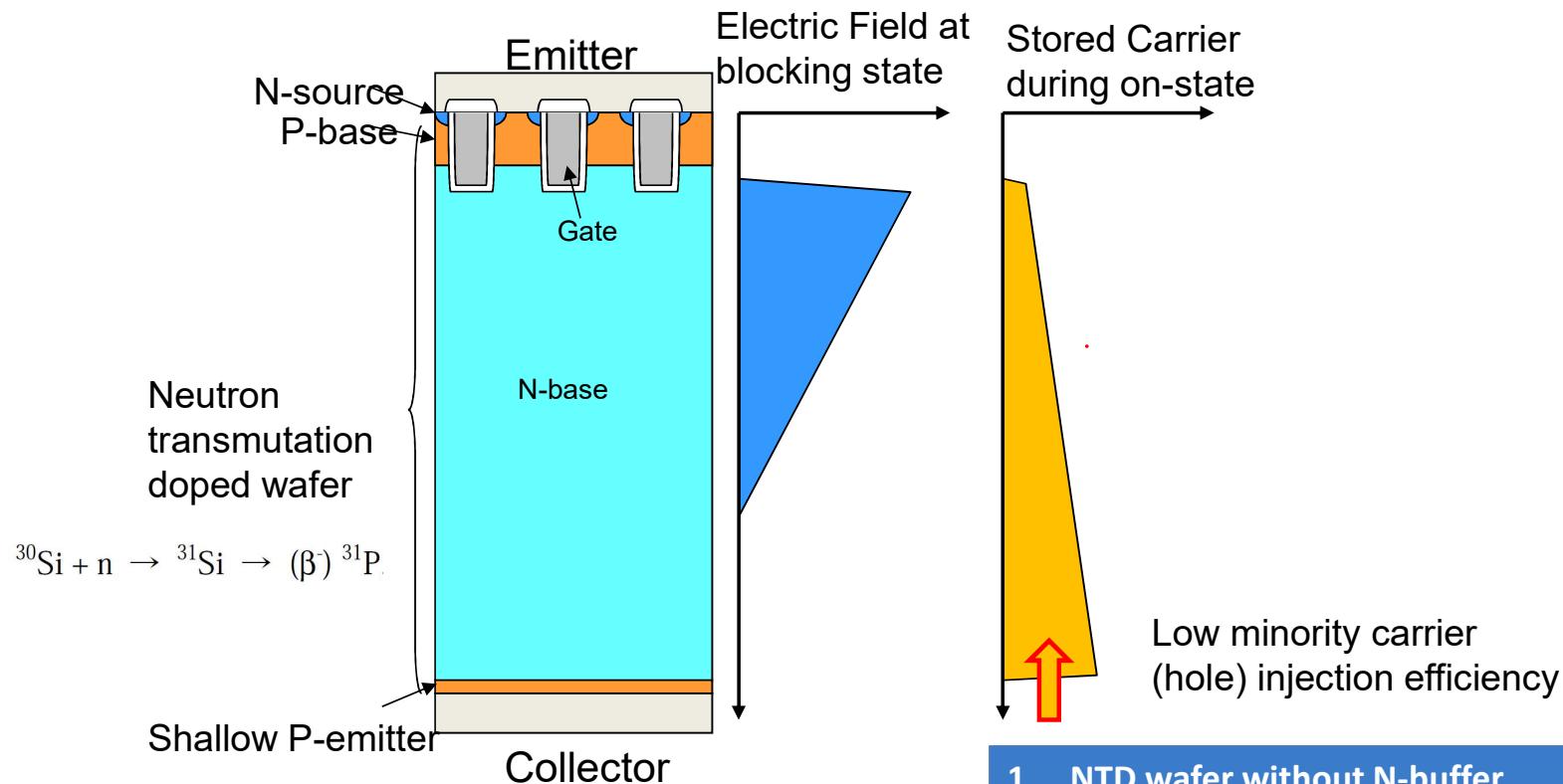


# Punch-through IGBT (PT-IGBT)



1. Epi grown N-buffer (field stop) and short / lightly doped N-base
2. High minority (hole) carrier injection from P-emitter
3. Low-conduction loss and large switching loss
4. Carrier lifetime control (high energy electron irradiation etc.) required

# Non-Punch-through IGBT (NPT-IGBT)



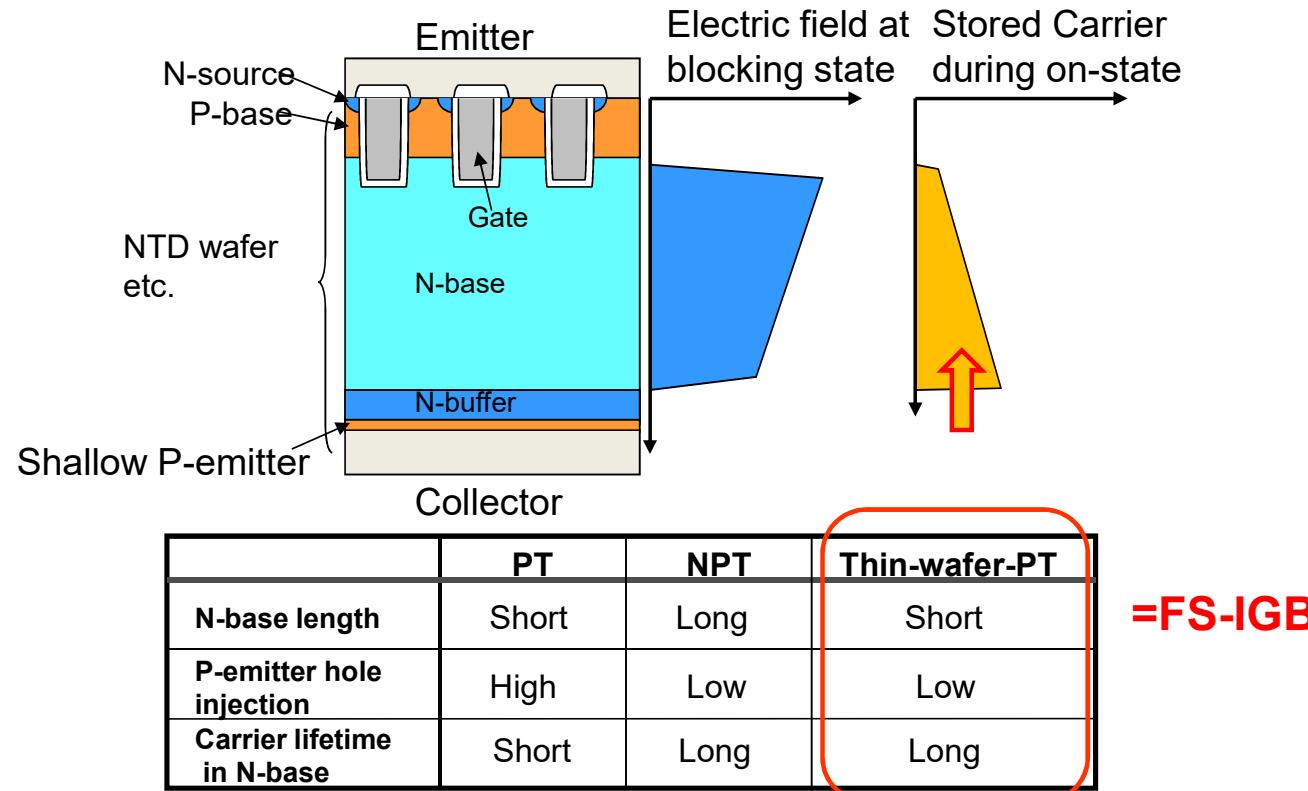
Neutron transmutation doping

M. Tanenbaum and A. D. Mills J. Electrochem. Soc., vol. 108, pp.171 1961  
J. Cornu and R. Sittig IEEE Trans. Electron Devices, vol. ED-22, pp.108 1975  
IAEA-TECDOC-1681, Neutron Transmutation Doping of Silicon at Research Reactors,  
2012

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1. NTD wafer without N-buffer
2. Low minority (hole) carrier injection from P-emitter
3. Higher-conduction loss and lower switching loss
4. No carrier lifetime control required

# Thin wafer IGBT technology



## Thin Wafer Technology

-Reduction of turn-off tail current with short N-base

-Reduction of conduction loss with short N-base

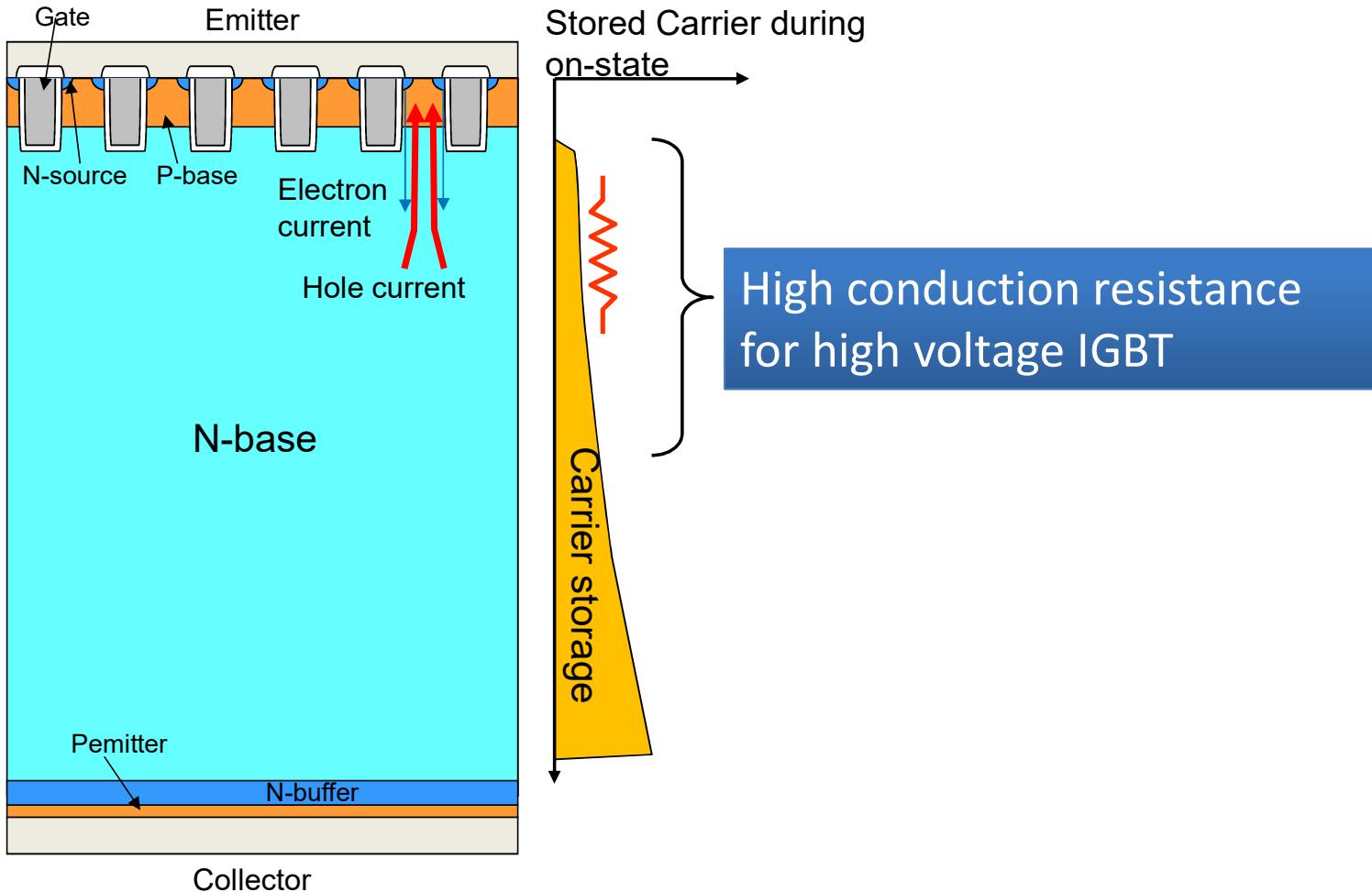
## Low Hole Injection P-emitter with long carrier lifetime

-Reduction of turn-off tail current with low hole injection

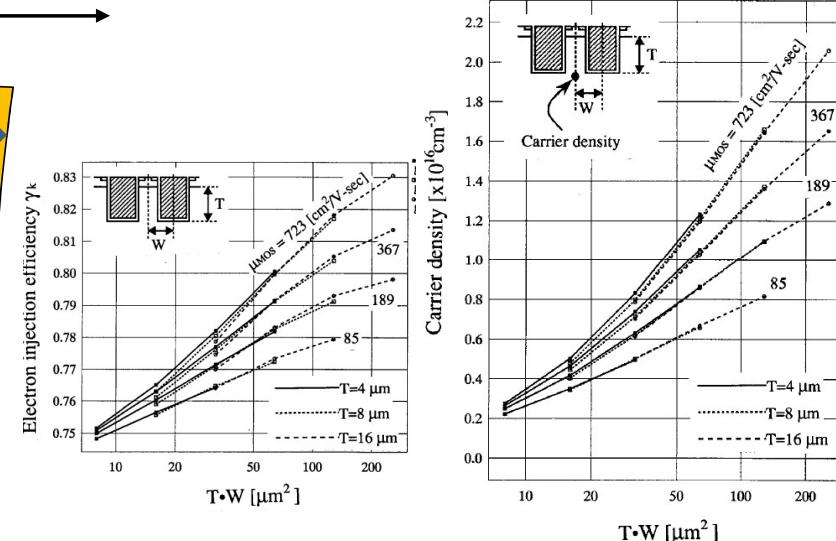
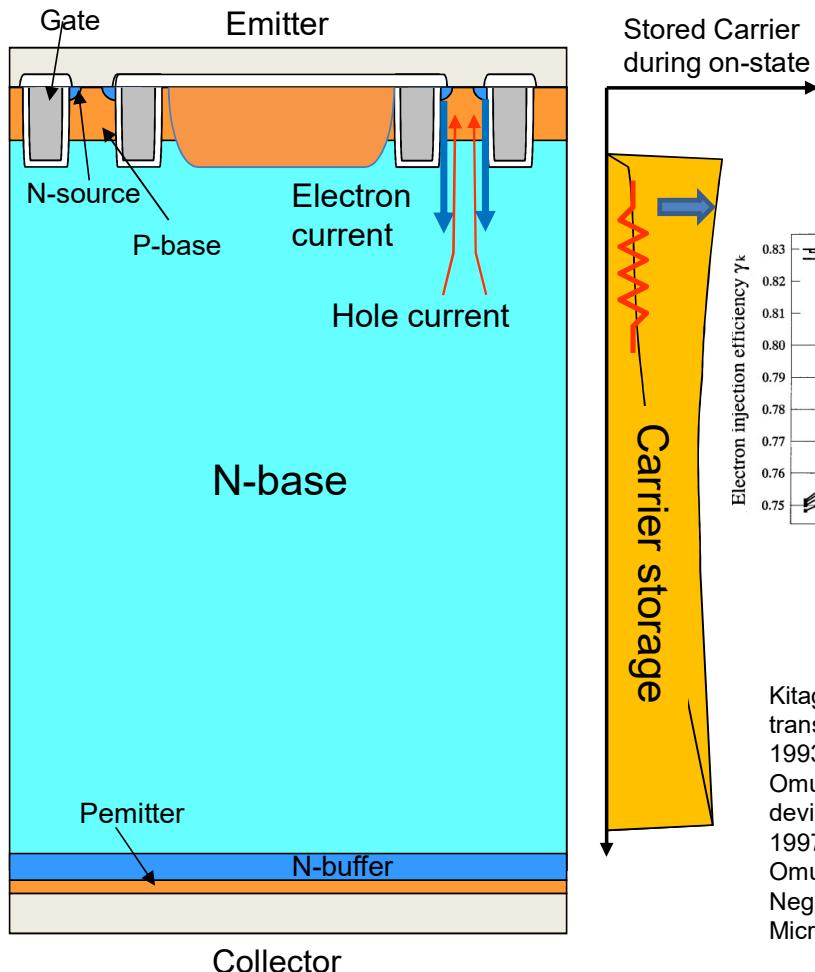
-Better thermal coefficient without carrier lifetime control

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## Problem in High Voltage IGBT Device Design



# Electron Injection Enhancement Effect



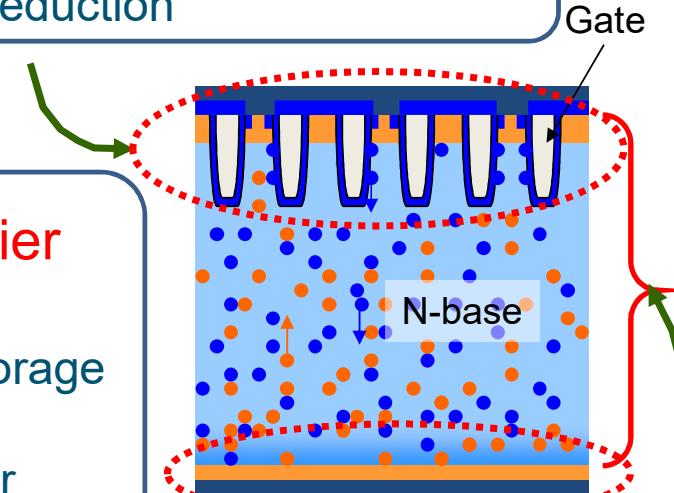
Kitagawa et al. "A 4500 V injection enhanced insulated gate bipolar transistor (IEGT) operating in a mode similar to a thyristor," IEDM'93, 1993.

Omura et al. "Carrier injection enhancement effect of high voltage MOS devices-device physics and design concept," ISPSD 97, pp. 217-220, 1997.

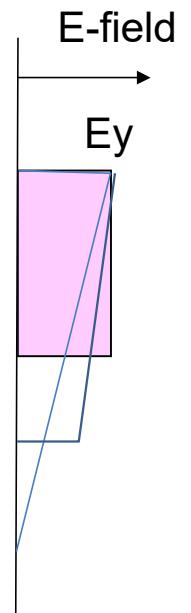
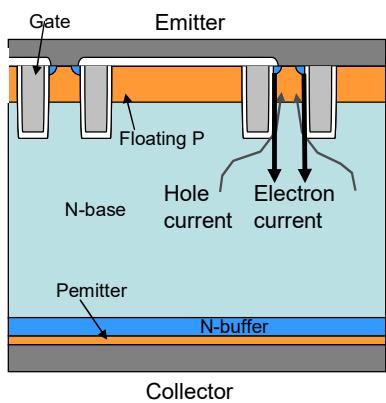
Omura, "High Voltage MOS Device Design: Injection Enhancement and Negative Gate Capacitance, (ETH thesis 2000), Series in Microelectronics Vol. 150, Hartung-Gorre Verlag, 2005.

**Trench gate technology with special structure enhances majority carrier (electron) injection in N-base → Low conduction loss under high current density**

# Summary of IGBT Technology

- Trench Gate
    - Conduction loss reduction with electron injection enhancement
    - Channel resistance, JFET resistance reduction
  - Low Injection P-emitter + Long Carrier Lifetime
    - Turn-off loss reduction with low hole storage in N-base
    - Better thermal coefficient without carrier lifetime control
  - Thin Wafer Technology
    - Both conduction and turn-off loss reduction with short N-base
- 
- The diagram illustrates the cross-section of an IGBT device. It features a top layer labeled 'Gate' with a dashed red outline. Below it is a blue region labeled 'N-base'. At the bottom is an orange region labeled 'P-emitter'. Arrows indicate carrier movement from the N-base into the P-emitter. A green arrow points from the 'Low Injection P-emitter + Long Carrier Lifetime' section to the P-emitter layer. Another green arrow points from the 'Thin Wafer Technology' section to the N-base layer.

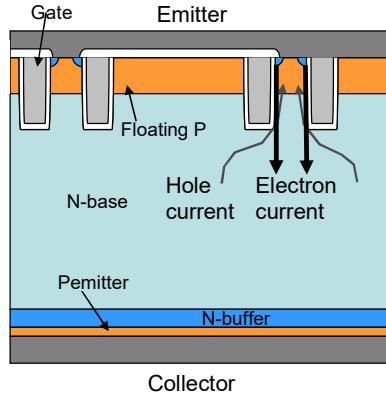
# Breakdown Voltage and N-base length



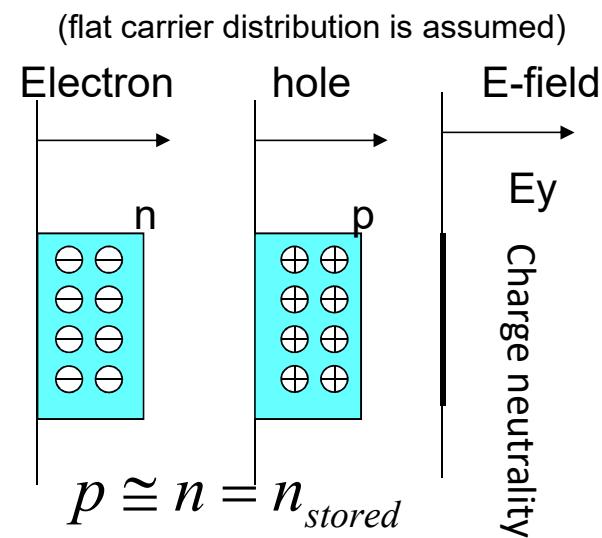
$$2 \frac{V_B}{E_{crit}} \geq L_{n-base} \geq \frac{V_B}{E_{crit}}$$

# Current Conduction

## Conduction



Stored Carrier density  
 $n_{stored}$



$$\begin{aligned} J_{n-base} &= q\mu_n n_{stored} E_{cond} + q\mu_p n_{stored} E_{cond} \\ &= q(\mu_n + \mu_p) n_{stored} \frac{V_{n-base}}{L_{n-base}} \end{aligned}$$

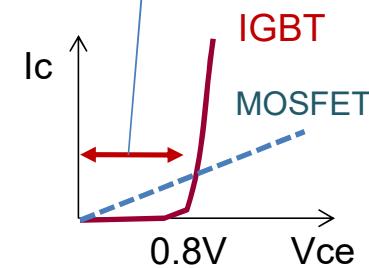
PN-junction built-in potential

$$V_{built-in} = 2 \frac{kT}{q} \ln \frac{n_{stored}}{n_i}$$

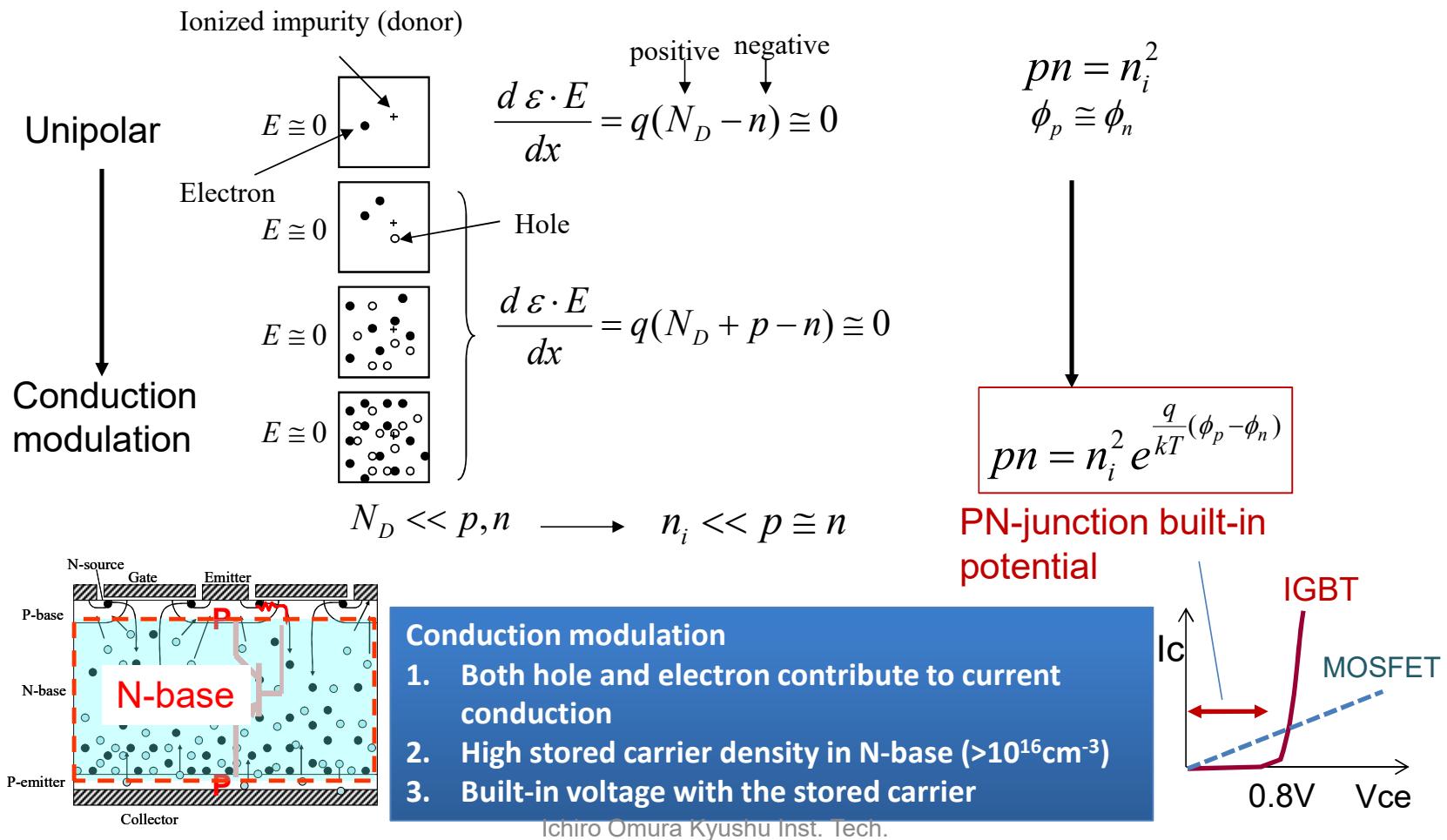
N-base conduction resistance

$$R_{N-base} = \frac{1 \sim 2 V_B}{q(\mu_n + \mu_p) \cdot n_{stored} \cdot E_{crit}}$$

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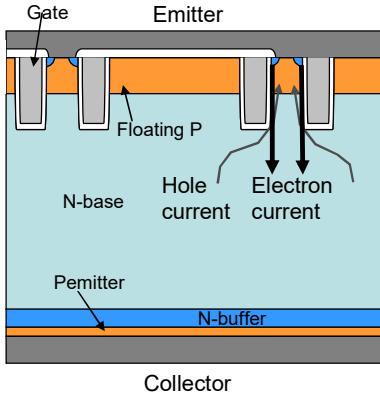


# Conduction modulation in N-base

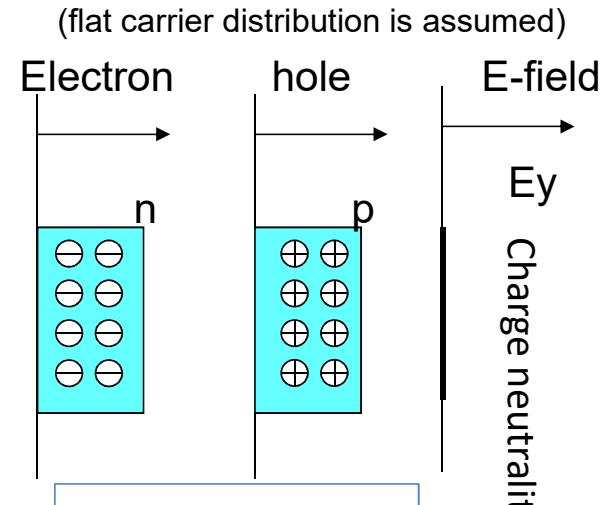


# Current Conduction

## Conduction



Stored Carrier density  
 $n_{stored}$



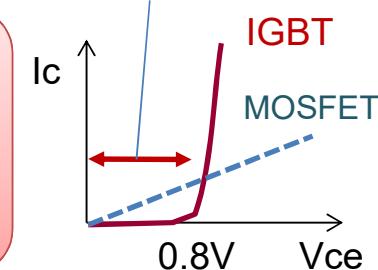
$$p \cong n = n_{stored}$$

$$n_{stored}^2 = n_i^2 e^{\frac{q}{kT}(\phi_p - \phi_n)}$$

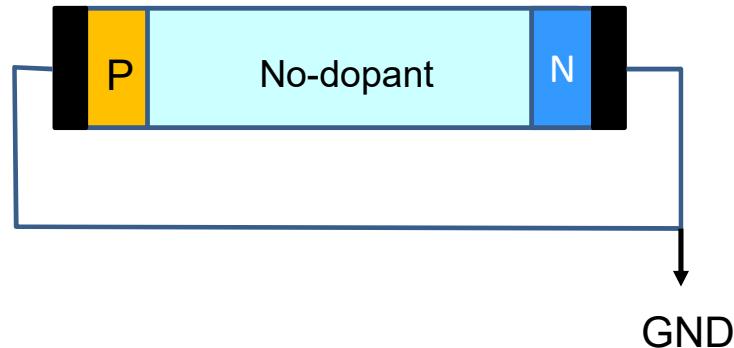
$$e^{\frac{q}{kT}(\phi_p - \phi_n)} = \frac{n_{stored}^2}{n_i^2}$$

PN-junction built-in potential

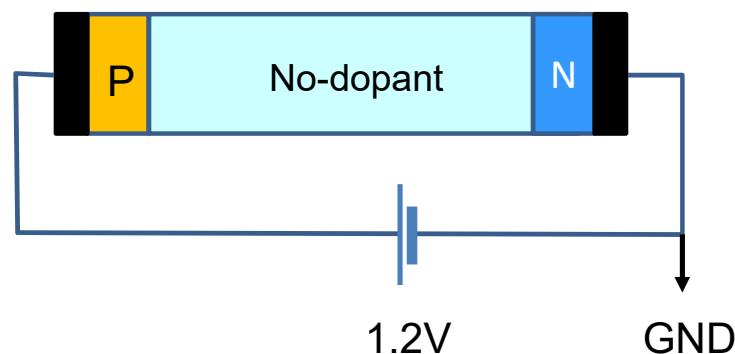
$$V_{built-in} = 2 \frac{kT}{q} \ln \frac{n_{stored}}{n_i}$$

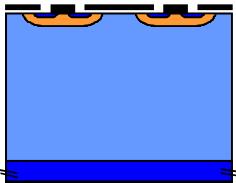
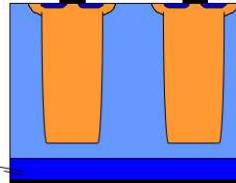
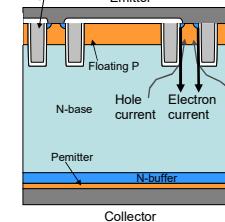


Problem: Draw potential distribution in PiN diode and electronce



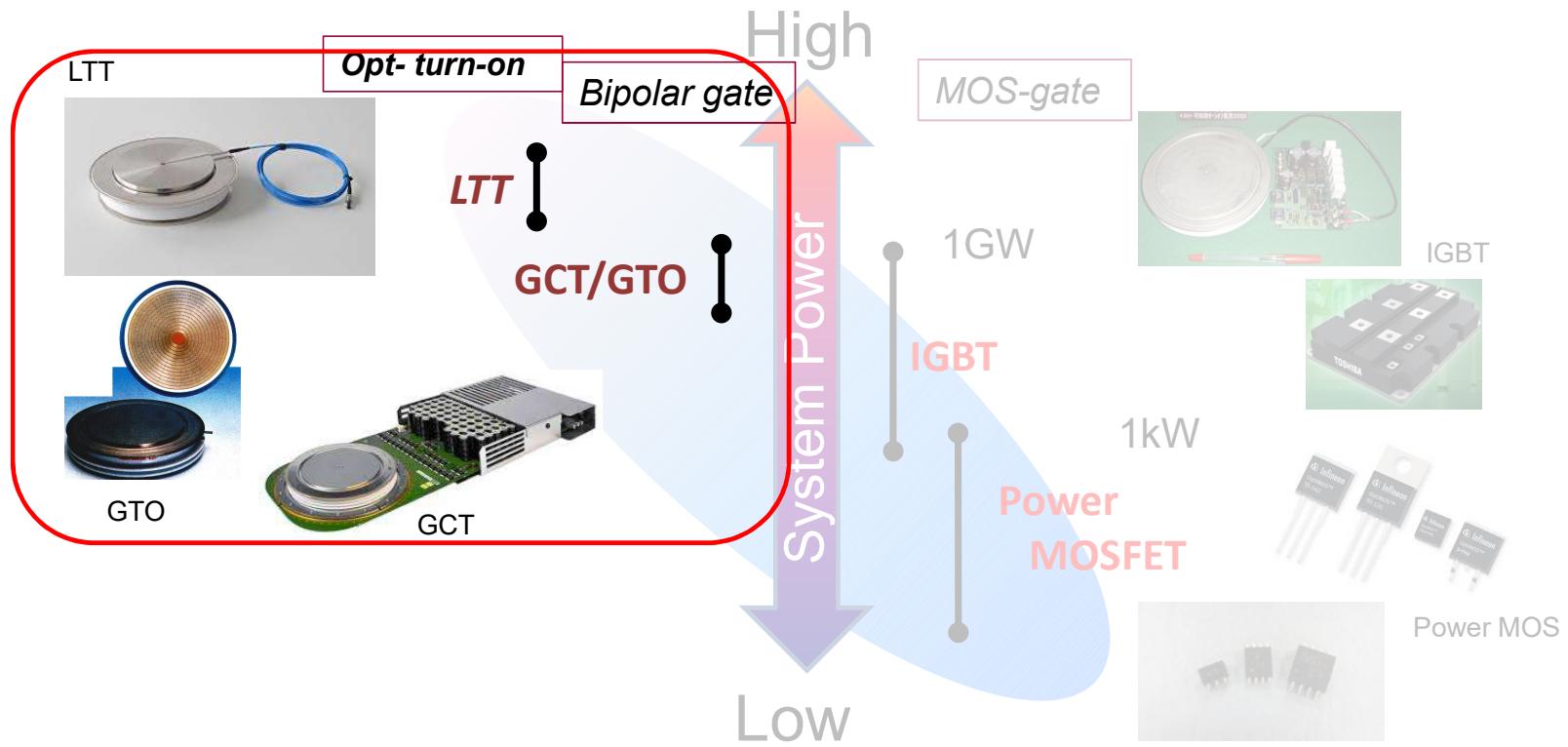
Problem: Draw potential distribution in PiN diode, assume constant stored carrier  $n_{store}$



	DMOSFET	SJ-MOSFET	IGBT
<b>Device Structure</b>			
<b>Drift Layer Doping (Stored carrier density)</b>	$N_D = \varepsilon \cdot \frac{E_{crit}^2}{2qV_B}$	$N_D = \varepsilon \cdot \frac{\sqrt{2}E_{crit}}{qW_{column}}$	$n_{stored}$ ( $>10^{16}\text{cm}^{-3}$ )
<b>Drift Layer Length (N-base length)</b>	$L_{drif} = \frac{2V_B}{E_{crit}}$	$L_{drif} = \frac{\sqrt{2} V_B}{E_{crit}}$	$L_{n-base} = \frac{1 \sim 2 V_B}{E_{crit}}$
<b>Drift Layer Resistance (N-base conduction resistance)</b>	$R_{drift} = \frac{4V_B^2}{\mu_n \varepsilon E_{crit}^3}$	$R_{drift} = \frac{2V_B \cdot W_{column}}{\mu_n \varepsilon E_{crit}^2}$	$R_{N-base} = \frac{1 \sim 2 V_B}{q(\mu_n + \mu_p) \cdot n_{stored} \cdot E_{crit}}$
<b>PN-junction built-in potential</b>	none	none	$V_{built-in} = 2 \frac{kT}{q} \ln \frac{n_{stored}}{n_i}$
<b>600V class device</b>	80-100 $\text{m}\Omega\text{cm}^2$	<10 $\text{m}\Omega\text{cm}^2$	~1.5V at 200A/cm <sup>2</sup>
	Assumption: N-column and P-column are same width		(flat carrier stored carrier distribution is assumed)

	DMOSFET	SJ-MOSFET	IGBT
<b>Device Structure</b>			
<b>V-I characteristics</b>			
<b>Switching charge (turn-off charge)</b>	 Charge in main-junction capacitance	 PN-column depletion charge	 Stored carrier sweep out

# Types of Power Semiconductors

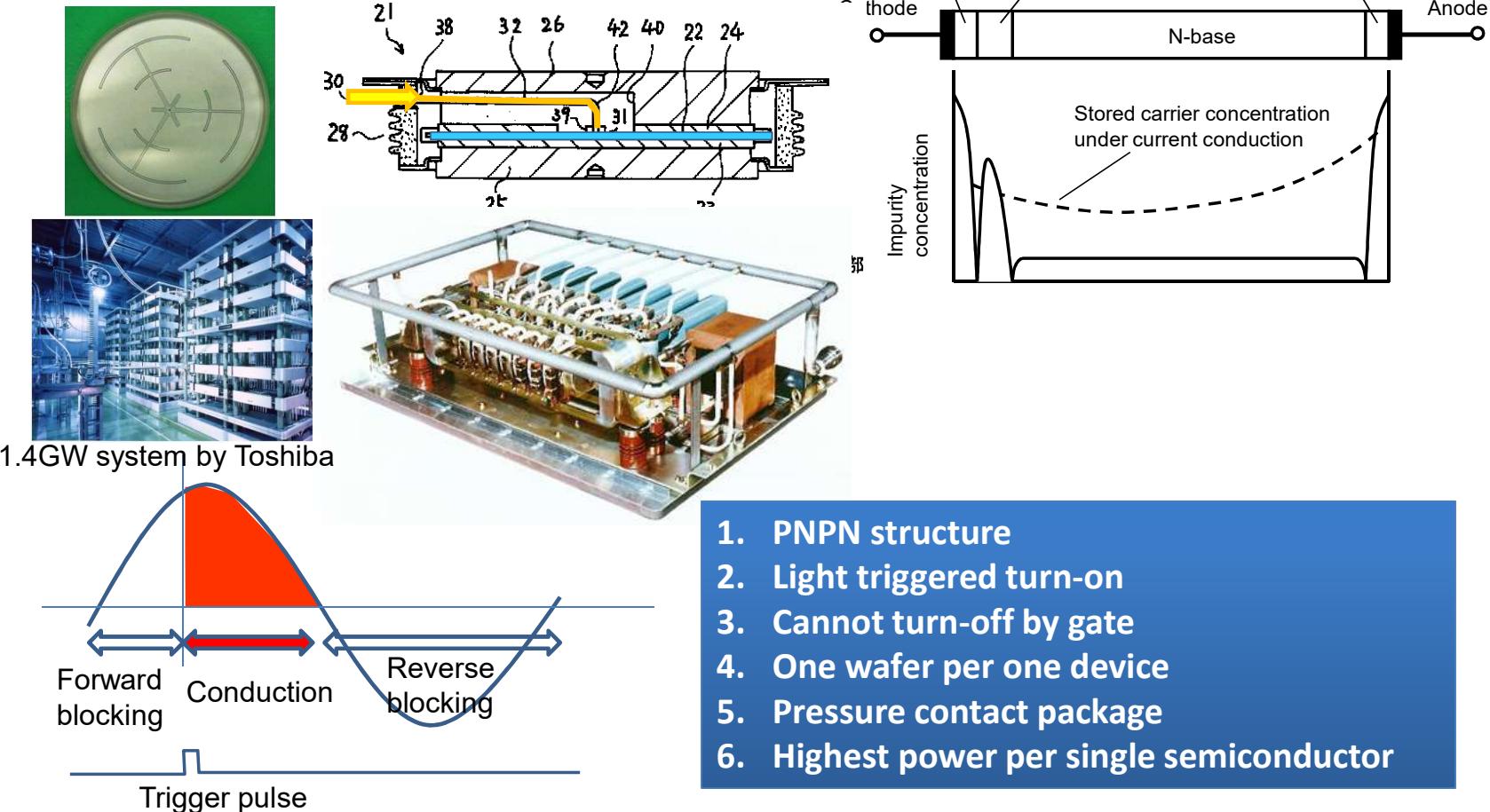


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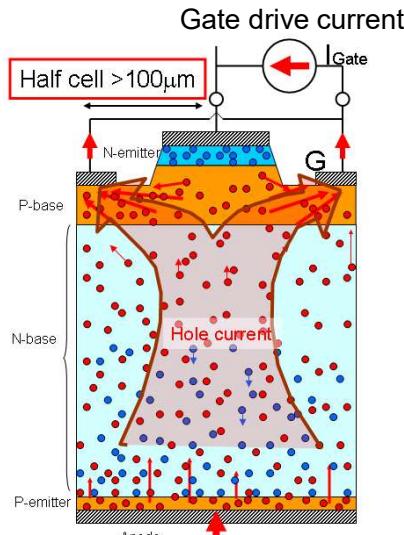
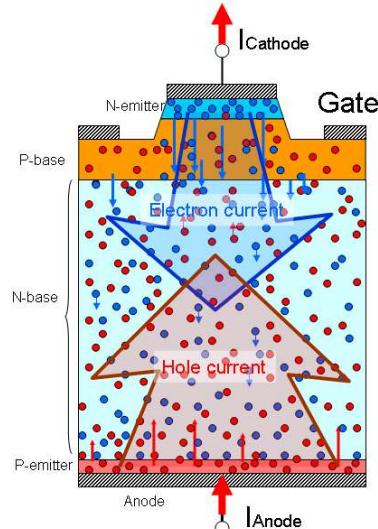
Photos:  
Infineon  
Toshiba  
ABB  
TMEIC

# Light Triggered Thyristor(LTT)

Photos: <http://dbnst.nii.ac.jp/>



# GCT: Gate Commutated Turn-off Thyristor



1. PNPN structure
2. One wafer per one device
3. > 100um cell size
4. Pressure contact package
5. Very low stray inductance integrated gate driver for couple of kA gate current
6. Highest power per single semiconductor turn-off device



ABB

Figure 1: A 91 mm HPT IGCT wafer with approximately 2700 cathode segments organized into ten segment rings. The gate metallization covers the rest of the wafer and surrounds all segments. The gate-contact ring separates the five peripheral segment rings from the central rings.



ABB

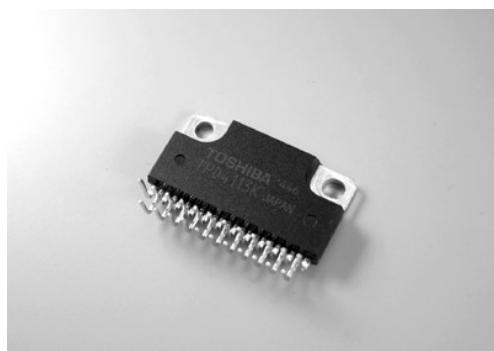
5.5kV, 5kA HPT IGCT  
Integrated gate circuit

# Lateral Devices

## Control and Power = Power IC

Motor Driver

$\sim 1\text{kV}$



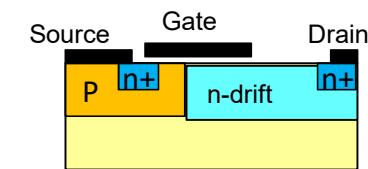
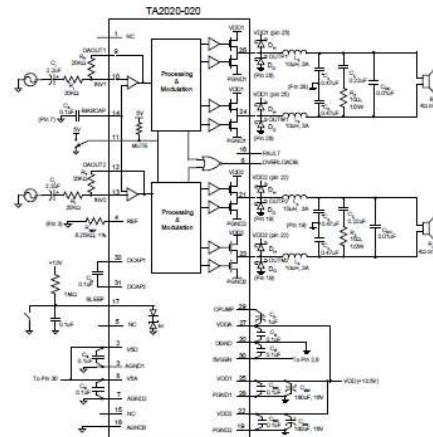
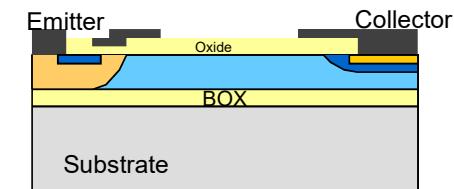
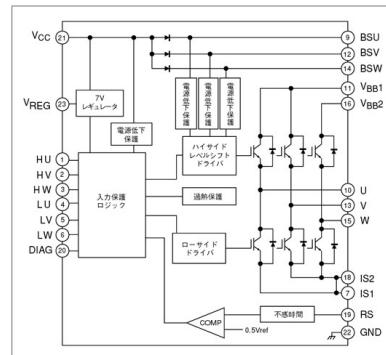
Toshiba

Audio Speaker Driver

$<100\text{V}$

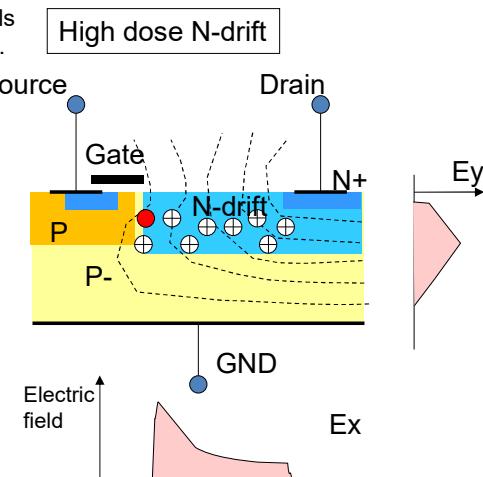
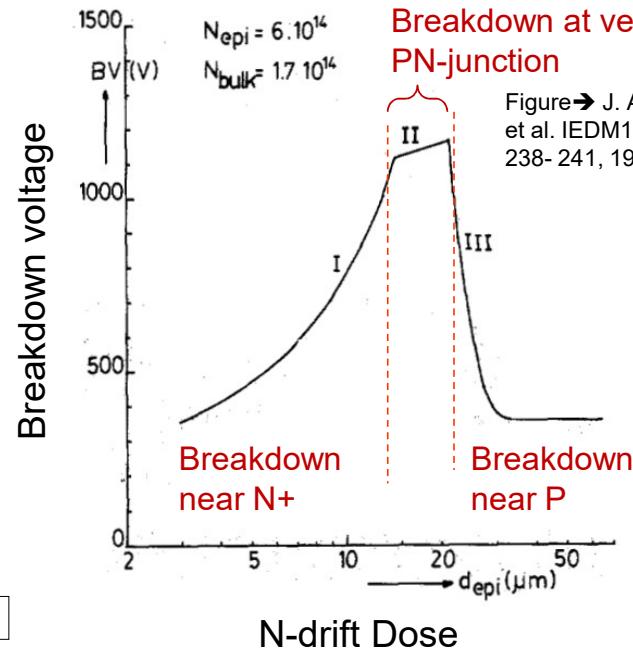
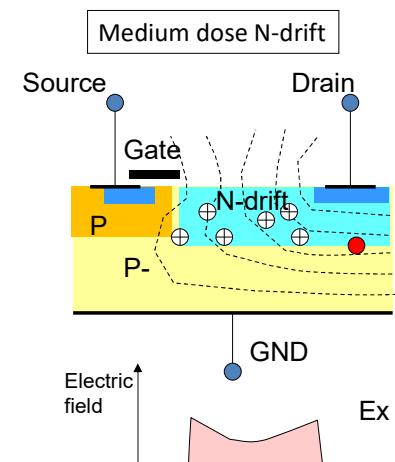
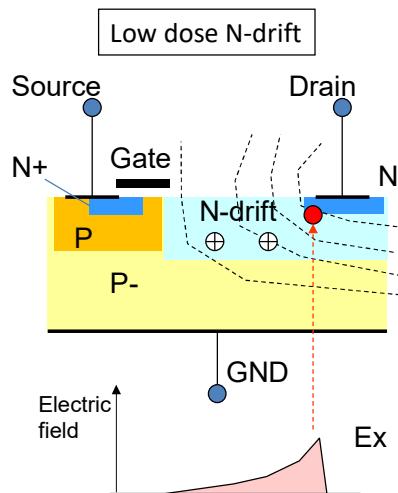


Trypath datasheet



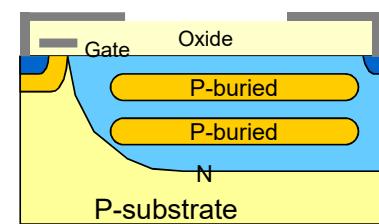
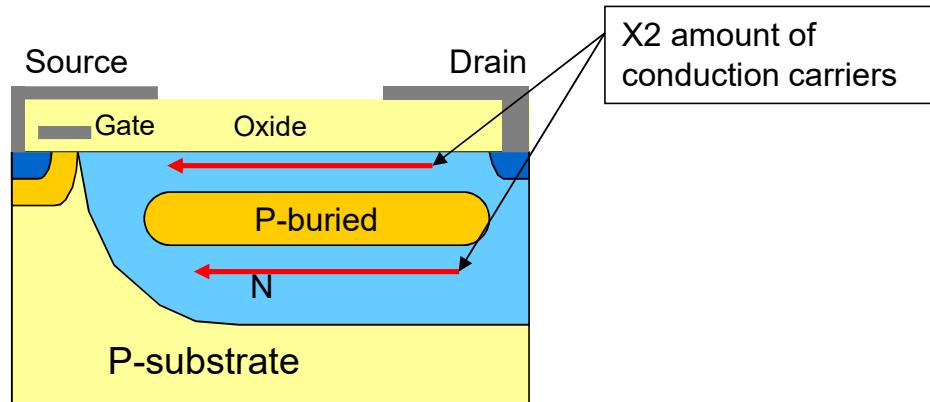
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# RESURF principle for breakdown voltage design



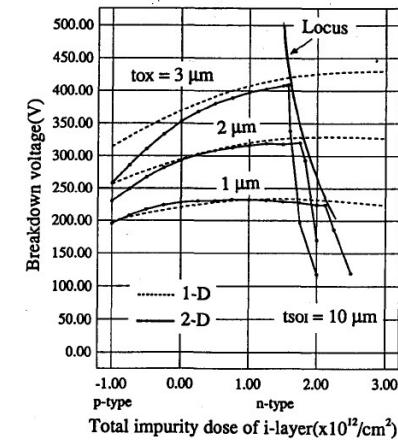
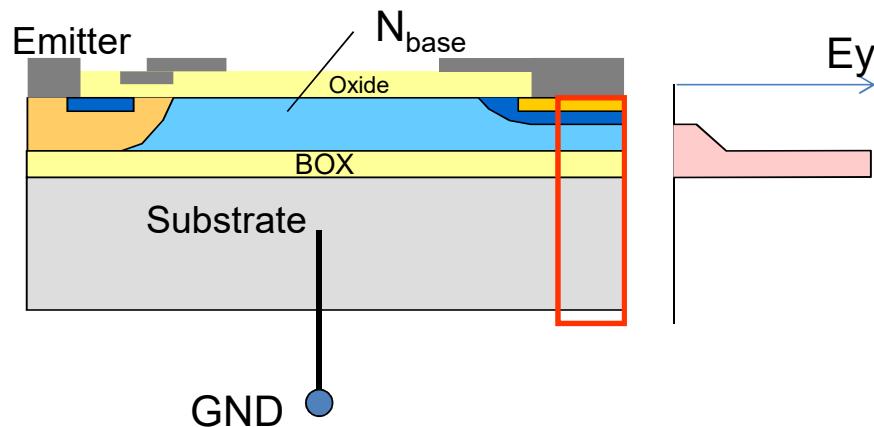
N-drift dose ( $\text{atm}/\text{cm}^2$ ) is the key parameter for breakdown voltage design ( $\sim 1\text{e}12/\text{cm}^2$ )

# Lateral “Super Junction” MOSFET



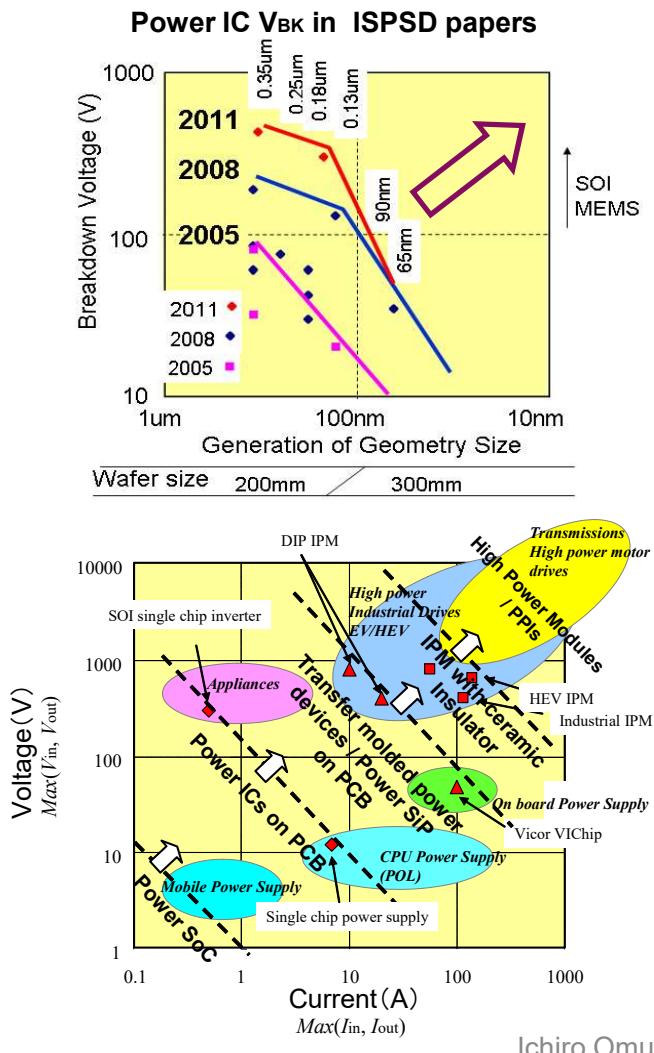
D. Disney et al. A new 600V lateral PMOS device with a buried conduction layer, pp.41-44, ISPSD' 03

## SOI IGBT



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# Future Power ICs



Future HV Power IC will be ...

*Digital Rich*  
Power IC

*Kilowatt*  
Power IC

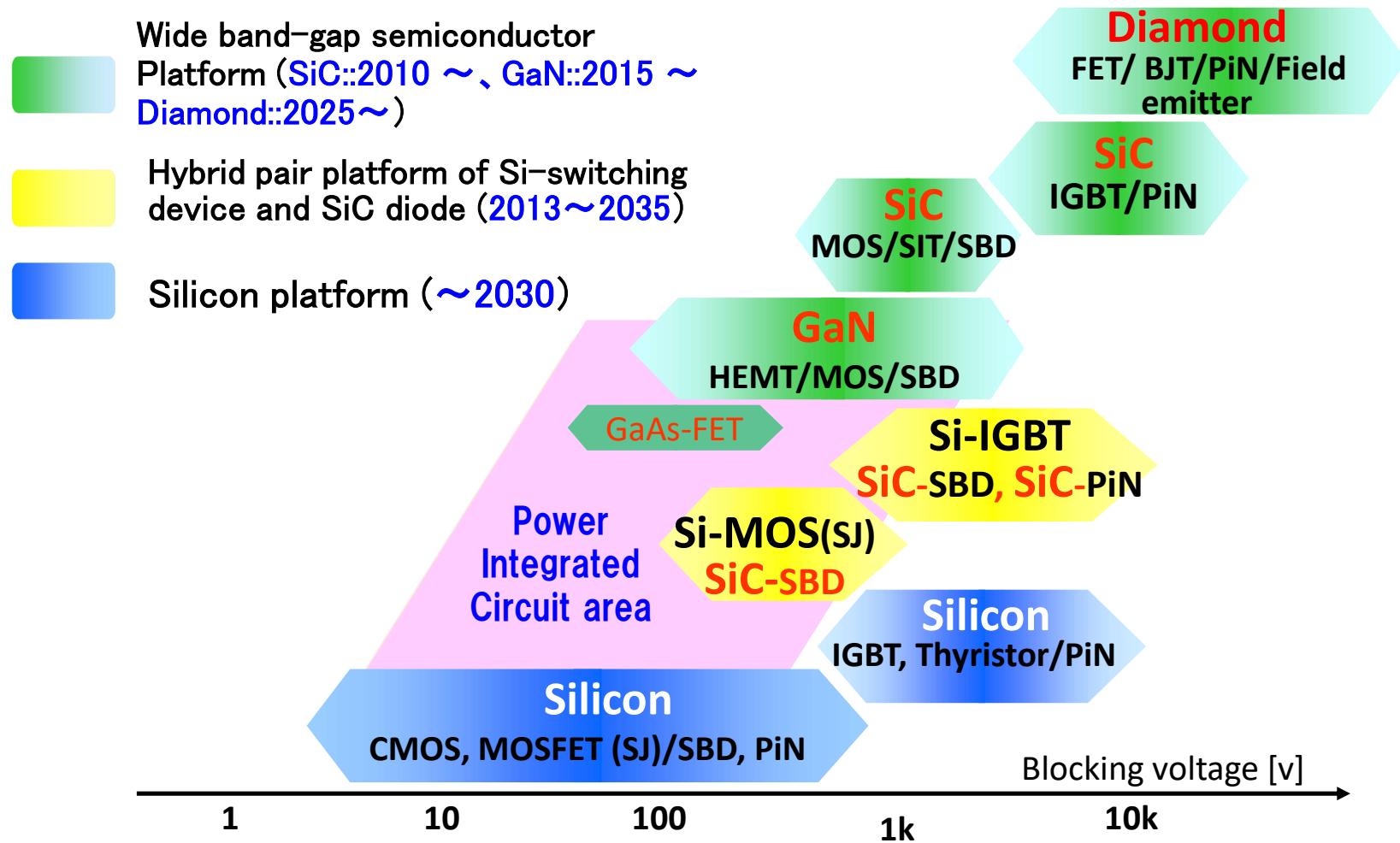
Ichiro Omura Kyushu Inst. Tech.

Omura, ECPE workshop Jan. 2012

Omura, CIPS 2010

# Future Possibility

# Advanced power devices Road map



H. Ohashi et al. "Role of Simulation Technology for the Progress in Power Devices and Their Applications," IEEE T-ED, Vol. 60, issue 2, 2013.

# Future possibility

- 1) Si-power devices still have much room for development toward ultimate MOSFETs and IGBTs.
- 2) The combination of Si-switching devices and SiC freewheeling diodes will be a significant step not only for strengthening the SiC market but also for Si-device development.
- 3) Si-IGBT will be replaced by SiC MOSFET in the voltage range of more than 1000 V in some applications, and SiC-IGBT has the potential to be used for applications of more than 10 kV. (Si-IGBT for volume market, SiC for high end market)
- 4) GaN power devices will replace some of Si-power ICs and will be used for faster switching applications.
- 5) The unique properties of diamond have potential for new power devices particularly in high-voltage applications.
- 6) The ultimate CMOS has the potential to be used for power integrated devices in ICT applications.

H Ohashi, I Omura - IEEE transactions on electron devices, 2013

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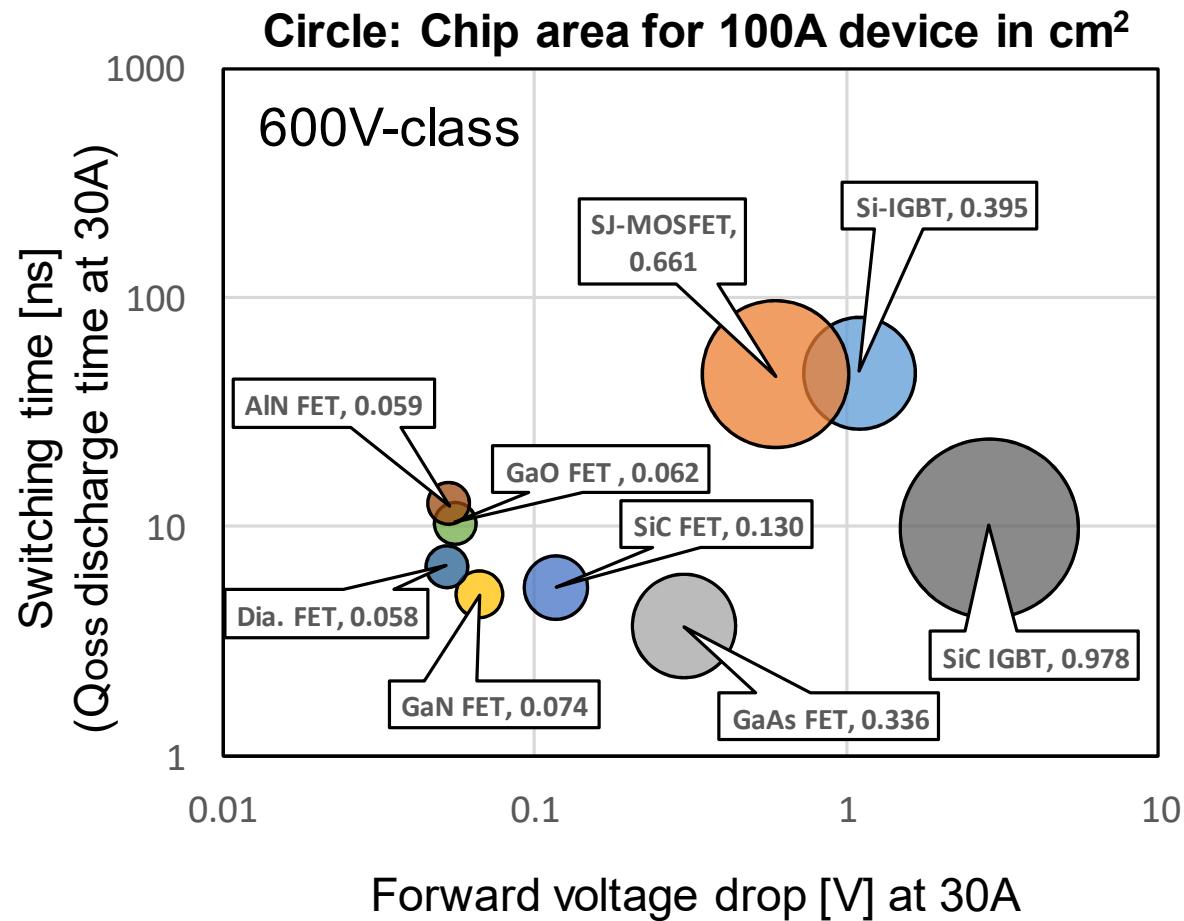
# Possible applications for WBG devices

Application	System Power, voltage	Typical Device type	Typical Circuit topology	Device Voltage and current	Switching Frequency	Package	WBG device possibility
UHVDC	1GW-8GW -800kV	Thyristor	MMC / series connected	4.5kV-8kV 3kA-5kA	50-60Hz	Pressure contact	>25kV SiC/GaN double injection bipolar, >50kV diamond device
HVDC	50MW-1GW 40kV – 250kV	IGBT	MMC / series connected	2.5kV-6.5kV 2kA-3kA	>50Hz	Pressure contact	>25kV SiC/GaN double injection bipolar, >50kV diamond device
Medium voltage AC drives / Traction	1MW-50MW	IGBT IGCT (GTO)	2-level / 3-level voltage source inverter	2.5kV-6.5kV 0.5kA-8kA	>300Hz	Module, Pressure contact	WBG vertical unipolar device with new topology at higher frequency, 13-25kV Double injection bipolar with high frequency 2-level
EV/HEV power train	10-200kW	IGBT	2-level voltage source inverter / chopper	500V-1000V 100A-500A	1kHz-5kHz	6 in 1, 12 in 1 module, water cooled	Vertical unipolar device, higher frequency
Wind-farm	1MW-5MW	IGBT	2-level / 3-level voltage source inverter	1000V-6.5kV 500A-2.5kA	500Hz-5kHz	DBC Module, Pressure contact	Vertical unipolar device
Large scale PV-inverter	100kW-3MW	IGBT	2-level / 3-level voltage source inverter	1000V-6.5kV 500A-2.5kA	500Hz-5kHz	DBC Module	Vertical unipolar device
Data center HVDC	100kW-1MW	IGBT, SJ-MOSFET	Isolated DC-DC	800-1.2kV 25A-250A	>10kHz	Transfer molded discrete, DBC Module	Vertical unipolar device, higher frequency
Appliance (Air-conditioner)	1kW-2kW	IGBT / SJ-MOSFET	2-level voltage source inverter	600V 5A-10A	1-10kHz	Transfer molded module	WBG Power IC
IH-cooker	1-3kW	IGBT	Soft switching	600V 5A-10A	30kHz-	Transfer molded discrete	WBG Power IC
EV Quick charger	20-50kW	IGBT SJ-MOSFET	2 level converter, Isolated DC-DC	600V-1200V 20A-100A	5kHz-50kHz	Transfer molded discrete, DBC module	Vertical unipolar device, higher frequency
EV charger	1.5-5kW	IGBT SJ-MOSFET	2 level converter Isolated DC-DC	600V 5-10A	5-50kHz	Transfer Molded discrete, DBC module	Vertical unipolar device, power IC with higher frequency

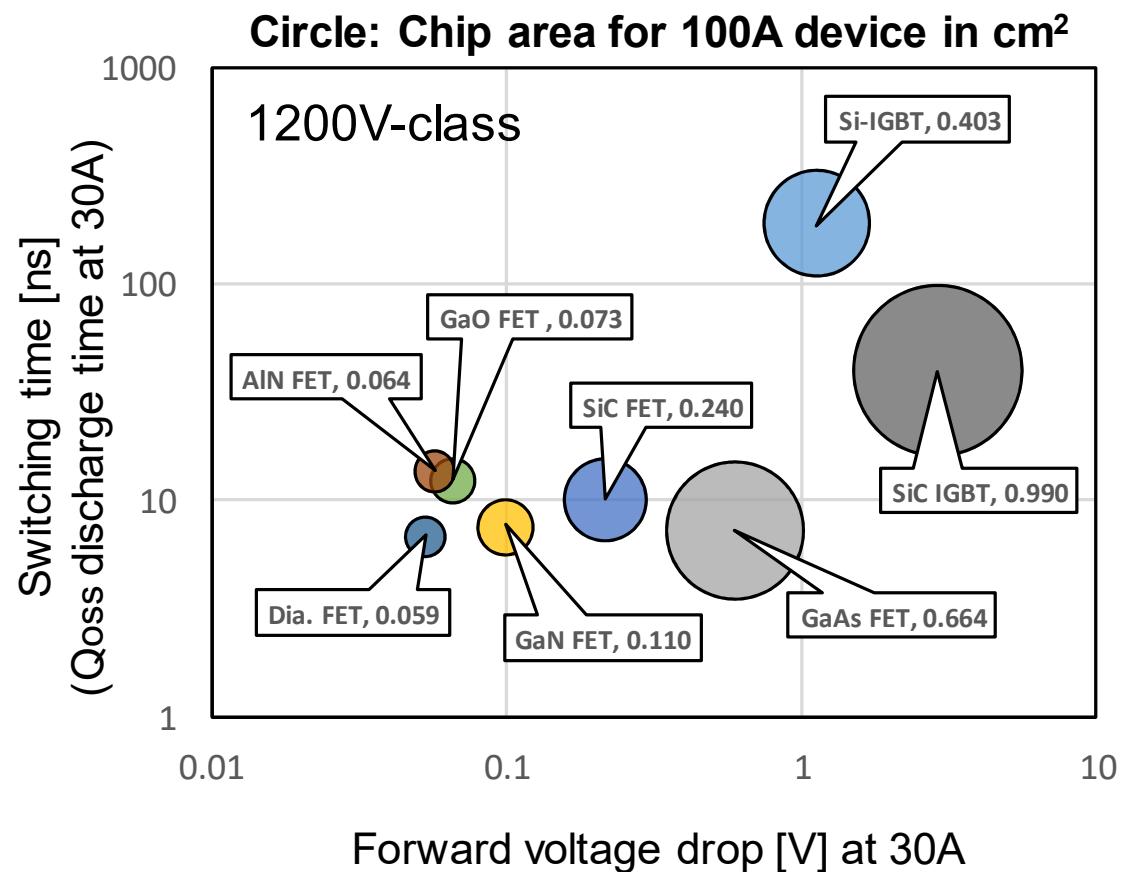
## Calculation assumptions (vertical devices)

Items	Values and assumptions	Remarks
<b>Device voltage</b>	600V, 1200V, 4.5kV, 25kV classes	20% margin added for breakdown voltage
<b>FET model</b>	Classical model with triangle electric field distribution along N-drift	
<b>Superjunction model</b>	P-column and N-column has same aspect ration of 10.	
<b>IGBT model (Double injection device model)</b>	Flat stored carrier distribution in N-base is assumed (i.e. sufficiently long carrier lifetime is assumed) with giving stored carrier density of $1.0\text{-}2.0\text{e}16/\text{cm}^3$ . Forward offset voltage is calculated from the ratio of stored carrier density to intrinsic carrier density.	Soft Punch-through design for IGBT.
<b>Conduction loss density limit</b>	$\leq 300\text{W/cm}^2$ for 600V and 1200V, $\leq 200\text{W/cm}^2$ for 4.5kV, $\leq 100\text{W/cm}^2$ for 25kV	Used for chip area calculation
<b>Series resistances</b>	Total series resistance (sum of channel resistance, JFET resistance, substrate resistance, contact resistance etc. ) is assumed to be $0.1\text{m}\Omega\text{cm}^2$	Series resistance is added to device resistance
<b>Chip area for 100A device</b>	Chip active area is determined to fit the conduction loss density ( $\text{W/cm}^2$ ) limit for 100A conduction. Edge termination area is not included.	Corresponding to chip area for rated current of 100A
<b>Forward voltage drop (at 30A)</b>	Voltage drop at conduction current of 30A	30% of rated current as average operation condition
<b>Switching time (at 30A)</b>	Discharge time of $Q_{\text{OSS}}$ at 30A switching. $Q_{\text{OSS}}$ is set to N-drift depletion charge at half of device voltage for FET, PN column depletion charge for SJ-MOSFET and open base turn-off charge for sweeping out total stored charge in N-base for IGBT. Ichiro Omura Kyushu Inst. Tech.	30% of rated current

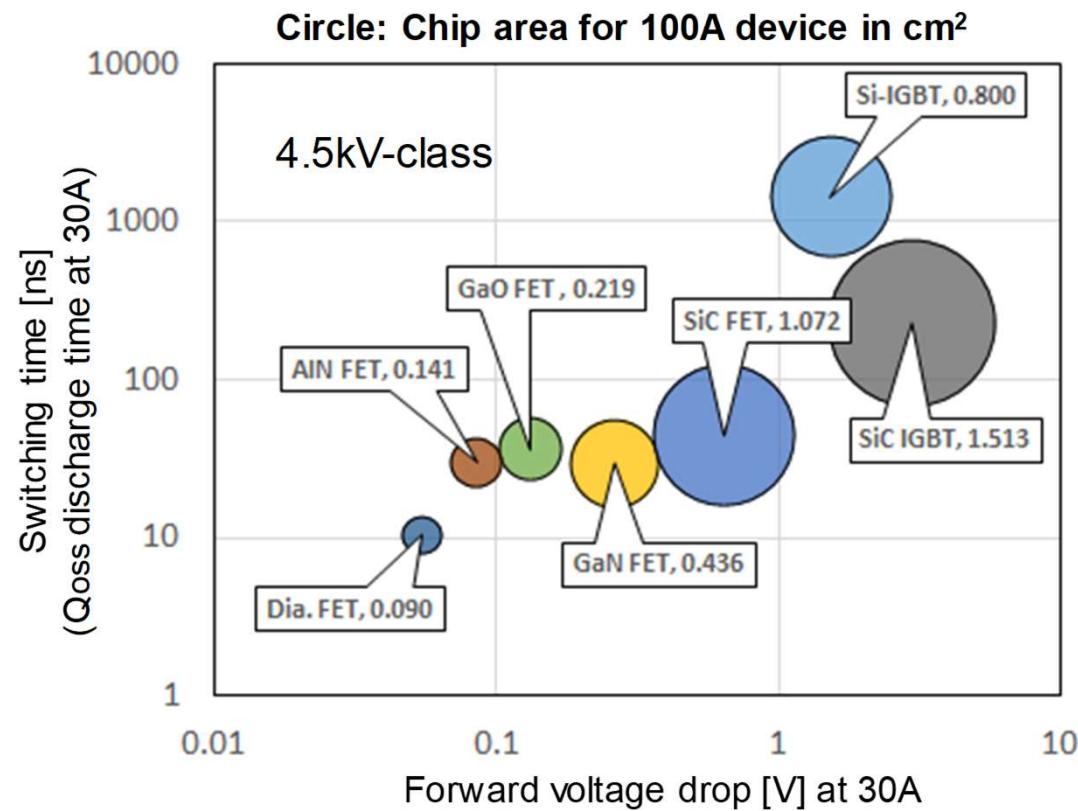
## 600 V case comparison



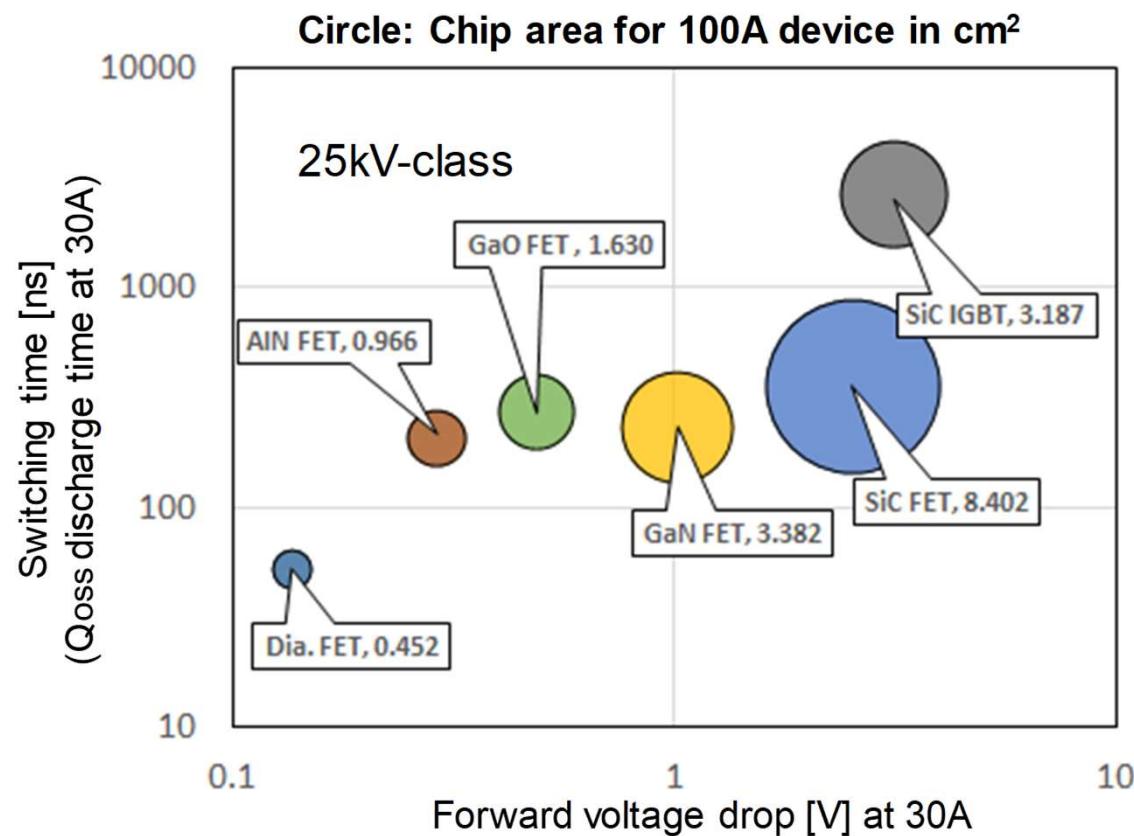
## 1200V case comparison



## 4.5kV case comparison



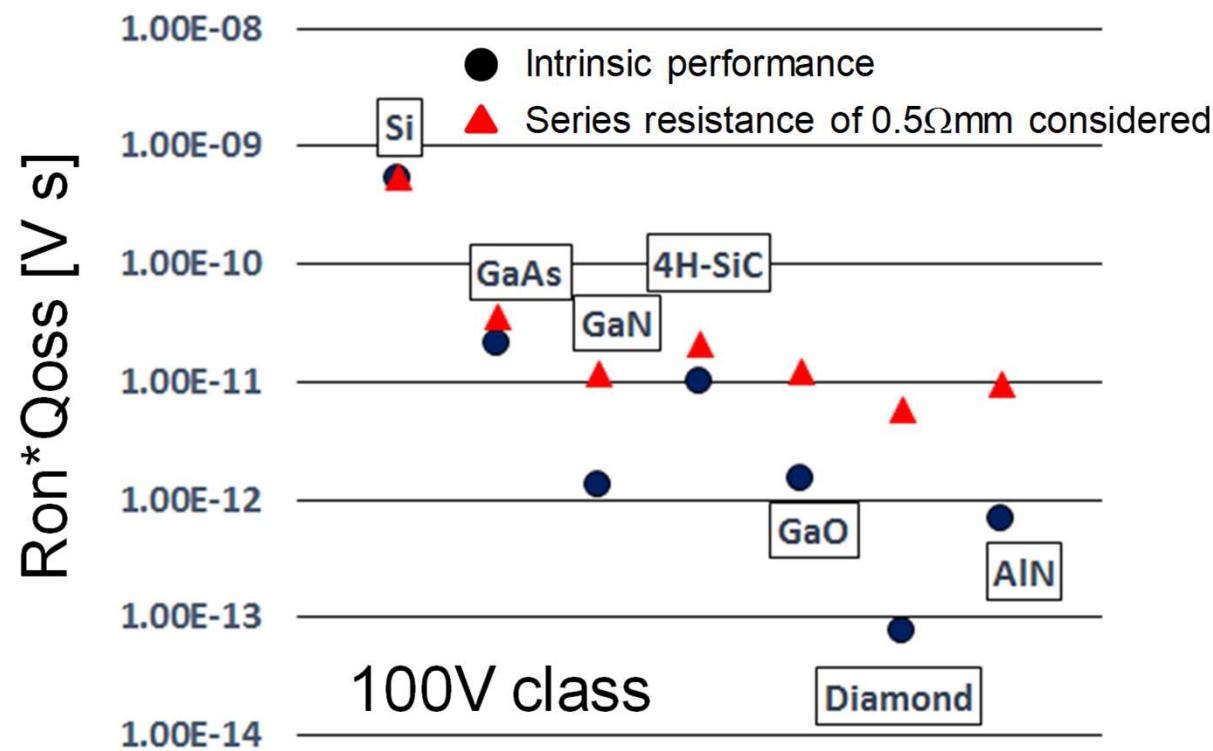
## 25kV case comparison



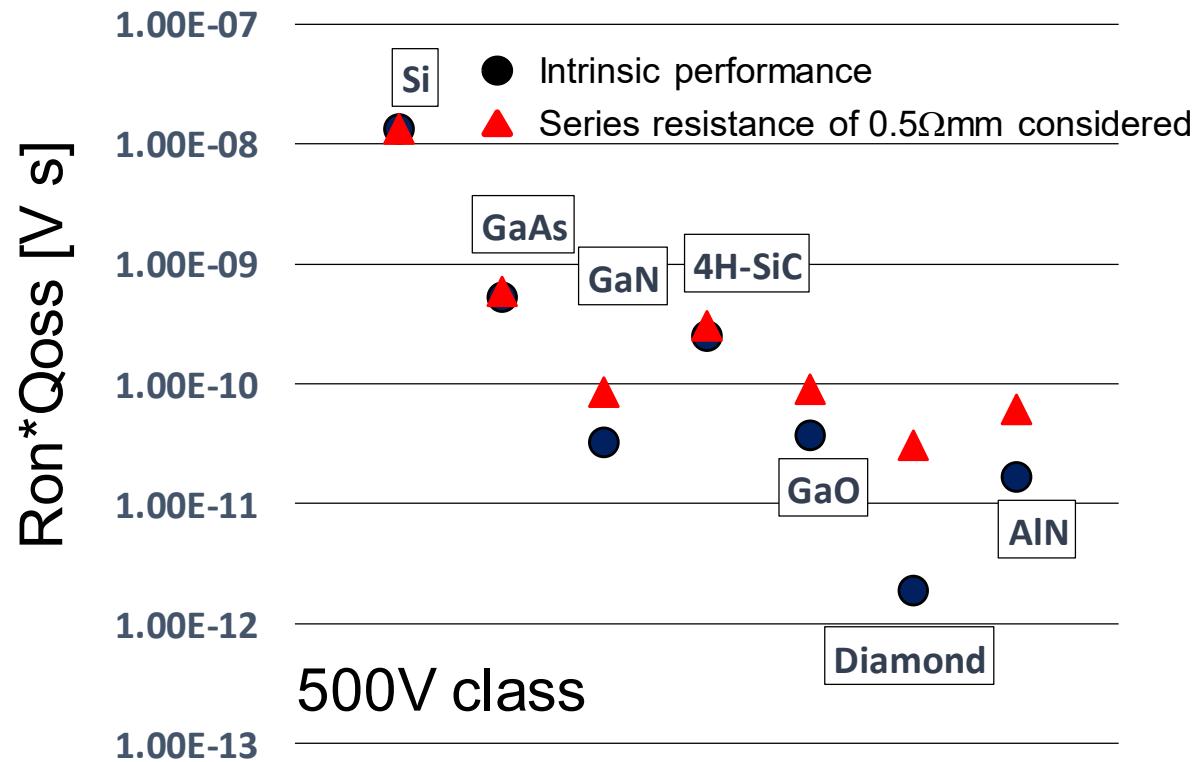
# Calculation assumptions (Lateral devices)

Items	Values and assumptions	Remarks
<b>Device voltage</b>	100V, 500V classes	20% margin added for breakdown voltage
<b>Drift layer model</b>	Critical electric field is decomposed to horizontal part and vertical part so that horizontal part is used for drift layer length calculation and vertical part field for drift layer conduction charge density calculation.	
<b>Qoss/W</b>	Assumed to be total conduction electron charge in drift layer for device width W	
<b>Ron*W</b>	-Intrinsic drift layer resistance for device width W or -Sum of intrinsic drift layer resistance and additional series resistance of $0.5\Omega\text{mm}$ . The series resistance represents channel resistance, contact resistance etc.	2DEG mobility is used for GaN
<b>Ron*Qoss</b>	FOM for high voltage lateral high speed device.	Gate driving effect is not included in the model

## 100 V case comparision



## 500V case comparison

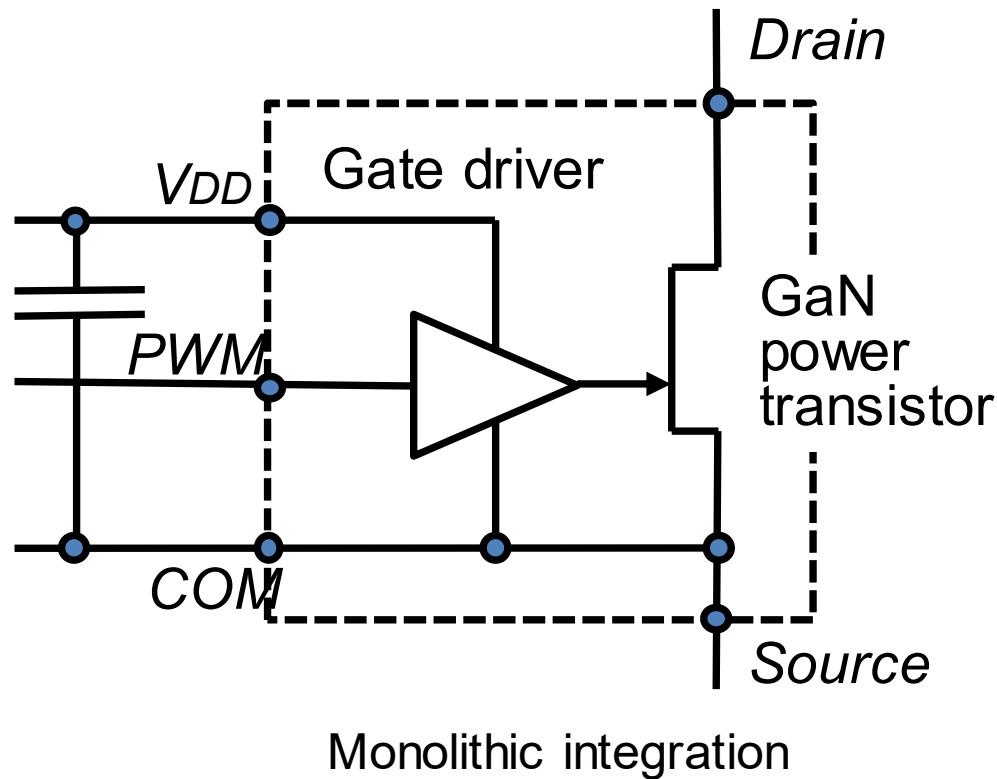


## Reference GaN device integration possibility

	<b>Power Device</b>	<b>Gate drive / signal isolation</b>	<b>Analog</b>	<b>CMOS like logic</b>
<b>Feature size</b>	<1 micron	<0.5 micron +high gm	0.35-1 micron	<0.25 micron
<b>Number of metal layers</b>	1-2 layers	2 layers	>2 layers	>> 2 layers
<b>Frequency</b>	10 kHz for motor drive ~10 MHz for power supply >10 MHz for class E, F	100 kHz 100 MHz >100 MHz	100 kHz 100 MHz >100 MHz	(>1GHz)
<b>Voltage</b>	400V-1200V for motor drive and AC/DC, DC/AC 30-200V for DC/DC	5 V for gate drive + high voltage signal isolation	3.3 V – 5 V	<2.5V
<b>Power loss</b>	-	1-5% of power device	1% of power device	1-5% of power device
<b>Uniformity across wafer/ Wafer bending</b>	Depends on wafer handling yield	Wafer bending < 10 micron	Severe uniformity required	Severe uniformity required
<b>Complementary transistor</b>	Not required	Better to have	Required	Indispensable
<b>Compact model</b>	Required	Required	Indispensable	Indispensable
<b>Technology barrier</b>	-	-	high	Very high

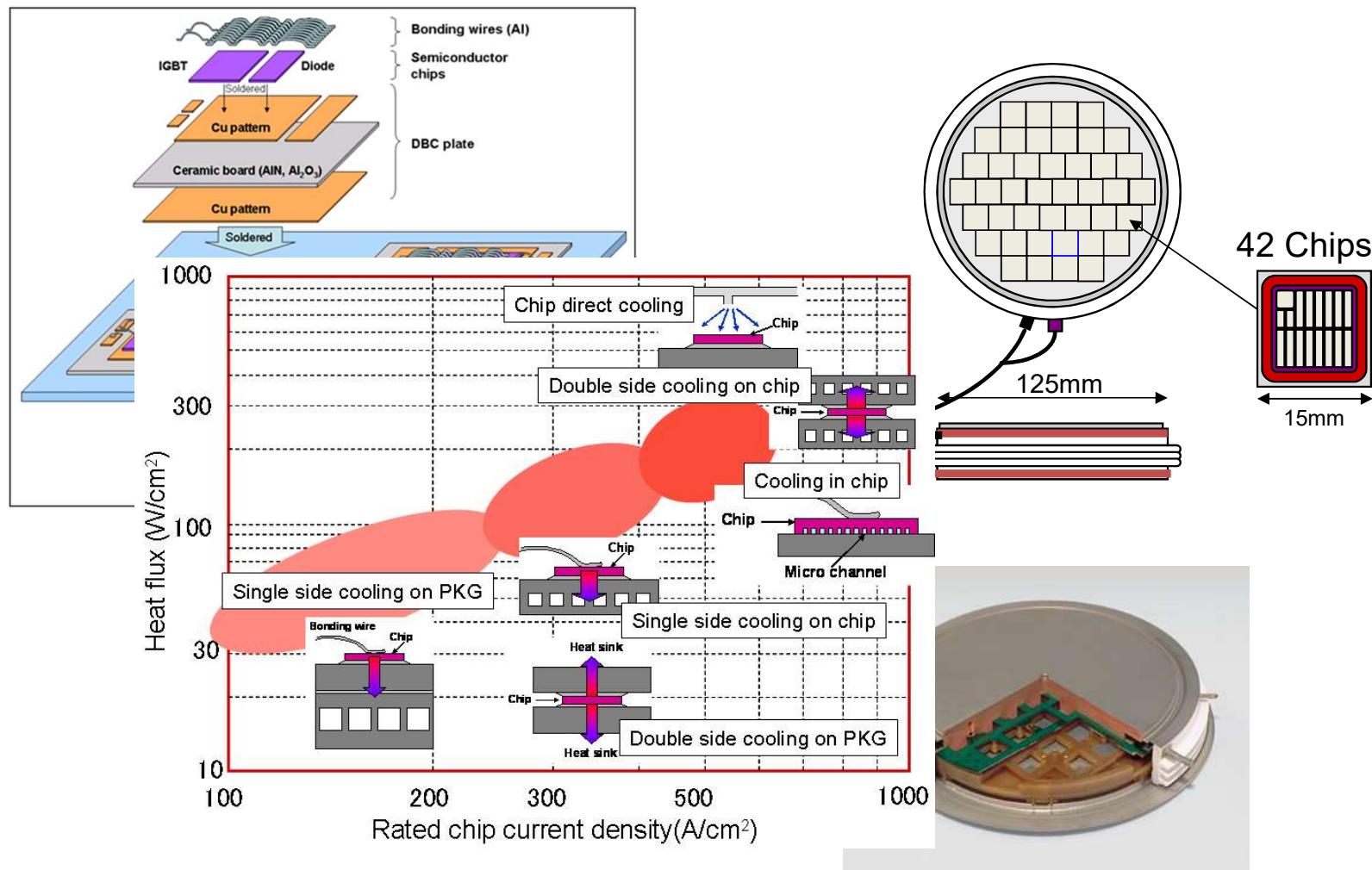
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# Navitas semiconductor solution



# Related Technology

# Examples of High Power IGBT Package



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Shen, Omura, "Power Semiconductor Devices for Hybrid, Electric, and Fuel Cell Vehicles" Proc. Of the IEEE, Issue 4, 2007

# Silicon wafer trend

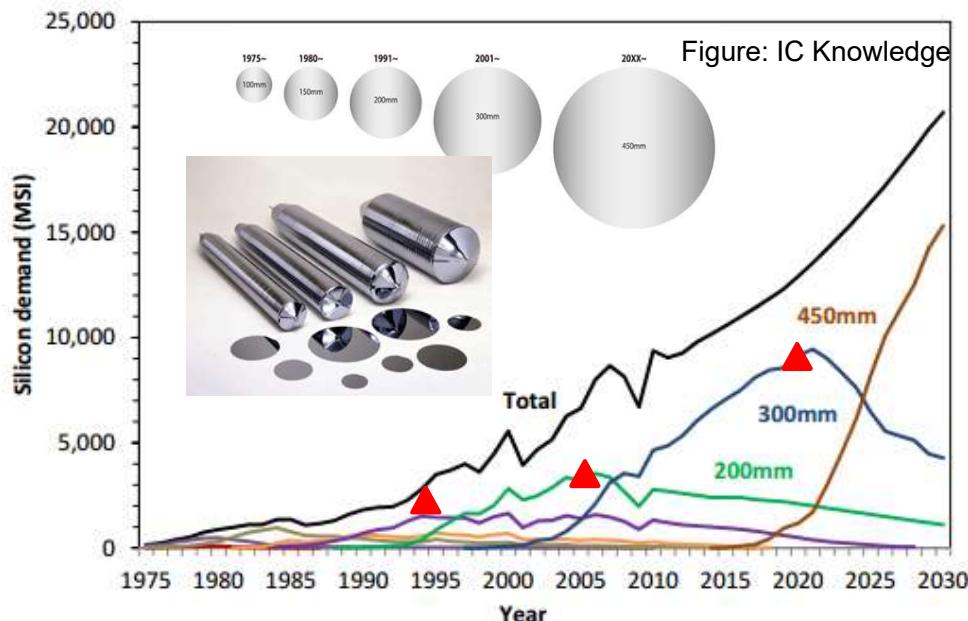
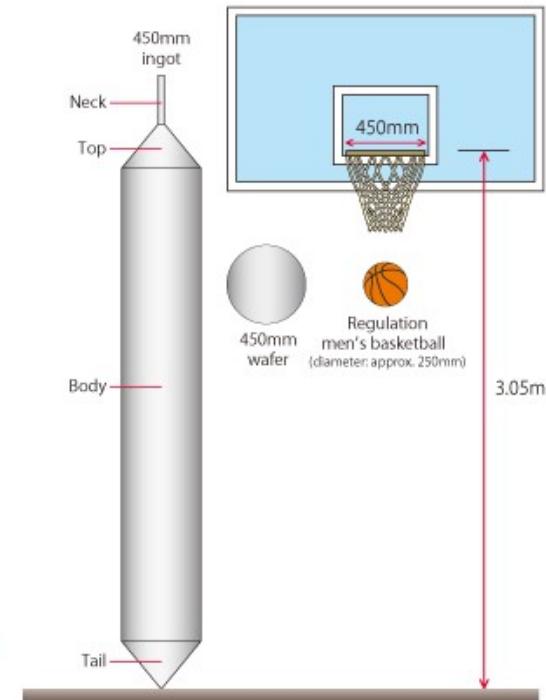


Figure 4. Worldwide Silicon Demand by Wafer Size [2].

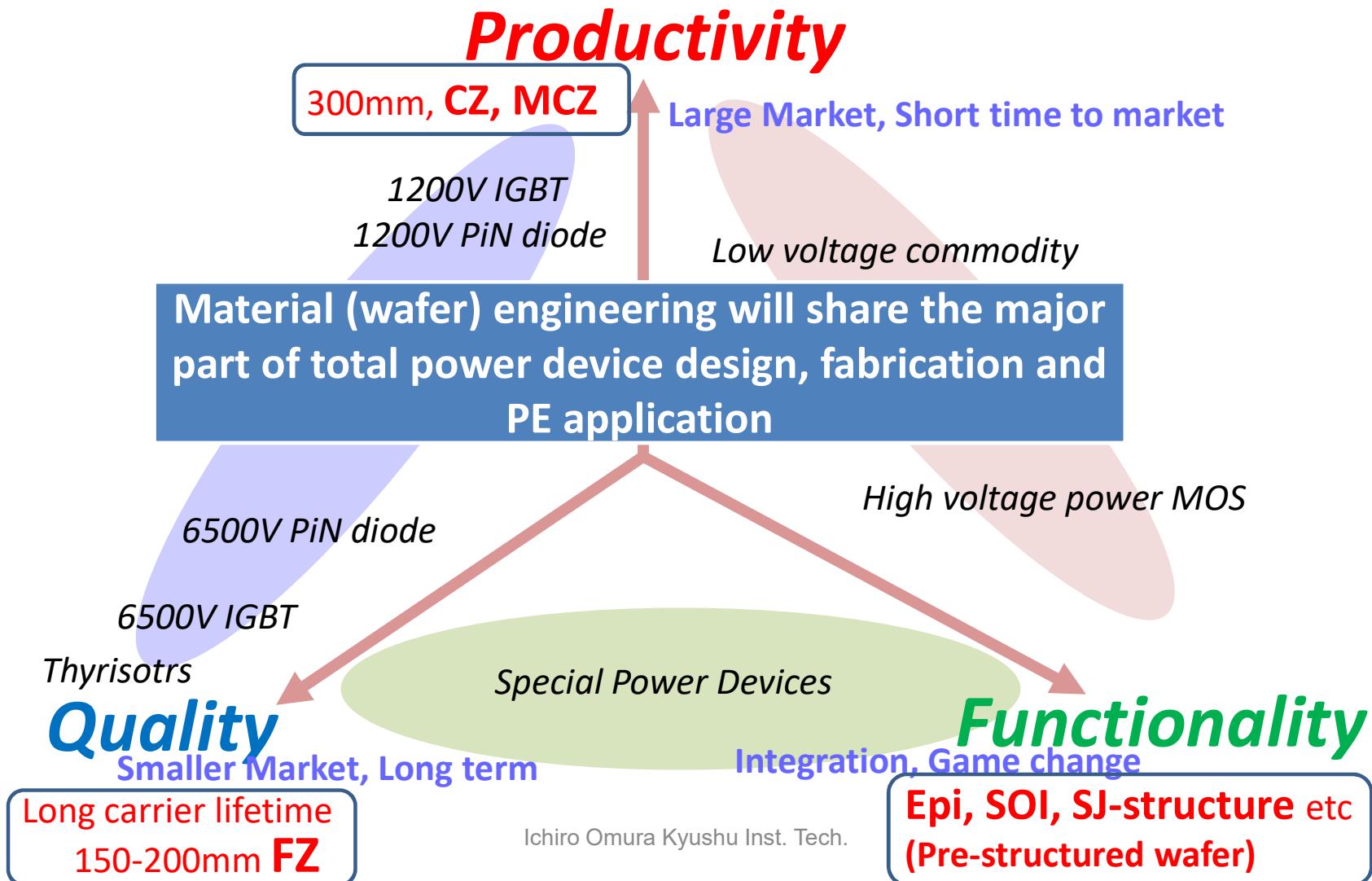


Interestingly, it is estimated that a 450mm silicon ingot would be roughly the same diameter and height as a basketball hoop.

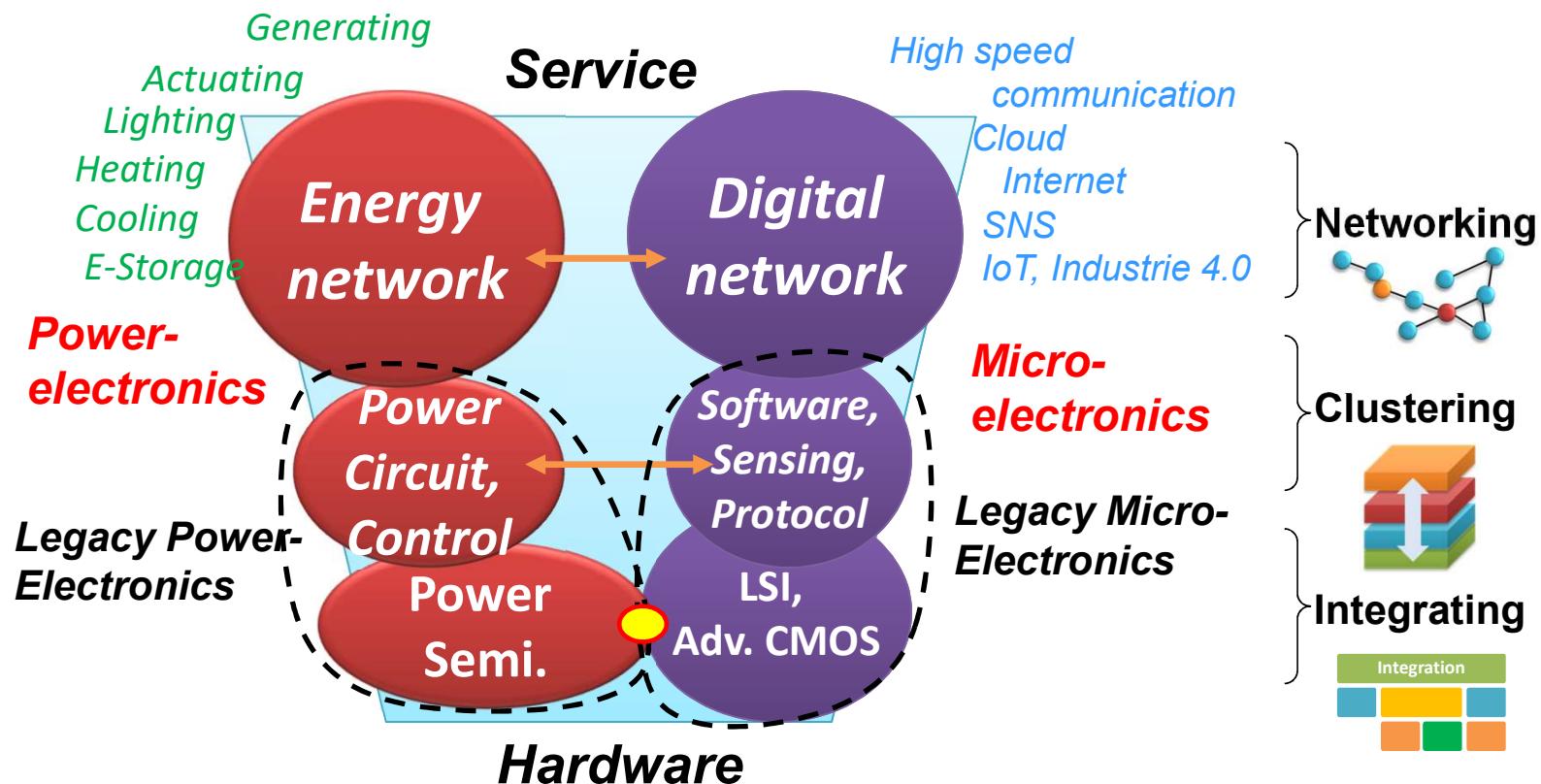
**SiMCO**

Strong productivity of wafer to meet huge demands

# Wafer technology(Silicon)



# Power electronics and micro electronics forming Cyber-Physical System



- Electron devices are the key technology for future energy networking
- New phase of electronics has started with close link between power and micro electronics for future sustainable society

See also

Z. John Shen, Ichiro Omura

Article Power Semiconductor Devices for Hybrid, Electric, and Fuel Cell Vehicles

Proceedings of the IEEE 05/2007; 95(4-95):778 - 789.

H. Ohashi and I. Omura “Role of Simulation Technology for the Progress in Power Devices and Their Applications,” IEEE T-ED, Vol. 60, issue 2, 2013.

P. Chow, I. Omura, M. Higashiwaki, H. Kawarada and V. Para, “Smart Power Devices and ICs Using GaAs and Wide and Extreme Bandgap Semiconductors,” IEEE Transactions on Electron Devices ( Volume: 64, Issue: 3, March 2017 )

