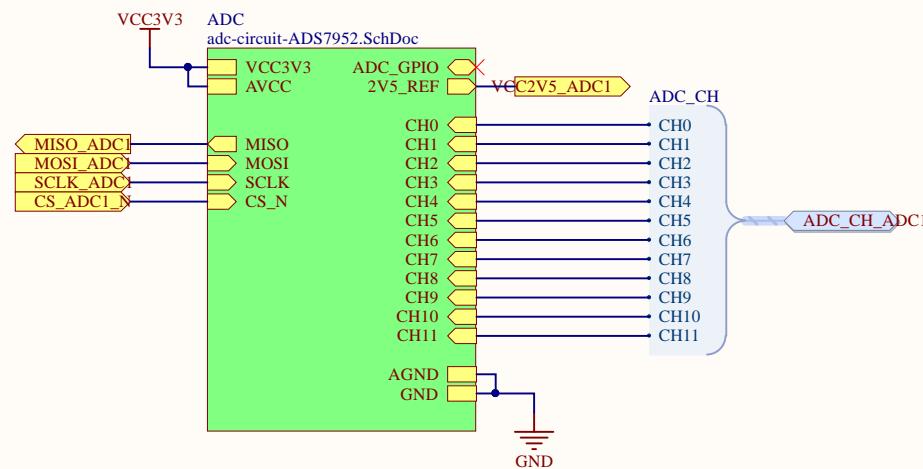


A

A

ANALOG TO DIGITAL CONVERTER



B

B

Breaks out the ADC channels into harnesses

D

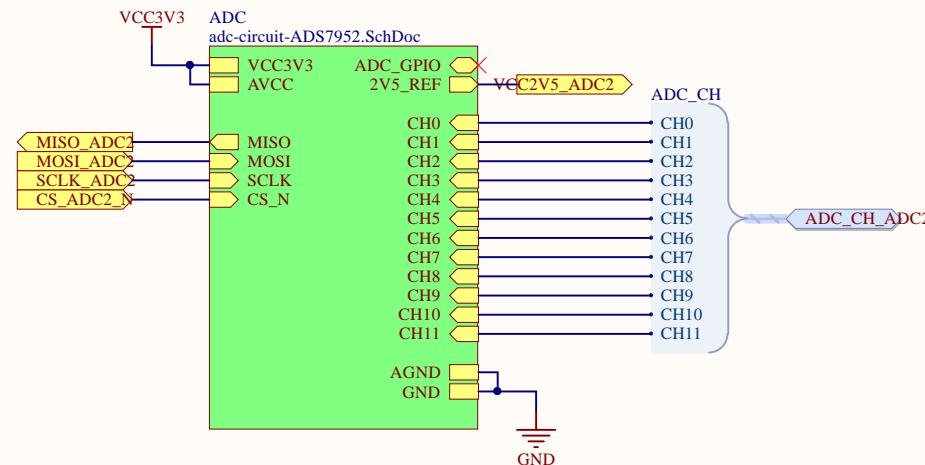
D

Title		UTAT SS
ADC Breakout.SchDoc		
Size	Number	Revision
A4	2.1	v4.2
Date:	2019-09-10	Sheet 2.1 of 47
File:	C:\Users\.\ADC Breakout.SchDoc	Drawn By: Lorna Lan, Dylan Vogel

A

A

ANALOG TO DIGITAL CONVERTER



B

B

Breaks out the ADC channels into harnesses

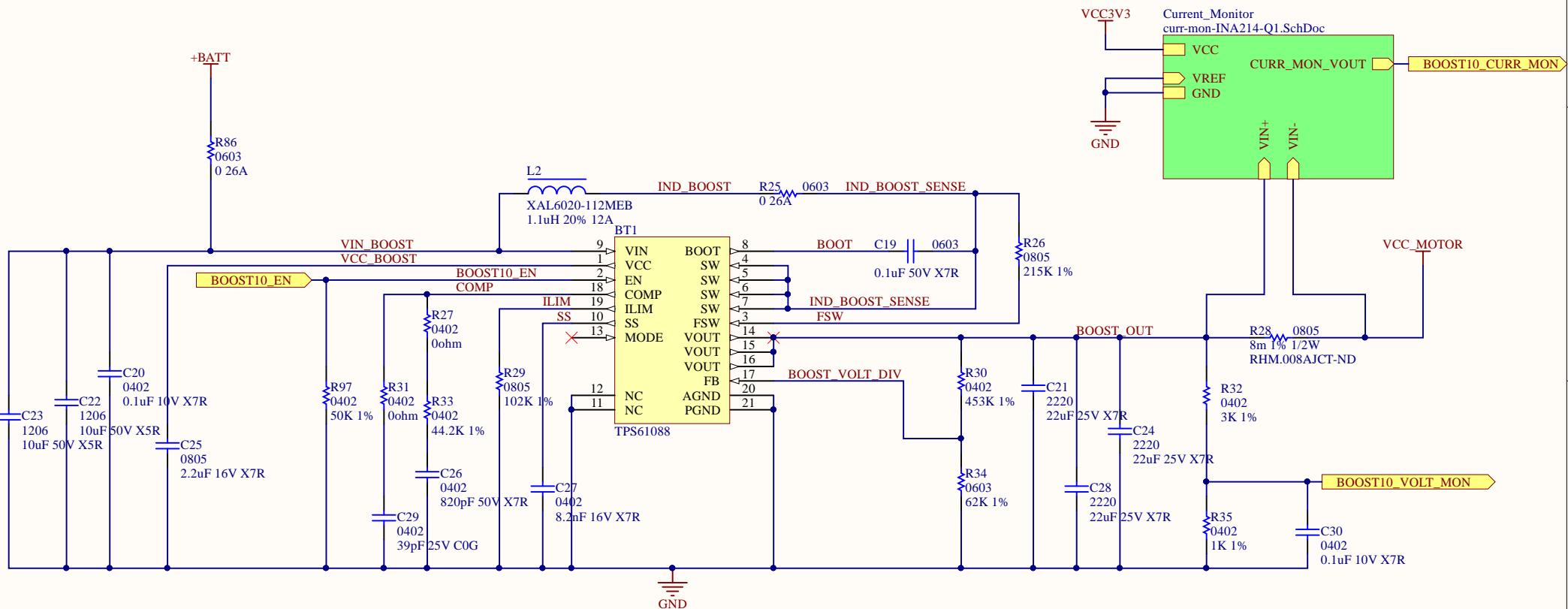
D

D

Title		UTAT SS
ADC Breakout.SchDoc		
Size	Number	Revision
A4	2.2	v4.2
Date:	2019-09-10	Sheet 2.2 of 47
File:	C:\Users\.\ADC Breakout.SchDoc	Drawn By: Lorna Lan, Dylan Vogel

1 2 3 4

A



Title		UTAT SS
Size	Number	Revision
A4	3	v4.3
Date:	2019-09-10	Sheet 3 of 47
File:	C:\Users\.\boost-converter.SchDoc	Drawn By: Lorna Lan, Jaden Reimer

WEBENCH simulation link:

Parameters:
TPS61088RHLR 3.6V-4.2V to 10.00V @ 2.8A<https://webench.ti.com/appinfo/webench/scripts/SDP.cgi?ID=CCD7917E>
D8455F42

1 2 3 4

A

A

B

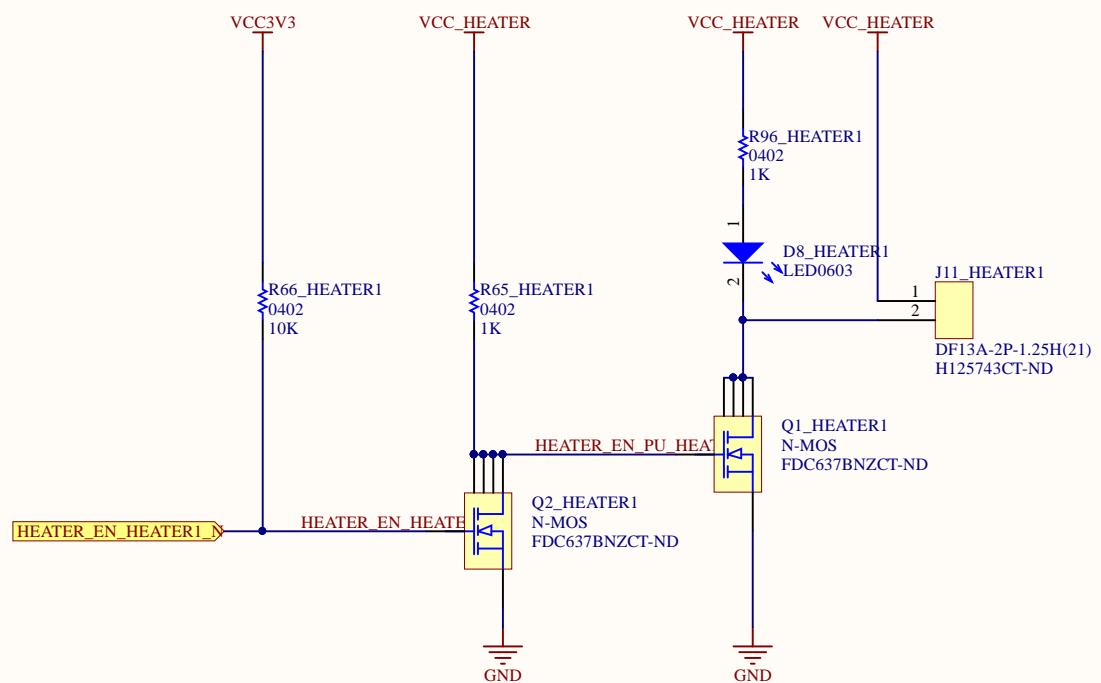
B

C

C

D

D



Title		
Heater Control.SchDoc		UTAT SS
Size	Number	Revision
A4	4.1	v4.2
Date:	2019-09-10	Sheet 4.1 of 47
File:	C:\Users\.\Heater Control.SchDoc	Drawn By: Lorna Lan

A

A

B

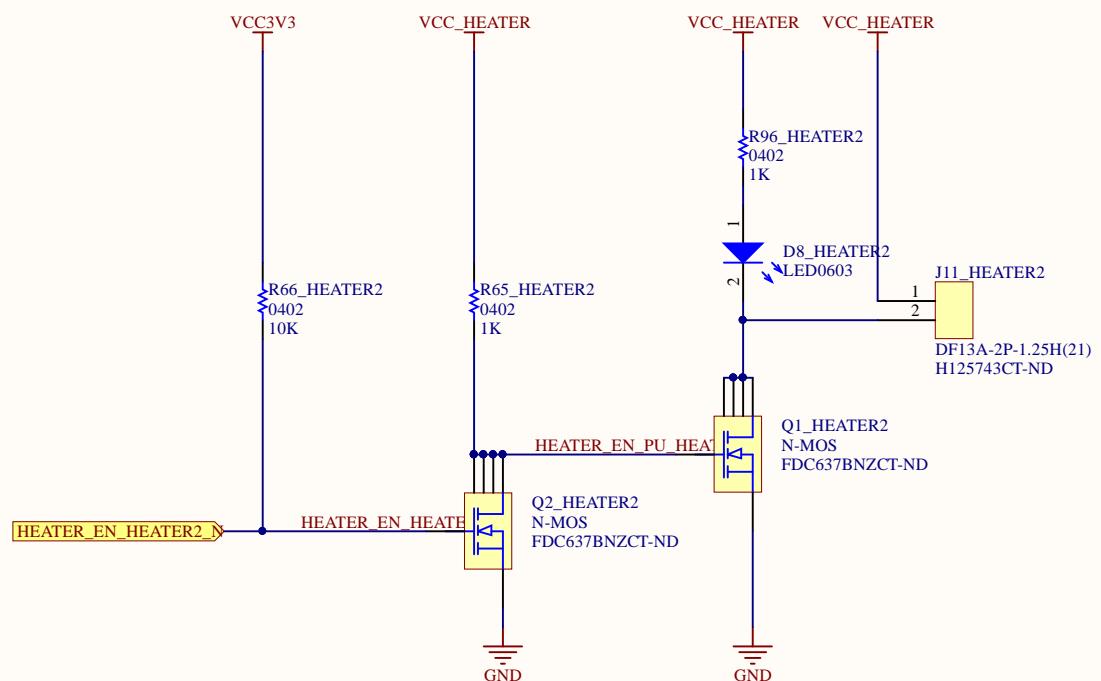
B

C

C

D

D



Title		
Heater Control.SchDoc		UTAT SS
Size	Number	Revision
A4	4.2	v4.2
Date:	2019-09-10	Sheet 4.2 of 47
File:	C:\Users\.\Heater Control.SchDoc	Drawn By: Lorna Lan

A

A

B

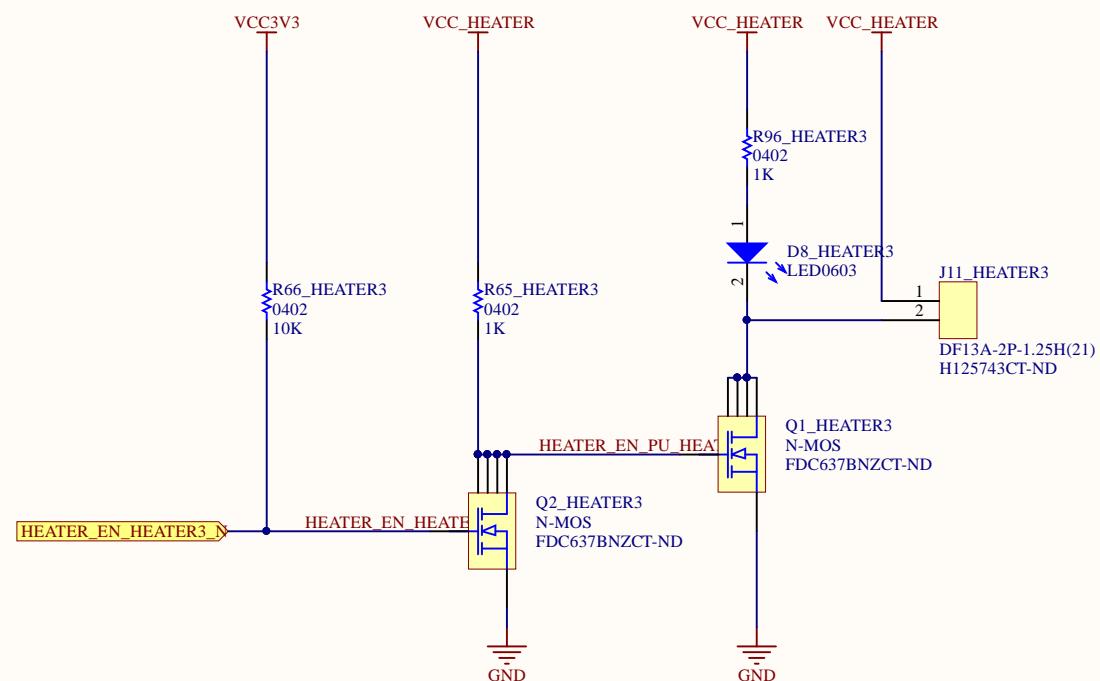
B

C

C

D

D



Title		
Heater Control.SchDoc		UTAT SS
Size	Number	Revision
A4	4.3	v4.2
Date:	2019-09-10	Sheet 4.3 of 47
File:	C:\Users\.\Heater Control.SchDoc	Drawn By: Lorna Lan

A

A

B

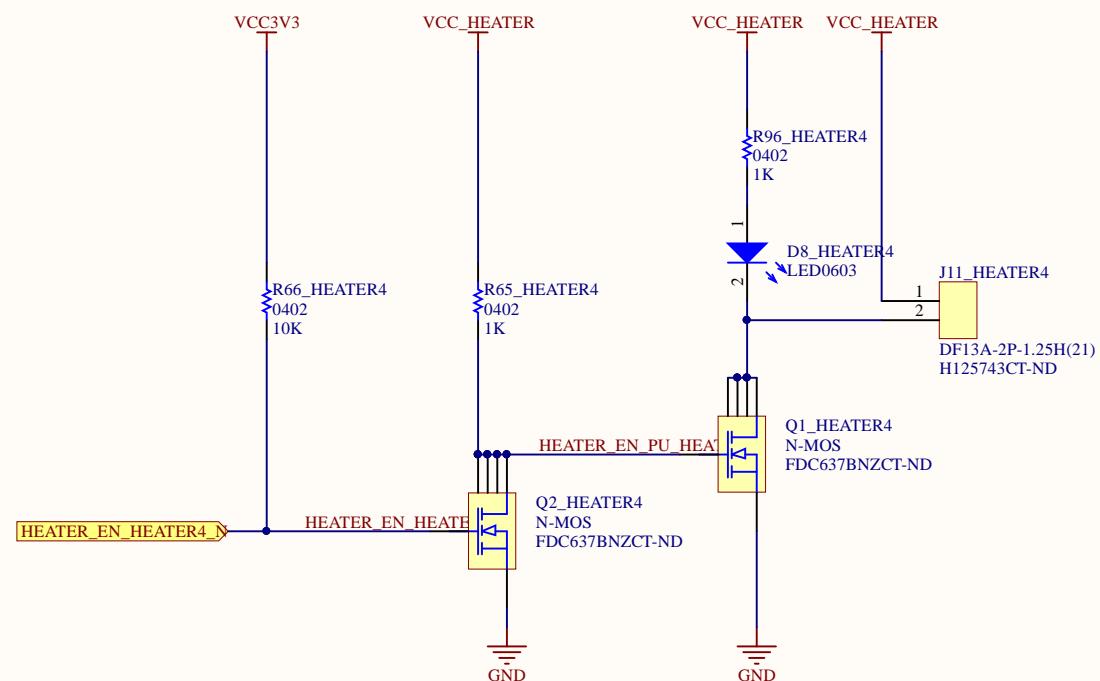
B

C

C

D

D



Title		
Heater Control.SchDoc		UTAT SS
Size	Number	Revision
A4	4.4	v4.2
Date:	2019-09-10	Sheet 4.4 of 47
File:	C:\Users\.\Heater Control.SchDoc	Drawn By: Lorna Lan

A

A

B

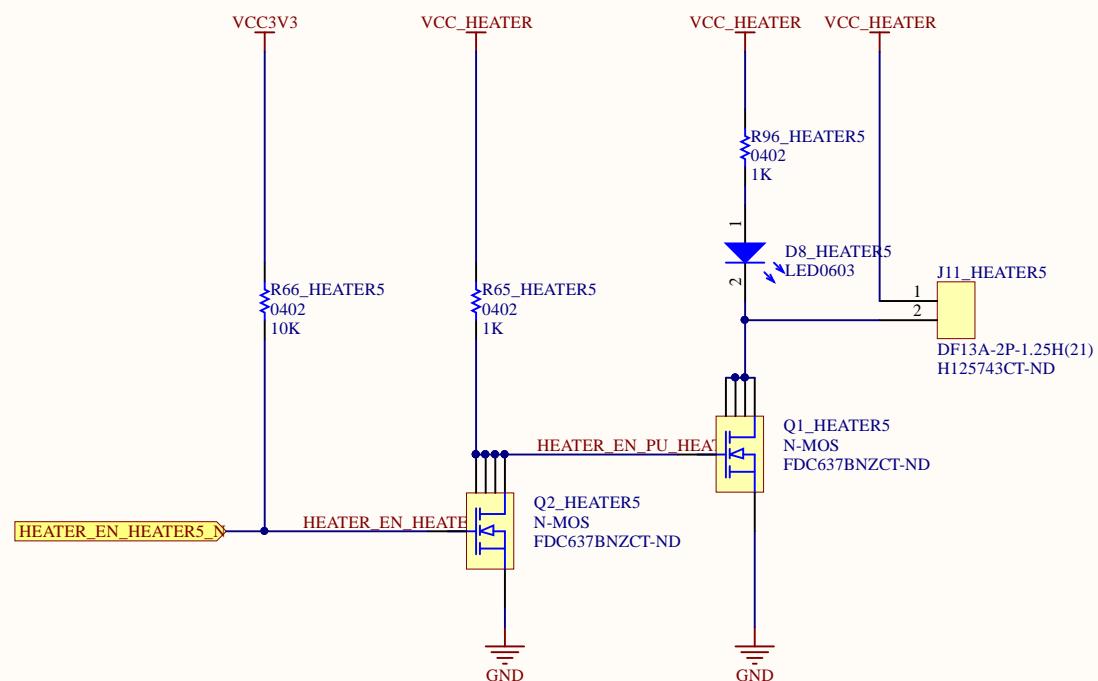
B

C

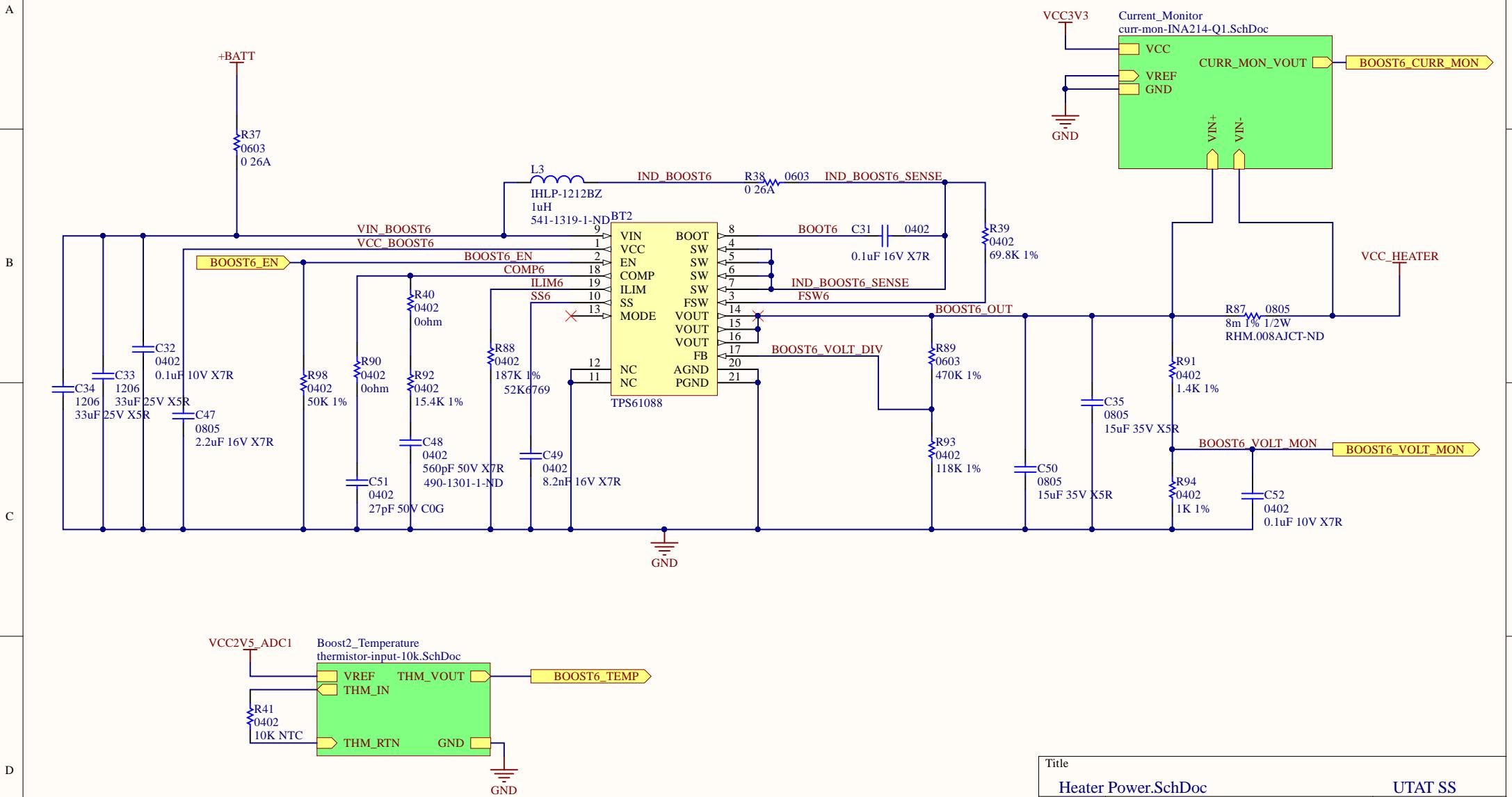
C

D

D

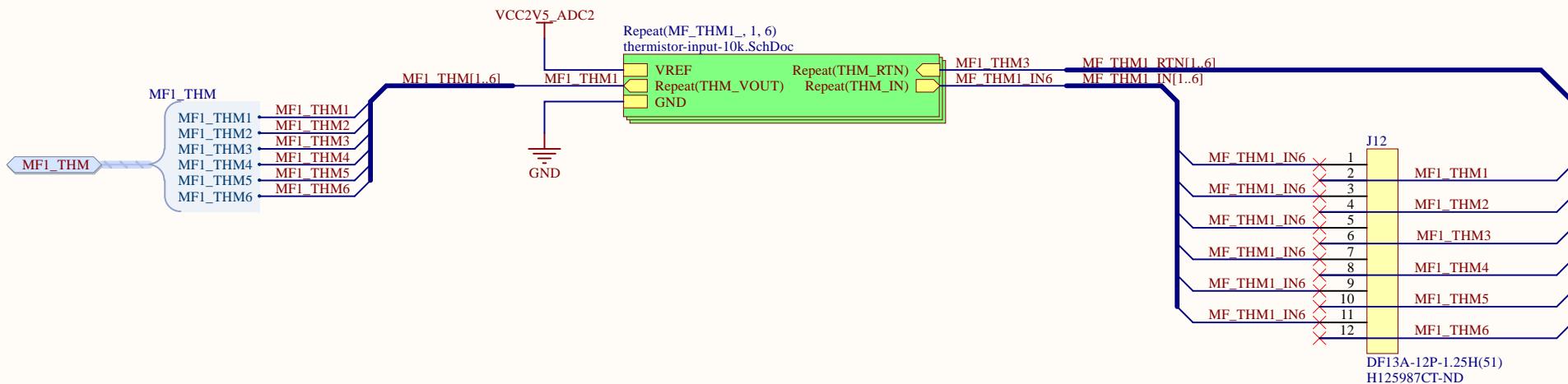


Title		
Heater Control.SchDoc		UTAT SS
Size	Number	Revision
A4	4.5	v4.2
Date:	2019-09-10	Sheet 4.5 of 47
File:	C:\Users\.\Heater Control.SchDoc	Drawn By: Lorna Lan

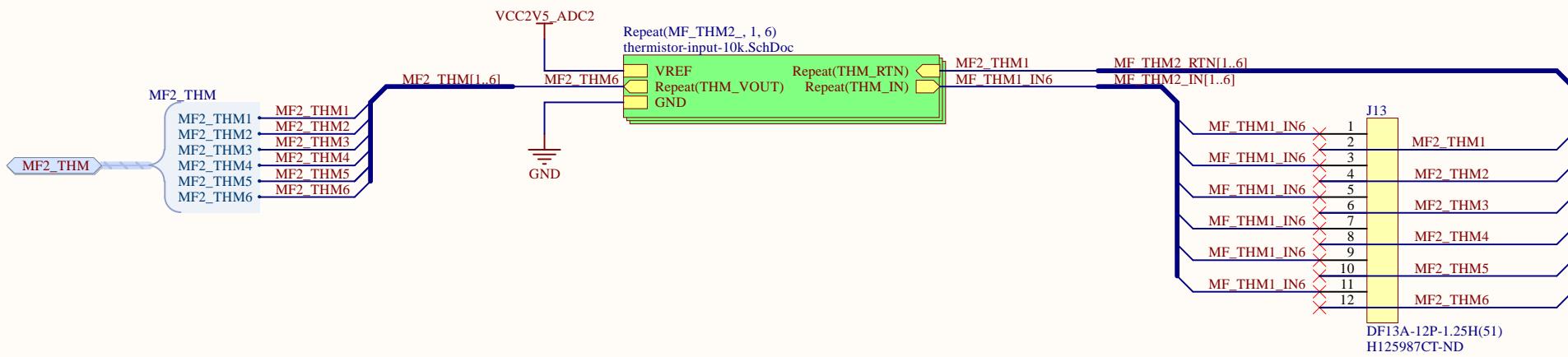


Title		
Heater Power.SchDoc		UTAT SS
Size	Number	Revision
A4	5	v4.1
Date:	2019-09-10	Sheet 5 of 47
File:	C:\Users\.\Heater Power.SchDoc	Drawn By: Lorna Lan

A



B



C

Title		
MF Thermistors.SchDoc		UTAT SS
Size	Number	Revision
A4	6	v4.1
Date:	2019-09-10	Sheet 6 of 47
File:	C:\Users\.\MF Thermistors.SchDoc	Drawn By: Lorna Lan, Dylan Vogel

A

B

C

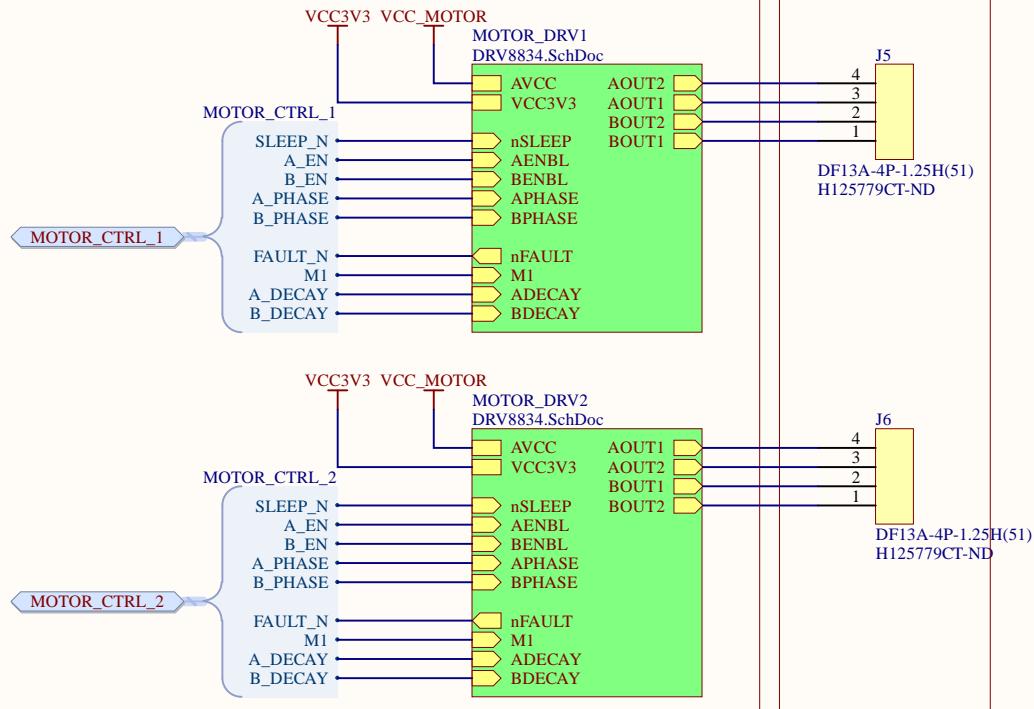
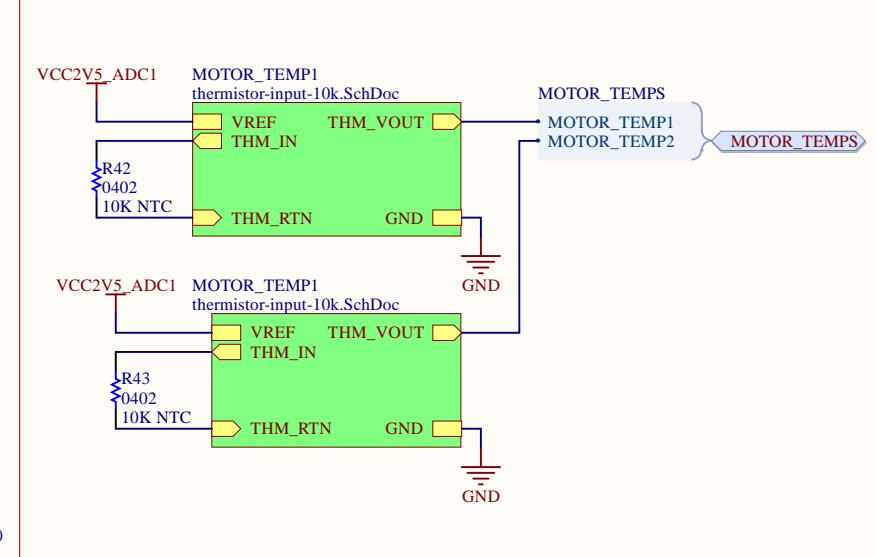
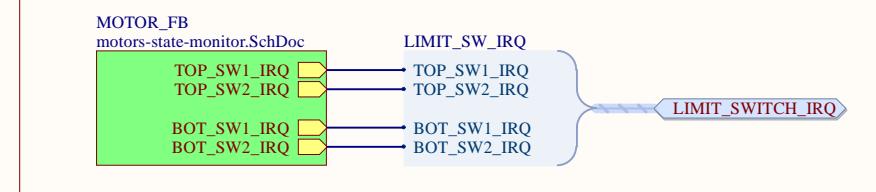
D

A

B

C

D

MOTOR DRIVERS**MOTOR CONNECTORS****MOTOR LIMIT SWITCHES**

Title

Motors.SchDoc**UTAT SS**

Size	Number	Revision
A4	7	v4.2
Date:	2019-09-10	Sheet 7 of 47
File:	C:\Users\.\Motors.SchDoc	Drawn By: Lorna Lan, Dylan Vogel

A

A

B

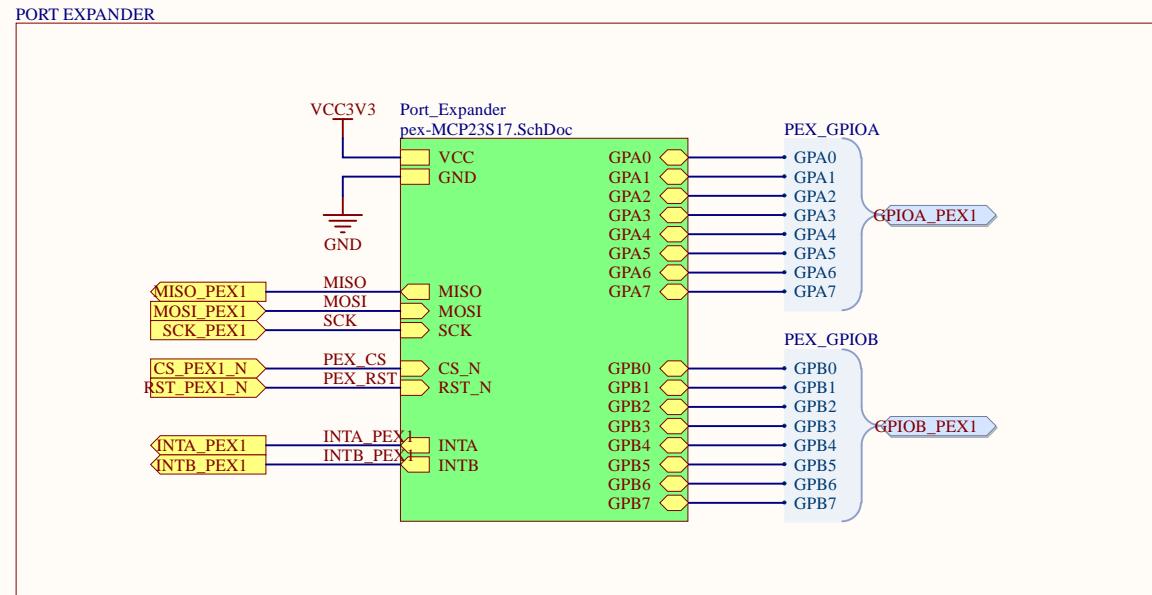
B

C

C

D

D



Breaks out the Port Expander GPIOs into harnesses

ADDRESS: 0b001

Title		UTAT SS
Port Expander Breakout.SchDoc		
Size	Number	Revision
A4	8.1	v4.2
Date:	2019-09-10	Sheet 8.1 of 47
File:	C:\Users\.\Port Expander Breakout.SchDoc	Drawn By: Dylan Vogel

A

A

B

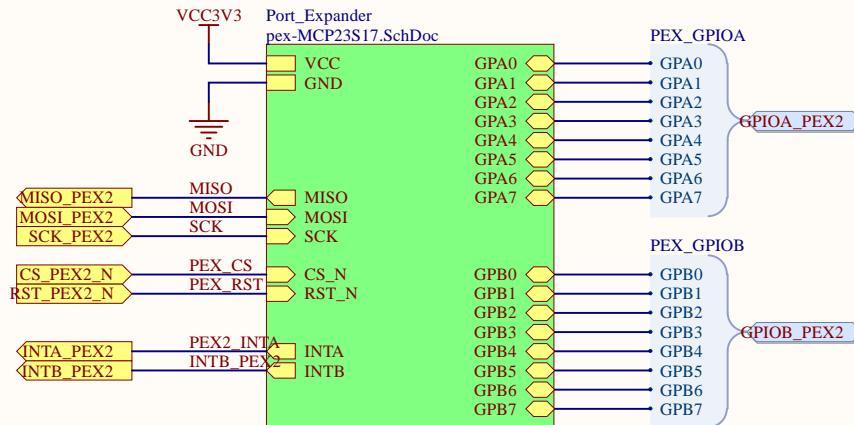
B

C

C

D

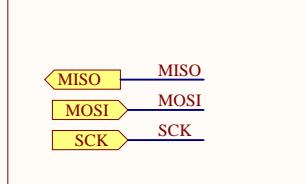
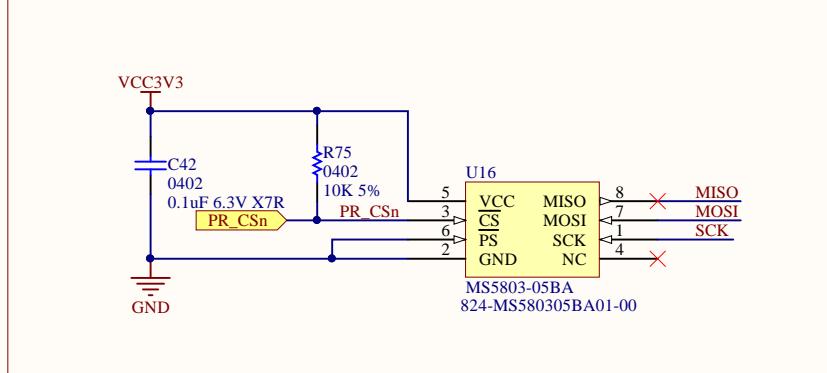
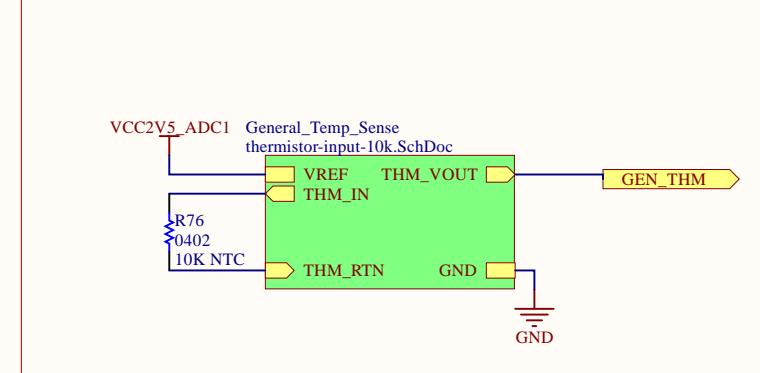
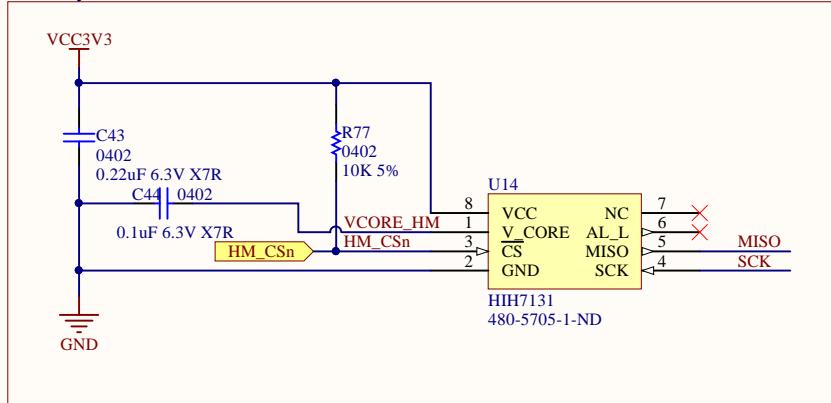
D

PORT EXPANDER

Breaks out the Port Expander GPIOs into harnesses

ADDRESS: 0b010

Title		UTAT SS
Size	Number	Revision
A4	8.2	v4.2
Date:	2019-09-10	Sheet 8.2 of 47
File:	C:\Users\.\Port Expander Breakout.SchDoc	Drawn By: Dylan Vogel

Sensor SPI Line**Pressure Sensor****General/Ambient Temperature Thermistor****Humidity sensor**

Title		UTAT SS
Size	Number	Revision
A4	9	v4.2
Date:	2019-09-10	Sheet 9 of 47
File:	C:\Users\.\sensors.SchDoc	Drawn By: Dylan Vogel, Lorna Lan

A

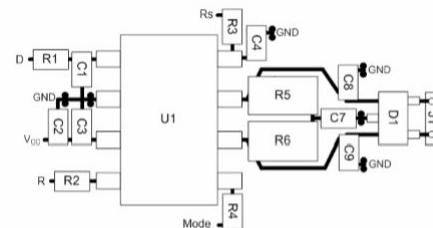
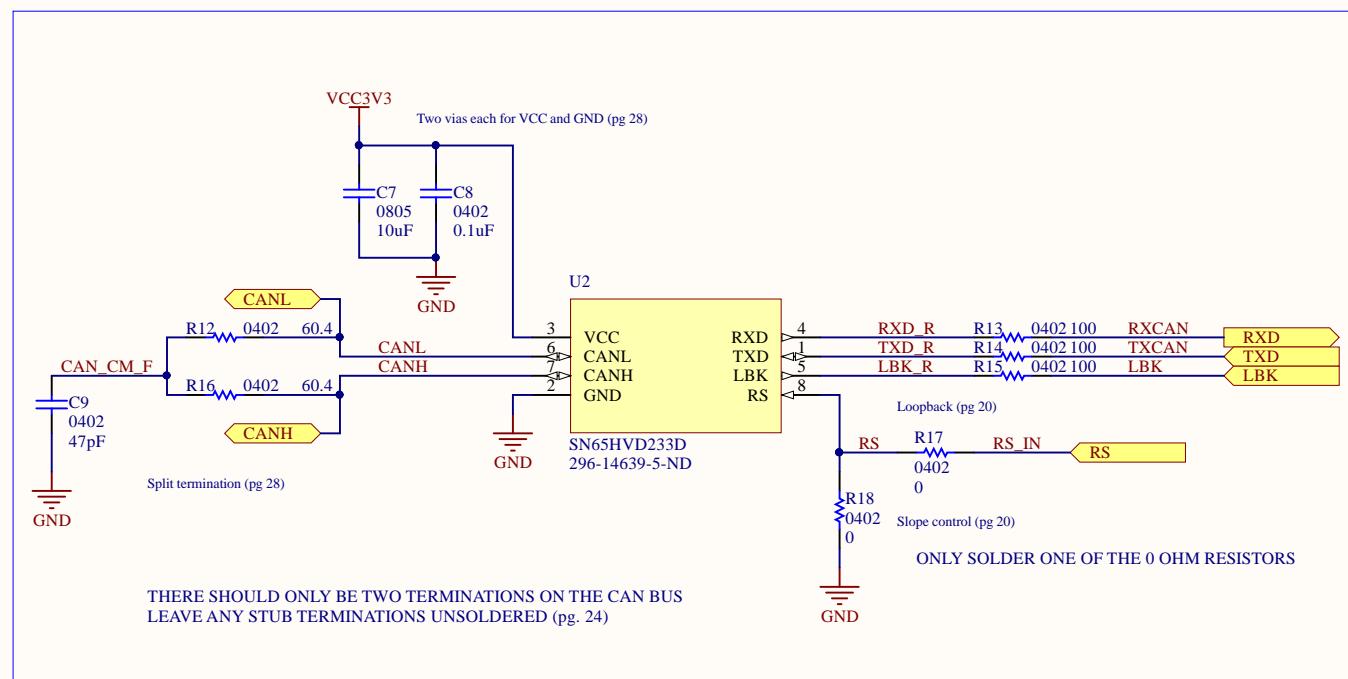
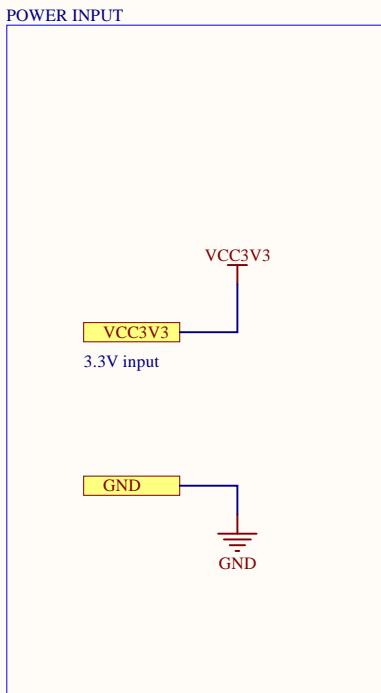


Figure 41. Layout Example Schematic

See pg. 28 of the datasheet for layout guidelines

This schematic implements the SN65HVD233 CAN transceiver with loopback control and two options for slope control.

A 0 Ohm resistor can be soldered to GND to permanently put the device in high speed mode (20 V / us slew), or a 0 Ohm resistor can be soldered to the RS port to control the device via an external microcontroller. Connecting the RS pin to a microcontroller allows the device to be put into low-power mode by setting the RS pin high.

- Device is meant to be used in a 3.3 V system
- 100 Ohm current limiting resistors placed on the digital lines to minimize digital noise to the device
- Only two CAN transceivers on the bus should have 120 ohm terminations. Other devices should be placed on 'stub' networks where the terminations are left unsoldered

Title		UTAT SS
can-SN65HVD233.SchDoc		Revision
Size	Number	
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 10 of 47
File:	C:\Users\.\can-SN65HVD233.SchDoc	Drawn By: Dylan Vogel

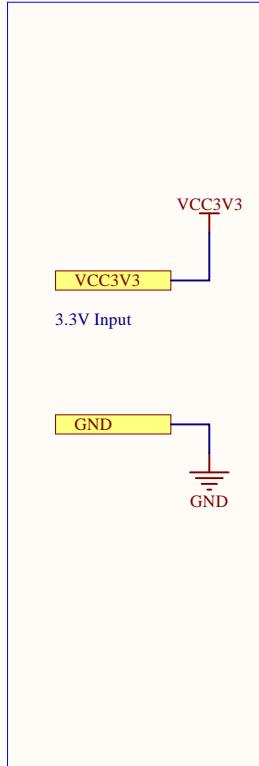
A

B

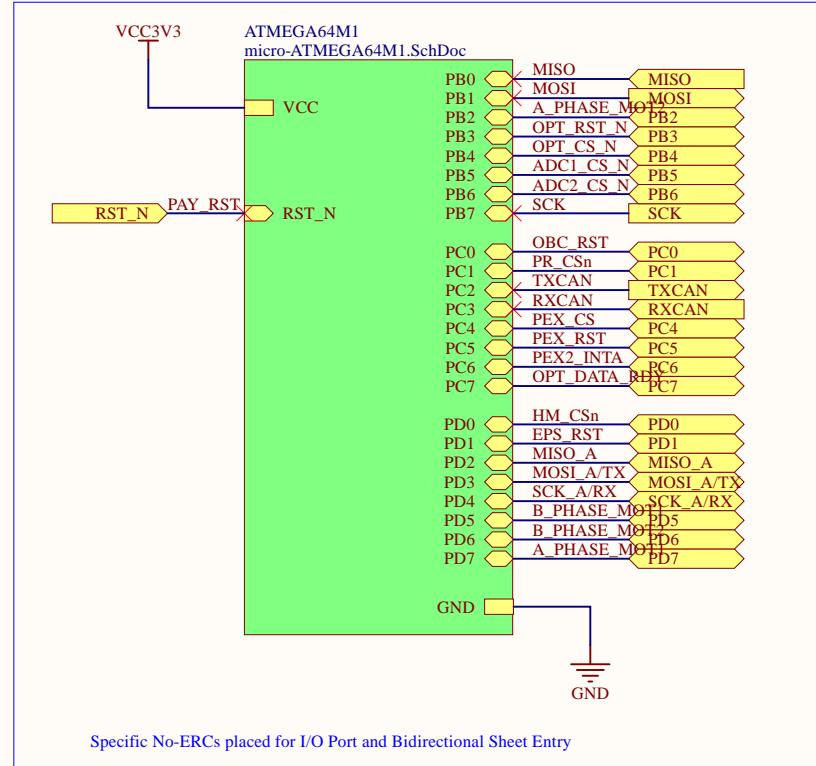
C

D

POWER INPUTS

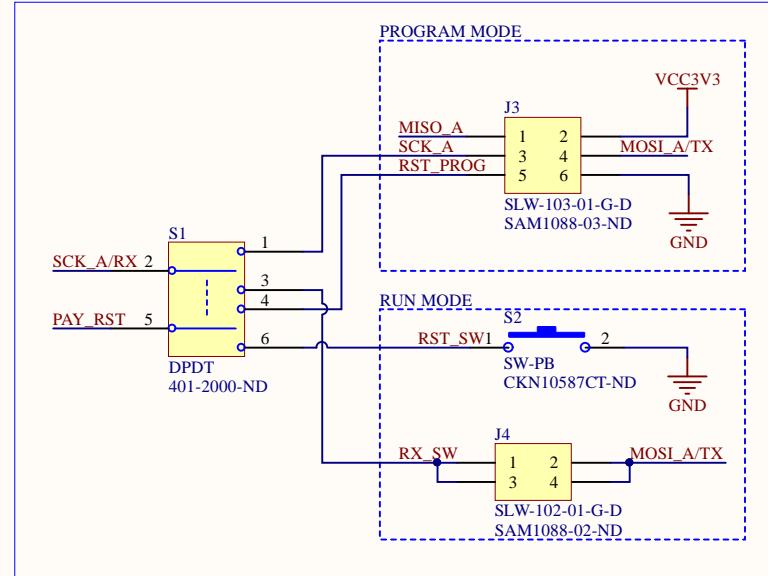


ATMEGA32M1

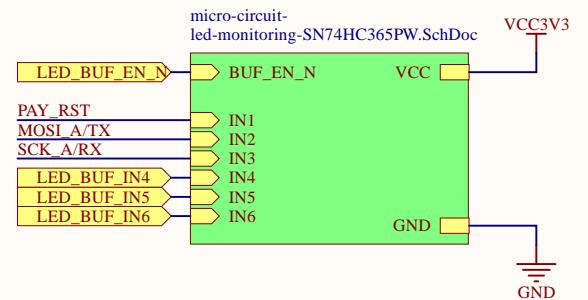


Specific No-ERCs placed for I/O Port and Bidirectional Sheet Entry

MODE SELECT CIRCUITRY



LED MONITORING



This schematic extends the functionality already included in the micro-ATMEGA32M1 schematic, adding a mode select switch, programming header, reset button and LED indication for TX, RX and RSTn.

- IN[4:6] of the LED buffer have been left unconnected, but are broken out on ports LED_BUF_IN[4:6]. They can be connected in the schematic which includes this sheet to monitor up to an additional 3 lines. Highly recommend more blinking lights.

Title		
micro-circuit-ATMEGA64M1.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-09-10	Sheet 11 of 47
File:	C:\Users\.\micro-circuit-ATMEGA64M1.SchDoc	Created By: Dylan Vogel

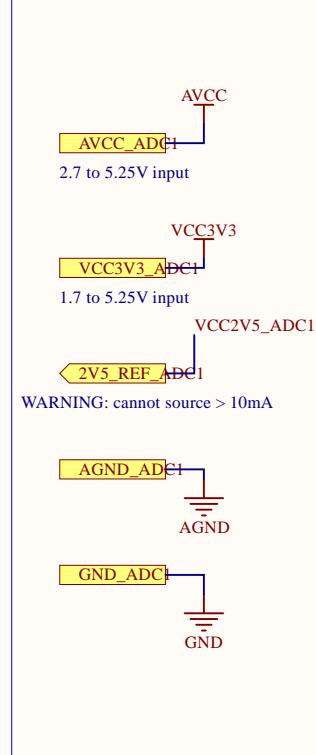
1

2

3

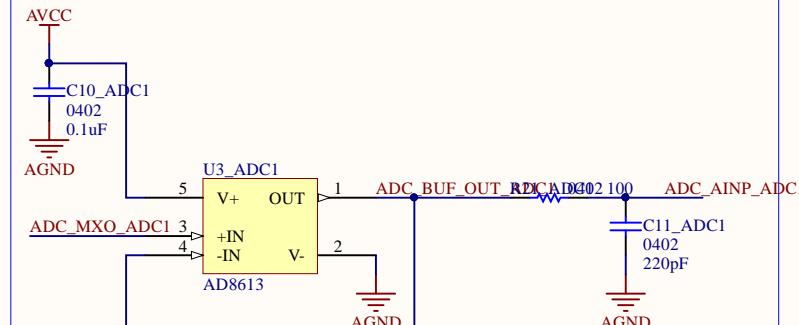
4

POWER PORTS
AVCC >= VCC (pg 51)



ADC INPUT BUFFER

See pg. 50 for discussion of unity buffer design procedure



ADC

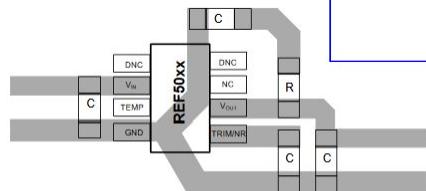
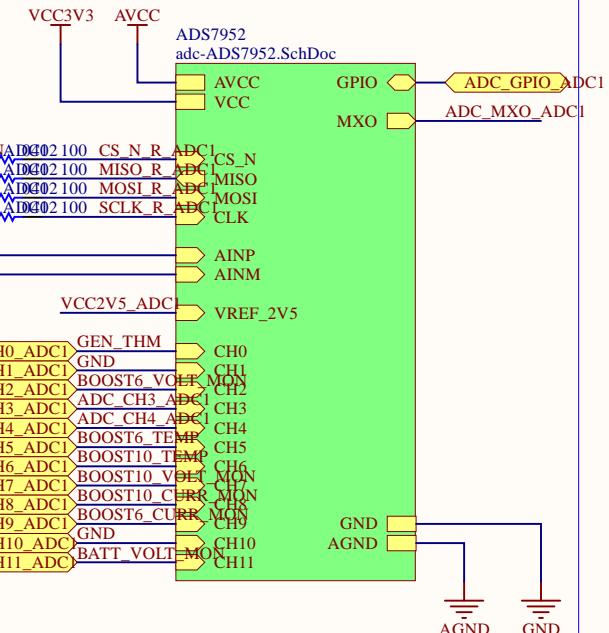


Figure 44. Layout Example

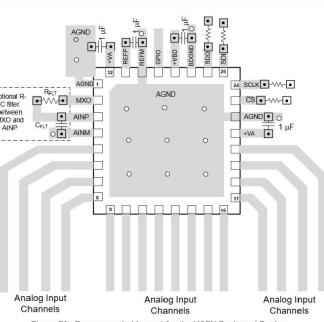


Figure 70. Recommended Layout for the VQFN Packaged Device

This schematic implements the ADS7952 analog-to-digital converter with a 2.5V reference and a unity-gain buffer on the output of the internal multiplexer.

- Recommended input impedance should be < 1K. Higher source impedances possible with slower sampling.
- Breaks out 2V5 for use as reference outside the circuit
- All necessary bypassing and pull-ups implemented in the ADS7952 schematic
- In most low-performance applications, AVCC and VCC can be tied together
- In the layout, the pins tied to AGND should be put on a local GND pour and then tied to the global ground plane with low-impedance.
- 100 ohm resistors on the SPI input help to isolate the ADC from digital noise

Title

adc-circuit-ADS7952.SchDoc

UTAT SS

Size

A4

Number

PCBS-COMMON

Revision
1.1

Date: 2019-09-10

Sheet 12.1.bf 47

File: C:\Users\.\adc-circuit-ADS7952.SchDoc Drawn By: Dylan Vogel

1

2

3

4

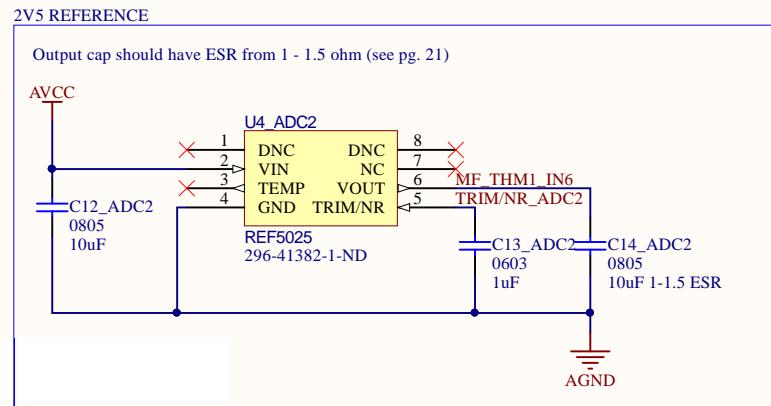
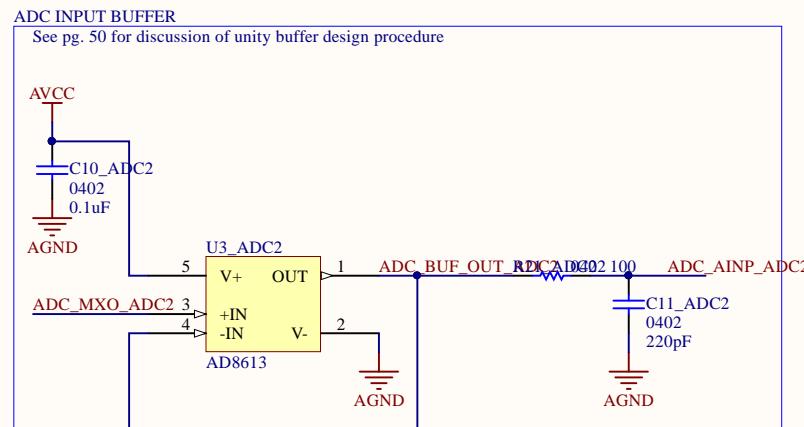
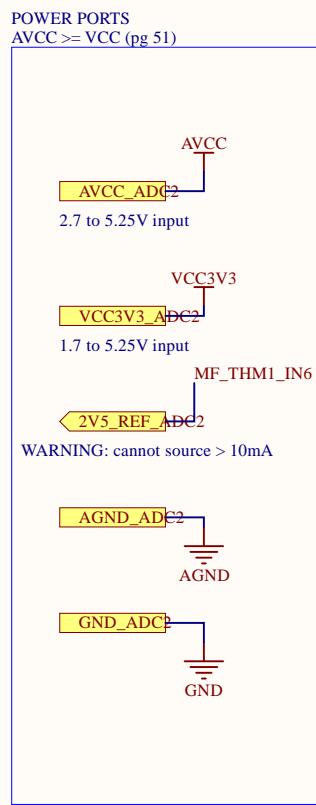
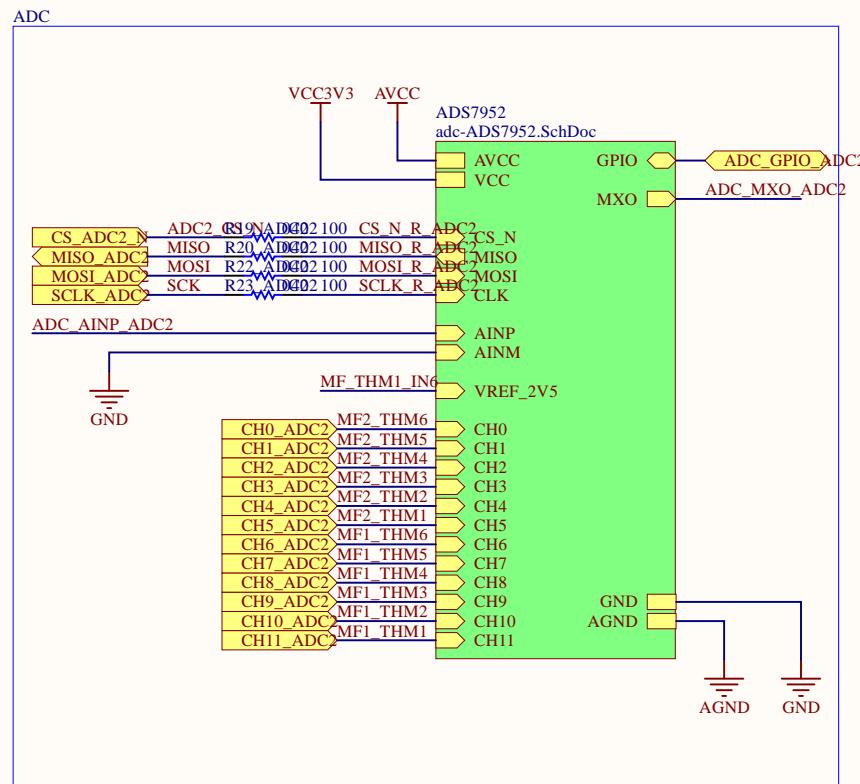
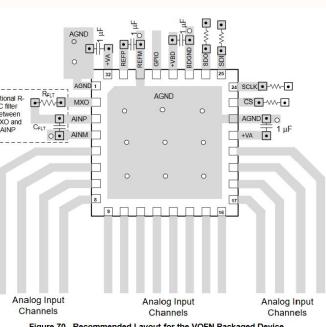


Figure 44. Layout Example



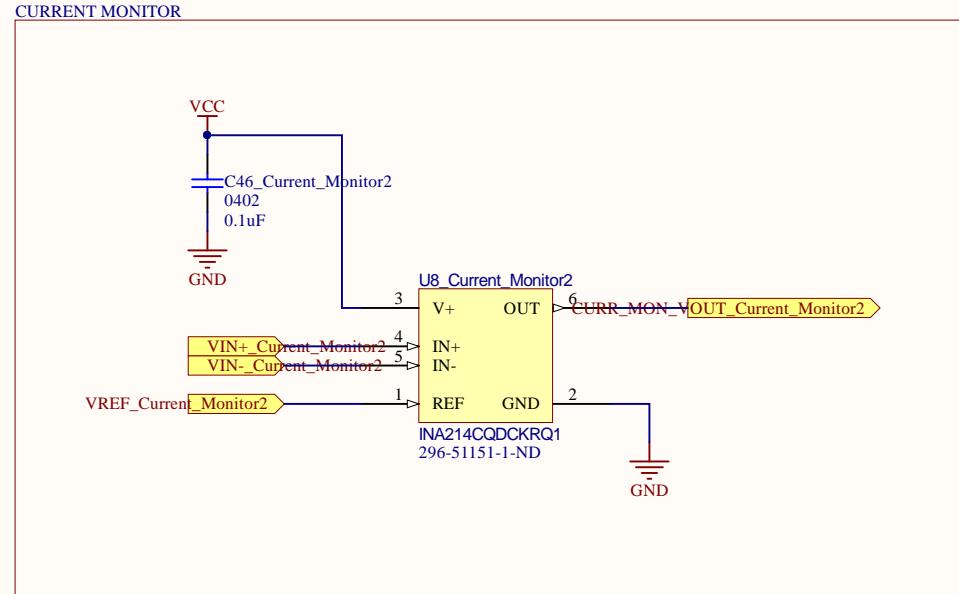
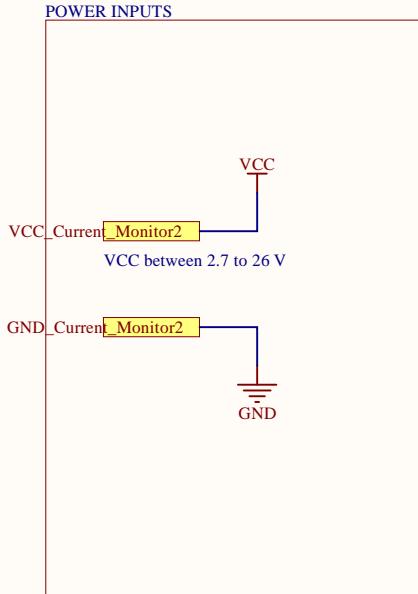
This schematic implements the ADS7952 analog-to-digital converter with a 2.5V reference and a unity-gain buffer on the output of the internal multiplexer.

- Recommended input impedance should be $< 1\text{K}$. Higher source impedances possible with slower sampling.
 - Breaks out 2V5 for use as reference outside the circuit
 - All necessary bypassing and pull-ups implemented in the ADS7952 schematic
 - In most low-performance applications, AVCC and VCC can be tied together
 - In the layout, the pins tied to AGND should be put on a local GND pour and then tied to the global ground plane with low-impedance.
 - 100 ohm resistors on the SPI input help to isolate the ADC from digital noise

Title		UTAT SS	
Size	Number	Revision	
A4	PCBS-COMMON	1.1	
Date:	2019-09-10	Sheet	12.2.bf 47
File:	C:\Users\.\adc-circuit-ADS7952.SchDoc	Drawn By:	Dylan Vogel

A

A



B

B

C

C

This schematic implements the INA214-Q1 automotive grade, voltage output, high- or low-side, bidirectional, zero-drift current shunt monitor

Application Information:

- This amplifier has an internal gain of 100x
- Place a small value current sense resistor ($1 \rightarrow 10 \text{ mOhm}$) in series with the current you're trying to monitor. Connect VIN+ of the current monitor to the positive terminal of the resistor, and VIN- to the negative terminal.
- Assume the worst-case input voltage offset is 100uV. This allows you to calculate your expected measurement error. No strict guideline on what this should be, but if your full-scale current generates a voltage of 10mV across your sense resistor, that's 1% error. Typical error will be lower than this.

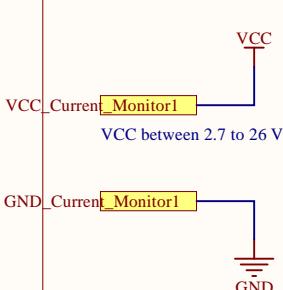
- For unidirectional operation (current in one direction) connect VREF to GND
- For bidirectional operation, UTAT recommends connecting VREF to the stable 2.5V reference you probably already use for your ADC. Pop a 0.1uF on your VREF connection in that case.
- To calculate your current range for bidirectional, understand that forward current will cause VOUT to rise from 2.5 V up to VCC - 0.2 V. Reverse current will cause VOUT to drop from 2.5V to GND. Divide this voltage swing in each direction by $(100 * R_{sense})$ to figure out your max current

Title		
curr-mon-INA214-Q1.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.0
Date:	2019-09-10	Sheet 13 of 47
File:	C:\Users\.\curr-mon-INA214-Q1.SchDoc	Drawn By: J. Reimer, D. Vogel

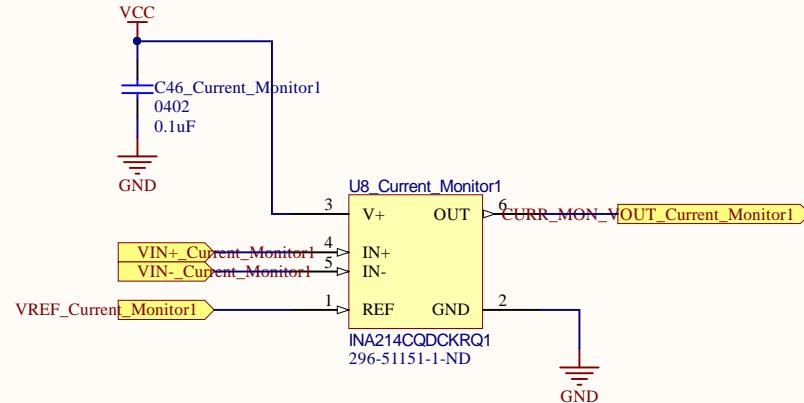
A

A

POWER INPUTS



CURRENT MONITOR



B

B

C

C

This schematic implements the INA214-Q1 automotive grade, voltage output, high- or low-side, bidirectional, zero-drift current shunt monitor

Application Information:

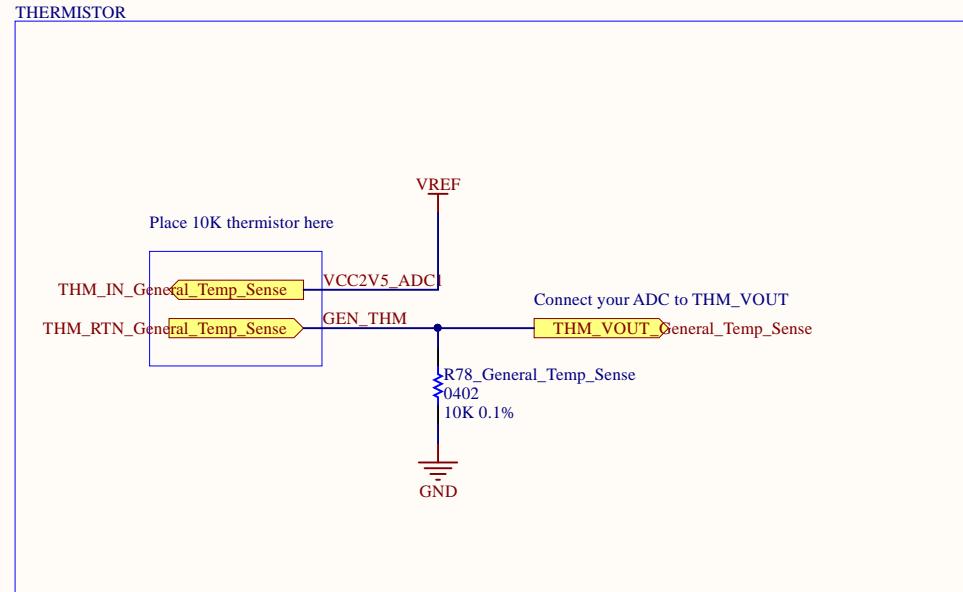
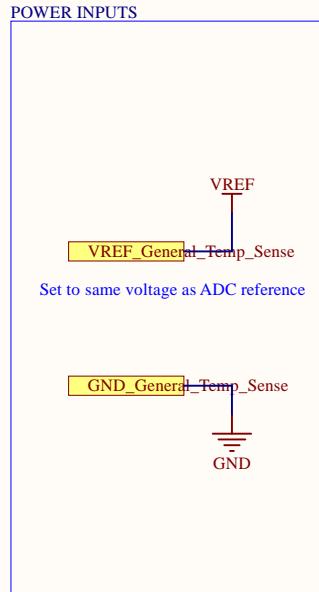
- This amplifier has an internal gain of 100x
- Place a small value current sense resistor ($1 \rightarrow 10 \text{ mOhm}$) in series with the current you're trying to monitor. Connect VIN+ of the current monitor to the positive terminal of the resistor, and VIN- to the negative terminal.
- Assume the worst-case input voltage offset is 100uV. This allows you to calculate your expected measurement error. No strict guideline on what this should be, but if your full-scale current generates a voltage of 10mV across your sense resistor, that's 1% error. Typical error will be lower than this.

- For unidirectional operation (current in one direction) connect VREF to GND
- For bidirectional operation, UTAT recommends connecting VREF to the stable 2.5V reference you probably already use for your ADC. Pop a 0.1uF on your VREF connection in that case.
- To calculate your current range for bidirectional, understand that forward current will cause VOUT to rise from 2.5 V up to VCC - 0.2 V. Reverse current will cause VOUT to drop from 2.5V to GND. Divide this voltage swing in each direction by $(100 * R_{sense})$ to figure out your max current

Title		
curr-mon-INA214-Q1.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.0
Date:	2019-09-10	Sheet 13 of 47
File:	C:\Users\.\curr-mon-INA214-Q1.SchDoc	Drawn By: J. Reimer, D. Vogel

A

A



B

B

C

C

D

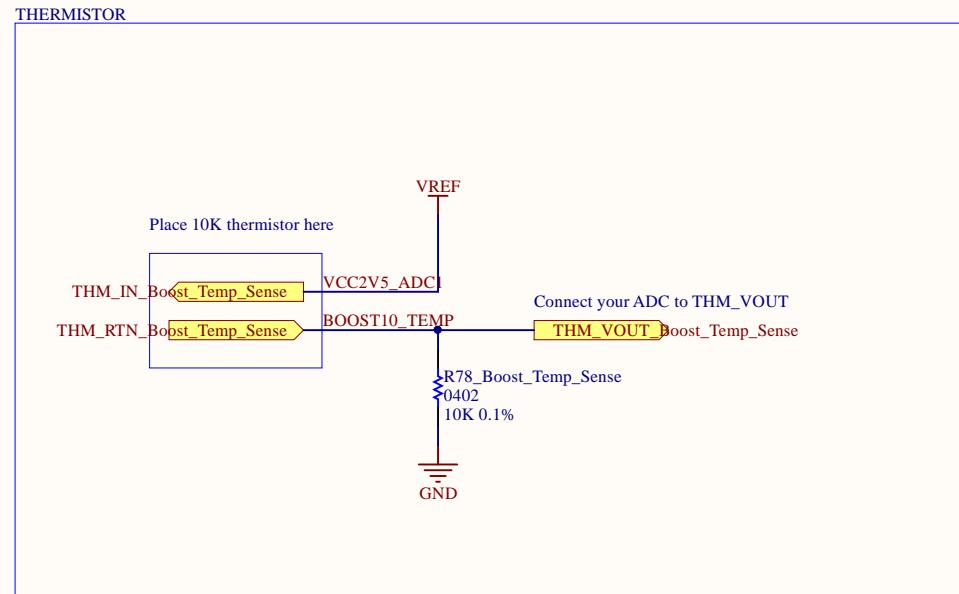
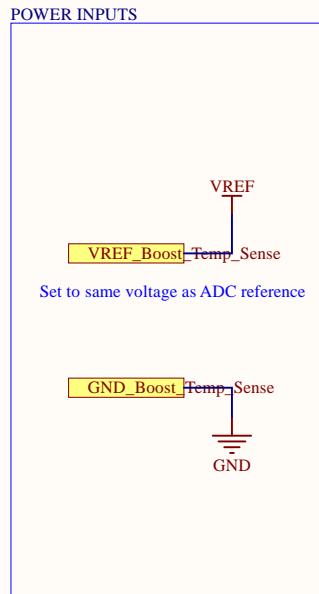
D

Title
thermistor-input-10k.SchDoc UTAT SS

Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14 of 47
File:	C:\Users\.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

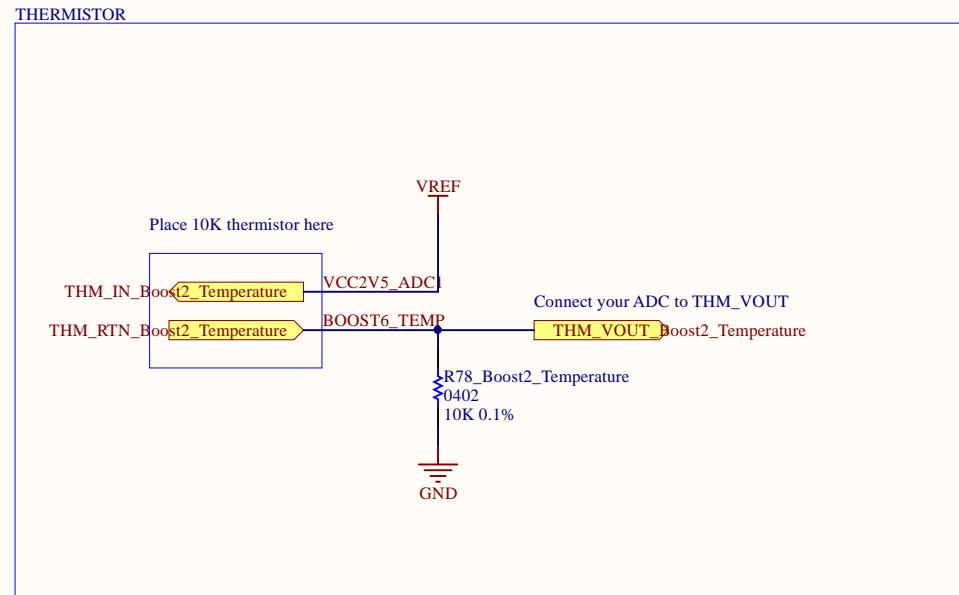
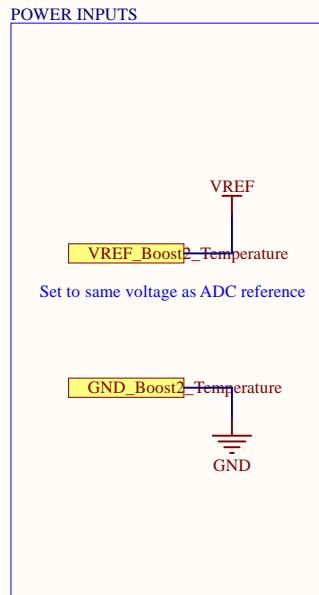
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D

Title		
thermistor-input-10k.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14 of 47
File:	C:\Users\.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

D

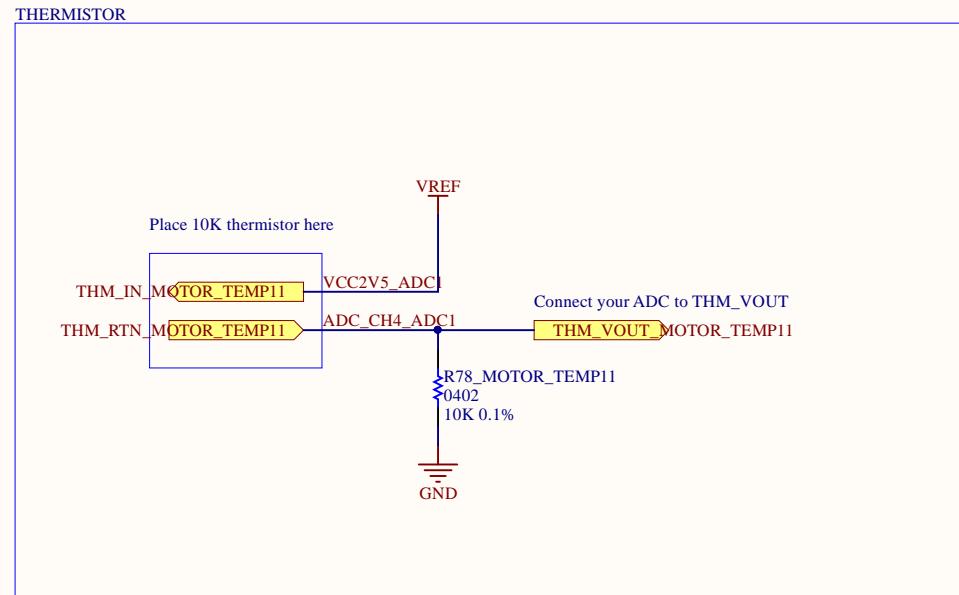
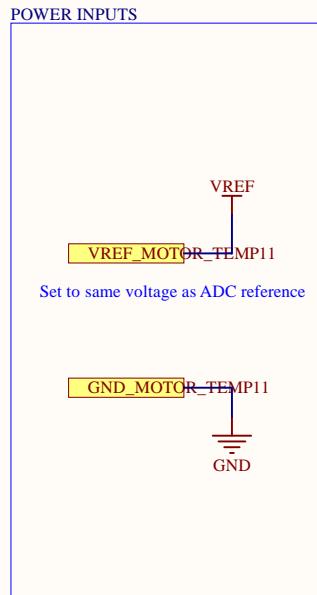
D

Title
thermistor-input-10k.SchDoc UTAT SS

Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14 of 47
File:	C:\Users\.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

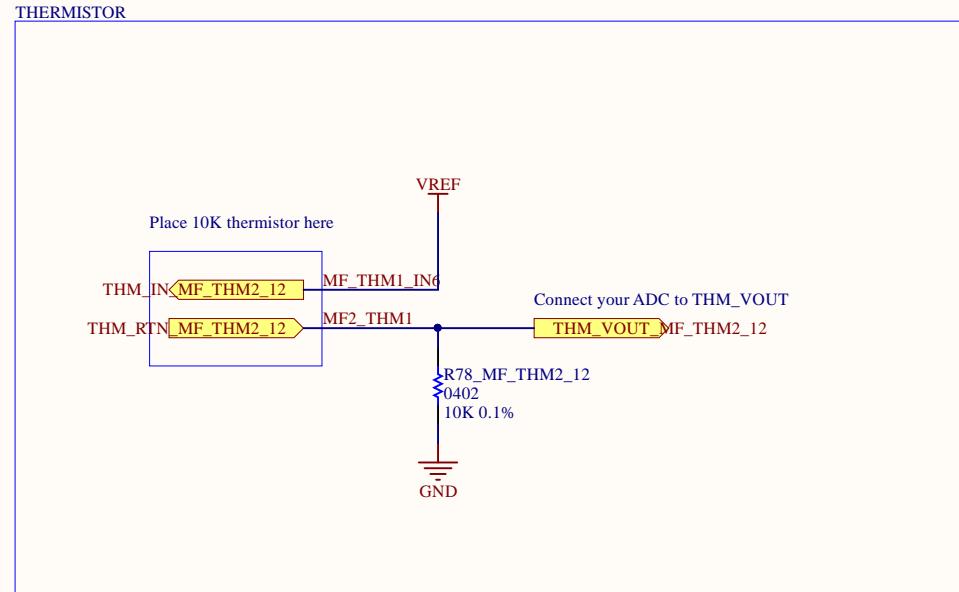
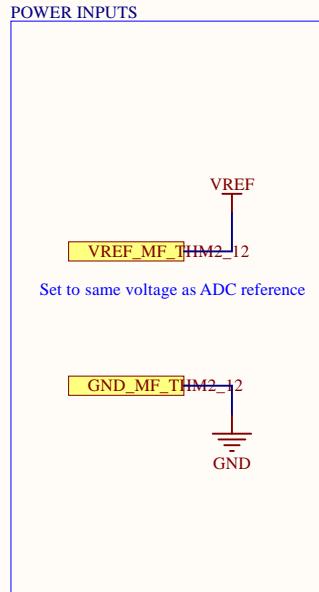
D

D

Title		
thermistor-input-10k.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.1 of 47
File:	C:\Users\.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

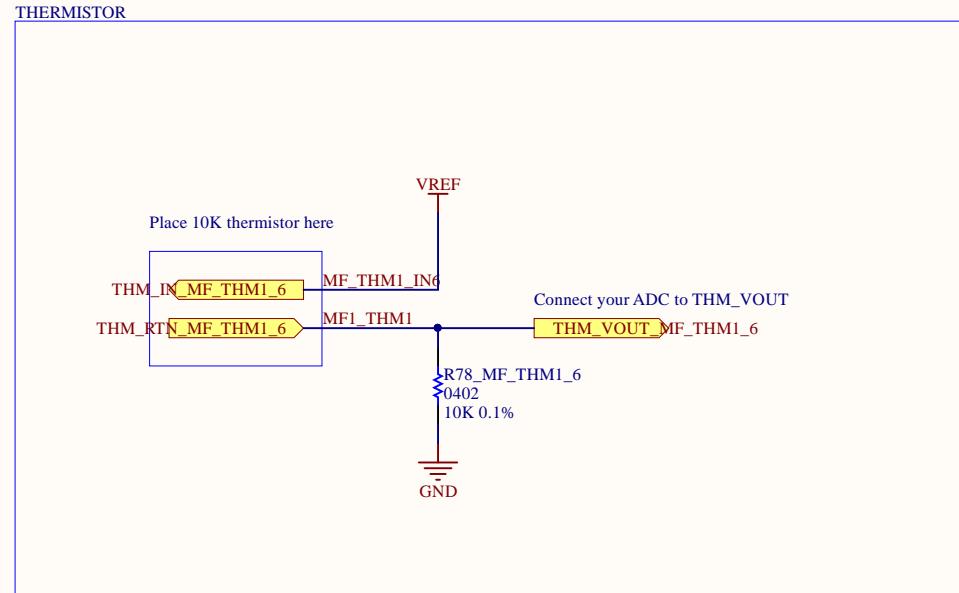
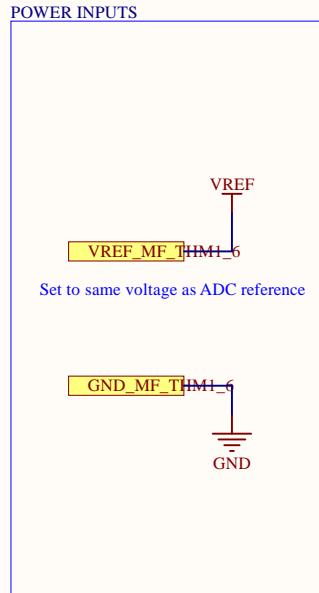
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D

Title		
thermistor-input-10k.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.1 of 47
File:	C:\Users\.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

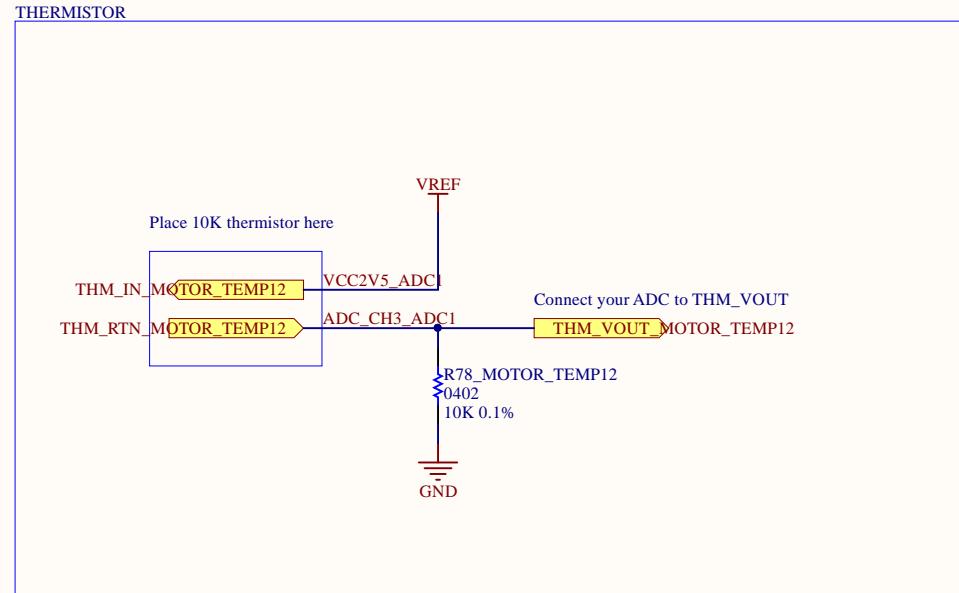
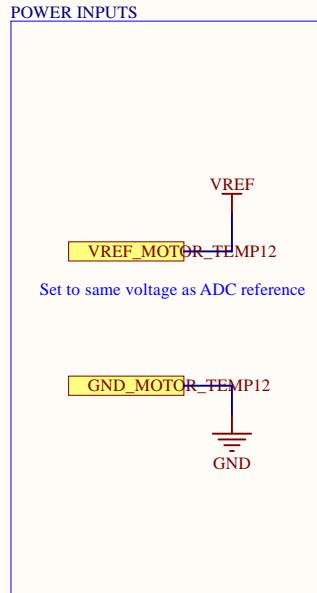
D

D

Title		
thermistor-input-10k.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.1 of 47
File:	C:\Users\.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

D

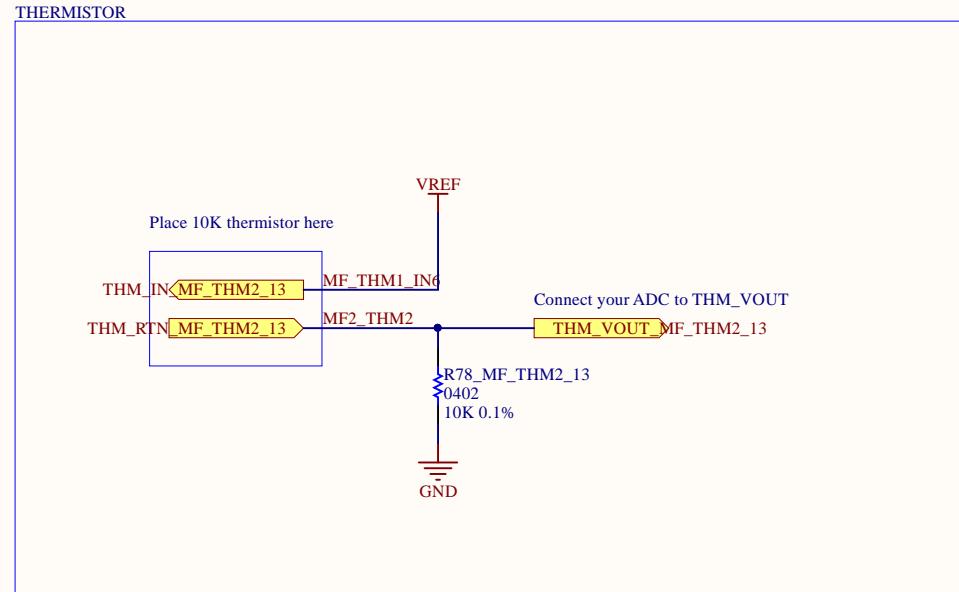
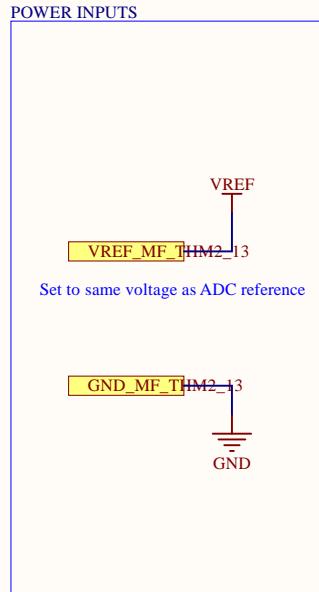
D

Title
thermistor-input-10k.SchDoc UTAT SS

Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.2 of 47
File:	C:\Users\.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

D

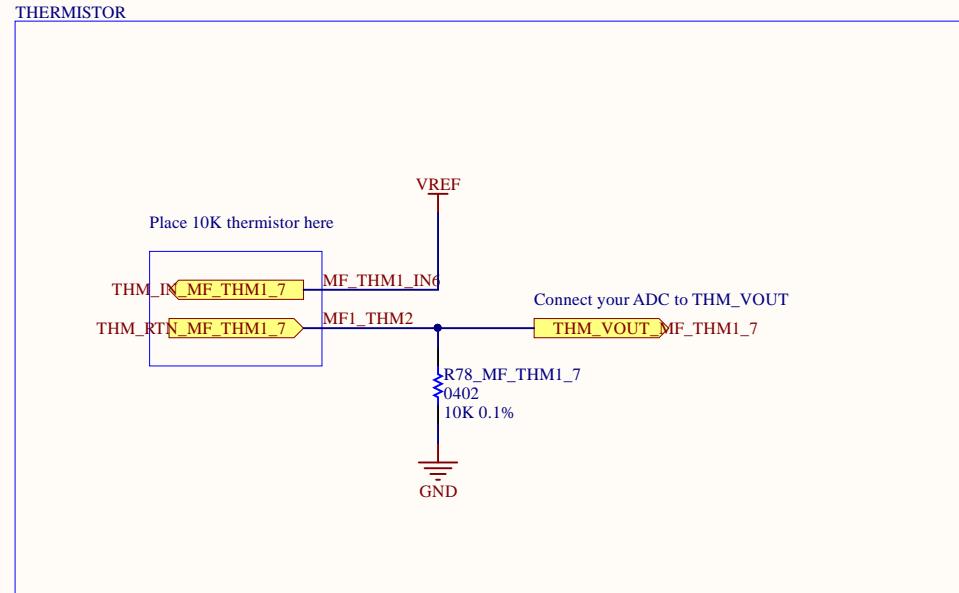
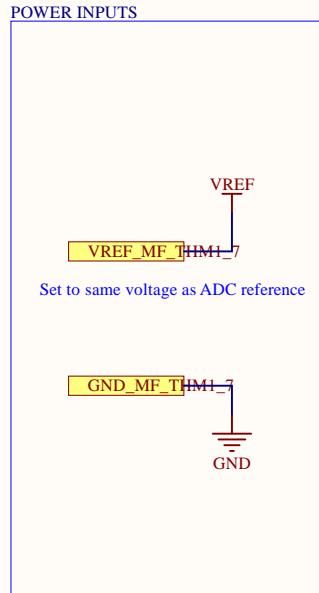
D

Title: thermistor-input-10k.SchDoc UTAT SS

Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.2 of 47
File:	C:\Users.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

D

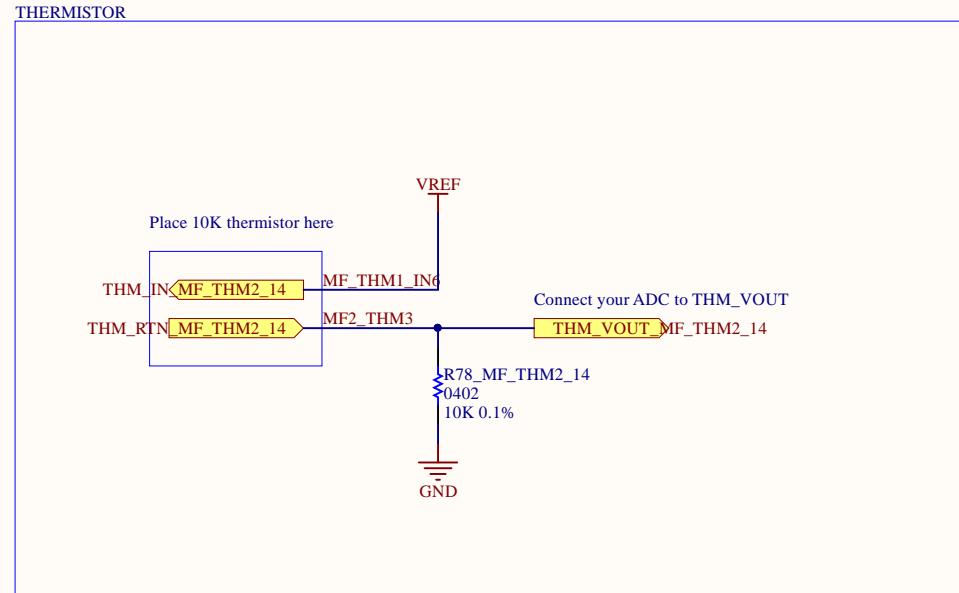
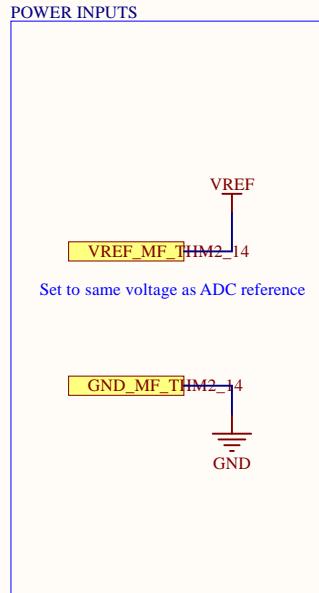
D

Title
thermistor-input-10k.SchDoc UTAT SS

Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.2 of 47
File:	C:\Users\.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

D

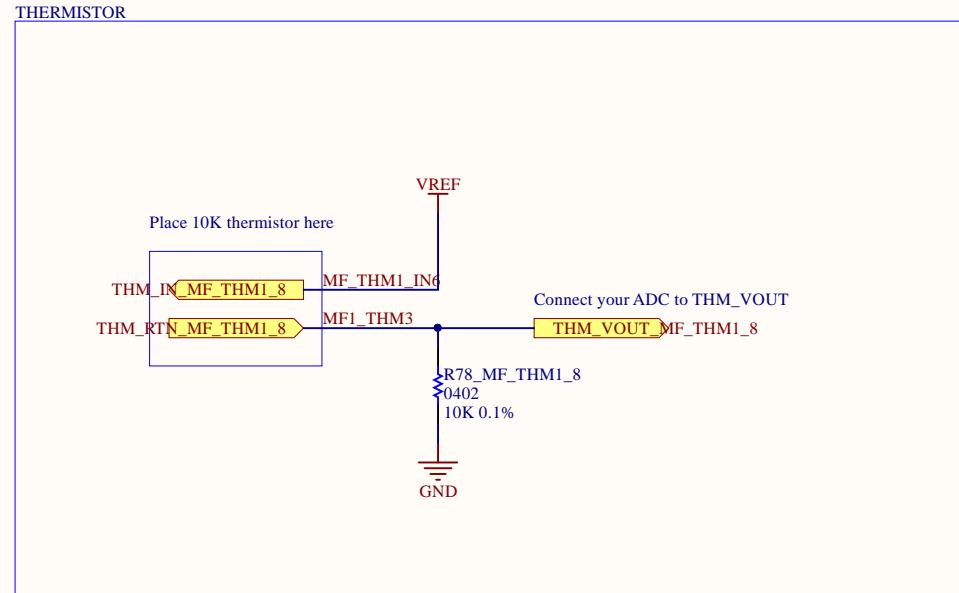
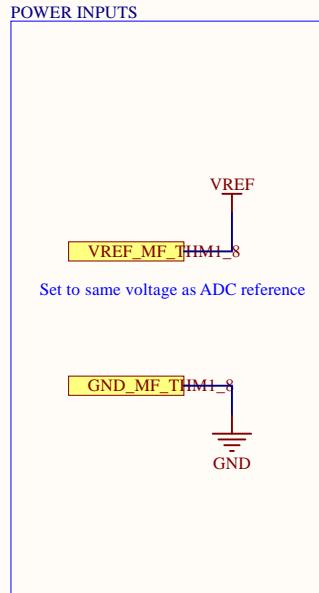
D

Title: thermistor-input-10k.SchDoc UTAT SS

Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.3 of 47
File:	C:\Users.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

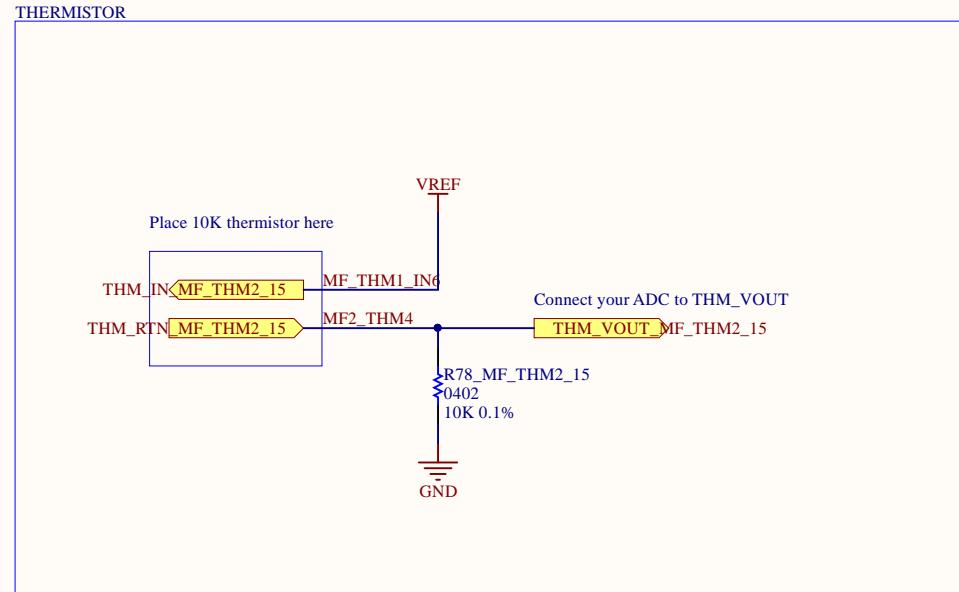
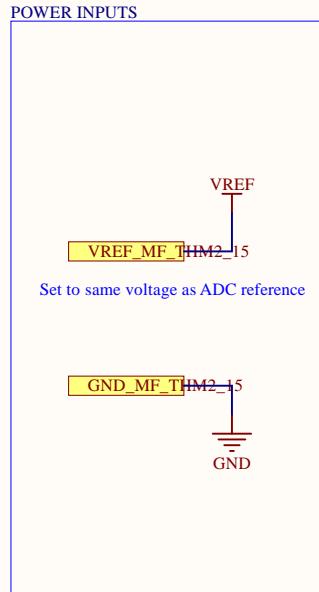
D

D

Title		
thermistor-input-10k.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.3 of 47
File:	C:\Users\.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

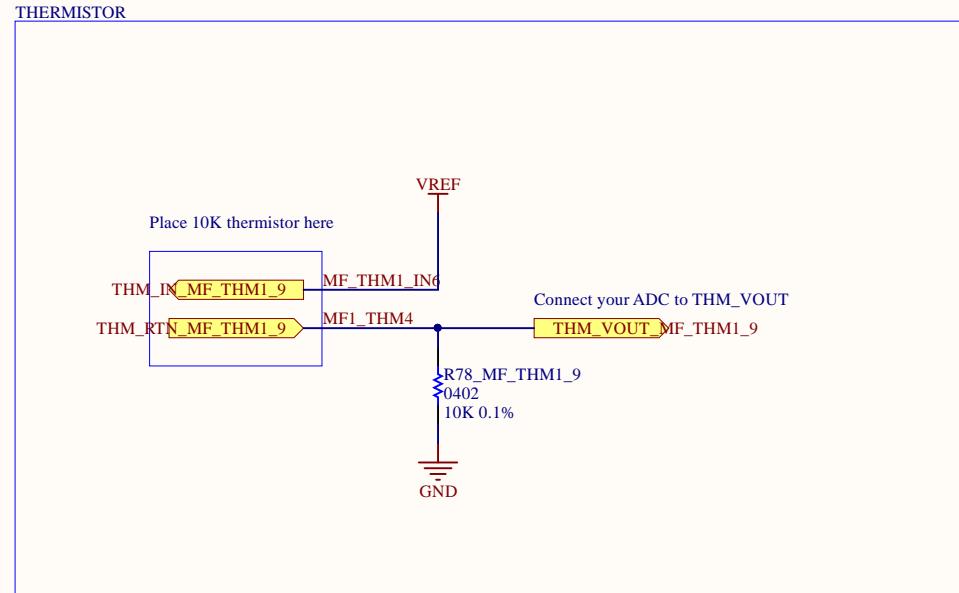
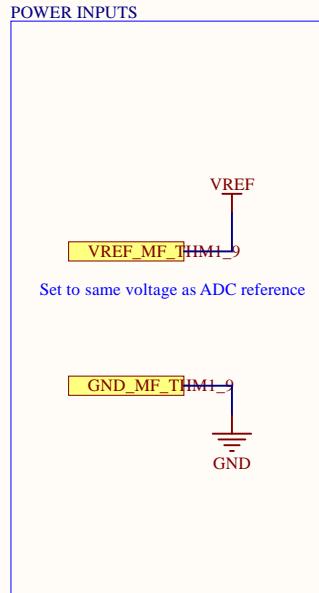
D

D

Title		
thermistor-input-10k.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.4 of 47
File:	C:\Users\.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

D

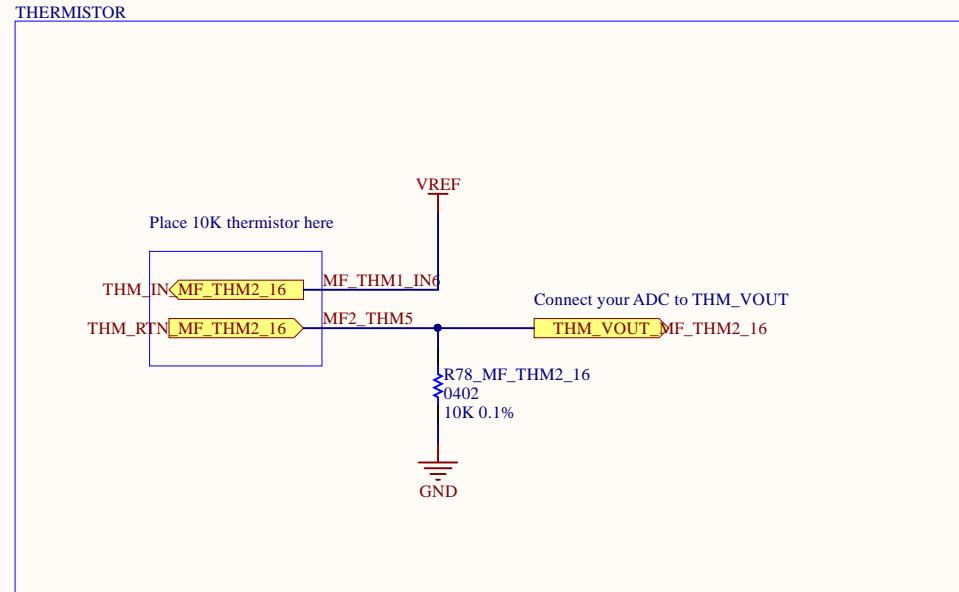
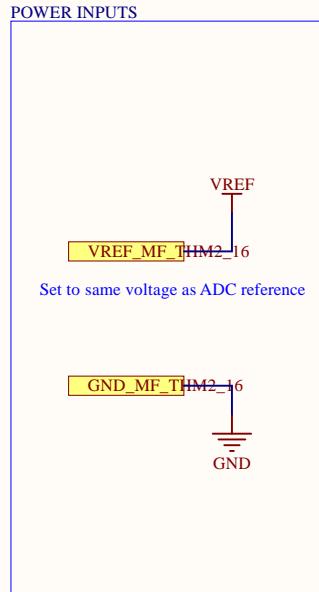
D

Title: thermistor-input-10k.SchDoc UTAT SS

Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.4 of 47
File:	C:\Users.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

D

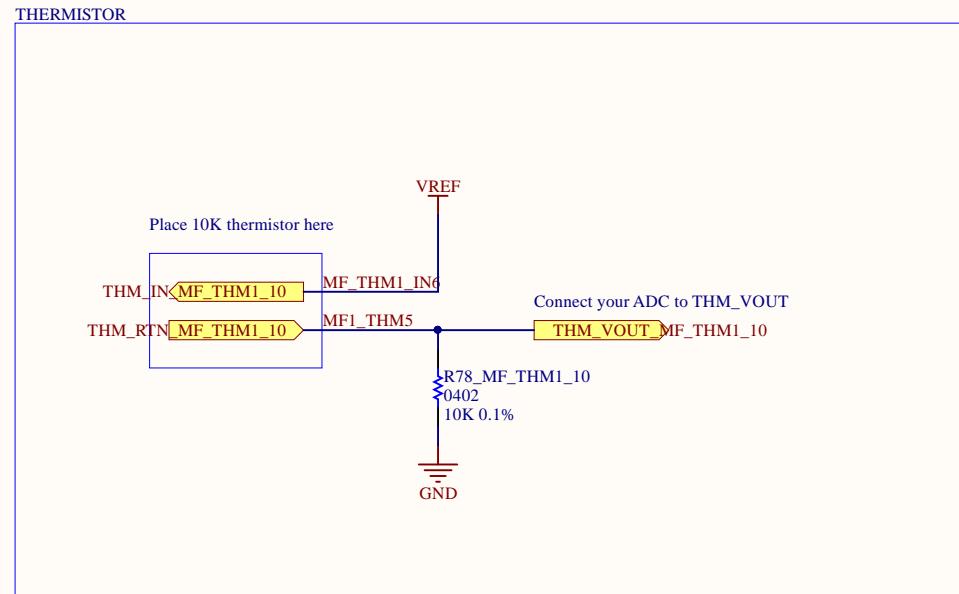
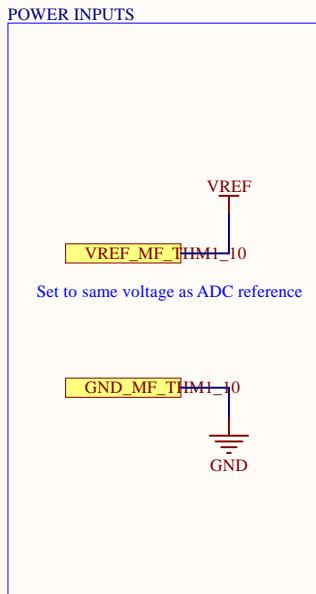
D

Title: thermistor-input-10k.SchDoc UTAT SS

Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.5 of 47
File:	C:\Users.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

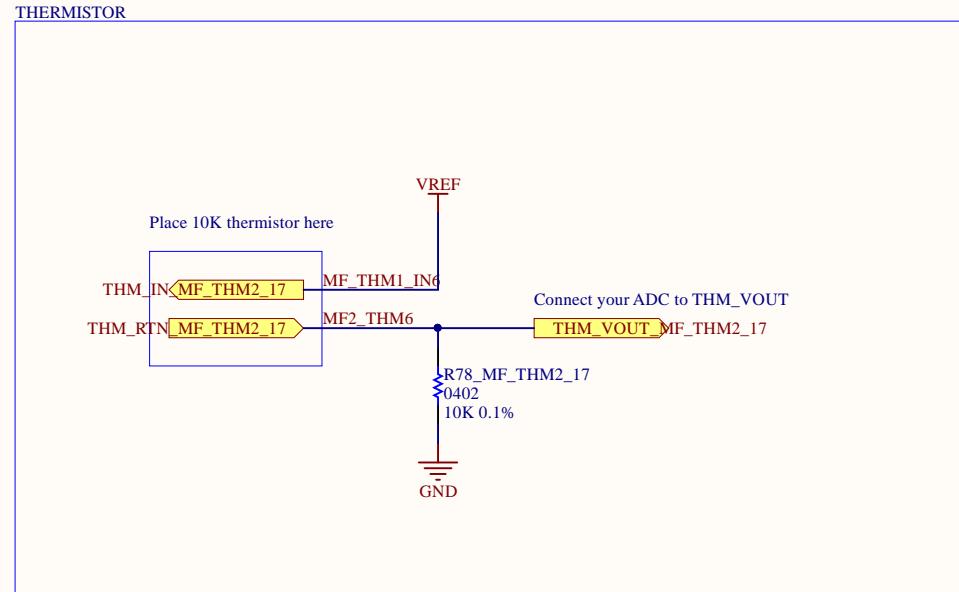
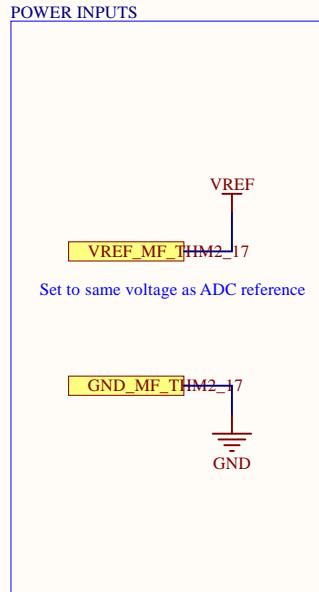
D

D

Title		
thermistor-input-10k.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.5 of 47
File:	C:\Users\.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

C

D

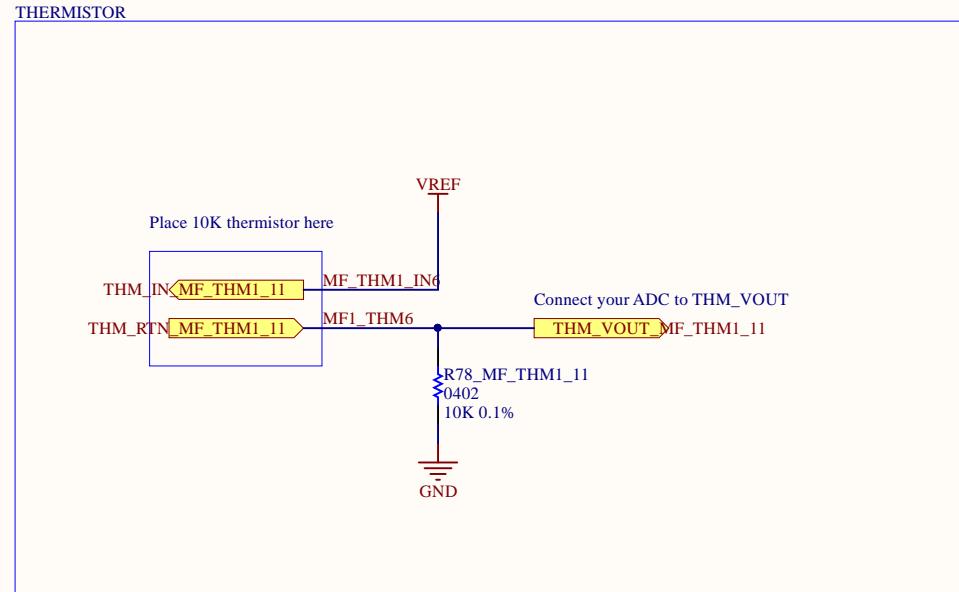
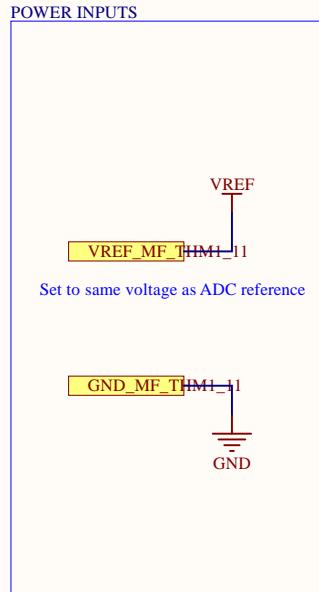
D

Title
thermistor-input-10k.SchDoc UTAT SS

Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.6 of 47
File:	C:\Users\.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

A

A



B

B

C

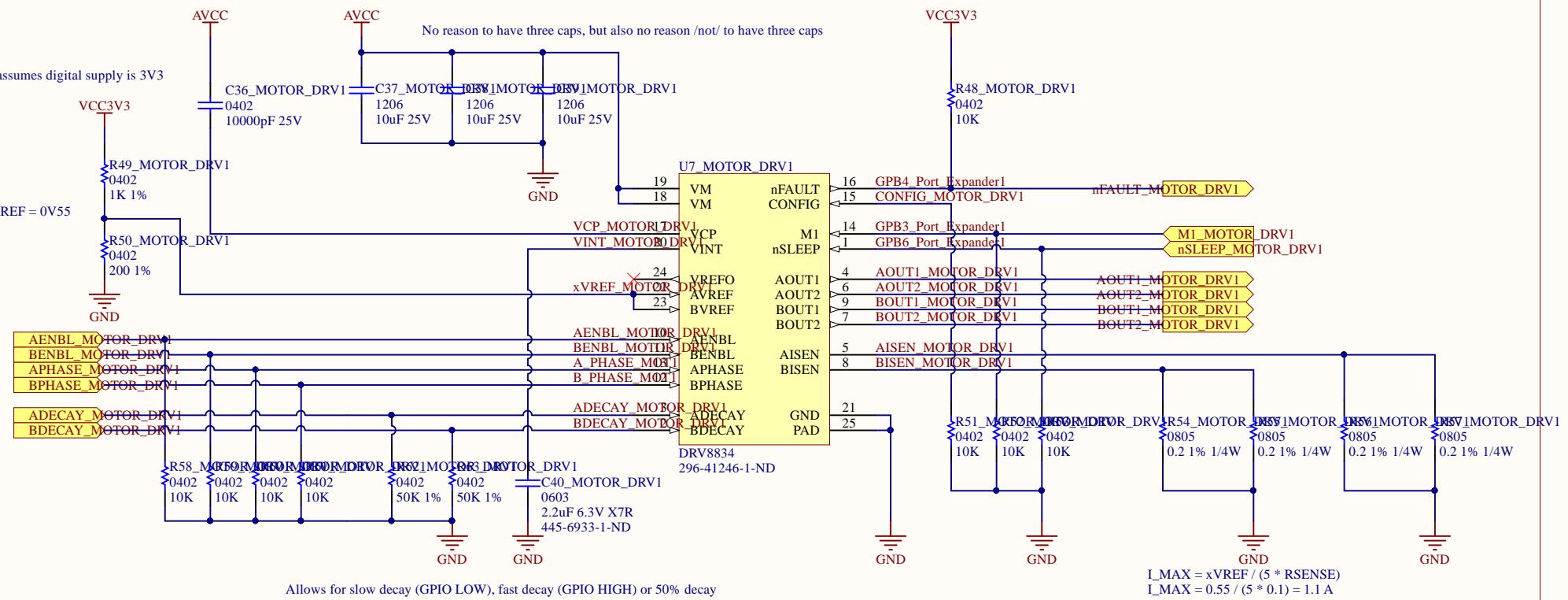
C

D

D

Title		
thermistor-input-10k.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.2
Date:	2019-09-10	Sheet 14.6 of 47
File:	C:\Users.\thermistor-input-10k.SchDoc	Drawn By: B. Almeida, D. Vogel

DRV8834 LAYOUT



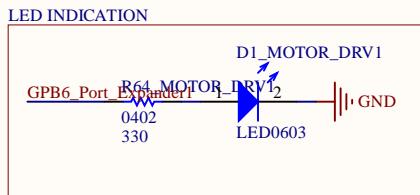
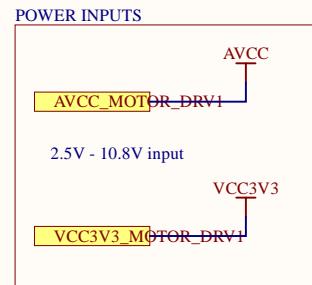
DRV8834 Motor Driver Notes

Datasheet: <http://www.ti.com/lit/ds/symlink/dr8834.pdf>

Indexer mode of this motor driver was tested to be not functioning, so everything is set in hardware to implement only the PHASE/ENABLE mode.

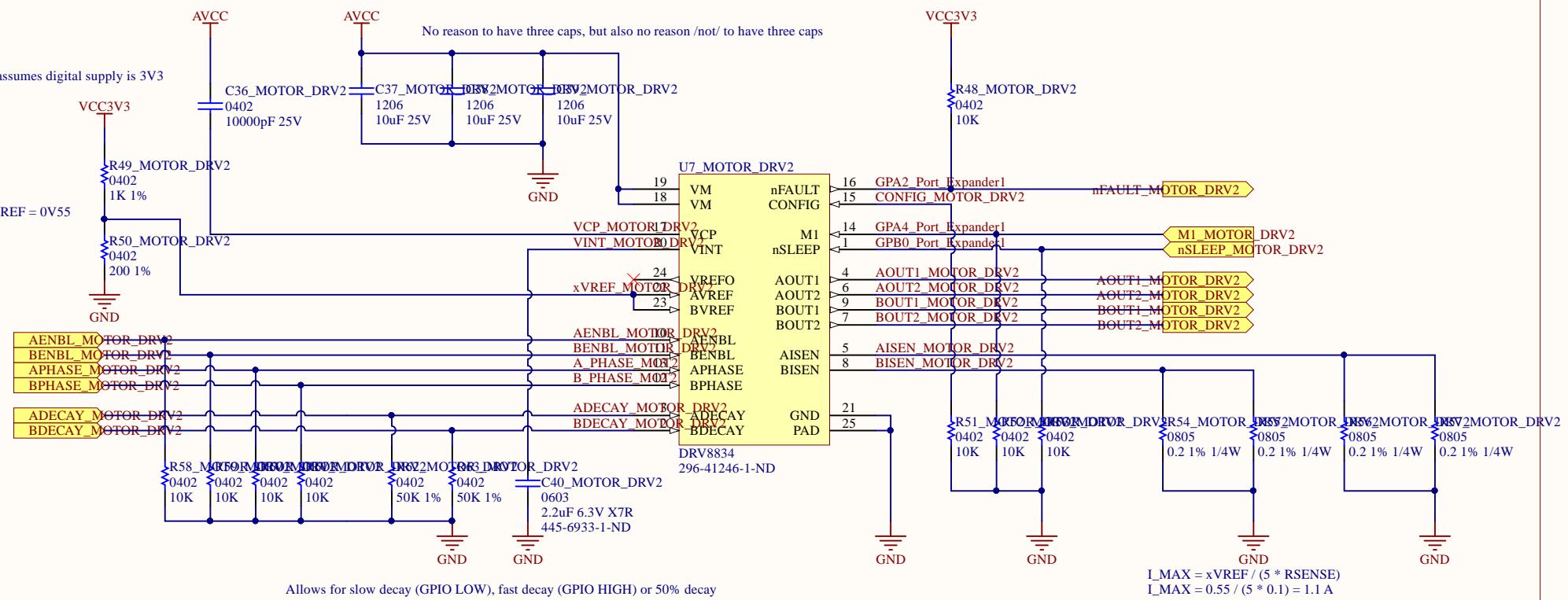
Implemented a voltage divider to set-up the xVREF voltage if want to modify xISEN and the resistor later. VREFO is left unconnected.

About decay settings: decay mode is selected by the voltage presented at the xDECAY pins in PHASE/ENABLE mode. It is also recommended with a pull-down to ground and a GPIO for setting.



Title		
DRV8834.SchDoc		UTAT SS
Size	Number	Revision
A4	15.1	v4.2
Date:	2019-09-10	Sheet 15.1 of 47
File:	C:\Users\.\DRV8834.SchDoc	Drawn By: Lorna Lan, Dylan Vogel

DRV8834 LAYOUT



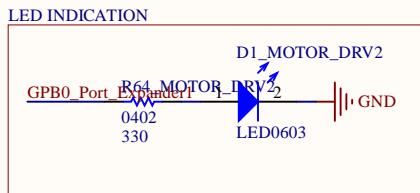
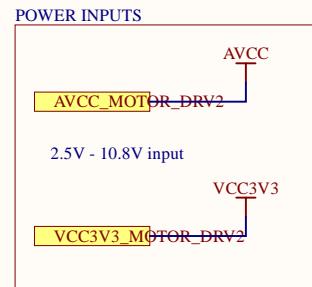
DRV8834 Motor Driver Notes

Datasheet: <http://www.ti.com/lit/ds/symlink/dr8834.pdf>

Indexer mode of this motor driver was tested to be not functioning, so everything is set in hardware to implement only the PHASE/ENABLE mode.

Implemented a voltage divider to set-up the xVREF voltage if want to modify xISEN and the resistor later. VREFO is left unconnected.

About decay settings: decay mode is selected by the voltage presented at the xDECAY pins in PHASE/ENABLE mode. It is also recommended with a pull-down to ground and a GPIO for setting.



Title		
DRV8834.SchDoc		UTAT SS
Size	Number	Revision
A4	15.2	v4.2
Date:	2019-09-10	Sheet 15.2 of 47
File:	C:\Users\.\DRV8834.SchDoc	Drawn By: Lorna Lan, Dylan Vogel

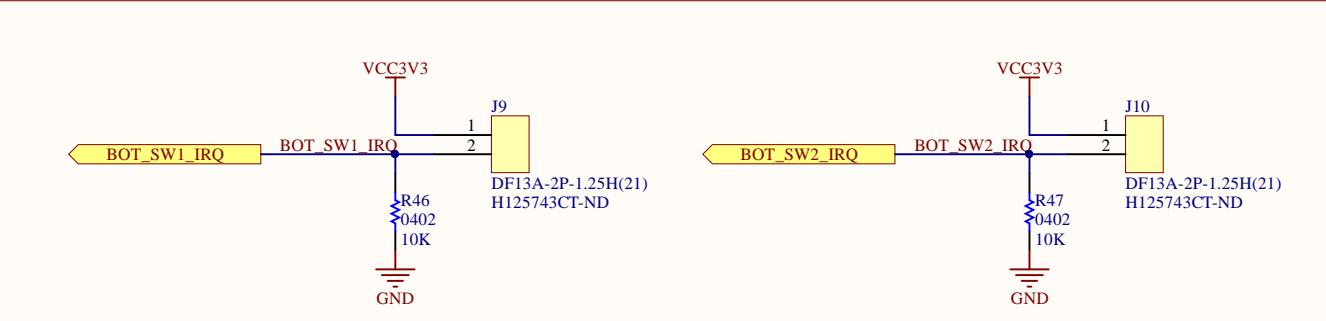
A

TOP LIMIT SWITCHES



B

BOTTOM LIMIT SWITCHES



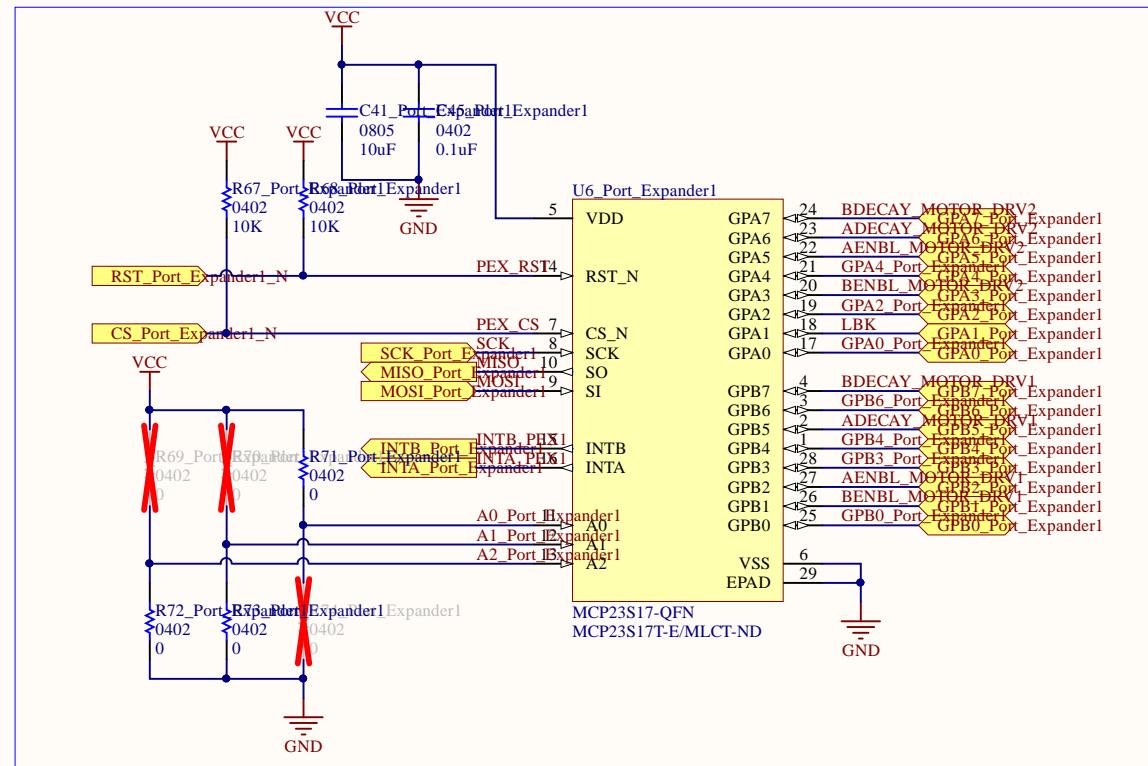
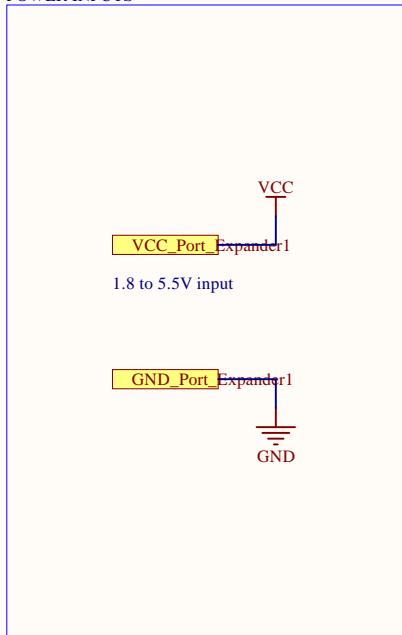
C

CONNECT TO NORMALLY-OPEN SWITCH FOR RISING EDGE INTERRUPT

D

Title		UTAT SS
motors-state-monitor.SchDoc		
Size	Number	Revision
A4	16	v4.2
Date:	2019-09-10	Sheet 16 of 47
File:	C:\Users\.\motors-state-monitor.SchDoc	Drawn By: Lorna Lan, Dylan Vogel

POWER INPUTS



ADDRESS: 0b001

CHANNEL SELECTION

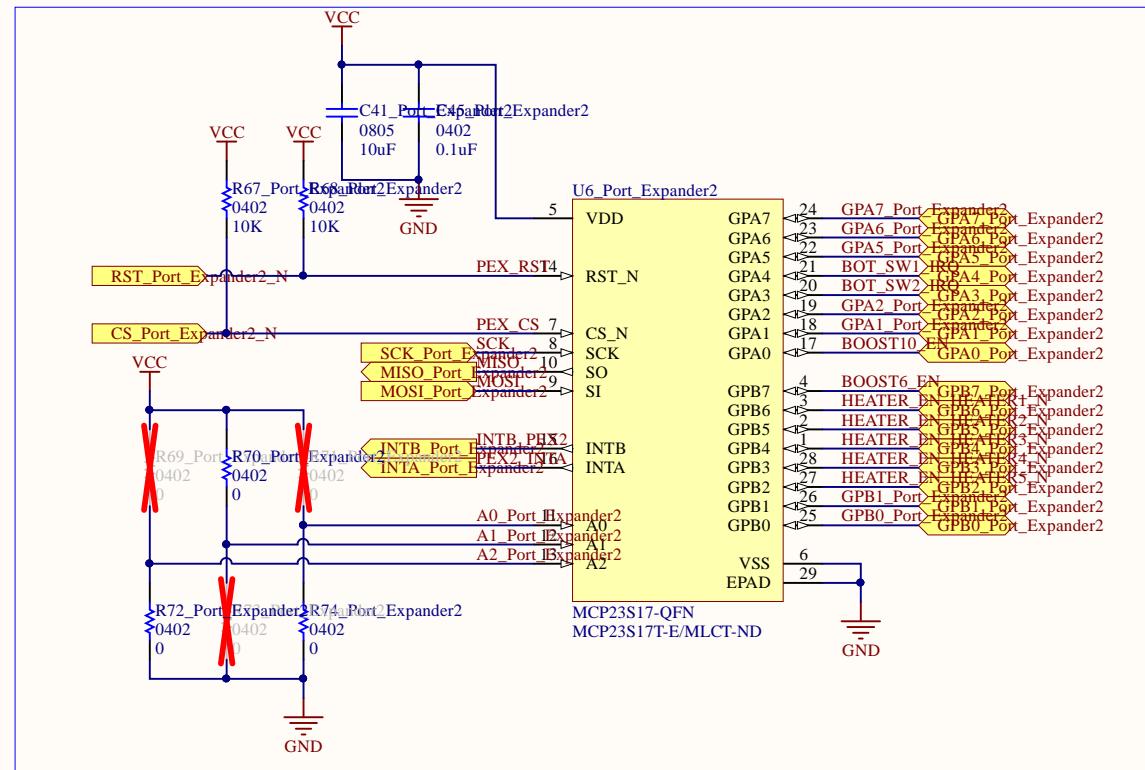
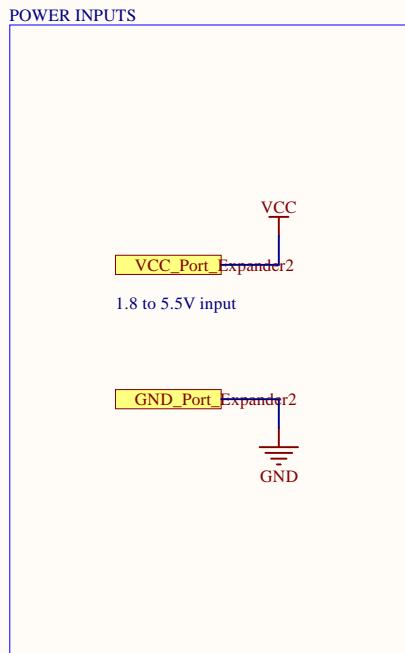
ONLY SOLDER ONE 0 OHM FROM EACH PAIR
PEX ADDRESS = A2 A1 A0
VCC == 1 GND == 0

This schematic implements the MCP23S17 SPI port expander, and does some common-sense things like adding a bypass capacitor to the power supply and pull-up resistors to **RST_N** and **CS_N**.

Multiple port expanders can be connected to the same **CS_N** line, and accessed via a device address that is used during software communication. This address is set in hardware via the **A2**, **A1** and **A0** pins. Soldering a 0 ohm resistor to **VCC** will set that bit to 1, and soldering to **GND** will set that bit to 0.

In the schematic which includes this file, you should make some note of the relevant hardware address that should be soldered during manufacturing.

Title		
pex-MCP23S17.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-09-10	Sheet 17.1.1 of 47
File:	C:\Users.\pex-MCP23S17.SchDoc	Drawn By: Dylan Vogel



ADDRESS: 0b010

CHANNEL SELECTION

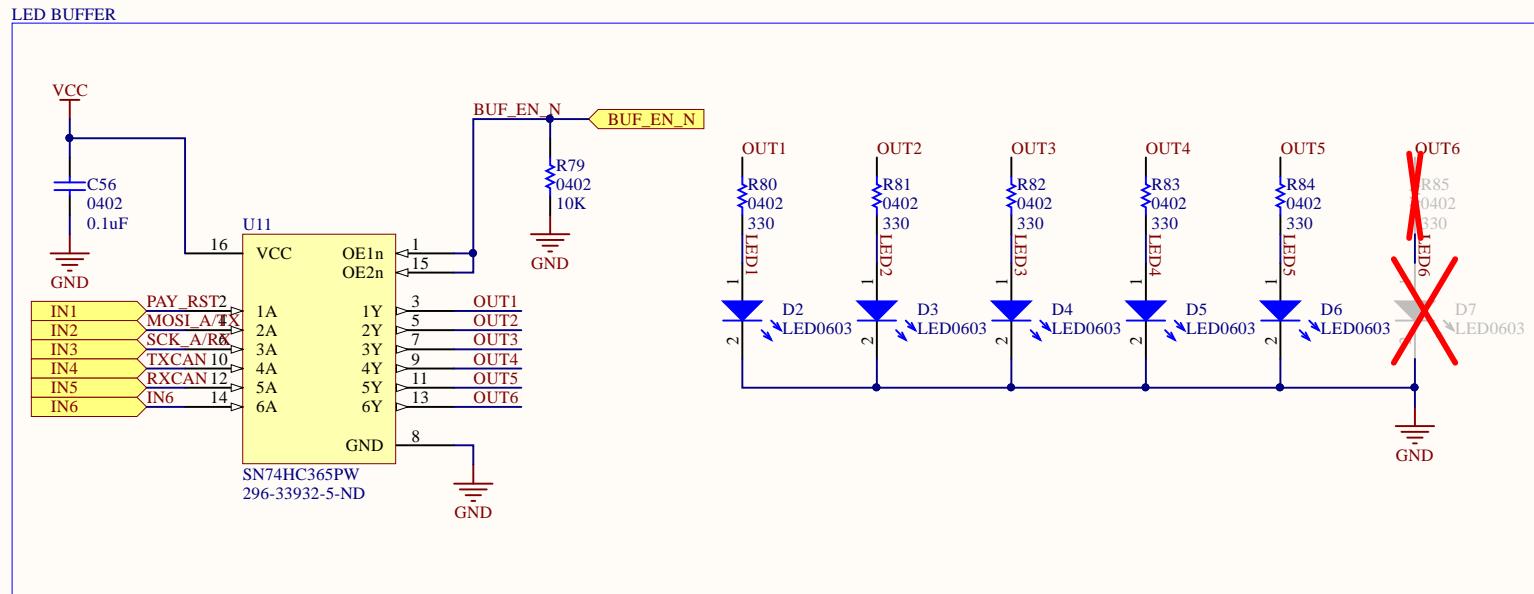
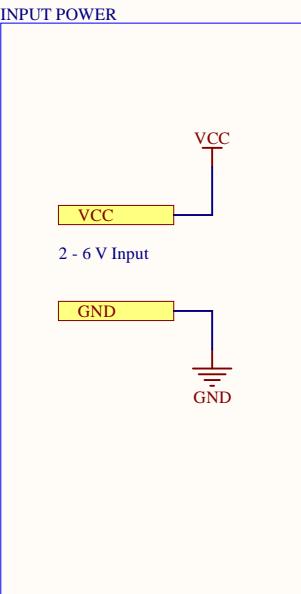
**ONLY SOLDER ONE 0 OHM FROM EACH PAIR
PEX ADDRESS = A2 A1 A0
VCC == 1 GND == 0**

This schematic implements the MCP23S17 SPI port expander, and does some common-sense things like adding a bypass capacitor to the power supply and pull-up resistors to RST_N and CS_N.

Multiple port expanders can be connected to the same CS_N line, and accessed via a device address that is used during software communication. This address is set in hardware via the A2, A1 and A0 pins. Soldering a 0 ohm resistor to VCC will set that bit to 1, and soldering to GND will set that bit to 0.

In the schematic which includes this file, you should make some note of the relevant hardware address that should be soldered during manufacturing.

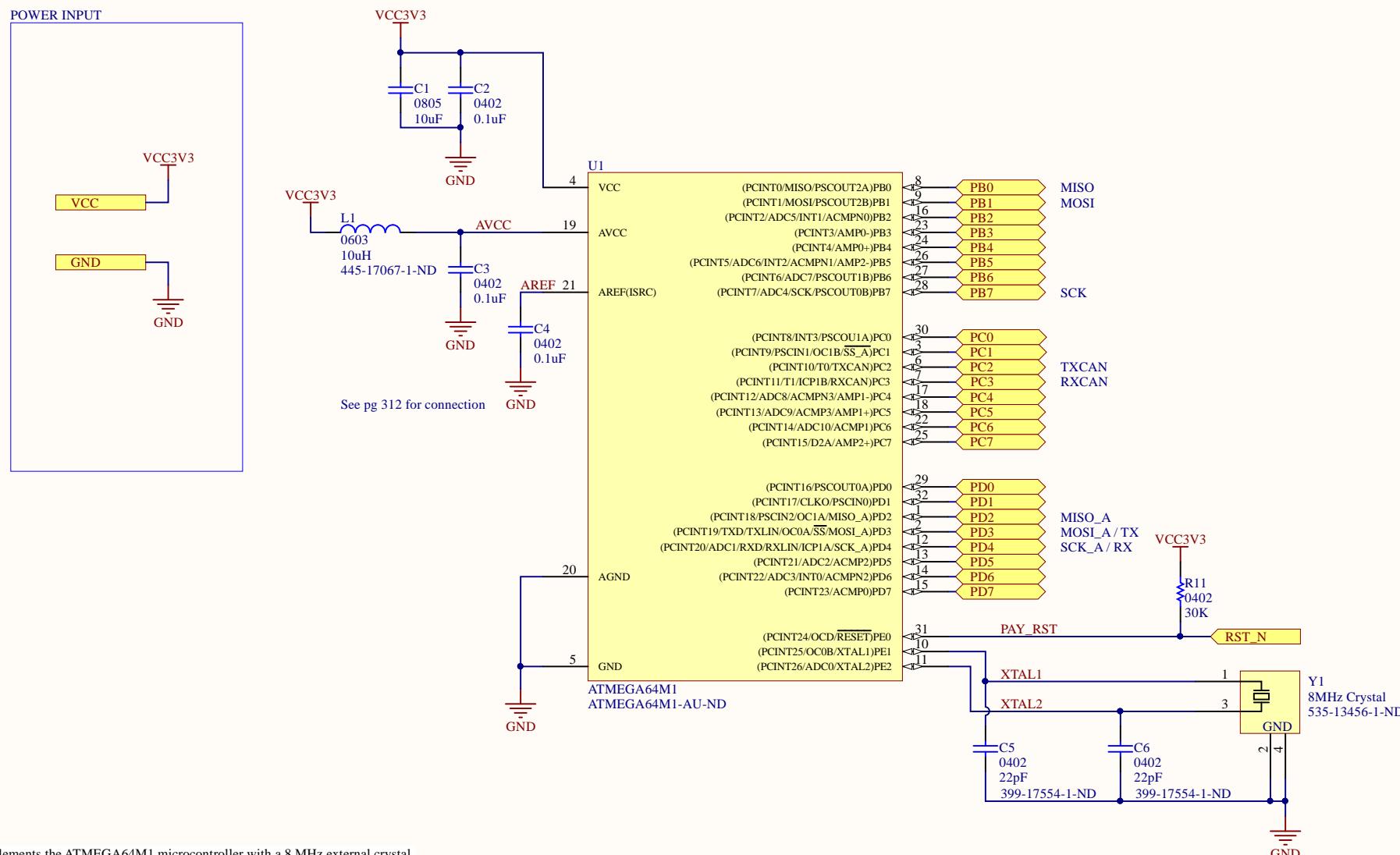
Title		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-09-10	Sheet 17.2.1 of 47
File:	C:\Users\...\pex-MCP23S17.SchDoc	Drawn By: Dylan Vogel



This schematic implements the SN74HC365PW non-inverting, tri-state hex buffer as an LED monitoring circuit. Connecting a signal to IN[1:6] will light up the corresponding LED on OUT[1:6].

- The BUF_EN_N input can be connected to a microcontroller to control the buffer. An input HIGH will set the outputs to high-impedance and disable the LEDs.
- In the schematic symbol which references this schematic sheet, parameters LED[1:6] can be added to specify the colour of each LED. See the micro-circuit common sheet for an example of this.
- Unconnected inputs should be grounded if you don't want random flickering of the LEDs.

Title		UTAT SS
led-monitoring-SN74HC365PW.SchDoc		
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-09-10	Sheet 18 of 47
File:	C:\Users...\led-monitoring-SN74HC365PW.SchDoc	By: Dylan Vogel

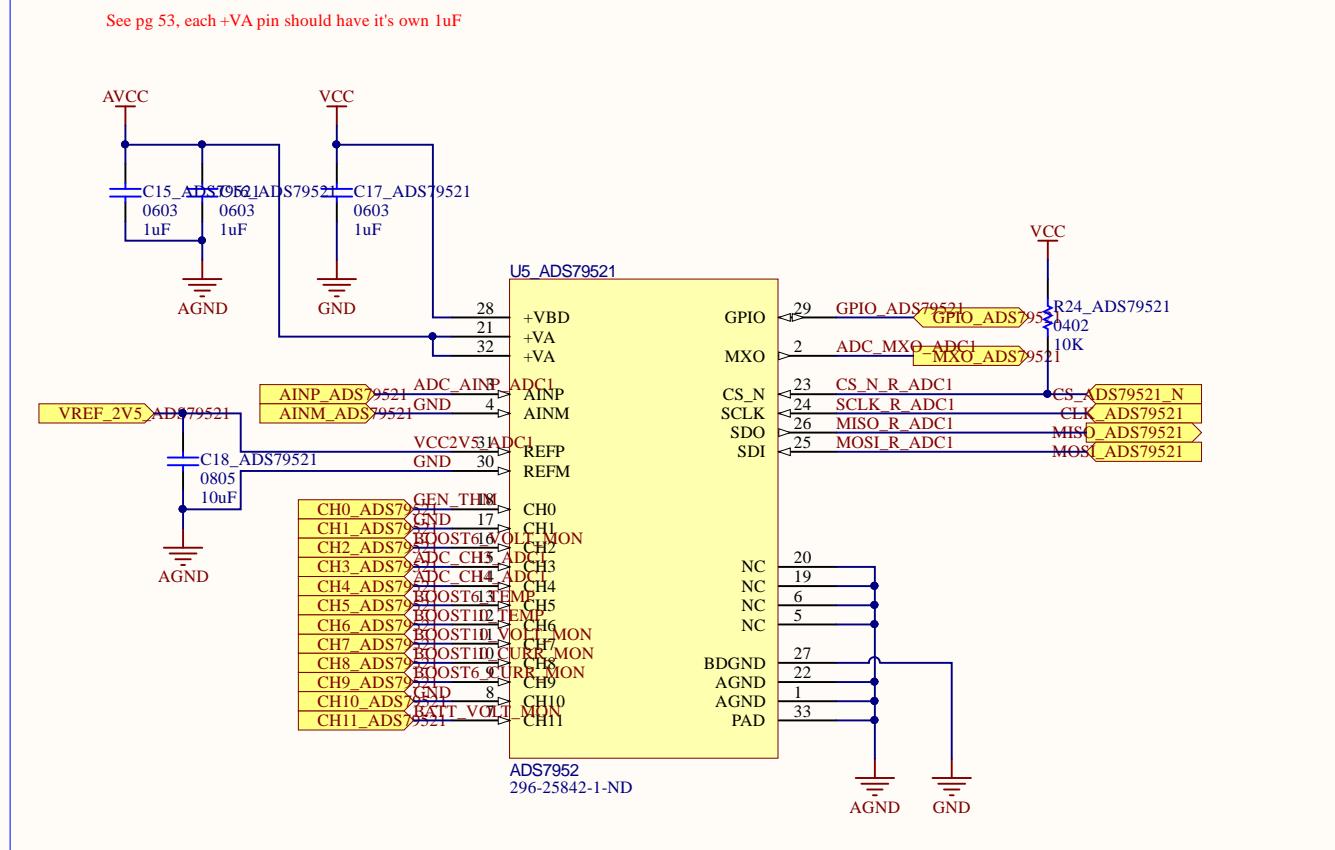
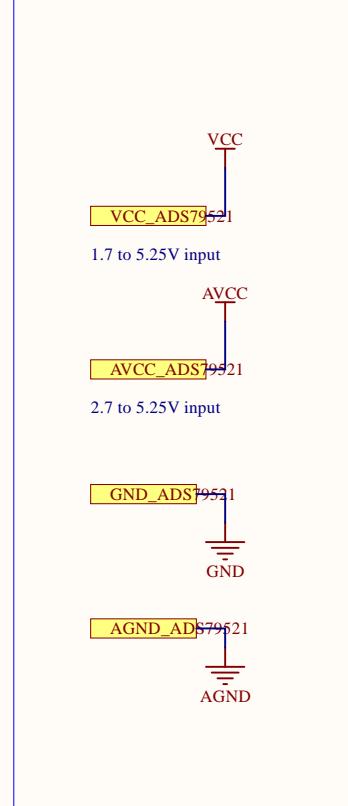


This schematic implements the ATMEGA64M1 microcontroller with a 8 MHz external crystal and necessary power connections.

- Crystal is connected in a Pierce configuration, values of the capacitors were calculated based on the capacitance of the crystal and ESR.
 - I would read through 18.5.2 and 18.6.2 of the complete 64M1 datasheet if you're interested in the motivation behind the ADC input connections. They recommend connecting AVCC through a RC lowpass network to minimize noise.
 - If the ADC functionality of the device is used, either AVCC or the internal 2.56 V source can be selected in software as the reference voltage.

Title		UTAT SS
micro-ATMEGA64M1.SchDoc		
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-09-10	Sheet 19 of 47
File:	C:\Users\...\micro-ATMEGA64M1.SchDoc	Drawn By: Dylan Vogel

POWER INPUTS
AVCC >= VCC (pg 51)

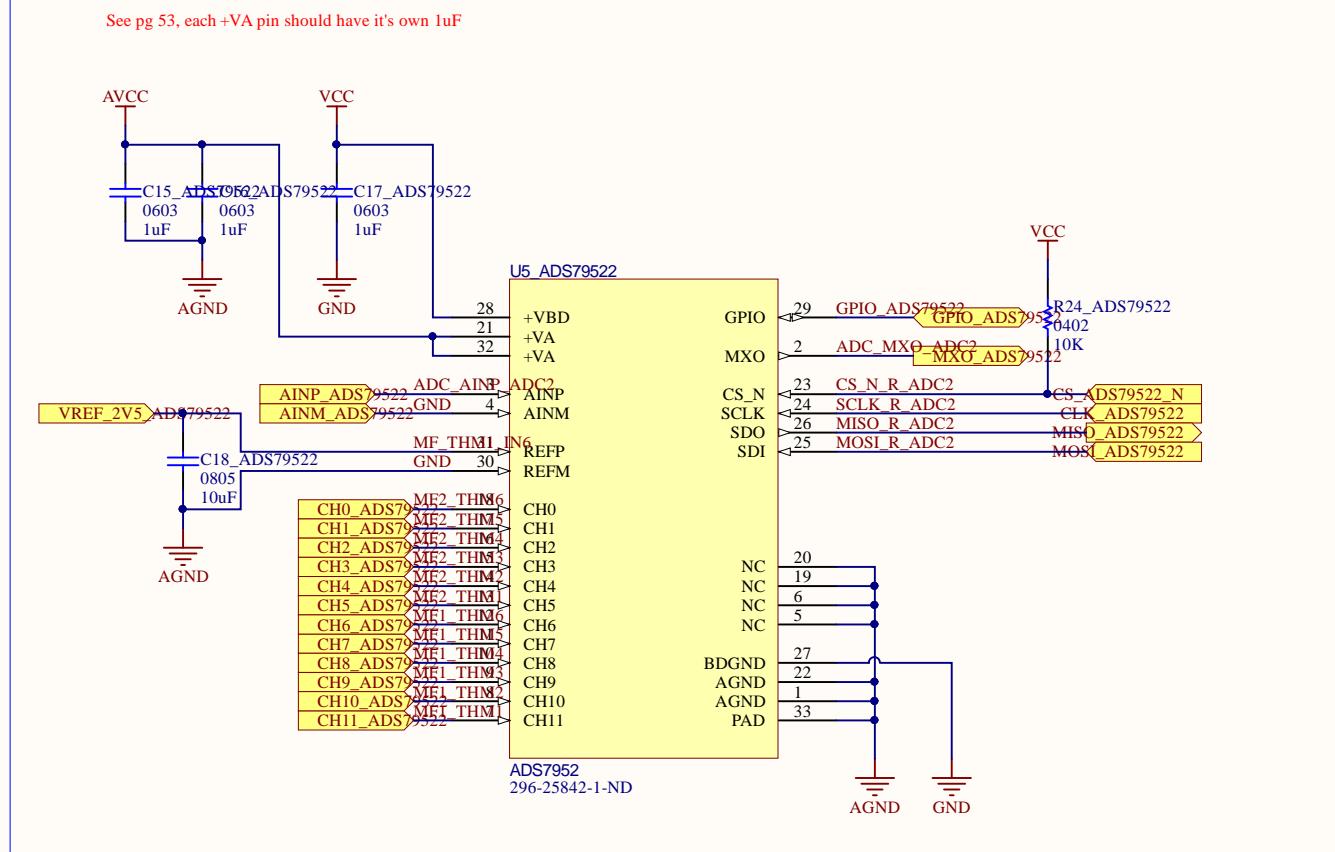
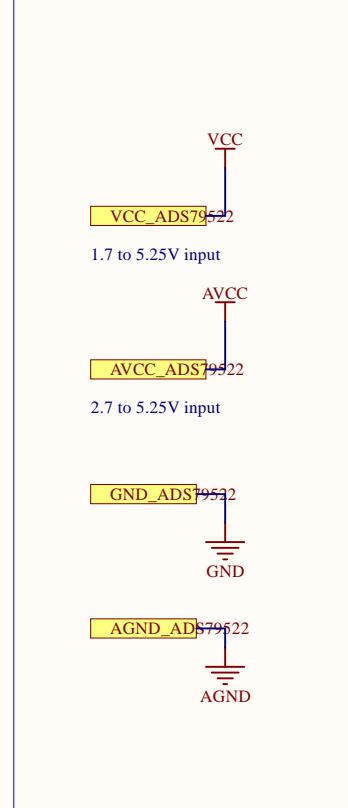


12 CHANNEL ADC

D

Title		
adc-ADS7952.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-09-10	Sheet 20.1.bf 47
File:	C:\Users\.\adc-ADS7952.SchDoc	Drawn By: Dylan Vogel

POWER INPUTS
AVCC >= VCC (pg 51)



12 CHANNEL ADC

Title		
adc-ADS7952.SchDoc		UTAT SS
Size	Number	Revision
A4	PCBS-COMMON	1.1
Date:	2019-09-10	Sheet 20.2.bf 47
File:	C:\Users\.\adc-ADS7952.SchDoc	Drawn By: Dylan Vogel

