VEHICLE COLLISION AVOIDANCE WITH INTEGRATED PARKING GUIDANCE SYSTEM

A PROJECT REPORT

Submitted by

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in partial fulfillment for the award of the degree

of

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in

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We express our sincere gratitude to our Respected Correspondent **Dr. K. S. Lakshmi,** Ph.D and Principal **Dr. K. S. Babai,** B.Sc., B.E., M.S.,Ph.D, F.I.E., M.I.S.T.E.,for their constant encouragement, which has been our motivation to strive towards excellence. We wish to express our heartiest thanks to our Dean Academic **Dr. K. Umarani,** M.E., Ph.D.

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ABSTRACT

The project mainly concentrates on vehicle collision avoidance through vehicular communication and parking guidance system to enable effective parking. The driver assistant features are implemented using vehicle to vehicle and vehicle to infrastructure communication.

In our project we implement the forward collision avoidance system in which the vehicles transmit details to other vehicles in case of hard braking of the front vehicle or presence of any obstacle through ultra sonic sensing.

Emergency vehicles have a hard time making people aware of their presence. We include the emergency alert broadcast facility to emergency vehicles like ambulances, fire engines, etc., where the driver can respond and pave way for it.

The parking in big cities has become one of the key causes of the city traffic congestion. Sending parking details directly to the vehicle is one of the effective way to improve the parking situation. To design this parking guidance system we are using Infrared sensors which can detect the presence and absence of vehicles.

We have developed a prototype which facilitates all the three features namely vehicle collision avoidance, emergency vehicle alert and parking guidance.

LIST OF TABLES

LIST OF ABBREVIATIONS

S NO.	ABBREVIATION	DESCRIPTION
1.	DSRC	Dedicated Short Range Communication
2.	EEPROM	Electrically Erasable Programmable Read Only Memory
3.	EPO	Extended prediction Orbit
4.	EUSART	Enhanced Universal Synchronous/ Asynchronous Receiver/Transmitter
5.	LCD	Liquid Crystal display
6.	LED	Light Emitting Diode
7.	LOS	Line Of Sight
8.	GPS	Global Positioning System
9.	GSM	Global System for Mobile communication
10.	I^2C	Inter Integrated Circuit
11.	MCU	Micro controller
12.	MSSP	Master Synchronous Serial Port
13.	NMEA	National Marine Electronics association
14.	OBU	On Board Unit
15.	PIC	Peripheral Interface Controller
16.	PWM	Pulse Width Modulation
17.	RADAR	RAdio Detection And Ranging

18.	RAM	Random Access Memory
19.	RFID	Radio Frequency Identification
20.	RISC	Reduced Instruction Set Computers
21.	ROM	Read Only Memory
22.	RSU	Road Side Unit
23.	SFR	Special Function Register
24.	SKG	SKynet Global limited
25.	SPI	Serial Peripheral Interface
26.	TTFF	Time To First Fix
25.	UART	Universal Asynchronous Receiver/Transmitter
26.	USART	Universal Synchronous/Asynchronous Receiver/Transmitter
27.	VANET	Vehicular Adhoc NETworks
28.	WITS	Wireless sensor network for Intelligent Transportation system
29.	WSN	Wireless Sensor Networks

LIST OF FIGURES

CHAPTER-1

INTRODUCTION

1.1 ROAD SAFETY

Road traffic safety refers to methods and measures for reducing the risk of a person using the road network being killed or seriously injured. The users of a road include pedestrians, cyclists, motorists, their passengers, and passengers of on-road public transport, mainly buses and trams.

The vehicle collision and its impact emerged as the major problem in the last two decades when the use of the automobile increased to a subsequent number A traffic collision, also known as a motor vehicle collision (MC), traffic accident, motor vehicle accident, car accident, automobile accident, road traffic collision, road traffic accident, wreck, car crash, or car smash occurs when a vehicle collides with another vehicle, pedestrian, animal, road debris, or other stationary obstruction, such as a tree or utility pole. Traffic collisions may result in injury, death, vehicle damage, or/and property damage.

A number of factors contribute to the risk of collision, including vehicle design, speed of operation, road design, road environment, driver skill and/or impairment, and driver behaviour. Out of these driver's unawareness leads to maximum number of accidents. Worldwide, motor vehicle collisions lead to death and disability as well as financial costs to both society and the individuals involved.

Road injuries resulted in 1.4 million deaths in 2013 up from 1.1 million deaths in 1990. Almost all high-income countries have decreasing death rates, while the majority of low-income countries having increased deaths rates due to traffic collisions. Middle-income countries have the highest rate with 20 deaths per 80,000 inhabitants, 80% of all road fatalities by only 52% of all vehicles.

In order to avoid such situations and provide the driver with assistance researches are undertaken by different companies and research centres. Different technologies like VANET , WSN, Electromagnetic Interface etc.

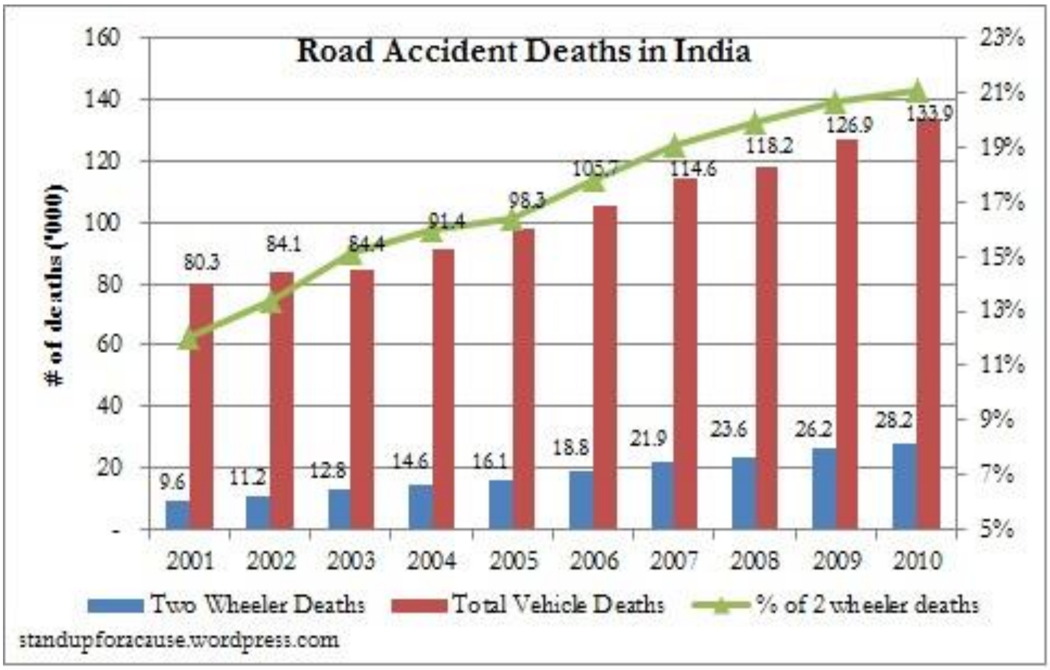

Figure 1. Statistics on number of road accident deaths

Emerging wireless technologies for vehicle-to-vehicle (V2V) and vehicle to-roadside (V2R) communications such as DSRC [1] are promising to dramatically reduce the number of fatal roadway accidents by providing early warnings.

CHAPTER 2

LITERATURE SURVEY

Internet can also be used monitor the traffic status. This concept was prop by Hu Lingling et al(2011).According to this concept, a vehicle is allotted with a unique identification number and it's written electronically in the RFID tag. When the vehicle reaches the base station area, the RFID tag is read and Internet facility is provided. Using GPS, the traffic status is obtained through internet thereby the drivers can take ultimate free path to reach their destination easily. The drawbacks of this system are given by

1. Unwanted delay in reading the RFID tag
2. Internet users are increased nowadays lads to network traffic. Therefore deadline can't be met some time in real-time application using Internet.

Pravin P Ashtankar et al(2009) proposed a solution to prevent accidents. The central idea of the system is to enable vehicles within each other proximity to be aware of their own location and then estimate their position with respect to other vehicles. This is accomplished with the help of two main technologies called GPS and RADAR. The drawbacks of this system are given by

1. The non unique spectral properties of their retuned RADAR signal that may lead to the improper detection .
2. The targets which are nearer to the RADAR cannot be detected easily rather it saturated the receiver

Navin kumar et al (2012) stated that traffic information can be broadcasted using visible light communication. According to their proposal the currently available traffic light controller made with light emitting diode can be used to broadcast the traffic data. This is line of sight communication. The vehicle which receives the information can relay it to the vehicle behind it using brake lights at the rear panel. This leads to adhoc v2v communication. LOS communication between the v2i and i2v are also possible to get information about present traffic condition. This system is proved to be effective if the communication range is less than 40m as LED’s and currently available TLC have been used, this system is cost effective. The drawbacks

1.the communication range must be within 40m and should be LOS.

2.Since normal LED’s cannot be focused for long distance,therefore high power led’s are needed which inturn increases the cost.

Another major proposal was given by Mounib khanafer et al (2009). The wireless sensor network for intelligent transportation system(WITS) collects and communicates information to organize the traffic at intersections. This depends on fixed infrastructure composed of roadside units and intersection units. The communication is supported between v2v and v2i. Vehicle units send vehicle parameters to roadside units. Roadside units work on aggregating the received data before transferring them to the intersection unit which relays them to the final strategy subsystem. Drawbacks

1. This system is over dependent on infrastructure nodes located on the roadside.
2. No solution is proposed to avoid the collision in the communication between the vehicles.

Nazmus S Nafi and Jamil y khan(2012) suggested a solution to avoid the long waiting time at the junctions for the green signals. This scheme contains vehicles with onboard unit and will communicate with RSU. The RSU will get status info of the VLC and sends to OBU in range. Based on this information the driver can increase or decrease the speed to avoid wasting time. Drawbacks

1. Not suitable to reduce traffic congestion

2. status information must be updated frequently

S.Saravanan and T.Kavitha proposed a system for obstacle tracking using RFID and GSM. The obstacle detection is carried out using ultrasonic sensor. If any obstacles are detected, the information is sent to the operator who navigates the vehicle through Global System for Mobile communication (GSM). Drawbacks

1. Can’t be used over a wide number of users.
2. Doesn’t give information of emergency vehicles

Shival Dubey & Abdul Wahid Ansari proposed a Electromagnetic anti-collision device to avoid Vehicular Head to Head/Back collision that estimates the distance between the two vehicles running extreme traffic condition. It incorporates distance finding between two vehicles using ultrasonic range finder. In will work in two stages: - A Range finder will continuously track the distance between two vehicles moving and sends it to the ECM using these inputs if it finds the vehicle in the vicinity of the other it will automatically actuate the sensor strip for Electromagnetic Induction. Drawbacks

1. It is not cost efficient
2. Includes more hardware

Jie Liu et al. proposed a vehicle-to-vehicle communication protocol for cooperative collision warning. One major technical challenge addressed in this paper is to achieve low-latency in delivering emergency warnings in various road situations. Based on a careful analysis of application requirements, we design an effective protocol, comprising congestion control policies, service differentiation mechanisms and methods for emergency warning dissemination. Simulation results demonstrate that the proposed protocol achieves low latency in delivering emergency warnings and efficient bandwidth usage in stressful road scenarios.

Dr. Andreas Festag et al. Vehicular communication based on short-range wireless technology opens up novel applications improving road safety and travel comfort. Ad hoc networking enables a direct communication among cars as well as between cars and road-side communication devices. Geocast is an ad hoc routing scheme which is specifically considered in Europe as a core networking concept for future CAR-2-X systems. It provides wireless multi-hop communication and allows for geographical addressing and routing. This paper describes advanced concepts and mechanisms to deploy Geocast in realistic environments and presents NEC's CAR-2-X platform.

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CHAPTER-3

BLOCK DIAGRAM

The features included in our project can be explained using three main block diagrams.

3.1 CIVILIAN VEHICLE

The block diagram of the civilian vehicle where forward collsion avoidance feature and Infrastructure communication(parking guidance) has been equipped is shown in fig.1.

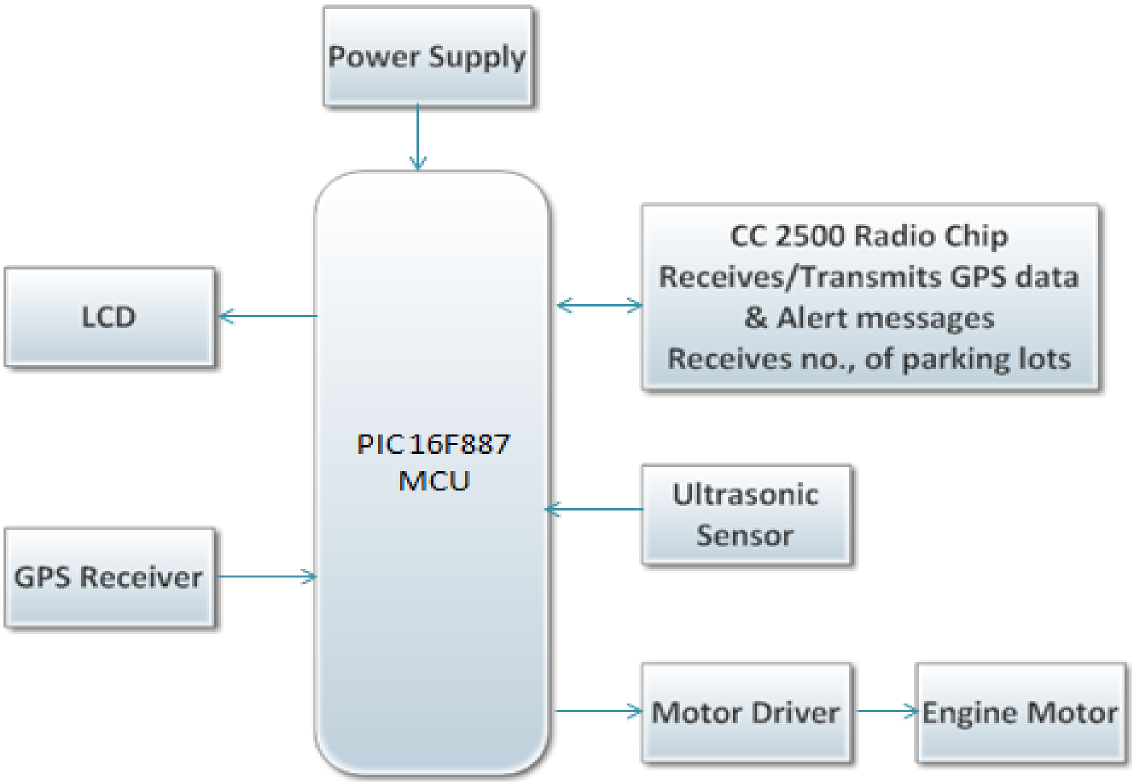

Figure 2. Block Diagram of Civilian vehicle

3.2 EMERGENCY VEHICLE

The emergency vehicle can also act as an ordinary vehicle. The block diagram of an emergency vehicle which broadcasts emergency messages is shown in fig.2.

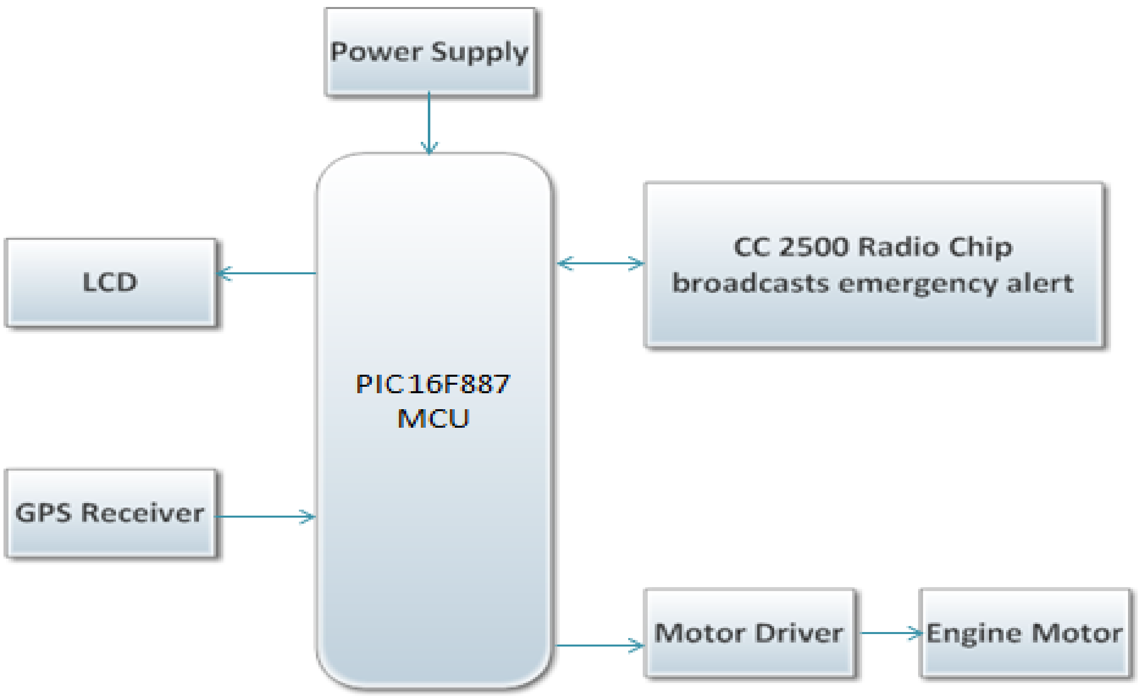

Figure 3. Block diagram of Emergency vehicle

3.3 INFRASTRUCTURE MODULE

The Infrastructure module assisting the parking guidance feature has been shown in fig.3.

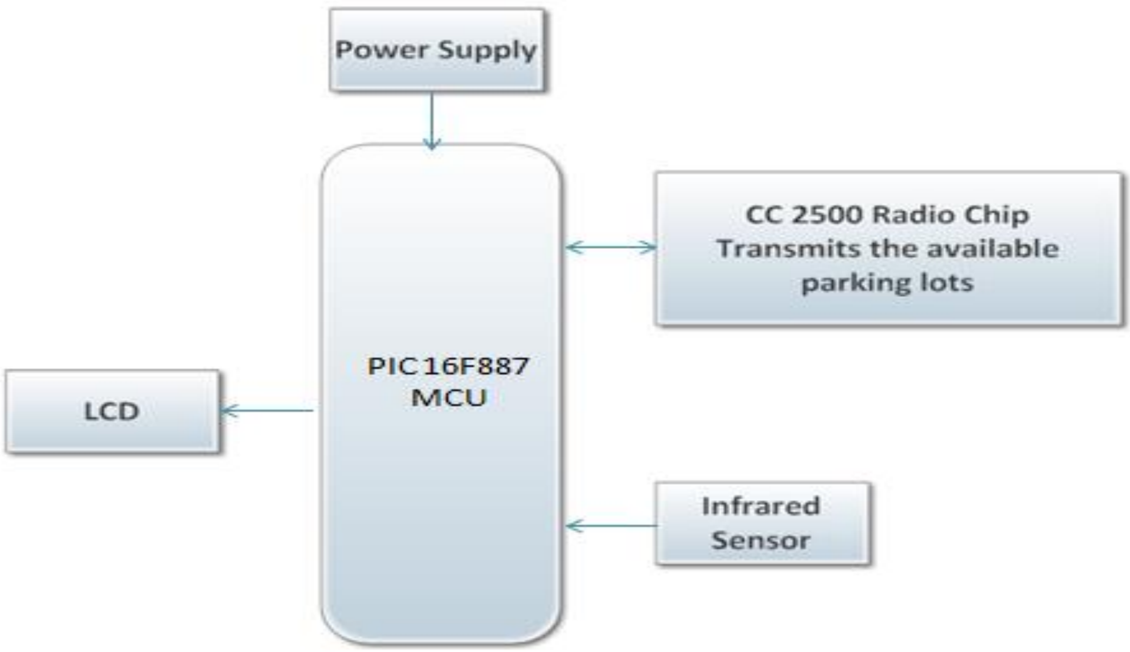

Figure 4. Block diagram of Infrastructure module

CHAPTER 4

PIC MICROCONTROLLER 16F887

4.1 INTRODUCTION TO MICRO CONTROLLER

A microcontroller is a small computer on a single integrated circuit containing a processor core, memory, and programmable input/output peripherals used mainly for embedded applications.

In our project, we use this powerful yet easy-to-program, CMOS FLASH-based 8-bit pic microcontroller which packs Microchip's powerful PIC architecture into an 40 pin package. For its low price, wide applications and easy availability it is used in industries, machine control, etc.

The important features it includes are,

- RISC Architecture with 35 instructions, all of which are single cycle instructions except for branches which has two cycles.
- Operating frequency of 0-20MHz.
- Precision internal oscillator with frequency range of 8-31 KHz.
- Power supply voltage of 2-5.5V.
- 8K ROM memory with FLASH. The chip could be reprogrammed upto 80,000 times.
- 368 bytes RAM Memory.
- 256 bytes EEPROM Memory.
- 3 independent timers/counters
- Watch dog timer.
- 35 input/output pins(ports A,B,C,D&E)
- A/D Converter with 14 channels of 8 bit resolution.
- Enhanced USART module which supports RS-232,RS-485 and LIN2.0.

- Master Synchronous Serial Port which supports SPI and I^2C mode.
- 2 Analogue comparators with fixed voltage reference of 0.6V.
- PWM output steering control.

4.2 PIN DIAGRAM

40-pin PDIP

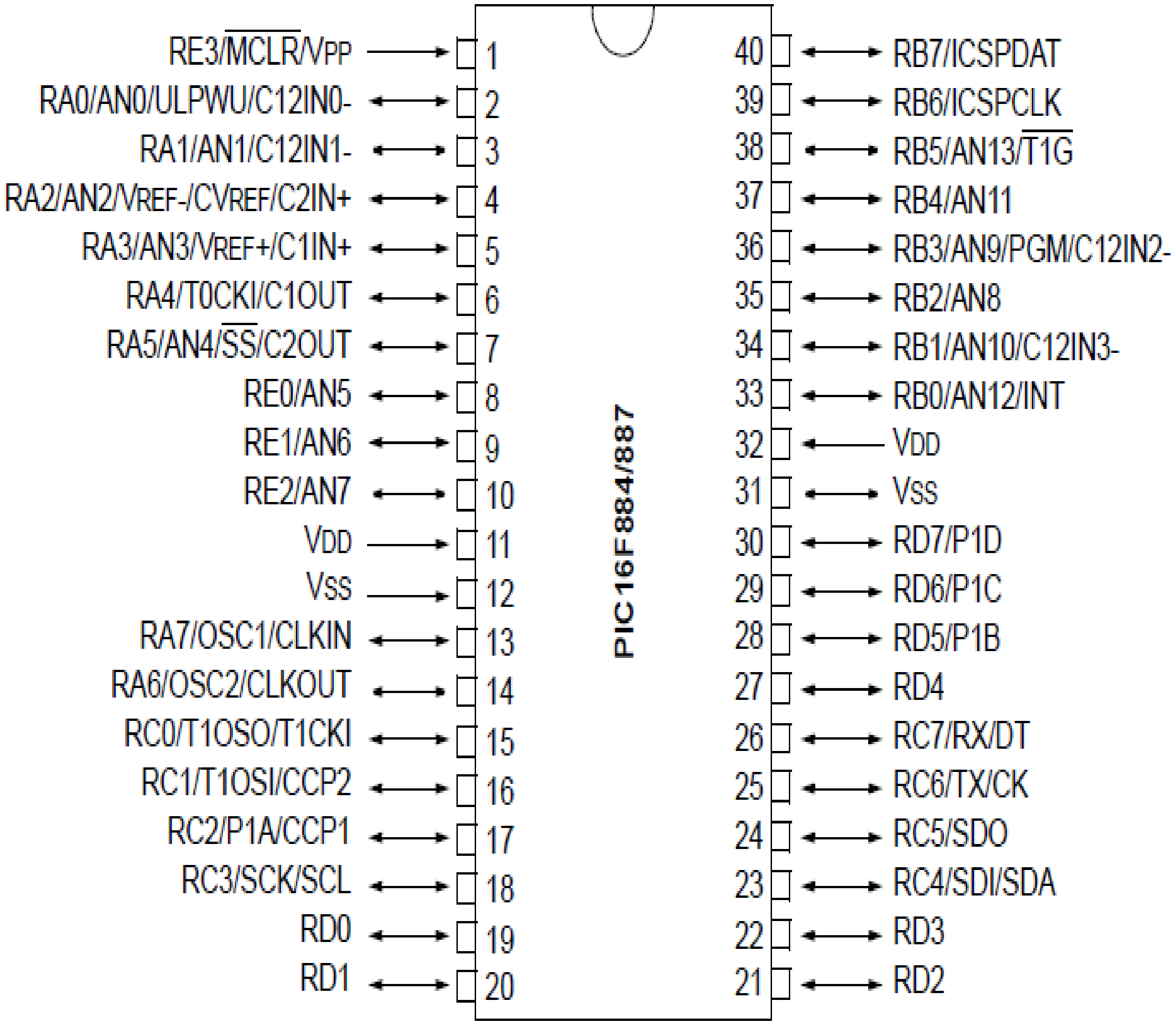

Figure 5. PIN diagram of PIC 16F887

4.3 BLOCK DIAGRAM

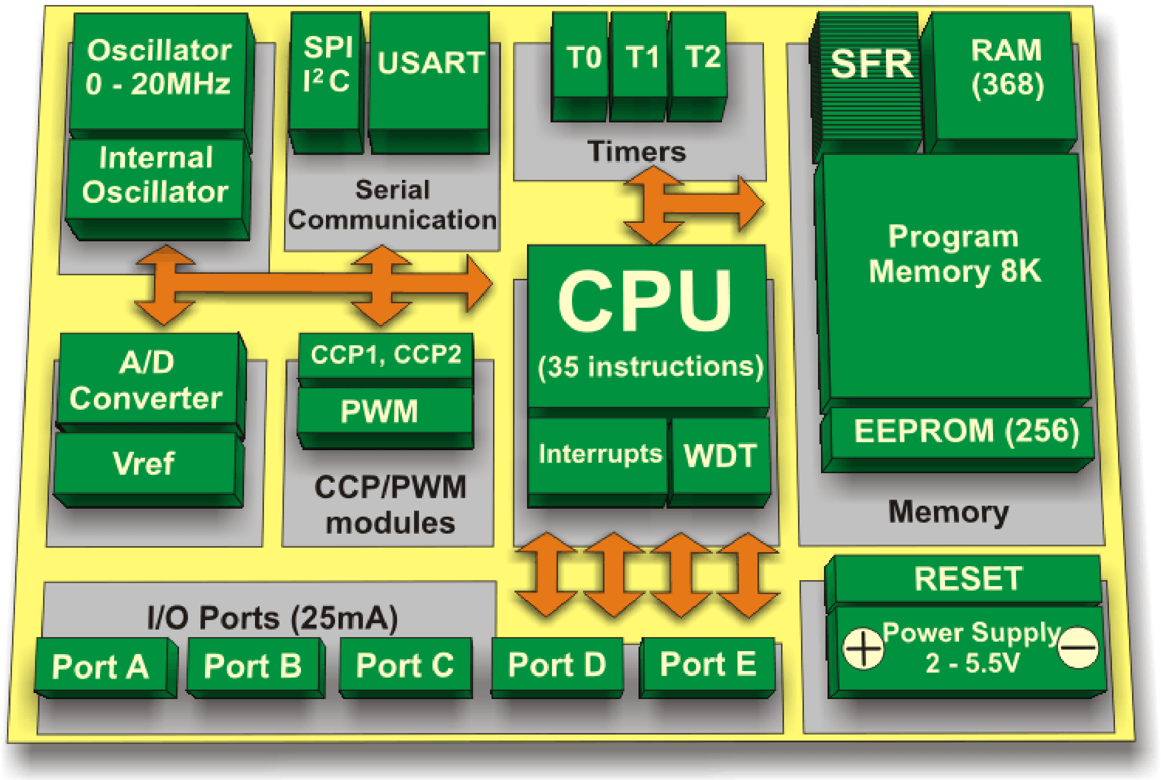

Figure 6. Block diagram of PIC 16F887

4.3.1 MEMORY UNIT

The PIC16F887 has three types of memory ROM, RAM and EEPROM. All of them has specific functions, features and organization.

4.3.1.1 PROGRAM MEMORY-ROM

ROM memory is used to permanently save the program being executed. This is why it is often called ‘program memory’. The PIC16F887 has 8Kb of ROM (in total of 8192 locations). Since the ROM memory is made with FLASH technology, its contents can be changed by providing a special programming voltage (13V).However, it is not necessary to explain it in detail as being automatically performed by means of a special program on the PC and a simple electronic device called the programmer.

4.3.1.2 EEPROM MEMORY

Similar to program memory, the contents of EEPROM is permanently saved, even when the power goes off. However, unlike ROM, the contents of EEPROM can be changed during the operation of the microcontroller. This is why this memory (256 locations) is perfect for permanently saving some of the results created and used during the operation.

4.3.1.3 DATA MEMORY-RAM

This is the most complex part of microcontroller memory. In this case, it consists of two parts: general-purpose registers and special-function registers (SFR). All these registers are divided into four memory banks. Two bits of status register will perform bank selection. Most commonly used SFRs will have the same address in all the four banks.

- **GENERAL-PURPOSE REGISTERS-**General-purpose registers are used for storing temporary data and results created during operation.
- **SPECIAL FUNCTION REGISTERS (SFRS)-**Special-function registers are also RAM memory locations, but unlike general-purpose registers, their purpose is predetermined during manufacturing process and cannot be changed. Since their bits are connected to particular circuits on the chip (A/D converter, serial communication module, etc.), any change of their contents directly affects the operation of the microcontroller or some of its circuits. For example, the ADCON0 register controls the operation of A/D converter.

Addr.	Name	Addr.	Name	Addr.	Name	Addr.	Name
00h	INDF	80h	INDF	100h	INDF	180h	INDF
01h	TMR0	81h	OPTION_REG	101h	TMR0	181h	OPTION_REG
02h	PCL	82h	PCL	102h	PCL	182h	PCL
03h	STATUS	83h	STATUS	103h	STATUS	183h	STATUS
04h	FSR	84h	FSR	104h	FSR	184h	FSR
05h	PORTA	85h	TRISA	105h	WDTCON	185h	SRCON
06h	PORTB	86h	TRISB	106h	PORTB	186h	TRISB
07h	PORTC	87h	TRISC	107h	CM1CON0	187h	BAUDCTL
08h	PORTD	88h	TRISD	108h	CM2CON0	188h	ANSEL
09h	PORTE	89h	TRISE	109h	CM2CON1	189h	ANSELH
0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah	PCLATH
0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh	INTCON
0Ch	PIR1	8Ch	PIE1	10Ch	EEDAT	18Ch	EECON1
0Dh	PIR2	8Dh	PIE2	10Dh	EEADR	18Dh	EECON2
0Eh	TMR1L	8Eh	PCON	10Eh	EEDATH	18Eh	Not Used
0Fh	TMR1H	8Fh	OSCCON	10Fh	EEADRH	18Fh	Not Used
10h	T1CON	90h	OSCTUNE	110h	General Purpose Registers 96 bytes	190h	General Purpose Registers 96 bytes
11h	TMR2	91h	SSPCON2				
12h	T2CON	92h	PR2				
13h	SSPBUF	93h	SSPADD				
14h	SSPCON	94h	SSPSTAT				
15h	CCPR1L	95h	WPUB				
16h	CCPR1H	96h	IOCB				
17h	CCP1CON	97h	VRCON				
18h	RCSTA	98h	TXSTA				
19h	TXREG	99h	SPBRG				
1Ah	RCREG	9Ah	SPBRGH				
1Bh	CCPR2L	9Bh	PWM1CON				
1Ch	CCPR2H	9Ch	ECCPAS				
1Dh	CCP2CON	9Dh	PSTRCON				
1Eh	ADRESH	9Eh	ADRESL				
1Fh	ADCON0	9Fh	ADCON1				
20h	General Purpose Registers 96 bytes	A0h	General Purpose Registers 80 bytes				
7Fh		FFh		17Fh		1EFh	
	Bank 0		**Bank 1**		**Bank 2**		**Bank 3**

Figure 7. Four Memory Banks of RAM

4.3.1.4 STACK

A part of RAM used as stack consists of eight 13-bit registers. Before the microcontroller starts to execute a subroutine (CALL instruction) or when an interrupt occurs, the address of the first next instruction to execute is pushed onto the stack, i.e. one of its registers. Data is always circularly pushed onto the stack. It means that after the stack has been pushed eight times, the ninth push overwrites the value that was stored with the first push.

4.3.2 INPUT/OUTPUT PORTS

In order to synchronize the operation of I/O ports with the internal 8-bit organization of the microcontroller, they are, similar to registers, grouped into five ports denoted by A, B, C, D and E. All of them have several features in common.

- For practical reasons, many I/O pins are multifunctional. If a pin performs any of these functions, it may not be used as a general-purpose input/output pin.
- Every port has its 'satellite', i.e. the corresponding TRIS register: TRISA, TRISB, TRISC etc. which determines the performance of port bits, but not their contents.

By clearing any bit of the TRIS register (bit=0), the corresponding port pin is configured as an output. Similarly, by setting any bit of the TRIS register (bit=1), the corresponding port pin is configured as an input. 0 = Output, 1 = Input.

4.3.2.1 PORT A and TRIS A registers

Port A is an 8-bit wide, bidirectional port. Bits of the TRIS A and ANSEL registers control the Port A pins. All Port A pins act as digital inputs/outputs. Five of them can also be analog inputs (denoted by AN).

	R/W (x)	R/W (x)	R/W (x)	R/W (x)	R/W (x)	R/W (x)	R/W (x)	R/W (x)	Features
PORTA	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Bit name
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	Features
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	Bit name
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

Legend

R/W	Readable/Writable bit
(x)	After reset, bit is unknown
(1)	After reset, bit is set

Figure 8. PORT A and TRIS A registers

RA0 = AN0 (determined by the ANS0 bit of the ANSEL register)
RA1 = AN1 (determined by the ANS1 bit of the ANSEL register)
RA2 = AN2 (determined by the ANS2 bit of the ANSEL register)
RA3 = AN3 (determined by the ANS3 bit of the ANSEL register)
RA5 = AN4 (determined by the ANS4 bit of the ANSEL register)

TRIS A register determine which of the pins are to be configured as inputs and which ones as outputs, the appropriate bits of the ANSEL register determine whether pins are to be configured as analog inputs or digital inputs/outputs.

4.3.2.2 PORT B and TRIS B registers

Port B is an 8-bit wide, bidirectional port. Bits of the TRISB register determine the function of its pins. Similar to port A, a logic one (1) in the TRISB register configures the appropriate port B pin as an input and vice versa. Six pins of this port can act as analog inputs (AN). The bits of the ANSELH register determine whether these pins are to be configured as analog inputs or digital inputs/outputs.

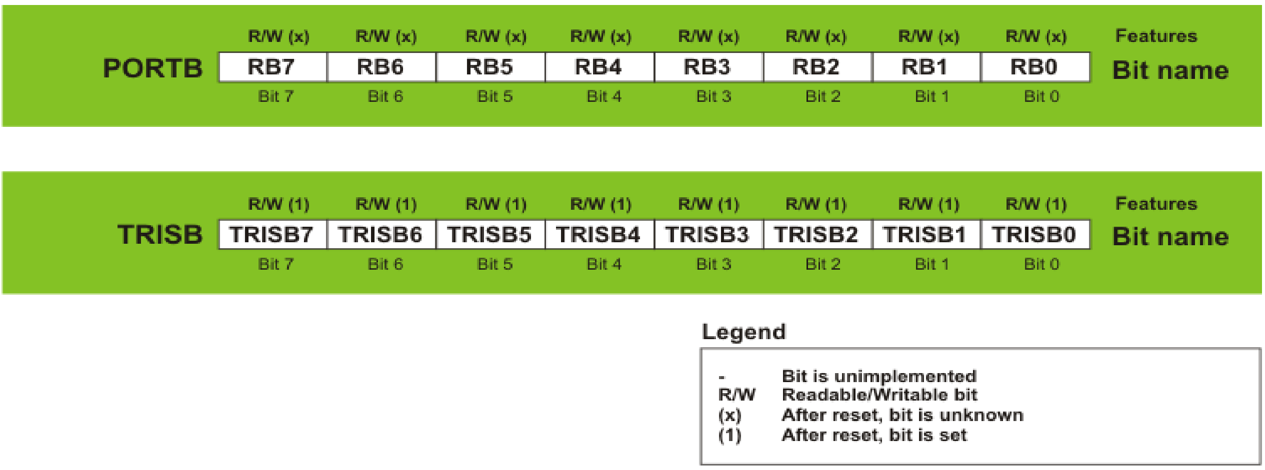

Figure 9. PORT B and TRIS B registers

RB0 = AN12 (determined by the ANS12 bit of the ANSELH register) The RB0/INT pin is the only ‘true’ external interrupt source. It can be configured to react to signal raising edge (zero-to-one transition) or signal falling edge (one-to-zero transition).

RB1 = AN8 (determined by the ANS8 bit of the ANSELH register)

RB2 = AN8 (determined by the ANS8 bit of the ANSELH register)

RB3 = AN9 (determined by the ANS9 bit of the ANSELH register)

RB4 = AN11 (determined by the ANS11 bit of the ANSELH register)

RB5 = AN13 (determined by the ANS13 bit of the ANSELH register)

This port has several features which distinguish it from other ports and make its pins commonly used

- All the port B pins have built in pull-up resistors, which make them ideal for connection to push buttons (keyboard), switches and opto-couplers. In order to connect these resistors to the microcontroller ports, the appropriate bit of the WPUB register should be set.
- If enabled, each port B bit configured as an input may cause an interrupt by changing its logic state. In order to enable pins to cause an interrupt, the appropriate bit of the IOCB register should be set.

The PIC16F887 does not have any special pins for programming (the process of writing a program to ROM). Port pins, normally available as general-purpose I/O pins, are used for this purpose. To be more precise, it is about port B pins used for clock (RB6) and data transfer (RB7) during program loading.

4.3.2.3 PORT C and TRIS C registers

Port C is an 8-bit wide bidirectional port. Bits of the TRIS C register determine the function of its pins. Similar to other ports, a logic one (1) in the TRIS C register configures the appropriate po,rt C pin as an input.

	R/W (x)	R/W (x)	R/W (x)	R/W (x)	R/W (x)	R/W (x)	R/W (x)	R/W (x)	Features
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	Bit name
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	Features
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	Bit name
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

Legend

R/W	Readable/Writable bit
(x)	After reset, bit is unknown
(1)	After reset, bit is set

Figure 10. PORT C and TRIS C registers

4.3.2.4 PORT D and TRIS D registers

Port D is an 8-bit wide, bidirectional port. Bits of the TRIS D register determine the function of its pins. A logic one (1) in the TRIS D register configures the appropriate port D pin as an input.

	R/W (x)	R/W (x)	R/W (x)	R/W (x)	R/W (x)	R/W (x)	R/W (x)	R/W (x)	Features
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	Bit name
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	R/W (1)	Features
TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	Bit name
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

Legend

R/W	Readable/Writable bit
(x)	After reset, bit is unknown
(1)	After reset, bit is set

Figure 11. PORT D and TRIS D registers

4.3.2.5 PORT E and TRIS E registers

Port E is a 4-bit wide, bidirectional port. The TRIS E register's bits determine the function of its pins. Similar to other ports, a logic one (1) in the TRIS E register configures the appropriate port E pin as an input.

The exception is the RE3 pin which is always configured as an input.

PORTE									
					R/W (x)	R/W (x)	R/W (x)	R/W (x)	Features
PORTE	-	-	-	-	RE3	RE2	RE1	RE0	Bit name
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

TRISE									
					R (1)	R/W (1)	R/W (1)	R/W (1)	Features
TRISE	-	-	-	-	TRISE3	TRISE2	TRISE1	TRISE0	Bit name
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	

Legend

-	Bit is unimplemented
R/W	Readable/Writable bit
R	Readable bit
(x)	After reset, bit is unknown
(1)	After reset, bit is set

Figure 12. PORT E and TRIS E registers

Similar to ports A and B, three pins can be configured as analog inputs in this case. The ANSELH register bits determine whether a pin will act as an analog input (AN) or digital input/output.

RE0 = AN5 (determined by the ANS5 bit of the ANSEL register) RE1 = AN6 (determined by the ANS6 bit of the ANSEL register) and RE2 = AN7 (determined by the ANS7 bit of the ANSEL register).

4.3.2.6. ANSEL and ANSELH register

The ANSEL and ANSELH registers are used to configure the input mode of an I/O pin to analog or digital.

To configure a pin as an analog input, the appropriate bit of the ANSEL or ANSELH registers must be set (1). To configure a pin as a digital input/output, the appropriate bit must be cleared (0).The state of the ANSEL bits has no influence on digital output functions. The result of any attempt to read a port pin configured as an analog input will be 0

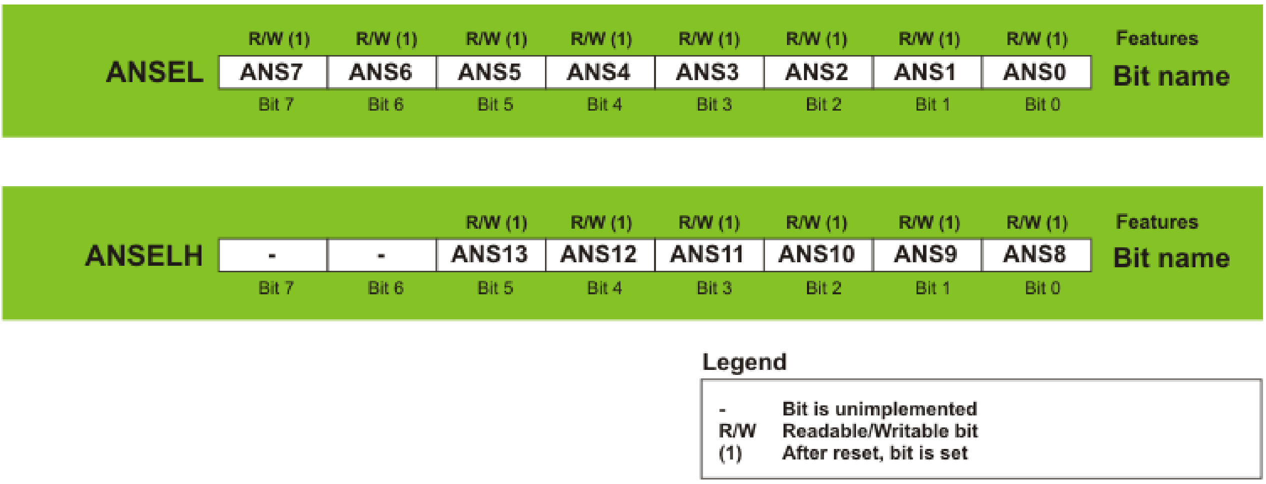

Figure 13. ANSEL and ANSELH registers

4.3.3 TIMERS

The PIC 16F887 basically has three timer modules. These timer modules are usually denoted by the symbols TIMER-0, TIMER-1, and TIMER-2.These modules help to perform various timing and counting functions inside the chip.

4.3.3.1 TIMER TMR0

The timer TMR0 has a wide range of application in practice. The timer TMR0 module is an 8-bit timer/counter with the following features:

- 8-bit prescalar(shared with Watchdog timer)
- Programmable internal or external clock source;
- Interrupt on overflow; and
- Programmable external clock edge selection.

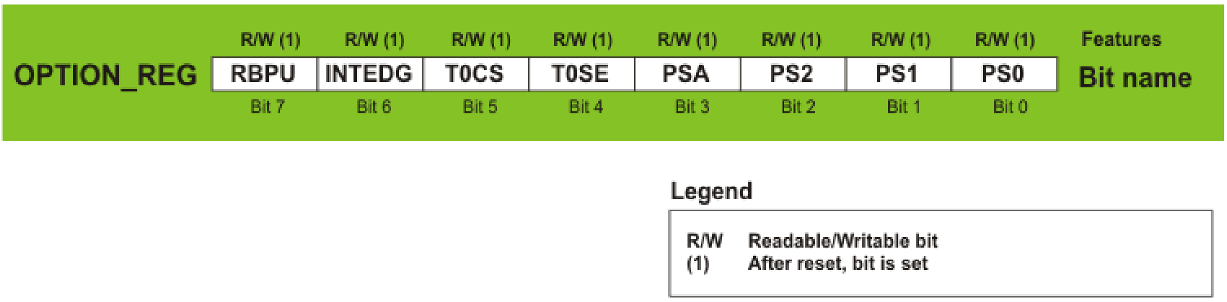

Figure 14. Option register

The operation of TMR0 depends on the bits stored in the Option register.

- **RBPU - PORTB Pull-up enable bit**
  - 0 - PORTB pull-up resistors are disabled.
  - 1 - PORTB pins can be connected to pull-up resistors.
- **INTEDG - Interrupt Edge Select bit**
  - 0 - Interrupt on rising edge of the INT pin (0-1).
  - 1 - Interrupt on falling edge of the INT pin (1-0).
- **T0CS - TMR0 Clock Select bit**
  - 0 - Pulses are brought to TMR0 timer/counter input through the RA4 pin.
  - 1 - Timer uses internal cycle clock.
- **T0SE - TMR0 Source Edge Select bit**
  - 0 - Increment on high-to-low transition on the TMR0 pin.
  - 1 - Increment on low-to-high transition on the TMR0 pin.
- **PSA - Prescaler Assignment bit**
  - 0 - Prescaler is assigned to the WDT.
  - 1 - Prescaler is assigned to the TMR0 timer/counter.
- **PS2, PS1, PS0 - Prescaler Rate Select bit**
    - Prescaler rate is adjusted by combining these bits.

PS2	PS1	PS0	TMR0	WDT
0	0	0	1:2	1:1
0	0	1	1:4	1:2
0	1	0	1:8	1:4
0	1	1	1:16	1:8
1	0	0	1:32	1:16
1	0	1	1:64	1:32

1	1	0	1:128	1:64
1	1	1	1:256	1:128

Table 1. Different PSR for timer/counter and watchdog timer

Step 1: To select mode:

- Timer mode is selected by the T0CS bit of the OPTION_REG register, (T0CS: 0=timer, 1=counter).
- When used, the prescaler should be assigned to the timer/counter by clearing the PSA bit of the OPTION_REG register. The prescaler rate is set by using the PS2-PS0 bits of the same register.
- When using interrupt, the GIE and TMR0IE bits of the INTCON register should be set.

Step 2: Measuring and Counting

To measure time:

- Reset the TMR0 register or write some known value to it.
- Elapsed time (in microseconds when using 4MHz quartz) is measured by reading the TMR0 register.
- The flag bit TMR0IF of the INTCON register is automatically set every time the TMR0 register overflows. If enabled, an interrupt occurs.

To count pulses:

- The polarity of pulses are to be counted on the RA4 pin is selected by the TOSE bit of the OPTION_REG register (T0SE: 0=positive, 1=negative pulses).
- Number of pulses may be read from the TMR0 register. The prescaler and interrupt are used in the same manner as in timer mode.

4.3.3.2 TIMER TMR1

Timer TMR1 module is a 16-bit timer/counter, which means that it consists of two registers (TMR1L and TMR1H). It can count up 65.535 pulses in a single cycle, i.e. before the counting starts from zero.

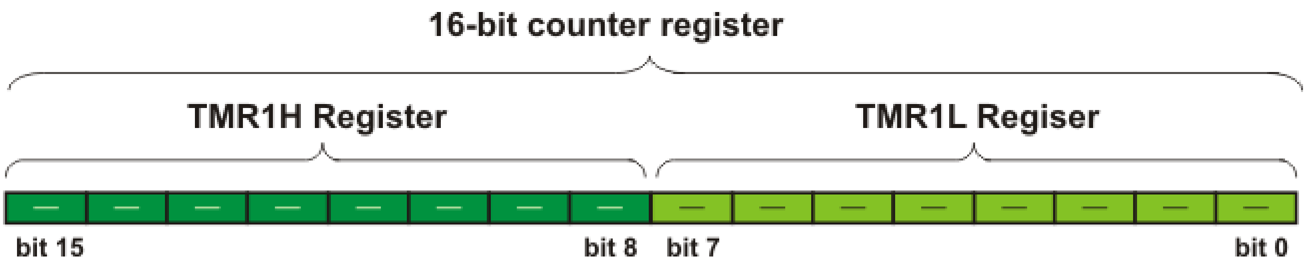

Figure 15. TMR1 16 bit register

The TMR1 timer has following features:

- 16-bit timer/counter register pair;
- Programmable internal or external clock source;
- 3-bit prescaler;
- Optional LP oscillator;
- Synchronous or asynchronous operation;
- Timer TMR1 gate control (count enable) via comparator or T1G pin;
- Interrupt on overflow;
- Wake-up on overflow (external clock); and
- Time base for Capture/Compare function.

T1CON Register

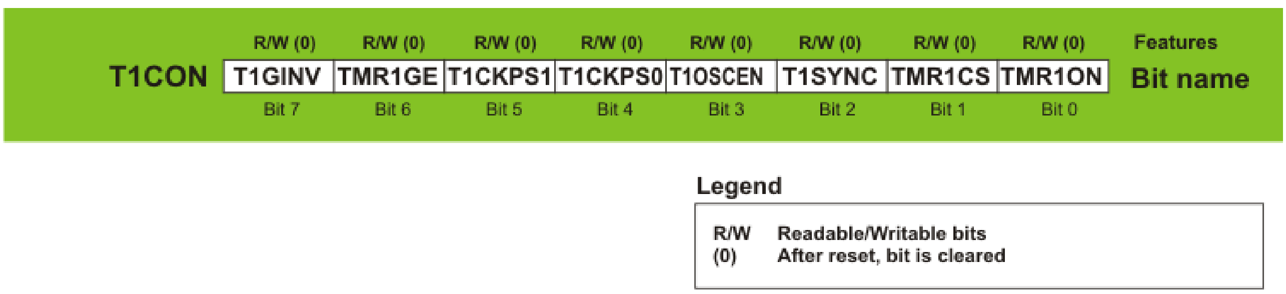

Figure 16. T1CON register

T1GINV - Timer1 Gate Invert bit acts as logic state inverter on the T1G pin gate or the comparator C2 output (C2OUT) gate. It enables the timer to mea sure time whilst the gate is high or low.

- 1 - Timer 1 counts when the T1G pin or bit C2OUT gate is high (1).

- 0 - Timer 1 counts when the T1G pin or bit C2OUT gate is low (0).

TMR1GE - Timer1 Gate Enable bit determines whether the T1G pin or comparator C2 output (C2OUT) gate will be active or not. This bit is functional only in the event that the timer TMR1 is on (bit TMR1ON = 1). Otherwise, this bit is ignored.

- 1 - Timer TMR1 is on only if Timer1 gate is not active.
- 0 - Gate has no influence on the timer TMR1.

T1CKPS1, T1CKPS0 - Determine the rate of the prescaler assigned to the timer TMR1.

T1CKPS1	T1CKPS0	PRESCALER RATE
0	0	1:1
0	1	1:2
1	0	1:4
1	1	1:8

Table 2. Different prescalar rates assigned to TMR1

T1OSCEN - LP Oscillator Enable Control bit

- 1 - LP oscillator is enabled for timer TMR1 clock (oscillator with low power consumption and frequency 32.768 kHz).
- 0 - LP oscillator is off.

T1SYNC - Timer1 External Clock Input Synchronization Control bit enables synchronization of the LP oscillator input or T1CKI pin input with the microcontroller internal clock. This bit is ignored while counting pulses from the main oscillator (bit TMR1CS = 0).

- 1 - Do not synchronize external clock input.
- 0 - Synchronize external clock input.

TMR1CS - Timer TMR1 Clock Source Select bit

- 1 - Count pulses on the T1CKI pin (on the rising edge 0-1).
- 0 - Count pulses of the microcontroller internal clock.

TMR1ON - Timer1 On bit

- 1 - Enable timer TMR1.
- 0 - Stop timer TMR1.

The timer TMR1 module may operate in one of two basic modes, that is as a timer or a counter.

- **TMR1 IN TIMER MODE-**In order to select this mode, it is necessary to clear the TMR1CS bit. After this, the 16-bit register will be incremented on every pulse generated by the internal oscillator.In this mode, the T1SYNC bit does not affect the timer because it counts internal clock pulses. Since the whole electronics uses these pulses, there is no need for synchronization.

- **TMR1 IN COUNTER MODE-**Timer TMR1 starts to operate as a counter by setting the TMR1CS bit. It counts pulses brought to the PC0/T1CKI pin and is incremented on the rising edge of the external clock input T1CKI. If the control bit T1SYNC of the T1CON register is cleared, the external clock inputs will be synchronized on their way to the TMR1 register. In other words, the timer TMR1 is synchronized to the microcontroller system clock and is called a synchronous counter.

4.3.3.3 TIMER TMR2

Timer TMR2 module is an 8-bit timer which operates in a very specific way. The timer TMR2 is controlled by several bits of the T2CON register.

T2CON Register

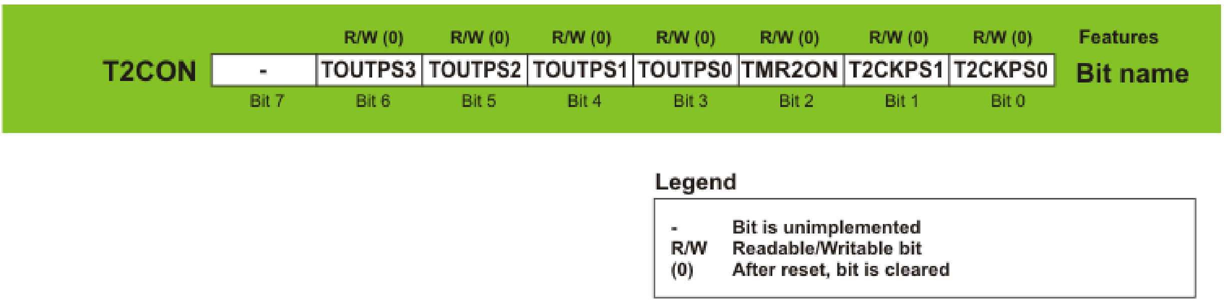

Figure 17. T2CON register

TMR2ON - Timer2 On bit turns the timer TMR2 on.

- 1 - Timer TMR2 is on.
- 0 - Timer TMR2 is off.

T2CKPS1, T2CKPS0 - Timer2 Clock Prescale bits determine the prescaler rate.

TOUTPS3 - TOUTPS0 - Timer2 Output Postcaler Select bits are used to determine the postscaler rate.

4.3.4 SERIAL COMMUNICATION MODULES

The microcontroller provides serial communication using either the EUSART or MSSP modules.

4.3.4.1 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER(EUSART)

This module is a serial I/O communication peripheral unit. It is also known as Serial Communications Interface (SCI). It contains all clock generators, shift registers and data buffers necessary to perform an input/output serial data transfer independently of the device program execution. As its name states, apart from using the clock for synchronization, this module can also establish asynchronous connection, which makes it unique for some of the applications. The EUSART system integrated into the PIC16F887 microcontroller has the following features:

- Full-duplex asynchronous transmit and receive

- Programmable 8- or 9-bit wide characters
- Address detection in 9-bit mode
- Input buffer overrun error detection and
- Half-duplex communication in synchronous mode.

TXSTA Register

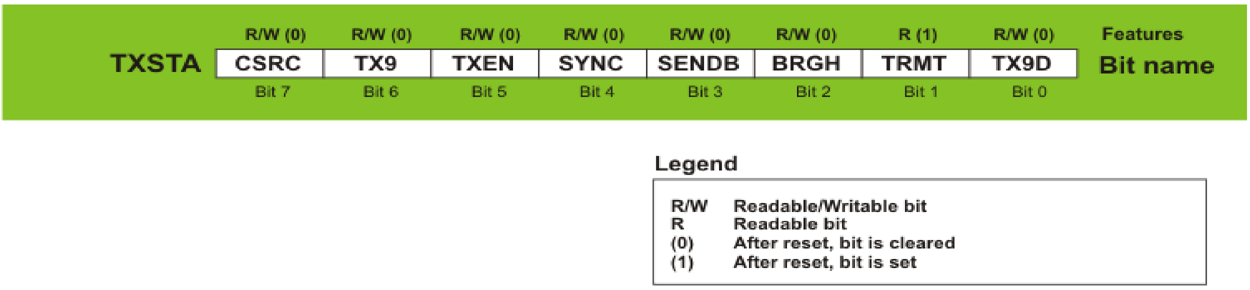

Figure 18. TXSTA register

CSRC - Clock Source Select bit - determines clock source. It is used only in synchronous mode.

- 1 - Master mode. Clock is generated internally from Baud Rate Generator.
- 0 - Slave mode. Clock is generated from external source.

TX9 - 9-bit Transmit Enable bit-determines if there is a 9 bit transmission.

- 1 - 9-bit data transmission via EUSART system.
- 0 - 8-bit data transmission via EUSART system.

TXEN - Transmit Enable bit

- 1 - Transmission enabled.
- 0 - Transmission disabled.

SYNC - EUSART Mode Select bit

- 1 - EUSART operates in synchronous mode.
- 0 - EUSART operates in asynchronous mode.

SENDB - Send Break Character bit is only used in asynchronous mode and when it is required to observe LIN bus standard.

- 1 - Break character transmission is enabled.

- 0 - Break character transmission is completed.

BRGH - High Baud Rate Select bit determines baud rate in asynchronous mode. It does not affect EUSART in synchronous mode.

- 1 - EUSART operates at high speed.
- 0 - EUSART operates at low speed.

TRMT - Transmit Shift Register Status bit

- 1 - TSR register is empty.
- 0 - TSR register is full.

TX9D - Ninth bit of Transmit Data can be used as address or parity bit.

In order to enable data transmission via EUSART module, it is necessary to configure it to operate as a transmitter. In other words, it is necessary to define the state of the following bits:

- **TXEN = 1** - EUSART transmitter is enabled by setting the TXEN bit of the TXSTA register.
- **SYNC = 0** - EUSART is configured to operate in asynchronous mode by clearing the SYNC bit of the TXSTA register
- .**SPEN = 1** - By setting the SPEN bit of the RCSTA register, EUSART is enabled and the TX/CK pin is automatically configured as an output.

RCSTA Register

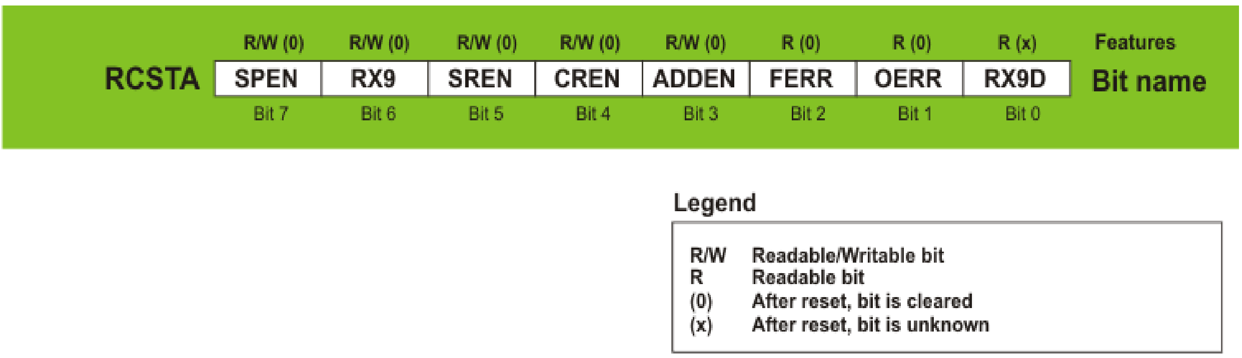

Figure 19. RCSTA register

SPEN - Serial Port Enable bit

- 1 - Serial port enabled. RX/DT and TX/CK pins are automatically configured as input and output, respectively.
- 0 - Serial port disabled.

RX9 - 9-bit Receive Enable bit

- 1 - Reception of 9-bit data via EUSART system.
- 0 - Reception of 8-bit data via EUSART system.

SREN - Single Receive Enable bit is used only in synchronous mode when the microcontroller operates as master.

- 1 - Single receive enabled.
- 0 - Single receive disabled.

CREN - Continuous Receive Enable bit acts differently depending on EUSART mode.

Asynchronous mode:

- 1 - Receiver enabled.
- 0 - Receiver disabled.

Synchronous mode:

- 1 - Enables continuous receive until the CREN bit is cleared.
- 0 - Disables continuous receive.

ADDEN - Address Detect Enable bit is only used in address detect mode.

- 1 - Enables address detection on 9-bit data receive.
- 0 - Disables address detection. The ninth bit can be used as parity bit.

FERR - Framing Error bit

- 1 - On receive, Framing Error is detected.
- 0 - No framing error.

OERR - Overrun Error bit.

- 1 - On receive, Overrun Error is detected.

- 0 - No overrun error.

RX9D - Ninth bit of Received Data can be used as address or parity bit.

EUSART BAUD RATE GENERATOR

The BRG timer consists of two 8-bit registers making one 16-bit register.

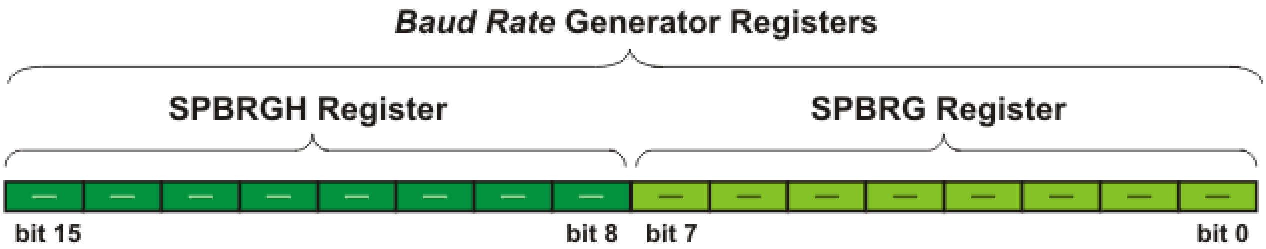

Figure 20. Baud rate generator

4.3.4.2 MASTER SYNCHRONOUS SERIAL PORT(MSSP)

The main feature of this type of communication is that it is synchronous and suitable for use in systems with a single master and one or more slaves. A master device contains a circuit for baud rate generation and supplies all devices in the system with the clock. Slave devices may in this way eliminate the internal clock generation circuit. The MSSP module can operate in one out of two modes:

- SPI mode (Serial Peripheral Interface); and
- I^2C mode (Inter-Integrated Circuit).

4.3.4.2.1 SERIAL PERIPHERAL INTERFACE MODE

The module starts to operate by setting the SSPEN bit

First Step - Data to be transmitted should be written to the buffer register SSPBUF. If the SPI module operates in master mode, the microcontroller will automatically perform the following steps 2, 3 and 4. If the SPI module operates as Slave, the microcontroller will not perform these steps until the SCK pin detects clock signal.

Second Step - The data is now moved to the SSPSR register and the SSPBUF register is not cleared.

Third Step - This data is then shifted to the output pin (MSB bit first) while the register is simultaneously being filled with bits through the input pin. In Master mode, the microcontroller itself generates clock, while the Slave mode uses external clock (the SCK pin).

Fourth Step- The SSPSR register is full once 8 bits of data have been received. It is indicated by setting the BF bit of the SSPSTAT register and the SSPIF bit of the PIR1 register. The received data (one byte) is automatically moved from the SSPSR register to the SSPBUF register. Since serial data transmission is performed automatically, the rest of the program is normally executed while the data transmission is in progress. In this case, the function of the SSPIF bit is to generate an interrupt when one byte transmission is completed.

Fifth Step - Finally, the data stored in the SSPBUF register is ready for use and should be moved to a desired register.

4.3.4.2 I^{2}C MODE

I^{2}C mode (Inter IC Bus) is especially suitable when the microcontroller and an integrated circuit, which the microcontroller should exchange data with, are within the same device. Similar to serial communication in SPI mode, data transfer in I^{2}C mode is synchronous and bidirectional. This time only two pins are used for data transmission. These are the SDA (Serial Data) and SCL (Serial Clock) pins. The user must configure these pins as inputs or outputs through the TRISC bits.

By observing particular rules (protocols), this mode enables up to 122 different components to be simultaneously connected in a simple way by using only two valuable I/O pins.

Clock, necessary to synchronize the operation of both devices, is always generated by a master device (a microcontroller) and its frequency directly affects the baud rate.

When master and slave components are synchronized by the clock, every data exchange is always initiated by the master. Once the MSSP module has been enabled, it waits for a Start condition to occur. The master device first sends the START bit (logic zero) through the SDA pin, then a 7-bit address of the selected slave device, and finally, the bit which requires data write (0) or read (1) to the device. In other words, the eight bits are shifted to the SSPSR register following the start condition. All slave devices sharing the same transmission line will simultaneously receive the first byte, but only one of them has the address to match and receives the whole data .Once the first byte has been sent (only 8-bit data are transmitted), master goes into receive mode and waits for acknowledgment from the receive device that address match has occurred. If the slave device sends acknowledge data bit (1), data transfer will be continued until the master device (microcontroller) sends the Stop bit.

4.3.5. RESET

Reset condition causes the microcontroller to immediately stop operation and clear its registers. A reset signal may be generated externally at any moment (low logic level on the MCLR pin). If needed, it can also be generated by internal control logic. Power-on always causes reset. Since there are many transitional events taking place when power supply is turned on (switch contact flashing and sparkling, slow voltage rise, gradual clock frequency stabilization etc.), it is necessary to provide a certain time delay for the microcontroller before it starts to operate.

CHAPTER-5

SENSORS

5.1 ULTRASONIC SENSOR MODULE -HC - SR04

Ultrasonic ranging module HC - SR04 provides 2cm - 400cm non-contact measurement function, the ranging accuracy can reach to 3mm. The modules includes ultrasonic transmitters, receiver and control circuit.

5.1.1 WORKING PRINCIPLE

1. Using IO trigger for at least 8us high level signal
2. The Module automatically sends eight 40 kHz and detect whether there is a pulse signal back.
3. The Module automatically sends eight 40 kHz and detect whether there is a pulse signal back.

5.1.2 FORMULA

Test distance = (high level time × velocity of sound (340m/s) / 2

5.1.3 PARAMETERS

Working Voltage	DC 5 V
Working Current	15mA
Working Frequency	40Hz
Max Range	4m
Min Range	2cm
MeasuringAngle	15 degree
Trigger Input Signal	10uS TTL pulse
Echo Output Signal	Input TTL lever signal and the range in proportion
Dimension	45*20*15mm

Table 3. Parameters of Ultrasonic Sensor

Figure 21. Ultrasonic Sensor

5.1.4 TIMING DIAGRAM

The Timing diagram is shown below. You only need to supply a short 8uS pulse to the trigger input to start the ranging, and then the module will send out an 8 cycle burst of ultrasound at 40 kHz and raise its echo. The Echo is a distance object that is pulse width and the range in proportion .You can calculate the range through the time interval between sending trigger signal and receiving echo signal. Formula: uS / 58 = centimeters or uS / 148 =inch; or: the range = high level time * velocity (340M/S) / 2; we suggest to use over 60ms measurement cycle, in order to prevent trigger signal to the echo signal.

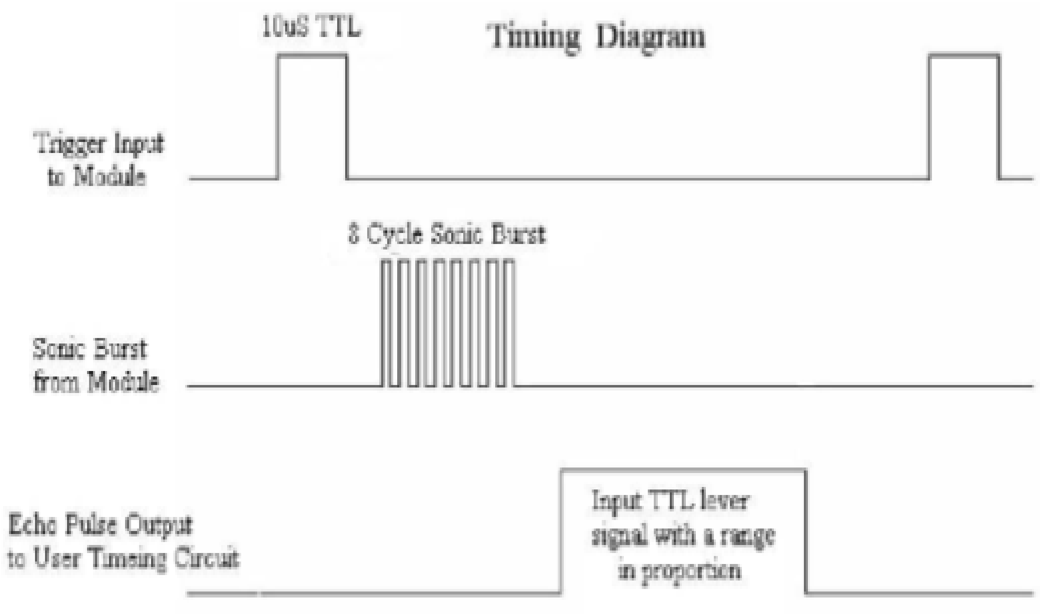

Figure 22. Timing Diagram

5.2 IR SENSOR MODULE-LM358

5.2.1 DESCRIPTION

The LM358 series consists of two independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM358 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

5.2.2 UNIQUE CHARACTERISTICS

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated.

5.2.3 FEATURES

1. Available in 8-Bump micro SMD chip sized package, (See AN-1112)
2. Internally frequency compensated for unity gain
3. Large dc voltage gain: 80 dB
4. Wide bandwidth (unity gain): 1 MHz (temperature compensated)
5. Wide power supply range: — Single supply: 3V to 32V — or dual supplies: ±1.5V to ±16V
6. Very low supply current drain (500 μA)—essentially independent of supply voltage
7. Low input offset voltage: 2 mV
8. Input common-mode voltage range includes ground
9. Differential input voltage range equal to the power supply voltage
10. Large output voltage swing

Figure 23. IR Sensor Module

5.2.5 ELECTRICAL CHARACTERSTICS

$V^+ = +5.0V$, (Note 4), unless otherwise stated

Parameter		Conditions	LM158A			LM358A			LM158/LM258			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Large Signal Voltage Gain		$V^+ = 15V$, $T_A = 25°C$, $R_L \geq 2\ k\Omega$, (For $V_O = 1V$ to $11V$)	50	100		25	100		50	100		V/mV
Common-Mode Rejection Ratio		$T_A = 25°C$, $V_{CM} = 0V$ to $V^+ - 1.5V$	70	85		65	85		70	85		dB
Power Supply Rejection Ratio		$V^+ = 5V$ to $30V$ (LM2904, $V^+ = 5V$ to $26V$), $T_A = 25°C$	65	100		65	100		65	100		dB
Amplifier-to-Amplifier Coupling		f = 1 kHz to 20 kHz, $T_A = 25°C$ (Input Referred), (Note 8)		−120			−120			−120		dB
Output Current	Source	$V_{IN}^+ = 1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$	20	40		20	40		20	40		mA
	Sink	$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$ $V^+ = 15V$, $T_A = 25°C$, $V_O = 2V$	10	20		10	20		10	20		mA
		$V_{IN}^- = 1V$, $V_{IN}^+ = 0V$ $T_A = 25°C$, $V_O = 200\ mV$, $V^+ = 15V$	12	50		12	50		12	50		μA
Short Circuit to Ground		$T_A = 25°C$, (Note 2), $V^+ = 15V$		40	60		40	60		40	60	mA
Input Offset Voltage		(Note 5)			4			5			7	mV
Input Offset Voltage Drift		$R_S = 0\Omega$		7	15		7	20		7		μV/°C
Input Offset Current		$I_{IN(+)} - I_{IN(-)}$			30			75			100	nA
Input Offset Current Drift		$R_S = 0\Omega$		10	200		10	300		10		pA/°C
Input Bias Current		$I_{IN(+)}$ or $I_{IN(-)}$		40	100		40	200		40	300	nA
Input Common-Mode Voltage Range		$V^+ = 30\ V$, (Note 7) (LM2904, $V^+ = 26V$)	0		V^+-2	0		V^+-2	0		V^+-2	V

Table 4. Electrical Characteristics of LM358

5.2.4 ADVANTAGES

1. Two internally compensated op amps n Eliminates need for dual supplies
2. Allows direct sensing near GND and VOUT also goes to GND
3. Compatible with all forms of logic n Power drain suitable for battery operation

CHAPTER 6

GPS

The Global Positioning System receiver receives antenna signals from the space segment (i.e.) Satellites. There are a number of receiver modules and these are cable of receiving signals from different number of satellites.

6.1 GPS MODULE-SKG13C

The SKG13C is a complete GPS engine module that features super sensitivity, ultra low power and small form factor. The GPS signal is applied to the antenna input of module, and a complete serial data message with position, velocity and time information is presented at the serial interface with NMEA protocol or custom protocol. It is based on the high performance features of the MediaTek MT3339 single-chip architecture, Its –165dBm tracking sensitivity extends positioning coverage into place like urban canyons and dense foliage environment where the GPS was not possible before. The small form factor and low power consumption make the module easy to integrate into portable device like PNDs, mobile phones, cameras and vehicle navigation systems.

Figure 24. SKG 13C

6.2 FEATURES

1. Ultra high sensitivity:-165dBm
2. Extremely fast TTFF at low signal level
3. Built-in 12 multi-tone active interference canceller
4. Low power consumption: Typical 18mA@3.3V
5. ±8ns high accuracy time pulse (1PPS)
6. Advanced Features: AlwaysLocate; AIC; EPO;EASY
7. QZSS,SBAS(WAAS,EGNOS,MSAS,GAGAN)
8. Indoor and outdoor multi-path detection and compensation
9. Small form factor: 15x13x2.2mm

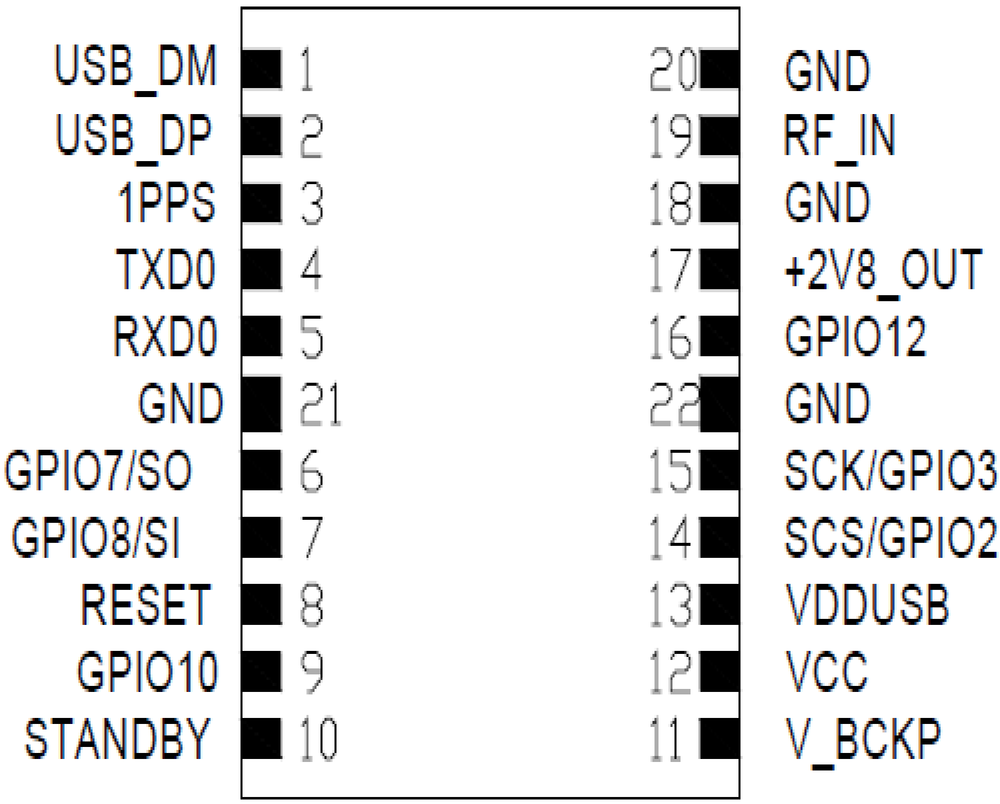

Figure 25. PIN diagram

Pin No.	Pin name	I/O	Description	Remark
1	RXD1	O	UART Serial Data Input 1	Leave open if not used
2	TXD1	I	UART Serial Data Output 1	Leave open if not used
3	PPS	O	Time pulse Signal	Leave open if not used
4	TXD0	O	UART Serial Data Output 0	Leave open if not used
5	RXD0	I	UART Serial Data Input 0	Leave open if not used
6	NC			
7	FIXLED	O	Fixed LED Output	Leave open if not used
8	RESET	I	Module Reset (Active Low Status)	Leave open if not used
9	32K CLK_OUT	O	32.768KHz clock output from RTC	Leave open if not used
10	GPIO13/EINT1	I	Wakeup signal input from such a G sensor	Currently version do not support
11	V_BCKP	I	RTC and backup SRAM power (2.0-4.2V)	May be connect to Battery
12	VCC	I	Module Power Supply	Operating range: 3.0V to 4.2V
13	NC			
14	GPIO14	I/O	General Purpose I/O	Leave open if not used
15	GPIO15	I/O	General Purpose I/O	Leave open if not used
16	NC			
17	VCC_OUT	O	VCC power output	Leave open if not used
18	GND	G	Ground	
19	RF_IN	I	GPS Signal Input	50Ω@1.57542GHz
20	GND	G	Ground	
21	GND	G	Ground	
22	GND	G	Ground	

Table 5. PIN Description

6.3 ANTENNA

The SKG13C GPS receiver is designed for supporting the active antenna or passive antenna connected with pin RF_IN. The gain of active antenna should be no more than 25dB (18~20dB Typical). The maximum noise figure should be no more than 1.5dB and output impedance is at 50 Ohm.

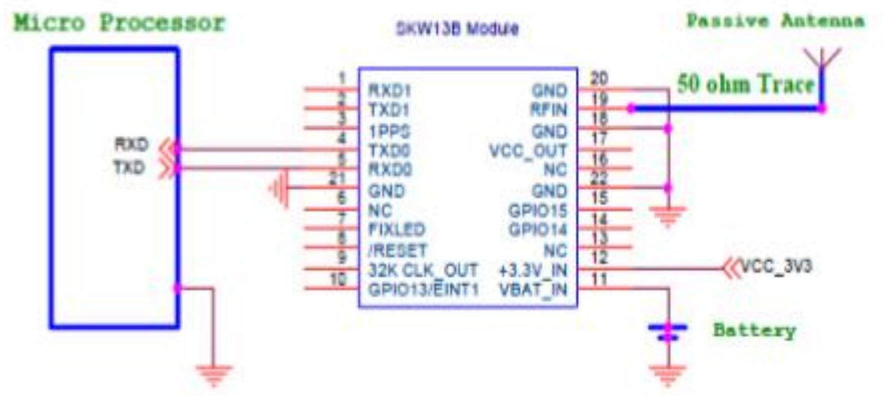

Figure 26. SKG13C application circuit that use passive antenna

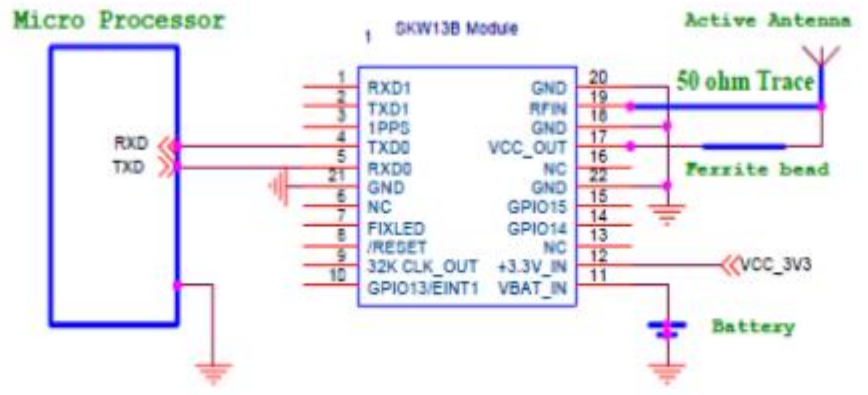

Figure 27. SKG13C application circuit that use active antenna

6.4 ADVANCED SOFTWARE FEATURES

6.4.1 STANDBY MODE

User can issue software command to make GPS module go into standby mode that consumes less than 200uA current. GPS module will be awaked when receiving any byte. The following flow chart is an example to make GPS module go into standby mode and then wake up.

6.4.2 PERIODIC MODE

When GPS module is commanded to periodic mode, it will be in operation and standby periodically. Its status of power consumption is as below chart

6.4.3 ALWAYSLOCATE™

AlwaysLocateTM is an intelligent controller of periodic mode. Depending on the environment and motion conditions, GPS module can adaptively adjust working/standby time to achieve balance of positioning accuracy and power consumption. In this mode, the host CPU does not need to control GPS module until the host CPU needs the GPS position data. The following flow chart is an example to make GPS module go into Always Locate Tm mode and then back to normal operation mode.

6.4.4 AGPS SUPPORT FOR FAST TTFF (EPO™)

The AGPS (EPO™) supply the predicated Extended Prediction Orbit data to speed TTFF ,users can download the EPO data to GPS engine from the FTP server by internet or wireless network ,the GPS engine will use the EPO data to assist position calculation when the navigation information of satellites are not enough or weak signal zone **.**

6.4.5 EASY™

The EASY™ is embedded assist system for quick positioning, the GPS engine will calculate and predict automatically the single emperies (Max. up to 3 days)when power on ,and save the predict information into the memory , GPS engine will use these information for positioning if no enough information from satellites , so the function will be helpful for positioning and TTFF improvement under indoor or urban condition ,the Backup power (VBACKUP) is necessary .

6.4.6 PERFORMANCE SPECIFICATION AND ELECTRICAL CHARACTERISTICS

Parameter	Specification	
Receiver Type	L1 frequency band, C/A code, 22 Tracking / 66 Acquisition-Channel	
Sensitivity	Tracking Acquisition	-165dBm Typical -148dBm Typical
Accuracy	Position Velocity Timing (PPS)	3.0m CEP50 without SA(Typical Open Sky) 0.1m/s without SA 10ns RMS
Acquisition Time	Cold Start Warm Start Hot Start Re-Acquisition	23s(Typical Open Sky) 2-3s 1s <1s
Assisted GPS support	EPO	
Power Consumption	Tracking Acquisition	18mA @3.3V Typical 22mA @3.3V
Navigation Data Update Rate	Max 10Hz	Default 1Hz
Operational Limits	Altitude Velocity Acceleration	Max 18,000m Max 515m/s Less than 4g

Table 6. Performance Specification

Parameter	Symbol	Min	Max	Units
Power Supply				
Power Supply Volt.	VCC	-0.3	4.3	V
Input Pins				
Input voltage on any input connection	VIO	-0.3	3.6	V
Backup Battery	V_BCKP	-0.3	4.3	V
RF input power	RF_IN		10	dBm
Human Body Model ESD capability	RF_IN		2000	V
Machine Model ESD capability	RF_IN		100	V
Environment				
Storage Temperature	Tstg	-40	125	°C
Peak Reflow Soldering Temperature <10s	Tpeak		260	°C
Humidity			95	%

Table 7. Electrical Characteristics

6.4.7 SOFTWARE PROTOCOL

6.4.7.1 NMEA 0183 PROTOCOL

The NMEA protocol is an ASCII-based protocol, Records start with a $ and with carriage return/line feed. GPS specific messages all start with $GPxxx where xxx is a three-letter identifier of the message data that follows. NMEA messages have a checksum, which allows detection of corrupted data transfers.

The SkyNav SKG13C supports the following NMEA-0183 messages: GGA, GLL, GSA, GSV, RMC VTG, ZDA. The module default NMEA-0183 output is set up GGA、GSA、RMC、GSV and default baud rate is set up 4800bps.

NMEA Record	Description	Default
GGA	Global positioning system fixed data	Y
GLL	Geographic position—latitude/longitude	N
GSA	GNSS DOP and active satellites	Y
GSV	GNSS satellites in view	Y
RMC	Recommended minimum specific GNSS data	Y
VTG	Course over ground and ground speed	N
ZDA	Date and Time	N

Table 8 . NMEA Record

6.4.7.2 GGA-Global Positioning System Fixed Data

This sentence contains the position, time and quality of the navigation fix.

$GPGGA,021514.000,2232.1799,N,11401.1823,E,1,6,1.25,84.0,M,-2.2,M,,*74

Name	Example	Units	Description
Message ID	$GPGGA		GGA protocol header
UTC Position	021514.000		hhmmss.sss
Latitude	2232.1799		ddmm.mmmm
N/S indicator	N		N=north or S=south
Longitude	11401.1823		dddmm.mmmm
E/W Indicator	E		E=east or W=west
Position Fix Indicator	1		See Table 2-1
Satellites Used	6		Range 0 to 12
HDOP	1.25		Horizontal Dilution of Precision
MSL Altitude	84.0	meters	Altitude (referenced to the Ellipsoid)
AltUnit	M	meters	Altitude Unit
GeoSep	-2.2	meters	Geoidal Separation
GeoSepUnit	M	meters	Geoidal Separation Unit
Age of Diff.Corr.	<Null>	second	Null fields when it is not Used
Diff.Ref.Station ID	<Null>		Null fields when it is not Used
Checksum	*74		
EOL	<CR> <LF>		End of message termination

Table 9.GGA Data Format

CHAPTER-7

RADIO CHIP CC 2500

7.1 CC 2500 RF MODEM

CC2500 RF Modem is a transceiver module which provides easy to use RF communication at 2.4 Ghz. It can be used to transmit and receive data at multiple baud rates from any standard CMOS/TTL source. This module is a direct line in replacement for the serial communication and it requires no extra hardware and no extra coding to turn the wired communication into wireless one.

It works in Half Duplex mode i.e. it provides communication in both directions, but only one direction at same time (not simultaneously). This switching from receiver to transmitter mode is done automatically.

7.2 FEATURES OF CC 2500

- Supports Multiple Baud rates (4800/7600/17200/38400).
- Works on ISM band (2.4 GHz) which is reserved internationally so no need to apply for license.
- Supports multiple frequencies within the same band rate thus avoiding data collision.
- No complex wireless connection software or intimate knowledge of RF is required to connect your serial devices.
- Designed to be as easy to use as cables.
- No external Antenna required.
- Plug and play device.
- Works on 5-7v DC supply.
- Standard UART Interface.

7.3 RF PERFORMANCE

- High sensitivity (–84 dBm at 2.4 kBaud,1% packet error rate)
- Low current consumption (13.3 mA in RX,250 kBaud, input well above sensitivity limit)
- Programmable output power up to +1 dBm
- Excellent receiver selectivity and blocking performance
- Programmable data rate from 1.2 to 500 kBaud.

7.4 SPECIFICATION

Name	Min	Typical	Max	Units
Working Voltage	4.5	5	8	GHz
Frequency		2.4		Volts
Range	15	25	30	Meters

Table 10.Specifications of Radio chip

7.5 PIN CONFIGURATION

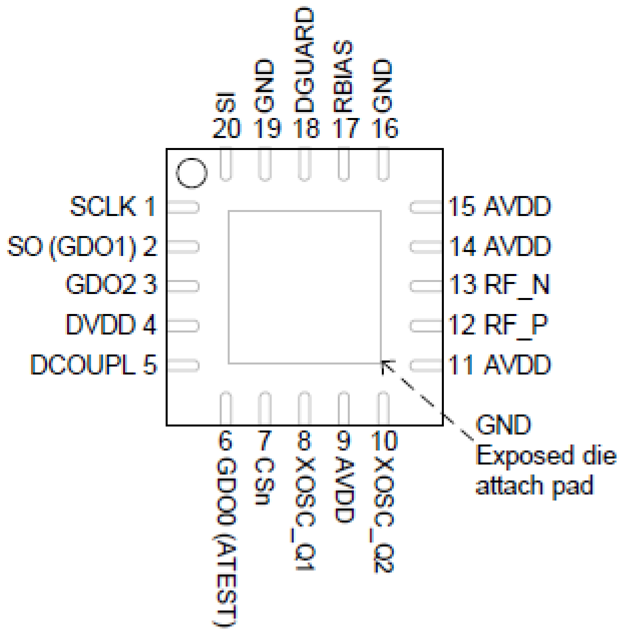

Figure 28. PIN configuration

7.6 CIRCUIT DESCRIPTION

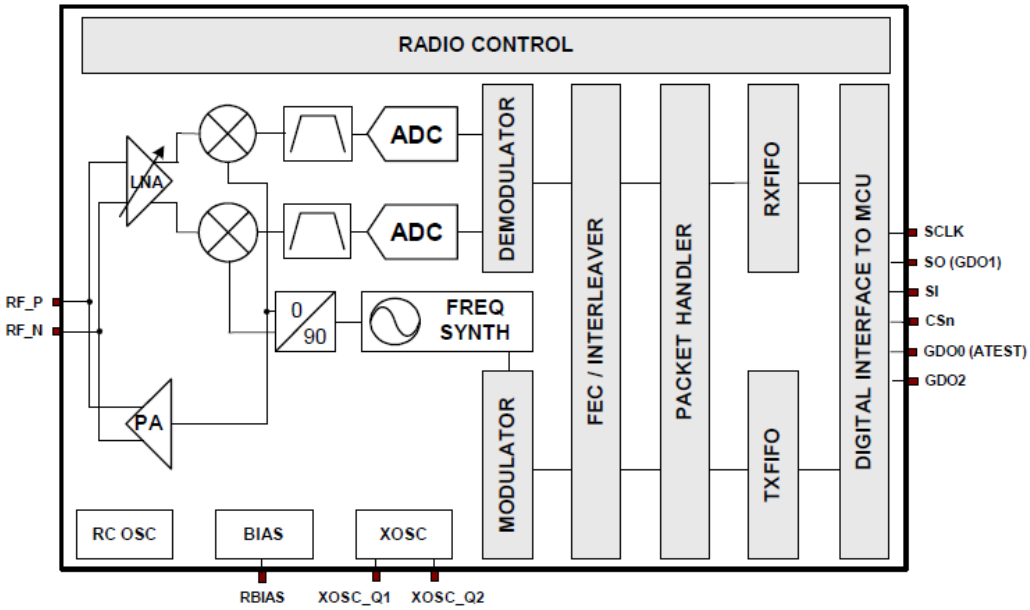

Figure 29. Block diagram

CC2500 features a low-IF receiver. The received RF signal is amplified by the lownoise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitised by the ADCs. Automatic gain control (AGC), fine channel filtering, demodulation

bit/packet synchronization are performed digitally.

The transmitter part of CC2500 is based on direct synthesis of the RF frequency. The frequency synthesizer includes a completely on-chip LC VCO and a 70 degrees phase shifter for generating the I and Q LO signals to the down-conversion mixers in receive mode. A crystal is to be connected to XOSC_Q1 and XOSC_Q2. The crystal oscillator generates the

reference frequency for the synthesizer, as well as clocks for the ADC and the digital part. A 4-wire SPI serial interface is used for configuration and data buffer access. The digital baseband includes support for channel configuration, packet handling, and data buffering.

CHAPTER-8

LIQUID CRYSTAL DISPLAY(LCD)

8.1 INTRODUCTION

A liquid crystal display (LCD) is a thin, flat electronic visual display that uses the light modulating properties of liquid crystals (LCs). LCs does not emit light directly. They are used in a wide range of applications, including computer monitors, television, instrument panels, aircraft cockpit displays, etc. LCDs have displaced cathode ray tube (CRT) displays in most applications. They are usually more compact, lightweight, portable, less expensive, more reliable.

Each pixel of an LCD typically consists of a layer of molecules aligned between two transparent electrodes, and two polarizing filters, the axes of transmission of which are (in most of the cases) perpendicular to each other. With no actual liquid crystal between the polarizing filters, light passing through the first filter would be blocked by the second (crossed) polarizer. In most of the cases the liquid crystal has double refraction.

The surfaces of the electrodes that are in contact with the liquid crystal material are treated so as to align the liquid crystal molecules in a particular direction. Electrodes are made of a transparent conductor called Indium Tin Oxide (ITO).

Before applying an electric field, the orientation of the liquid crystal molecules is determined by the alignment at the surfaces of electrodes. In a twisted nematic device the surface alignment directions at the two electrodes are perpendicular to each other, and so the molecules arrange themselves in a helical structure, or twist. This reduces the rotation of the polarization of the incident light, and the device appears grey. If the applied voltage is large enough, the liquid crystal molecules in the center of the layer are almost completely untwisted and the polarization of the incident light is not rotated as it passes through the liquid crystal layer. This light will then be mainly polarized perpendicular to the second filter, and thus be blocked and the pixel will appear black. By controlling the voltage applied across the liquid crystal layer in each pixel, light can be allowed to pass through in varying amounts thus constituting different levels of gray.

8.2 PIN DESCRIPTION

The most common used LCDs found in the market today are 1 line,2line, or 4 line LCDs which have only one controller and support at most of 80 characters, whereas LCDs supporting more than 80 characters make use of 2HD44780 controllers. More LCDs with 1 controller has 14 pins and LCDs with 2 controller has 16pins.

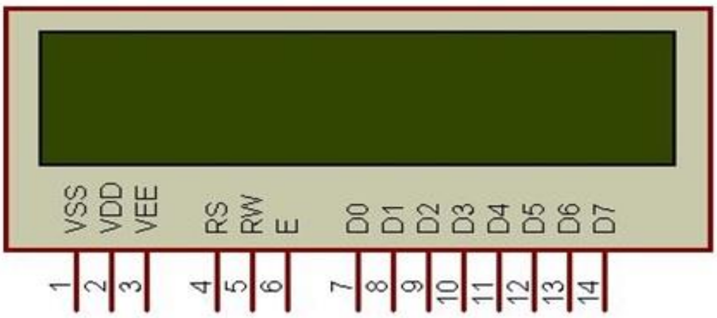

Figure 30. Pin diagram of 2x16 LCD

8.3 FEATURES

- 5 x 8 dots with cursor.
- Built-in controller (KS 0066 or Equivalent)
- + 5V power supply (Also available for + 3V)
- 1/16 duty cycle

- B/L to be driven by pin 1, pin 2 or pin 15, pin 16 or A.K (LED)
- N.V. optional for + 3V power supply.

PIN NO.,	SYMBOL	FUNCTION
1.	Vss	GND
2.	Vdd	+3V or +5V
3.	Vo	Contrast Adjustment
4.	RS	H/L Register Select Signal
5.	R/Ŵ	H/L Read and Write Signal
6.	E	H→L Enable Signal
7.	DB0	H/L Data Bus Line
8.	DB1	H/L Data Bus Line
9.	DB2	H/L Data Bus Line
8.	DB3	H/L Data Bus Line
11.	DB4	H/L Data Bus Line
12.	DB5	H/L Data Bus Line
13.	DB6	H/L Data Bus Line
14.	DB7	H/L Data Bus Line
15.	A/Vee	+4.2V for LED/Negative Voltage Output
16.	K	Power Supply for B/L (0V)

Table 11.Pin details of LCD

8.4 DISPLAY CHARACTER ADDRESS CODE

Display Position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DD RAM Address	00	01														0F
DD RAM Address	40	41														4F

Figure 31. Address code for displaying character

8.5 BF- BUSY FLAG

Busy flag is an status indicator flag for LCD. When we send a command or data to the LCD for processing, this flag is set (BF=1) and as soon as the instruction is executed successfully this flag is cleared (BF=0). This is helpful in producing and exact amount of delay for the LCD processing. To read busy flag, the condition RS=0 and R/W=1 must be met and the MSB of the LCD data bus (D7) act as busy flag. When BF =1 means LCD is busy and will not accept next command or data and BF=0 means LCD is ready for the next command or data to process.

8.6 INSTRUCTION AND DATA REGISTER

There are two 8-bit registers in HD44780 controller Instruction and Data register. Instruction register corresponds to the register where you send commands to LCD e.g LCD shift command, LCD clear, LCD address etc. and Data register is used for storing data which is to be displayed on LCD. when send the enable signal of the LCD is asserted, the data on the pins is latched in to the data register and data is then moved automatically to the DDRAM and hence is displayed on the LCD.

Data register is not only used for sending data to DDRAM but also for CGRAM, the address where you want to send the data, is decided by the instruction you send to LCD. We will discuss more on LCD instruction set further in this chapter.

8.7 COMMANDS AND INSTRUCTION SET

Only the instruction register (IR) and the data register (DR) of the LCD can be controlled by the MCU. Before starting the internal operation of the LCD, control information is temporarily stored into these registers to allow interfacing with various MCUs, which operate at different speeds, or various peripheral control devices. The internal operation of the LCD is determined by signals sent from the MCU. These signals, which include register selection signal (RS), read/write signal (R/W), and the data bus (DB0 to DB7), make up the LCD instructions (Table 3).

No.	Instruction	Hex	Decimal
1	Function Set: 8-bit, 1 Line, 5x7 Dots	0x30	48
2	Function Set: 8-bit, 2 Line, 5x7 Dots	0x38	56
3	Function Set: 4-bit, 1 Line, 5x7 Dots	0x20	32
4	Function Set: 4-bit, 2 Line, 5x7 Dots	0x28	40
5	Entry Mode	0x06	6
6	Display off Cursor off (clearing display without clearing DDRAM content)	0x08	8
7	Display on Cursor on	0x0E	14
8	Display on Cursor off	0x0C	12
9	Display on Cursor blinking	0x0F	15
10	Shift entire display left	0x18	24
12	Shift entire display right	0x1C	30
13	Move cursor left by one character	0x10	16
14	Move cursor right by one character	0x14	20
15	Clear Display (also clear DDRAM content)	0x01	1

Table 13. Commands

There are four categories of instructions that:

- Designate LCD functions, such as display format, data length, etc.
- Set internal RAM addresses
- Perform data transfer with internal RAM
- Perform the miscellaneous functions.

CHAPTER-9

SCENARIOS

9.1 FORWARD COLLISION AVOIDANCE

Forward collision avoidance feature is performed using Ultrasonic sensors. The sensor allow us to look further away in space and further ahead in time. The collision avoidance system is an automobile safety system designed to reduce the severity of an accident. Forward collision avoidance system aims at avoiding or atleast mitigating host vehicle frontal collision.The system gives an alert to encourage the driver to decelerate in advance with signal on display.

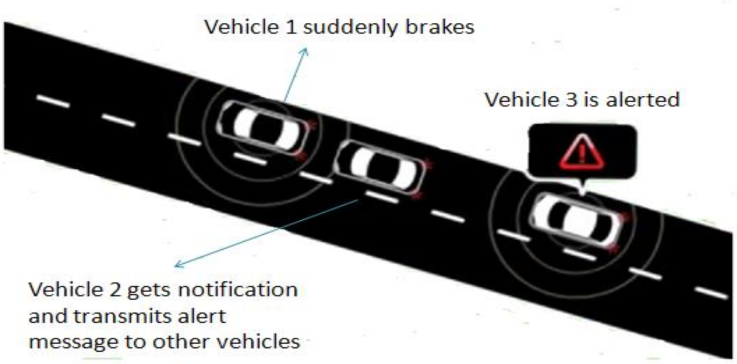

Figure 32. Vehicle collision avoidance scenario

When the vehicle suddenly brakes and when the distance between the vehicle and the one behind is lower , the vehicle behind is alerted and further it transmits the alert message to all the vehicles thereby avoiding collision occurance.

9.1.1 WORKING PRINCIPLE

Ultrasonic sensors work on a principle similar to radar or sonar which evaluates attributes of target by interpreting the echoes from radio or sound waves respectively. Ultrasonic sensors generate high frequency sound waves and evaluates the echo which is received back by the sensor. Sensors calculate the time interval between sending the signal and receiving the echo to determine the distance to an object. This technology is used for measuring distance.

This sensor works on Doppler Effect.It consists of a ultrasonic transmitter and a receiver. The transmitter transmits the signal in one direction. This transmitted signal is reflected back by the obstacle and received by the receiver. So the total time taken by the signal to get transmitted and to received back will be used to calculate the distance between the ultrasonic sensor and the obstacle.

9.1.2 FLOW DIAGRAM

The ultrasonic sensor installed in front of the vehicle monitors the relative distance of the vehicle directly ahead/obstacle. If the distance is greater than the threshold value, the sensor indicates high threat of collision and threatens the driver. The vehicle transmits alert messages to other vehicles.

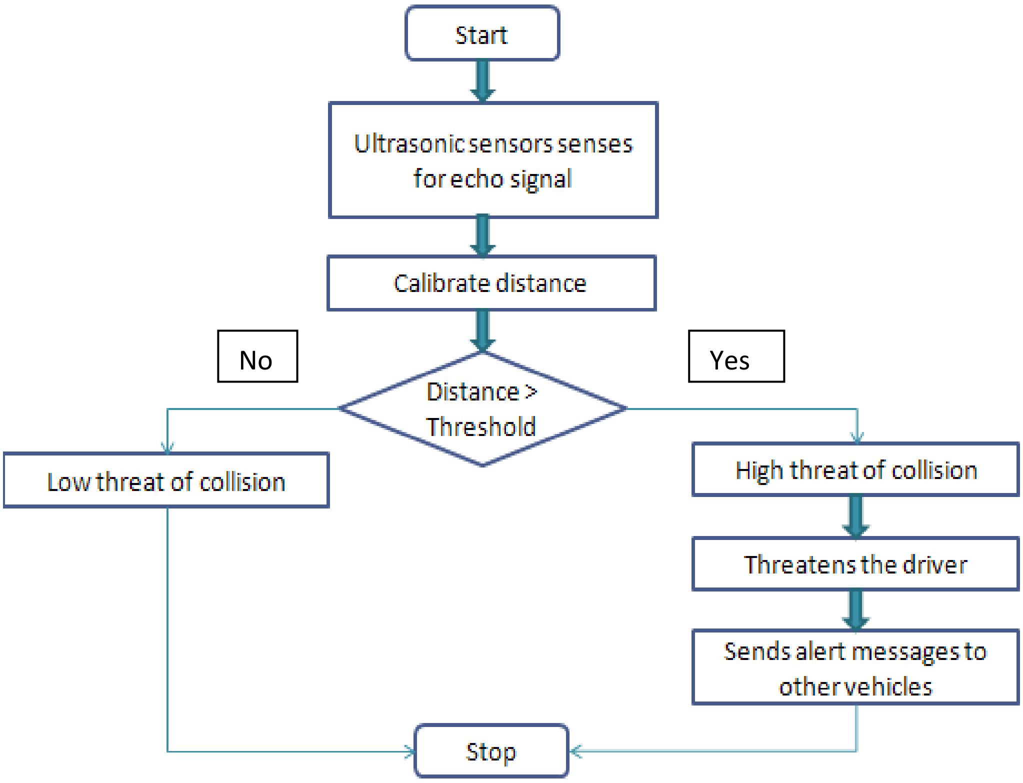

Figure 33. The flow diagram of civilian vehicle

9.2 EMERGENCY VEHICLE ALERT

Today, most cars are much more soundproof than ever before; most have air-conditioning so windows are usually closed; and many have high power stereos playing the radio or CD's at levels that cancel all sounds coming from outside the car. Some drivers are hearing impaired. These factors combine to make it difficult to build lights, sirens and horns that will alert the drivers inside their cars. Emergency vehicles have a hard time making people aware of their presence. In our project emergency alert message is sent to all other vehicles and thus providing the free passage for the fast moving emergency vehicle.

9.2.1 FLOW DIAGRAM

The Emergency vehicle can act also as ordinary vehicle. The latitude and longitude values are got by the emergency vehicle thereby calculating the direction of the vehicle approximately and sends emergency alert message to all the vehicles in its proximity.

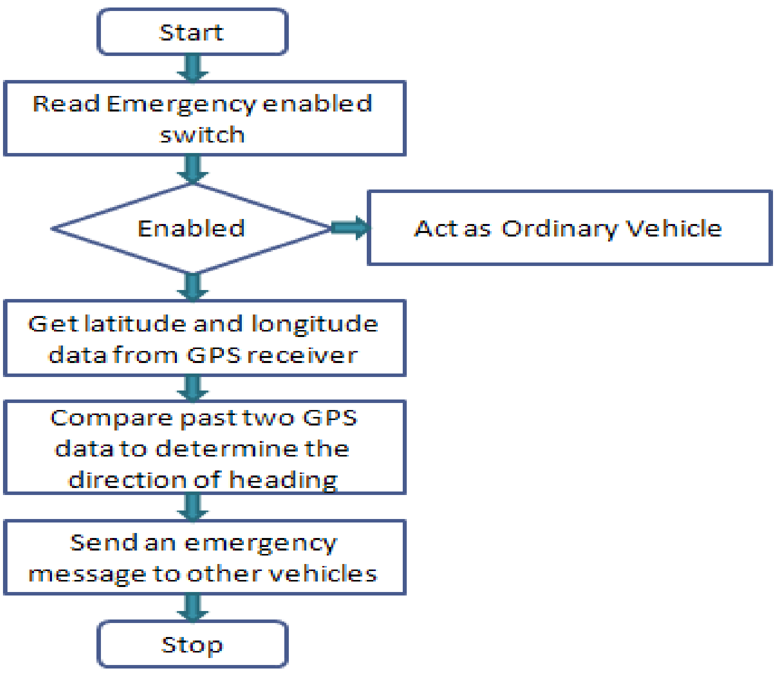

Figure 34. The flow diagram of emergency vehicle

9.3 PARKING GUIDANCE

The parking in big cities has become one of the key causes of the city traffic congestion. Even when a collision has occurred, the roads would be congested with vehicles and to clear traffic until the road is cleared parking guidance is absolute necessity for vehicles. Sending parking details directly to the vehicle is one of the effective way to improve the parking situation. To design this parking guidance system we are using Infrared sensors. These sensors find the free lots for parking. It can detect the presence of vehicle in lots on request and display it on LCD in its Central monitoring unit and send the details to the requested vehicle.

9.3.1 FLOW DIAGRAM

On request by the vehicle, the infrastructure module senses for the vacant lots using Infrared sensors. The gathered details are transmitted from the Infrastructure module to the vehicle requested for the parking details.

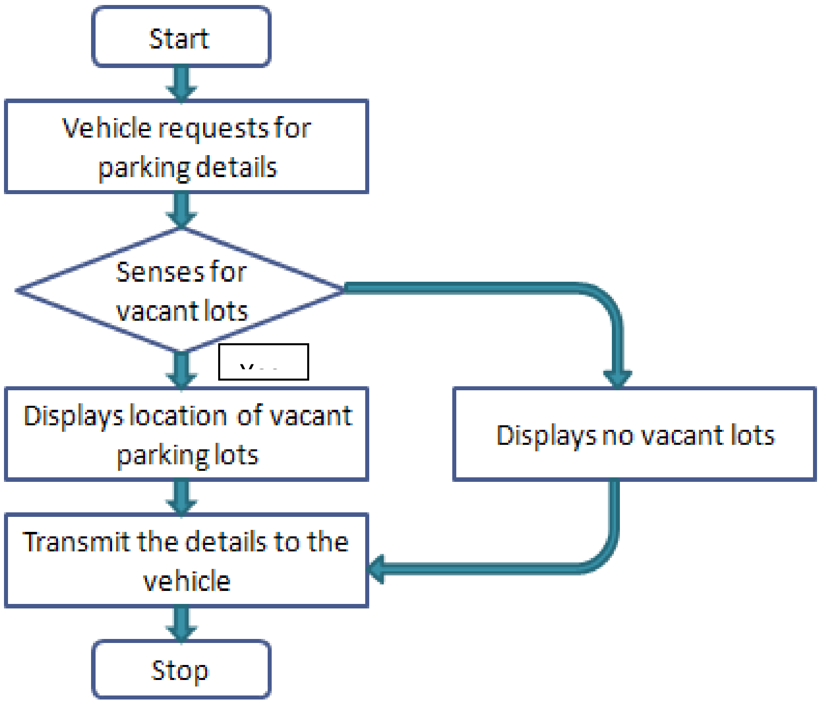

Figure 35. The flow diagram of Infrastructure module

9.3.2 WORKING PRINCIPLE

The Infrastructure module would be constantly broadcasting its own unique message signal(probably characters). If the vehicle needs a parking space, it would send an acknowledgment signal back to the infrastructure. The IR transmitter constantly transmits the IR rays which would be bounced back and received by the IR receiver if a vehicle is present, else it would not. There will be a difference in the voltage levels in the comparators of the IC LM358.When the car is present the output of the comparator goes low whereas in its absence the output would be high. Thus the location of free parking lots would be sent to the MCU in the infrastructure which in turn sends the same to the vehicle which makes the requisition.

CHAPTER 10

CONCLUSION

The project considers three important features – forward collision avoidance, emergency vehicle alert and parking guidance. The project is implemented by considering the significant conditions. The vehicle to vehicle communication is implemented and is verified with the help of prototype. The design is implemented for a short range and changing the range can be implemented in real time applications. Message is transmitted from the victim to the other vehicles present within the range. This continuous transfer was established by using the UART.

Under the emergency scenario the emergency vehicles like ambulance, fire engine shall broadcast an alert message to other vehicles within its proximity in real time. The parking situation which is a major problem in big cities is highly improved by sending the parking details directly to the vehicles.

The features implemented in our project is an initiation which could be implemented in real time cars with further advancements. The advancements that could be made are as follows,

- In Forward vehicle collision avoidance, speed sensors and camera module can be added to enhance the safety.
- In Infrastructure communication, traffic-light control can also be included.

APPENDIX

1)//*** Civilian Vehicle ***//

```
//---------LCD comments-----------------------------------------------
// LCD module connections
sbit LCD_RS at RD4_bit;
sbit LCD_EN at RD5_bit;
sbit LCD_D4 at RD0_bit;
sbit LCD_D5 at RD1_bit;
sbit LCD_D6 at RD2_bit;
sbit LCD_D7 at RD3_bit;
sbit LCD_RS_Direction at TRISD4_bit;
sbit LCD_EN_Direction at TRISD5_bit;
sbit LCD_D4_Direction at TRISD0_bit;
sbit LCD_D5_Direction at TRISD1_bit;
sbit LCD_D6_Direction at TRISD2_bit;
sbit LCD_D7_Direction at TRISD3_bit;
//LCD connections ends
// End LCD module connections
unsigned char uart_rd;
unsigned char Recbuf[10];
```

```
unsigned char tmp;

unsigned int Reccnt=0;

unsigned int i;

void Rec_buf_init(void)

{

 for(i=0;i<10;i++)

 {

 Recbuf[i]=0;

 }

}

void check()

{

 if((PORTA&0x01)==0x01)

 {

 Lcd_Cmd(_LCD_CLEAR);

 Lcd_Out(1,1,"Free slots:");

 UART1_Write('D');

do

{

 if(UART1_Data_Ready()==1)
```

```
{
tmp= UART1_Read();
Delay_ms(10);
 Lcd_Chr_CP(tmp);
 Delay_ms(10);
}
}while(tmp!='E');
tmp=0;
}
}
void main()
{
ANSEL  = 0;                       // Configure analog pins as digital
ANSELH = 0;
C1ON_bit = 0;                       // Disable comparators
C2ON_bit = 0;
TRISC=0;                               //PORTC as output for Motors
PORTC=0x00;                        //clear PORTC pins
TRISA=0x0F;//set PORTA 0,1,2,3, pins are input for switches or other inputs
 PORTA=0x00;
```

```
UART1_Init(9600);

Delay_ms(100);

Lcd_Init();                    // Initialize LCD

Lcd_Cmd(_LCD_CLEAR);

Rec_buf_init();

PORTC=0x05;

Lcd_Out(1,1,"Civilian Vehicle");

Delay_ms(1000);

while(1)

{

 PORTC=0x05

 UART1_Write_Text("Ready");

if(UART1_Data_Ready()==1)

{

uart_rd=UART1_Read();

Lcd_Out(1,1,"Seems like a");

Lcd_Out(2,1,"Distrubance");

Delay_ms(500);

switch(uart_rd)

{
```

```
 case 'E':
 Lcd_Cmd(_LCD_CLEAR);
 Lcd_Out(1,1,"Emergency Vehicle");
 Lcd_Out(2,1,"Appearing");
PORTC=0x09;                          //left
Delay_ms(2000);
 PORTC=0x05;
Delay_ms(1000);
 PORTC=0x06;                          //right
Delay_ms(2000);
PORTC=0x05;
Delay_ms(2000);
PORTC=0x00;
Delay_ms(5000);
break;
case 'P':
Lcd_Cmd(_LCD_CLEAR);
Lcd_Out(1,1,"Infrastructure Block");
Lcd_Out(2,1,"Ahead");
Delay_ms(1000);
```

```
Lcd_Cmd(_LCD_CLEAR);

Lcd_Out(1,1,"Check ?");

Delay_ms(2000);

check();

break;

case 'O':

Lcd_Cmd(_LCD_CLEAR);

Lcd_Out(1,1,"Front Vehivle");

Lcd_Out(2,1,"Stopped");

PORTC=0x00;

Delay_ms(2000);

break;

}

}

}

}
```

2)Emergency vehicle

```
  // LCD module connections

sbit LCD_RS at RD4_bit;

sbit LCD_EN at RD5_bit;
```

```
sbit LCD_D4 at RD0_bit;

sbit LCD_D5 at RD1_bit;

sbit LCD_D6 at RD2_bit;

sbit LCD_D7 at RD3_bit;

sbit LCD_RS_Direction at TRISD4_bit;

sbit LCD_EN_Direction at TRISD5_bit;

sbit LCD_D4_Direction at TRISD0_bit;

sbit LCD_D5_Direction at TRISD1_bit;

sbit LCD_D6_Direction at TRISD2_bit;

sbit LCD_D7_Direction at TRISD3_bit;

// End LCD module connections

//2.9v

#define THLD_RAIN 600

#define THLD_LDR 600

//3,5,8 sec

#define THLD_TIME_1 1200

#define THLD_TIME_2 2000

#define THLD_TIME_3 3200

//1: 3sec Forward:

//2: 3sec left & forward,
```

```
//3: 3sec Right & forward,

//4: 3sec Left & Reverse,

//5: 3sec Right & Reverse and

//6: Stop

char uart_rd;

char adc_char=0;

unsigned char mov_steps=0;

unsigned int cnt;

unsigned char ch;

unsigned int adc_toxic;

unsigned int adc_fire;

unsigned int adc_human;

unsigned char adc_val;

unsigned int emer_flag=0;

long tlong;

/***** GPS Processing****************/

unsigned char Lat_rec_buf[20];

unsigned char Long_rec_buf[20];

unsigned char uart_rdc;

unsigned char SMS_Flag=0;
```

```
unsigned int temp=0;

unsigned int a,b;

unsigned char txt1[5];

void Rec_bufinit(void)

{

unsigned char i=0;

for(i=0;i<20;i++)

{

Lat_rec_buf[i]=0;

Long_rec_buf[i]=0;

}

}

void main()

{

INTCON = 0;                          // disable all interrupts

ANSEL  = 0x00;                          // Configure AN2 pin as analog input

ANSELH = 0;                          // Configure other AN pins as digital I/O

C1ON_bit = 0;                          // Disable comparators

C2ON_bit = 0;

TRISA  = 0x0F;
```

```
TRISB  = 0x00;

TRISC = 0x00;                    // designate PORTC pins as output

TRISB=0x80;

PORTB=0x00;

Lcd_Init();

Lcd_Cmd(_LCD_CURSOR_OFF);        // send command to LCD (cursor off)

Lcd_Cmd(_LCD_CLEAR);             // send command  to LCD (clear LCD)

UART1_Init(9600);

Delay_ms(100);

Lcd_Out(1,1,"V&V");

Delay_ms(500);

T1CON = 0x10;

PORTC = 0x0A;/*Motor to Rotate */

if((PORTA&0x01)==0x01)

{

emer_flag=0;

Lcd_Out(1,1,"CIVILIAN");

}

else

{
```

```
emer_flag=1;

Lcd_Out(1,1,"EMERGENCY");

}

Delay_ms(2000);

while (1)

{

if(emer_flag==0)

{

TMR1H = 0;

TMR1L = 0;

PORTB=0x40;                // send trigger on D6

Delay_us(10);           //10uS Delay

PORTB=0x00;

while(!((PORTB&0x80)==0x80));         //Waiting for Echo 1

T1CON=T1CON|0x01;//Set Timer1: Start

while((PORTB&0x80)==0x80);         //Waiting for Echo1 goes LOW

T1CON=T1CON&0xFE; //Clear Timer1: Stop

a = (TMR1L | (TMR1H<<8));   //Reads Timer Value

a = a/58.82;              //Converts Time to Distance

a = a + 1;                //Distance Calibration
```

```
if(a<=20)

{

Lcd_Out(2,1,"OBS");

Delay_ms(200);

UART1_Write('O');

Delay_ms(200);

}

else

{

Lcd_Out(2,1,"NBS");

Delay_ms(500);

}

}

else

{

if(PORTA&0x02==0x02)

{

UART1_Write('E');

Delay_ms(200);

}
```

```
else if(PORTA&0x04==0x04)

{

UART1_Write('W');

Delay_ms(200);

}

else

{

UART1_Write('M');

Delay_ms(200);

}

temp=0;

while((UART1_Read())!='$');        //wait till '' receive  }

while((UART1_Read())!='G');        //wait till '' receive  }

while((UART1_Read())!='P');        //wait till '' receive  }

while((UART1_Read())!='G');        //wait till '' receive  }

while((UART1_Read())!='G');        //wait till '' receive  }

while((UART1_Read())!='A');        //wait till '' receive  }

while((UART1_Read())!=',');        //wait till '' receive  }

while((UART1_Read())!='.');        //wait till '' receive  }

while((UART1_Read())!='0');        //wait till '' receive  }
```

```
while((UART1_Read())!=',');         //wait till '' receive  }

while((UART1_Read())!='N');         //wait till '' receive  }

do{

if(UART1_Data_Ready()!= 0)

{

uart_rdc = UART1_Read();

Lat_rec_buf[temp]= uart_rdc;

temp++;

if(temp==9)break;

}

}while(uart_rdc!='N');

while((UART1_Read())!='N');         //wait till '' receive  }

while((UART1_Read())!=',');         //wait till '' receive  }

temp=0;

do

{

if(UART1_Data_Ready()!= 0)

{

uart_rdc = UART1_Read();

Long_rec_buf[temp]= uart_rdc;
```

```
temp++;

if(temp==9)break;

}

}while(uart_rdc!='\n');

Lat_rec_buf[temp+1]='\0';

Lcd_Cmd(_LCD_CLEAR);

Lcd_Out(1,4,Lat_rec_buf);

Lcd_Out(1,1,"LT:");

Long_rec_buf[temp+1]='\0';

Lcd_Out(2,4,Long_rec_buf);

Lcd_Out(2,1,"LG:");

Delay_ms(2000);

}

}

}//~!
```

3)Infrastructure

```
// LCD module connections

sbit LCD_RS at RD4_bit;

sbit LCD_EN at RD5_bit;

sbit LCD_D4 at RD0_bit;
```

```
sbit LCD_D5 at RD1_bit;

sbit LCD_D6 at RD2_bit;

sbit LCD_D7 at RD3_bit;

sbit LCD_RS_Direction at TRISD4_bit;

sbit LCD_EN_Direction at TRISD5_bit;

sbit LCD_D4_Direction at TRISD0_bit;

sbit LCD_D5_Direction at TRISD1_bit;

sbit LCD_D6_Direction at TRISD2_bit;

sbit LCD_D7_Direction at TRISD3_bit;

// End LCD module connections

unsigned short count=0;

unsigned char cnt;

unsigned char total;

unsigned char uart_rd;

void main()

{

ANSEL  = 0;                     // Configure AN pins as digital I/O

ANSELH = 0;

C1ON_bit = 0;                   // Disable comparators

C2ON_bit = 0;
```

```
TRISA=0xFF;
PORTA=0x00;
Lcd_Init();                    // Initialize LCD
Lcd_Cmd(_LCD_CLEAR);             // Clear display
Lcd_Cmd(_LCD_CURSOR_OFF);        // Cursor off
 UART1_Init(9600);
Delay_ms(100);
while(1)
{
count=0;
UART1_Write('P');
Lcd_Cmd(_LCD_CLEAR);
if(PORTA.F0==1)
{
Lcd_Out(2,2,"P1");
count++;
Delay_ms(10);
}
if(PORTA.F1==1)
{
```

```
Lcd_Out(2,6,"P2");
count++;
Delay_ms(10);
}
if(PORTA.F2==1)
{
Lcd_Out(2,10,"P3");
count++;
Delay_ms(10);
}
if(PORTA.F3==1)
{
Lcd_Out(2,14,"P4");
count++;
Delay_ms(10);
}
 if(count==0)
{
Lcd_Out(1,13,"0");
UART1_Write('0');
```

```
}
if(count==1)
{
Lcd_Out(1,13,"1");
UART1_Write('1');
}
if(count==2)
{
Lcd_Out(1,13,"2");
UART1_Write('2');
}
if(count==3)
{
Lcd_Out(1,13,"3");
UART1_Write('3');
}
if(count==4)
{
Lcd_Out(1,13,"4");
UART1_Write('4');
```

```
}
if(UART1_Data_Ready())
        {
        uart_rd=UART1_Read();
        switch(uart_rd)
            {
        case 'D':
              if(PORTA.F0==1)
               {
                UART1_Write('1');
               }
              if(PORTA.F1==1)
               {
                UART1_Write('2');
               }
              if(PORTA.F2==1)
               {
                UART1_Write('3');
               }
              if(PORTA.F3==1)
```

```
          {
           UART1_Write('4');
          }
          Delay_ms(10);
          UART1_Write('E');
          break;
case 'T':
          if(count==0)
           {
           Lcd_Out(1,13,"0");
           UART1_Write('0');
           }
          if(count==1)
           {
           Lcd_Out(1,13,"1");
           UART1_Write('1');
           }
          if(count==2)
           {
           Lcd_Out(1,13,"2");
```

```
UART1_Write('2');
}
if(count==3)
{
 Lcd_Out(1,13,"3");
 UART1_Write('3');
}
if(count==4)
{
 Lcd_Out(1,13,"4");
 UART1_Write('4');
}
break;
}//switch end
}
Lcd_Out(1,1,"Free slots:");
Delay_ms(3000); }
}
}
```