INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, NAGPUR

Department of Electronics and Communication Engineering

Academic Session: JULY to DECEMBER (Odd Semester)

CMOS LAB (ECL-312)

V Semester ECE-IoT

Date:05/08/2024

Experiment No.2(A)

Aim: To plot V-I characterstics of NMOS devices.

Software Required: WinSpice.

Theory:

- **NMOS (N-channel Metal-Oxide-Semiconductor) transistor** is a type of MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) where the majority carriers are electrons.
- It operates in three regions: **Cutoff, Linear (Ohmic), and Saturation**.
    - **Cutoff Region:** The NMOS is OFF. No current flows from drain to source (ID = 0). This occurs when the gate-source voltage (VGS) is less than the threshold voltage (Vth).
    - **Linear (Ohmic) Region:** The NMOS is ON. The drain current (ID) increases linearly with an increase in VDS, similar to a resistor. This occurs when VGS > Vth and VDS < (VGS - Vth).
    - **Saturation Region:** The NMOS is fully ON, and the drain current (ID) is relatively independent of VDS, depending primarily on VGS. This occurs when VDS ≥ (VGS - Vth).
- The characteristic curves of an NMOS transistor are plots of the drain current (ID) versus the drain-source voltage (VDS) for different values of gate-source voltage (VGS).

Codes:

I. With respect to change in Vg:

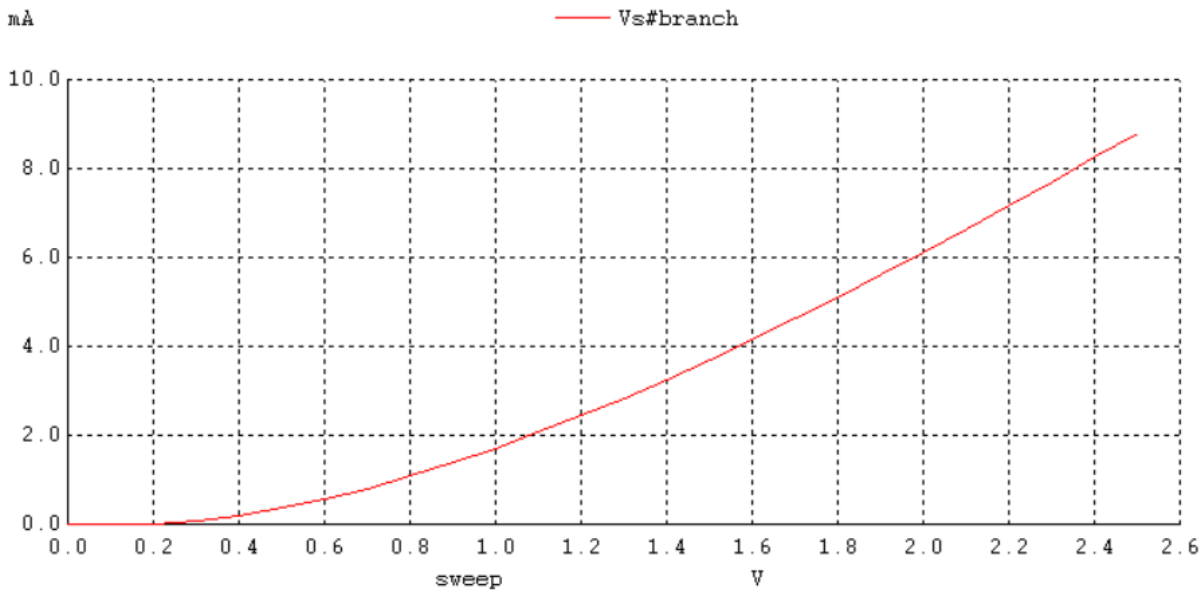
```
*LAB 2*
Vd 3 0 dc 3V
Vg 1 0 dc 2V
Vs 3 2 dc 0V
.model nmod nmos level=54 version=4.7
M1 2 1 0 0 nmod w=0.1mm l=0.01mm
.dc Vg 0 2.5 0.1
.control
run
plot i(Vs)
.endc
.end
```

II. Change in Vg for each step of Vd:

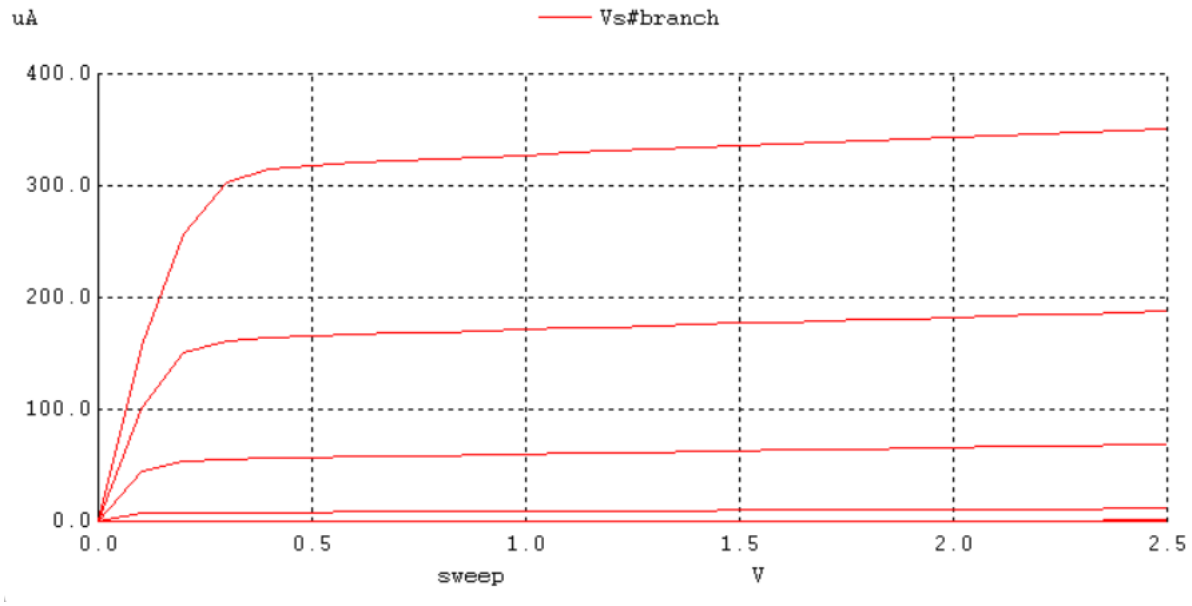
```
*LAB 2*
Vd 3 0 dc 3V
Vg 1 0 dc 2V
Vs 3 2 dc 0V
.model nmod nmos level=54 version=4.7
M1 2 1 0 0 nmod w=0.1mm l=0.01mm
.dc Vd 0 2.5 0.1 Vg 0 0.5 0.1
.control
run
plot i(Vs)
.endc
.end
```

Output:

I. With respect to change in Vg:



II. Change in Vg for each step of Vd:



Result/ Conclusion:

By plotting the V-I characteristics using WinSpice, you can visualize the different regions of operation for the NMOS transistor and better understand its behavior

under varying conditions. This understanding is crucial for designing and analyzing circuits that utilize NMOS transistors.