INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, NAGPUR

Department of Electronics and Communication Engineering

Academic Session: JULY to DECEMBER (Odd Semester)

CMOS LAB (ECL-312)

V Semester ECE-IoT

Date:23/09/2024

Experiment No.6

Aim: To design the layout for a Full Adder using CMOS technology in Microwind and perform the necessary analysis.

Software Required: MICROWIND

Theory:

A Full Adder is a combinational circuit that adds three bits (A, B, and Cin) to produce two outputs: the sum (S) and carry (Cout). In CMOS technology, Full Adders are constructed using a combination of NAND, NOR, and XOR gates. The layout of a Full Adder involves creating the transistor-level design and connecting these gates to implement the Boolean equations for Sum and Carry.

The Boolean equations for the Full Adder are: • Sum (S) = (A ⊕ B) ⊕ Cin • Carry (Cout) = (A · B) + (Cin · (A ⊕ B)) The Boolean equations for the 6T SRAM are:

Where:

- ⊕ denotes the XOR operation.
- · denotes the AND operation.

In CMOS layout design, the Full Adder circuit consists of PMOS and NMOS transistors, with proper routing of diffusion, polysilicon, and metal layers to form the logical gates required to perform the addition operation.

Netlist:

- **SUM**

Cin(A'B'+AB)+Cin'(A'B+AB')

```
.subckt pass_inv 1 2 3
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
.ends

va 14 0 pulse (0 5 0 0 0 100m 200m)
vb 15 0 dc 0v
vcin 10 0 dc 0v
vdd 2 0 dc 5v
x_a 14 2 12 pass_inv
x_b 15 2 13 pass_inv
x_c 10 2 11 pass_inv
x_o 19 2 23 pass_inv
m1 16 10 0 0 nmod w=100u l=10u
m2 17 13 16 16 nmod w=100u l=10u
m3 19 12 17 17 nmod w=100u l=10u
m4 18 15 16 16 nmod w=100u l=10u
m5 19 14 18 18 nmod w=100u l=10u
m6 20 11 0 0 nmod w=100u l=10u
m7 21 15 20 20 nmod w=100u l=10u
m8 19 12 21 21 nmod w=100u l=10u
m9 19 14 22 22 nmod w=100u l=10u
m10 22 13 20 20 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
m11 19 2 0 0 pmod w=100u l=10u
.model pmod pmos level=54 version=4.7
.tran 0.1m 400m
.control
run
plot V(23) V(14)
.endc
.end
```

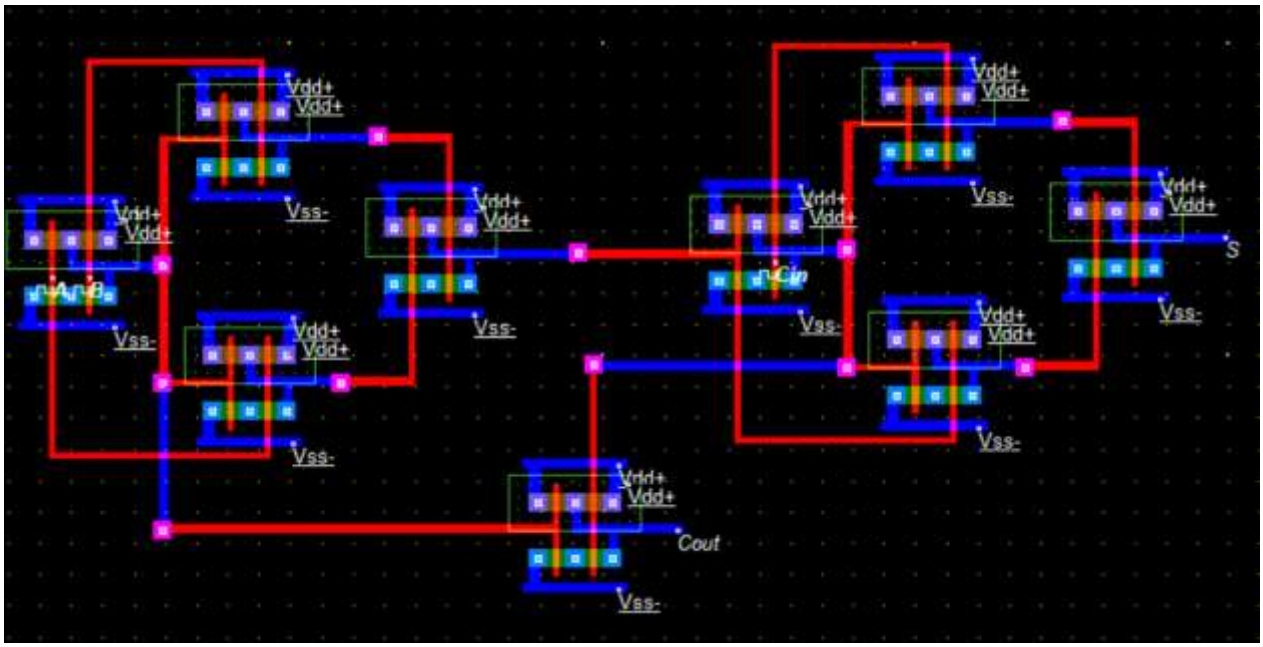
- **COUT**

Cout=AB+BCin+ACin

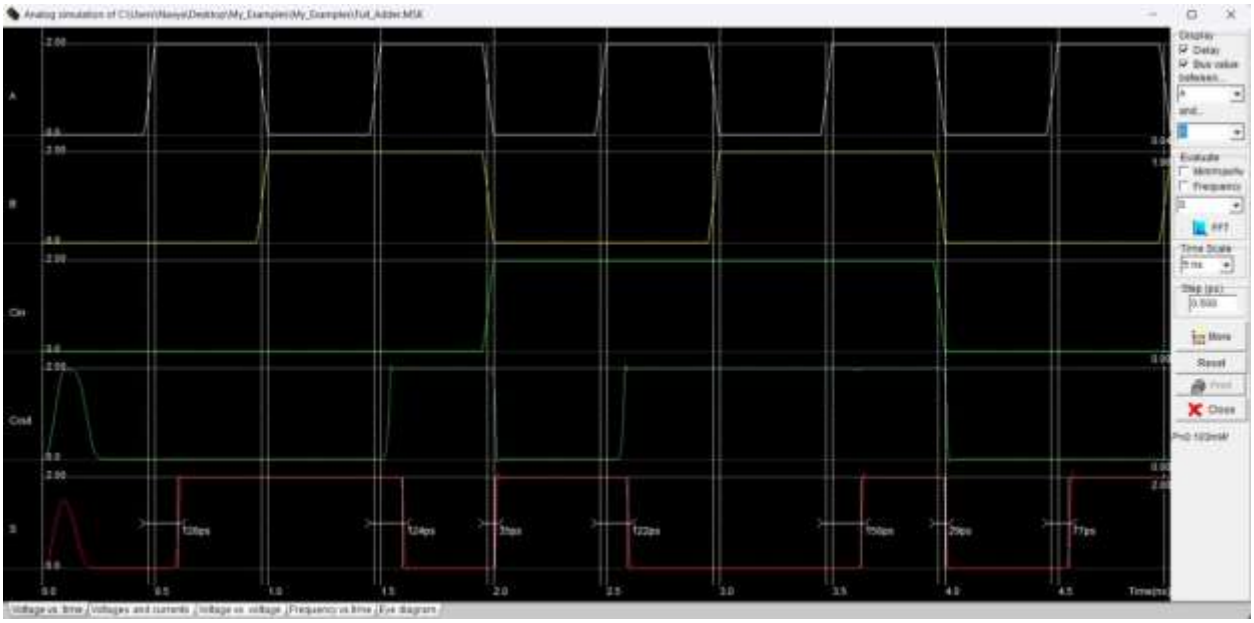
```
.subckt pass_inv 1 2 3
m1 3 1 0 0 nmod w=100u l=10u
m2 3 1 2 2 pmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
.ends
va 14 0 pulse(0 5 0 0 0 100m 200m)
vb 15 0 dc 0v
vcin 10 0 dc 0v
vdd 2 0 dc 5v
x_cout 16 2 17 pass_inv
m1 11 15 0 0 nmod w=100u l=10u
m2 16 14 11 11 nmod w=100u l=10u
m3 12 10 0 0 nmod w=100u l=10u
m4 16 15 12 12 nmod w=100u l=10u
m5 13 10 0 0 nmod w=100u l=10u
m6 16 14 13 13 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
m7 16 0 2 2 pmod w=100u l=10u
.model pmod pmos level=54 version=4.7
.tran 0.1m 400m
.control
run
plot V(17) V(14)
.endc
.end
```

Layouts:

FULL ADDER



Output:



VOLTAGE TIME ANANLYSIS

Result/ Conclusion:

The CMOS layout design for the Full Adder was successfully implemented in Microwind. The design process involved creating the necessary XOR, AND, and OR gates using PMOS and NMOS transistors, followed by interconnecting them to form the Full Adder circuit. The layout was validated using Design Rule Checking (DRC) and Layout vs. Schematic (LVS) verification to ensure correctness. Simulation results confirmed that the Full Adder operates correctly, with accurate Sum and Carry outputs for all possible input combinations, demonstrating the effective application of CMOS layout design techniques in Microwind.