INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, NAGPUR

Department of Electronics and Communication Engineering

Academic Session: JULY to DECEMBER (Odd Semester)

CMOS LAB (ECL-312)

V Semester ECE-IoT

Date:19/08/2024

Experiment No.4

Aim: To design CMOS circuit for the given equations using sub-circuit approach.

Software Required: WinSpice.

Theory:

CMOS Logic Gates

- **CMOS Inverter:** The basic building block of CMOS technology is the inverter, which consists of one PMOS and one NMOS transistor.
- **CMOS NAND and NOR Gates:** More complex logic gates like NAND and NOR can be built by combining multiple PMOS and NMOS transistors.

Sub-Circuit Approach The sub-circuit approach involves breaking down a complex Boolean expression into simpler sub-expressions that can be realized using basic CMOS logic gates. Each sub-expression is designed separately as a sub-circuit, which is then combined to form the overall circuit.

Codes:

I. Y=ABC+D:

```
**abc+d**
.subckt pass_and 1 2 3 4
M1 1 2 4 4 nmod w=100u l=10u
M2 2 3 4 4 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.ends
.subckt pass_or 1 2 3 4
M1 2 2 4 4 nmod w=100u l=10u
M2 1 3 4 4 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.ends
.subckt pass_inv 1 2 3
M1 3 1 0 0 pmod w=100u l=10u
M2 3 1 2 2 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
.ends
Va 10 0 pulse(0 5 0 0 0 100m 200m)
Vb 11 0 dc 5
Vc 14 0 dc 5
Vd 17 0 dc 0
Vdd 2 0 dc 5
Xb 11 2 12 pass_inv
Xc 14 2 15 pass_inv
Xd 17 2 18 pass_inv
Xa_and_b 10 11 12 13 pass_and
Xab_and_c 13 14 15 16 pass_and
Xabc_or_d 16 17 18 19 pass_or
.tran 0.1m 400m
.control
run
plot v(10) v(19)
.endc
.end
```

II. Y=(AB+C)D:

```
**(AB+C)D**
.subckt pass_and 1 2 3 4
M1 1 2 4 4 nmod w=100u l=10u
M2 2 3 4 4 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.ends
.subckt pass_or 1 2 3 4
M1 2 2 4 4 nmod w=100u l=10u
M2 1 3 4 4 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.ends
.subckt pass_inv 1 2 3
M1 3 1 0 0 pmod w=100u l=10u
M2 3 1 2 2 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
.ends
Vdd 2 0 dc 5
Va 10 0 pulse(0 5 0 0 0 100m 200m)
Vb 11 0 dc 5
Vc 14 0 dc 5
Vd 17 0 dc 5
Xb 11 2 12 pass_inv
Xc 14 2 15 pass_inv
```

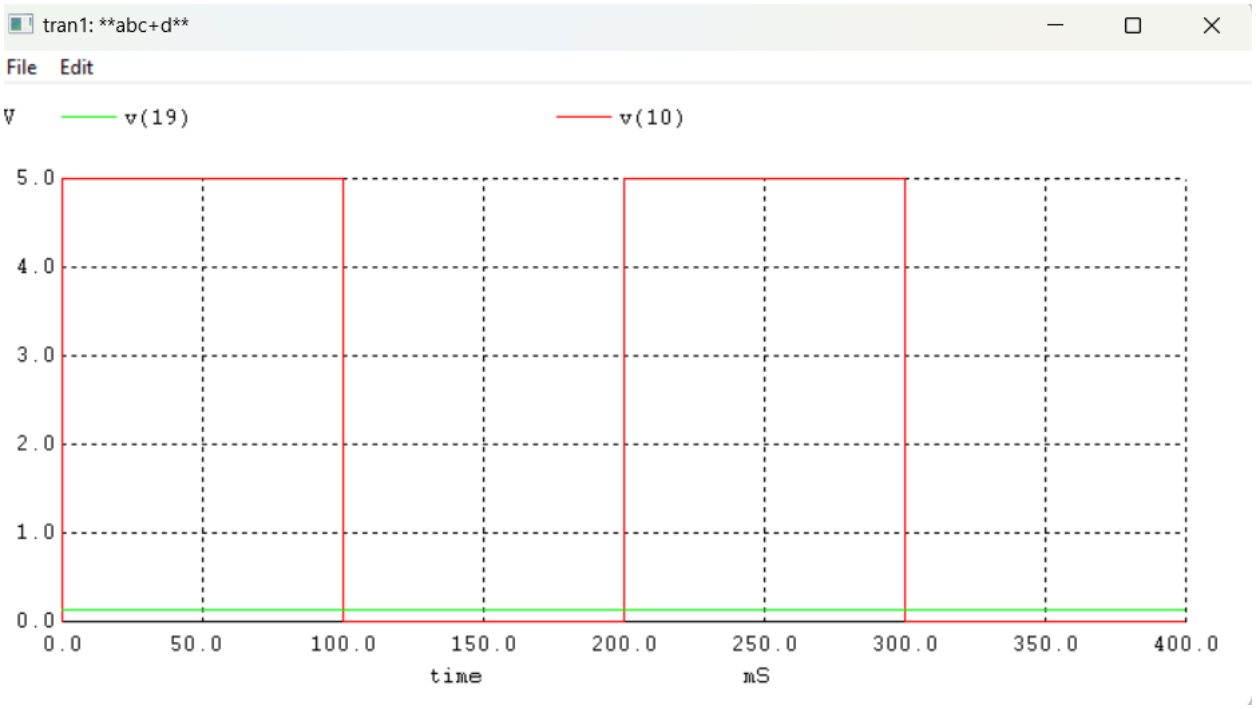
```
Xd 17 2 18 pass_inv

Xa_and_b 10 11 12 13 pass_and
Xab_or_c 13 14 15 16 pass_or
Xab_c_and_d 16 17 18 19 pass_and
.tran 0.1m 400m
.control
run
plot v(10) v(19)
.endc
.end
```

III. Y=AB+C(D+E):

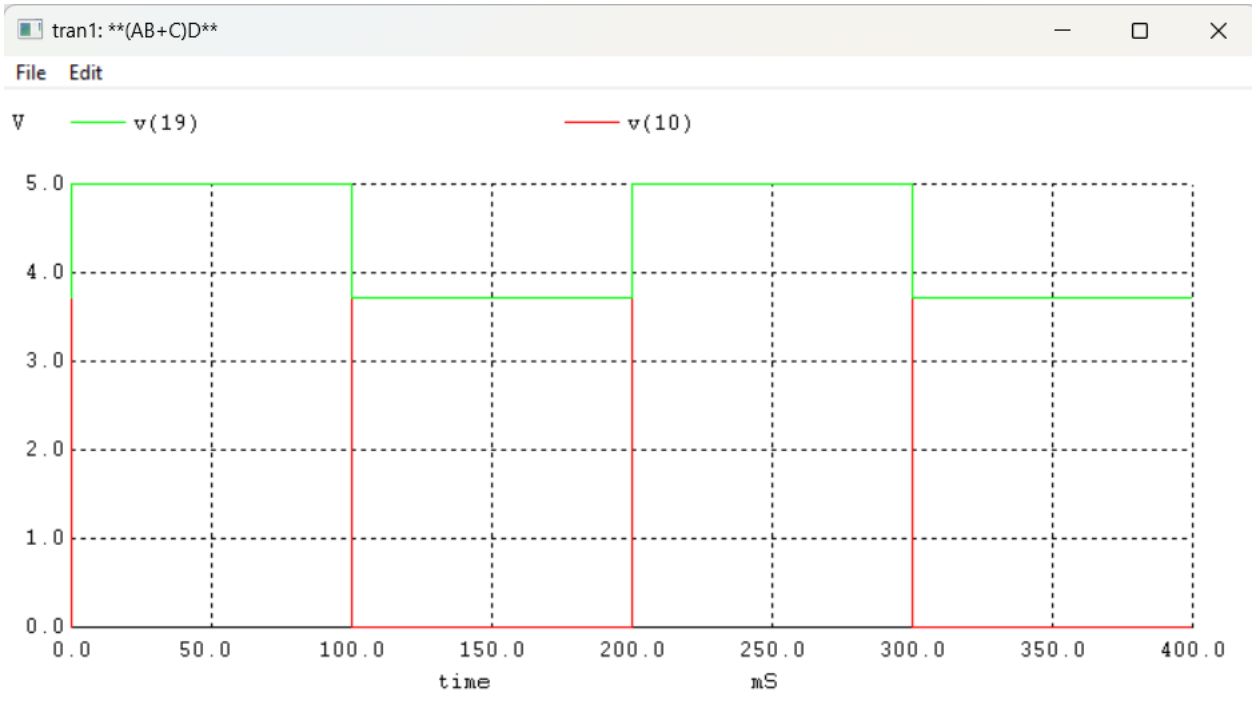
```
.subckt pass_and 1 2 3 4
M1 1 2 4 4 nmod w=100u l=10u
M2 2 3 4 4 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.ends
.subckt pass_or 1 2 3 4
M1 2 2 4 4 nmod w=100u l=10u
M2 1 3 4 4 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.ends
.subckt pass_inv 1 2 3
M1 3 1 0 0 pmod w=100u l=10u
M2 3 1 2 2 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
.ends
Vdd 2 0 dc 5
Va 10 0 pulse(0 5 0 0 0 100m 200m)
Vb 11 0 dc 5
Vc 14 0 dc 5
Vd 17 0 dc 5
Ve 20 0 dc 5
Xb 11 2 12 pass_inv
Xc 14 2 15 pass_inv
Xd 17 2 18 pass_inv
Xe 20 2 21 pass_inv
Xa_and_b 10 11 12 13 pass_and
Xd_and_e 17 20 21 22 pass_or
Xc_and_de 14 22 23 24 pass_and
Xab_or_cde 13 24 25 26 pass_or
.tran 0.1m 400m
.control
run
plot v(10) v(26)
.endc
.end
```

Output:

I. Y=ABC+D:



II. Y=(AB+C)D:



III. Y=AB+C(D+E):

Result/ Conclusion:

By following the sub-circuit approach, complex CMOS circuits can be designed in a modular manner, which simplifies the design process and improves the accuracy of the final circuit. This lab exercise provides practical experience in CMOS circuit design and verification.