INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, NAGPUR

Department of Electronics and Communication Engineering

Academic Session: JULY to DECEMBER (Odd Semester)

CMOS LAB (ECL-312)

V Semester ECE-IoT

Date:12/08/2024

Experiment No.3

Aim: CMOS Circuit Design.

Software Required: WinSpice.

Theory:

CMOS Logic Gates

- **CMOS Inverter (NOT Gate):** The simplest CMOS circuit, consisting of one PMOS and one NMOS transistor.
- **Operation:** PMOS transistors pull the output high when the input is low, while NMOS transistors pull the output low when the input is high.

CMOS Circuit Design Process

1. **Schematic Design:** Draw the circuit diagram using PMOS and NMOS transistors.
2. **Netlist Creation:** Convert the schematic into a text-based netlist for simulation.
3. **Simulation with WinSpice:** Analyze the circuit's behavior using DC, transient, and sometimes AC analysis.
4. **Post-Simulation Analysis:** Review the output waveforms to ensure proper operation.

Codes:

I. INVERTER:

```
*LAB 3A*
Vdd 2 0 dc 3V
.model nmod nmos level=54 version=4.7
M1 3 1 0 0 nmod w=100u l=10u
.model pmod pmos level=54 version=4.7
M2 3 1 2 2 pmod w=100u l=10u
V1 1 0 pulse( 0 5 0 0 0 100 200)
.tran 0.1 400
.control
run
plot V(1) V(3)
.endc
.end
```

II. INVERTER FOR CHANGE IN INPUT FROM 0 TO 5V LINEARLY:

```
*LAB 3B*
Vdd 2 0 dc 3v
.model nmod nmos level = 54 version = 4.7
M1 3 1 0 0 nmod w = 1u l = 10u
.model pmod pmos level = 54 version = 4.7
M2 3 1 2 2 pmod w = 100u l = 10u
V1 1 0 dc 5v
.dc V1 0 5 0.1
.control
run
plot V(1) V(3)
.endc
.end
```

III. NOR GATE:

```
*LAB 3C*
Vdd 5 0 dc 3v
.model nmod nmos level = 54 version = 4.7
M1 3 2 0 0 nmod w = 100u l = 10u
M2 3 1 0 0 nmod w = 100u l = 10u
.model pmod pmos level = 54 version = 4.7
M3 4 2 3 3 pmod w = 100u l = 10u
M4 5 1 4 4 pmod w = 100u l = 10u
V1 1 0 pulse(0 5 0 0 0 100 200)
V2 2 0 dc 0V
.tran 0.1 400
.control
run
plot v(1) v(3)
.endc
.end
```

IV. AND GATE:

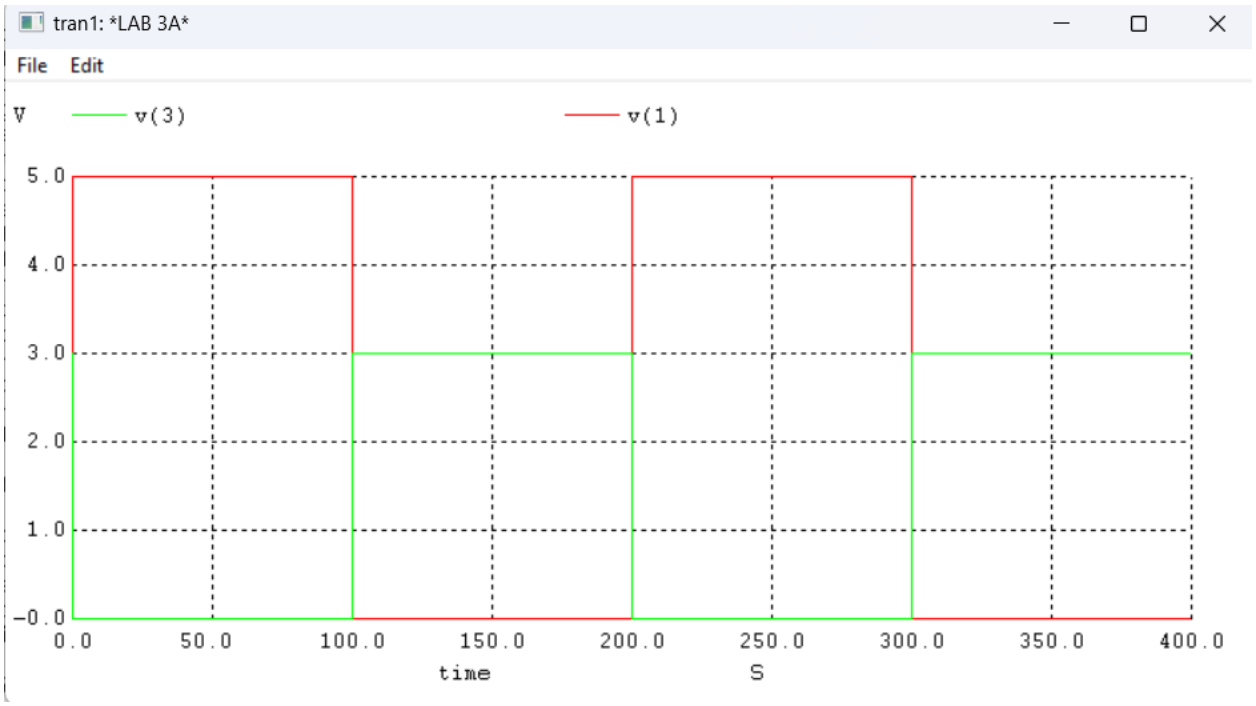
```
*LAB 3D*
Vdd 5 0 dc 3V
.model pmod pmos level = 54 version = 4.7
M1 4 1 5 5 pmod w = 100u l = 10u
M2 4 3 5 5 pmod w = 100u l = 10u
.model nmod nmos level = 54 version = 4.7
M3 4 3 2 2 nmod w = 100u l = 10u
M4 2 1 0 0 nmod w = 100u l = 10u
V1 1 0 pulse(0 5 0 0 0 100m 200m)
V3 3 0 pulse(0 5 0 0 0 50m 400m)
.tran 0.1m 400m
.control
run
plot V(1) V(3) V(4)
.endc
.end
```

V. Y = ~(A(B + C) + DE):

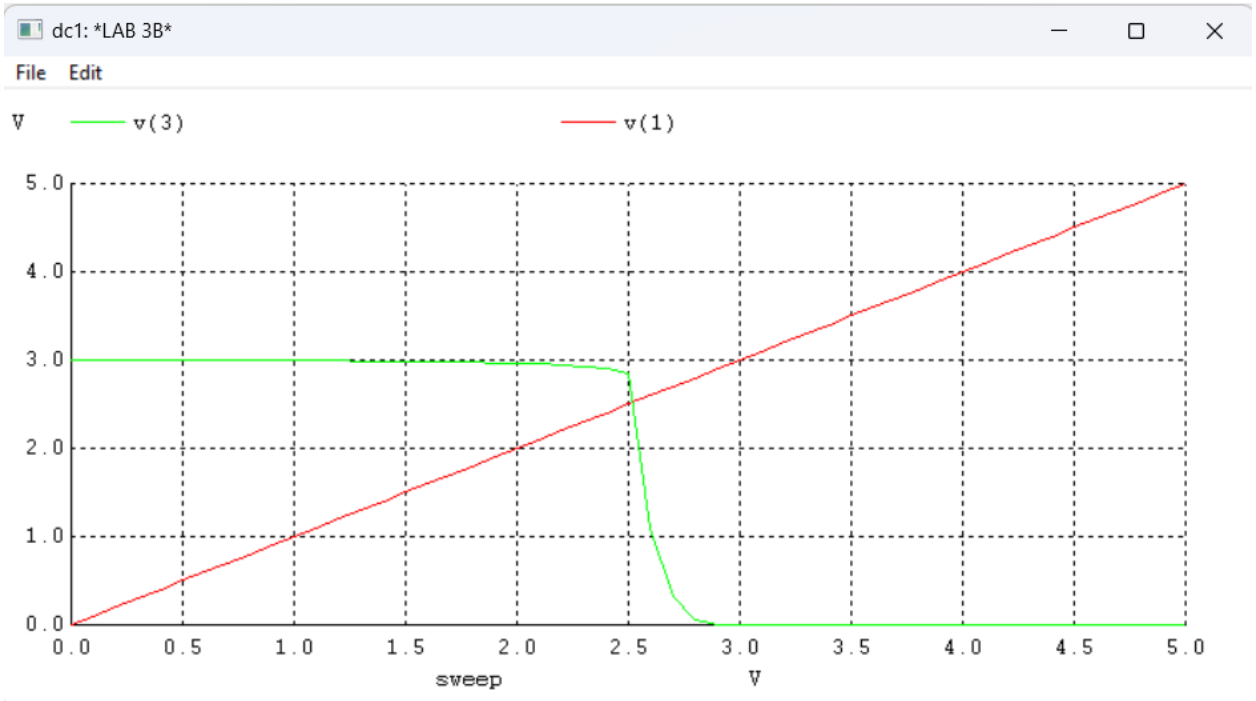
```
*LAB 3E*
Vdd 11 0 dc 3V
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
M1 8 1 6 6 nmod w=100u l=10u
M2 6 2 0 0 nmod w=100u l=10u
M3 6 3 0 0 nmod w=100u l=10u
M4 8 4 7 7 nmod w=100u l=10u
M5 7 5 0 0 nmod w=100u l=10u
M6 11 1 9 9 pmod w=200u l=10u
M7 11 2 10 10 pmod w=200u l=10u
M8 10 3 9 9 pmod w=200u l=10u
M9 9 4 8 8 pmod w=200u l=10u
M10 9 5 8 8 pmod w=200u l=10u
V1 1 0 pulse ( 0 3 0 0.1u 0.1u 10u 20u)
V2 2 0 pulse ( 0 3 0 0.1u 0.1u 20u 40u)
V3 3 0 pulse ( 0 3 0 0.1u 0.1u 40u 60u)
V4 4 0 pulse ( 0 3 0 0.1u 0.1u 60u 80u)
V5 5 0 dc 0V
.tran 10u 320u 20u
.control
run
plot V(8) V(1) V(2) V(3) V(4) V(5)
.endc
.end
```

Output:

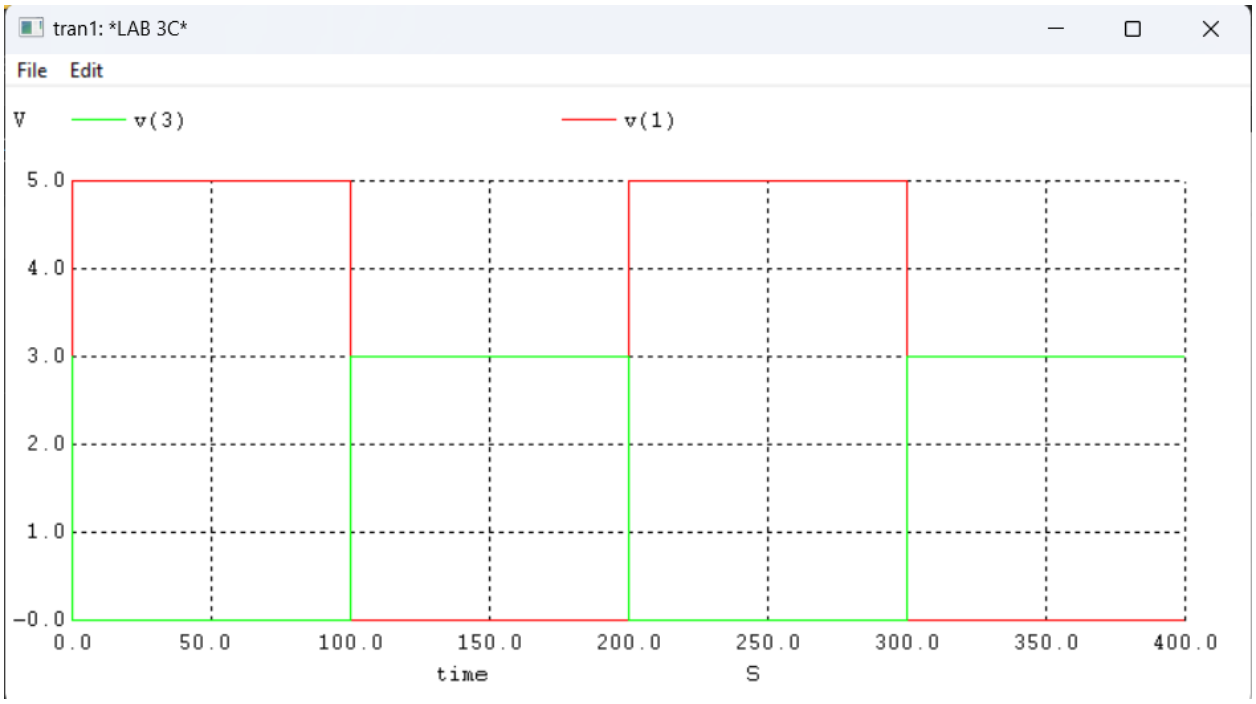
I. INVERTER:



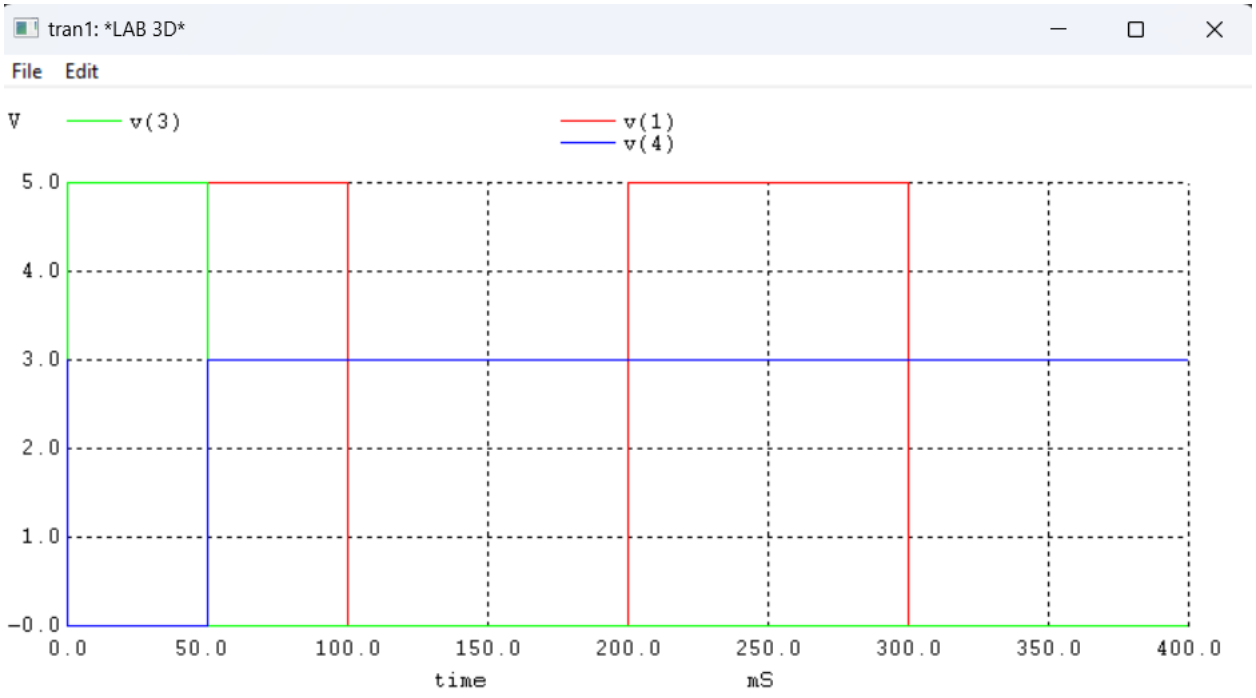
II. INVERTER FOR CHANGE IN INPUT FROM 0 TO 5V LINEARLY:



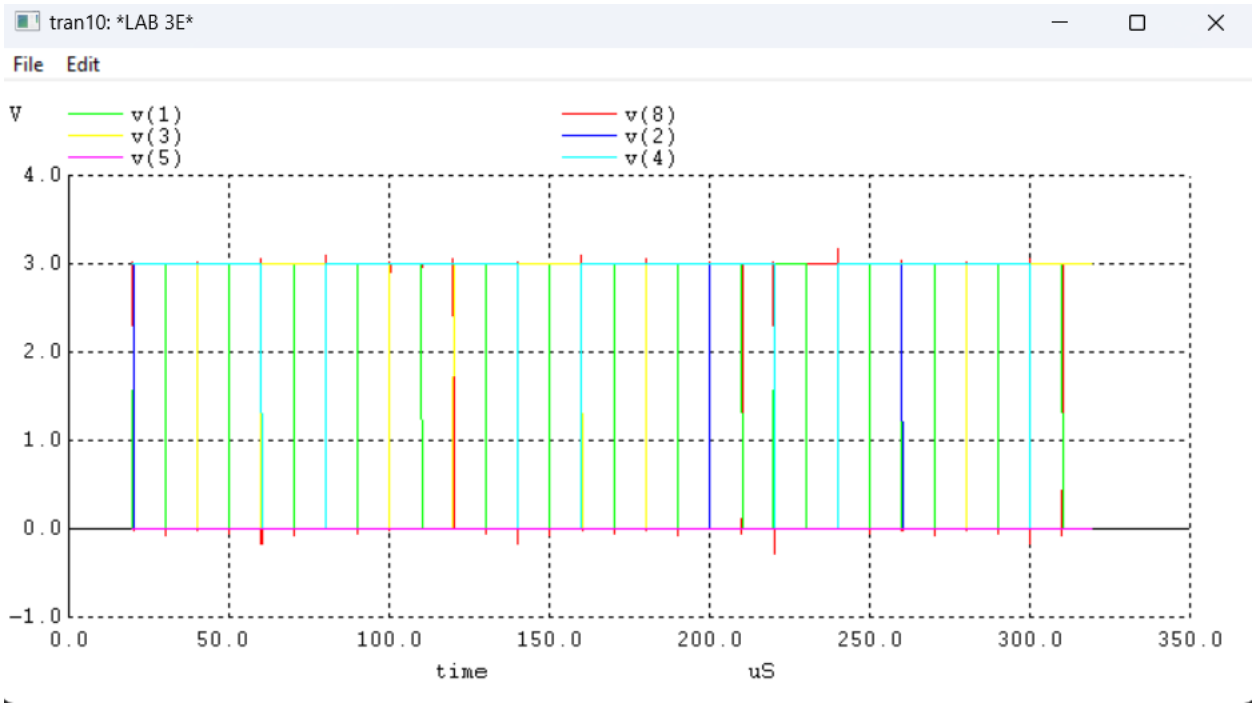
III. NOR GATE:



III. AND GATE:



IV. Y = ~(A(B + C) + DE):



Result/ Conclusion:

CMOS circuit design in WinSpice involves creating a netlist, simulating the circuit, and analyzing the results to ensure the design meets the required specifications. Understanding CMOS basics and simulation techniques is crucial for successful digital circuit design.