INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, NAGPUR

Department of Electronics and Communication Engineering

Academic Session: JULY to DECEMBER (Odd Semester)

CMOS LAB (ECL-312)

V Semester ECE-IoT

Date:05/08/2024

Experiment No.2(B)

Aim: To plot V-I characterstics of PMOS devices.

Software Required: WinSpice.

Theory:

A PMOS (P-channel Metal-Oxide-Semiconductor) transistor is another type of MOSFET, where the majority carriers are holes. The operation of a PMOS transistor is similar to that of an NMOS, but the polarity of the voltages and the type of charge carriers are reversed.

It operates in three regions: Cutoff, Linear (Ohmic), and Saturation.

1. **Cutoff Region:**
   - The PMOS is OFF, and no current flows from drain to source (ID = 0). This occurs when the gate-source voltage (VSG) is less than the threshold voltage (Vth). Since the voltages are negative in a PMOS, this means that the gate-source voltage (VSG) must be less negative than the threshold voltage for the PMOS to be in the cutoff region.
2. **Linear (Ohmic) Region:**
   - The PMOS is ON, and the drain current (ID) increases linearly with an increase in VSD, behaving like a resistor. This occurs when VSG > Vth and VSD < (VSG - Vth). For PMOS, VSG and VSD are typically negative, and Vth is a negative value as well.
3. **Saturation Region:**
   - The PMOS is fully ON, and the drain current (ID) is relatively independent of VSD, depending primarily on VSG. This occurs when VSD ≥ (VSG - Vth). In this region, the current is determined by the gate-source voltage (VSG), and the transistor acts like a current source.

Codes:

I. With respect to change in Vg:

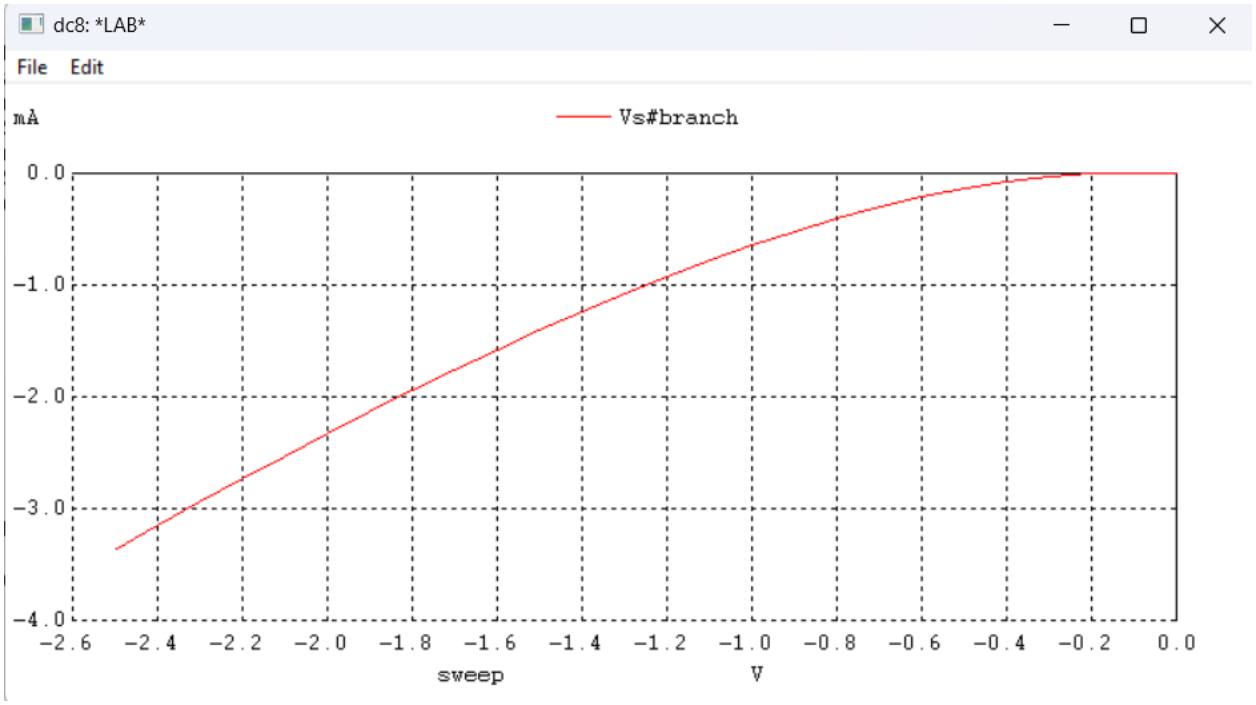
```
*LAB*
Vd 3 0 dc -3V
Vg 1 0 dc -2V
Vs 3 2 dc 0V
.model pmod pmos level=54 version=4.7
M1 2 1 0 0 pmod w=0.1mm l=0.01mm
.dc Vg 0 -2.5 -0.1
.control
run
plot i(Vs)
.endc
.end
```

II. Change in Vg for each step of Vd:

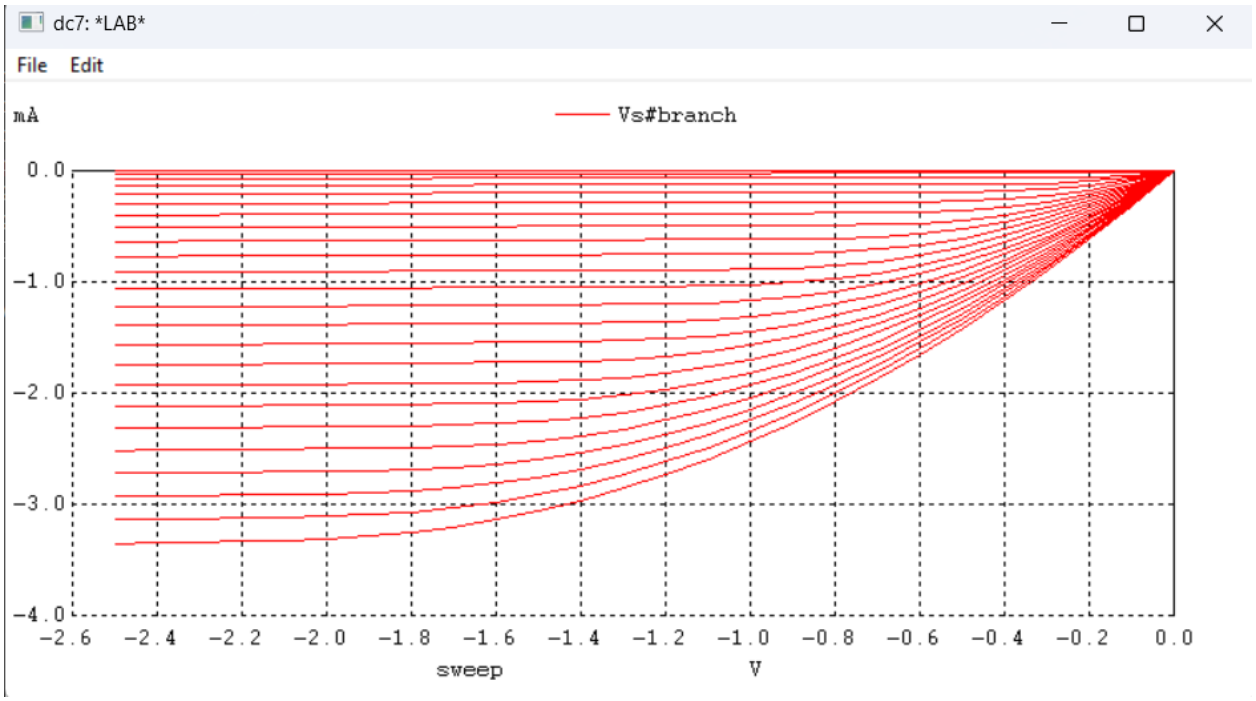
```
*LAB*
Vd 3 0 dc -3V
Vg 1 0 dc -2V
Vs 3 2 dc 0V
.model pmod pmos level=54 version=4.7
M1 2 1 0 0 pmod w=0.1mm l=0.01mm
.dc Vd 0 -2.5 -0.1 Vg 0 -2.5 -0.1
.control
run
plot i(Vs)
.endc
.end
```

Output:

I. With respect to change in Vg:



II. Change in Vg for each step of Vd:



Result/ Conclusion:

By plotting the V-I characteristics using WinSpice, you can visualize the different regions of operation for the PMOS transistor and better understand its behavior under varying conditions. This understanding is crucial for designing and analyzing circuits that utilize PMOS transistors.