INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, NAGPUR

Department of Electronics and Communication Engineering
Academic Session: JULY to DECEMBER (Odd Semester)

CMOS LAB (ECL-312)
V Semester ECE-IoT

Date:14/10/2024

Experiment No.7

Aim: To design the layout for a Full Adder using CMOS technology in Microwind and perform the necessary analysis.

Software Required: MICROWIND

Theory:

A 6T SRAM (Static Random Access Memory) cell is a fundamental memory unit used in digitalsystems for data storage. It is composed of six transistors: four transistors forming two cross- coupled inverters and two access transistors that allow the cell to be read and written.

The 6T SRAM cell operates as follows:

1. **Cross-coupled Inverters:** The two inverters store a bit of data, either 0 or 1, by holdingthe voltage levels in the internal nodes (Q and Q').
2. **Access Transistors:** These transistors control the access to the storage nodes during the read and write operations. When the wordline (WL) is high, the access transistors connectthe storage nodes to the bitlines (BL and BLB), allowing for data access.

The Boolean equations for the 6T SRAM are:

- **Q = (WL · (BL' · Q' + BL · Q))**
- **Q' = (WL · (BL · Q + BL' · Q'))**

Where:

- **WL** is the wordline that enables reading and writing.
- **BL** and **BLB** are the bitlines.
- **Q** and **Q'** are the storage nodes, holding the data.

The layout design involves placing PMOS and NMOS transistors in the correct configurationand ensuring proper routing of diffusion, polysilicon, and metal layers to achieve the SRAM functionality.

Netlist:

- **WRITE MODE**

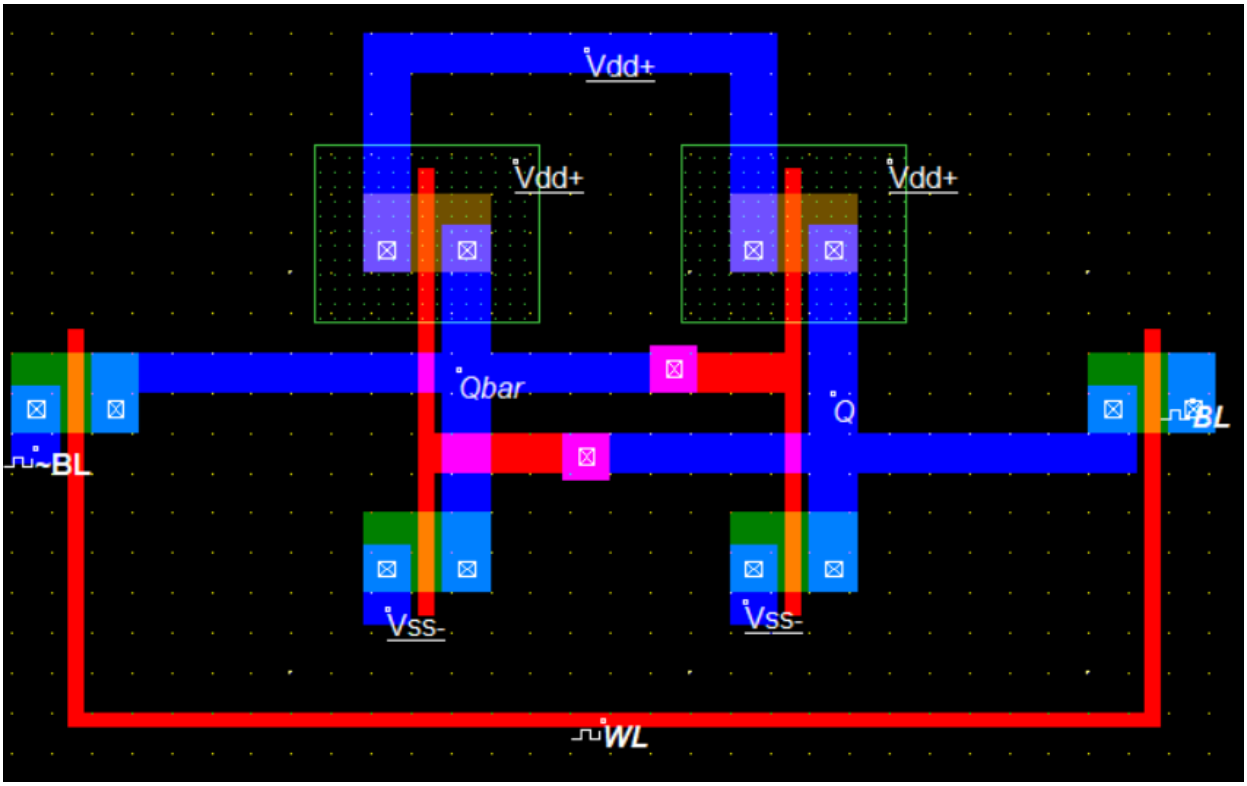
```
**6T SRAM WRITE MODE**
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
.subckt inverter 1 2 3
M1 3 1 0 0 pmod w=100u l=10u
M2 3 1 2 2 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
.ends
Vdd 2 0 dc 5
Vwl 6 0 dc 5
Vbit 7 0 dc 5
Vbitbar 8 0 dc 0
Xq 1 2 3 inverter
Xqbar 3 2 1 inverter
M5 7 6 3 3 pmod w=100u l=10u
M6 8 6 1 1 pmod w=100u l=10u
.tran 0.1m 400m
.control
run
plot v(7) v(8) v(3) v(1)
.endc
.end
```

- **READ MODE**

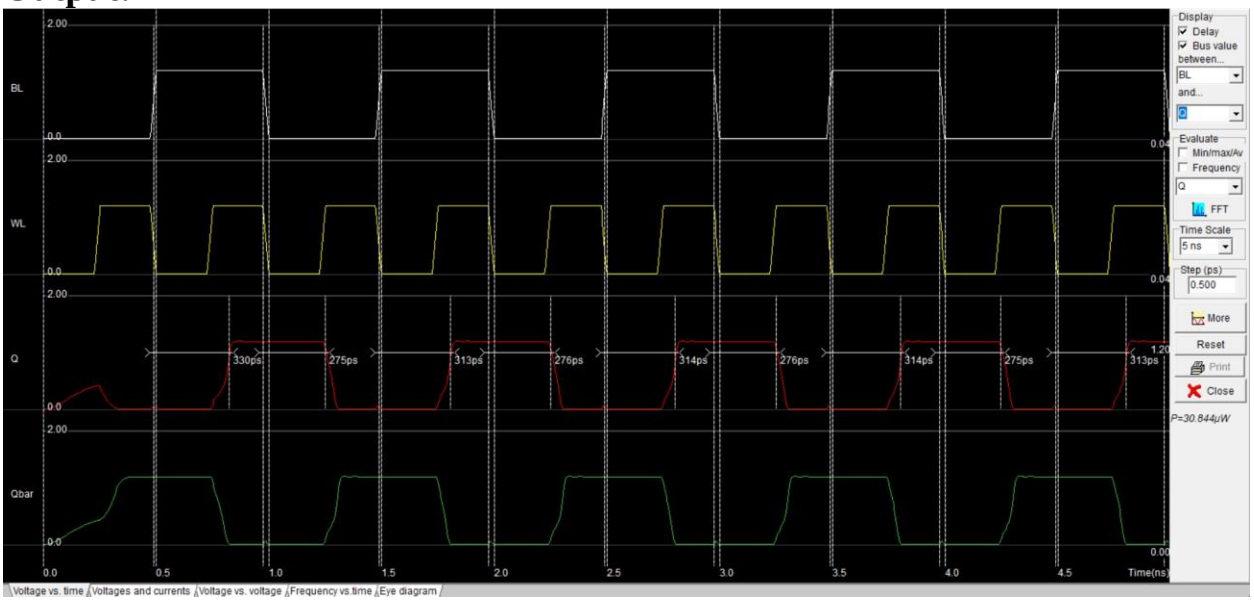
```
**6T SRAM READ MODE**
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
.subckt inverter 1 2 3
M1 3 1 0 0 pmod w=100u l=10u
M2 3 1 2 2 nmod w=100u l=10u
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7
.ends
Vdd 2 0 dc 5
Vwl 6 0 dc 5
Vq 3 0 dc 5
Vqbar 1 0 dc 0
Xq 1 2 3 inverter
Xqbar 3 2 1 inverter
M5 7 6 3 3 nmod w=100u l=10u
M6 8 6 1 1 nmod w=100u l=10u
C7 7 0 1u IC=2.5
C8 8 0 1u IC=2.5
.tran 0.1m 400m
.control
run
plot v(7) v(8) v(3) v(1)
.endc
.end
```

Layouts:

6T SRAM CELL :



Output:



VOLTAGE TIME ANANLYSIS

Result/ Conclusion:

The CMOS layout design for the 6T SRAM cell was successfully implemented in Microwind. The design process involved creating the necessary cross-coupled inverters and access transistorsto store and retrieve data. Proper routing of the metal layers ensured correct functionality of the SRAM cell.

The layout was validated using Design Rule Checking (DRC) and Layout vs. Schematic (LVS)verification to ensure compliance with design rules. Simulation results confirmed that the 6T SRAM cell functions correctly, with stable storage nodes (Q and Q') and proper read/write operations, demonstrating the effective application of CMOS layout design techniques in Microwind.