INDIAN INSTITUTE OF INFORMATION TECHNOLOGY, NAGPUR

Department of Electronics and Communication Engineering

Academic Session: JULY to DECEMBER (Odd Semester)

CMOS LAB (ECL-312)

V Semester ECE-IoT

Date:12/08/2024

Experiment No.5

Aim: To make Layout of the following Boolean Function and perform their analysis.

a) Inverter

b) Three Input NAND gate

c) ((A+B+C).D)'

Software Required: MICROWIND

Theory:

In CMOS layout design, the transistors are represented geometrically using layers of materials that correspond to different elements of the transistor. These layers include:

1. **Diffusion Layers (n-diffusion and p-diffusion):** Represent the source and drain regions of transistors.
2. **Gate Poly Layer (Polysilicon):** Forms the gate terminal of each transistor.
3. **Metal Layers (M1, M2, etc.):** Used to make the interconnections between the source, drain, and gate terminals.
4. **Well Layers (p-well, n-well):** Form the substrate regions that house the transistors.

Netlists:

I. INVERTER :

```
*INVERTER*
 Vdd 2 0 dc 3V
.model nmod nmos level=54 version=4.7
 M1 3 1 0 0 nmod w=100u l=10u
.model pmod pmos level=54 version=4.7
M2 3 1 2 2 pmod w=100u l=10u V1 1 0 pulse( 0 5 0 0 0 100 200)
.tran 0.1 400
.control
run
 plot V(1) V(3)
 .endc
 .end
```

II. THREE INPUT NAND GATE :

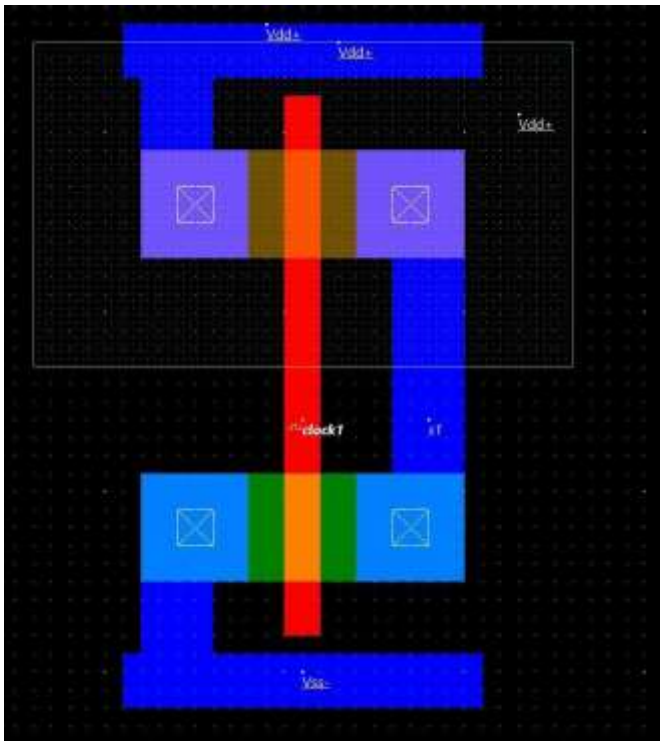
```
**3-INPUT NAND**
V1 1 0 DC 0V PULSE(0 4V 0 0.1N 0.1N 1NS 2NS)
V2 2 0 DC 0V PULSE(0 4V 0 0.1N 0.1N 2NS 4NS)
V3 3 0 DC 0V PULSE(0 4V 0 0.1N 0.1N 4NS 8NS)
VDD 5 0 DC 5V
.model N1 nmos level=49 version=3.3.0
.model P1 pmos level=49 version=3.3.0
MP1 4 1 5 5 P1 W=360U L=180N
MP2 4 2 5 5 P1 W=360U L=180N
MP3 4 3 5 5 P1 W=360U L=180N
MN1 4 1 6 6 N1 W=360U L=180N
MN2 6 2 7 7 N1 W=360U L=180N
MN3 7 3 0 0 N1 W=360U L=180N
.TRAN 0.1NS 8NS
.CONTROL
RUN
PLOT V(1) V(2) V(3) V(4)
.ENDC
.END
```

III. ~((A+B+C).D)

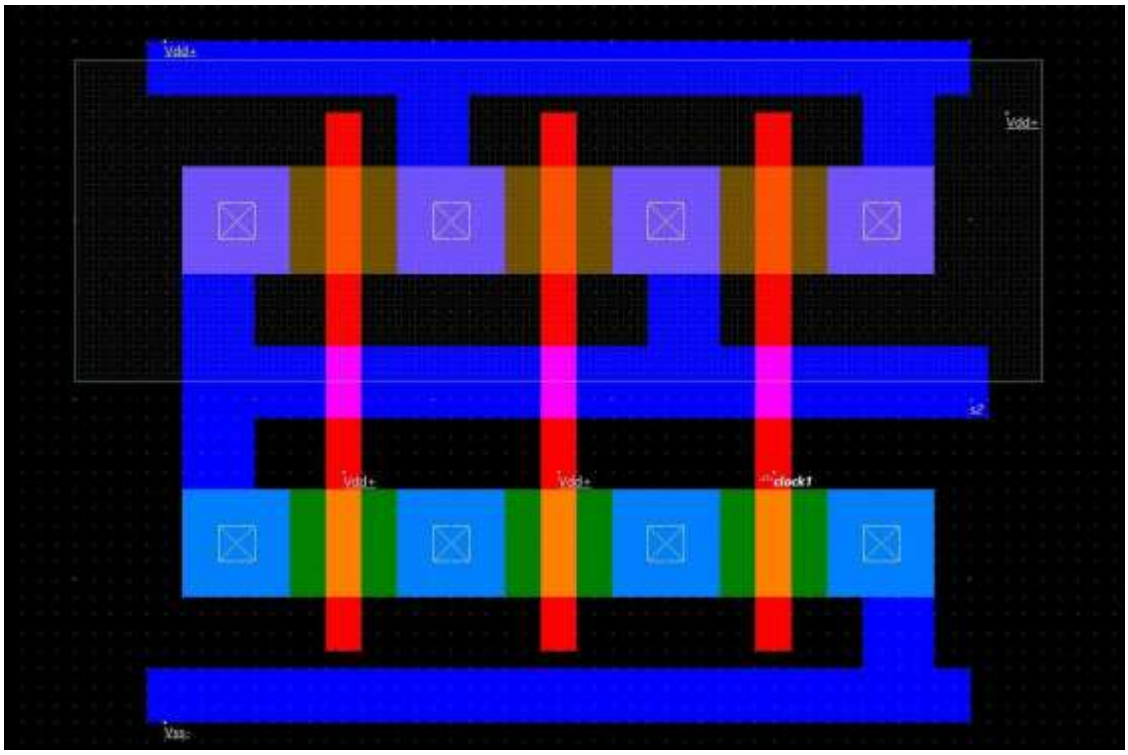
```
*** Y = (A+B+C).D ***
.model nmod nmos level=54 version=4.7
.model pmod pmos level=54 version=4.7

Vdd 5 0 dc 5

Va 1 0 pulse(0 5 0 0 0 50m 100m)
Vb 2 0 pulse(0 5 0 0 0 100m 100m)
Vc 3 0 pulse(0 5 0 0 0 200m 400m)
Vd 4 0 dc 5


M1 6 4 0 0 nmod w=100u l=10u
M2 7 1 6 6 nmod w=100u l=10u
M3 7 2 6 6 nmod w=100u l=10u
M4 7 3 6 6 nmod w=100u l=10u

M5 7 3 8 8 pmod w=200u l=10u
M6 8 2 9 9 pmod w=200u l=10u
M7 9 1 5 5 pmod w=200u l=10u
M8 7 4 5 5 pmod w=200u l=10u

.tran 0.1m 800m
.control
run
plot v(7) v(1) v(2) v(3) v(4)
.endc
.end
```

Layouts:

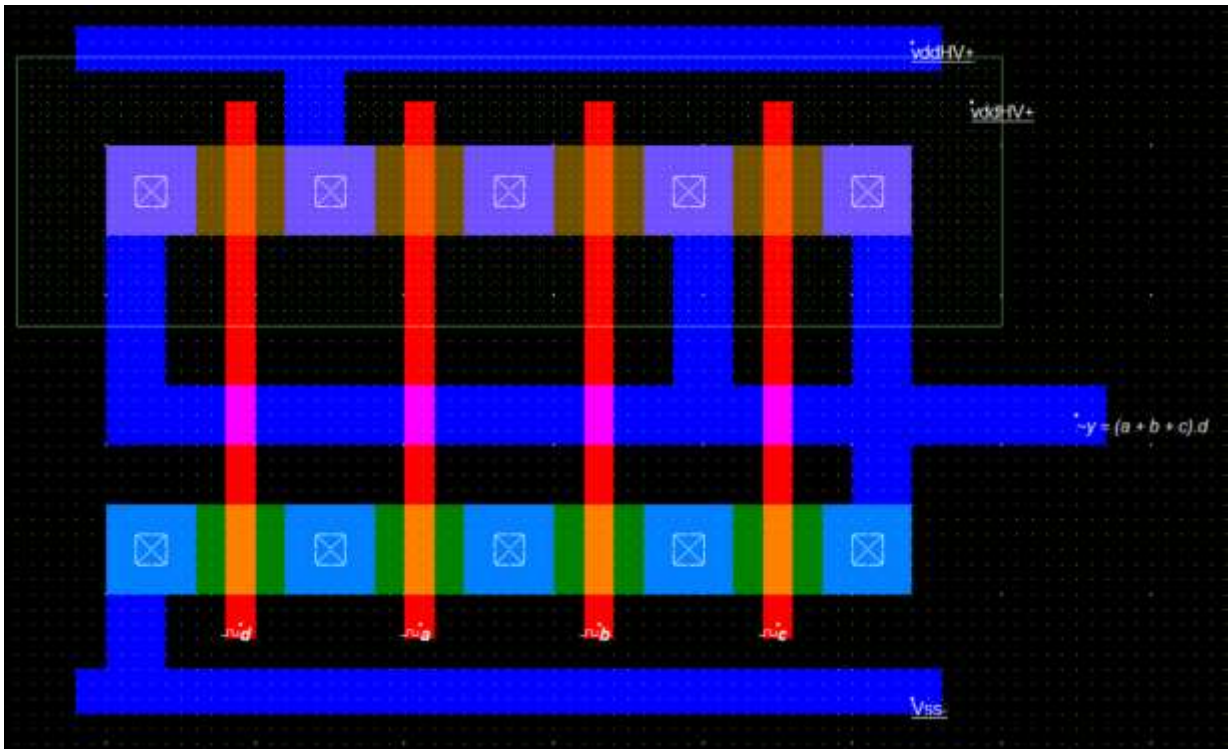
I. INVERTER :



II. THREE INPUT NAND GATE :

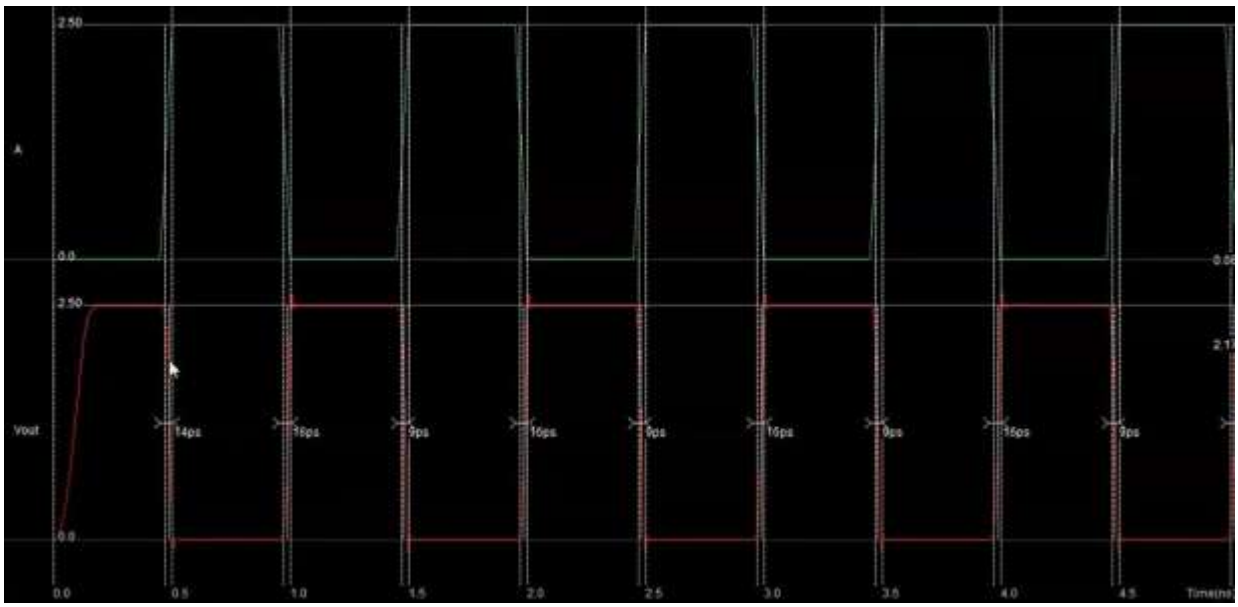


III. ((A+B+C).D)



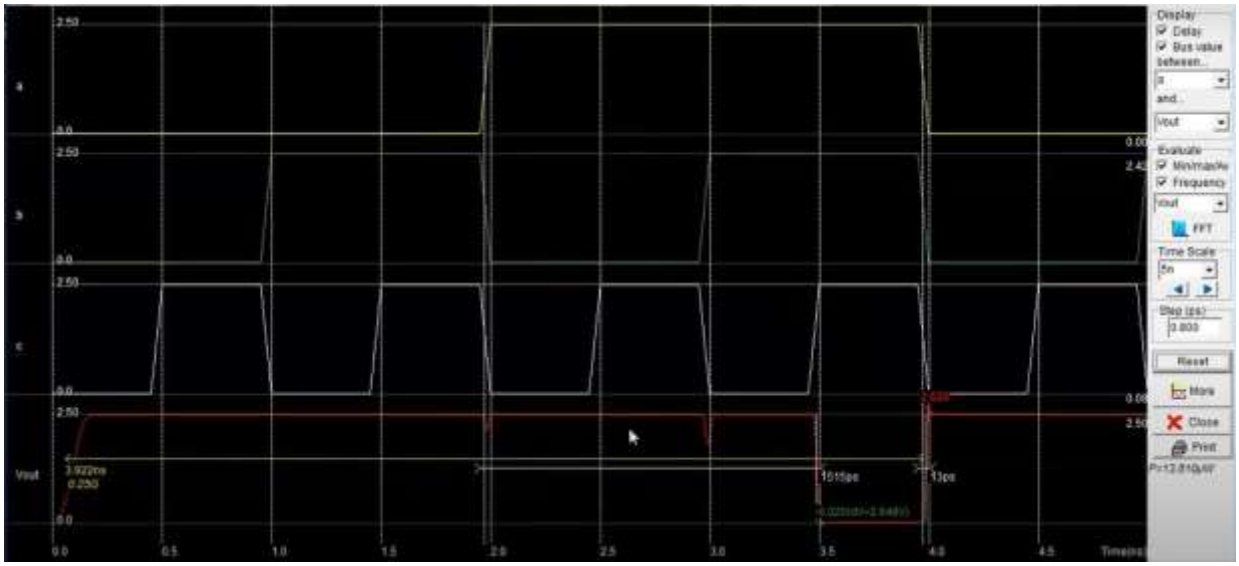
Output:

I. INVERTER



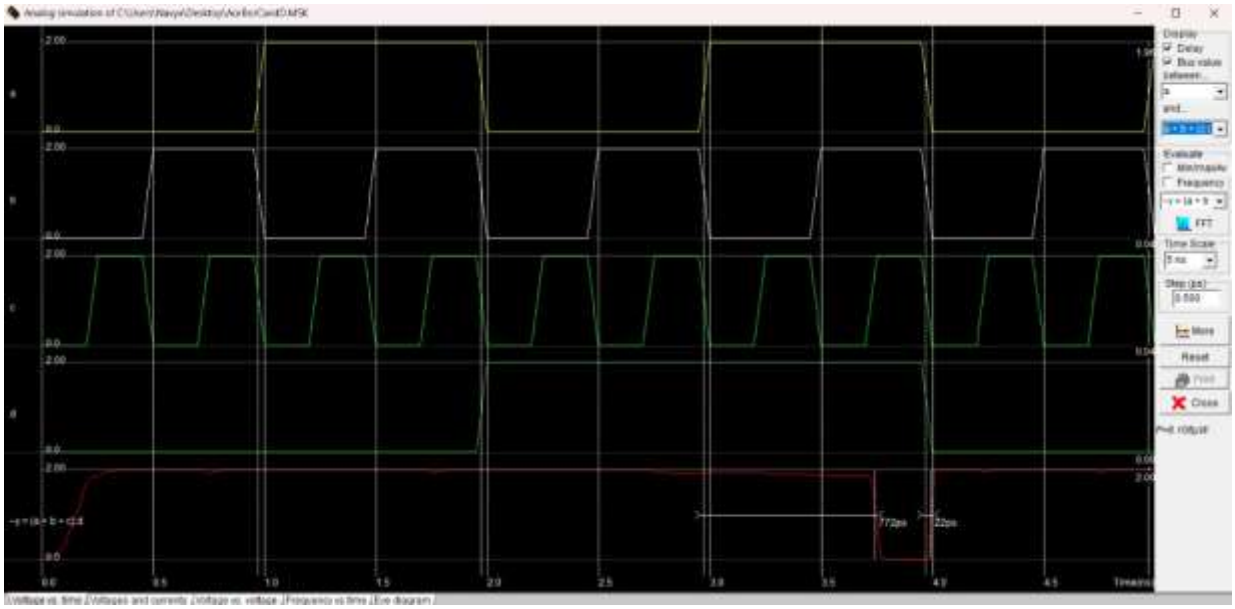
VOLTAGE TIME ANANLYSIS

II. THREE INPUT NANAD GATE



VOLTAGE TIME ANANLYSIS

III. ((A+B+C).D)’



VOLTAGE TIME ANALYSIS

Result/ Conclusion:

The CMOS layout design for the Boolean functions—Inverter, Three-Input NAND Gate, and ~((A + B + C).D))—involved translating their logical schematics into physical layouts using Microwind. The process included placing transistors, making the necessary connections, and routing metal layers.

The layouts were validated through Design Rule Checking (DRC) and Layout vs. Schematic (LVS) checks. Simulations confirmed the proper functionality of the designs, demonstrating the successful application of CMOS layout techniques in Microwind.