PROJECT REPORT ON CHARGE PUMP CIRCUIT

A report submitted for the partial fulfilment of the requirements of the course

ECL-312: CMOS DESIGN

Submission date: 13TH November 2024

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1. INTRODUCTION:

A CMOS charge pump is a type of electronic circuit that generates higher output voltages from a lower supply voltage. Charge pumps are widely used in integrated circuits where a small chip area and low power consumption are required. These circuits are commonly applied in non-volatile memory, LCD drivers, flash memories, and various power management systems that need voltages higher than the supply voltage.

This project explores the design and functionality of a five-stage CMOS charge pump that (The Dickson Charge pump circuit) can step up an input voltage to a higher output voltage by using a combination of capacitors, MOSFET switches, and clock signals. The circuit utilizes two-phase clock signals to charge and discharge capacitors, thus transferring and boosting the voltage across multiple stages.

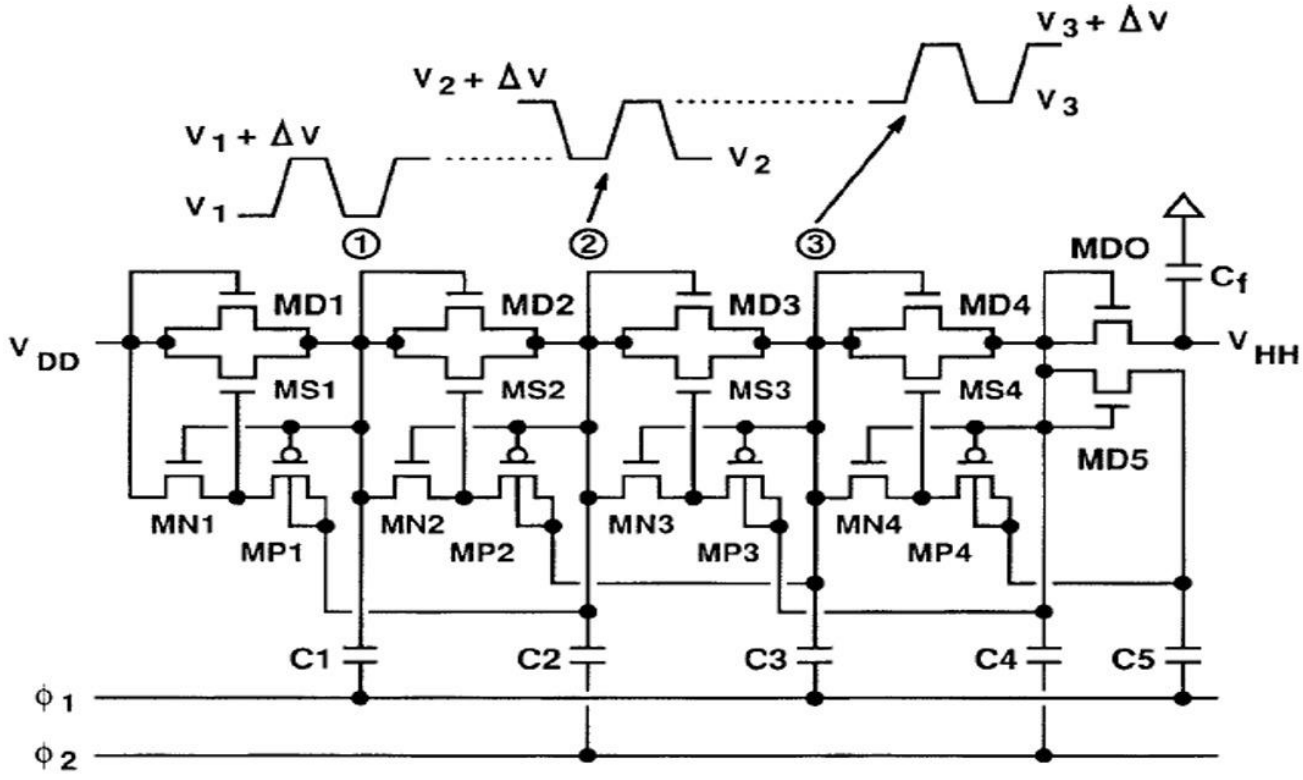

FIG 1: The Dickson Charge pump circuit

2. WORKING:

The CMOS charge pump circuit operates by using multiple stages of capacitors and MOSFET switches to successively increase the voltage at each stage. The main components in each stage are:

MOSFET Switches: Each stage contains NMOS and PMOS transistors that act as switches to control the flow of charge.
Capacitors: Each stage capacitor is charged and then discharged to transfer energy to the next stage.

The charge pump circuit works as follows:

Clock Phases: Two clock signals ($\phi 1$ and $\phi 2$) drive the circuit. These clocks are complementary, with one clock signal going high while the other is low. This alternating pattern is essential for transferring charge from one stage to the next.

Stage Operation: Each stage comprises an NMOS-PMOS switch combination and a capacitor. When $\phi 1$ is high, certain transistors allow the capacitor in that stage to charge. When $\phi 2$ is high, charge is transferred from one capacitor to the next, raising the voltage level at each stage.

Voltage Boosting: The input voltage is boosted incrementally with each stage due to the cumulative effect of the charge-pump stages. In each stage, a small voltage increment (ΔV) is added, resulting in a significantly higher voltage at the output after all stages.
Output Filtering: At the final stage, a capacitor (Cf) is added to stabilize and filter the output, reducing ripple and producing a steady high-voltage DC output.

CHARGE PUMP FOR PLL APPLICATION:

In a Voltage-Controlled Oscillator (VCO) within a Phase-Locked Loop (PLL), charge pump circuits adjust the control voltage that sets the VCO's frequency. When the VCO's output phase doesn't match a reference signal, the phase detector directs the charge pump to add or remove charge on a capacitor, adjusting the control voltage. This change tunes the VCO frequency, bringing it in sync with the reference. Once matched, the charge pump keeps the control voltage steady, stabilizing the VCO frequency. This makes charge pumps crucial for precise frequency control in PLL-based systems.

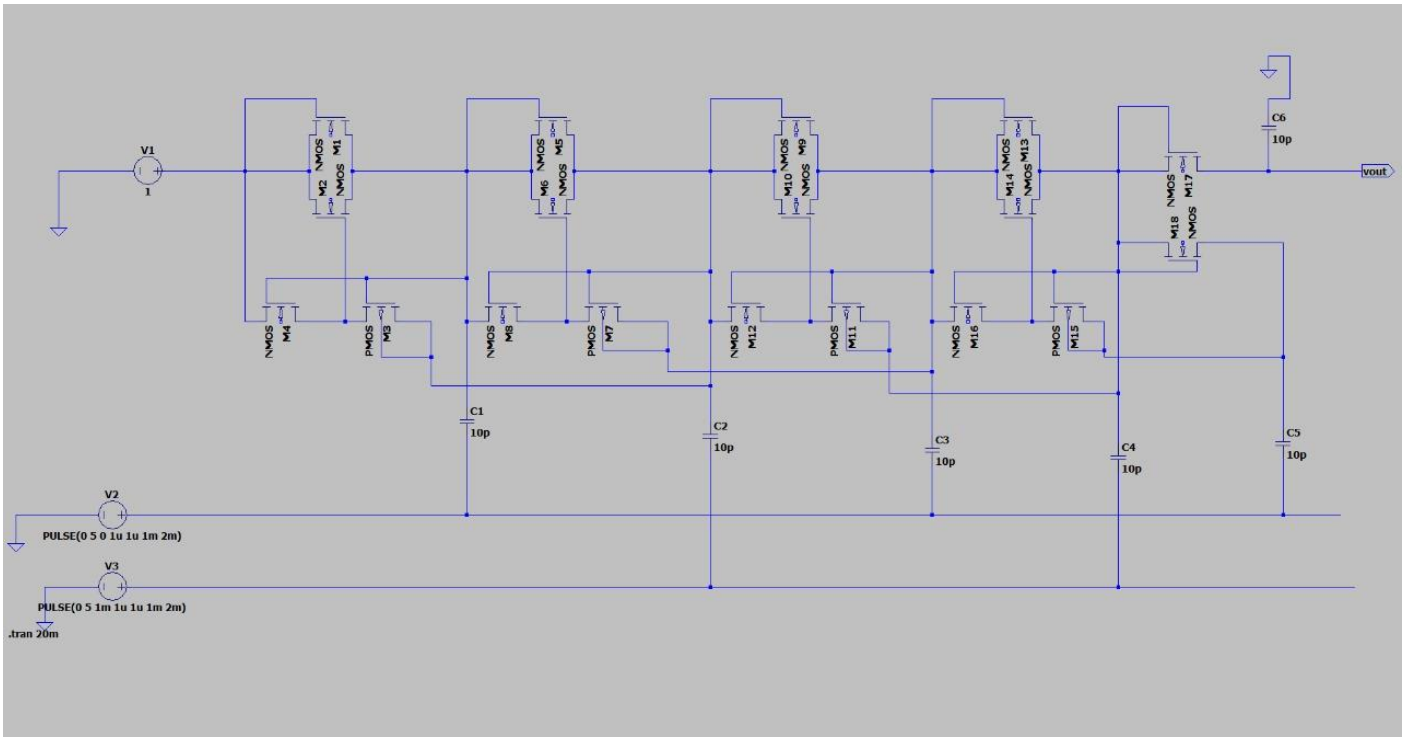

FIG 2: Schematic design of Charge pump circuit

Description:

When ϕ_1 goes high, capacitor C_1 charges up to V_9 through the diode-connected transistor MD_1. As ϕ_1 goes low and ϕ_2 goes high, MS_1 connects C_1 to the next stage, transferring the stored charge and raising the voltage to $V_1 + \Delta V$. This increased voltage is passed to the next stage. In subsequent stages (C_2 to C_5, MS_2 to MS_4, MD_2 to MD_5), each capacitor (C_2, C_3, etc.) continues this process, incrementally boosting the voltage by ΔV at each stage. The charge transfer switches MS_2, MS_3, etc., are controlled by pass transistors MN_2, MP_2, etc., to allow charge transfer from one capacitor to the next without reverse flow. Diode-connected transistors MD_2, MD_3, etc., ensure that charge flows only in the forward direction, further increasing the voltage step-by-step. After the last stage (stage 5), the voltage reaches the output terminal VHH. Finally, capacitor Cf at the output terminal smooths out the high voltage output by filtering any residual ripple.

3. LAYOUT DESIGN:

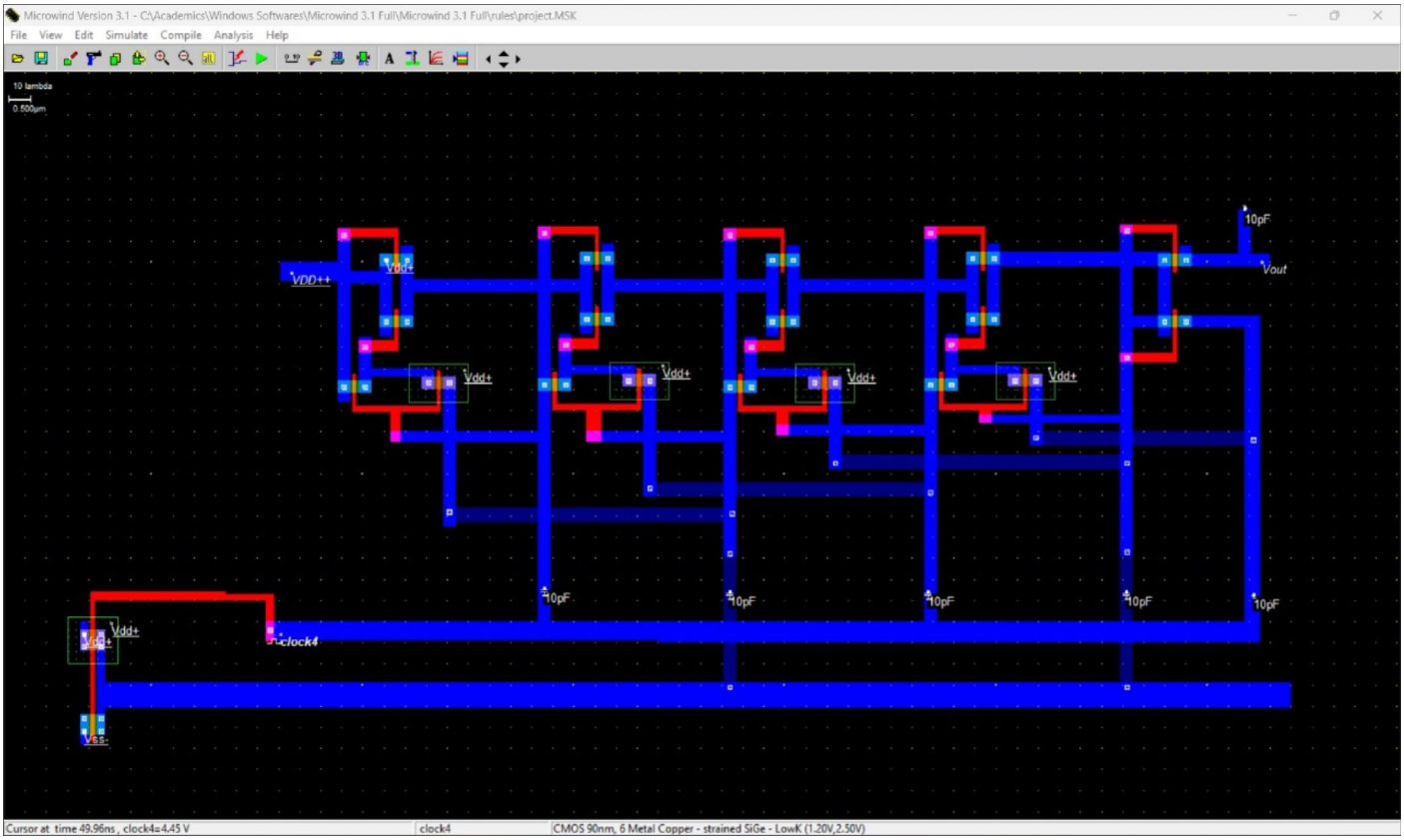

FIG 3: Layout design on Microwind software

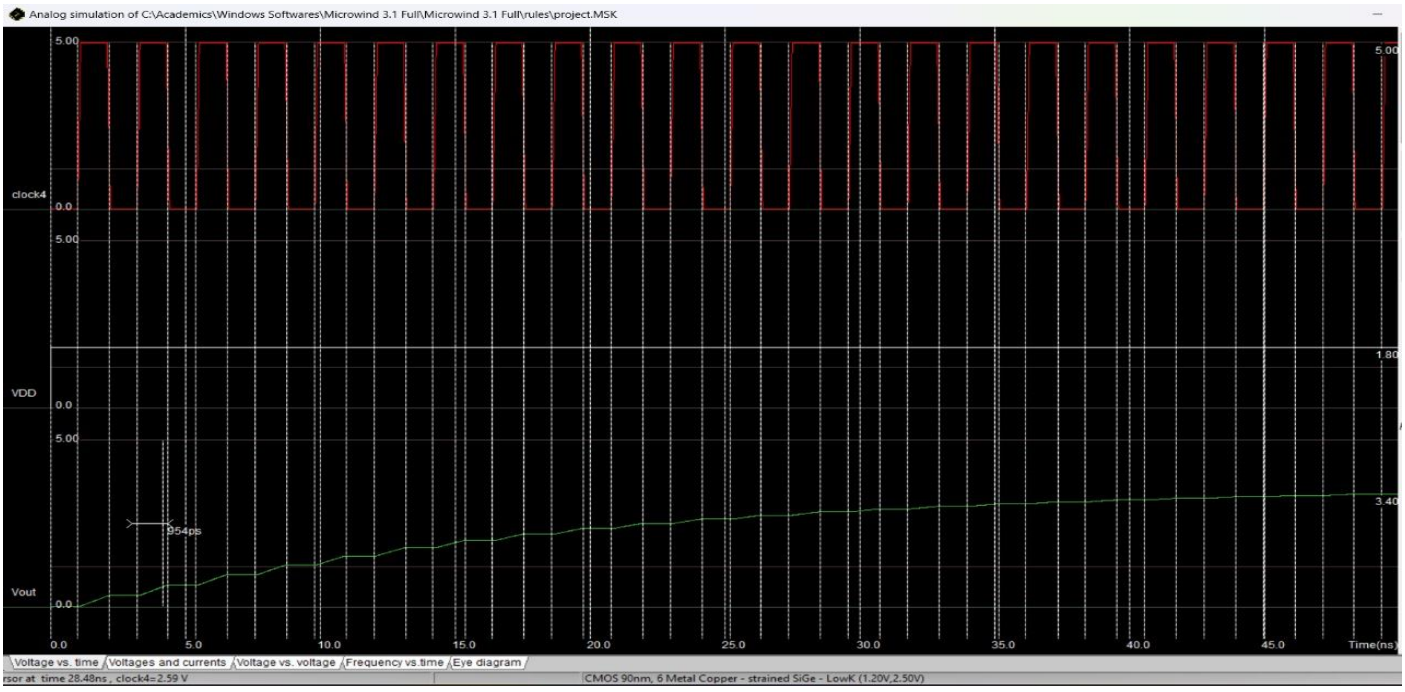

FIG 4: Microwind software output

4. NETLIST:

*charge pump circuit

```
VDD 1 0 DC 1.20
Vclock1 7 0 DC 0 PULSE(0.00 5.00 1.00N 0.10N 0.10N 1.00N 2.20N)
V14 14 0 DC 1.80V

* Switch Transistors
MN1 7 16 9 0 N1  W= 0.30U L= 0.10U
MN2 7 17 8 0 N1  W= 0.30U L= 0.10U
MN3 7 7 13 0 N1  W= 0.30U L= 0.10U
MN4 7 18 10 0 N1  W= 0.30U L= 0.10U
MN5 14 14 7 0 N1  W= 0.30U L= 0.10U
MN6 14 11 7 0 N1  W= 0.30U L= 0.10U
MN7 14 19 11 0 N1  W= 0.30U L= 0.10U
MN8 0 7 7 0 N1  W= 0.50U L= 0.10U
MP1 8 17 7 1 P1  W= 0.30U L= 0.10U
MP2 9 16 7 1 P1  W= 0.30U L= 0.10U
MP3 10 18 7 1 P1  W= 0.30U L= 0.10U
MP4 11 19 7 1 P1  W= 0.30U L= 0.10U
MP5 1 7 7 1 P1  W= 0.50U L= 0.10U

* charge-transfer capacitors
C1 13 0 10pF
C2 7 0 10pF
C3 7 0 10pF
C4 7 0 10pF
C5 7 0 10pF
C6 7 0 10pF


* n-MOS low leakage
.MODEL N1 NMOS LEVEL=14 VTHO=0.28 U0=0.060 TOXE= 1.2E-9 LINT=0.015U

* p-MOS low leakage
.MODEL P1 PMOS LEVEL=14 VTHO=-0.32 U0=0.027 TOXE= 1.2E-9 LINT=0.015U

* Transient analysis

.control
tran 0.1N 50.00N
print  V(13) V(7) V(14)
plot  V(13) V(7) V(14)
.endc
.END
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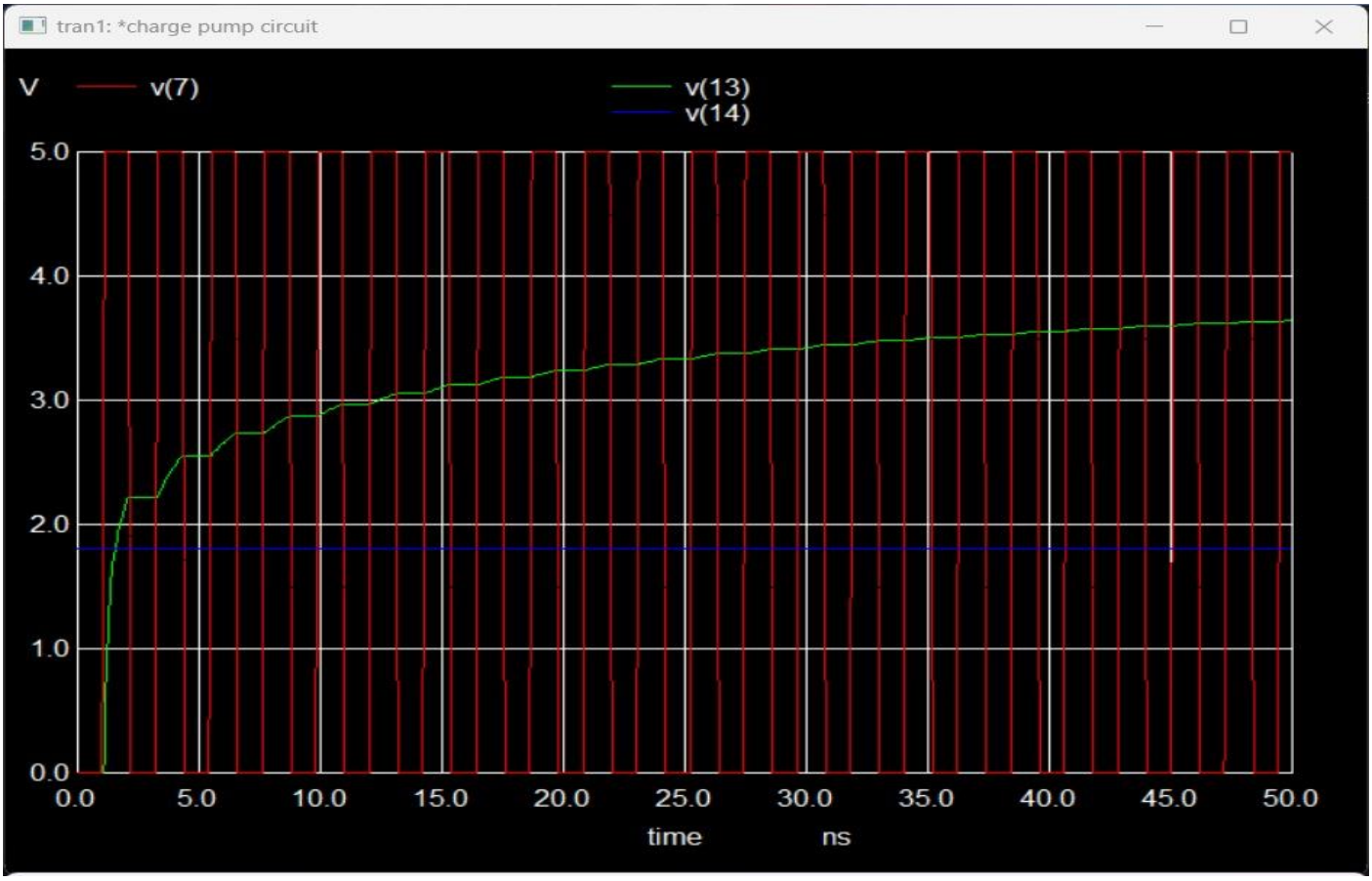

FIG 5: NGSpice software output

5. Features:

The CMOS charge pump circuit designed in this project has several notable features:

Low Power Consumption: Using CMOS technology enables lower power dissipation, making the circuit ideal for battery-operated and portable devices.

High Efficiency: The design minimizes energy loss, especially in low-power applications where efficiency is critical.

Scalability: The circuit can be extended with more stages to achieve even higher output voltages, depending on application requirements.

Compact Design: CMOS technology allows for high integration density, making this circuit suitable for embedding within ICs.

Dual Clock Operation: The use of two clock phases ensures efficient charge transfer and minimizes switching losses, optimizing performance.

6. Conclusion:

The CMOS charge pump is a versatile and efficient circuit that provides high-voltage output from a low-voltage supply, essential for a wide range of applications in modern electronics. This project demonstrates the functionality of a five-stage CMOS charge pump, showing how charge is transferred and boosted through the stages using MOS transistors and capacitors. With continued advancements in CMOS technology, charge pumps are expected to find even broader applications in power management, IoT devices, and energy-harvesting systems.

References

https://www.researchgate.net/publication/4106174_High_voltage_charge_pump_using_standard_CMOS_technology

https://ieeexplore.ieee.org/document/7732062