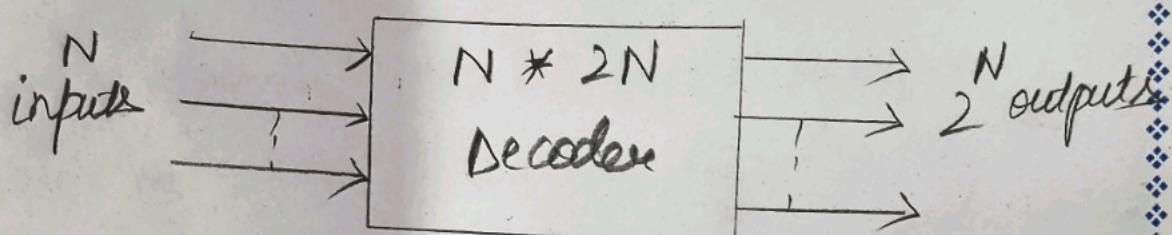


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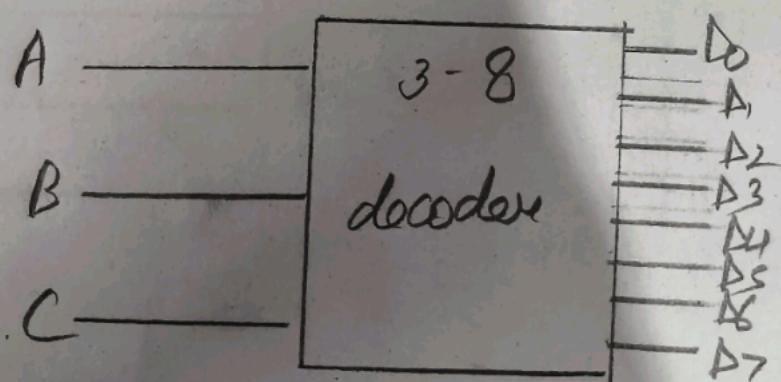
Experiment No 3

Objective : Implementing 3-8 line Decoder

Theory : The combinational circuit that change the binary information into 2^N output lines known as Decoder



3 to 8 Line decoder : It is known as Binary to Octal Number Decoder. In a 3 to 8 line decoder, there is a total of eight outputs, ie $B_0, B_1, B_2, B_3, B_4, B_5, B_6, B_7$ and three inputs A, B and C. This circuit has an enable input (E), when enable E is set to 1, one of these few outputs will be 1.



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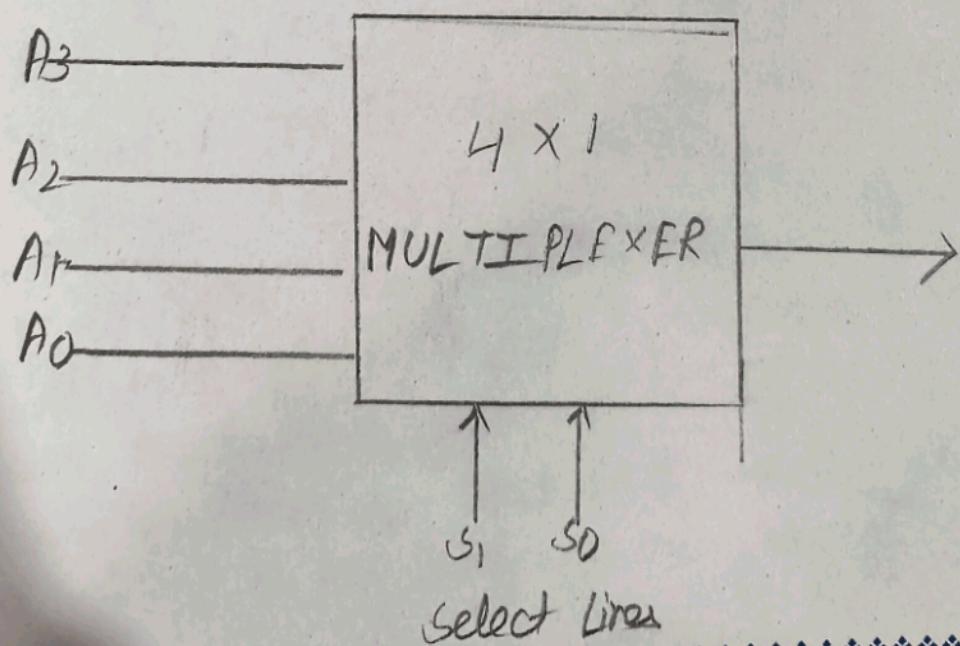
Experiment - 4

Objective: Implementing 4x1 and 8x1 MUX

Theory: A multiplexer is a combinational circuit that has 2^n input lines and output line. The binary information is received from the input lines and directed to the output line.

4x1 Multiplexer: In the 4x1 Multiplexer, there are four input ie A_0, A_1, A_2 and A_3 two selection line ie S_0 and S_1 and single output line ie

Block diagram



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Experiment - 5

Objective: Verify Excitation Table of various flip-flops.

Apparatus:- IC 7400 (NAND Gate), IC 7402 (HOR) IC 7404 (NOT), IC - 7486 (Ex-OR), connecting wires, breadboard.

Theory: The excitation table of the SR flip flop can be constructed from the information available in the truth table.

From the truth table, we can observe that when the present state is $Q_n = 0$, the next state becomes $Q_{n+1} = 0$ for two input values $S=0, R=0$ and $S=0, R=1$. From this we can say that for state transition from $Q_n = 0$ to $Q_{n+1} = 0$ the excitation of inputs required are $S=0$ and $R=0$ or 1. Since K has two values 0 and 1. It is denoted by as a don't care condition.

T flip flop:- The following figure shows the truth table of T flip flop from which the excitation table is derived.

Similarly, from the truth table, we can also observe when $T=1$, the state of the flip flop toggles.

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It is completed. Thus for the function of the state from either 0 to 1 or from 1 to 0, the excitation input is $T=1$.

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Experiment No. 1

Objective :- Design 8 bit I/O system with four 8-bit internal registers

Apparatus:

S.No	Component	Specification	Qty
1	D flip Flop	IC 7474	2
2	OR gate	IC 7432	1
3	IC Trainer		1
4	PATCH CORDS		15

Theory:- A register is capable of shifting its binary info in one or both direction is known as shift register. The logical configuration of shift register consist of a D flip-flop cascaded with output of one Flip Flop connected to input of next Flip-flop. All flip-flops receive common clock pulses which cause the shift in o/p of the flip flop.

Procedure:-

- 1- Connections are given as per circuit diagram
- 2- Logical inputs are given as per circuit diagram
- 3- Observe the output and verify the truth table

Result:- Verified 8 bit I/O system with four 8-bit internal registers

Objective - Design of a 8-bit Arithmetic logic Unit

Theory - The designing of 8-bit ALU using programming language. It includes writing, Compiling and simulating Verilog code in ModelSim a wireless platform

First, install Model Sim on a Window PC

- 1- Start Model Sim from desktop, we will see Model Sim 10.4 dialogue window.
- 2- Create a project by clicking 'Jumpstart the Welcome Screen'
- 3- Save your code from file menu
compiling / debugging project files
Select Compute \rightarrow Compile all options
- 4- The compilation result is shown on the main window
green tick is shown against each file name
which means there are no errors in the project.

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Truth Table

Input	Output
S ₁ S ₀	Y
0 0	A ₀
0 1	A ₁
1 0	A ₂
1 1	A ₃

Logical Expression For Y

$$Y = S_0' S_1' A_0 + S_1 S_0' A_1 + S_1 S_0 A_2 + S_1' S_0 A_3$$

8x1 Multiplexer

In the 8x1 Multiplexer, there are total eight inputs, A₀, A₁, A₂, A₃, A₄, A₅, A₆ and A₇ selection Lines ie S₀, S₁ and S₂ and single output ie Y

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Experiment 8

Objectives : Design the data path of a computer from its register transfer language description

Theory: Register Transfer Language, RTL is a powerful high level method of describing the architecture of a circuit, VHDL code and schematics are often created from RTL. A typical RTL statement will look like

$$A \cup B \rightarrow R_1 = R_2$$

For RTL we will use the following symbols

\rightarrow Register Transfer

$[]$ word Index

$>$ Bit index

$\leftarrow \rightarrow$ If then

$=$ Definition

$\#$ Concatenation

$\wedge \vee \times \text{OR}$ logical operators

$+ - * /$ Arithmetic operators

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Experiment - 9

Objective: Design the Control Unit of a Computer using either hardwiring or any C programming based on its Register Transfer Language description.

Theory: Control Unit is a part of the CPU which directs the operation of processor. It fetches internal instructions of the program from the main memory to the processor instruction register.

Types of Control Unit

- 1) Hardwired Control Unit: In this unit, the control signals that are important for instruction execution control are generated by specially designed hardwired logical circuits in which we cannot modify the signal generation.
- 2) Decoder of the Cicle: - A no of signals generated by the Control Signal generator matrix are sent back to input of the next control state generator. This matrix combines these signals with matrix. The timing unit based on the rectangular patterns usually applied by the quartz generator.

Objectives:

Implement a simple instruction set computer with a control unit and a data path

Experiment - 18

Theory:

I-type instruction

6	5	5	6
OP Code	Rs	Rt	Immediate

R-type Instruction

opcode	Rs	Rt	Ra	shamt	funct
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I-type Instruction \rightarrow [opcode] offset

When we look at the instruction cycle of any processor, it should involve the following operation:

- 1) Fetch instruction from memory
- 2) Decode the instruction
- 3) Fetch the operands
- 4) Execute the instruction
- 5) Write the result

Result :- Implementation of simple instruction set is verified from this output working