Microcontroller System Laboratory

Experiment 4 – Part 1, 2, 3

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Part 1 – Saw-tooth Waveform Generation

Objective

Write a program to generate a saw-tooth waveform through the DAC interface. Display the waveform on DAC scope. Find the maximum frequency and the maximum amplitude that can be achieved in the simulator.

Circuit Diagram

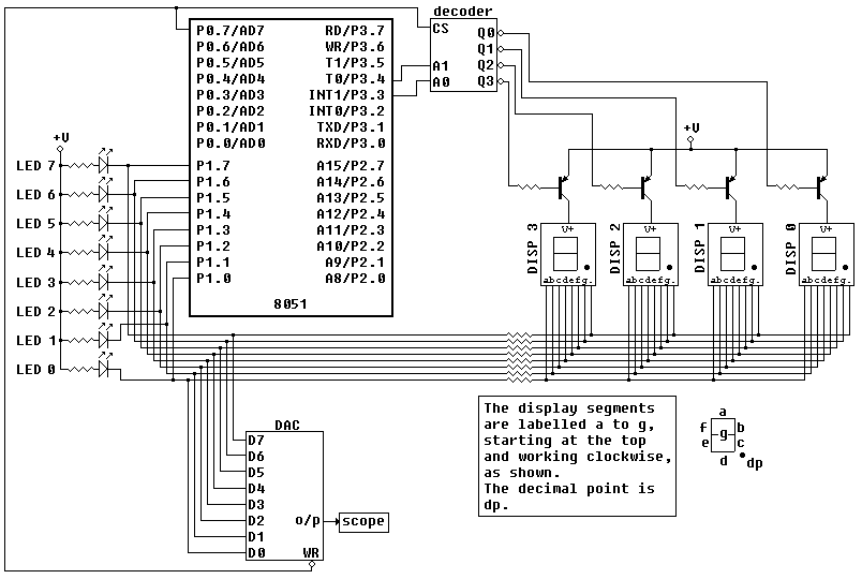

Fig. 1. Circuit diagram

Code

```
ORG 0000H       ; reset registers
N EQU 4         ; slope of saw-tooth waveform
CLR P0.7        ; enable DAC WR line

start:          ; start new cycle
  MOV A, #00H   ; initializing accumulator to zero

loop:           ; update current cycle
  MOV P1, A     ; move the content of A to P1 for display
  ADD A, #N     ; increment accumulator by N
  JNB CY, loop  ; condition to break current cycle and start new cycle
  SJMP start    ; start new cycle
  END
```

Waveform

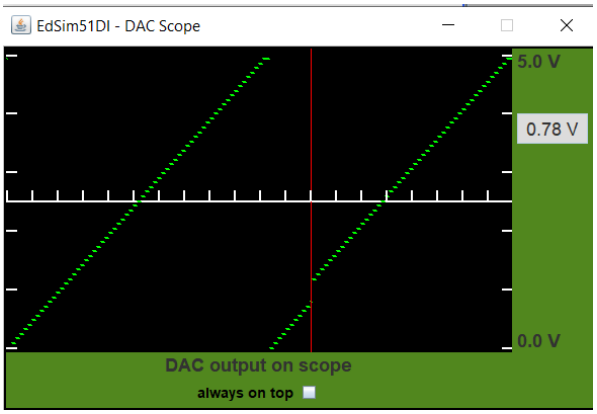

Fig. 2. Sawtooth waveform

Discussion

- In this part, a saw-tooth signal was simulated using DAC module in Edsim simulator.
- The Digital to Analog converter (DAC) is a device, that is widely used for converting digital pulses to analog signals.
- In Edsim, the MC1408 (DAC0808) Digital to Analog Converter is used.
- This chip uses R/2R ladder method. This method can achieve a much higher degree of precision. DACs are judged by its resolution. The resolution is a function of the number of binary inputs.
- **MC1408 (DAC0808)**
    - In this chip the digital inputs are converted to current.
    - The output current is known as I_{out} by connecting a resistor to the output to convert into voltage.
    - The total current provided by the I_{out} pin is basically a function of the binary numbers at the input pins $D_0 - D_7$ (D_0 is the LSB and D_7 is the MSB) of DAC0808 and the reference current I_{ref}.
    - The following formula is showing the function of I_{out}:

$$I_{Out} = I_{ref}\left(\frac{D7}{2} + \frac{D6}{4} + \frac{D5}{8} + \frac{D4}{16} + \frac{D3}{32} + \frac{D2}{64} + \frac{D1}{128} + \frac{D0}{256}\right)$$

- **Saw-tooth Signal Generation**
    - The vectors are reset using `ORG 0000H`, the slope of saw-tooth is defined by N
    - P0.7 is set to logic low, to enable DAC WR line (see circuit diagram).
    - The start module constructs a new cycle of the saw-tooth signal.
    - The accumulator is incremented in the loop module, until the cycle breaking condition is met.
    - For this experiment, the breaking condition is decided by the carry-overflow in the accumulator.
    - When the condition is satisfied, start module is called to initiate a new cycle.
    - The frequency of waveforms can be made arbitrarily high, however they might not be distinctly representing that function anymore because of utilization of limited points. Hence the values stated in the following points will state the frequency where the candidate himself feels that it still represents that function. It is a very subjective value and can change with perspective.
    - Amplitude of all the waveforms were 5V peak to peak (almost) (it can be easily done by taking a very low(say 4,6) and highest value(255) to the port of ADC.
    - The resolution of the DAC is 0.02V and the peak value of DAC is 5V,although total distinct possible values are 0 to 255 for a full scale of 5V, the resolution is approximated to 0.02V.

Part 2 – Ramp Signal Generation

Objective
Display inverted ramp signal on the DAC Scope. Change the slope of the ramp signal to 30^{o} and 60^{o}

Circuit Diagram

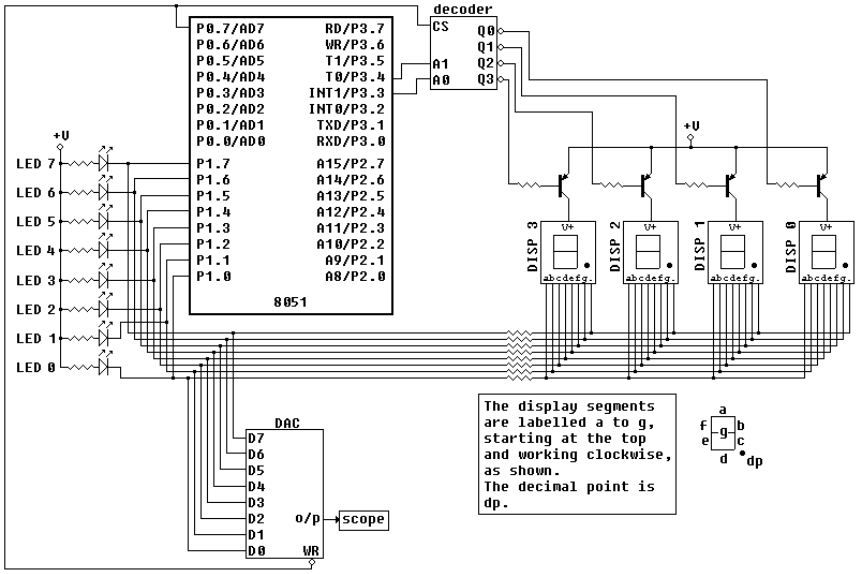

Fig. 3. Circuit diagram

Code
```
ORG 0000H       ; reset registers
N EQU 4         ; slope of ramp waveform
CLR P0.7        ; enable DAC WR line

start:
  MOV A, #255

loop:
  MOV P1, A     ; move content of accumulator to P1 for display
  SUBB A, #N    ; decrement accumulator by N
  JMP loop      ; jump back to loop
```

Waveform

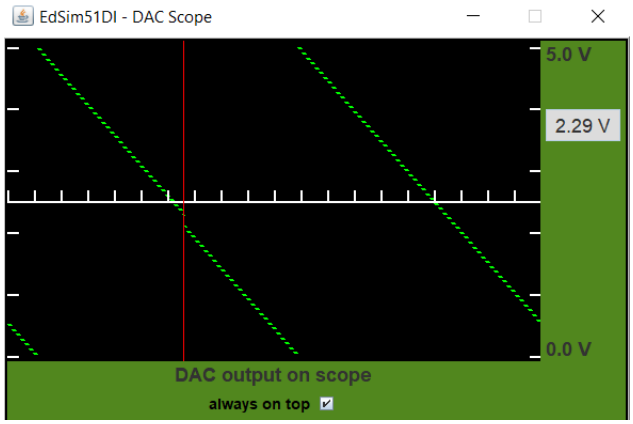

Fig. 4. Inverse ramp waveform

Discussion

- In this part, a saw-tooth signal was simulated using DAC module in Edsim simulator.
- The Digital to Analog converter (DAC) is a device, that is widely used for converting digital pulses to analog signals.
- In Edsim, the MC1408 (DAC0808) Digital to Analog Converter is used.
- This chip uses R/2R ladder method. This method can achieve a much higher degree of precision. DACs are judged by its resolution. The resolution is a function of the number of binary inputs.
- **MC1408 (DAC0808)**
    - In this chip the digital inputs are converted to current.
    - The output current is known as I_{out} by connecting a resistor to the output to convert into voltage.
    - The total current provided by the I_{out} pin is basically a function of the binary numbers at the input pins $D_0 - D_7$ (D_0 is the LSB and D_7 is the MSB) of DAC0808 and the reference current I_{ref}.
    - The following formula is showing the function of I_{out}:

$$I_{Out} = I_{ref}\left(\frac{D7}{2} + \frac{D6}{4} + \frac{D5}{8} + \frac{D4}{16} + \frac{D3}{32} + \frac{D2}{64} + \frac{D1}{128} + \frac{D0}{256}\right)$$

- **Ramp Signal Generation**
    - The vectors are reset using `ORG 0000H`, the slope of saw-tooth is defined by N
    - P0.7 is set to logic low, to enable DAC WR line (see circuit diagram).
    - The value of accumulator is set to highest value in the start module.
    - In the loop module, the accumulator is indefinitely decremented using provided slope.
    - Amplitude of all the waveforms were 5V peak to peak (almost) divided into 256 equi-spaced level.
    - The resolution of the DAC is 0.02V and the peak value of DAC is 5V, although total distinct possible values are 0 to 255 for a full scale of 5V, the resolution is approximated to 0.02V.
    - Hence, as soon as the voltage crosses 5 V, overflow takes place and the bits are reset to zero. Hence, the ramp signal is observed to be same as saw-tooth signal in DAC display.

Part 3 – Trapezoidal Signal Generation

Objective

Write programs to generate a trapezoidal waveform having 40% duty ratio with 5% rise time and 5% fall time, through the DAC interface. Display the waveform on DAC scope.

Circuit Diagram

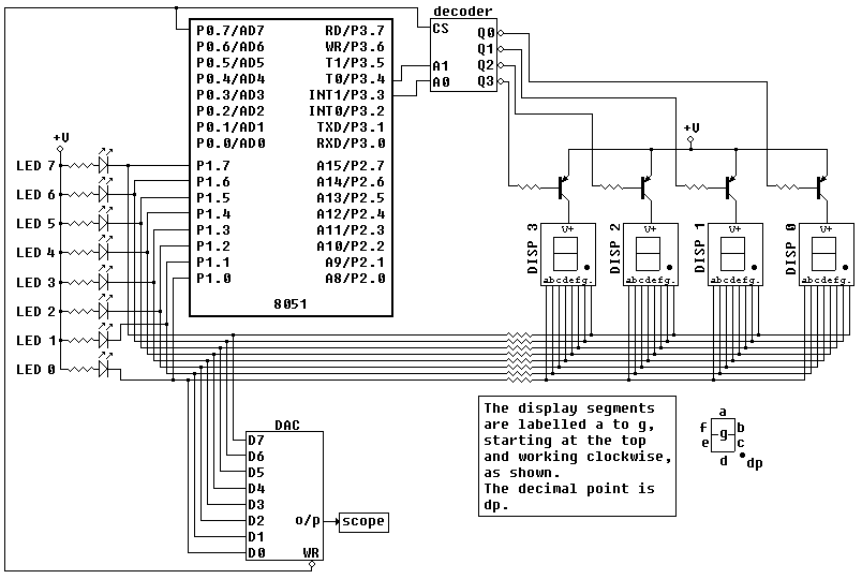

Fig. 5. Circuit diagram

Code

```
ORG 0000H        ; reset registers
CLR P0.7         ; enabling DAC WR line

N EQU 16         ; slope of trapezoid
N1 EQU 15        ; always N - 1

OT EQU 40H       ; on time
FT EQU 50H       ; off time

start:
  MOV A,#00H     ; initializing accumulator to zero

rise:
  MOV P1, A      ; moving content of accumulator to ADC input (to P1)
  ADD A, #N      ; incrementing accumulator (during rise time)
  JNB CY, rise   ; while overflow doesn't happen, keep incrementing
  MOV A, P1
  MOV R7, #OT    ; initializing on-time

logicHigh:       ; DUTY ON
  DJNZ R7, logicHigh

temp:            ; temp module added to fix the falling condition
  MOV P1,A
  SUBB A,#N1

fall:
  MOV P1,A       ; moving content of accumulator to ADC input (to P1)
  SUBB A,#N      ; decrementing accumulator (during fall time)
```

```
  JNZ fall       ; while accumulator is not zero, keep decrementing
  MOV P1, A;
  MOV R7, #FT;

logicLow:        ; DUTY OFF
  DJNZ R7,logicLow;

SJMP start
```

Waveform

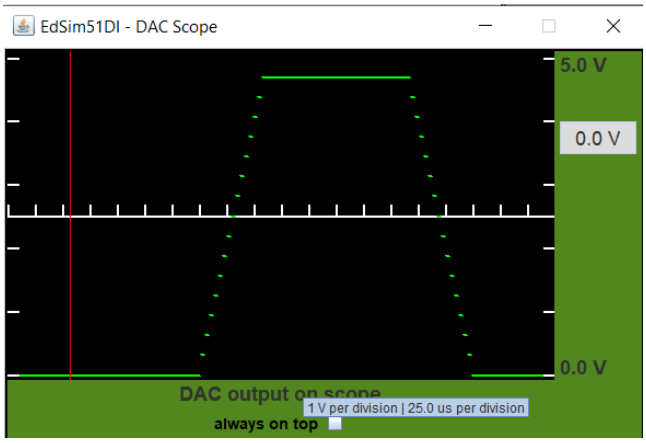

Fig. 6. Trapezoid waveform

Discussion

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- **Ramp Signal Generation**
    - The vectors are reset using `ORG 0000H`, the slope of saw-tooth is defined by N
    - P0.7 is set to logic low, to enable DAC WR line (see circuit diagram).
    - The on-duty time and off-duty time are specified as well.
    - The start module constructs a new cycle of trapezoid waveform, by setting the accumulator to zero.
    - Then for 5% time, the rise module increases the value of accumulator to maximum possible value until overflow occurs as per the increment slope.

- Then for 40% time, the value of accumulator is not changed as observed in logicHigh module.
- Then, the value of accumulator is decreased until it becomes zero to depict the fall time.
- Then for the remaining time of the cycle (50%), the accumulator remains at zero in logicLow module.
- After all this instructions are executed, the control jumps to start to initiate a new cycle.