VLSI Engineering Lab (Analog)

Experiment 1

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Objective

Designing a CMOS-based inverter and evaluating its switching threshold by changing transistor parameters

Circuit Diagram

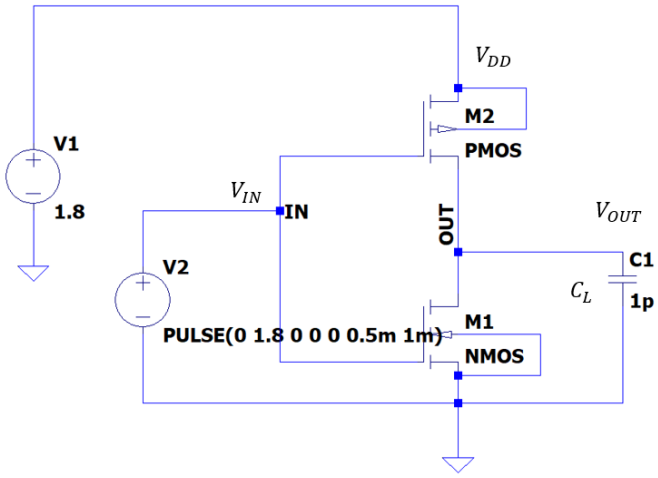


Fig. 1. Schematic of CMOS-based inverter

Description

Fig. 1. shows the circuit diagram of a static CMOS inverter. Its operation is readily understood with the aid of the simple switch model of the MOS transistor: the transistor is nothing more than a switch with an infinite off-resistance (for $|V_{GS}| < |V_T|$), and a finite on-resistance for the other case. Hence, when V_{IN} is high and is equal to V_{DD}, the NMOS transistor is on, while PMOS is off. This yields the equivalent circuit of Fig. 2. A direct path exists between V_{OUT} and the ground node, resulting in a steady-state value of $0\ V$. On the other hand, when the input voltage is low ($0\ V$), NMOS and PMOS transistors are off and on, respectively. The equivalent circuit of Fig. 3 shows that a path exists between V_{DD} and V_{OUT} yielding a high output voltage. The gate clearly functions as an inverter.

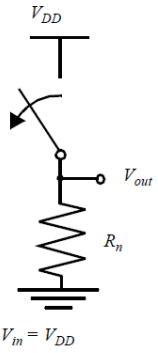


Fig. 2. V_{IN} is high

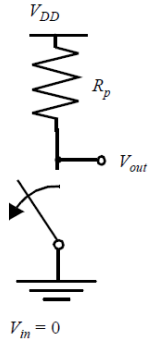


Fig. 3. V_{IN} is low

The nature and form of the voltage-transfer characteristics (VTC) can be graphically deduced by superimposing the current characteristics of the NMOS and the PMOS devices. It requires that the $I - V$ characteristics of the NMOS and PMOS devices are tranformed onto a common co-ordinate set. We have selected the input voltage V_{IN}, the output voltage V_{OUT} and the NMOS drain current I_{DN} as variables of choice. The PMOS $I - V$ relations can be translated into this variable space by following relations.

$$I_{DSp} = -I_{DSn}$$
$$V_{GSn} = V_{in} \ ; \ V_{GSp} = V_{in} - V_{DD}$$
$$V_{DSn} = V_{out} \ ; \ V_{DSp} = V_{out} - V_{DD}$$

The VTC of the inverter exhibits a very narrow transition zone. This results from the high gain during switching transient, when both NMOS and PMOS are simultaneously on, and in saturation. In that operation region, a small change in the input voltage results in large output variation.

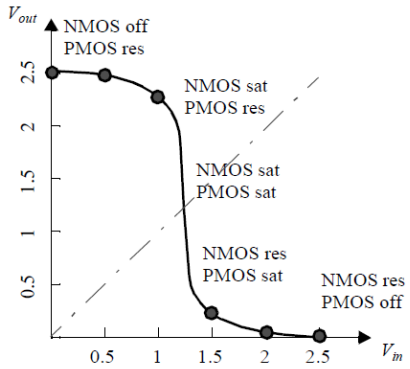


Fig. 4. Voltage-transfer characteristics of an inverter

Observations

For simulation, the gate length of NMOS and PMOS device is fixed at 180nm. The width of NMOS device is fixed at 10um and different VTC plots are obtained by varying the width of PMOS device.

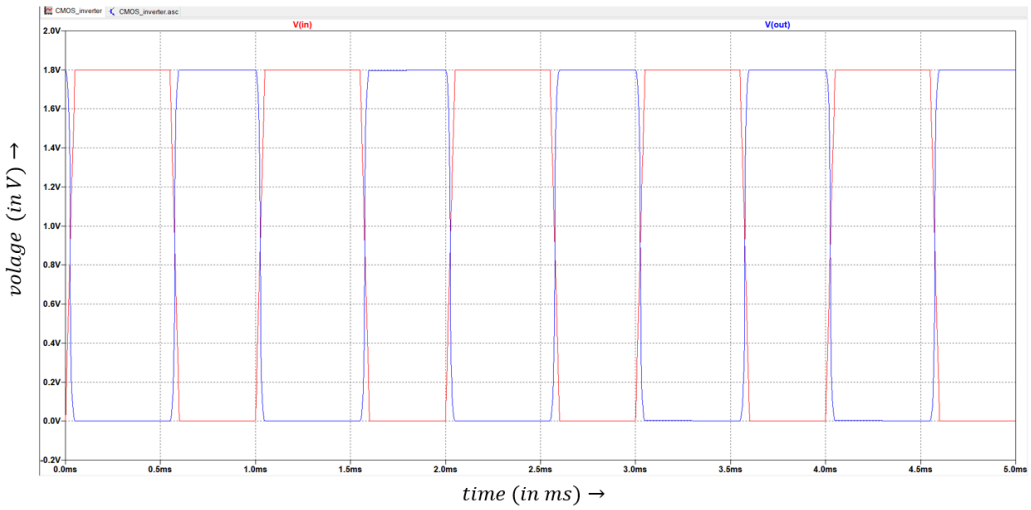


Fig. 5. Variation of input and output voltage with time

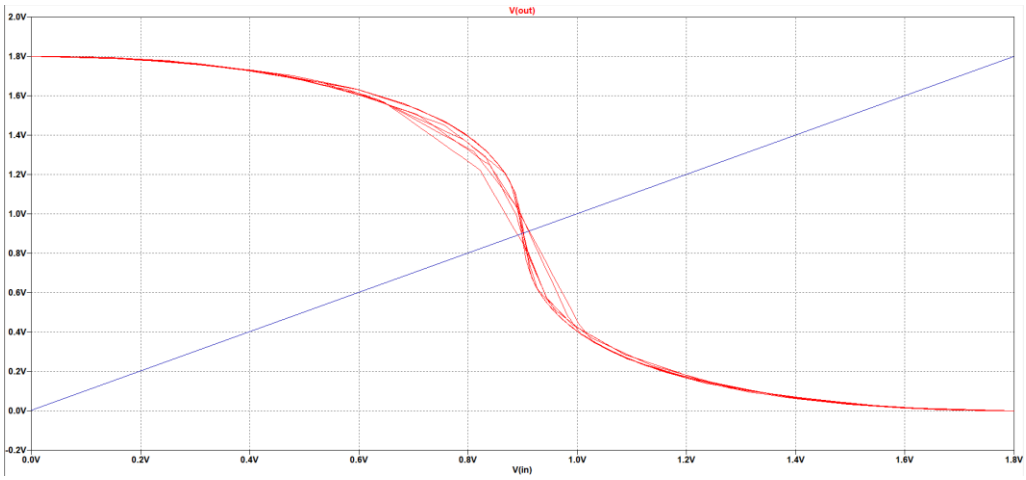


Fig. 6. Voltage-transfer characteristics of CMOS inverter when W(PMOS) = 10um

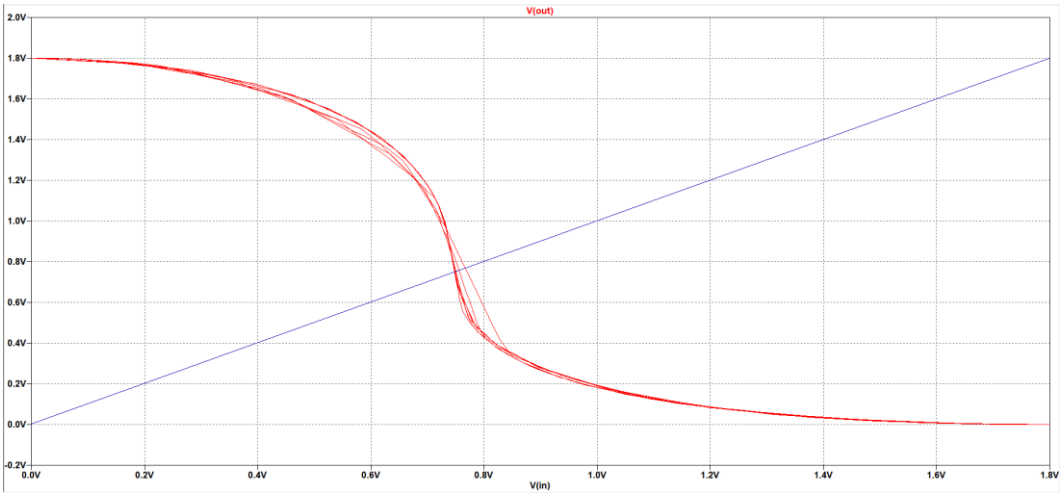


Fig. 7. Voltage-transfer characteristics of CMOS inverter when W(PMOS) = 5um

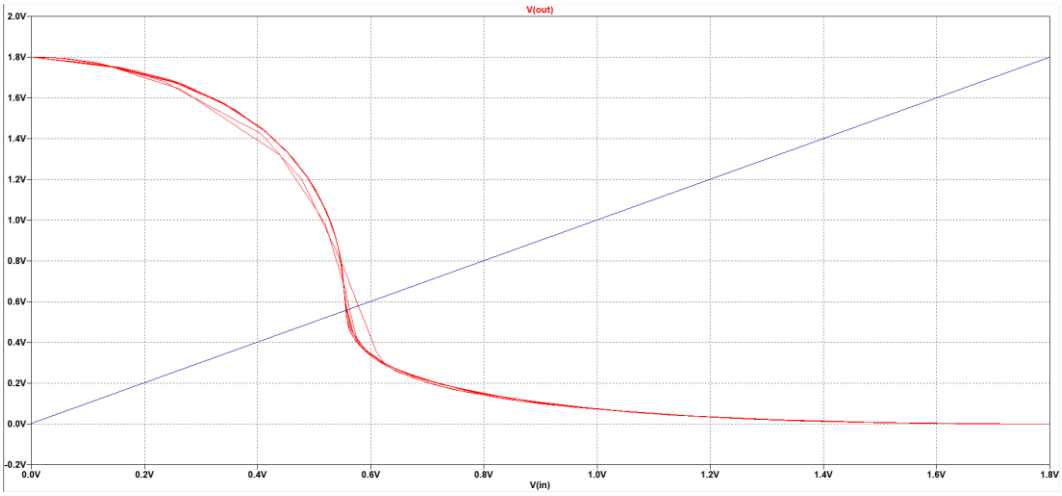


Fig. 8. Voltage-transfer characteristics of CMOS inverter when W(PMOS) = 2um

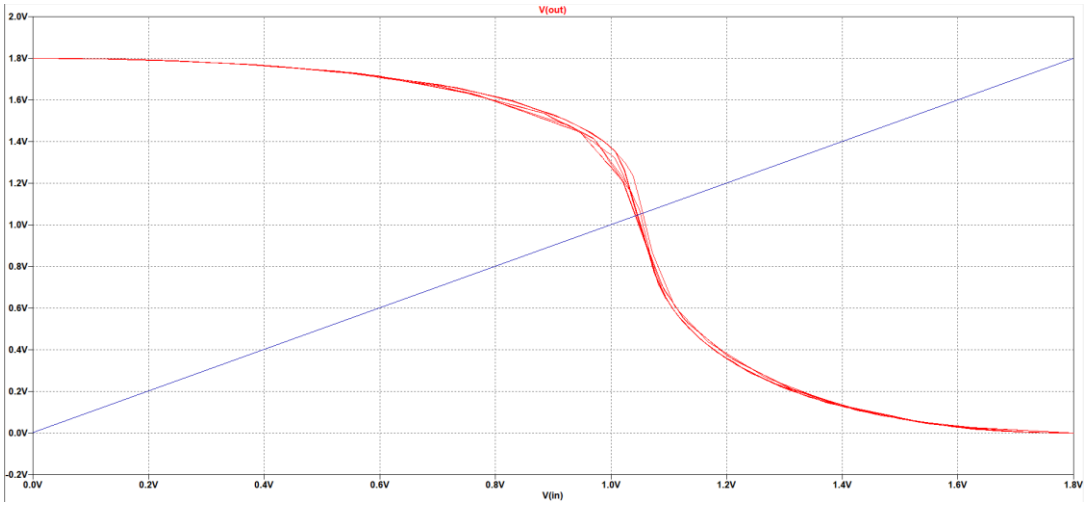


Fig. 9. Voltage-transfer characteristics of CMOS inverter when W(PMOS) = 20um

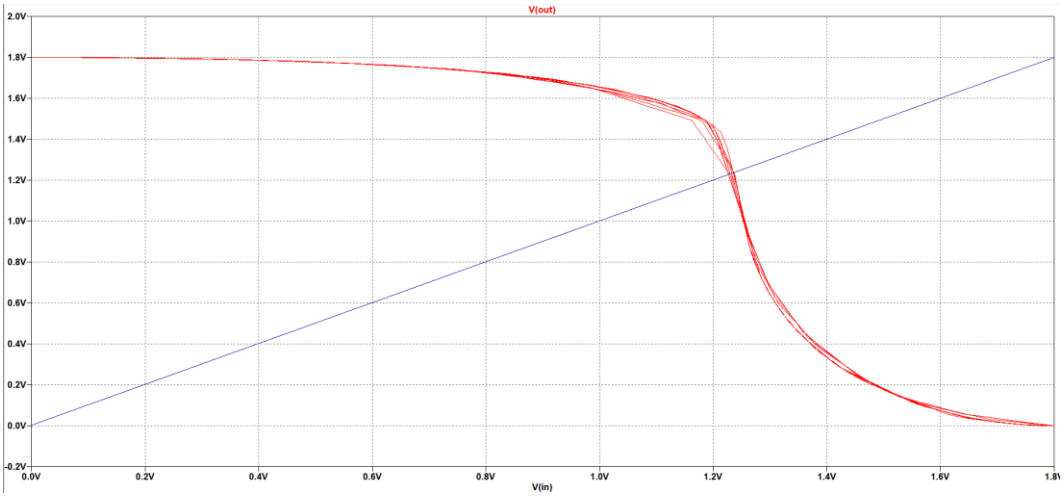


Fig. 10. Voltage-transfer characteristics of CMOS inverter when W(PMOS) = 50um

Table 1. Variation of switching threshold voltage with ratio of width of PMOS and NMOS devices

S. No.	W_p/W_n	Switching Threshold (in V)
1	5	1.23
2	2	1.04
3	1	0.90
4	0.5	0.75
5	0.2	0.57

Discussion

- The CMOS inverter is biased with $V_{DD} = 1.8\,V$ and the input voltage is given as a pulse with $V_{ON} = 1.8\,V$ and $V_{OFF} = 0\,V$ with $t_{ON} = 0.5\,ms$ and $t_{OFF} = 0.5\,ms$.
- The gate length of PMOS and NMOS devices is fixed at $180\,nm$ and the width of NMOS is fixed at $10\,\mu m$. The width of PMOS is varied and its effect on the switching threshold voltage is observed.
- Fig. 1. shows the time domain representation of input and output voltage signal. It can be observed that the rise time and fall time is not zero (due to load capacitance).
- A capacitance is added as a load because in VLSI engineering, the output of the inverter may be used to drive some other CMOS device. The gate oxide of that device is modelled here as capacitance.
- The load capacitance value was chosen near picofarad range to make the charging and discharging time constant very small, thus making the inverter **fast**.
- For simulation, the conduction parameter $K = \mu C_{ox}$ for PMOS and NMOS devices were equal. That's why for equal width of PMOS and NMOS devices, the switching threshold voltage is observed at $V_{DD}/2$.
- It is observed that increasing gate length of PMOS with respect to NMOS shifts the switching threshold voltage more towards the V_{DD}, and decreasing the same shifts the switching threshold voltage more towards $0\,V$.

The last point can be understood as follows. Let V_M denotes the switching threshold. Observe that the region where the line $V_{OUT} = V_{IN}$ intersects the VTC, both the PMOS and NMOS are in saturation (since $V_{GS} = V_{DS}$). An analytical expression for V_M can be obtained by equating the current through the transistor. After simplifying, we get the following equation:

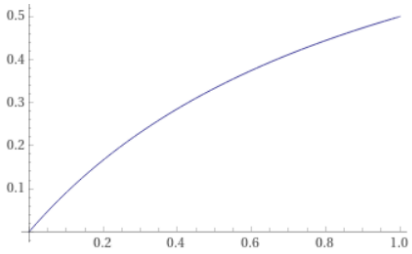
$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1 + r}$$

where $r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{\upsilon_{satp} W_p}{\upsilon_{satn} W_n}$

If we assume that V_{DD} is much larger as compared to threshold voltage and saturation voltage above expression can be simplified into:

$$V_M \approx \frac{r V_{DD}}{1 + r}$$

Thus if r is varied between 0 and 1, we would get following plot:



Therefore, we can see that when W_p/W_n increases, the switching threshold must increase theoretically. The same is observed during the simulation.

Conclusion

In this experiment, we simulated a CMOS inverter and observed the effect of different width of devices on the switching threshold voltage. Theoretically, the switching threshold should increase as W_p/W_n increases (other parameters remaining constant). The same was observed during simulation of the inverter.