# EC39004 VLSI Lab-Analog

The students will perform the following experiments in this semester by using LTspice:

**Experiment 1:** CMOS inverter design.

**Experiment 2:** Common source amplifier with resistive and active loads.

**Experiment 3:** Operational amplifier design and circuits.

**Task for every experiment:** The task for performing the soft-experiments is quite generalized and open (as per your choice of circuit parameters and simulation settings, while the circuit connections must remain same as described in the classes). Repeat the steps as per the tutorial videos (LTspice ones) in MS teams 'VLSI Lab-Analog' (also as per the discussions during the classes). Try adjusting/ changing the circuit parameters/ values logically (while considering associated theory) and also play with the simulation settings. Obtain similar plots (max. 3 for each graph type) and other results as per your wish while changing the parameters of your choice.

**Format for report submissions:** LTspice simulations only, no page limit, max. file size is 5 MB.

1. Aim/ objective of the experiment (1 or 2 sentences).
2. Circuit/ schematic diagram (screen-shot from LTspice) with caption and labels.
3. Description (15 to 20 sentences): Write about the design process and simulation commands/ settings/ configurations that are adopted for simulation.
4. Simulation Results/ Observations/ Tables: Include screen-shots and other data from LTspice after performing simulations in your PC; multiple plots with varied parameters must be presented here. Make sure to include the figure captions and the labels for x- and y-axes along with correct units, wherever applicable.
5. Discussions (15 to 20 sentences): Write about your observations, design considerations, and parameters that affect the results [MOSFET sizing (W, L), power supply voltage, input signals and parameters, load capacitance/ resistance), how and why the simulated plots change with modifications in physical and simulation parameters, possibly explain along with equations that may be relevant].
6. Summary/ conclusion (2 to 5 sentences).

**Report file naming convention:**

RollNo_Name_ExperimentNumber.pdf

e.g. 20EC10001_AsishShaik_Experiment1.pdf

**Important Notes:**

1. (Previously informed) You must get yourself accessed through the following link for attending the classes (VLSI Lab-Analog):

https://teams.microsoft.com/l/team/19%3aaf8a7063f7d2431db489544a8cc81763%40thread.tacv2/conversations?groupId=f2863356-3e3d-458a-bc40-c3bcd19b90f8&tenantId=71dbb522-5704-4537-9f25-6ad2dcd4278d

2. (Previously informed) Install 'LT Spice' from the link: https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html

   'LT Spice' is a circuit simulation software, which is freely downloadable. You need to complete your assignments/ lab work by using this software. In addition, you need to learn 'Cadence' tools, which is a professional and industry-standard software-chain for integrated circuit design. Both the platforms are included in your syllabus for viva and quiz as well.
3. Uploading link for the reports will be provided separately (MS teams or Moodle).
4. Deadline for experiments is the subsequent week's class date (11 pm).
5. Make sure to change multiple parameters in every experiment by your own in order to avoid overlap with others (avoid similar presentation/ writings/ results as that of your class mates), while ensuring the overall presentation and results are correct. Experiment reports with technical correctness, uniquely drawn schematics, parameter selections, results/ observations, and plots will gain full marks. Very strictly, any evidence of copying will lead to penalty in marks.
6. Evaluation scheme (tentative) for 'VLSI Lab-Analog' (out of 70 marks; will be scaled to 50 later):
   a. Attendance: 10 marks
   b. Reports: 4 x 10 marks
   c. Quiz/ viva: 20 marks