VLSI Engineering Lab (Analog)

Experiment 3 – Common Source Amplifier with Active Load

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Objective

Designing a common source amplifier with active load and observing the change in the gain and bandwidth with variation of different parameters

Circuit Diagram

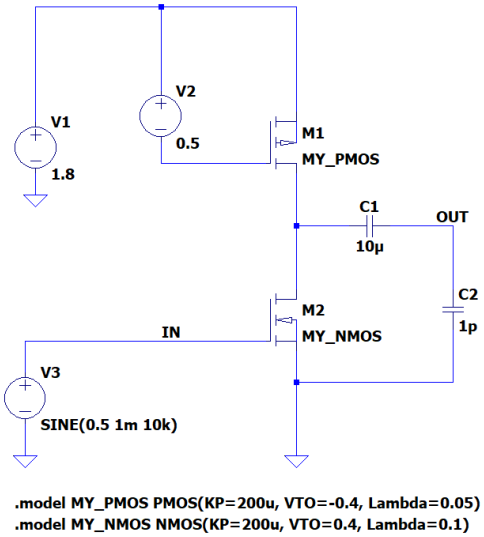

Fig. 1. Schematic of common source amplifier with active load

Theory

Fig. 1. shows the circuit diagram of a common source amplifier with an active load. For understanding its operation, we first need to analyse how CS amplifier with current-source biasing works.

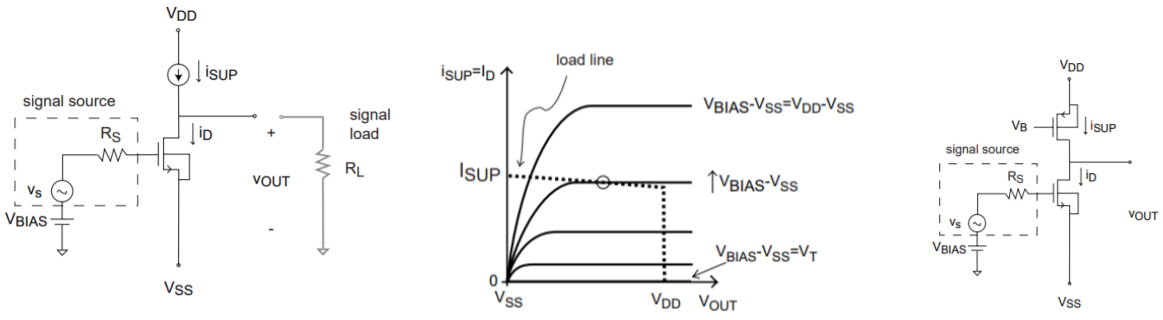

Fig. 2. (left) Schematic of common source amplifier with current source, **(middle)** load-line view, **(right)** CS amplifier with PMOS as current source

Assuming both the transistors in saturation. First, we need to fix what should be I_{SUP}, the current flowing through PMOS and NMOS. The value of V_B required for given I_{SUP}, is given as:

$$I_{SUP} = -I_{Dp} = \left(\frac{W}{2L}\right)_p \mu_p C_{ox}\left(V_{DD} - V_B + V_{Tp}\right)^2$$

We have,

$$I_{SUP} = I_{Dn} = \left(\frac{W}{2L}\right)_n \mu_n C_{ox}(V_{BIAS} - V_{ss} - V_{Tn})^2$$

As gate length for a given technology is fixed, we can only vary width of MOS devices and biasing voltages. For this experiment, we have made $\mu_p C_{ox} = \mu_n C_{ox}$. Therefore,

$$W_p\left(V_{DD} - V_B + V_{Tp}\right)^2 = W_n(V_{BIAS} - V_{Tn})^2$$

since $V_{ss} = 0\ V$ in this case. Further simplifying, we get

$$V_{SGp} = \sqrt{\frac{W_n}{W_p}}(V_{BIAS} - V_{Tn}) - V_{Tp}$$

Above equation must be satisfied for proper functioning of the amplifier. Putting the default values of the quantities in above equation, we get

$$V_2 = \sqrt{\frac{W_n}{W_p}}(0.5 - 0.4) + 0.4 = 0.4 + 0.1\sqrt{\frac{W_n}{W_p}}$$

Signal swing

The upswing is limited by PMOS leaving saturation. We have,

$$V_{DD} - v_{OUT} \geq V_{SD-sat,p} = V_{DD} - V_B + V_{Tp}$$

This implies,

$$v_{OUT} \leq V_B - V_{Tp}$$

Downswing is limited by NMOS leaving saturation.

$$v_{OUT} \geq V_{BIAS} - V_{Tn}$$

Gain

The gain of any topology is given as,

$$A_v = -g_{m,eff}R_{out} = -g_{m,n}\left(r_{o,n}||r_{o,p}\right)$$

We have,

$$g_{m,n} = \sqrt{2I_{SUP}\left(\frac{W}{L}\right)_n \mu_n C_{ox}};\ r_{o,n} \approx \frac{1}{\lambda_n I_{SUP}} \propto \frac{L_n}{I_{SUP}}; r_{o,p} \approx \frac{1}{\lambda_p I_{SUP}} \propto \frac{L_p}{I_{SUP}};$$

Plots

The default values of elements used while simulation is as given in Fig. 1. Moreover, for NMOS and PMOS device, the gate length is fixed at 180 nm and default value of the width of devices is 1.8 um. We can observe from Fig. 3. that the output voltage signal is inverted and amplified with respect to the input voltage signal. The AC voltage gain in this case is $20\log\left(\frac{150\ mV}{1\ mV}\right) = 43.52\ dB$. During simulation, we observe the effect of changing:

- Current through NMOS and PMOS
- Width of NMOS and PMOS

on the gain and bandwidth of the CS amplifier.

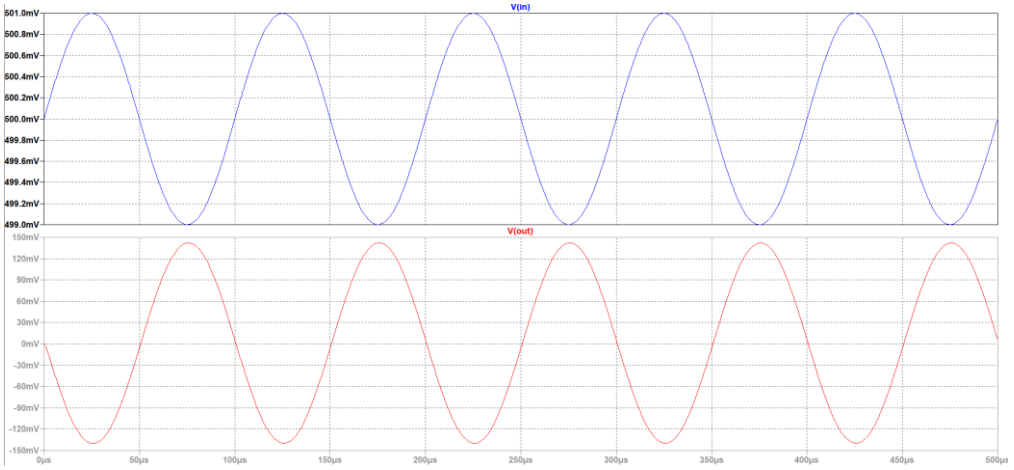

Fig. 3. Input and output voltage signal of CS amplifier

1 Changing current through MOS devices (keeping $W_p = W_n$)

1.1 $I_{SUP} = 10\ uA, V_2 = V_3(offset) = 0.5\ V$

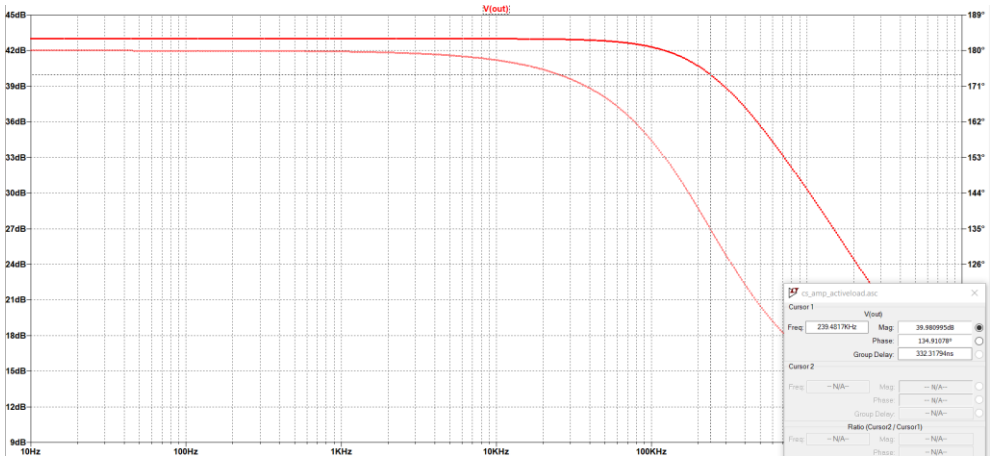

Fig. 4. Bode plot of voltage gain. A_v = 43 dB and B = 239.48 KHz

1.2 $I_{SUP} = 40\ uA, V_2 = V_3(offset) = 0.6\ V$

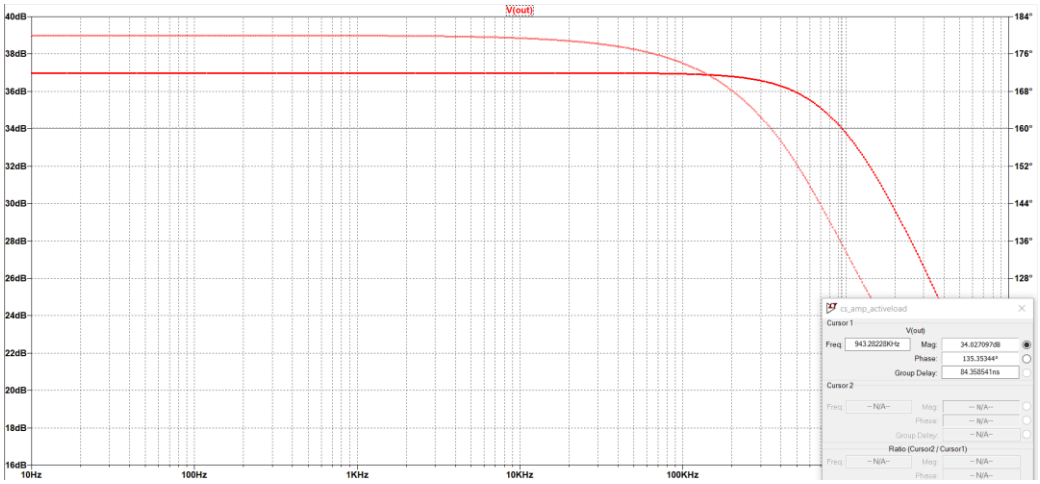

Fig. 5. Bode plot of voltage gain. A_v = 37 dB and B = 943.28 KHz

1.3 $I_{SUP} = 90\ uA, V_2 = V_3(offset) = 0.7\ V$

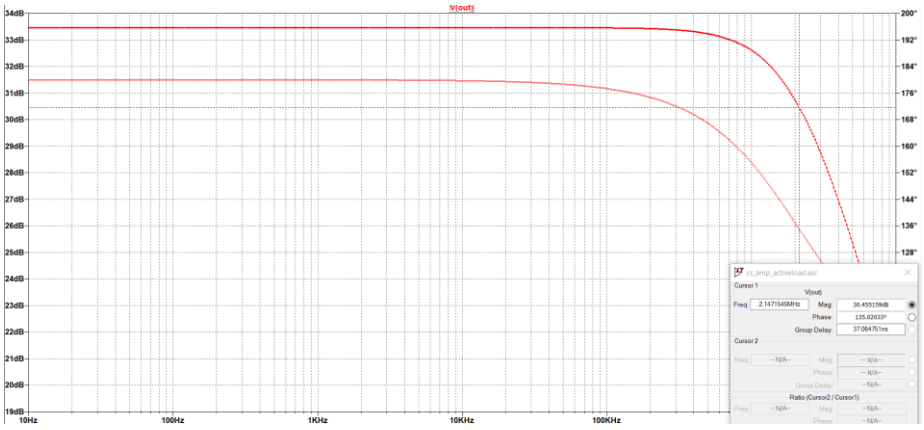

Fig. 6. Bode plot of voltage gain. A_v = 33.46 dB and B = 2147.15 KHz

2 Changing width of MOS devices

For simulation purpose, the width of PMOS is fixed at 1.8 um and width of NMOS is varied as multiple of 1.8 um. The value of voltage source V_2 which is equal to V_{SDp} is fixed at 0.6 V, hence I_{SUP} is fixed at 40 uA. As the width of NMOS will be changing in the simulation, we need to change the DC-offset of voltage source V_3 as per the equation given in theory section.

2.1 $W_n = 1.8\ um, V_3(offset) = 0.6\ V$

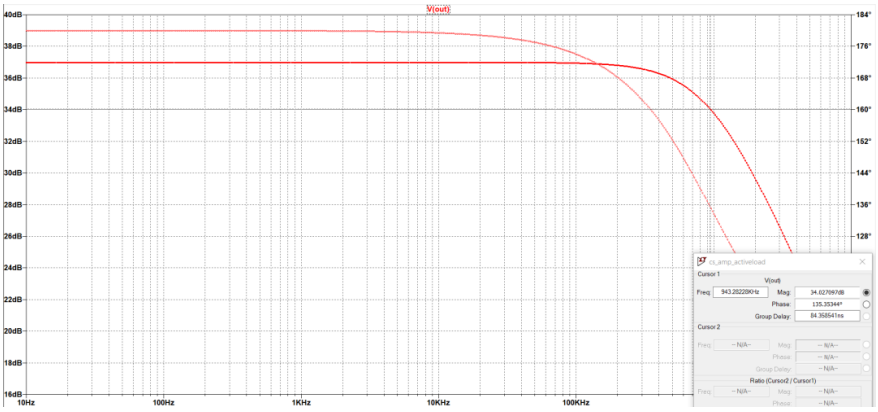

Fig. 7. Bode plot of voltage gain. A_v = 37 dB and B = 943.28 KHz

2.2 $W_n = 7.2\ um, V_3(offset) = 0.5\ V$

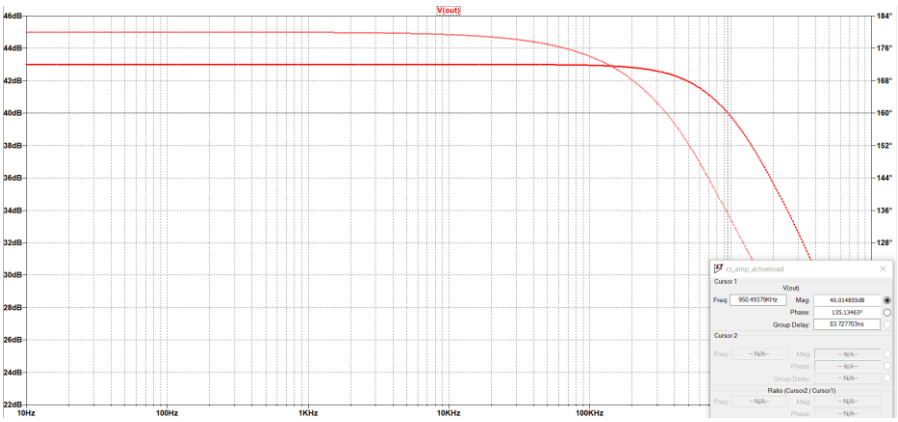

Fig. 8. Bode plot of voltage gain. A_v = 43 dB and B = 950.49 KHz

2.3 $W_n = 28.8\,um, V_3(offset) = 0.45\,V$

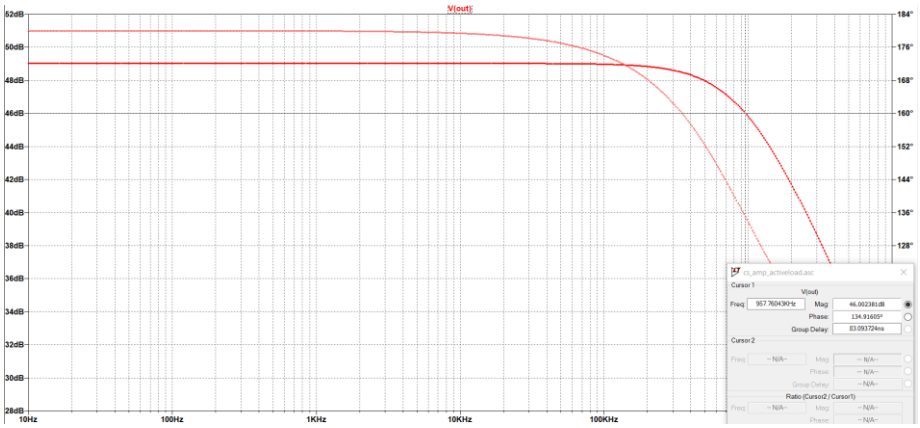

Fig. 9. Bode plot of voltage gain. A_v = 49 dB and B = 957.76 KHz

Results

Table 1. Variation in gain and bandwidth with supply current

#	***Supply current*** (in uA)	***Gain*** (in dB)	***Bandwidth*** (in KHz)
1	10	43.00	239.48
2	40	37.00	943.28
3	90	33.46	2147.15

Table 2. Variation in gain and bandwidth with width of NMOS

#	***Width of NMOS*** (in um)	***Gain*** (in dB)	***Bandwidth*** (in KHz)
1	1.8	37.00	943.28
2	7.2	43.00	950.49
3	28.8	49.00	957.76

Discussion

- The common source amplifier with active load is biased using three voltage sources V_1, V_2 and V_3, with latter being used for supplying the AC signal as well.
- Custom model for NMOS and PMOS is implemented in the simulation, with details given in Fig. 1.
- CS amplifier with active load is similar to a CS amplifier with a current mirror, where the Q-point of the circuit is defined by the value of supply current.
- From Fig. 3. we can observe that the output voltage signal is inverted and amplified with respect to the input voltage signal. Inversion is due to the negative sign in the gain equation and amplification is due to proper values of the parameters.
- From the bode plots obtained from the simulations, it can be seen that there is no lower cut-off frequency. This is because no compensating / coupling capacitances are used in the schematic as shown in Fig. 1.
- From Fig. 4, 5, 6 and Table 1, it can be observed that as the value of supply current I_{SUP} is increased, the gain of the CS amplifier decreases; however, the bandwidth of operation is observed to increase. From the equations defined in the theory section, it is clear that $A_v = -g_{m,eff}R_{out} = -g_{m,n}(r_{o,n}||r_{o,p})$. However, $g_{m,n} \propto \sqrt{I_{SUP}}$, but $r_{o,n} \propto \frac{1}{I_{SUP}}$ and $r_{o,p} \propto \frac{1}{I_{SUP}}$. Hence, the overall dependence is given as $A_v \propto \frac{1}{\sqrt{I_{SUP}}}$. Therefore, as I_{SUP} increases,

theoretically, A_v should decrease. The decrease in bandwidth is due to the fact that for a given amplifier, the gain-bandwidth product is fairly constant.

- From Fig. 7, 8, 9 and Table 2, it can be observed that as the value of NMOS width W_n is increased, the gain of the CS amplifier increases; however, the bandwidth of operation is observed to increase as well. From the equations defined in the theory section, it is clear that $A_v = -g_{m,eff}R_{out} = -g_{m,n}(r_{o,n}||r_{o,p})$. From the same equation, it can be observed that $g_{m,n} \propto \sqrt{W_n}$ and $r_{o,n}$ are fairly independent with variation in W_n. Thus, as width of NMOS is increased, theoretically, A_v should increase as well. Now for the bandwidth, it must be noted that as NMOS width W_n is changed, the whole device changes and gain-bandwidth product is not constant in this case.

Conclusion

In this experiment, we simulated a CS amplifier with active load and studied the effect of changing values of width of NMOS device and supply current on the gain and the bandwidth of the amplifier. The results can be summarized as,

Parameter	***Change in Gain with increase in parameter value***	***Change in Bandwidth with increase in parameter value***
Supply current	Decreases	Increases
NMOS width	Increases	Increases