VLSI Engineering Lab (Analog)

Experiment 2 – Common Source Amplifier

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Objective

Designing a common source amplifier and observing the change in the gain and bandwidth with variation of different parameters

Circuit Diagram

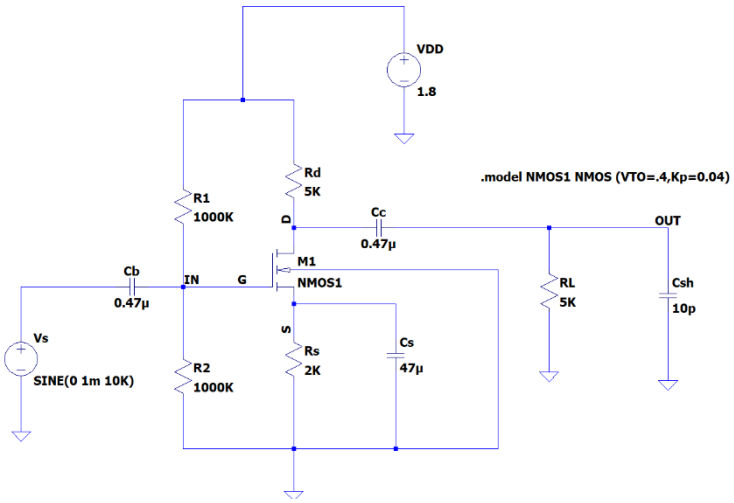

Fig. 1. Schematic of common source amplifier

Theory

Fig. 1. shows the circuit diagram of a common source amplifier with source resistance. For simulation, an NMOS device with threshold voltage $V_{TH} = 0.4\,V$ is used. This means, for the device to be in saturation, two conditions are to satisfied.

$$V_{GS} > V_{TH}$$

$$V_{DS} > V_{GS} - V_{TH}$$

These conditions are satisfied in the design, which is evident from Fig. 2.

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        --- Operating Point ---

V(s):           0.4             voltage
V(n001):        1.8             voltage
V(d):           0.8             voltage
V(g):           0.9             voltage
V(out):         1.88e-015       voltage
V(n002):        0               voltage
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Fig. 2. DC operating point of above schematic

For understanding the dependence of AC voltage gain A_V, small signal analysis of the schematic is required.

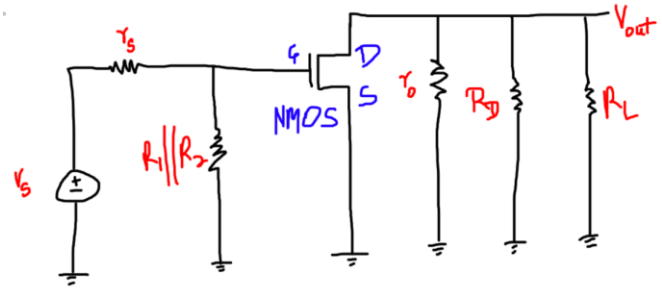

Fig. 3. Small signal model of schematic

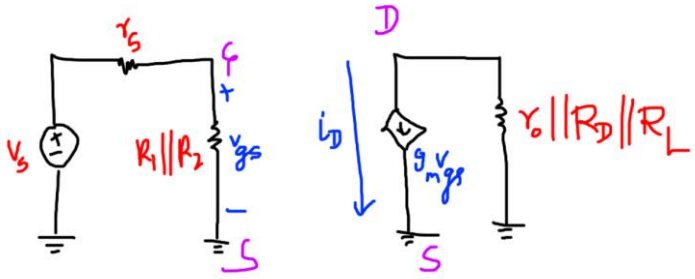

Fig. 4. Hybrid-π model of schematic

Using Fig. 4. we have,

$$v_{out} = -i_d(r_o||R_D||R_L) \quad [1]$$

We can see that,

$$i_d = g_m v_{gs} = \frac{g_m(R_1||R_2)}{r_s + R_1||R_2} v_s \quad [2]$$

Therefore,

$$A_v = \frac{v_{out}}{v_s} = -\frac{g_m(R_1||R_2)}{r_s + R_1||R_2}(r_o||R_D||R_L) \quad [3]$$

We can see that gain of amplifier depends upon transistor parameters, load resistance, drain resistance, etc.

Plots

The default values of elements used while simulation is as given in Fig. 1. Moreover, for NMOS device, default gate length is 180 nm and default width is 2 um.

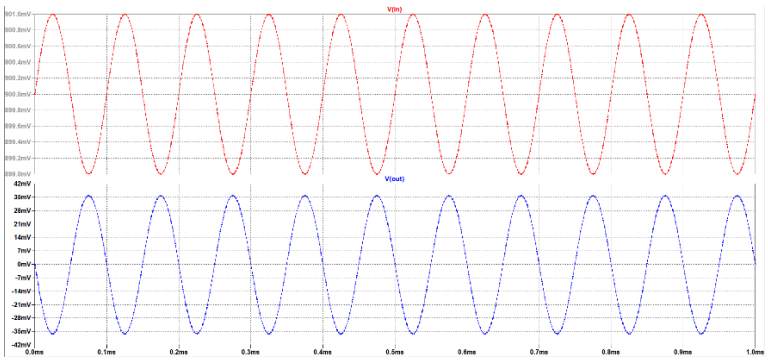

Fig. 5. Input and output voltage signal of CS amplifier

We can observe from Fig. 5. that the output voltage signal is inverted and amplified with respect to the input voltage signal. The AC voltage gain in this case is $20\log\left(\frac{35\ mV}{1\ mV}\right) = 30.88\ dB$. During simulation, we observe the effect of changing:

- Width of NMOS device
- Load resistance R_L
- Drain resistance R_D
- Source resistance R_s

on the AC voltage gain A_v and the bandwidth of operation B.

1 Variation of amplifier gain and bandwidth with width of NMOS device

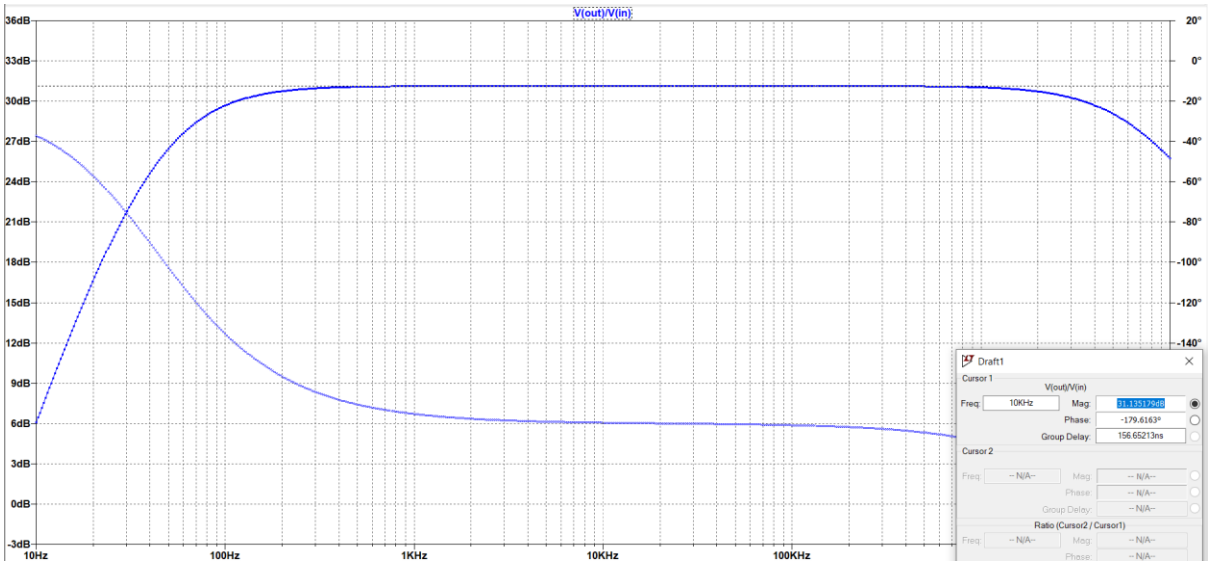

Fig. 6. Bode plot of AC voltage gain A_v for $W = 2\mu m$. The gain observed is 31.14 dB and the bandwidth is 6.371 MHz

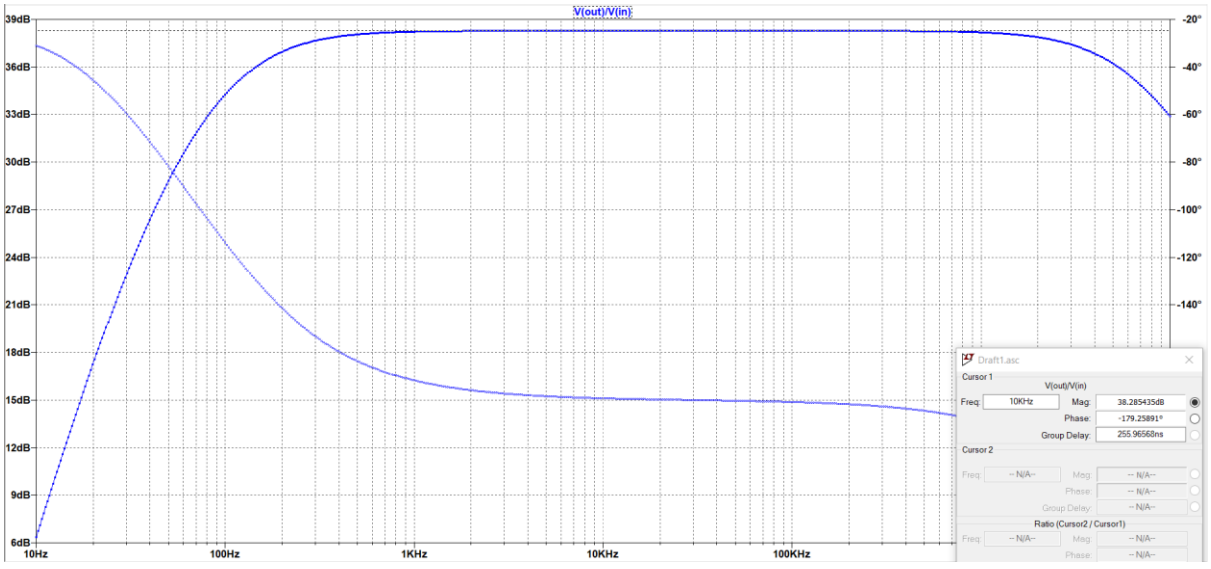

Fig. 7. Bode plot of AC voltage gain A_v for $W = 10\mu m$. The gain observed is 38.28 dB and the bandwidth is 6.371 MHz

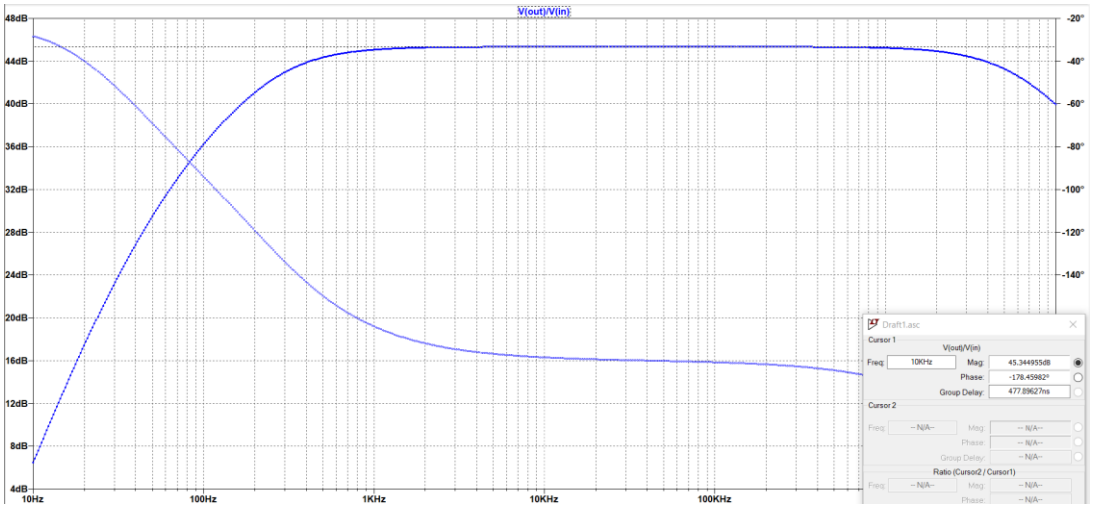

Fig. 8. Bode plot of AC voltage gain A_v for $W = 50\mu m$. The gain observed is 45.34 dB and the bandwidth is 6.371 MHz

2 Variation of amplifier gain and bandwidth with load resistance R_L

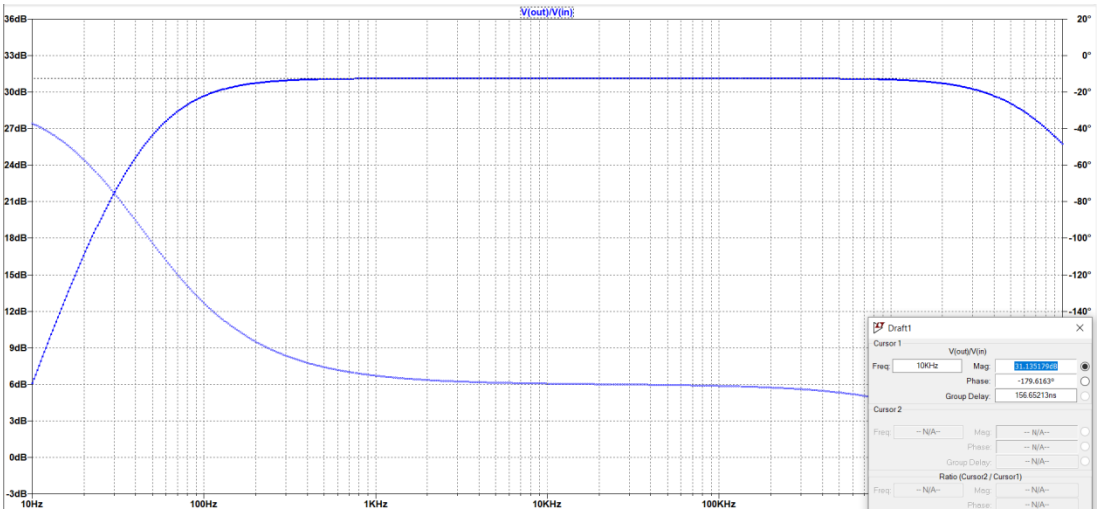

Fig. 9. Bode plot of AC voltage gain A_v for $R_L = 5\ K\Omega$. The gain observed is 31.14 dB and the bandwidth is 6.371 MHz

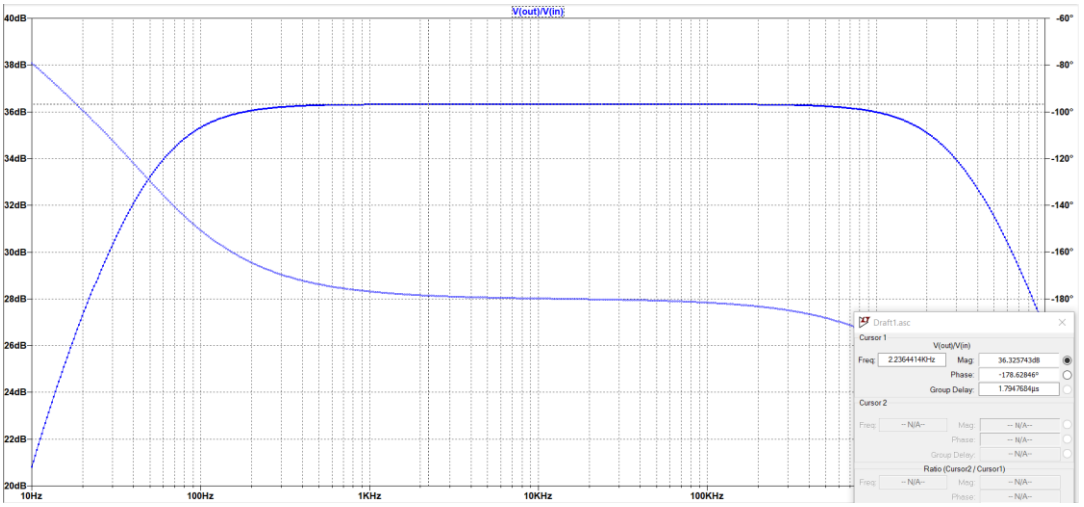

Fig. 10. Bode plot of AC voltage gain A_v for $R_L = 50\ K\Omega$. The gain observed is 36.32 dB and the bandwidth is 3.484 MHz

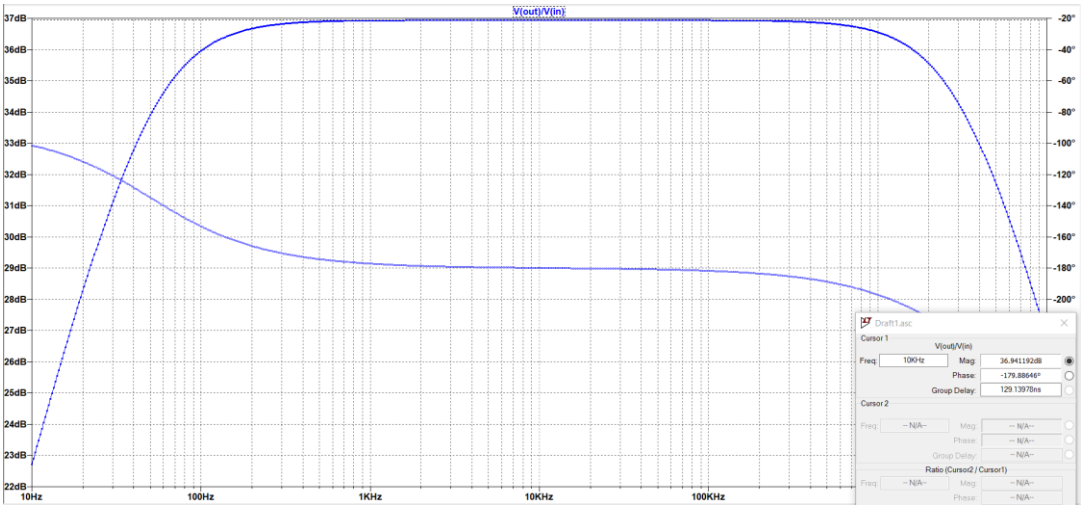

Fig. 11. Bode plot of AC voltage gain A_v for $R_L = 200\ K\Omega$. The gain observed is 36.94 dB and the bandwidth is 3.252 MHz

3 Variation of amplifier gain and bandwidth with drain resistance R_D

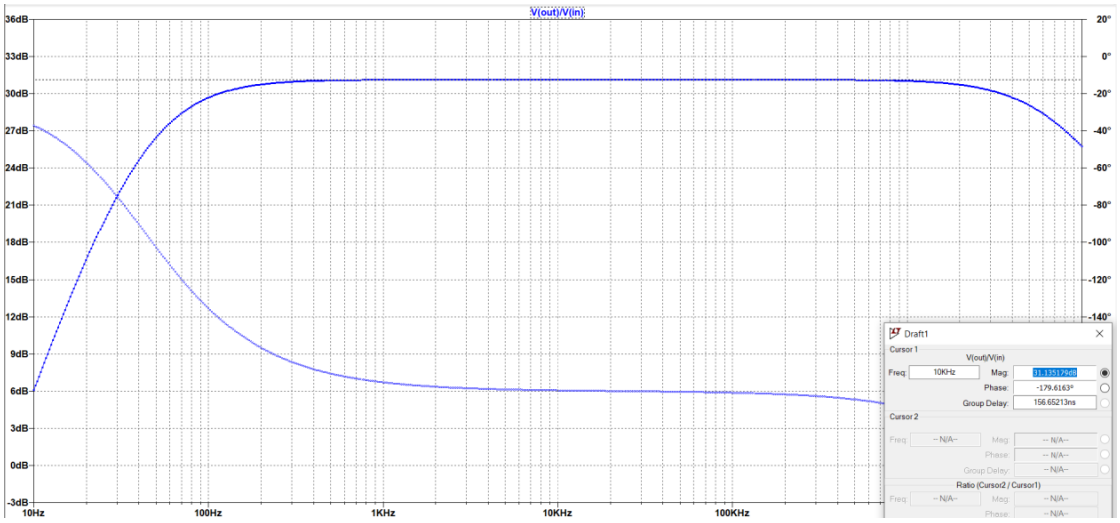

Fig. 12. Bode plot of AC voltage gain A_v for $R_D = 5\ K\Omega$. The gain observed is 31.14 dB and the bandwidth is 6.371 MHz

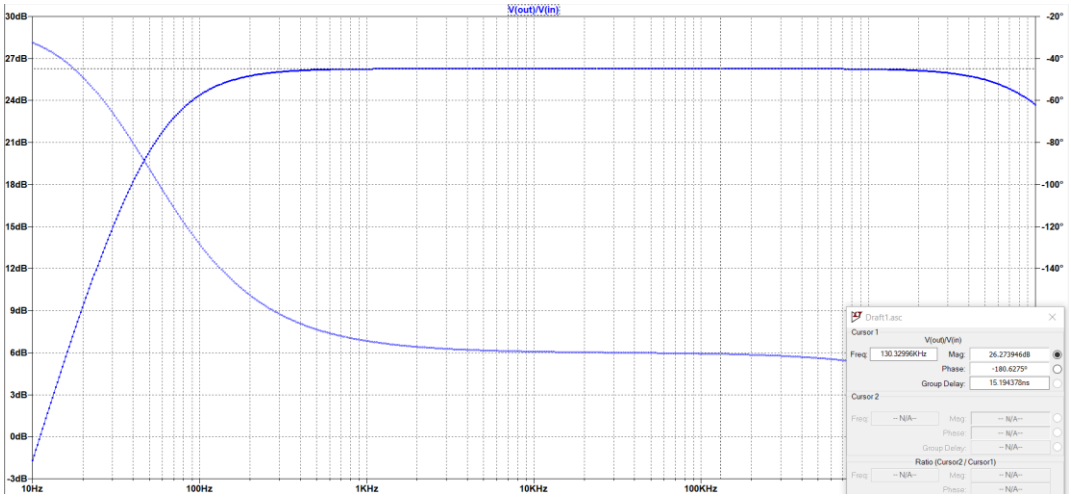

Fig. 13. Bode plot of AC voltage gain A_v for $R_D = 2\ K\Omega$. The gain observed is 26.27 dB and the bandwidth is 11.157 MHz

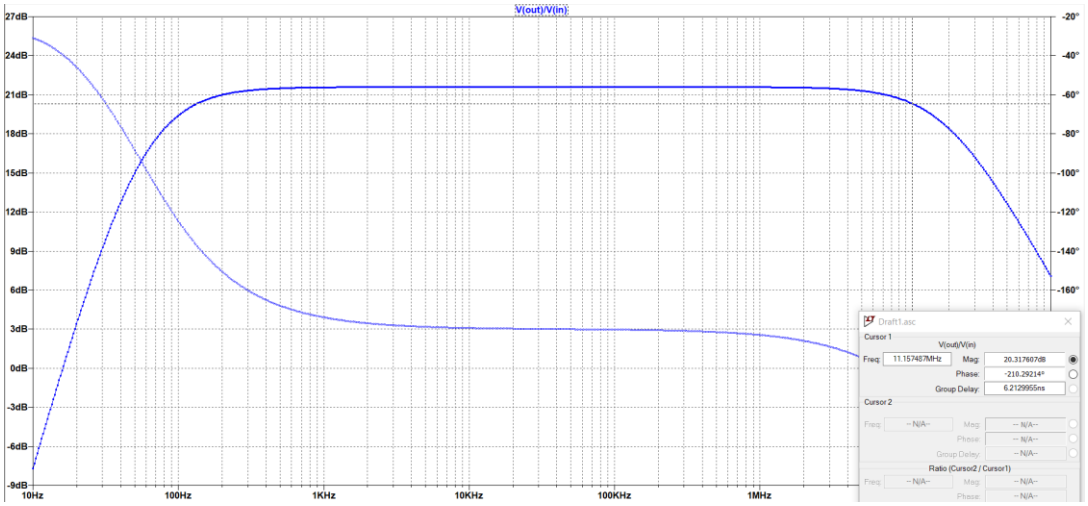

Fig. 14. Bode plot of AC voltage gain A_v for $R_D = 1\ K\Omega$. The gain observed is 21.59 dB and the bandwidth is 19.048 MHz

4 Variation of amplifier gain and bandwidth with source resistance R_S

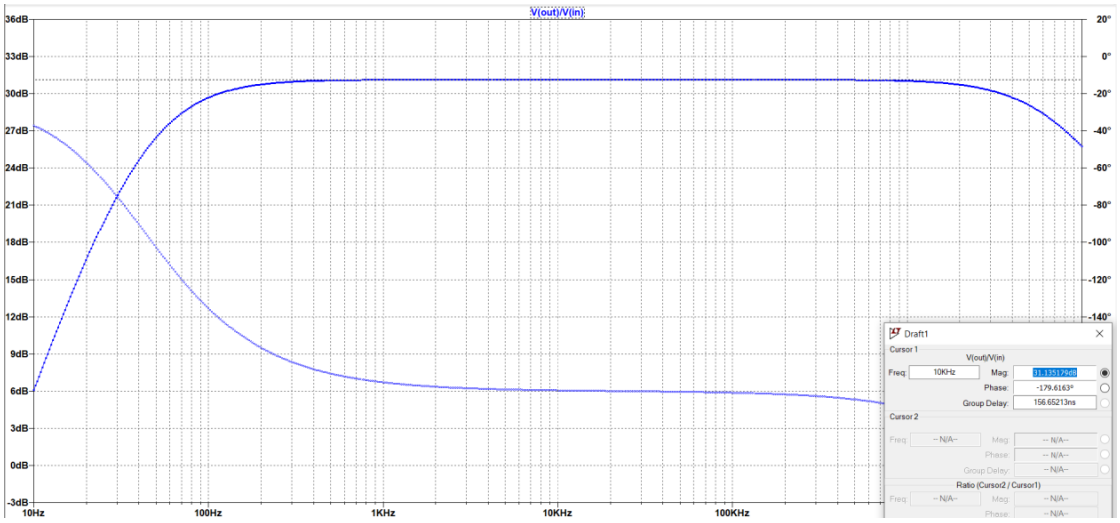

Fig. 15. Bode plot of AC voltage gain A_v for $R_s = 2\ K\Omega$. The gain observed is 31.14 dB and the bandwidth is 6.371 MHz

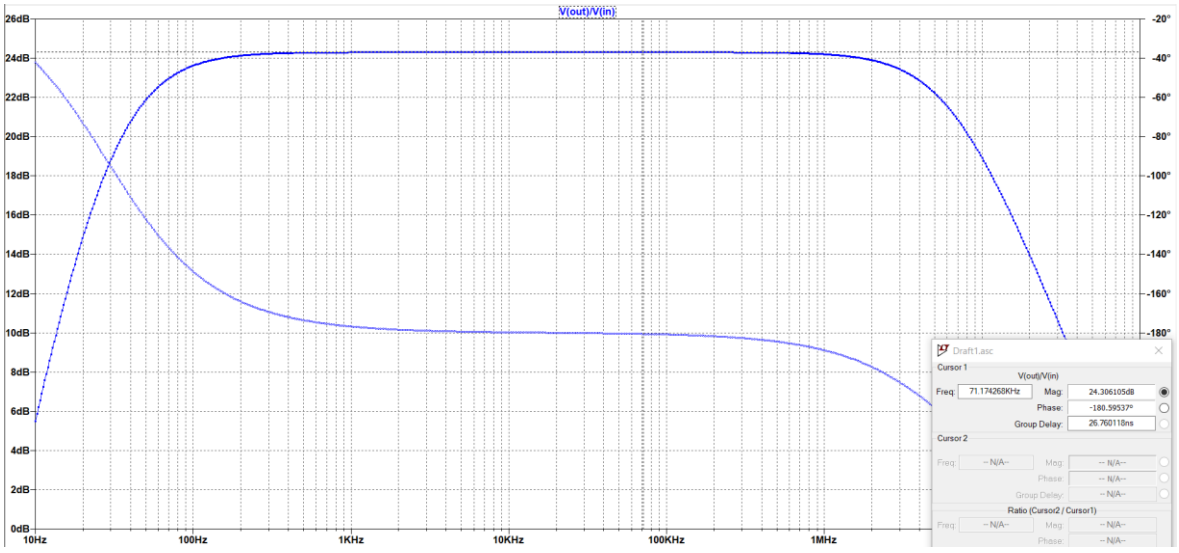

Fig. 16. Bode plot of AC voltage gain A_v for $R_s = 10\ K\Omega$. The gain observed is 24.30 dB and the bandwidth is 6.362 MHz

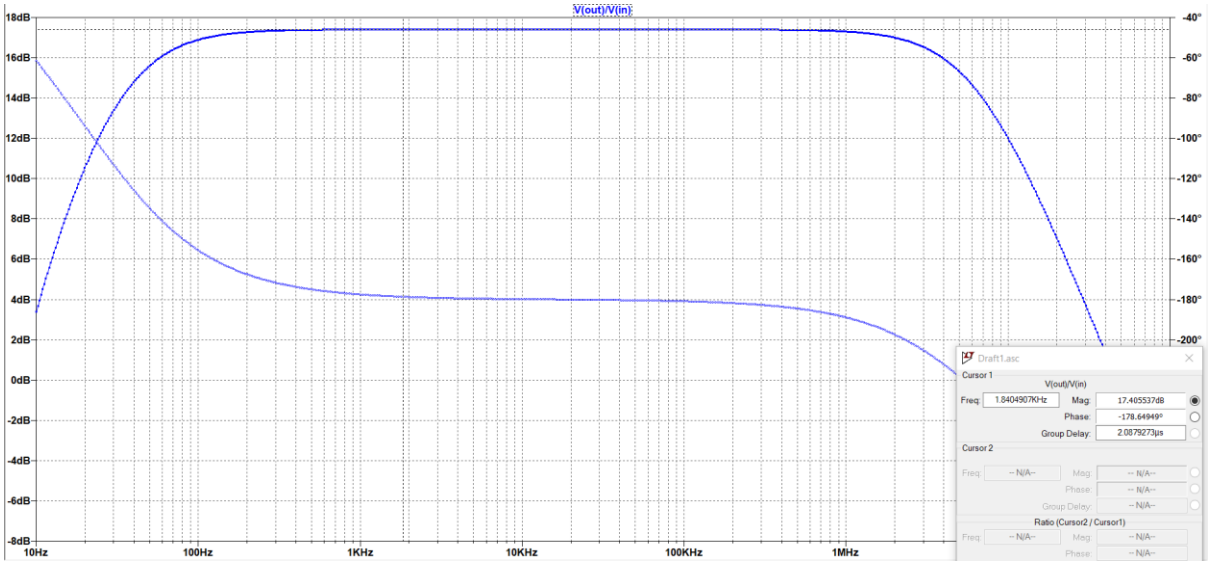

Fig. 17. Bode plot of AC voltage gain A_v for $R_s = 50\ K\Omega$. The gain observed is 17.41 dB and the bandwidth is 6.362 MHz

Results

Table 1. Variation in gain and bandwidth with width of NMOS

#	***Width of NMOS*** (in um)	***Gain*** (in dB)	***Bandwidth*** (in MHz)
1	2	31.14	6.371
2	10	38.28	6.371
3	50	45.34	6.371

Table 2. Variation in gain and bandwidth with load resistance

#	***Load resistance*** (in kΩ)	***Gain*** (in dB)	***Bandwidth*** (in MHz)
1	5	31.14	6.371
2	50	36.32	3.484
3	200	36.94	3.252

Table 3. Variation in gain and bandwidth with drain resistance

#	***Drain resistance*** (in kΩ)	***Gain*** (in dB)	***Bandwidth*** (in MHz)
1	5	31.14	6.371
2	2	26.27	11.157
3	1	21.59	19.048

Table 4. Variation in gain and bandwidth with source resistance

#	***Source resistance*** (in kΩ)	***Gain*** (in dB)	***Bandwidth*** (in MHz)
1	2	31.14	6.371
2	10	24.30	6.362
3	50	17.41	6.362

Discussion

- The common source amplifier is biased with voltage-divider biasing with $V_{DD} = 1.8\,V$ such that $V_G = 0.9\,V$. As the threshold voltage of NMOS used is $0.4\,V$. Hence, for proper functioning $V_S < 0.5\,V$.
- The values of resistances used is chosen such that the transistor remain in saturation region over the course of simulation.
- From Fig. 5. we can observe that the output voltage signal is inverted and amplified with respect to the input voltage signal. Inversion is due to the negative sign in the gain equation and amplification is due to proper values of the parameters.
- In Fig. 6, 7, 8 and Table 1, the change in the gain and the bandwidth of the CS amplifier with respect to width of the NMOS device is observed. It can be seen that as the width of NMOS device is increased, the gain of CS amplifier increases. However, there is no effect of changing width on the bandwidth of operation. Increase in gain with increase in width can be attributed to the fact that higher width means more current-driving capability, hence larger trans-conductance g_m.
- In Fig. 9, 10, 11 and Table 2, variation of the gain and the bandwidth of CS amplifier is observed as the value of load resistance is changed. It has been observed that as the value of load resistance increases, the gain of the CS amplifier increases, however, the 3 dB bandwidth decreases. Increase in gain with increase in load resistance is evident from eqn. 3. For the given amplifier, the gain-bandwidth is constant. Hence, if gain increases, bandwidth decreases and vice-versa.
- In Fig. 12, 13, 14 and Table 3, variation of the gain and bandwidth of CS amplifier is observed as the value of drain resistance is changed. It has been observed that as the value of drain resistance decreases, the gain of CS amplifier decreases, however, the 3 dB bandwidth increases. Decrease in gain with decrease in drain resistance is evident from eqn. 3. As the gain-bandwidth product is constant, bandwidth increases with decrease in gain.
- Care must be taken while varying the value of drain resistance as high value of drain resistance may put the NMOS in triode region.
- In Fig 15, 16, 17 and Table 4, variation of the gain and bandwidth of CS amplifier is observed as the value of source resistance is changed. It has been observed that as the value of source resistance is increased, the gain of the amplifier decreases, however, the bandwidth remains fairly constant. Decrease in gain with increase in source resistance is not explicit in eqn. 3, but can be understood via the DC analysis of the schematic.
  For NMOS, the transconductance is given as,

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

  As the value of source resistance is increased, the drain current I_D decreases, hence transconductance g_m decreases, which in turn, decreases the gain of the CS amplifier.

Conclusion

In this experiment, we simulated a CS amplifier and studied the effect of changing values of width of NMOS device, load resistance, drain resistance and source resistance on the gain and the bandwidth of the amplifier. The results can be summarized as,

Parameter	***Change in Gain with increase in parameter value***	***Change in Bandwidth with increase in parameter value***
Width of NMOS	Increases	Remains constant
Load resistance	Increases	Decreases
Drain resistance	Increases	Decreases
Source resistance	Decreases	Remains constant