DIGITAL ELECTRONIC CIRCUITS LAB

EXPERIMENT 9

Utkarsh Patel (18EC30048)

Objective

- To implement a (4×4) bit multiplier using registers and down-counters

Circuit Diagram

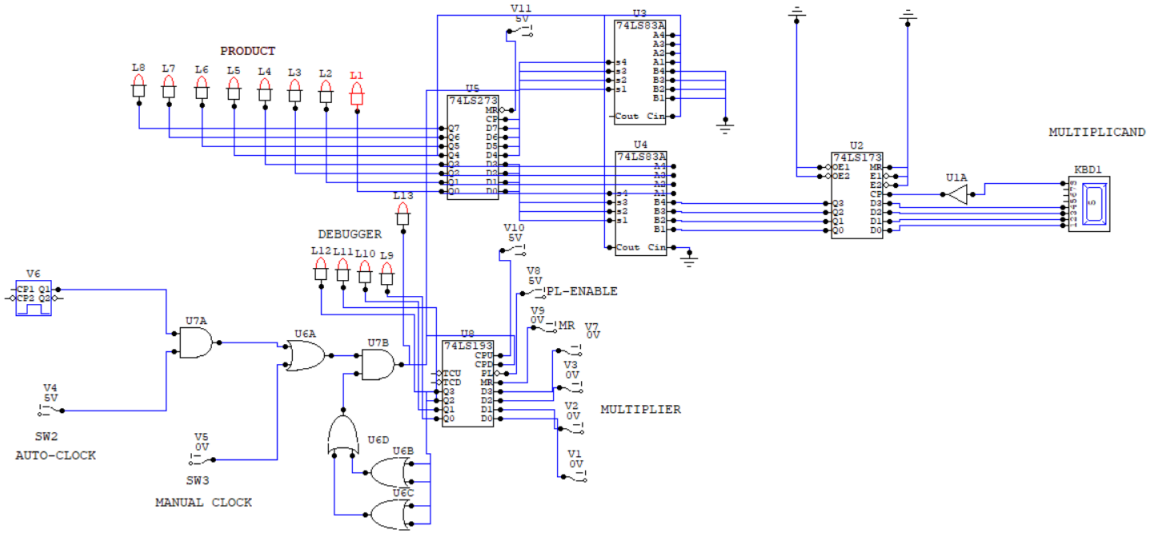

Fig 1. Circuit designed for the experiment

Discussion

1. In this experiment, a (4×4) bit multiplier is to be realised. Hence, we have a 4 bit *multiplicand* and a 4 bit *multiplier*. The product will be a 8 bit unsigned integer.
2. For taking *multiplicand* as input, *ASCII* keyboard is used, and for taking *multiplier* as input, logic switches are used. For displaying the product, we used 8 LED lamps.
3. The *multiplicand* is saved in IC 74173, which is a quad DFF with input and output enable, here acting as a register.
4. The *multiplier* is fed as input to IC 74273, which is a synchronous dual counter. For this experiment, we are using the down-counter only, hence the forward-counter is set to active high (inactive).
5. Now, standard multiplication algorithm is followed. The *multiplicand* is added recursively using feedbacks and IC 7483 until the *multiplier* reduces to one. As we are decreasing the multiplier in each pass, that's why we used the down-counter.

SIMULATION

6. We input the *multiplicand* in the *ASCII* keyboard, and provide the *multiplier* to IC 74273. Writing into IC 74273 is done as follows:
    a. Set MR to active high, and then reset it to active low so as to reset $Q_3Q_2Q_1Q_0$ to 0000.
    b. Reset $PL - enable$ to active low, provide the *multiplier* using logic switches, and set $PL - enable$ back to active high. Doing so, we are making $Q_3Q_2Q_1Q_0 = multiplier$.
7. For this experiment, two types of control enable are provided for clock: Manual and automatic. In each case, a $0 \rightarrow 1$ transition reduces $Q_3Q_2Q_1Q_0$ by 1. A special care has to be taken for case when $Q_3Q_2Q_1Q_0 = 0000$. In this case, if a $0 \rightarrow 1$ transition is provided to CPD terminal, $Q_3Q_2Q_1Q_0$ becomes 1111. Hence, to avoid this situation and to end the iteration when $Q_3Q_2Q_1Q_0 = 0000$, we use a auto-clock enable given as $E = Q_3 + Q_2 + Q_1 + Q_0$. If E becomes active low, the iteration ends and the final output is displayed as product.