DIGITAL ELECTRONIC CIRCUITS LAB

EXPERIMENT 10

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Objective

- To implement a (4 × 4) bit serial parallel multiplier

Required Components

S. No.	Component	Use
1	IC 7495	It is a 4 – bit shift register. Required for getting each bit of multiplier one at a time from LSB to MSB.
2	IC 7483	It is a 4 – bit adder. Two of them are required in this experiment to design 8 – bit adder.
3	IC 74273	It is an 8 – bit positive edge triggered DFF with active low MR. It is required to store the current partial sum.

Circuit Diagram

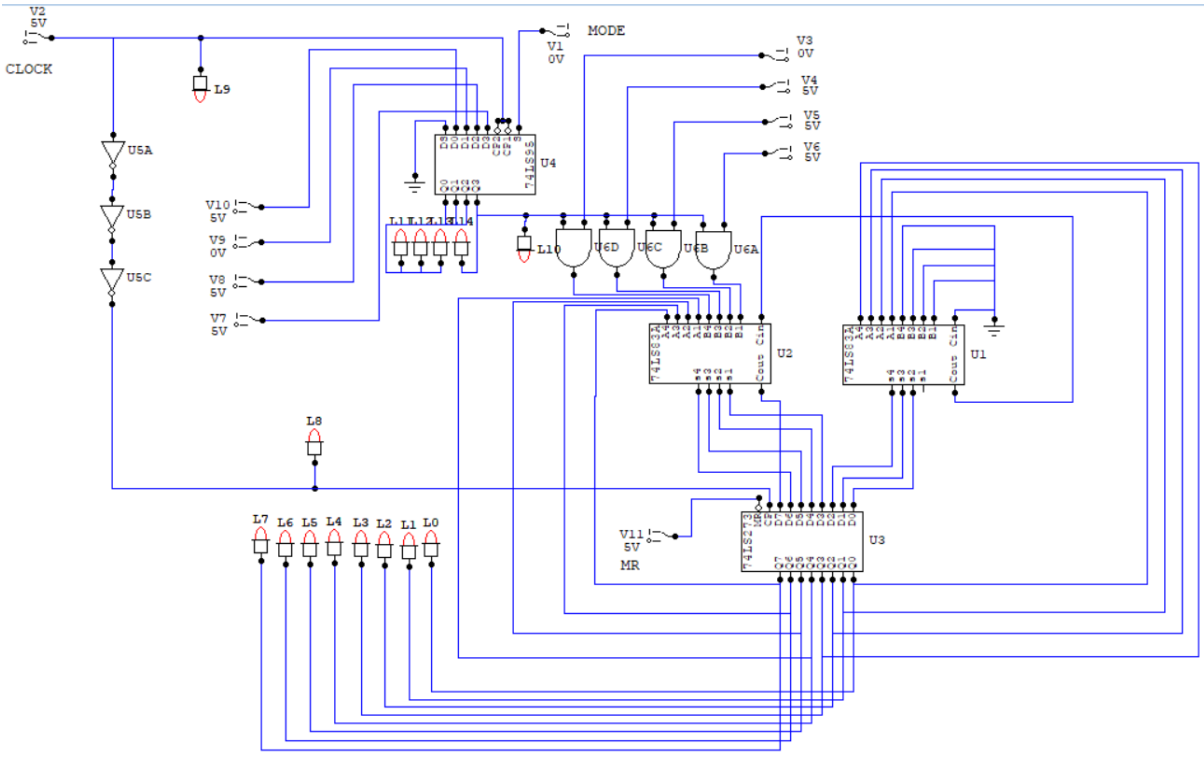

Fig 1. Circuit designed for the experiment

Discussion

1. In this experiment, a (4×4) bit serial parallel multiplier is to be designed.

2. Let $A = a_3a_2a_1a_0$ be the multiplicand and $B = b_3b_2b_1b_0$ be the multiplier. The standard multiplication algorithm is used in this experiment. Let $P = p_7p_6p_5p_4p_3p_2p_1p_0$ be the required product. Then, it is known that $P = 2^3PP_3 + 2^2PP_2 + 2^1PP_1 + 2^0PP_0$ where $PP_i = A * b_i$ is the partial product. Multiplying by powers of 2 simply left shifts the given partial product.

3. **Algorithm used:** For computing the final product, we need to compute the partial products first. We designed an $8-$ bit adder that computes $Z = \frac{1}{2}(X + Y)$, and instead of realizing PP_i, we computed $2^4PP_i, i = 0 \ldots 3$. The algorithm is as follows:

   $Z \coloneqq 0, i \coloneqq 0$
   $LOOP$
   $\quad X \coloneqq 2^4PP_i; Z \coloneqq \frac{1}{2}(Z + X); i \coloneqq i + 1;$
   $UNTIL(i < 4)$

   When the loop terminates, it is easy to observe that $Z = P$.

4. **SIMULATION**
   - The multiplier $B = b_3b_2b_1b_0$ is fed to IC 7495 by connecting b_3, b_2, b_1, b_0 to D_0, D_1, D_2, D_3 respectively and S is set to low, and a manual clock is provided and then S is set to high again. Doing this we will have $Q_0Q_1Q_2Q_3 = b_3b_2b_1b_0$, Q_0 is the MSB here, and Q_3 is the LSB.
   - For computing the partial products, S must be set to low all the times. The required bit of multiplier can be accessed from Q_3 terminal. We then apply a manual clock pulse. During the $1 - 0$ transition, $Q_0Q_1Q_2Q_3$ becomes $D_sQ_0Q_1Q_2$. As D_s is set to logic low, this operation is a right shift. This $1 - 0$ transition is basically a $0 - 1$ transition for IC 74273 (as 3 inverters are placed in its path, it is also done to generate a delay for the proper operation) and then it performs the operation for the given iteration as specified in the algorithm.
   - After 4 such operations, the required product will be computed.