DIGITAL ELECTRONIC CIRCUITS LAB

EXPERIMENT 11

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Objective

- To implement an 8 – bit binary to BCD converter

Circuit Diagram

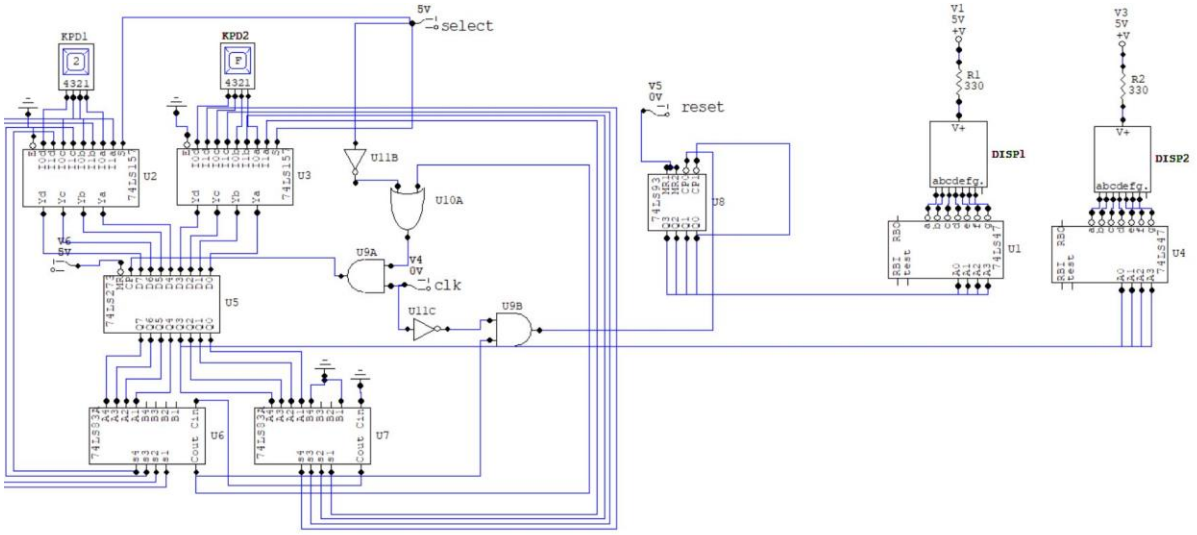

Fig 1. Circuit designed for the experiment

Simulation

In the following simulation, I have provided hexadecimal input 2*F* which corresponds to 0010 1111 in binary. We can see that the decimal number to be obtained will be 47. The same was observed as the output in the 7-segment displays.

https://drive.google.com/file/d/1oDHpanbUW0bZl-If_A9In50BQfXM3g0r/view?usp=sharing

Discussion

- In this experiment, an $8-$ bit binary to BCD converter is designed.
- For this purpose, I used:
  - IC 74157 (Qnty - 2) which is a quad 2-to-1 MUX
  - IC 74273 (Qnty - 1) which is an octal positive edge triggered DFF
  - IC 7483 (Qnty - 2) which is a 4 –bit adder
  - IC 7493 (Qnty - 1) which is a MOD16 counter with negative edge trigger
- The *select* was initially set to 0 so that the original binary number can be copied to register, after this, *select* was set to 1 throughout the experiment.
- At the start of the experiment, IC 74273 and IC 7493 were reset using MR.
- **Algorithm:** Let $B = b_7b_6b_5b_4b_3b_2b_1b_0$ and let in its BCD representation, BD_1 denotes four MSBs and BD_2 represents four LSBs. Then, we can obtain BD_1 and BD_2 as follows:

```
1. cnt := 0
2. let B be the binary representation of the number and D be decimal
   representation
3. while (D > 10) do
4.     D := D – 10
5.     cnt := cnt + 1
6. BD1 := cnt; BD2 := LSB4(B)
```

- Manual clock pulse was given to carry out the steps of the algorithm.
- Step 4 of the algorithm is carried out by two IC 7483.
- Step 5 of the algorithm is carried out by IC 7493
- Condition check in Step 3 of the algorithm is given by the value of c_{out} of the $8-$ bit addition. However, in practice, it is or-ed with compliment of *select*.
- Final output is displayed using 7-segment displays.