

CA Assignment - 2

Serial Bus

Serial bus system - It has 6 registers each can store 4 bits of data.

Other components used are - 3x8 decoders, 2x1 Mux, OR gates, etc.

To transfer data from one register to another(bit-wise), we have implemented a serial bus.

Variables :- A, B ,C ,D ,A' ,B' , C'.

Step - 1:- To load registers

- Initially all the variables(A,B,C,D,A',B',C') must be set to 0.
- Then, provide inputs to the registers(Input 0 to Input 5).
- Change the clock cycle.
Finally values will be loaded to all the registers.

Step - 2:- To transfer values.

- Now set D as 1.
- Select the source register using the variables A, B, C.
(Change value at 2 place)
- Select the destination register using the variables A', B', C'.
- Change the clock cycle.
Finally the source value will reach the destination.

In this system single bit is transferred,

Thus, at the source circular shift will take place and at destination shift operation will occur(on the basis of the source bit transferred)

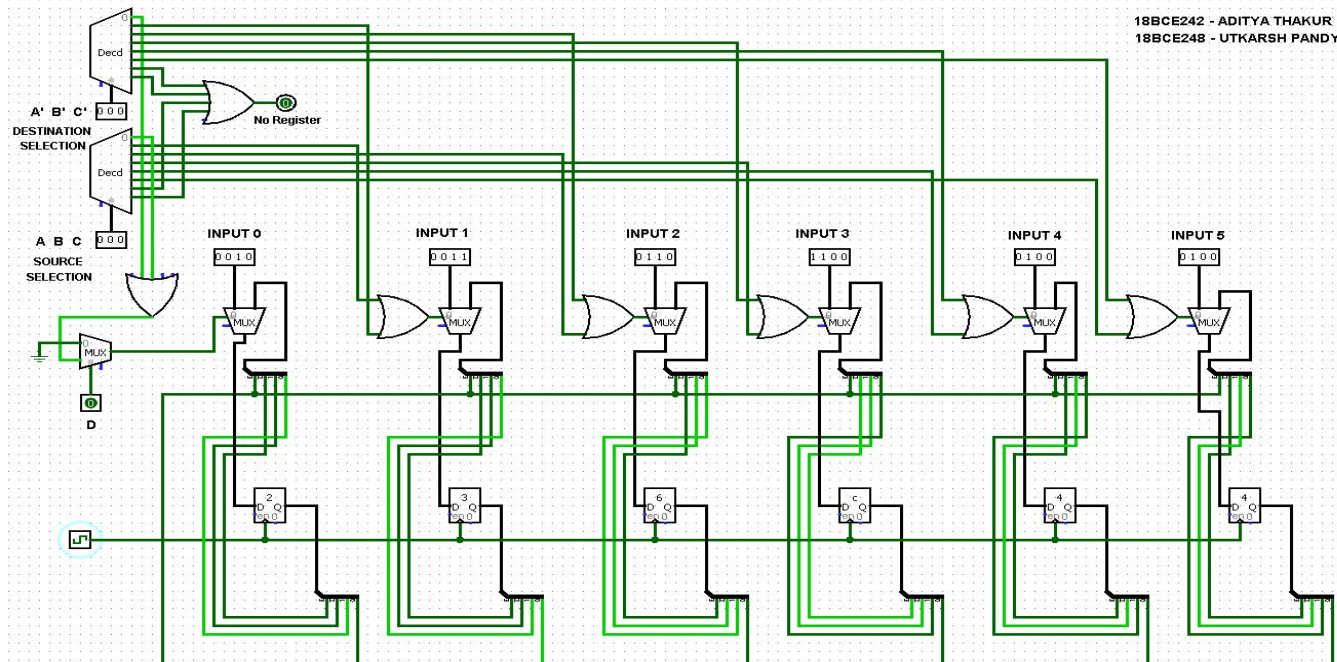
➤ Values are loaded into the registers.

A B C - ARE USED TO SELECT SOURCE REGISTER
A' B' C' - ARE USED TO SELECT DESTINATION REGISTER
INITIALLY FOR LOADING INPUT TO ANY REGISTER,
ALL THE VARIABLES A, B, C, A', B', C', D MUST BE 0

SERIAL BUS

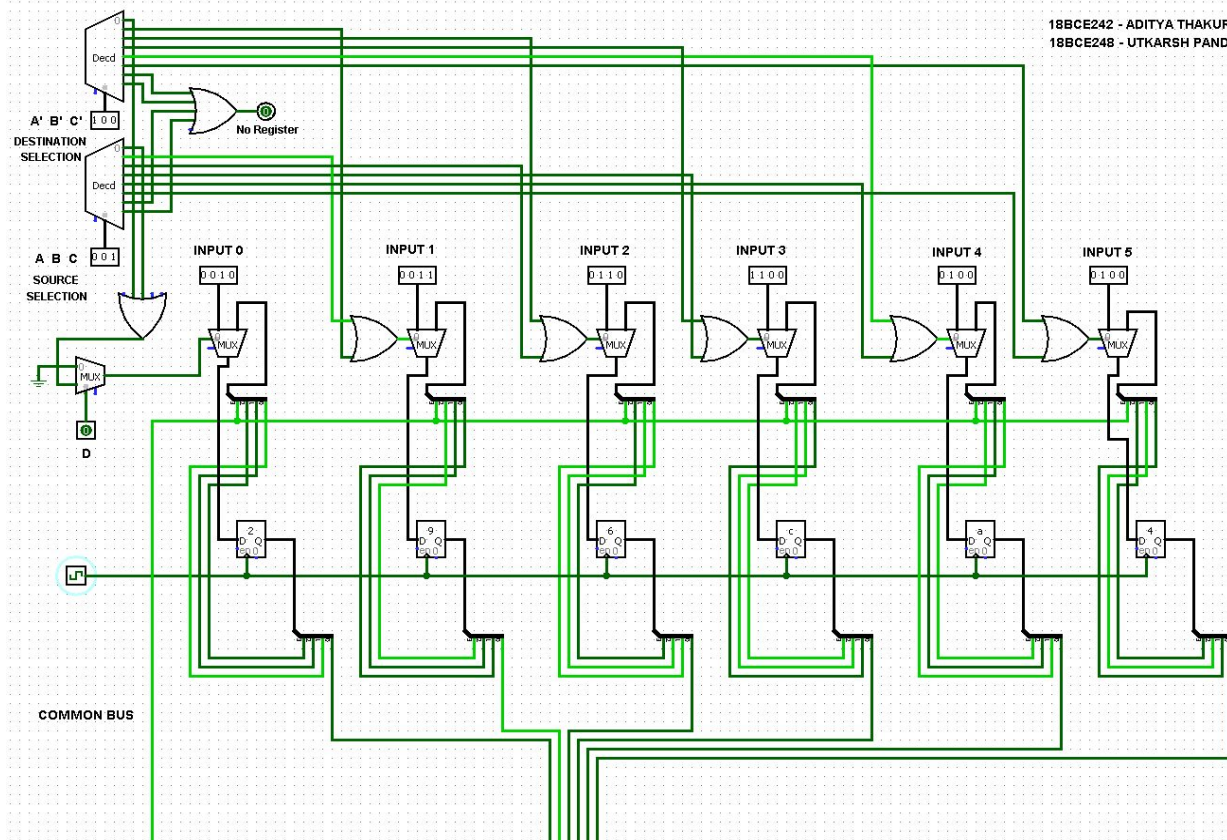
SOURCE - Circular Shift Operation
DESTINATION - Shift Operation

18BCE242 - ADITYA THAKUR
18BCE248 - UTKARSH PANDYA



➤ After the Shift Operation

18BCE242 - ADITYA THAKUR
18BCE248 - UTKARSH PANDYA



Example (From above image) :-

Initial value in Register 0 :- 2 (0010)

Initial value in Register 1 :- 3 (0011)

Initial value in Register 2 :- 6 (0110)

Initial value in Register 3 :- C (1100)

Initial value in Register 4 :- 4 (0100)

Initial value in Register 5 :- 4 (0100)

Variable :-

- Source : ABC - 001 (Reg - 1)
- Destination : A'B'C' - 100 (Reg - 4)
- Means transferring the least significant bit of Reg-1 to Reg-4

Register 0 :- 2 (0010) No change

Register 1 :- 9 (1001) Circular shift operation in source(Reg - 1)

Register 2 :- 6 (0110) No change

Register 3 :- C (1100) No change

Register 4 :- A (1010) source bit(Reg - 1) is transferred to destination(Reg - 4)

Register 5 :- 4 (0100) No change