Design of Energy Efficient High Speed Parallel ADC

A PROJECT REPORT

Submitted by

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BONAFIDE CERTIFICATE

Certified that this project report "**Design of Energy Efficient High Speed Parallel ADC"** is the bonafide work of "**Bhanuday Bharadwaj (20BEC1145), Shagun (20BEC1014), Utkarsh Singh (21BEC8006)**" who carried out the project work under my/our supervision.

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INTERNAL EXAMINER	**EXTERNAL EXAMINER**

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CHAPTER 1: INTRODUCTION

1.1 Identification of client/need/relevant contemporary issue

An analog signal is a constantly fluctuating illustration of a circumstance, which may be directly measured the human voice, video, radio, and others. Alternatively, a digital signal is presented inside the form of bits, and at any given time it is able to take simplest constrained number of values, as an example, in case of a virtual pc, there are best states which are either one or zero. An analog signal generates non-stop records, even as a virtual signal includes discrete facts. An analog-to-virtual converter (ADC) is a digital integrated circuit that converts analog signal (non-stop information) into digital shape (discrete records).

Growing disposable profits and technological advancements complement the analog-to-digital converters market but complicated layout of the ADC hampers this marketplace growth. Therefore, encouragement in digitization of work tactics by government in rising economies, and continuous aggressive pressure to broaden excessive-overall performance and efficient tool is expected to present numerous possibilities for market enlargement.

1.2 Identification of problems

Understanding the Logic and Design of Energy Efficient High-Speed Parallel ADC. Design an energy-efficient high-speed parallel ADC that can maintain high performance while minimizing power consumption. Reducing power consumption and enabling faster data processing without compromising accuracy. The modelling and design of ADC for Low Power Applications. The theory of operation of comparators is explored, and a model to predict the transient behavior of 45 nm is represented. Stimulating them under specified test benches.

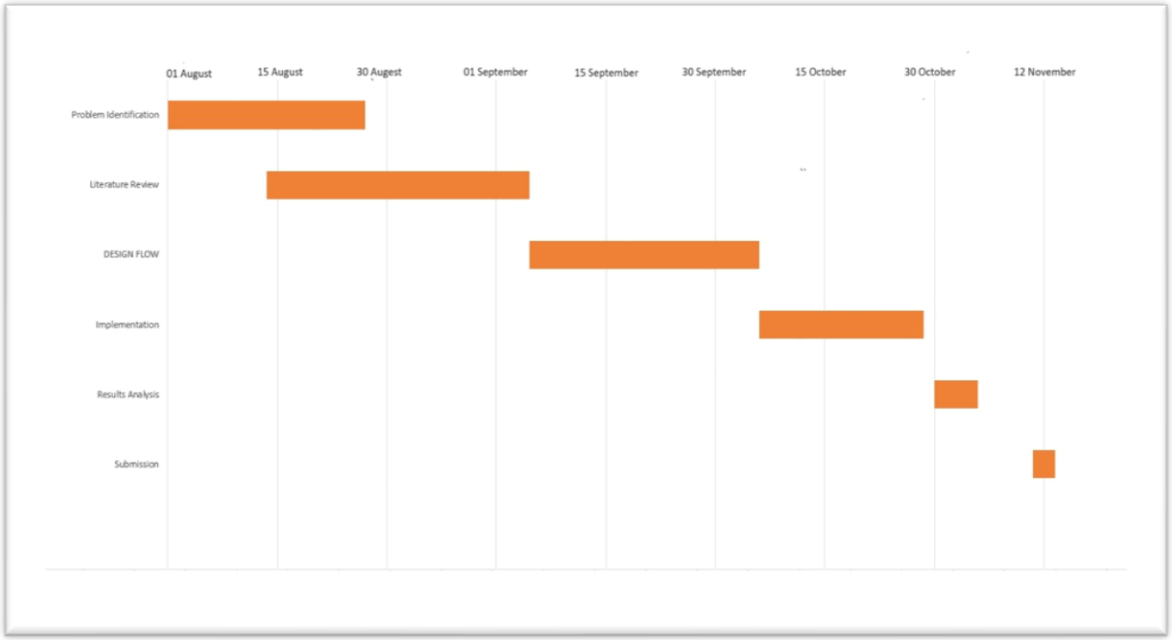
1.3 Identification of Task

This project cab be executed by performing the underlying steps in a distributed and systematic manner:

1. Study about the analog to digital converter.
2. Read papers and prepare a literature review.
3. Division of task among the three team members.
4. Discussions of about the different ways to convert analog to digital signal.

5. Design the comparators.
6. Used comparators in ADC circuit design.

1.4 Timeline



1.5 Organization of the report

The report begins with an introduction about the analog to digital converters and also about the comparators. Then, it talks about the software platform virtuoso cadence where the ADC circuit is design.

After that, it lists the literature reviews about the various papers we have referred listing their key findings and potholes. Specifying the problem statement and goals and objective of the project.

After that, we discussed the design flow process, where the report discussed the flow of our design as well as the limitations of the design, feature analysis, and finalisation. We also discussed the design's execution and methodology.

After that, we hired someone to analyse and validate the results. The study concludes by outlining the project's future scope and the conclusions reached. Finally, we have offered the project's references.

1.6 Introduction to Analog to Digital Converter

Almost all environmental variables that can be measured are analog, such as temperature, sound, pressure, and light. Consider a temperature monitoring system where digital computers and processors are unable to acquire, analyse, and analyse

temperature data from sensors. Therefore, in order for this system to connect with digital processors like microcontrollers and microprocessors, an intermediary device is required to transform the analog temperature data into digital data. Analog to digital converters (ADCs) are electrical integrated circuits that are used to transform analog signals, like voltages, into binary (or digital) form, which consists of 1s and 0s. Most ADCs take voltage inputs ranging from 0 to 10V, -5V to +5V, and so on, and output a binary integer as a digital value in response.

1.6.1 What is Analog to Digital Converter?

An Analog to Digital Converter (ADC) is a crucial component in electronics that transforms continuous analog signals into discrete digital signals. It's commonly used in various devices like smartphones, digital cameras, sensors, and more.

The primary function of an ADC is to convert real-world analog signals, which are continuously variable in amplitude, into digital data, which consists of discrete values or binary numbers. This conversion enables digital processing, storage, and manipulation of the signals, making it easier to transmit, store, and analyze information.

ADCs work by sampling the input analog signal at specific intervals, measuring its amplitude at each sample point, and assigning a digital value to represent that amplitude. The rate at which the signal is sampled (sampling frequency) and the precision of the digital representation (in bits) affect the accuracy of the converted digital signal.

The main features of ADC are Two types-

- **Sample Rate:** This refers to how frequently the analog signal is measured and converted into its digital counterpart.
- **Bit Resolution:** This refers to the number of bits used to represent each sample of the analog signal.

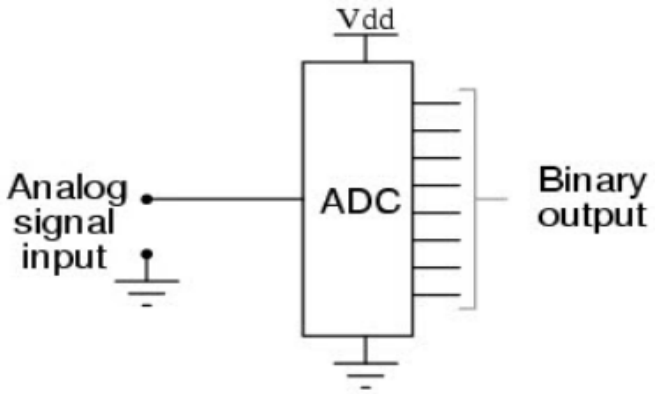


Fig.1.6.1 Analog to Digital Converter

One of the key benefits of an ADC converter is its high data collecting rate, even with multiplexed inputs. The precision and speed of data acquisition from many sensors have risen with the development of multiple ADC integrated circuits (ICs). High-performance ADCs are characterised by better measurement repeatability, low power consumption, precise throughput, high linearity, strong signal-to-noise ratio (SNR), and other dynamic features.

Among the many applications for ADCs are measurement and control systems, industrial instruments, communication systems, and all other sensory-based systems. ADCs are grouped based on a variety of factors, including cost, bit rates, power consumption, and performance.

1.6.2 ADC Block Diagram

The block diagram of ADC includes the quantize, hold, sample and encoder. Following the process of ADC can be like, the analog signal is first applied to the first block, which is a sample, whenever a precise sampling frequency can be achieved. Within the second block, similar to Hold, the sample's amplitude value can be held as well as maintained. Through the third block like quantize, the hold sample can be quantized into a discrete value. A binary number is created from the discrete amplitude by the final block-style encoder.

Sample: The analog signal can be sampled at a precise interval of time in the sample block. Sampling, in the context of signal processing, refers to the process of converting a continuous signal (analog) into a series of discrete data points at specific intervals in time. This process allows the representation of a continuous-time signal in a discrete format, making it suitable for digital processing, transmission, and storage. Although

the samples are discrete with respect to time, they are employed in continuous amplitude and have real value. The sample frequency is crucial for converting the signal. Consequently, a precise rate can be maintained. Sampling is a critical concept in digital signal processing, allowing the representation and manipulation of real-world analog signals in various digital systems. The sample rate can be fixed based on the needs of the system.

Sampling- The continuous analog signal is sampled at specific intervals in time. This process captures the analog signal's amplitude or voltage at discrete points in time.

Sampling Rate- The rate at which the signal is sampled is defined by the sampling frequency or sampling rate, measured in samples per second (Hz) or samples per unit time. The Nyquist-Shannon Sampling Theorem guides the choice of the sampling rate to avoid aliasing.

There are three sample methods are-

- **Ideal Sampling:** It is also known to as Instantaneous Sampling. Ideal sampling samples pulses from an analog stream. This is the best sampling technique. However, it is difficult to use. Ideal sampling refers to the theoretical process of capturing a continuous analog signal at precise intervals to produce a sampled representation without introducing any distortion or loss of information. In an ideal sampling scenario, the sampling process perfectly captures the original analog signal without any aliasing or degradation.

  While ideal sampling is a theoretical concept, real-world systems aim to achieve sampling as close to ideal as possible. Engineers employ anti-aliasing filters, high-quality analog-to-digital converters (ADCs), and proper sampling techniques to minimize distortions and accurately represent analog signals in digital form.

  Despite the challenges and limitations, striving for ideal sampling remains a fundamental goal in signal processing, ensuring accurate and reliable conversion of analog signals to digital representations for a wide array of applications in modern technology.

- **Natural Sampling:** It is a useful sampling technique in which each pulse has a finite width equal to T. The outcome is a series of samples that keep the analog signal's structure. Natural sampling, also known as zero-order hold sampling or impulse sampling, is a type of signal sampling method used in analog-to-digital

conversion. Unlike ideal or conventional sampling methods, natural sampling involves holding the value of the input signal constant between discrete sampling instants.

While natural sampling provides a straightforward method to comprehend sampling concepts, its practical application is limited due to its inherent shortcomings, especially in high-fidelity analog-to-digital conversion scenarios. More advanced sampling methods and reconstruction techniques are typically employed in modern signal processing to achieve more accurate representations of analog signals in the digital domain.

- **Flat top sampling:** This type of sample is simpler to get than natural sampling. This sampling method uses a circuit to keep the samples' tops constant. The most used sampling technique is this one. Flat-top sampling, also known as flat-top windowing, is a signal processing technique used in data acquisition and analysis to reduce spectral leakage or distortion in the frequency domain caused by finite-length sampling of signals with non-integer periodicity.

  Flat-top sampling is a signal processing technique employed to mitigate spectral leakage in frequency analysis, allowing for more accurate identification and estimation of frequency components present in signals during spectral analysis.

Hold: It is the second block in an ADC and serves no use other than to hold the sample amplitude until the subsequent sample is collected. Therefore, hold's value doesn't change until the following sample. an Analog-to-Digital Converter (ADC), "hold" refers to a specific stage or component within the ADC circuitry known as the sample-and-hold (S/H) circuit. The sample-and-hold circuit is a fundamental component within many ADCs. Its primary function is to "sample" the input analog voltage at discrete intervals and "hold" that voltage steady long enough for the ADC to convert it into a digital value. the "hold" phase in an ADC's sample-and-hold circuit is the stage where the captured analog voltage is maintained steady and unchanged, providing a stable input for the ADC's conversion process, ensuring accurate and reliable digital conversion of analog signals.

Quantize: This third block of an ADC is primarily utilised for quantization. This has the primary purpose of changing the amplitude from continuous (analog) to discrete. Quantization is a fundamental concept in digital signal processing and analog-to-digital conversion, involving the process of approximating or representing continuous analog

values with a finite set of discrete values. The hold block's continuous amplitude value transitions into discrete amplitude during the quantize block. Since the signal now contains discrete amplitude and time information, it will be in digital form.

Quantization is an essential process in converting analog signals to digital form, enabling digital signal processing and manipulation. Balancing resolution, quantization error, and dynamic range considerations is crucial in achieving accurate and efficient representation of analog signals in digital systems.

Quantization- After sampling, the continuous amplitude values obtained are mapped to a finite set of discrete digital values. This involves dividing the continuous range of analog voltage levels into a limited number of discrete levels or bins.

Resolution- The number of bits used for quantization determines the resolution of the digital representation. Higher resolution (more bits) allows for finer distinctions between analog levels, resulting in higher accuracy.

Encoder: An encoder, the last component of the ADC, transforms the signal from digital to binary form. An encoder is a component or circuitry responsible for converting the output of the ADC into a digital code. We are aware that binary signals are used to operate digital devices. Therefore, using an encoder, it is necessary to convert the signal from digital to binary. So, this is how an ADC converts an analog signal to a digital one. The full conversion can be completed in less than one microsecond. The quantized levels are then encoded into digital values, typically using binary code. Each quantized level is represented by a specific binary code, forming the digital output of the ADC.

In an ADC, the encoder serves a critical role in converting the ADC's analog-to-digital converted output into a digital code, facilitating the representation of analog signals in the digital domain for further processing, analysis, or transmission within digital systems.

1.6.3 Analog to Digital Conversion Process

Analog to digital signal conversion can be done using a variety of techniques. These converters are increasingly used as a bridge between analog and digital signal processing, with output displayed on an LCD via a microcontroller. Finding the output signal word that corresponds to an analog signal is the goal of an A/D converter.

The ADC's performance can be assessed by its performance in relation to several aspects. The next two key elements are outlined below based on that.

A digital signal is one that can only take on one of a finite number of values at any given time and expresses data as a sequence of discrete values.

Any continuous signal that exhibits time variation and is a representation of another time-varying quantity, or is equivalent to another time-varying signal, is said to be an analog signal.

1.6.4 Factors of Bandwidth

a. **SNR (Signal-to-Noise Ratio):** The Signal-to-Noise Ratio (SNR) is a measure used to quantify the level of signal strength compared to the level of background noise present in a system or a signal. Science and engineering employ the signal-to-noise ratio (SNR) to compare the strength of a desired signal to the strength of background noise. It is described as the signal-to-noise power ratio, which is frequently given in decibels.

   Signal- Represents the desired or useful information or the strength of the primary signal being measured or processed.

   Noise- Refers to unwanted or random fluctuations or disturbances that obscure or interfere with the signal.

   The SNR is typically expressed in decibels (dB) and is calculated as the ratio of the power of the signal to the power of the noise.

   SNR (dB)=10log10(Noise Power/Signal Power) The Signal-to-Noise Ratio serves as a critical metric in assessing the quality and reliability of signals in various systems. A higher SNR signifies a stronger, more discernible signal compared to background noise, contributing to clearer, more accurate signal processing, communication, and data transmission.

b. **Bandwidth:** An ADC's bandwidth can be calculated by estimating the sampling rate. To create discrete values, the analog source can be sampled repeatedly per second. The basic swept frequency's spectral output, as determined by the FFT analysis, is lowered by 3 dB at the frequency that defines an ADC's analog bandwidth.

   Bandwidth refers to the range of frequencies that a system can handle or the amount of data that can be transmitted in a fixed amount of time.

   For instance, in the context of an internet connection, bandwidth often refers to the maximum data transfer rate or capacity of that connection. The higher the bandwidth, the more data can be transmitted in a given amount of time, allowing for faster internet speeds.

In terms of signals or circuits, bandwidth can refer to the range of frequencies within a continuous set of frequencies that a circuit can handle without significant loss of signal or distortion. It's a measure of how much information or signal can be passed through a system.

Bandwidth is crucial in various electronic applications, whether in communication systems, signal processing, or networking, as it directly influences the speed and efficiency of data transmission.

1.7 Types of Analogs to Digital Converters

Analog to digital converters come in a variety of varieties, some of which include:

- Dual Slope A/D Converter
- Flash A/D Converter
- Successive Approximation A/D Converter
- Semi-flash ADC
- Sigma-Delta ADC
- Pipelined ADC

i. Dual Slope A/D Converter:

The comparison voltage for this type of ADC converter is provided by an integrator circuit consisting of a trio of operational amplifiers, a resistor, and a capacitor. From zero to the predetermined value of Vref, the integrator's output displays a sawtooth waveform. When the integrator waveform is started, the counter starts counting and goes from 0 to 2^n-1, where n is the ADC's bit count. An analog-to-digital converter that operates on the basis of integrating an unknown input voltage for a predetermined amount of time and then discharging it using a predetermined amount of time and a known reference voltage is called a dual slope analog-to-digital converter (ADC).

Dual Slope ADCs are known for their inherent noise rejection capabilities because noise affecting the measurement during the integration phase also affects the measurement during the discharge phase in the opposite direction, canceling out to some extent. This makes them suitable for applications requiring good resolution and accuracy, such as in multimeters and precision measurement instruments.

However, they may not be the fastest ADCs available due to the sequential nature of their operations, which can result in slower conversion rates compared to some other types of ADCs like successive approximation or flash ADCs.

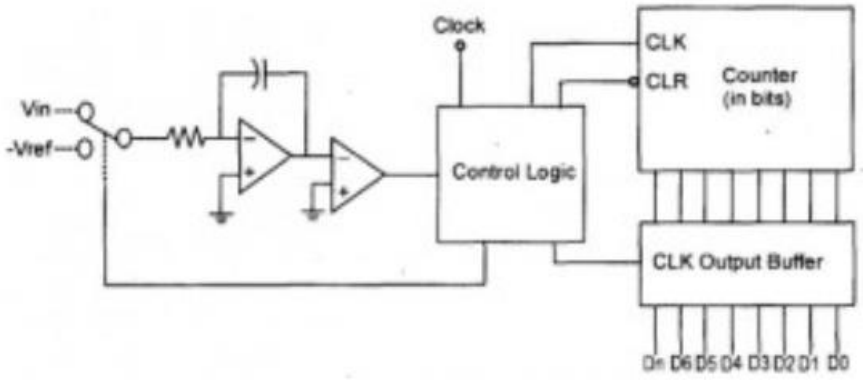


Fig.1.7.1 Dual Slope Analog to Digital Converter

ii. Flash A/D Converter

Three operational amplifiers, a resistor, and a capacitor make up the integrator circuit that supplies the comparison voltage for this kind of ADC converter. The output of the integrator shows a sawtooth waveform from zero to the preset value of Vref. The counter counts from 0 to 2^n-1, where n is the bit count of the ADC, when the integrator waveform is initiated. Dual slope analog-to-digital converters (ADCs) are those that function by first integrating an unknown input voltage for a predefined period of time, and then discharging it using a predetermined period of time and a known reference voltage.

Due to their speed and simplicity, flash ADCs are commonly used in applications like high-speed data acquisition, telecommunications, and applications where rapid conversion is essential, even if at the expense of power or complexity.

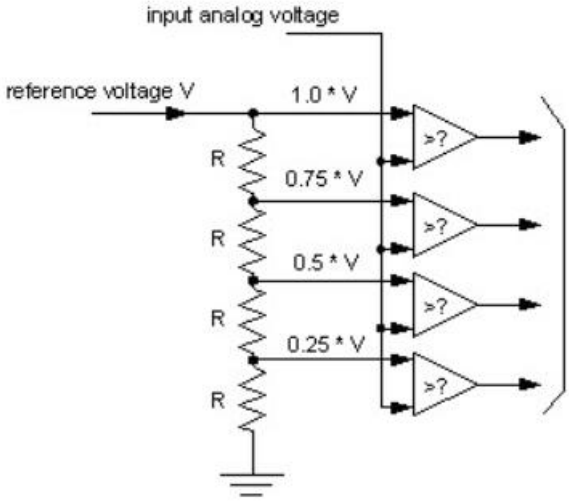


Fig.1.7.2 Flash A/D Converter

Flash ADCs are known for their high speed because they perform all the comparisons simultaneously. However, they have some limitations, especially in terms of the number of comparators required. To achieve higher resolution (more bits of output), a large number of comparators are needed, leading to increased complexity, power consumption, and cost.

As a result, Flash ADCs are often used in applications where speed is paramount, such as in high-speed data acquisition, digital oscilloscopes, and other systems where real-time conversion of analog signals to digital data is critical.

iii. Successive Approximation A/D Converter

The SAR ADC is a relatively new ADC integrated circuit that operates at a significantly faster pace than dual slope and flash ADCs because it uses digital logic to converge the analogue input voltage to the nearest value. This circuit consists of a comparator, output latches, D/A converter, and sequential approximation register (SAR). An analog-to-digital converter, or successive approximation ADC, is a popular kind of ADC that strikes a compromise between speed and resolution. Using a binary search technique, it approximates the analogue input voltage to its digital counterpart one step at a time.

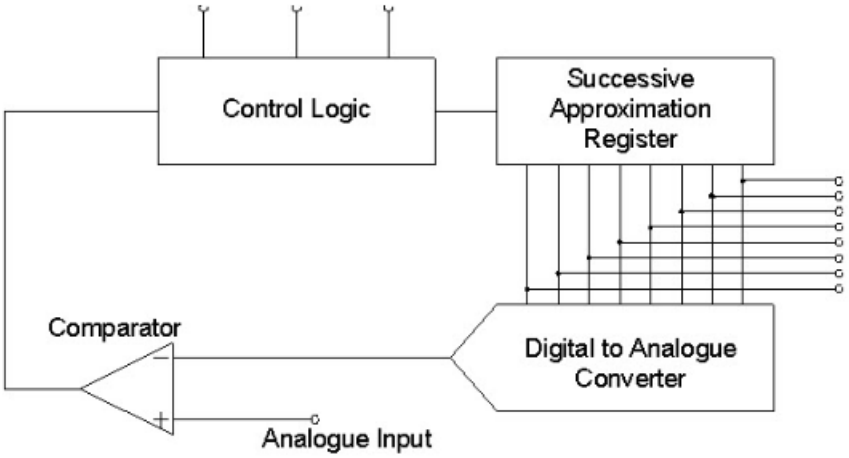


Fig.1.7.3 Successive Approximation A/D Converter

When the LOW to HIGH transition is implemented, the MSB is set, and the SAR is reset at the start. Next, a D/A converter is used to construct the analogue version of the MSB, and the output is compared to the analogue input Vin. If the output of the comparator is LOW, the SAR will clear the MSB. If not, the MSB will be shifted to the next location. Up until Q0, when the SAR results in the parallel output lines containing proper data, all the bits are verified in this way.

Successive Approximation ADCs offer good resolution and are relatively faster than some other types (e.g., dual slope ADCs) due to their iterative but systematic approach. They strike a balance between speed and complexity compared to Flash ADCs, which are faster but can be more complex for higher resolutions.

These ADCs are commonly found in various applications, including sensors, data acquisition systems, and audio devices, where moderate speed and resolution are required. They are also popular in microcontrollers and other embedded systems due to their efficient use of resources and moderate speed/resolution trade-off.

iv. Semi-Flash ADC

A Semi-Flash Analog to Digital Converter (ADC) is a hybrid design that combines elements from both flash and successive approximation ADC architectures. It aims to strike a balance between the speed of a flash ADC and the reduced hardware complexity of a successive approximation ADC.

v. Sigma-Delta ADC

The Sigma-Delta Analog to Digital Converter (ADC) is an advanced type of converter known for its high resolution and suitability for high-precision

applications, particularly where high-resolution measurements and low noise are essential.

vi. Pipelined ADC

A Pipelined Analog to Digital Converter (ADC) is a high-speed, high-resolution converter architecture that divides the analog-to-digital conversion process into several stages, or pipeline stages, to achieve both high speed and high resolution.

• It is used for a coarse conversion. This converter functions as a better conversion by permitting a temporary conversion with a range of bits. The change is then evaluated with respect to the input signal.

•By striking a compromise between SARs and flash analogue to digital converters, pipelined systems usually offer a high resolution, fast speed, and compact size.

Pipelined ADCs offer advantages of both speed and high resolution by breaking down the conversion process into smaller, more manageable stages. They can achieve higher speeds compared to successive approximation or dual slope ADCs, making them suitable for applications where both speed and resolution are critical, such as in communication systems, high-speed data acquisition, and imaging devices.

However, they can be more complex and require precise calibration between stages to maintain accuracy. The complexity and power consumption increase with the number of stages, which can affect their practical implementation in some applications.

1.8 Comparator

A comparator is a fundamental component in electronics used to compare two voltages or currents and determine their relationship: whether one voltage is greater than, less than, or equal to the other. It's a building block in various circuits and plays a crucial role in many applications, especially in analog-to-digital conversion.

A comparator in electronics is a circuit or device used to compare two voltages or analog signals and determine their relationship: whether one is greater than, less than, or equal to the other. It takes in two analog voltage inputs (often labelled as V+ and V-) and produces a digital output based on the comparison result. The output is typically in the form of a logic signal, where one state (usually high or '1') indicates that V+ is greater than V-, and the other state (usually low or '0') indicates the opposite.

The peration of a comparator is quite simple: if V+ is greater than V-, the output is at one logic level; if V+ is less than V-, the output is at the other logic level. Most comparators have very high gain and are designed to quickly respond to changes in input voltages.

1.8.4 Types of Comparators

There are two types of comparators are:

a. Inverting
b. Non-Inverting

Inverting: Analog to Digital Converters (ADCs), the term "inverting" typically refers to the architecture or configuration of the input stage rather than the concept of inverting signals as seen in operational amplifiers. An ADC can have various input configurations, and one common configuration is the differential or single-ended input.

An inverting comparator is a type of comparator circuit used in electronics to compare two voltages and produce an output based on their relationship. Comparators are often used in analog-to-digital converters (ADCs), oscillators, and control systems.

The inverting comparator, specifically, is a comparator with negative feedback that drives its non-inverting terminal to a specific voltage level, often ground (0 volts).

The following schematic depicts the circuit for an inverting comparator.

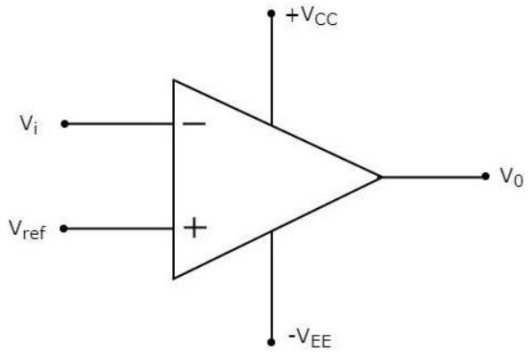


Fig. 1.8.1 Diagram of Inverting

The behavior makes the inverting comparator act like a digital switch, producing a binary output based on whether the input voltage is higher or lower than the reference voltage.

In practical applications, this functionality is useful for tasks like threshold detection, where the comparator's output switches states based on whether the input voltage crosses a certain threshold level. This switching behavior finds applications in various electronic systems, such as in window comparators, voltage level detectors, and zero-crossing detectors.

Non-Inverting: Analog to Digital Converters (ADCs), the terms "non-inverting" and "inverting" are not commonly used as they are in operational amplifiers. However, the concept of non-inverting can be loosely applied when discussing the input configurations or stages within an ADC. A non-converting comparator is a type of comparator circuit that is solely focused on comparing two input voltages and producing a digital output based on their relationship, without converting the input voltage into a digital representation. Unlike analog-to-digital converters (ADCs), which convert an analog input into a digital output, a non-converting comparator simply determines whether one voltage is higher or lower than another. The following figure displays a non-inverting comparator's circuit diagram.

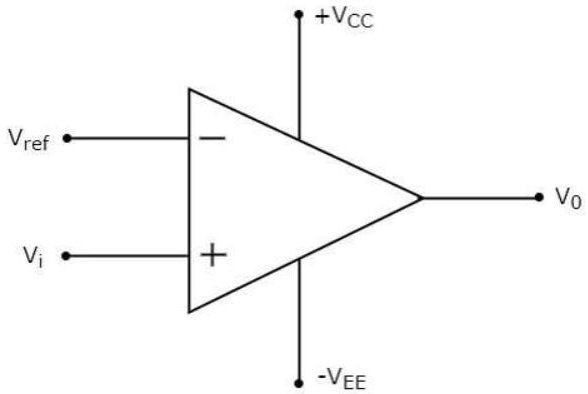


Fig. 1.8.2 Diagram of Non-Inverting

Their quick response and ability to determine voltage relationships make non-converting comparators valuable in various electronic systems where rapid decision-making based on voltage levels is necessary, such as in motor control, power management, sensor interfaces, and signal conditioning circuits.

CHAPTER 2: LITERATURE SURVEY

2.1 Analog-to-Digital Converter Survey and Analysis

The article discusses the analysis of analog-to-digital converters (ADCs) and their architectures. The article analyzes the limitations of ADCs, which are summarized in Fig. 8. For a 50 impedance and a 1 V peak-to-peak input signal, the limit is approximately four orders of magnitude beyond the state-of-the-art, which is aperture jitter limited. The various ADC architectures are covered in the article, starting with flash, the quickest parallel approach, and ending with integration, which is both the slowest and most likely the most accurate. While a small number of converters have been realised in gallium arsenide (GaAs) and indium phosphide (InP), silicon has been used to construct the majority of them.

Comparators are used by the flash architecture, where the resolution is specified. To measure overflow conditions, flash converters frequently come with one or two extra comparators. At the same time, each comparator samples the analogue input voltage. Thus, this ADC is rapid by nature. The 3-bit, 8 Gs/s Nyquist flash converter mentioned above is the fastest ADC that has been reported. The maximum sampling rate for this ADC was 14 Gs/s.

For high-resolution applications, the flash architecture's parallelism has disadvantages. In addition, the number of comparators increases exponentially as the distance between neighbouring reference voltages decreases exponentially. As a result, relatively large ICs are needed for this design. It dissipates power very quickly. Component matching in the parallel comparator channels is challenging. Lastly, the analogue input bandwidth decreases with increasing input capacitance.

Key Finding:

- • ADC restrictions are covered in the paper and are summarised. The limit is nearly four orders of magnitude beyond the aperture jitter limiting state-of-the-art for a 50 impedance and a 1 V peak-to-peak input signal.
- • The essay examines the various ADC architectures, starting with flash, the quickest parallel approach, and moving on to integrating, which is both the slowest and most likely the most accurate. While a small number of converters have been realised in gallium arsenide (GaAs) and indium phosphide (InP), silicon has been used to construct the majority of them.

- • Comparators are used in the flash architecture, where the resolution is specified. To measure overflow conditions, flash converters frequently come with one or two extra comparators. At the same time, each comparator samples the analogue input voltage. Thus, this ADC is rapid by nature. The 3-bit, 8 Gs/s Nyquist flash converter mentioned above is the fastest ADC that has been reported. The maximum sampling rate for this ADC was 14 Gs/s.

Timeline of the Reported Problem: 1999

Authors: Robert H. Walden

2.2 A Low-Power Reconfigurable Analog-to-Digital Converter

This article presents a reconfigurable, low-power, CMOS analog-to-digital converter that can digitise signals with a broad bandwidth and resolution and adaptive power consumption. The opamps' bias currents are adjusted by the phase-locked loop (PLL) in relation to the converter sampling frequency. As a result, the converter may function throughout a large frequency range. By alternating between pipeline and delta-sigma modes in its construction, the converter accomplishes this. A variety of other power-saving features are also included in this converter, such as delta-sigma mode opamp chopping, pipeline mode global converter chopping, pipeline mode opamp scaling, pipeline mode opamp sharing between successive stages, and thermal noise limited design.

The development and explanation of a reconfigurable ADC with adaptive power consumption that can digitize signals between 0 and 10 MHz in bandwidth and between 6 and 16 bits in resolution. It uses three layers of reconfiguration to achieve its broad range of reconfiguration. At the outset of reconfiguring the design, the converter can be configured in either the pipeline mode or the delta-sigma mode. The SNR can be altered at the second level, known as parameter reconfiguration, by modifying a number of factors, such as the values of the capacitors, the length of the converter in pipeline mode, and the oversampling ratio in delta-sigma mode, among others. Finally, a PLL technique can be used to modify the converter op-amp's bandwidth.

In order to remove opamp offset in the pipeline mode, this research also suggests global offset chopping. This method can tolerate offset from charge injection and other sources and requires no additional power. Compared to the usual method, this one can result in less thermal noise

and faster closed-loop settling since it does not require connecting switches in series with the opamp inputs and outputs. A series of duplicate converter opamps is utilised to build the VCO used in the PLL. This PLL approach works over about four orders of bias-current fluctuation and permits the opamp bias currents to be continuously varied along the data rate.

The converter exhibits measured performance that is comparable with cutting-edge custom-built converters over a wide variety of operating conditions as a result of the aforementioned characteristics as well as other circuit designs discussed in the article.

Key Finding:

- A low-power reconfigurable analog-to-digital converter with adaptive power consumption that can digitise signals over a broad bandwidth and resolution range is described in the paper
- By altering its circuit characteristics, switching between pipeline and delta-sigma modes, and adjusting the bias currents of the op-amps in relation to the converter sampling frequency, the converter is able to operate over a wide range.

Timeline of the Reported Problem: 2001

Authors: Kush Gulati and Hae-Seung Lee

2.3 A 6-bit 1.2-GS/s Low-Power Flash-ADC in 0.13-µm Digital CMOS

The article covers a 6-bit flash analog-to-digital converter (ADC) that only requires two reference voltages at the input to attain excellent resolution through the use of an 8-2-2-2 interpolation scheme. During the amplification phase, the reference voltages are produced by capacitive voltage division, avoiding the power penalty and silicon area associated with a low-resistive reference ladder. Because of the interpolation topology, matching, and noise requirements for the sampling capacitors at the input stage, the ADC's input capacitance is very low—only 400 fF.

The ADC's gain stages are gradually scaled down by a factor of 2, resulting in an extremely small architecture. The most crucial specification for the ADC's dc performance is the input referred offset. The final comparator stage's offset, which takes into account dynamic effects, can reach an 80 mV one-sigma value. The input referred offset must be decreased in order to provide sufficient gain in the previous amplifiers. There is a differential pair and a resistive

load in each amplifier block. For mismatch calculations, MOS and resistor devices must both be considered. The offset sampling is provided via PMOS switches connected between inputs and outputs. The amplifier's bandwidth is designed to be three to four times greater than the converter's sample rate. The gain of each stage is set to be approximately 2.5 to achieve the chain's maximum bandwidth. As a result, the 80-mV offset voltage mentioned above is decreased to approximately 2-mV input referred offset, which is equivalent to 1/16 LSB for a 1-V reference voltage. This results in a total gain of around 39.

Key Finding:

- The article presents a 6-bit 1.2-GS/s flash ADC with wide analog bandwidth and low power, realized in a standard digital 0.13 µm CMOS copper technology.
- The article describes a 6-bit flash ADC that uses an 8-2-2-2 interpolation topology to achieve high resolution with only two reference voltages at the input.

Timeline of the Reported Problem: 2005

Authors: Christoph Sandner, Martin Clara, Andreas Santner, Thomas Hartig, and Franz Kuttner

2.4 A 3.5 GS/s 5-b Flash ADC in 90 nm CMOS

Technical report or research paper with title "A 3.5 GS/s 5-b Flash ADC in 90 nm CMOS" is attached to this item. The paper describes the design and implementation of a 5-bit flash ADC (analog-to-digital converter) in 90 nm CMOS technology. 20 µm by 20 µm inductors are used in a 5-bit flash ADC to increase the bandwidth and regeneration speed of the comparator. Switched-cascode techniques reduce comparator kickback. Without sacrificing high-speed performance, offset cancellation can be achieved by adjusting the comparator reference voltages. A measured SNDR of 27.5 dB and 23.6 dB are obtained by the ADC using a 5 MHz input at 4 GS/s and a 1 GHz input at 3.5 GS/s, respectively. The power consumption is 227 mW at 3.5 GS/s. (clock buffer and ladder included). The document includes references to more related publications as well as acknowledgments to various people.

The paper also includes several figures, including a micrograph of the ADC, DNL and INL plots, and SNDR plots.

The 90 nm Intel CMOS technology is used to construct the 5-bit resolution ADC. Its features include an input range of approximately 320 mV (LSB = 20 mV), a 1.8 V clock buffer, and 1.4 V analogue and digital supplies. The sample rate can reach 4 GS/s, and the power consumption is 227 mW. An overview of the ADC performance is given in Table I, together with DNL, INL, and SNDR statistics. The paper's discussion of the ADC architecture also includes information on the buffer design and resistor ladder implementation. The measurement results of the investigation are presented in the conclusion along with SNDR plots for different input frequencies and DNL and INL plots both before and after calibration. The proposed offset calibration method is shown to improve ADC linearity.

Key Finding:

- The design and implementation of a 5-bit flash ADC with a sampling rate of up to 4 GS/s and a resolution of 5 bits.
- The ADC is implemented in 90 nm Intel CMOS and has a supply of 1.4 V analog, 1.4 V digital, and 1.8 V clock buffer, and an input range of ±320 mV (LSB = 20 mV).
- The power consumption is 227 mW.

Timeline of the Reported Problem: 2006

Authors: Sunghyun Park, Yorgos Palaskas, Ashoke Ravi, Ralph E. Bishop, and Michael P. Flynn

2.5 Analog-to-Digital Converters: A Comparative Study and Performance Analysis

This research paper explores various state-of-the-art analog-to-digital converters (ADCs) and provides a comparative study of their performance parameters, including power consumption, resolution, and sampling rate. The paper discusses the different types of ADCs and their applications in biomedical, communication, and signal processing systems. Flash ADCs use multiple comparators to convert analog signals into digital form and offer high speed but are expensive and power inefficient. Ramp ADCs use a staircase-like conversion process and have low speed but minimal quantization noise. SAR (Successive Approximation Register) ADCs use a synthetic approximation register to determine the value of each bit in the digital conversion and offer faster operation than Ramp ADCs. Integrating ADCs utilize an integrator,

comparator, and counter to determine the approximate conversion value and provide better resolution but require precision components. Delta Sigma ADCs offer high resolution, low power consumption, and stability but have moderate speed and require more area for higher-order systems. The paper also discusses the trade-offs between different performance parameters and provides a summary of the performance of various ADCs in terms of their resolution, sampling rate, power consumption, conversion time, latency, accuracy, size, and cost. The choice of ADC depends on the specific application requirements, such as speed, power consumption, resolution, and cost. The paper concludes that there is a trade-off between different performance parameters, and the choice of ADC should be based on the specific requirements of the application.

Key Finding:

- The research paper provides a comparative study of different types of analog-to-digital converters (ADCs), including Flash ADCs, Ramp ADCs, SAR ADCs, Integrating ADCs, and Delta Sigma ADCs.
- The paper discusses the performance parameters of these ADCs, such as power consumption, resolution, sampling rate, conversion time, latency, accuracy, size, and cost.
- The paper concludes that the choice of ADC should be based on the specific requirements of the application, taking into consideration the trade-offs between different performance parameters.

Time Line of the Reported Problem: 2016

Authors: Saima Bashir, Samiya Ali, Suhaib Ahmed and Vipan Kakkar

2.6 Design of Comparators using CMOS Tanner EDA Tools

The design of a two-stage CMOS amplifier with an output inverter comparator and a CMOS-LTE comparator is covered in this article. The length, breadth, and multiplier values for each transistor are included in the paper's full circuit design material. The difficulties in attaining ideal matching between p-channel and n-channel transistors in a CMOS inverter are also covered.

The first stage of the amplifier uses an NMOS differential pair to lower the input offset voltage and boost gain. The widths of the input differential pair NMOS1-NMOS2 were increased in order to improve matching. A common-source amplifier is used to calculate the amplifier's total gain. To lessen the high parasitic capacitance of PMOS2, which delays the first stage, the area covered by the common source transistor PMOS2 is increased. The circuit's propagation delay is reduced as a result. The circuit's slew rate is increased and a little amount of gain is added at the third stage, which is an inverter buffer.

A CMOS inverter, a straightforward voltage-to-current transducer (VCT) with very low distortion and excellent frequency responsiveness, is used to create the CMOS-LTE comparator. However, the linear behaviour has poor power supply rejection (PSR) and is highly dependent on p-channel and n-channel transistor matching. Because the effective mobilities of electrons and holes depend on doping, bias voltages, and temperature, perfect matching is challenging to obtain in practise. The four-transistor CMOS transconductance element, whose behaviour resembles that of an inverting amplifier, provides a solution to this issue.

Key Finding:

- The design of a two-stage CMOS amplifier with an output inverter comparator and a CMOS-LTE comparator.
- The paper provides detailed information about the design of the circuit, including the length, width, and multiplier values for each transistor.
- The paper also discusses the challenges of achieving perfect matching between p-channel and n-channel transistors in a CMOS inverter and proposes a solution using a four-transistor CMOS transconductance element.

Timeline of the Reported Problem: 2017

Authors: Mehta Vimal & Poonam Pathak

2.7 Design and Simulation of Comparator Architectures for Various ADC Applications

The design and modelling of many CMOS comparators, which are mainly used to convert analogue signals to digital ones at a frequency of 1 M Hz, are shown in this study. These

comparators are intended for usage in situations where low power consumption, high precision, and high resolution are required.

A comparator is a circuit that, based on a comparison of two input voltages—one analogue and the other reference—produces binary values 0 or 1. Its low power dissipation, high speed, low noise, and good sweep rate make it useful in ADCs. Open loop, regenerative, and cascaded comparators are among the various varieties. Comparators are suited for high-speed applications and can be integrated into cascaded stages to shorten the propagation delay time

The model's ideal feature is the output transitioning between VOL and VOH, where a mismatch in threshold voltages and transistor transconductance parameters generates offset voltage in the comparator. A comparator requires differential input and high gain, allowing two stage operational amplifiers to be used. This allows for faster response and large bandwidth, but consumes more power**.** A comparator requires differential input and high gain, allowing two stage operational amplifiers to be used. This allows for faster response and large bandwidth, but consumes more power.

Key Finding:

- The paper presents the design of CMOS comparators optimized for low power dissipation, high accuracy, and high resolution, making them suitable for energy-efficient and precise analog-to-digital conversions.
- The comparators are tailored to operate at a frequency of 1 MHz, demonstrating their suitability for high-speed applications, while using techniques like cascaded stages and two-stage operational amplifiers to minimize propagation delay and enhance response time.
- The comparators are tailored to operate at a frequency of 1 MHz, demonstrating their suitability for high-speed applications, while using techniques like cascaded stages and two-stage operational amplifiers to minimize propagation delay and enhance response time.

Time Line of the Reported Problem: 2019

Authors: Disha Gaude, Bathini Poornima, K. M. Sudharshan, Prashant V. Joshi

2.8 Enhancing the Accuracy and Speed of Sampling in Image Sensors by Designing Analog to Digital Converter with Power Decrease Approach

This study work focuses on constructing an analogue to digital converter (ADC) with a power decrease strategy in order to improve the speed and accuracy of sampling in image sensors. The study emphasises how crucial small size and low power usage are for battery-powered portable electronics. A new fast and low-power ADC design intended for image processing applications is presented in this research. In comparison to the traditional method that relies on pixel values, the proposed method significantly reduces power by rereading the image for a subset of pixels.The importance of ADCs in diverse electronic systems and the requirement for lowering power consumption are covered in the study. It explores the power consumption of integrated analog to digital converters and the decreasing trend in power consumption over the years. The authors emphasize the growing demand for low power consumption and the importance of power reduction in image sensors, particularly in applications such as medical instruments, mobile phones, cars, military industries, and wireless sensor networks. Overall, the research paper provides insights into the design and optimization of ADCs for image sensors, highlighting the importance of low power consumption and presenting a novel approach to enhance accuracy and speed in sampling. The proposed design offers significant power reduction and improved efficiency for image processing applications.

Key Finding:

- This research paper focuses on enhancing the accuracy and speed of sampling in image sensors by designing a low-power and fast analog to digital converter (ADC) specifically for image processing applications.
- The paper discusses different techniques and approaches to decrease power consumption in ADCs, including auto zeroing, digital error correction, offset error compensation, convergence rate improvement, and power reduction in digital parts.
- The authors present the proposed design of a low-power and fast ADC for image sensors, discussing different power consumption sections and comparing the performance of the proposed design with existing samples. The simulation results demonstrate significant power reduction and improved efficiency.

Time Line of the Reported Problem: 2021

Authors: Zeinab Saeidiyan, Mohammad Hosein Fatehi

2.9 Analog-to-Digital Converter (ADC) Dynamic Parameter Method Based on the Sinusoidal Test Signal

The main focus of the document is to propose a new method for spectrum testing of Analog-to-Digital Converters (ADC) under incoherent sampling conditions. The method aims to overcome the limitations of existing methods, such as over-reliance on the selection of window types, inability to test high-resolution ADC, and increased test area. The suggested approach fits the incoherent fundamental wave and harmonic wave using a parameter fitting technique and estimates the frequency parameters of the fundamental frequency using Ensemble Empirical Mode Decomposition (EEMD) and the Hilbert transform. Reconstructing the coherent fundamental and harmonic waves is another step in the process. The reconstructed coherent waves are then added to the original data after the fitted incoherent waves have been subtracted. After the data has been rebuilt, the Discrete Fourier Transform (DFT) is calculated to produce an accurate spectrum analysis and ADC dynamic characteristics. The document includes a detailed explanation of the method, its mathematical basis, and its advantages over existing methods. The proposed method overcomes the limitations of existing methods in several ways. Firstly, it eliminates the over-reliance on the selection of window types, which is a common issue in spectrum testing methods. The windowing technique used in low-resolution ADC spectrum testing is not sufficient for accurate results in cases of large incoherence or high-resolution ADC testing. The proposed method does not rely on specific window types and can provide accurate results regardless of the level of incoherence or the resolution of the ADC. The issue of estimating the initial values in the four-parameter fitting method. In existing methods, the estimation of initial values can lead to test failures if there are prediction errors. The proposed method uses Ensemble Empirical Mode Decomposition (EEMD) and Hilbert transform to estimate the frequency parameters of the fundamental wave, eliminating the need for initial value estimation and ensuring accurate results.

Key Finding:

- The proposed method has better accuracy and wider applicability compared to the windowing method, as it eliminates spectrum leakage and does not require prior knowledge of the ADC resolution.
- The method can be used with low-precision signal generators and clock generators, reducing the cost and area of the test system.

- The technique fits the incoherent fundamental and harmonic waves using a parameter fitting approach, and it estimates the frequency parameters of the fundamental wave using Ensemble Empirical Mode Decomposition (EEMD) and the Hilbert transform.

Time Line of the Reported Problem: 2022

Authors: Jiang, J.; Li, J.; Zhang, D.; Hu, C.; Peng, X.; Sun, N.; Wang, S.; Zhang, Z., Cui,W

2.10 Spin–orbit torque flash analog-to-digital converter

In this paper, a proof-of-concept for a 3-bit spin-CMOS Flash ADC with a spin-orbit torque (SOT) switching mechanism is proposed, utilising in-plane anisotropy magnetic tunnel junctions (i-MTJs). According to the paper, performance of analog-to-digital converters (ADCs), which are essential parts of mixed-signal integrated circuits, has not advanced much in the past ten years. Spintronics, which is compatible with CMOS and has numerous applications in storage, neuromorphic computing, and other fields, is suggested as a solution to this problem in the article. The engineering of the heavy metal (HM) width sets the threshold for the comparators used in the proposed ADC, which are SOT-based MTJs. The precision of the suggested ADC is limited to two bits due to process fluctuations or mismatch, as demonstrated by Monte-Carlo simulations based on experimental observations. Furthermore, the largest integral and differential nonlinearities are 0.7319 and 0.739 LSB (least significant bit), respectively. The study provides a detailed explanation of the SOT switching process in the FL of the SOT-based MTJ and the operation of the current-mode Flash ADC. The essay compares and contrasts the proposed ADC with several designs proposed in the literature, outlining the advantages and disadvantages of each. The report contains microscopic images of the serial and parallel designs of the proposed ADC, as well as the MR dependence with the position of the MTJ for each design. The article concludes that the measured data from the characterization of the parallel configuration.

Additionally, Monte-Carlo simulations are used to estimate the ADC accuracy in the presence of MTJ and CMOS transistor process fluctuation or mismatch. The simulation results demonstrate the suggested ADC's proposed accuracy limitations to two bits, which can be improved by advancing MTJ fabrication technology.

Key Finding:

- According to Monte-Carlo calculations based on experimental observations, the precision of the suggested ADC is limited to 2 bits by the process variations/mismatch.
- The article suggests adopting spintronics, which is compatible with CMOS and has many uses in storage, neuromorphic computing, and other areas, as a solution to this issue.
- The mechanism of the current-mode Flash ADC and the SOT switching mechanism in the FL of the SOT-based MTJ in great detail.

Timeline of the Reported Problem: 2023

Authors: Hamdam Ghanatian, Luana Benetti, PedroAnacleto, Tim Böhnert, Hooman Farkhani, Ricardo Ferreira & Farshad Moradi

2.11 Enhancing the Accuracy and Speed of Sampling in Image Sensors by Designing Analog to Digital Converter with Power Decrease Approach

The two-stage open-loop comparator is the subject of this research study for the following reasons: Measures Common Mode Range Differential Voltage Gain Propagation Delay Slew Rate Dynamic Range of Output. The gain is negligible enough to eliminate the need for more than the two stages, but high enough to justify the usage of two. A power supply value of ±5V offers enough headroom to avoid the necessity of using the cascode arrangement. Due to the low required slew rate, big source and sink currents are not needed, nor is a push-pull arrangement.

With a delay time requirement of less than 750 ns, this is the most challenging criteria to meet. The following gives the equation for delay time. The smallest value of R can be computed to be 0.202M ohms using the equation above. The necessary minimum value of I7 is determined by two equations, and consideration must be given to the implications of each equation. First, one can find the minimal current required by taking into account the slew rate. Slew rate can be found using the formula I7/CL. It is possible to get the minimum value of I7 using this expression.

Key Finding:

- Metrics: Output Dynamic Range; Differential Voltage Gain; Propagation Delay; Slew Rate (fall edge).

- Differential Voltage Gain: Only the first stage gain was computed and matched to 120V/V in the computations.
- The first stage voltage gain's real value was 130V/V.
- All of the specifications are met by the designed comparator. Examining the designed comparator's utility is a straightforward process.Most likely, the comparator outlined above would be a component of a general-purpose ADC/DAC.
- Input Offset Voltage: The comparator that has been constructed has an input offset voltage of –4.04mV.

Source: *http://www.disctronics.co.uk/technology/dvdaudio/dvdaud_audio.htm*

† *Source: http://www.sony-middleeast.com/sacd/faq.htm*

CHAPTER 3: DESIGN FLOW PROCESS

3.1 Concept Generation

In this project, the main idea is to perform a ADC architecture with dynamic power scaling to address the trade-off between speed and energy efficiency. In a ADC, the conversion process is divided into stages, each with its own set of comparators. Dynamic Power Scaling involves adjusting the power supply voltage and/or clock frequency to reduce energy consumption during idle or low-demand periods while maintaining high-speed operation when needed. ADC are of importance in this era of digital systems because of there applications and needs listed below:

1. Real-Time Data Acquisition
2. Wireless Communication
3. Image and Video Processing
4. Signal Intelligence and Surveillance
5. High-Frequency Trading
6. Data Centres and Cloud Computing

Analog-to-Digital Converters (ADCs) play a pivotal role in the world of electronics, where various types of ADCs offer distinct mechanisms and characteristics to transform continuous analog signals into discrete digital data. These ADC variants, which include Flash ADCs, Successive Approximation ADCs (SAR ADCs), Pipeline ADCs, Delta-Sigma ADCs, Dual-Slope ADCs, Interpolating ADCs, Time-Interleaved ADCs, and Flash ADCs with Sub ranging, each possess unique attributes that influence their performance, power consumption, area utilization, and the intricacy of arithmetic operations.

3.2 Introduction to Tools Used:

Tools:

- Cadence Virtuoso
- Xilinx
- Verilog

3.2.1 Cadence Virtuoso: Cadence Virtuoso is a widely used electronic design automation (EDA) software suite developed by Cadence Design Systems. It is primarily used for designing and simulating integrated circuits (ICs) and semiconductor devices.

Advantage of Cadence Virtuoso:

- Comprehensive Toolset: Virtuoso offers a wide range of tools for every stage of the IC design process, providing designers with an integrated environment to work efficiently.
- Accuracy and Precision: The software's simulation and layout capabilities enable designers to create highly accurate and precise electronic circuits, essential for custom and analog IC design.
- Customization: Virtuoso allows users to create custom scripts and automation, tailoring the software to their specific needs and speeding up repetitive tasks.
- Integration: It can be seamlessly integrated with other EDA tools and design flows, making it compatible with various design methodologies.
- Analog and RF Design: Virtuoso excels in analog and RF design, making it a preferred choice for applications where signal integrity and precision are critical.
- Parasitic Extraction: The software can perform parasitic extraction, helping designers identify and mitigate issues related to parasitic capacitance and resistance.
- Industry Standard: Virtuoso is widely used in the semiconductor industry, making it easier for design teams to collaborate and share designs with other organizations.

Uses of Cadence Virtuoso :

- Custom IC Design: Virtuoso is widely used for custom integrated circuit (IC) design, particularly for designing analog and mixed-signal ICs. It provides tools for creating complex custom circuits with precise control over layout and performance.
- Analog and RF Design: Virtuoso is well-suited for designing analog and radio-frequency (RF) circuits, where signal integrity, noise, and precision are critical. It offers advanced simulation and layout capabilities for these applications.
- Digital IC Design: While Virtuoso is more commonly associated with analog design, it also supports digital IC design. Designers can use it for creating digital schematics and layouts.
- Integrated Circuit Simulation: Virtuoso includes simulation tools for analysing the behaviour of electronic circuits. Designers can perform transient, AC, DC, and other simulations to verify the performance of their designs.

- Physical Layout Design: The software allows engineers to create the physical layout of ICs. This involves placing and routing transistors, interconnects, and other components on the semiconductor die while adhering to design rules.
- Parasitic Extraction: Virtuoso can extract parasitic capacitance, resistance, and inductance information from layouts. This is essential for accurately predicting circuit behaviour and optimizing designs.
- Verification and Validation: Designers can use Virtuoso to verify the correctness of their designs, perform design rule checks (DRC), and ensure that their ICs meet manufacturing requirements.
- Automation and Scripting: Virtuoso supports automation through scripting, allowing designers to create custom scripts to streamline design tasks, automate repetitive actions, and customize workflows.
- RFIC (Radio-Frequency Integrated Circuit) Design: Virtuoso is commonly used for designing RFICs used in wireless communication systems, such as cellular phones, Wi-Fi, and Bluetooth devices.
- Mixed-Signal Design: Virtuoso supports the integration of analog and digital components in mixed-signal ICs, making it suitable for applications that require both types of functionalities.
- IC Packaging and Interconnect Design: It can be used to design the interconnects and package layout for ICs, considering factors like signal integrity, thermal management, and manufacturing constraints.
- Semiconductor Process Development: Some engineers and researchers use Virtuoso for process development and optimization, helping semiconductor foundries refine their manufacturing processes.
- Academic and Research: Virtuoso is also used in educational institutions and research environments for teaching and conducting semiconductor-related research.

Types of Cadence Virtuoso based on their architecture, configuration method, and capacity.

- Virtuoso Analog Design Environment (ADE): This is a common configuration for analog and mixed-signal design. It provides tools for designing, simulating, and verifying analog and mixed-signal integrated circuits.

- Virtuoso Digital Implementation: This configuration is focused on digital IC design and includes tools for digital schematic entry, RTL synthesis, and physical layout.
- Virtuoso Custom IC Design: Custom IC Design configurations are tailored for complex custom circuit design, often used for analog and mixed-signal designs with precise control over layout and performance.
- Virtuoso RF Design: This configuration is specialized for designing RFICs (Radio-Frequency Integrated Circuits) and microwave circuits, which require specific simulation and layout capabilities for high-frequency designs.
- Virtuoso Layout Suite: Virtuoso Layout Suite configurations are dedicated to physical layout design, including tools for IC layout and floor planning.
- Virtuoso Simulation and Analysis: This configuration focuses on simulation and analysis capabilities, offering various simulation types (e.g., transient, AC, DC) for verifying circuit behavior.
- Virtuoso Verification: This configuration is geared toward design verification and includes tools for performing design rule checks (DRC), layout versus schematic (LVS) checks, and other verification tasks.
- Virtuoso Extraction: Virtuoso Extraction configurations are specialized for parasitic extraction from layout designs, critical for accurate circuit behavior prediction.
- Virtuoso Integration with Other EDA Tools: Virtuoso can be configured and customized to integrate with third-party EDA tools, providing a versatile environment for designers to work with their preferred tools.
- Virtuoso Scalable Licensing: Cadence offers scalable licensing options to accommodate the varying needs of users and organizations. These configurations can be tailored based on the number of licenses, features, and capacity required.
- Virtuoso Enterprise Edition: The Enterprise Edition provides a comprehensive and fully featured version of Virtuoso suitable for large organizations and complex design projects.
- Virtuoso Academic Edition: Cadence offers academic editions of Virtuoso to educational institutions, providing access to EDA tools for teaching and research purposes.
- Virtuoso Cloud: Cadence has introduced cloud-based versions of Virtuoso, allowing users to access the software and resources remotely through cloud infrastructure, which can provide scalability and flexibility.

3.2.2 Xilinx: Xilinx ISE Design Suite is a software toolchain developed by Xilinx for designing and programming field-programmable gate arrays (FPGAs) and programmable logic devices (PLDs). It provides a comprehensive environment for FPGA and PLD design, verification, and programming, and supports the entire design flow from initial concept to final implementation. In this article, we will discuss the features, capabilities, and applications of Xilinx ISE Design Suite in detail.

The Xilinx ISE Design Suite includes a range of software tools that support various stages of the FPGA and PLD design process. These tools include:

- Design Entry: Xilinx ISE supports both graphical and text-based design entry methods. The graphical method involves using schematic capture tools to create the design, while the text-based method involves using a hardware description language (HDL), such as VHDL or Verilog. The suite also provides a system generator tool that allows users to create designs using Simulink, a graphical programming environment.
- Synthesis: Once the design has been entered, the next step is synthesis, which involves converting the design into a netlist of logic gates that can be programmed onto the FPGA or PLD. Xilinx ISE includes a powerful synthesis tool that can optimize the design for timing, area, and power.
- Simulation: Before the design is implemented on the FPGA or PLD, it is necessary to verify its functionality using simulation. Xilinx ISE provides a range of simulation tools that allow users to test the design using both functional and timing simulations. The suite also includes tools for debugging and analysis of simulation results.
- Implementation: Once the design has been verified, it is time to implement it on the FPGA or PLD. Xilinx ISE includes tools for place and route, which involves mapping the logic gates onto the FPGA or PLD and routing the interconnections between them. The suite also includes tools for timing analysis, which ensures that the design meets the required timing constraints.
- Programming: Finally, the design is programmed onto the FPGA or PLD using a programming tool. Xilinx ISE supports a range of programming methods, including JTAG, PROM, and flash programming.

3.2.3 Verilog: Verilog is a hardware description language (HDL) used for designing digital circuits and systems. The language was created as a way to model digital circuits using a high-level description, rather than using low-level schematics. This allowed designers to create complex digital systems more easily and efficiently.

There are two main ways to use Verilog: behavioral modeling and structural modeling. Behavioral modeling describes the function of the digital system without specifying its internal structure. This is useful for simulating and verifying the behavior of a system before it is implemented in hardware. Structural modeling describes the physical structure of the digital system, including the components that make it up and how they are connected. This is useful for synthesizing a design into an actual hardware implementation.

Advantages:

- Verilog is a powerful and flexible language that allows designers to model complex digital systems.
- Verilog is widely used in the semiconductor industry and has a large community of users, which makes it easier to find support and resources.
- Verilog supports both behavioral and structural modeling, which allows designers to choose the level of abstraction that best suits their design.
- Verilog is compatible with a wide range of simulation and synthesis tools, making it easy to integrate into existing design flows.

Uses:

- Verilog is used for designing digital circuits and systems, including ICs, FPGAs, and ASICs.
- Verilog is used in a wide range of applications, including telecommunications, networking, consumer electronics, and automotive.
- Verilog is often used in conjunction with other design tools, such as simulation and synthesis tools, to verify and optimize the design of digital circuits and systems.

3.3 Evaluation and Selection of Specific Features:

Any engineering project has certain constraints within which a system has to be built. These constraints are defined by different factors like type or nature of the project, scalability ambitions, current usage, future upgrades, compatibility with its surroundings, degree of

integration with other system, safety and many more. Here we will discuss about different type of constraints relating to its regulations, design, economy, environment, health, manufacturing, safety issues, professional and ethical issues and, at last, social and political issues. First, we will define the constraints and explain them individually what they are. Then we will design the system following those constraints. Any change in design must be in accordance with the constraints and upgradability must be in check with the ever-changing constraints.

Digital logic circuits are typically designed and implemented using programmable hardware in FPGA (Field Programmable Gate Array) based projects. There might be a number of laws and restrictions that need to be taken into account, depending on the nature and size of the project. Some of the constraints involve : Intellectual property rights, Export control, Safety and reliability, Power consumption, Emissions, Security, Data privacy, Environmental regulations.

3.3.1 Regulations Constraints

All of our design has to follow the regulation of that particular area i.e., the regulations provided by the local and federal government of that particular country. Any regulations unchecked may cause problems which when surfaces, may cause bad name to the design and add a negative connotation to the company. So, we will have to go through the guidelines of that area thoroughly. Such actions will also reduce lawsuits from people in case of any unwanted incident or accident.

3.2.2 Design Constraints

Designing an energy-efficient high-speed parallel Analog-to-Digital Converter (ADC) is a complex undertaking shaped by a multitude of design constraints. Foremost among these is the imperative for power efficiency. In a world increasingly focused on energy conservation, the ADC must deliver rapid data conversion while minimizing power consumption. Achieving this balance necessitates innovative circuit design, low-power component selection, and the potential integration of dynamic power scaling mechanisms to reduce energy use during idle periods. High-speed ADCs must ensure that the analog signals they digitize remain intact throughout the conversion process. This demands meticulous attention to printed circuit board (PCB) layout, noise reduction, and distortion prevention. Different industries and applications may enforce strict standards pertaining to safety, electromagnetic compatibility (EMC), and environmental sustainability, such as RoHS compliance. These standards steer design choices

and necessitate features like EMI shielding, safety mechanisms, and adherence to hazardous material restrictions. Size and form factor constraints can be particularly challenging, necessitating the deployment of advanced packaging technologies and integration techniques to achieve energy efficiency within limited physical space. Engineers must strike a balance between performance and cost-effectiveness, especially in consumer electronics. Security and privacy constraints gain significance in data-sensitive applications, demanding robust data encryption, secure storage, and compliance with data protection regulations. Reliability and longevity constraints are vital, with ADCs required to adhere to stringent quality and reliability standards, ensuring durability and consistent performance. In navigating these intricate constraints, ADC designers must meticulously balance competing demands to deliver a solution meeting the diverse requirements of applications while pushing technological boundaries.

3.2.3 Economic Constraints

Economic constraints are a critical aspect of designing energy-efficient high-speed parallel Analog-to-Digital Converters (ADCs). These constraints influence every phase of the design process, from initial concept to production and beyond.

In Development Costs the creation of a high-speed ADC involves substantial research, development, and engineering efforts. Economic constraints necessitate efficient resource allocation to manage costs effectively. Budget limitations may impact the scope of the project, affecting the level of innovation and the time-to-market. The choice of components and materials significantly impacts the cost of the ADC. High-performance, energy-efficient components often come at a premium, so cost-effectiveness must be balanced with performance goals. Economical component selection is essential to keep the overall production cost reasonable. The manufacturing process plays a pivotal role in economic constraints. Efficient and scalable manufacturing methods are crucial to achieving cost-effective production. Production costs, including labor, equipment, and facilities, must be carefully managed. Economic constraints are often driven by market dynamics. The competitiveness of the ADC in the marketplace influences pricing strategies and profit margins. Understanding market demand and pricing sensitivity is vital to economic success. For companies and organizations investing in ADC development, the economic constraint of achieving a satisfactory ROI is paramount. Assessing the potential returns against development costs is a central consideration in greenlighting ADC projects. Economic considerations extend beyond

initial development and production. The long-term costs of maintenance, support, and potential upgrades should be factored into the economic assessment. Energy-efficient ADCs that offer reduced operational costs over their lifecycle may provide a competitive advantage. Economies of scale can significantly impact production costs. Large-scale production typically results in cost reductions per unit, making it essential to anticipate scalability and volume requirements.

3.2.4 Environmental Constraints

The design of energy-efficient, high-speed parallel analog-to-digital converters (ADCs) faces many environmental constraints. These limitations can be broadly divided into physical, thermal and electrical limitations. ADC increases in speed and resolution require more cycles, resulting in more die and faster energy. chip area. This can create problems with packaging and integration into compact electronics. High-speed ADCs operate at high frequencies, making them susceptible to electromagnetic interference (EMI) and noise from other components. Circuit board. This reduces the accuracy and efficiency of the ADC. The integrity of the analog input signal is important for correct ADC conversion. Maintaining signal integrity on long lines and high noise levels can be difficult. Power consumption is a major issue in the design of high-speed ADCs because they are often used in portable and power devices. It is difficult to reduce energy consumption without sacrificing performance. The ADC's sensitivity to power supply noise affects its accuracy and stability. Maintaining clean and stable power is critical for effective ADC performance. The power distribution network (PDN) should be designed to provide good power to the ADC while minimizing distortion and noise. This may be difficult due to the current need for high-speed ADCs. Identifying these environmental limitations requires careful consideration of design options, circuit layout, packaging, and power management strategies. By effectively managing these parameters, designers can use energy-efficient, high-speed parallel ADCs that meet the needs of today's electronics.

3.2.5 Technical Constraints

The design of energy-saving, high-speed parallel analog-to-digital converters (ADCs) faces many limitations that can affect their performance and overall results. These parameters can be broadly divided into analog, digital and architectural considerations. High-speed ADCs are particularly susceptible to noise and interference from a variety of sources, such as power supplies, clock signals, and adjacent power lines. This reduces the signal-to-noise ratio (SNR) and reduces the accuracy of the ADC conversion. The S&H circuit is important for accurately

capturing analog input signals. Its performance in terms of acquisition time, aperture jitter, and setup time affects the overall accuracy of the ADC. Quantization error is a limitation of ADC and is caused by the number of digital signals. Code used to represent analog input signals. This error can be reduced by improving the ADC resolution, but this also increases the power consumption and complexity of the circuit Synchronizing the analog and digital parts of the ADC is important to ensure correct conversion. Clock distribution, delay changes, and jitter create synchronization challenges. Error corrections such as Hamming codes are frequently used in high-speed ADCs to reduce the impact of data transmission errors. However, this process is stressful and labor intensive Pipeline ADCs are widely used in high-speed applications, but they introduce latency due to the many stages of conversion. Striking the balance between latency and throughput is difficult. Parallel ADCs provide higher precision by converting multiple channels simultaneously. However, they cause circuit competition, power consumption, and synchronization competition.

3.2.6 Manufacturability Constraints

The design of energy-efficient, high-speed parallel analog-to-digital converters (ADCs) faces many manufacturing limitations that may hinder their mass production and widespread use. These constraints can be broadly divided into process variables, throughput constraints, and volume constraints. Semiconductor manufacturing processes exhibit inherent variations in device parameters such as transistor threshold voltage and gate oxide thickness. These inconsistencies can lead to differences in the performance of different ADC units, affecting consistency and reliability.ADC performance is temperature sensitive. Ensuring consistent performance across varying temperatures requires careful design and process control. Defects found in semiconductor materials or manufacturing processes cause ADC cells to malfunction, reducing yield, profit and increasing production cost. High-speed ADCs often require tight control of dimensions and dimensions. Meeting these stringent requirements can be difficult, especially in competitive processes.High-speed ADCs often require multiple layers of interconnect to accommodate complex configurations. Maintaining connectivity and minimizing crosstalk between layers can be challenging. Wire bonding is a method of connecting the ADC die to external components. However, the connection between cables introduces interference and inductance, affecting signal integrity at high frequencies.The package itself can introduce interference such as lead inductance and package capacitance that can degrade performance. Fast ADC. Solving these production limitations requires effective

collaboration between designers, process engineers and production teams. By understanding the limitations of the manufacturing process and designing accordingly, manufacturers can achieve a wide range of electronic, high-speed parallel ADCs.

3.2.7 Safety and Health Constraints

The design of electronic, high-speed parallel analog-to-digital converters (ADCs) must take into account many safety and health issues to ensure the protection of users and a tour. These restrictions can be broadly divided into electrical safety, electromagnetic compatibility (EMC) and environmental considerations. High-speed ADCs often operate at high voltage and can cause shocks if not properly isolated and protected. Designers should take appropriate safety precautions to prevent contact with high voltage equipment. High-speed ADCs may leak current, which could cause a power outage or safety. Designers must reduce current flow and take protective measures to avoid danger. ESD can damage electronic components, including ADCs. Designers must incorporate ESD protection measures into the design and manufacturing process to prevent ESD damage. High-speed ADCs can produce EMI that can interfere with other electronic devices. Designers should use EMI shielding, filtering, and grounding techniques to minimize EMI emissions and prevent interference. High-speed ADCs are subject to EMS, which may reduce their performance or performance. Designers must ensure that the ADC can withstand the EMS levels required in the operating environment. RFI generated by high-speed ADCs can interfere with radio communications. Designers must take reasonable steps to minimize RFI emissions and comply with relevant regulations. High-speed ADCs consume a lot of power, resulting in energy consumption and greenhouse gas emissions. Designers should try to minimize power consumption to reduce the ADC's environmental impact. The choice of components in the ADC design can affect the environment. Designers should prioritize the use of sustainable and recycled materials whenever possible. Disposal of electronic waste, including ADC, may pose environmental risks. Designers should consider end-of-life recycling and disposal options during design.

3.2.8 Professional & ethical constraints

The design of energy-efficient high-speed parallel analog-to-digital converters (adcs) must adhere to various professional and ethical constraints to ensure responsible and ethical

engineering practices. These constraints encompass aspects of intellectual property, safety, environmental responsibility, and professional conduct.engineers must respect and adhere to existing ip laws and regulations to avoid infringement on the intellectual property of others. This includes properly citing sources, obtaining necessary licenses, and avoiding unauthorized use of copyrighted materials.engineers should strive for originality in their designs and inventions. While protecting trade secrets is important, engineers also have a responsibility to disclose significant innovations through publications or patent applications to advance the field. Engineers should properly acknowledge the contributions of others, both within their teams and in the broader engineering community. Engineers have a responsibility to prioritize safety in their designs, considering potential hazards and implementing appropriate safety measures to protect users and the environment. This includes factors such as electrical safety, electromagnetic compatibility, and potential risks associated with the operation and disposal of the adc. Engineers must adhere to relevant safety standards and regulations established by regulatory bodies and industry organizations. These standards provide guidelines for designing safe products and minimizing potential hazards.engineers should conduct comprehensive tests to identify and address potential safety issues before releasing products to market. Engineers must maintain high standards of integrity and ethical conduct in their professional activities. This includes honesty, transparency, and avoiding conflicts of interest. Engineers should treat colleagues, collaborators, and stakeholders with respect, professionalism, and courtesy. This includes valuing diverse perspectives, engaging in constructive discussions, and resolving conflicts ethically.

3.2.9 Social and Political Constraints

The design of energy-efficient high-speed parallel analog-to-digital converters (adcs) faces various social and political constraints that can influence their development, adoption, and usage. These constraints encompass aspects of accessibility, affordability, government policies, and societal acceptance. The complexity of high-speed adcs may pose challenges for non-technical users, limiting their ability to understand, adopt, and utilize these technologies effectively. The deployment of high-speed adcs may depend on the availability of reliable infrastructure, such as stable power grids and high-speed communication networks, which may not be readily available in all regions. The development and manufacturing of high-speed adcs can be expensive, potentially making them unaffordable for some users and applications. Government and private funding for research and development in adc technology may be

limited, hindering advancements and reducing accessibility. Pricing strategies and market competition can influence the affordability of high-speed adcs, potentially making them inaccessible to price-sensitive users. Societal concerns about privacy and security concerns about data privacy and security associated with the use of high-speed adcs in applications like surveillance can hinder adoption. Ethical considerations regarding the potential misuse of high-speed adcs for surveillance or other purposes can influence public perception and acceptance. Addressing these social and political constraints requires a multifaceted approach involving collaboration between engineers, policymakers, educators, and the public. By promoting accessibility, affordability, responsible development, and public understanding, society can harness the potential of high-speed adcs while mitigating potential risks and ensuring their beneficial use for the betterment of humankind.

3.4 Analysis and Features Finalization Subject to Constraints

The design of energy-efficient, high-speed parallel analog-to-digital converters (ADCs) faces many constraints, including analog, digital, and architectural considerations. Analog suppression of noise and distortion, sample-and-hold (S&H) circuit performance, and quantization error. Limitations include high-speed digital circuits, data synchronization and error correction, and coding. Architectural constraints include pipeline architecture, parallel architecture, and power management. Manufacturers need to address process changes, yield issues and packaging to ensure ADC efficiency. Designers must consider electrical safety, electromagnetic compatibility (EMC) and the environment to ensure the safety and health of users and the environment.Engineers must comply with intellectual property (IP), safety, environmental liability and operating restrictions.

Social and political factors include accessibility, affordability, government policies and regulations, and social acceptance.

3.5 Alternate Design Plans

Implementation of Analog to digital converter (ADC) using mux as Priority Encoder

A priority encoder is a digital circuit that takes multiple inputs and outputs a binary code that represents the highest-priority input that is high. A multiplexer is a digital circuit that selects one of multiple inputs and outputs that input. To use a multiplexer as a priority encoder, you can connect the inputs of the multiplexer to the data inputs of the encoder. You can then connect

the select inputs of the multiplexer to the outputs of the encoder. The output of the multiplexer will then be the highest-priority input that is high.

For example, to use a 4-to-2 priority encoder, you would connect the inputs of the multiplexer to the data inputs of the encoder. You would then connect the select inputs of the multiplexer to the outputs of the encoder. The output of the multiplexer would then be the highest-priority input that is high.

Here is an example of how to use a multiplexer as a priority encoder:

```
mux = Mux(4, 2)
encoder = PriorityEncoder(4)

mux.connect_data_inputs(encoder.outputs)
mux.connect_select_inputs(encoder.outputs)

output = mux.output
```

In this example, the mux variable is a 4-to-2 multiplexer and the encoder variable is a 4-to-2 priority encoder. The connect_data_inputs() method connects the the data inputs of the multiplexer to the outputs of the encoder. The connect_select_inputs() method connects the select inputs of the multiplexer to the outputs of the encoder. The output variable is the output of the multiplexer. The output of the multiplexer will be the highest-priority input that is high. For example, if the input d0 is high and the other inputs are low, then the output of the multiplexer will be 0. If the input d1 is high and the other inputs are low, then the output of the multiplexer will be 1. If the input d2 is high and the other inputs are low, then the output of the multiplexer will be 2. And so on. Using a multiplexer as a priority encoder is a simple and efficient way to implement a priority encoder. Using a multiplexer as a priority encoder is a simple and efficient way to implement a priority encoder. However, it is not always the most efficient way to implement a priority encoder. For example, if the number of inputs is large, then it may be more efficient to use a different type of priority encoder.

Alternative 2:

"Implementation of Analog to digital converter (ADC) using PCSA as Priority Encoder"

The Pre-Charge Sense Amplifier (PCSA) with a special magnetic stripe and reference MTJ can be employed as a priority encoder due to its ability to detect and prioritize signals based on their strength. This configuration leverages the PCSA's inherent speed, low power consumption, and compact size, making it suitable for applications requiring efficient and reliable priority encoding. The PCSA with a special magnetic stripe and reference MTJ offers a unique approach to priority encoding, combining speed, power efficiency, and flexibility. While its complexity and potential noise sensitivity may pose challenges, its advantages make it a promising solution for applications demanding efficient and reliable priority encoding. PCSAs can prioritize memory access requests, ensuring efficient data retrieval and processing. PCSAs can prioritize data transfers on shared buses, preventing conflicts and optimizing data throughput. PCSAs can prioritize packet forwarding, ensuring that critical data packets receive preferential treatment.

Principle of Operation

The PCSA functions by amplifying the voltage difference between its input and reference nodes. The special magnetic stripe acts as a control mechanism, influencing the PCSA's behavior and enabling priority encoding. The reference MTJ provides a stable reference voltage, ensuring consistent and accurate operation.

Priority Encoding Implementation :The magnetic stripe encodes the priority levels of the input signals. The PCSA's configuration is adjusted based on the magnetic stripe's data, effectively setting the priority of each input. When an input signal arrives, the PCSA compares its strength against the reference voltage, prioritizing the strongest signal and generating an output accordingly.

CHAPTER 4: PROPOSED FOR PARALLEL ADC

4.1 Implementation of 4:1 OR-GATE

The OR gate is one of the types of the digital logic gate. As we know that in binary numbers (0 and 1), 0 is low and 1 is high. Thus, the output is high if and only if at least one of the supplied inputs is high; otherwise, it is low.

Inputs and outputs in OR Gate –

Input: An OR gate receives its binary signal from the user at its input terminals, where it applies logical operations to produce an output.

Output: The outcome of a logical operation on an OR gate's inputs is known as the output. It may have low (0) or high meanings (1). Following an operation, there is just one output given.

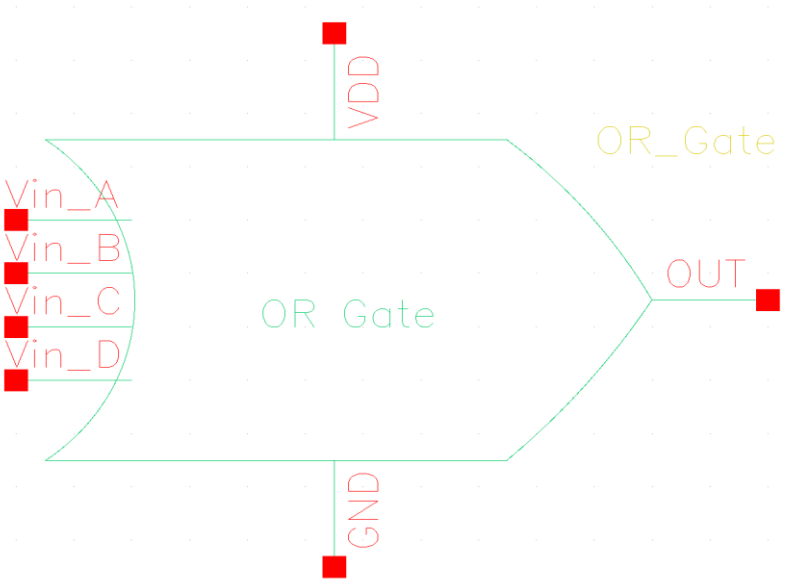


Fig. 4.1.1 Symbol of OR Gate

A 4:1 OR gate is a digital logic gate that takes in four inputs and produces one output based on a logical OR operation. In this context, the "4:1" refers to the number of input channels compared to the single output channel.

The output of a 4:1 OR gate will be high (logic 1) if any of the four input signals is high; otherwise, the output will be low (logic 0). This gate follows the principle of Boolean logic where the OR operation yields true (1) if at least one input is true.

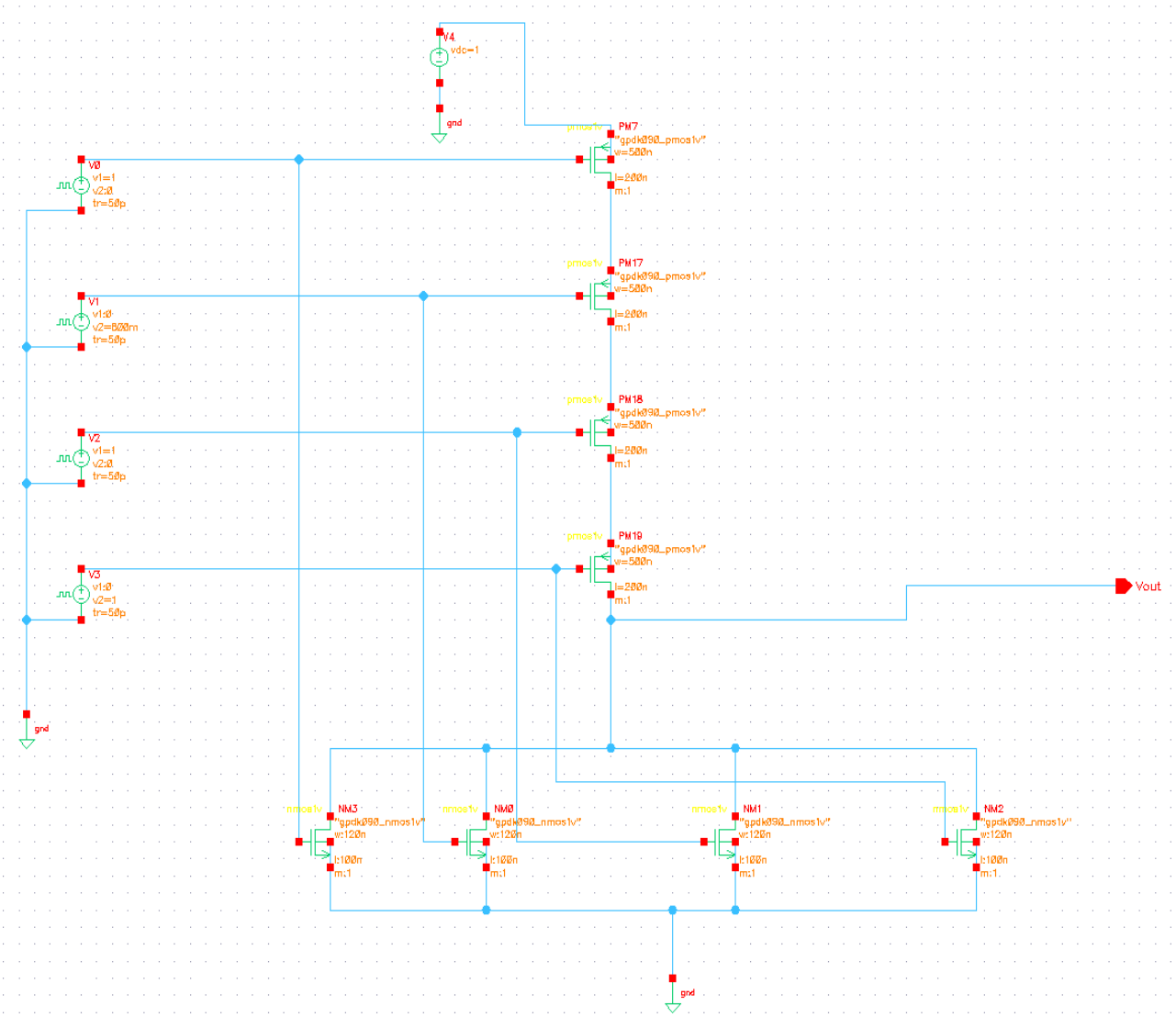


Fig. 4.1.1 Schematic of 4:1 OR Gate

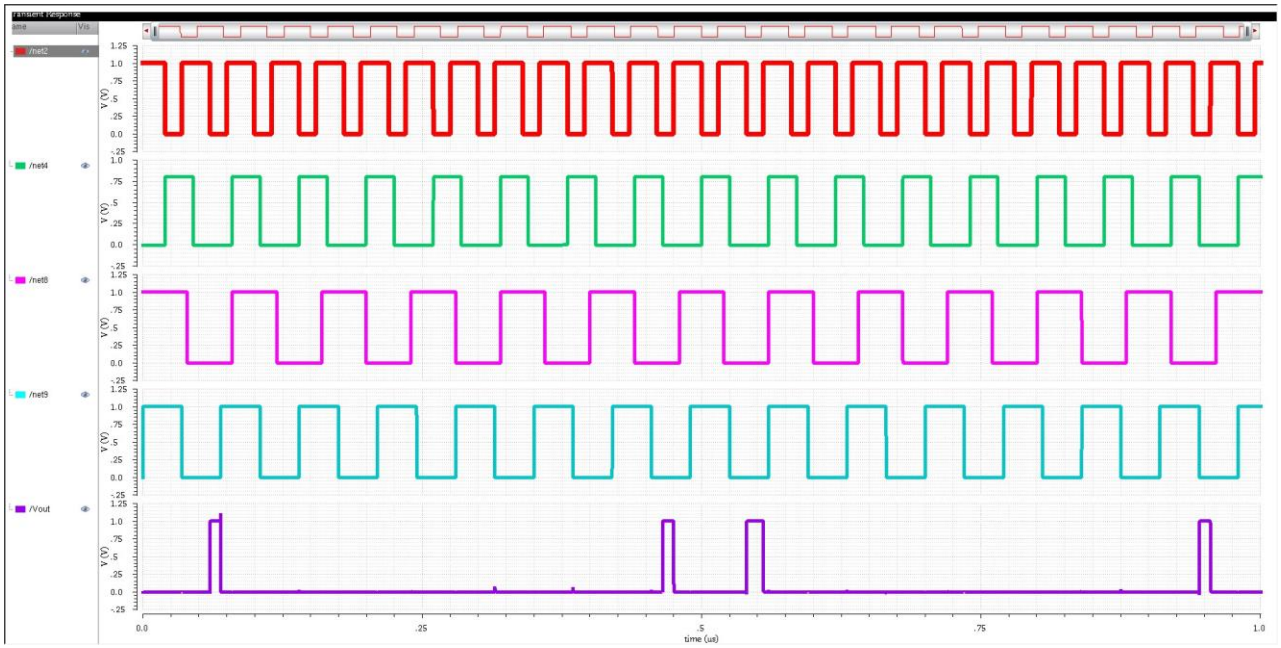


Fig. 4.1.2 Simulation of 4:1 OR Gate

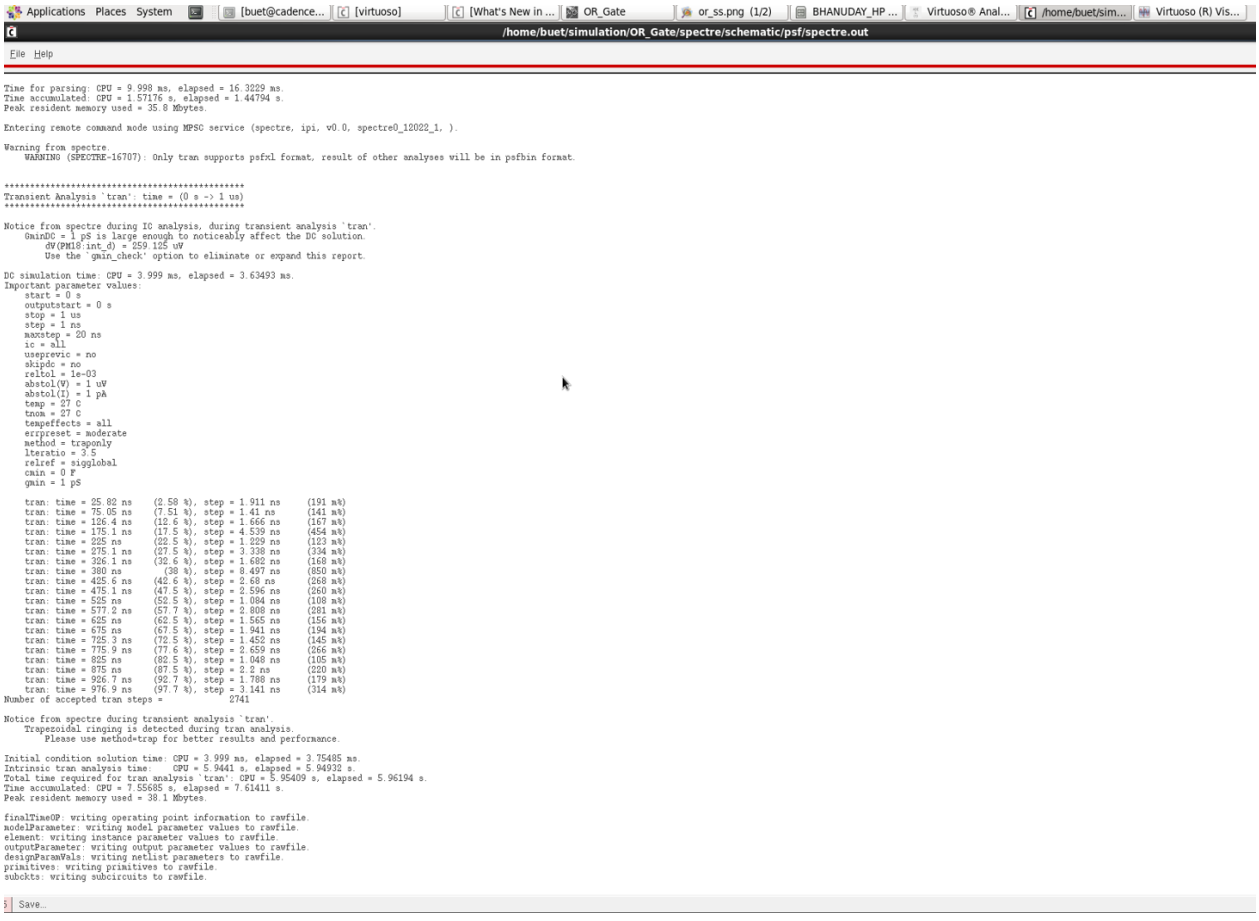


Fig. 4.1.3 Time Analysis of 4:1 OR Gate

4.2 Priority Encoder 8:3

A priority encoder is a digital circuit used in digital systems to encode multiple binary inputs into a smaller number of output lines, generally in a way that prioritizes the higher-order inputs when multiple inputs are active simultaneously.

Let's consider a basic example of a 4-input priority encoder. It takes four input lines (D0, D1, D2, and D3) and produces a two-bit binary output (Y1, Y0) indicating the highest-priority active input.

The priority encoder will assign a priority to each input such that if multiple inputs are active, it will encode the highest priority input only. The priority is typically given to the highest order active input (e.g., if D3 is active along with D2, D3 takes priority).

The highest priority input that is currently active is matched by the priority encoder's output. Thus, any other inputs with a lower priority will be ignored in the presence of an input with a higher priority.

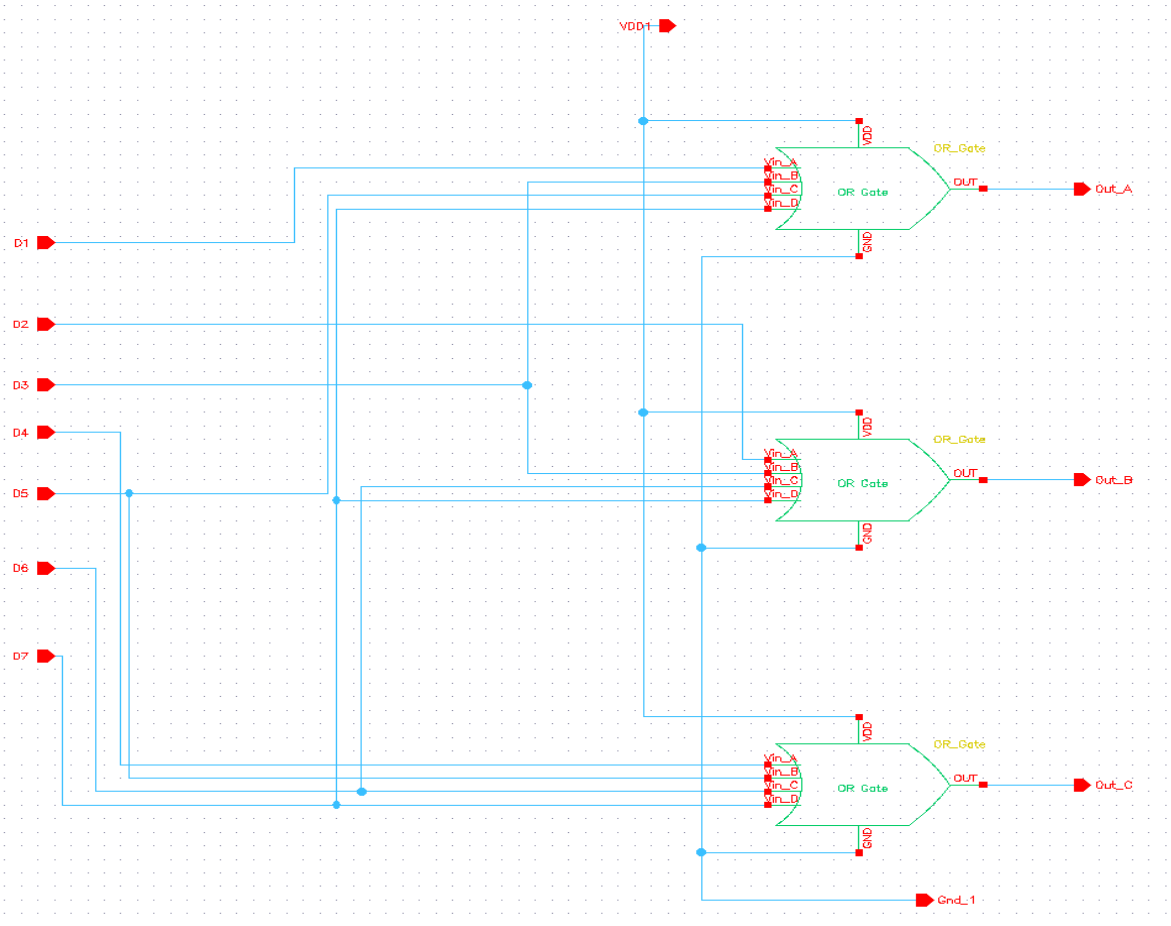


Fig. 4.2.1 Schematic of Priority Encoder 8:3

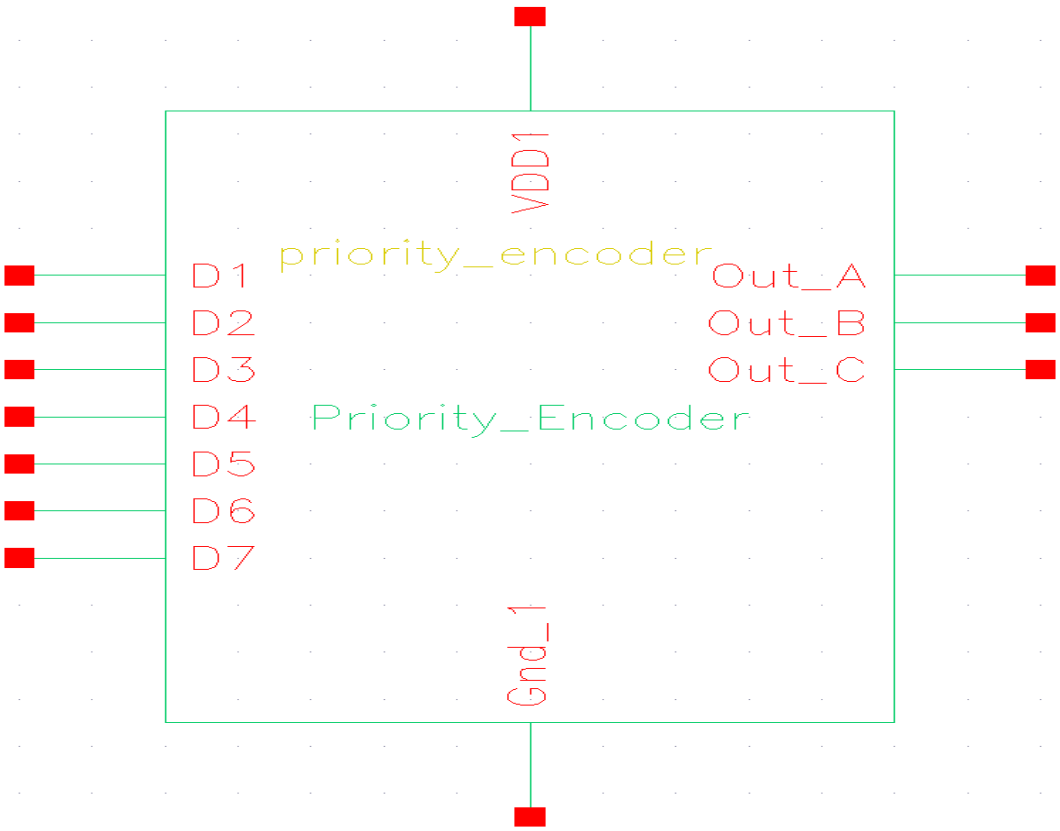


Fig. 4.2.2 Block Diagram of Priority Encoder 8:3

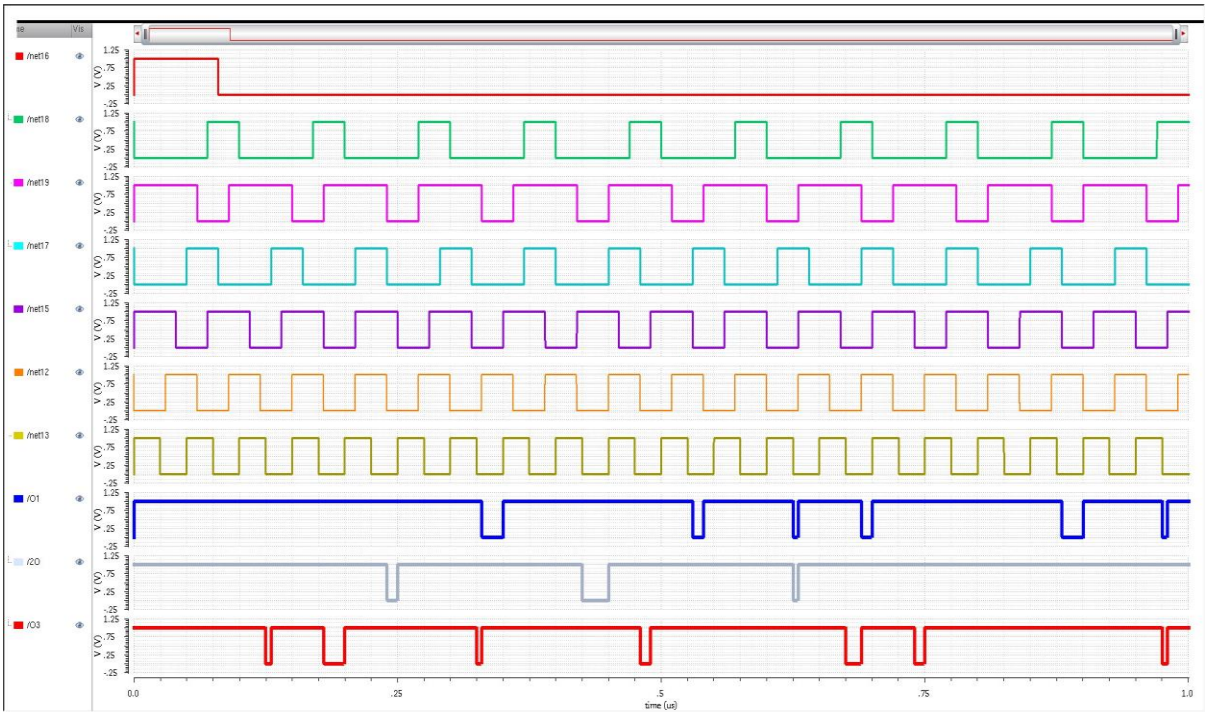


Fig. 4.2.3 Simulation of Priority Encoder 8:3

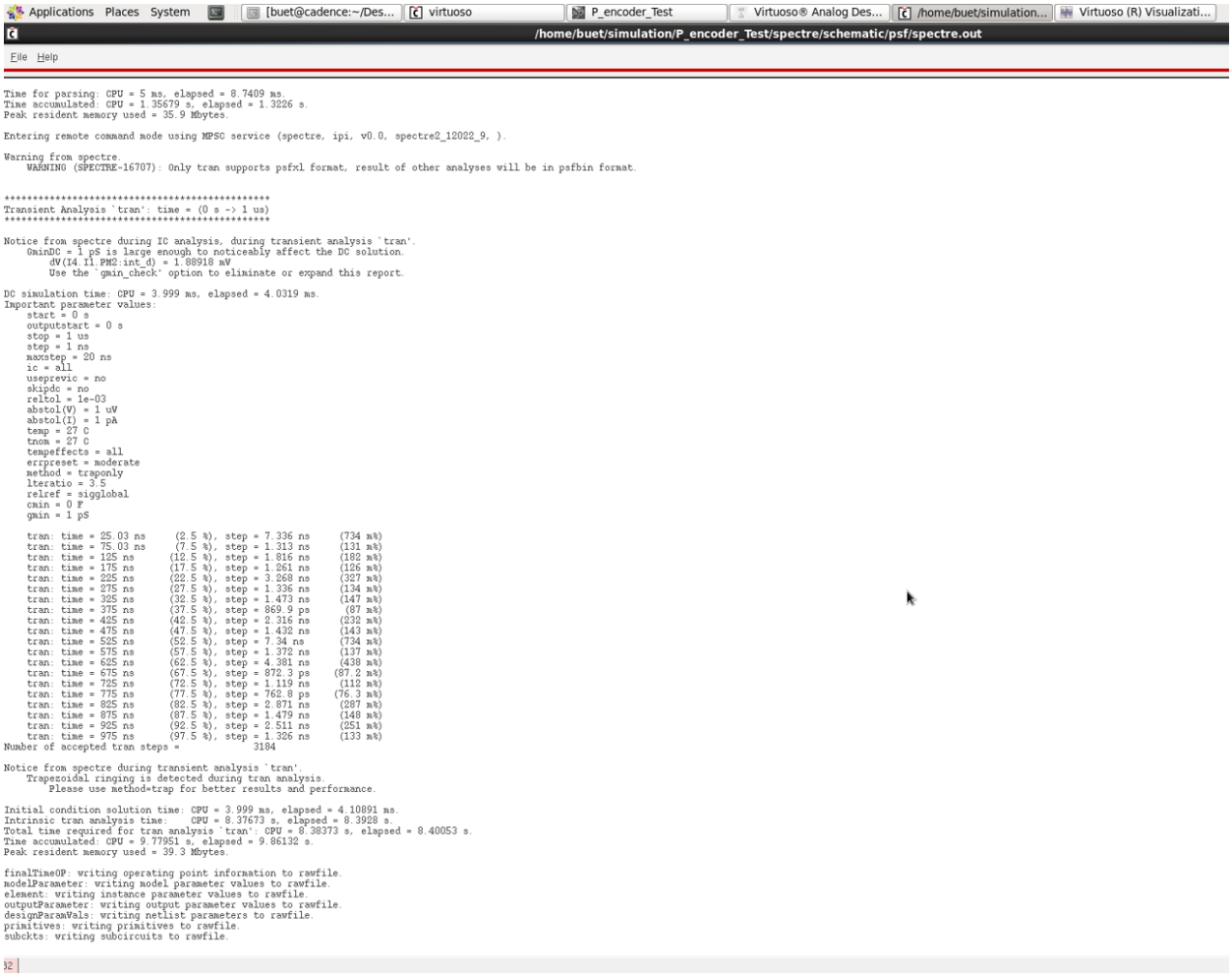


Fig. 4.2.4 Time Analysis of Priority Encoder 8:3

4.3 Implementation of Comparator

A comparator in electronics is a circuit or device used to compare two voltages or analog signals and determine their relationship: whether one is greater than, less than, or equal to the other.

It takes in two analog voltage inputs (often labelled as V+ and V-) and produces a digital output based on the comparison result. The output is typically in the form of a logic signal, where one state (usually high or '1') indicates that V+ is greater than V-, and the other state (usually low or '0') indicates the opposite.

The operation of a comparator is quite simple: if V+ is greater than V-, the output is at one logic level; if V+ is less than V-, the output is at the other logic level. Most comparators have very high gain and are designed to quickly respond to changes in input voltages.

Those comparators that drive their outputs between VOH and VOL for very small input voltage changes using a high-gain stage are an important class of comparators. A great example of an open-loop, high-gain comparator is the two-stage operational amplifier without compensation.

A two-stage open-loop comparator is an advanced form of a comparator circuit designed with two amplifier stages. This configuration is used to enhance the performance of the comparator, especially in terms of speed, precision, and reducing issues such as offset voltage or propagation delay.

Here's a basic breakdown of the two-stage open-loop comparator:

First Stage:

Input Stage: The first stage typically consists of a high-gain amplifier or differential amplifier that amplifies the voltage difference between the two input signals. This stage provides initial amplification and sets the basis for comparison.

Second Stage:

Output Stage: The output from the first stage feeds into a second amplifier stage that provides additional amplification and often includes circuitry to drive the output to rail-to-rail levels (close to the power supply voltage levels) to produce a digital output.

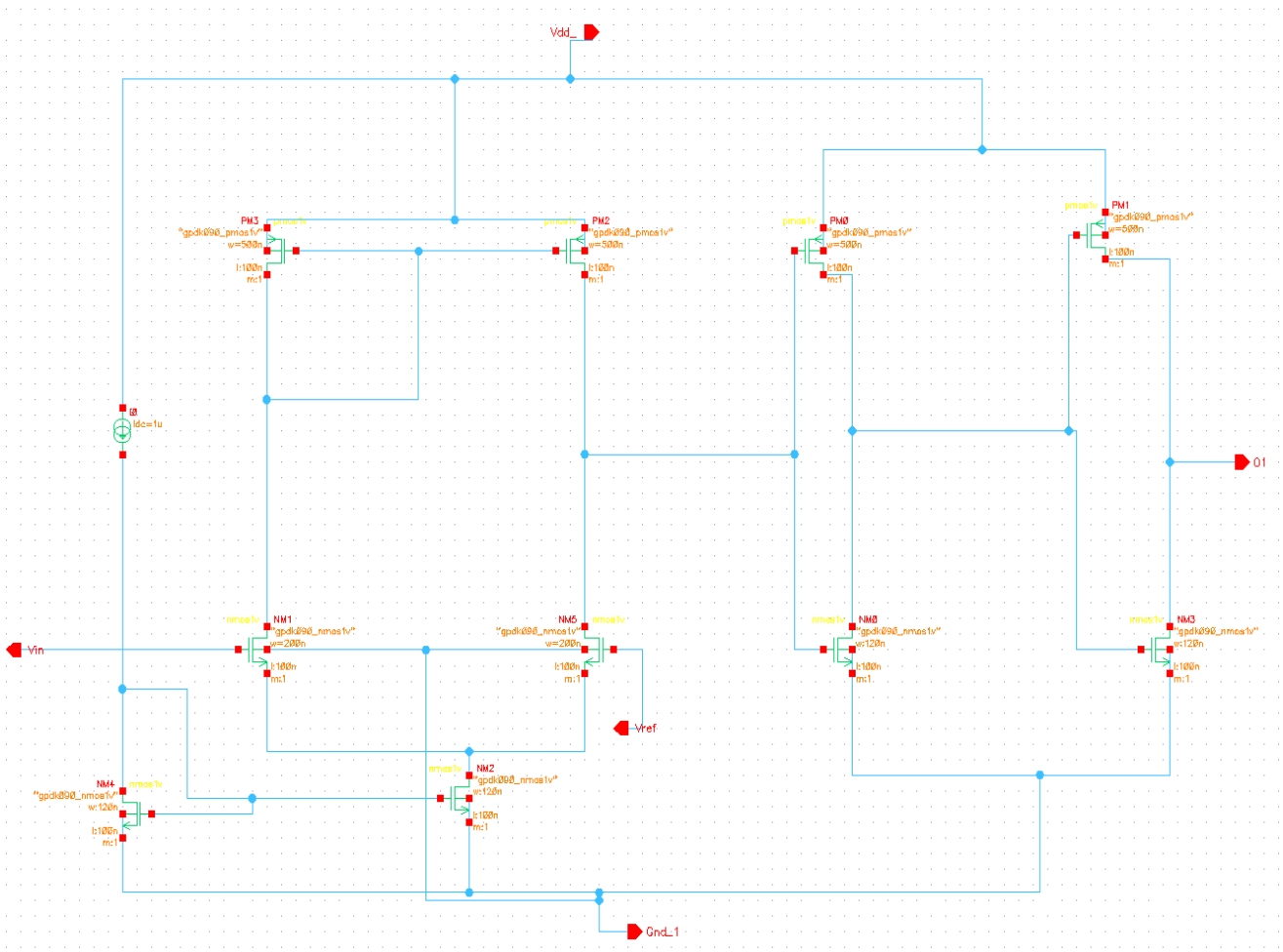


Fig. 4.3.1 Schematic of Comparator

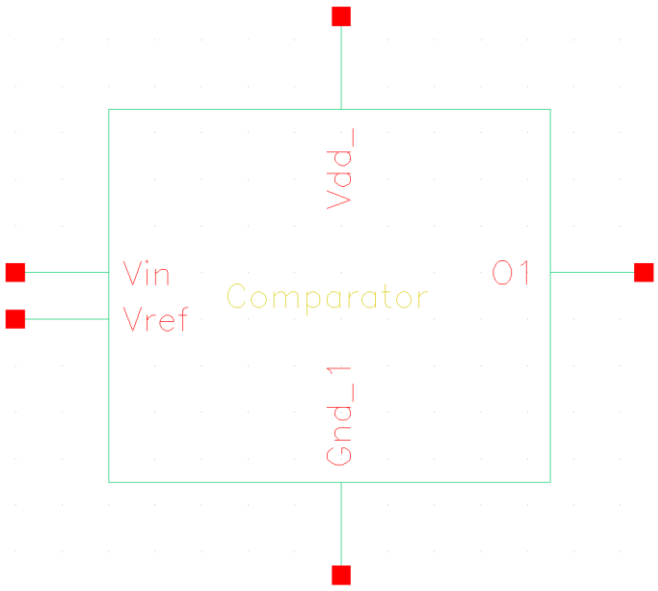


Fig. 4.3.2 Block diagram of Comparator

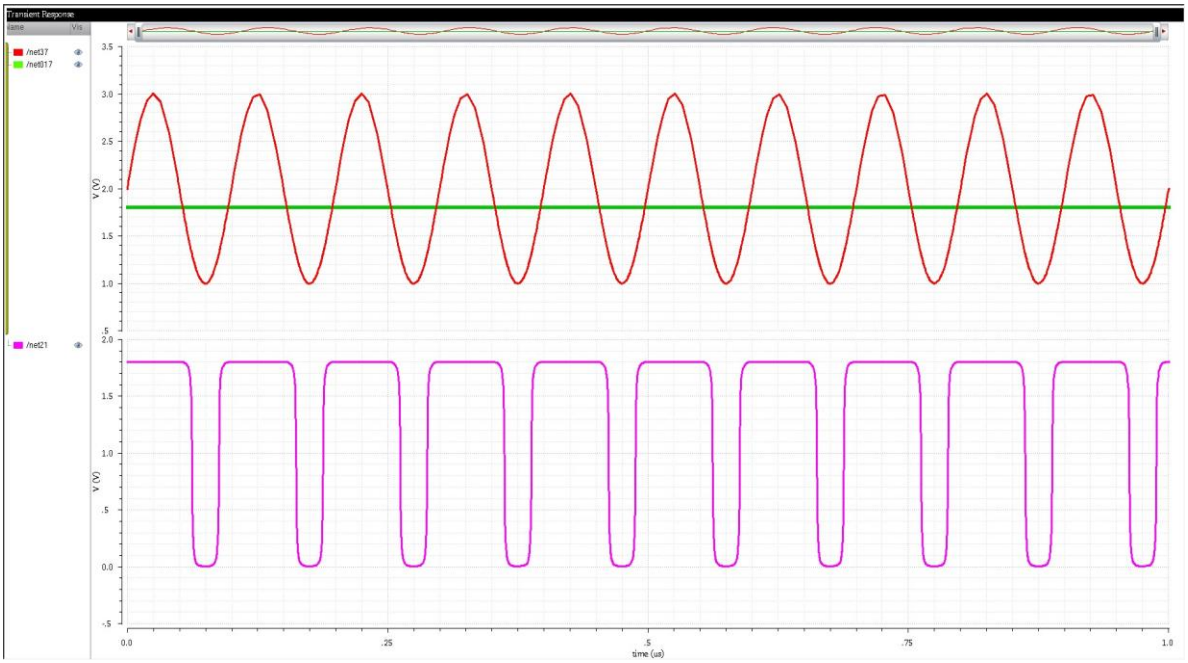
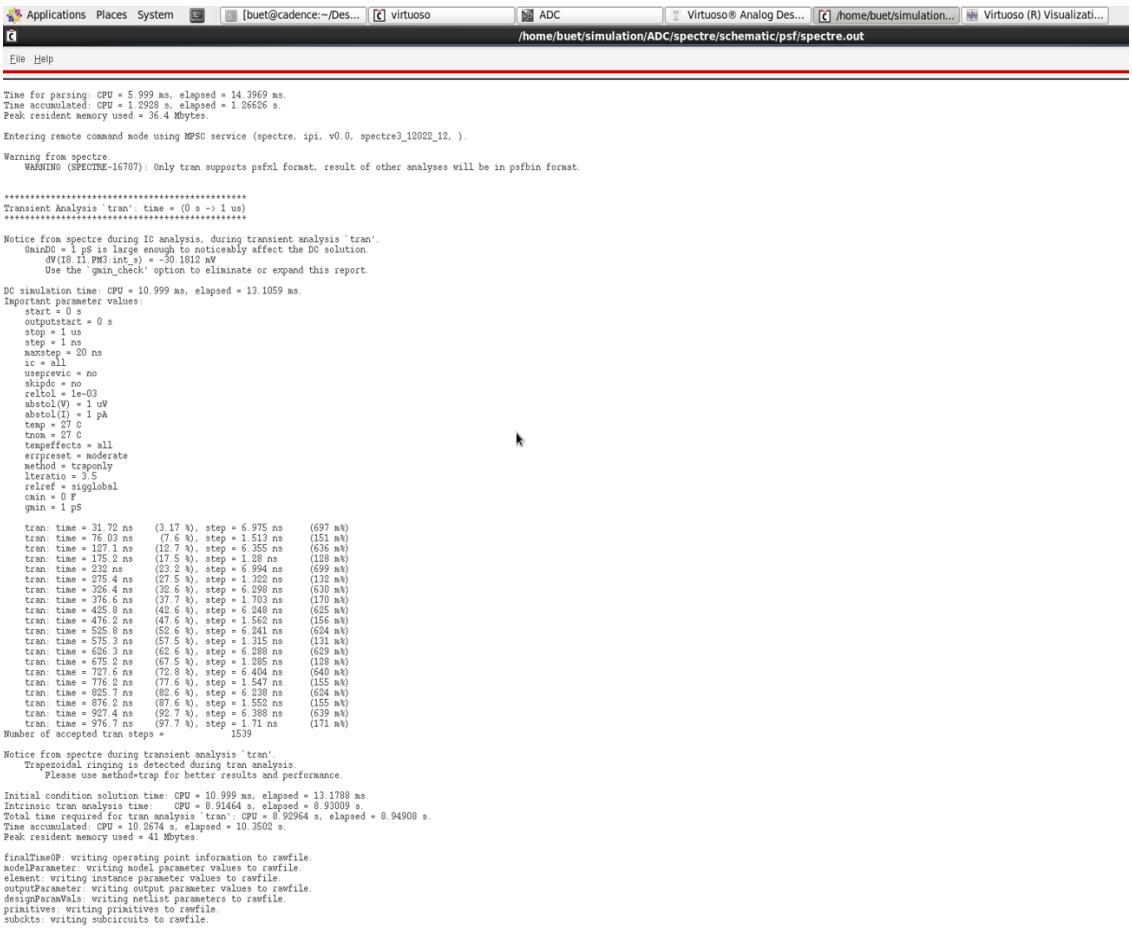


Fig. 4.3.3 Simulation of Comparator



```
Time for parsing: CPU = 5.999 ms, elapsed = 14.3969 ms.
Time accumulated: CPU = 1.2928 s, elapsed = 1.26626 s.
Peak resident memory used = 36.4 Mbytes.

Entering remote command mode using MPSC service (spectre, ipi, v0.0, spectre3_12022_12, ).

Warning from spectre.
    WARNING (SPECTRE-16707): Only tran supports psfxl format, result of other analyses will be in psfbin format.


*********************************************
Transient Analysis `tran': time = (0 s -> 1 us)
*********************************************

Notice from spectre during IC analysis, during transient analysis `tran'.
    GminDC = 1 pS is large enough to noticeably affect the DC solution.
        dV(I8.I1.PM3:int_s) = -30.1812 nV
        Use the `gmin_check' option to eliminate or expand this report.

DC simulation time: CPU = 10.999 ms, elapsed = 13.1059 ms.
Important parameter values:
    start = 0 s
    outputstart = 0 s
    stop = 1 us
    step = 1 ns
    maxstep = 20 ns
    ic = all
    useprevic = no
    skipdc = no
    reltol = 1e-03
    abstol(V) = 1 uV
    abstol(I) = 1 pA
    temp = 27 C
    tnom = 27 C
    tempeffects = all
    errpreset = moderate
    method = traponly
    lteratio = 3.5
    relref = sigglobal
    cmin = 0 F
    gmin = 1 pS

    tran: time = 31.72 ns     (3.17 %), step = 6.975 ns      (697 m%)
    tran: time = 76.03 ns      (7.6 %), step = 1.513 ns      (151 m%)
    tran: time = 127.1 ns     (12.7 %), step = 6.355 ns      (636 m%)
    tran: time = 175.2 ns     (17.5 %), step = 1.28 ns       (128 m%)
    tran: time = 232 ns       (23.2 %), step = 6.994 ns      (699 m%)
    tran: time = 275.4 ns     (27.5 %), step = 1.322 ns      (132 m%)
    tran: time = 326.4 ns     (32.6 %), step = 6.298 ns      (630 m%)
    tran: time = 376.6 ns     (37.7 %), step = 1.703 ns      (170 m%)
    tran: time = 425.8 ns     (42.6 %), step = 6.248 ns      (625 m%)
    tran: time = 476.2 ns     (47.6 %), step = 1.562 ns      (156 m%)
    tran: time = 525.8 ns     (52.6 %), step = 6.241 ns      (624 m%)
    tran: time = 575.3 ns     (57.5 %), step = 1.315 ns      (131 m%)
    tran: time = 626.3 ns     (62.6 %), step = 6.288 ns      (629 m%)
    tran: time = 675.2 ns     (67.5 %), step = 1.285 ns      (128 m%)
    tran: time = 727.6 ns     (72.8 %), step = 6.404 ns      (640 m%)
    tran: time = 776.2 ns     (77.6 %), step = 1.547 ns      (155 m%)
    tran: time = 825.7 ns     (82.6 %), step = 6.238 ns      (624 m%)
    tran: time = 876.2 ns     (87.6 %), step = 1.552 ns      (155 m%)
    tran: time = 927.4 ns     (92.7 %), step = 6.388 ns      (639 m%)
    tran: time = 976.7 ns     (97.7 %), step = 1.71 ns       (171 m%)
Number of accepted tran steps =                1539

Notice from spectre during transient analysis `tran'.
    Trapezoidal ringing is detected during tran analysis.
        Please use method=trap for better results and performance.

Initial condition solution time: CPU = 10.999 ms, elapsed = 13.1788 ms.
Intrinsic tran analysis time:    CPU = 8.91464 s, elapsed = 8.93009 s.
Total time required for tran analysis `tran': CPU = 8.92964 s, elapsed = 8.94908 s.
Time accumulated: CPU = 10.2674 s, elapsed = 10.3502 s.
Peak resident memory used = 41 Mbytes.

finalTimeOP: writing operating point information to rawfile.
modelParameter: writing model parameter values to rawfile.
element: writing instance parameter values to rawfile.
outputParameter: writing output parameter values to rawfile.
designParamVals: writing netlist parameters to rawfile.
primitives: writing primitives to rawfile.
subckts: writing subcircuits to rawfile.
```

Fig. 4.3.4 Time Analysis of Comparator

Overall, the use of a two-stage open-loop comparator can significantly improve the performance metrics important in many high-speed and precision analog applications compared to single-stage designs.

4.4 Analog to Digital Converter

Analog-to-digital converter is referred to as ADC. An Analog-to-Digital Converter (ADC) is a crucial component in electronics that converts analog signals into digital representations, allowing the processing and manipulation of real-world signals within digital systems. The primary function of this device, also known as an ADC, A/D, or A-to-D Converter, is signal conversion. It takes an analog signal and converts it to a digital format. There are several uses for AD converters, including digital music, radio, and digital photography, among other applications. Digital signal processing also employs it.

The ADC operates on a very basic concept. The ADC's operation is quite simple, it takes an analog signal and transforms it into a digital representation. It converts any kind of analog signal like sound or electricity into a digital representation. These ADC devices use billions of tiny binary digits to receive and store data.

These days, a wide range of technologies and electrical gadgets, including computers, smartphones, and many more, use analogue to digital converters. Analog-to-digital converters are primarily used to convert incoming signals from the physical world into the binary format—mostly in zero and one form—that computers use. These signals are commonly converted via ADC converters. In their analogue nature, signals such as sound and electricity can take on an endless number of shapes and forms. They can be processed and altered in a nearly different way using ADC.

This type of ADC uses a parallel structure with multiple comparators to quickly determine the input voltage's closest value from a set of reference voltage levels. It's very fast but can be limited in resolution due to the number of comparators needed for higher resolutions.

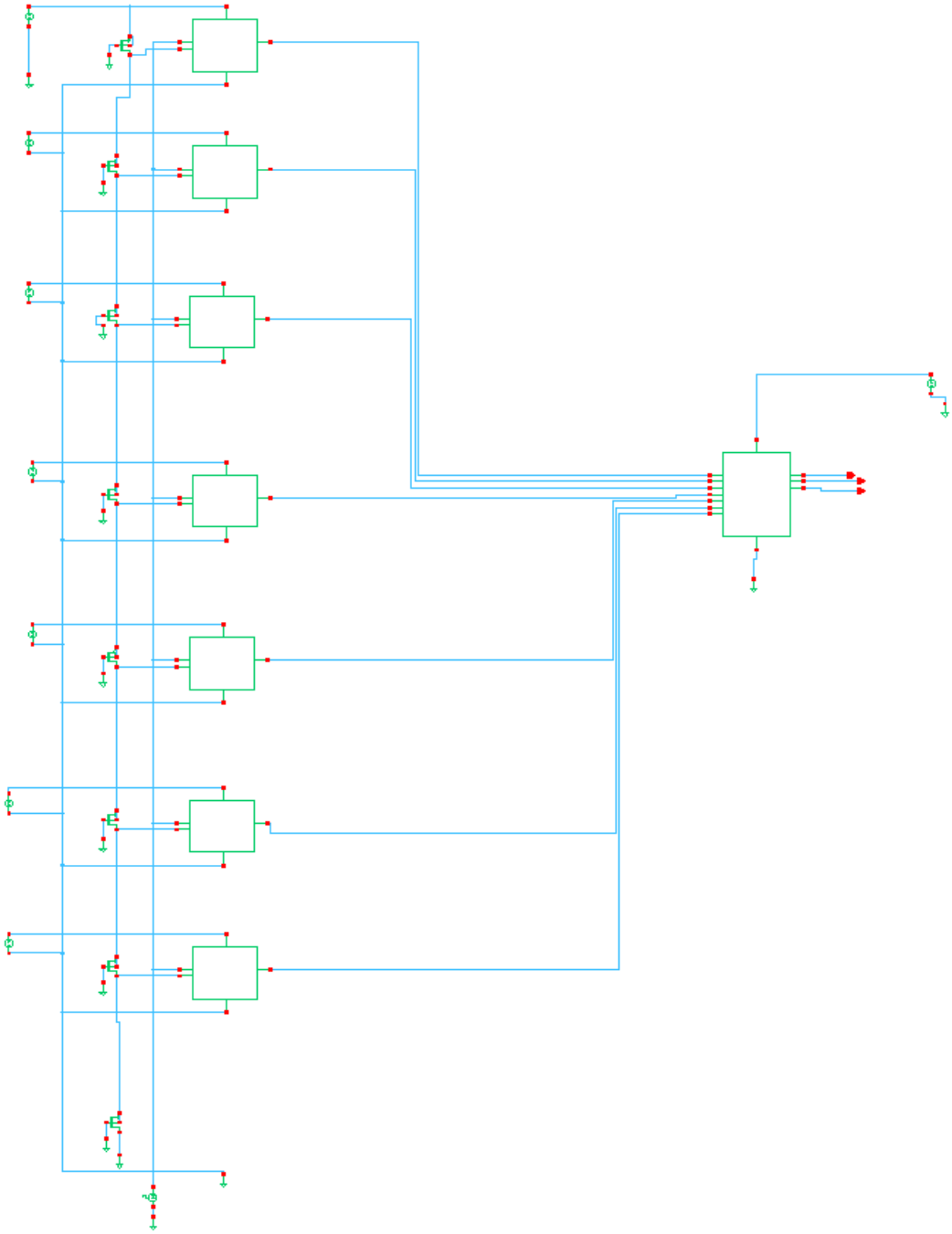


Fig. 4.4.1 Schematic of ADC

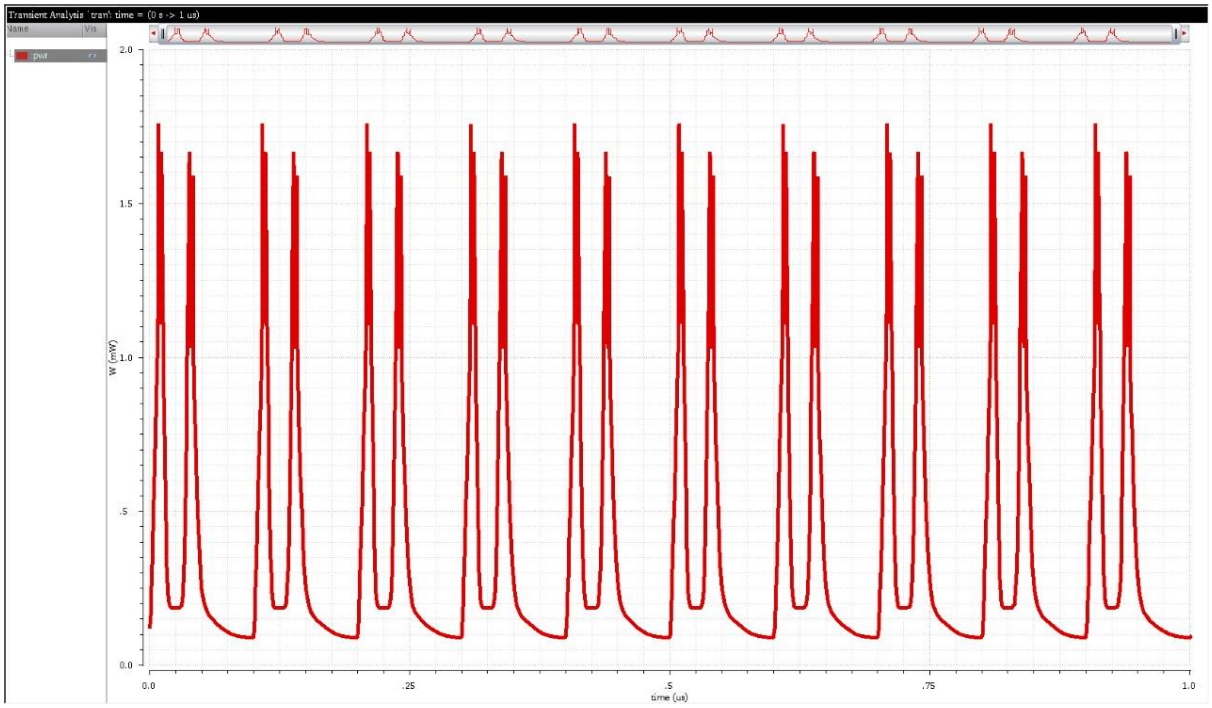


Fig.4.4.2 Power Analysis of ADC

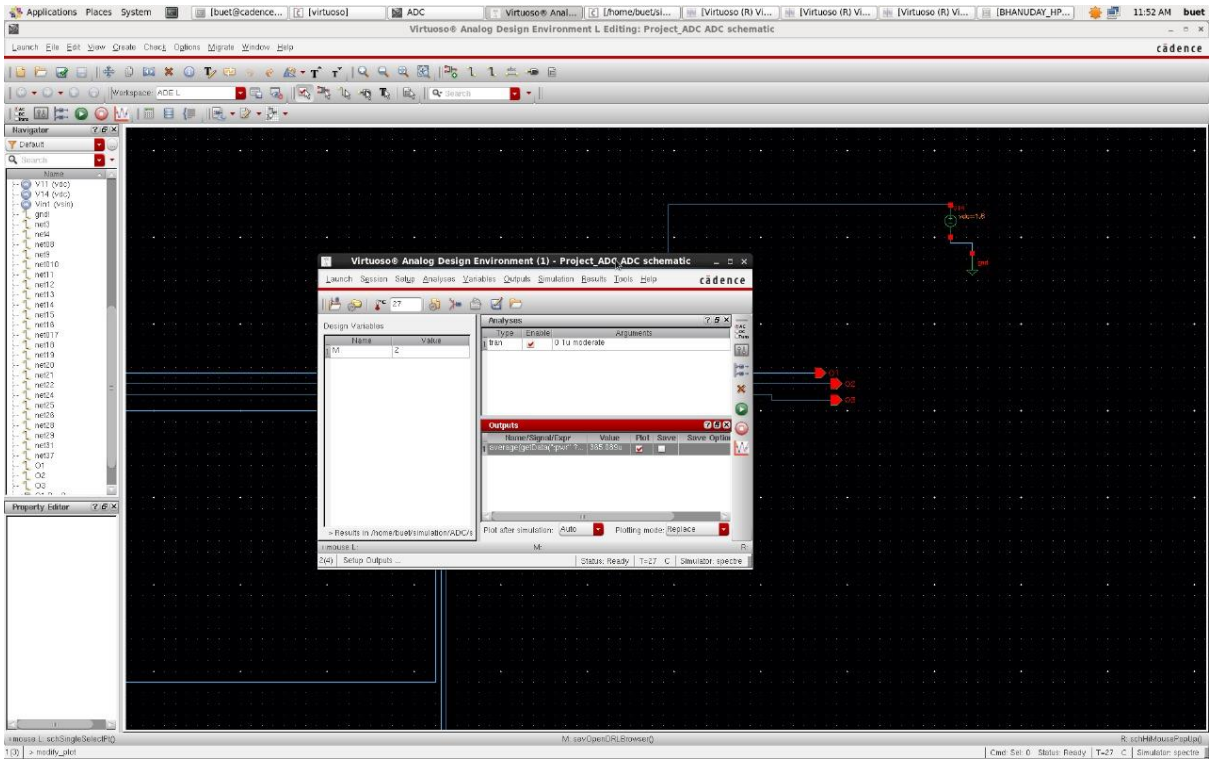


Fig.4.4.3 Power Analysis of ADC

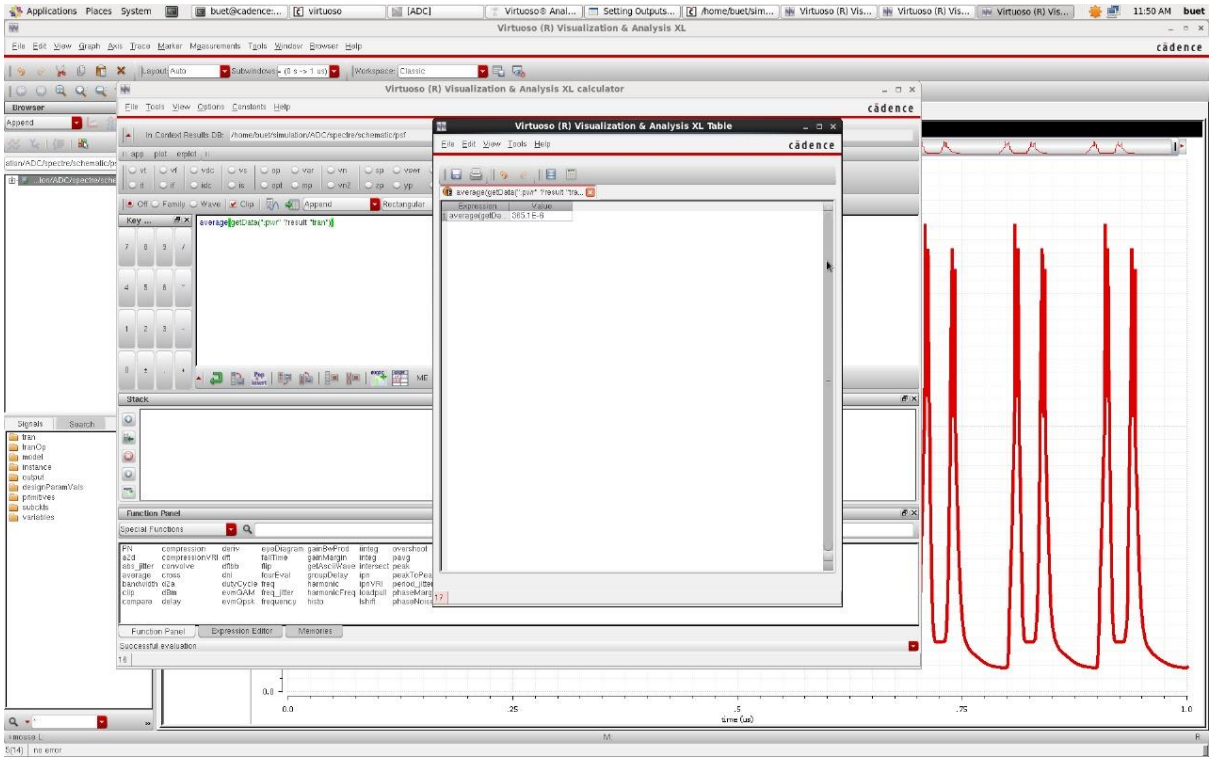


Fig.4.4.4 Delay Analysis of ADC

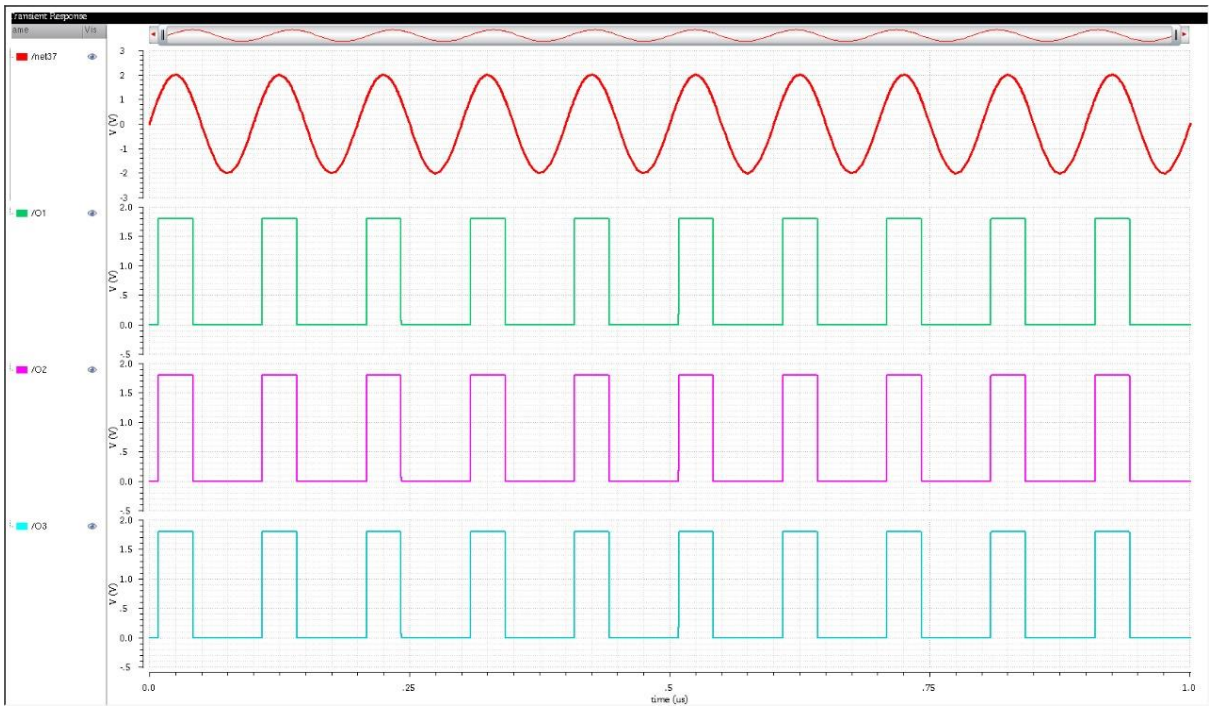


Fig.4.4.5 Digital Output of ADC

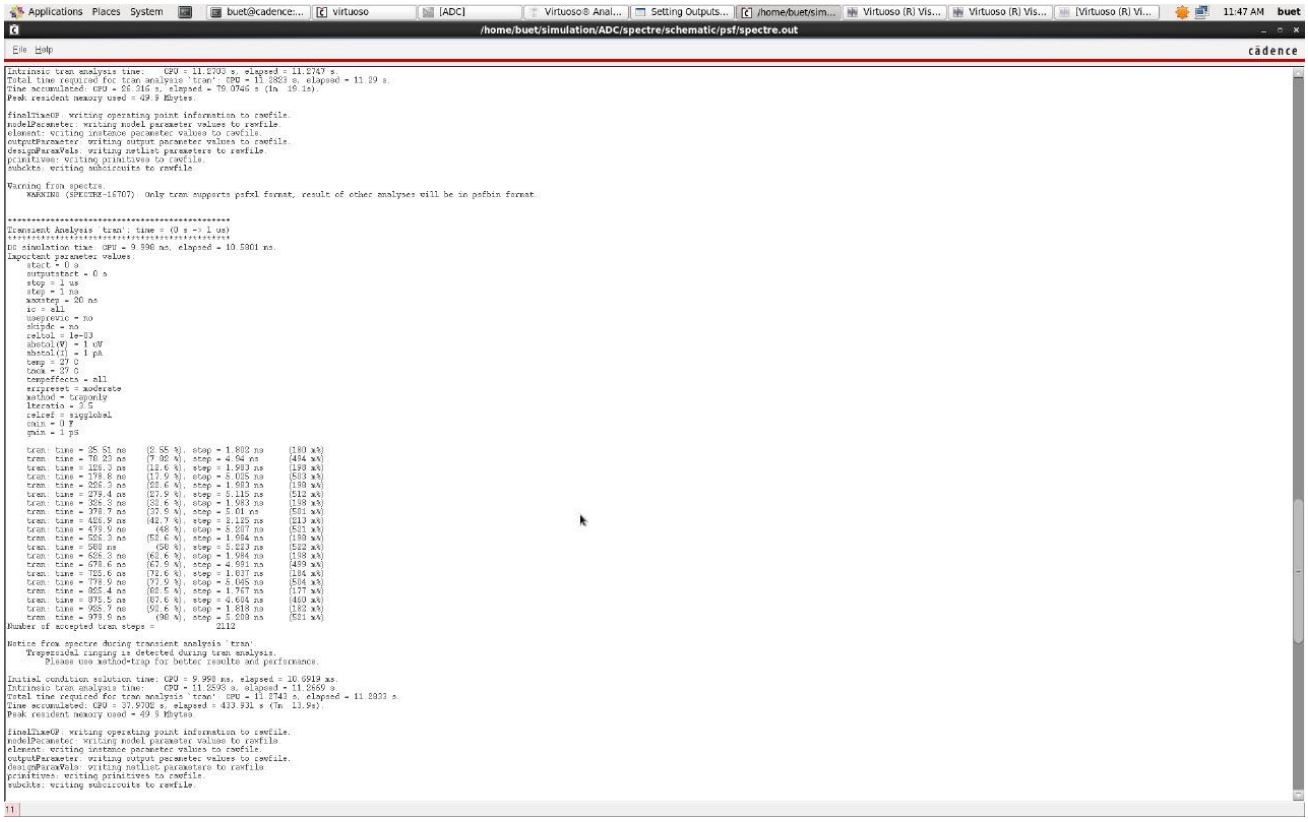


Fig4.4.6 Time Analysis of ADC

Table 4.4.1 Simulated Parameter

Analysis	**Resolution**	**Technology Node**	**Power**	**Delay**
Value	3-Bit	90nm	10.45mW	361.1 E-6

4.5 Comparison, Inference and Result

TABLE 1: PERFORMANCE COMPARSION OF VARIOUS ANALOG-TO-DIGITAL CONVERTERS

Topology	Flash	Counter	Single Slope	Dual Slope	SAR	Sigma Delta	Pipelined	Interleaving
Sampling Rate (Samples/Sec)	High (1G-10G)	Low (1-1k)	Low(100-1000)	Low (100-1000)	Medium(100k-10M)	Low (10k-1M)	Med-High (10M-100M)	Med-High (100M-1G)
Resolution (Bits)	Low(6-8)	Medium (10-12)	Medium-High (12-18)	Medium-High (12-18)	Medium-High (12-18)	High (16-24)	Medium-High (12-18)	Medium-High (12-18)
Power consumption	High	Medium-High	Low	Low	Low-Ultralow	Low	High	High
Latency	Low	Medium	Low-Medium	Low-Medium	Low	High	High	Low
Area	High	Low	Low	Low	Low	Medium	High	High
Accuracy	Low	Medium-High	Variable	High	Medium- High	High	Medium-High	Medium
Cost	High	Low	Medium	Medium	Low-High	Low	High	High
Conversion time (No. of cycles)	1	Depends on amplitude	2^N	$2*2^N$	Variable	High	2N/2 -1	Variable

Performance characteristics of ADCs, including sampling rate, the speed at which new digital values are extracted from the analogue signal, power consumption, the rate at which electrical energy is used in a circuit, conversion time, the amount of time the system takes to convert a discrete sample to a digital value, latency, accuracy, size, and cost have all been investigated to compare the various ADC topologies and are summarised here.

CHAPTER 5: CONCLUSION & FUTURE WORK

5.1 Conclusion

In conclusion, the magnetic flash analog-to-digital converter (ADC) has emerged as a revolutionary technology in the field of signal processing, offering significant advantages over traditional ADC architectures. the Analog to digital converter (ADC) has shown promising results in improving the performance and efficiency of converting analog input to digital output. The average power usage of eight analog inputs is calculated. In addition, the suggested magnetic ADC takes up less space than the traditional ADC. The utilization of magnetic tunnel junctions (MTJs) as comparators has enabled a substantial reduction in propagation delay, leading to enhanced circuit speed. Additionally, the compact nature of MTJs has resulted in a minimization of fabrication size, contributing to a more efficient and cost-effective design. Furthermore, the inherent low power consumption of MTJs has significantly reduced heat dissipation within the circuit, improving overall reliability and stability. In comparison to primitive ADCs, the magnetic flash ADC demonstrates a remarkable advancement in performance, offering faster conversion rates, smaller footprints, and lower power consumption.

The High-speed flash ADC architecture offers a scalable and parallel approach for addition operations, effectively reducing the propagation delay, minimising size in fabrication, decreasing the heat dissipation and enhancing overall circuit speed. Through extensive

simulations and comparisons with primitive Analog to digital converter, it has been demonstrated that the Parallel ADC can significantly outperform conventional ADC in terms of delay, power consumption, and area utilisation.

We have seen from above that a delay occurred for Magnetic High-speed parallel ADC < single slop ADC< Counter ADC<Pipelined ADC. Also, Power consumption for SAR<Single slop ADC<Magnetic flash ADC< Pipelined ADC.

Hence, we conclude on the basis of the above study that the performance of Magnetic Parallel ADC is best. As a result, this innovative ADC holds immense potential for applications in high-speed data acquisition, wideband communications, and optical and magnetic storage systems.

In our Simulated design we simulated 3-bit resolution ADC the circuit is based on 90nm technology node, on various analysis on candence virtuoso interface delay is 361.1 E-6, while power analysis report is 10.45mW in our proposed design for High-speed parallel ADC.

5.2 Future Work

Although the Analog to digital converter has demonstrated its effectiveness, there are still several areas that warrant further exploration and improvement. Some potential avenues for future work on ADC include:

1. **Optimization of the Architecture:** Investigate alternative architecture structures and configurations to optimize the trade-off between delay, power consumption, and area. Different architecture and interconnect schemes could be explored to enhance performance further.

2. **Error detection and correction:** Develop techniques to detect and correct errors that may occur during conversation operations using the ADC. Redundancy and error correcting codes could be implemented to improve the reliability of the ADC in critical applications. Circuit-level optimization: Explore circuit-level design techniques to minimize the power consumption and area utilization of the ADC. Investigate low-power design methodologies, transistor sizing, and interconnect optimization to achieve better performance metrics.

3. **Technology scaling and implementation:** Evaluate the scalability of the ADC in advanced technology nodes and investigate its performance in different process technologies. Consider the impact of process variations and develop techniques to mitigate their effects on ADC performance.

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Appendix

//Title: Compact model of Perpendicular Magnetic Anistropy (PMA) MTJ based on Spin transfer torque mechanism

//Version: Beta.1.0

//Date:25 January 2012

//Language: VerilogA

/*----------

In this model, it takes into account the static, dynamic and stochastic behavoirs of PMA MTJ nanopillar

1.MTJ resistance calculation based on brinkman model

2.TMR dependence on the bias voltage

3.Spin polarity calculation model for magnetic tunnel junction

4.Critical current calculation

5.Dynamic model (>critical current, also sun's model)

6.Stochastic model

The parameters are from the prototypes of Univ. Tohuku

----------*/

`resetall

`include "constants.vams"

`include "disciplines.vams"

```
`define explimit 85.0

`define exp(x) exp(min(max((x),-`explimit),`explimit))

`define sqrt(x) pow( (x), 0.5)


//Shape definition

`define rec 1

`define ellip 2

`define circle 3


/*-----------------------------------------

Electrical Constants

-----------------------------------------*/


/*----------Elementary Charge----------*/

`define e 1.6e-19

/*----------Bohr Magnetron Costant----------*/

`define ub 9.27e-28

/*----------Boltzmann Constant---------- */

`define Kb 1.38e-23

/*----------Planck's Constant---------- */

`define hbas 1.0545e-34

/*----------Electron Mass---------- */

`define m 9.10e-31

/*----------average heat capacity---------- */
```

```
`define Cv 3.47e6

/*----------Euler's constant---------------*/

`define C 0.577



module Model1(T1,T2,x,Ttrans,PI);


inout T1, T2;

electrical T1, T2;



/*----------X=store the state of the MTJ, non-volatile way---------- */

/*----------Ttrans=store the state of the MTJ with time influence, non-volatile way----------
*/

/*----------PI=switching probability---------- */

inout x,Ttrans,PI;

electrical x,Ttrans,PI;



/*----------------------------------------

MTJ Technology Parameters

(Corresponds to the HITACHI MTJ Process)

----------------------------------------*/


/*----------Gilbert Damping Coefficient---------------*/
```

```
parameter real  alpha=0.025;
/*----------GyroMagnetic Constant in Hz/Oe----------*/
parameter real  gamma=1.76e7;
/*----------Electron Polarization Percentage % ----------*/
parameter real  P=0.52;

/*----------Out of plane Magnetic Anisotropy in Oersteds----------*/
parameter real  Hk=0.1734e4;
/*----------Saturation Field in the Free Layer in Oersteds----------*/
parameter real  Ms=15800;
/*----------The Energy Barrier Height for MgO in electron-volt----------*/
parameter real  PhiBas=0.4;



/*----------Voltage bias when the TMR(real) is 1/2TMR(0) in Volt----------*/
parameter real  Vh=0.5;                  //experiental value with MgO barrier
/*----------Current Pulse width in second----------*/
parameter real  Pwidth=5e-9;

/*----------------------------------------
Device Parameters
(Corresponds to the HITACHI 240 x 80 MTJ)
----------------------------------------*/
/*----------Height of the Free Layer  in nm----------*/
parameter real  tsl=1.3e-9 from[0.8e-9:3.0e-9];
```

```
/*----------Length in nm----------*/
parameter real  a=40.0e-9;
/*----------Width in nm----------*/
parameter real  b=40.0e-9;
/*----------Radius in nm----------*/
parameter real  r=32.5e-9;
/*----------Height of the Oxide Barrier in nm----------*/
parameter real  tox=8.5e-10 from[8e-10:15e-10];
/*----------TMR(0) with Zero Volt Bias Voltage ----------*/
parameter real  TMR=1.2;

/*----------Shape of MTJ----------*/
parameter real SHAPE=2  from[1:3];  //SQUARE



/*----------MTJ State Parameters----------*/
/*----------Initial state of the MTJ, 0 = parallele, 1 = anti-parallele----*/
parameter integer       PAP=0 from[0:1];
/*----------Room temperature in Kelvin----------*/
parameter real          T= 300;//$random % 50 +323;
/*----------Resistance area product in ohmum2----------*/
parameter real          RA=5 from[5:15];
```

```
//variables

//Polaristion constant for the two states of STT-MTJ
real PolaP;      //Polarization state parallel of STT-MTJ
real PolaAP;     //Polarization state anti-parallel of STT-MTJ

real surface;    //Surface of MTJ

//Critical current density for the two states of STT-MTJ
real gp;         //Critical current density for P state
real gap;        //Critical current density for AP state

real Em;         //Variable of the Slonczewski model

//TMR real value for the two states of STT-MTJ
real TMRR;    //TMR real value for P state
real TMRRT;   //TMR real value for AP state

//Resistance of MTJ
real Ro;         //Resistance of MTJ when bias voltage = 0V
real Rap;        //Resistance value for AP state
real Rp;         //Resistance value for P state
```

```
//Voltage of MTJ
real Vb;        //V(T1,T2)
real Vc;        //V(T2,T1)

real Id; //Current of MTJ

//critial current for the two states of STT-MTJ
real IcAP;      //Critial current for AP state
real IcP;       //Critial current for P state

integer Teta;   //Parallele=0, Antiparallel=PI

real ix; //Current used to store the state of the MTJ

real tau;       //Probability parameter

real p;  //Probability density function

real FA; //Factor for calculating the resistance based on RA

integer seed;   //Used to initialize the random number generator

//Stochastic effects
real duration;  //time needed to be sure that the switching is effected
```

```
analog begin

        if (SHAPE==1)
                begin
                surface=a*b;    //SQUARE
                end
                else if (SHAPE==2)
                begin
                surface=`M_PI*a*b/4.0;          //ELLIPSE
                end
                else
                begin
                surface=`M_PI*r*r;    //ROUND
        end

Vc=V(T2,T1);
Vb=V(T1,T2);

//initial conditions
@(initial_step)
begin
```

```
FA=3322.53/RA;
Ro=(tox*1.0e10/(FA*`sqrt(PhiBas)*surface*1.0e12))*exp(1.025*tox*1.0e10*`sqrt(PhiBas));


Em=Ms*tsl*surface*Hk/2;

//States inititialisation
ix=PAP;
I(x)<+ ix;
I(Ttrans)<+ix;

I(PI)<+0;

end



if(V(Ttrans)==0)        //Case which the magnetizations of the two layers are parallel
        begin

        Teta=0;

        //Calcul of critical current
        PolaP=`sqrt(TMR*(TMR+2))/(2*(TMR+1));          //Polarization state parallel
```

```
gp=alpha*gamma*`e*Ms*tsl*Hk/(40*`M_PI*(`ub*PolaP));          //Critical current density

IcP=gp*surface;                    // Critical current

//TMR real
TMRR=TMR/(1+Vb*Vb/(Vh*Vh));

//Parallel resistance
Rp=Ro;

        if(Vb>=IcP*Rp)
                begin   //Current higher than critical current

                //STT-MTJ dynamic behavior : Sun model

duration=(`C+ln(`M_PI*`M_PI*(Em/(`Kb*T*40*`M_PI))/4))*`e*1000*Ms*surface*tsl*(1+P*P)/(4*`M_PI*2*`ub*P*10000*abs(Id-IcP));
                //Time needed to be sure that the switching is effected

                        if((duration<Pwidth))
                                begin   //Switching of the free layer always occurs
                                ix=-1.0;   //change the current state of MTJ
```

```
                    Id=Vb/Rp;
                end
                else
                    begin   //Switching of the free layer doesnt occur
                    ix=0.0;         //save the current state of MTJ
                    Id=Vb/Rp;
                end

        end

        else
            begin   //Current smaller than critical current

            ix=0.0;//save the current state of MTJ

            Id=Vb/Rp;
        end

end

if(V(Ttrans)!=0)        //Case which the magnetizations of the two layers are antiparallel

    begin
```

```
Teta=`M_PI;

PolaAP=`sqrt(TMR*(TMR+2))/(2*(TMR+1));        //Polarization state anti parallel

gap=alpha*gamma*`e*Ms*tsl*Hk/(40*`M_PI*(`ub*PolaAP));      //Critical current density

IcAP=gap*surface;     // Critical current

//TMR real

TMRRT=TMR/(1+Vb*Vb/(Vh*Vh));

// Antiparallel resistance

Rap=Ro*(1+TMRRT);

Rp=Ro;

        if(Vc>=(IcAP*Rap))

                begin   //Current higher than critical current

                //STT-MTJ dynamic behavior : Sun model

duration=(`C+ln(`M_PI*`M_PI*(Em/(`Kb*T*40*`M_PI))/4))*`e*1000*Ms*surface*tsl*(1+P*P)/(4*`M_PI*2*`ub*P*10000*abs(-Id-IcAP));

                //time needed to be sure that the switching is effected
```

```
                if((duration<Pwidth))
                        begin   //Switching of the free layer always occurs
                        ix=0.0;         //save the current state of MTJ

                        Id=Vb/(Rap);
                        //Id=(Vb*(1+TMRRT))/(Rap);
                end
                else
                        begin   //Switching of the free layer doesnt occur
                        ix=-1.0;                //save the current state of MTJ
                        Id=Vb/(Rap);
                end

        end

        else
                begin   //Current smaller than critical current

                ix=-1.0;        //save the current state of MTJ
                Id=Vb/(Rap);
        end

end
```

```
I(x)<+ix;          //Actualisation of the state of x with the value calculated

//Ttrans has the same function than x but it includes the time effects

V(Ttrans)<+transition(V(x),duration,1e-10,1e-10);

I(T1,T2)<+Id; //Actualisation of the current of MTJ with the value calculated

I(PI)<+-p;                  //Probability density function

end

endmodule
```