```
1   -- 8x1 Mux using Case Statement
2   ----------------------------------------------------------------------------------
3   library IEEE;                                       --Importing Library
4   use IEEE.STD_LOGIC_1164.ALL;
5
6
7   entity mux8x1_case is                               -- Entity Declaration
8       Port ( a0,a1,a2,a3,a4,a5,a6,a7 : in std_logic;    --Defining inputs and outputs
9              x,y,z: in std_logic;
10            b : out  STD_LOGIC);
11  end mux8x1_case;                                    --End of Entity
12
13  architecture Behavioral of mux8x1_case is           --Architecture Declaration
14
15  begin
16     process(a0,a1,a2,a3,a4,a5,a6,a7,x,y,z)           --Process Intialization
17     variable s: STD_LOGIC_vector(2 downto 0);        --Variable Declaration
18     begin
19     s(0):= x;
20     s(1):= y;
21     s(2):= z;
22        case s is                                     --Start of case Statement
23           when "000" => b <= a0;
24           when "001" => b <= a1;
25           when "010" => b <= a2;
26           when "011" => b <= a3;
27           when "100" => b <= a4;
28           when "101" => b <= a5;
29           when "110" => b <= a6;
30           when "111" => b <= a7;
31           when others => null;
32        end case;                                     --End of Case
33  end process;                                        --End of Process
34  end Behavioral;                                     --End of Architecture
35
36
```