

```
1  -- 1x8 Demux Using Case Statement
2  -----
3  library IEEE;                                --Importing Library
4  use IEEE.STD_LOGIC_1164.ALL;
5  entity demux1x8_case is                        -- Entity Declaration
6      Port ( a,s1,s2,s3 : in bit;                --Defining inputs and outputs
7              x : out bit_vector(7 downto 0));
8  end demux1x8_case;                            --End of Entity
9
10 architecture Behavioral of demux1x8_case is    --Architecture Declaration
11
12 begin
13 process(a,s1,s2,s3)                            --Process Initialization
14 variable sel: bit_vector(2 downto 0);          --Variable Declaration
15 variable b: bit_vector(7 downto 0);            --Variable Declaration
16 begin
17     sel(0) := s1; sel(1) := s2; sel(2) := s3;
18     case sel is
19         when "000" =>
20             b(0) := a; b(1) := '0'; b(2) := '0'; b(3) := '0'; b(4) := '0'; b(5) := '0'; b(6) := '0'; b(7) := '0';
21
22         when "001" =>
23             b(0) := '0'; b(1) := a; b(2) := '0'; b(3) := '0'; b(4) := '0'; b(5) := '0'; b(6) := '0'; b(7) :=
24             '0';
25
26         when "010" =>
27             b(0) := '0'; b(1) := '0'; b(2) := a; b(3) := '0'; b(4) := '0'; b(5) := '0'; b(6) := '0'; b(7) :=
28             '0';
29
30         when "011" =>
31             b(0) := '0'; b(1) := '0'; b(2) := '0'; b(3) := a; b(4) := '0'; b(5) := '0'; b(6) := '0'; b(7) :=
32             '0';
33
34         when "100" =>
35             b(0) := '0'; b(1) := '0'; b(2) := '0'; b(3) := '0'; b(4) := a; b(5) := '0'; b(6) := '0'; b(7) :=
36             '0';
37
38         when "101" =>
39             b(0) := '0'; b(1) := '0'; b(2) := '0'; b(3) := '0'; b(4) := '0'; b(5) := a; b(6) := '0'; b(7) :=
40             '0';
41
42         when "110" =>
43             b(0) := '0'; b(1) := '0'; b(2) := '0'; b(3) := '0'; b(4) := '0'; b(5) := '0'; b(6) := a; b(7) :=
44             '0';
45
46         when others =>
47             b(0) := '0'; b(1) := '0'; b(2) := '0'; b(3) := '0'; b(4) := '0'; b(5) := '0'; b(6) := '0'; b(7)
48             := a;
49
50     end case;                                --End of case
51     x <= b;                                  --Assigning value back to original signal
52 end process;                                --End of Process
53 end Behavioral;                             --End of Architecture
```