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1  --TESTBENCH FOR DIF_IFFT_8PT
2  LIBRARY ieee;                                --IMPORTING LIBRARY
3  USE ieee.std_logic_1164.ALL;
4  library work;                                --WORKING IN CURRENT(WORK) FOLDER
5  use work.dif_ifft_pkg.all;                   --USING PACKAGE DIF_IFFT_PKG
6  FROM WORK DIRECTORY
7  -----
8  ENTITY tb IS                                --TESTBENCH ENTITY DECLARATION
9  END tb;
10 -----
11 ARCHITECTURE behavior OF tb IS               --ARCHITECTURE DECLARATION
12 signal s,y : ar;                             --SIGNAL DECLARATION
13 begin
14 uut: entity work.dif_ifft_8pt PORT MAP (s => s,y => y);-- Instantiating the Unit
    Under Test (UUT)
15     -- Stimulus process
16     stim_proc: process
17     begin
18         s(0) <= (1.0,0.0);                    --GIVING INPUTS
19         s(1) <= (2.0,0.0);
20         s(2) <= (3.0,0.0);
21         s(3) <= (4.0,0.0);
22         s(4) <= (5.0,0.0);
23         s(5) <= (6.0,0.0);
24         s(6) <= (7.0,0.0);
25         s(7) <= (8.0,0.0);
26         wait;                                --WAIT STATEMENT
27     end process;                             --END OF PROCESS
28 end behavior;                                --END OF ARCHITECTURE
29 -----
-----
```