BTech CSE
1st Year Sem1

Full notes PDF

Utkarsh Aggarwal

ELECTRONICS ENGINEERING

(Utkarsh Aggarwal)
(B Tech 1st Year Sem-1)
(Electronics Notes)

BEC101 / BEC201 : FUNDAMENTALS OF ELECTRONICS ENGINEERING

Topics	Contact Hours
Unit-1	8
Semiconductor Diode: Depletion layer, V-I characteristics, ideal and practical Diodes, Diode Equivalent Circuits, Zener Diodes breakdown mechanism (Zener and avalanche) **Diode Application:** Diode Configuration, Half and Full Wave rectification, Clippers, Clampers, Zener diode as shunt regulator, Voltage-Multiplier Circuits **Special Purpose two terminal Devices:** Light-Emitting Diodes, Photo Diodes, Varactor Diodes, Tunnel Diodes.	
Unit-2	8
Bipolar Junction Transistor: Transistor Construction, Operation, Amplification action. Common Base, Common Emitter, Common Collector Configuration **Field Effect Transistor:** Construction and Characteristic of JFETs. Transfer Characteristic. MOSFET (MOS) (Depletion and Enhancement) Type, Transfer Characteristic.	
Unit-3	8
Operational Amplifiers: Introduction, Op-Amp basic, Practical Op-Amp Circuits (Inverting Amplifier, Non-inverting Amplifier, Unit Follower, Summing Amplifier, Integrator, Differentiator).Differential and Common-Mode Operation, Comparators.	
Unit-4	8
Digital Electronics: Number system & representation, Binary arithmetic, Introduction of Basic and Universal Gates, using Boolean algebra simplification of Boolean function. K Map Minimization upto 6 Variables.	
Unit-5	8
Fundamentals of Communication Engineering: Basics of signal representation and analysis, Electromagnetic spectrum Elements of a Communication System, Need of modulation and typical applications, Fundamentals of amplitude modulation and demodulation techniques. **Introduction to Wireless Communication:** Overview of wireless communication, cellular communication, different generations and standards in cellular communication systems, Fundamentals of Satellite & Radar Communication.	

Electronics Engenering (24/Nov/2022)

Semiconductor:- (Note)

Through semiconductors we can build tiny switches, working on electrical on/off concepts, No moving parts and electrically controlled.

Semiconductor Materials:-

A special class of materials/elements having a conductivity b/w a good conductor and an insulators.

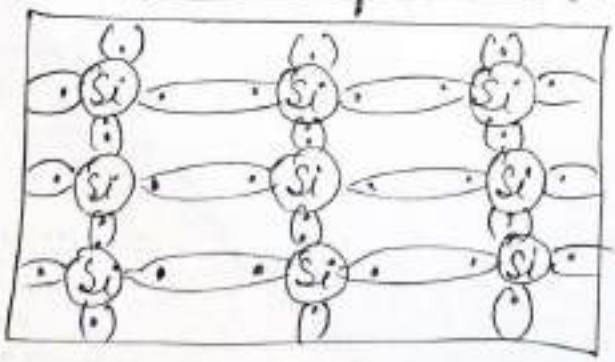
Types of Semiconductor Materials:-

① Single crystal	② compound
• They have a repeatitive crystal structure. (Eg)	• These are constructed of 2 or more semiconductor materials of different atomic structures.
Eg = Germanium (Tetra) (2,8,4) 14	Eg = • Gallium Arsenide ($Ga^{3}As^{5}$)
Silicon (Tetra) (2,8,18,4) 32	• (GaAsP)

* Silicon can make bond with 4 others.

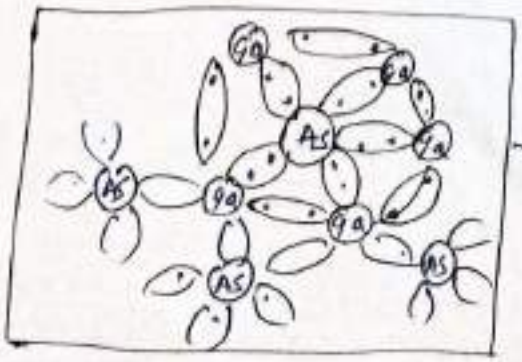
Q.Imp # why valence e^- are used to decide valency?
= cause they have min force of nucleus & can be easily knocked.

Structure of Silicon. (At microscopic level)



→ Single crystal

Structure of As with Ga



→ compound.

Note :- The term valence is used to indicate that the potential req'd to remove any one of these e^- from the atomic structure is significantly lower than that req'd for any other electron in the structure.

25/Nov/2022

Imp Question Intrinsic (Pure) semiconductor materials have free charge carriers at room temp why?

Ans it is possible for the valence e^- to absorb sufficient from external causes (such as heat energy & thermal energy from the surrounding medium) to break the covalent bond which results in free charge carriers

∴ At absolute temp = insulators.

Room temp 27°C/300K

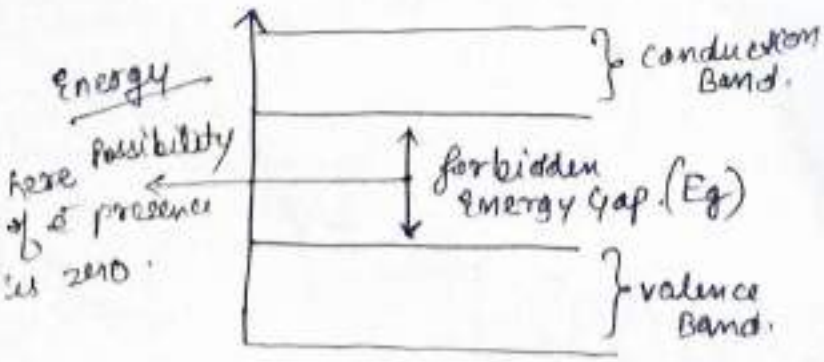
Imp Question Semiconductor materials have -ve temp coefficient. explain the statement?

Ans: for conductors the resistance increases with increase in temp. This is because the no of free of charge carrier in a conductor don't increase significantly with temperature in this manner they are said to have a +ve temp coefficient.

Semi conductors materials contains and increased level of conductivity with application of temp as the temp increases an increasing no of valence e^- absorbs sufficient thermal energy to break the covalent bond & thus contribute to the number of free charge carriers. ∴ Semi Cond materials have a -ve temp coefficient.

Concept of conduction Band

Per cubic metre Area have 10^{23} e^-



On single Atom we use energy levels on molecule we use Band.

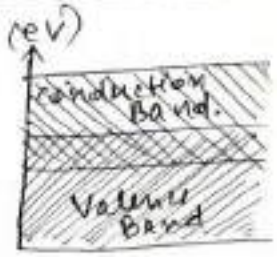
* The conduction Band represents the next larger group of permissible energy levels. There is an energy gap (eg) b/w the valence Band and conduction Band. An electron can be lifted from the valence band to the conduction band by adding some energy. This energy must be more than (Eg).

E_g = 0.67eV (germanium) 1.43eV (GaAs)
1.1eV (silicon) — most Preffered.
BASIC Reason. — thermally unstable.
left by Mam for further explanation

Imp why silicon is more widely used semiconductor material?
> As we know E_g (for Ge is = 0.67eV & for Si is 1.10V) thus E_g(Si) > E_g(Ge). in germanium valence e^- will need small energy to escape from the valence band so it increases more e^- & hole pair hence the leakage current is more in Germanium than silicon. this property makes Germanium more unstable at high temp. where as silicon is thermally stable

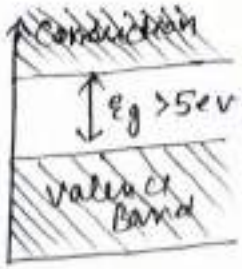
Classification Materials on basis of energy band diagram

* Conductors



There is no forbidden energy gap b/w the valence band & cond^n band the 2 bands actually overlaps. ∴ without supplying any external energy such as heat or light, a conductor already contains a large no of free e^- that's why they are good conductor

* Insulators



(Always)
Band Gap of Conductors
^
Semiconductors ($E_g \cong$ 1eV)
^
insulators (E_g > 5eV)
↓ increases

* Semiconduction

Insulators

An insulating material has a very wide forbidden energy gap (5eV or more) so it's practically impossible for an e^- in the valence band to jump the gap to reach the conduction band. That's why they are insulators.

Semi Conductors:-

In semi conductor the forbidden energy gap is not wide. It is of the order of 1eV. Energy provided by the heat at room temp is sufficient to lift the e^- from the valence band to the conduction band therefore at room temp, semi conductors are capable of conducting some electric current.

Intrinsic Semiconductor: Semiconductor in its purest form.

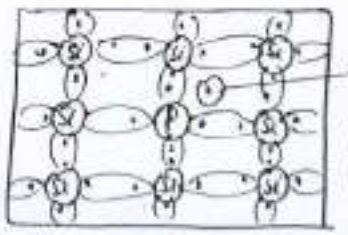
Extrinsic semiconductor: The process of adding impurities to a pure semi conductor to change its conductivity is known as doping. A doped semi conductor is known as extrinsic SC.

* Impurity materials can be of 2 types:-
  - Donor impurity → (Pentavalent) → (N-type) (P = Phosphorus)
  - Acceptor impurity → (trivalent) → (P-type)

N type extrinsic semiconductor materials:- (SC)

IMPURITIES: P AS Sb

- If a small amount of Pentavalent impurities are added to intrinsic (SC), N type (SC) is obtained.
- Impurities can be Phosphorus (P), Antimony (Sb) and Arsenic (As).



- Here 5th e^- has no chance of forming a covalent bond, in this way each impurity atom donates (1 e^-) to the conduction Band due to this reason pentavalent impurity is also known as donor type impurity.

(+) = Phosphorus atom
(majority) • = electrons free
(minority) o = holes by thermal generation.
□ = Slab of silicon.

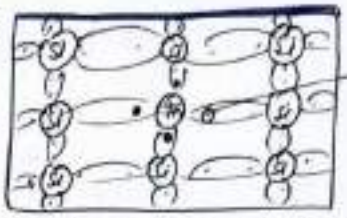
(The representation of N-type SC)

Electronics 25/NOV/2022

IMPURITIES
BalGaI

P type semiconductors

- if a small amount of trivalent impurity atoms are added to intrinsic (SC), P type (SC) is obtained.
- Impurities can be Boron, Al, Ga, Indium



→ holes created by Indium

- There are 3 valence e^- which forms covalent bonds with 3 neighbouring Silicon atoms but the 4 core bond of covalent is not complete.

(Imp) A vacancy that exist in the incomplete covalent Bond constitute a hole.

⊖ → immobile (-ve Acceptor) ion. Indium atoms.
• → electrons (minority)
o → holes (majority).

(The representation of P-type)

Q# Comparision b/w conductors & semiconductors.?
Q# Comparision b/w intrinsic & Extrinsic (SC)?
] Home Work

Answer-1 [Homework]

Conductors	Semiconductors
• These elements having no band gap, valence & conduction band overlaps.	• These elements have a band gap of 1ev.
• Needs no external energy like heat, light etc.	• Requires the energy = bandgap energy in form of A, light.
• As temp (↑) conductivity (↓)	• As temp (↑) conductivity (↑)
• Already have plenty of e^- (free) in it.	• free e^- are created as the bonds breaks on the influence of external energy.

Answer-2

(intrinsic semiconductor)

- It is the purest form of semiconductors humans achieved.
- these conductors have low and non benifial conductivity thus not preffered.

(Extrinsic semiconductor)

- It is the intrinsic semi-conductor which is doped with either tetravalent or trivalent impurities.
- These conductors can be used in our own way that's benificial.
- Impurities Added:-
  - ~~Tetra~~ Tetravalent (Acceptor)
  - Pentavalent (Donor)

(P type)

- holes (major)
- e^- (minor)
- Acceptor ions
- trivalent impurities (B AL GA I)
- Boron, Aluminium, Gallium, Indium.
-

Representation

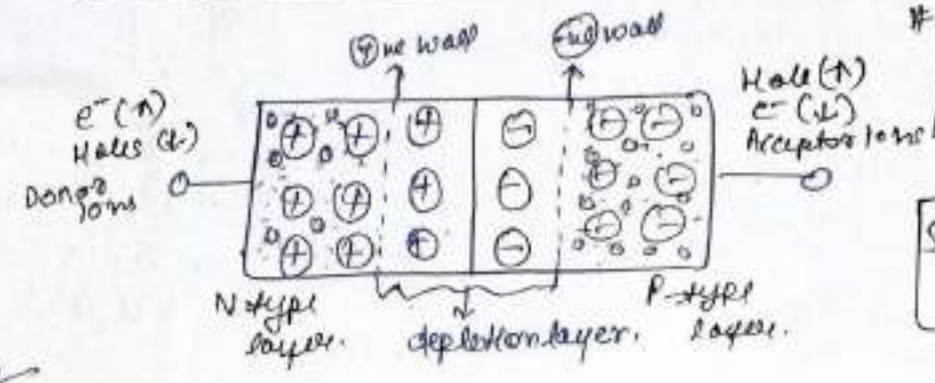
(N type)

- holes (minor)
- e^- (major)
- Donor ions
- Pentavalent impurities (P As Sb)
- Phosphorus, Arsenic, Antimony.
-

Representation

(P-N Junction Diode) 25/Nov/2022 and 30/Nov/2022

Depletion layer formation / space charge region on PN junc^n diode with no Bias :- (Vimp)



[Junction par recombination hoga.]

Symbol
Anode Cathode

~~V Imp~~

- A P-N junction is called as P-N Diode or semiconductor diode its a unidirectional 2 terminal (SC) device.

01/Dec/2022

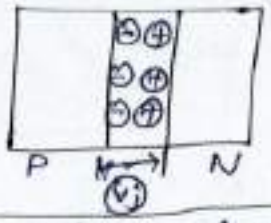
Depletion layer

- when PN junction forms holes from P-region diffuse in n-region & combines with e⁻.
- e⁻ from n region diffuse into p-region & combines with free holes.
- This process of diffusion takes place only for a short time, after few recombinations a force called barrier potential is setup automatically at the junction.
- further holes trying to diffuse into n-region are repelled by the donor ions; similarly for the e⁻ trying to diffuse into p-region are repelled by the acceptor ions. Thus further diffusion stops.
- The region of +ve & -ve immobile ion is called as depletion region. because there is a depletion of mobile charge carriers. this region contains immobile fixed ions which are electrically charged ∴ it's also known as space charge region

(Potential Barrier / junction potential)

01/Dec/2022

- Due to presence of immobile (+ve, -ve) ions on opposite sides of a junction, an electric field exists across the junction which is known as Potential barrier / junction potential.



V_j = 0.7 volt (silicon)

V_j = 0.3 volt (germanium)

DL = Depletion layer

more doping lesser the width of depletion layer

temp(↑) width DL (↓)

material se bhi farak pdta hai

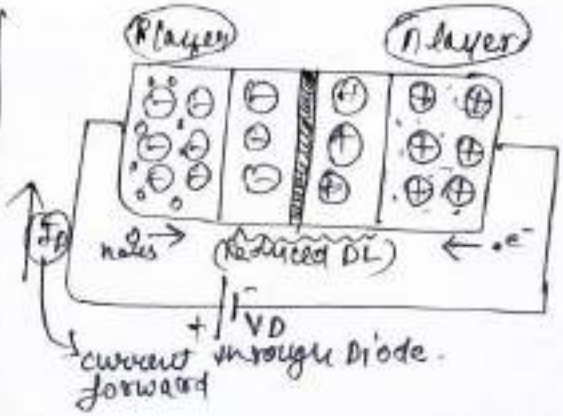
(Biasing of P-N junction Diode)

Applying the battery accross P-N junction is known as biasing.
It can be Biased in 2 ways:
- → Forward B (ON) (—▷|— , + −)
- → Reverse B (OFF) (— −|▷ —, − +)

(Forward Biasing) # → ($V_D > 0$)

In forward Biased condition the terminal of battery is connected P side and -ve terminal to the n-side.

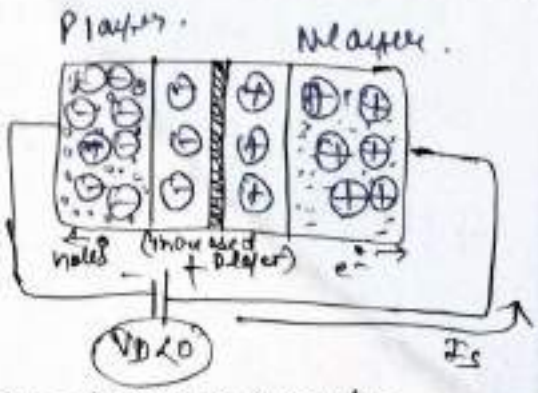
holes are repelled from +ve end and forced towards junction. same w/ the e^- also. This reduces barrier potential & DL also.



The reduction in the width of DL results in a heavy majority flow accross the junction.

(Reverse Biasing)

- Here +ve terminal is connected to n layer & -ve terminal to P layer. In P region holes are attracted towards negative terminal of battery where e^- are attracted towards the terminal of the battery.



I_S = Reverse saturation current

- Thus depletion layer increases in width. [Exam 01/Dec/2022.]

- A very small current flows due to minority charge carriers. The current that exist under R/w Bias condⁿ is called I_S. (R/w saturation current).

- The term "Saturation" comes from the fact that it reaches its max level very quickly and not change significantly with r/w bias potential.

[Diode Current Equation] # [02/Dec/2022]

(Schokley's Eqⁿ)

$$I_D = I_S\left(e^{\frac{V_D}{\eta V_T}} - 1\right)$$

I_D → Diode current

I_S → Reverse saturation current (fixed)

R/w → -ve
F/w → +ve

V_D = Potential apply
V_T = Thermal voltage.

Room temp = 27°C or 300 K

η = constant ⇒ 1 → Ge, 2 → Si

Thermal voltage $= \frac{kT}{q}$ or $\frac{T}{11600}$ — simplified one.

k = Boltzman Constant ⇒ 1.38×10^{-23} J/K.
T = Temperature (Kelvin)
q = e^- charge.

At room temp

V_T = 26 m volts
$= 26 \times 10^{-3}$ volts

Q:- Reverse saturation current at room temp (V_T = 26 m Volts.) is 0.3 μAmp (I_S). When reverse bias is applied to a germanium diode ($\eta = 1$) find value of current flowing in diode when 0.15 Volts (V_D) forward bias is applied?

Ans:

$$\cancel{I_D = I_S\left(e^{\frac{V_D}{\eta V_T}} - 1\right)}$$

$$\cancel{I_D = 0.3\left(e^{\frac{0.15V}{1 \times 26 \times 10^{-3}}} - 1\right)}$$

Ans: $I_D = I_S\left(e^{\frac{V_D}{nV_T}} - 1\right)$

$= 0.3\times10^{-6}\left[e^{\frac{0.15}{1\times26\times10^{-3}}} - 1\right]$

$= 0.3\times10^{-6}\left[e^{\frac{150}{26}} - 1\right]$

$= \boxed{94\times10^{-6} \text{ micro Amp}}$ Ans

Q2: forward current through a Silicon diode is 10mA ($n=2$, I_D) at room temp the corresponding f/w voltage is ($V_T = 26mV$) ($V_D = 0.75V$)

Calculate I_S ?

Ans: $I_D = I_S\left(e^{\frac{V_D}{nV_T}} - 1\right)$

$10mA = I_S\left(e^{\frac{0.75V}{2\times26}} - 1\right)$

$I_S = 5.44\times10^{-9}$ Amperes

Nano.

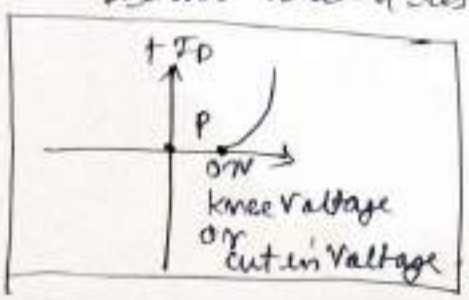
{ VI Characteristics of P-N Junction Diodes }

VI characteristics of a diode is simply a curve or graph b/w applied potential & resultant current. It can be divided into 2 parts:-

① Forward curve :- A/c to Schokley's eqn :-

$\boxed{I_D = I_S\left(e^{\frac{V_D}{nV_T}} - 1\right)}$ — ① $\boxed{I_D = \underbrace{I_S e^{\frac{V_D}{nV_T}}}_{①} - \underbrace{I_S}_{②}}$ — ②

for the values of V_D the 1st term of the above eqn will grow very quickly & totally overpower the effect of 2nd term which results in :-



$\boxed{I_D \cong I_S e^{\frac{V_D}{nV_T}}}$ — ③

$V_K = \begin{cases} 0.7 \text{ volt (Si)} \\ 0.3 \text{ volt (Ge)} \end{cases}$

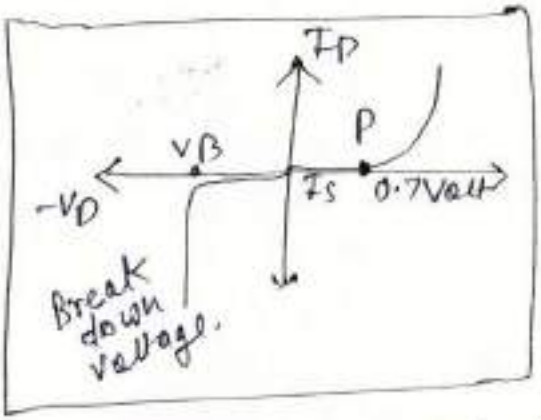
from the graph it's clear that upto point 'P' the diode current is zero. this is so because the applied voltage has to over come the barrier potential after that diode current increases rapidly.

The Voltage at which (I) starts increasing is known as **knee Volt (Vk)**

(2) **Reverse Curve** :- A/c to schokley's eqn.

$$I_D = I_S\left(e^{\frac{V_D}{nV_T}} - 1\right) \quad -(1) \qquad I_D = I_S e^{\frac{V_D}{nV_T}} - I_S \quad -(2)$$

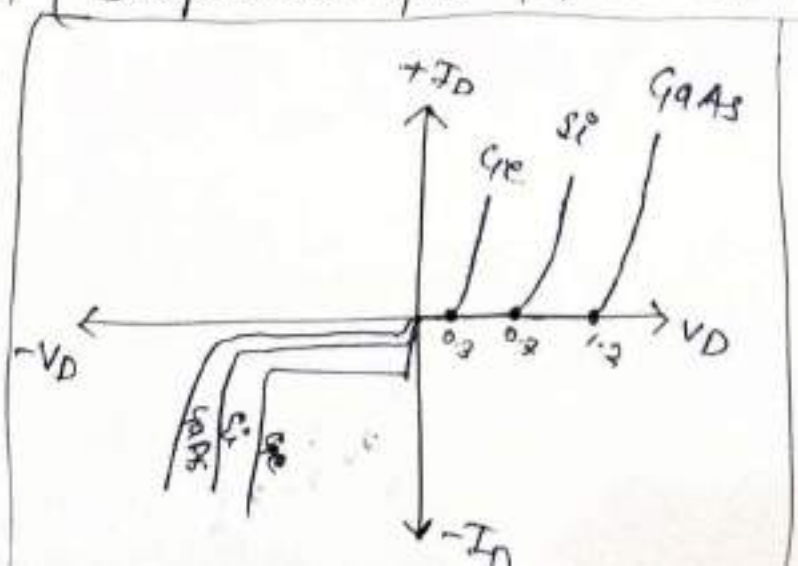
for -ve values of V_D the exponential term drops very quickly which results in. $I_D \simeq -I_S$ -(3)



Below the Breakdown (V_B) the diode current is very small & almost remains constant which is known as reverse saturation current (I_S)

* its due to movement of minority charge carriers.
* The R/w bias voltage at which junction breakdown occurs is known as breakdown voltage.

{Comparision b/w Ge, Si & GaAs diodes}



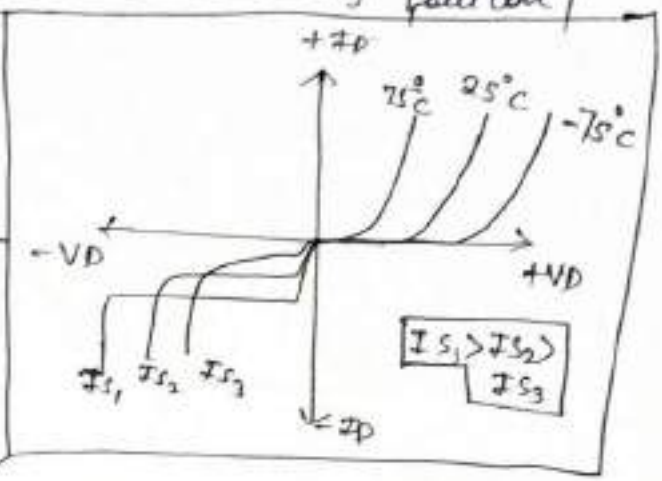
$I_S(GaAs) > I_S(Si) > I_S(Ge)$

02 Dec 2022

{ Temperature effects on VI curves } : Silicon

forward curve :- In f/w bias region the curve shifts to the left at a rate of 2.5 mV/per C°.

Reverse Curve :- In R/w bias region the R/w saturation current doubles for every 10°C rise in temperature.



Q:-1 At 20°C temperature a silicon diode contains 2 micro Ampere Reverse saturation Current. what will be the value of R/w Saturation (I) at 80°C?

Ans:- 128 micro Amperes

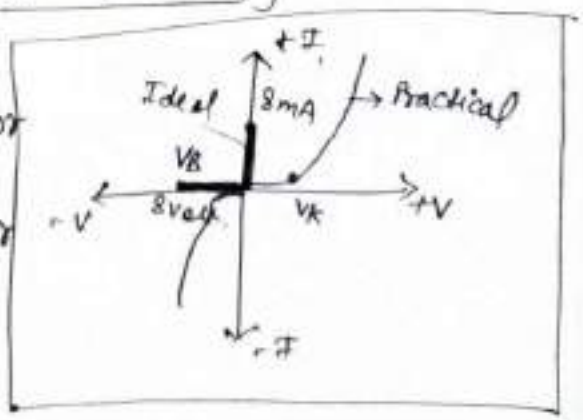
20 — 2¹	60 — 2⁵
30 — 2²	70 — 2⁶
40 — 2³	80 — 2⁷
50 — 2⁴	

(PIV) (P-Inverse Voltage) :-

its the maximum reverse voltage that can be applied to the P-N junction without damage to the junction.

06/Dec/2022 # { Ideal V/s Practical Diode } #

A diode would be ideal if a diode acts as a perfect conductor when forward biased (short Circuit) and as a perfect insulator (open circuit) when R/w Biased



6Dec/2022 Tuesday

ideal diode :- forward curve :

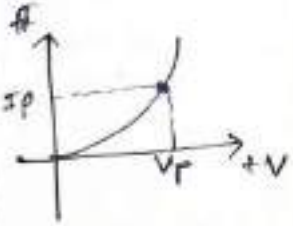
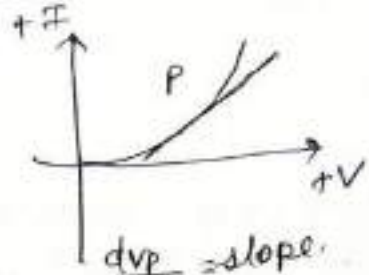
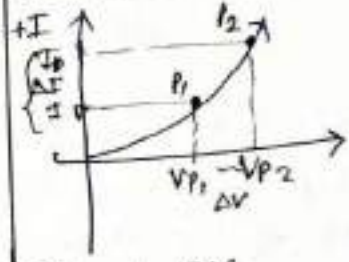
$$R_f = \frac{V_D}{I_D} = \frac{0}{3mA} = 0\,\Omega \text{ (short circuit)}$$

* Reverse curve

$$R_R = \frac{V_R}{I_R} = \frac{-8}{0} = \infty\,\Omega \text{ (open circuit)}$$

(Diode resistances)

* There are 3 types of diode resistance :-

	① DC/Static	② AC/Dynamic	③ Average
Types	DC Static Resistance	AC/Dynamic Resistance	Average resistance.
eqn.	$R_S = \frac{V_D}{I_D}$	$R_d = \frac{dV_D}{dI_D} = \frac{nV_T}{I_S e^{\frac{V_D}{nV_T}}}$	$R_{avg} = \frac{\Delta V_{D}}{\Delta I_D}$ / Point to Point.
char acter stics	defined as a point on curve.	defined by tangent on point.	defined by an straight line b/w 2 points.
graph	 $R_D = \frac{V_D}{I_D}\,\Omega$	 $\frac{dV_D}{dI_D}$ = slope.	 $R_{avg} = \frac{\Delta V}{\Delta I}$

(Derivation of R_D) # Shockley's eqn used

$$I_D = I_S\left(e^{\frac{V_D}{nV_T}} - 1\right)$$

$$I_D = I_S\,\frac{V_D}{nV_T} - I_S$$

diffn wrt V_D

$$\frac{dI_D}{dV_D} = \frac{I_S\, e^{\frac{V_D}{nV_T}}}{nV_T}$$

$$r_d = \frac{dV_D}{dI_D} = \frac{nV_T}{I_S e^{\frac{V_D}{nV_T}}}$$

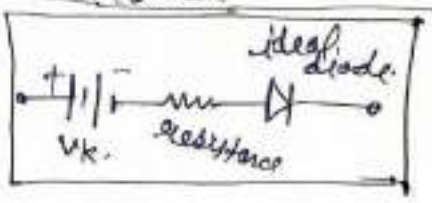
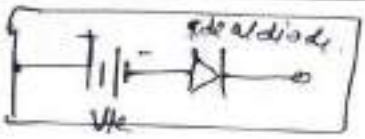
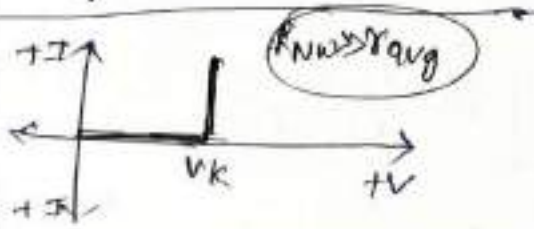
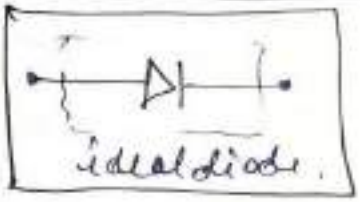
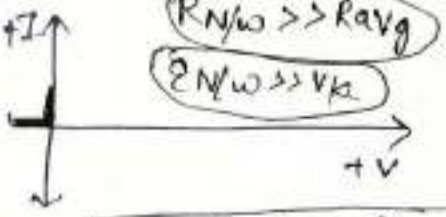
$$\boxed{r_d = \frac{nV_T}{I_D + I_S}}$$

06/Dec/2022 (electronics)

(Diode Equivalent Circuits)

An equivalent circuit is a combination of elements that represent actual terminal characteristics of a device

This table will come in short note.

Types	Model	characteristics
① Piecewise linear eqn circuit.		
② Simplified equivalent circuit -		
③ ideal diode equivalent circuit.		

avg = average R
N/w = network
R = resistance
Vk = knee Volts.
EN/w = source +|-

Abbreviations

Q:- Calculate AC resistance for a Ge ($\eta = 1$) semi conductor diode having f/w bias of 200 mV (V_D) & reverse saturation current of 1 μAmp (I_s) at room temp. ($V_T = 26$ mV)?

Ans:- $I_d = I_s\left[e^{\frac{V_D}{\eta V_T}} - 1\right]$

$I_d = 1\,\mu Amp\left[e^{\frac{200mV}{1 \times 26mV}}\right]$

$I_d = \frac{200}{2.19} = \underline{91.32\ \Omega}$

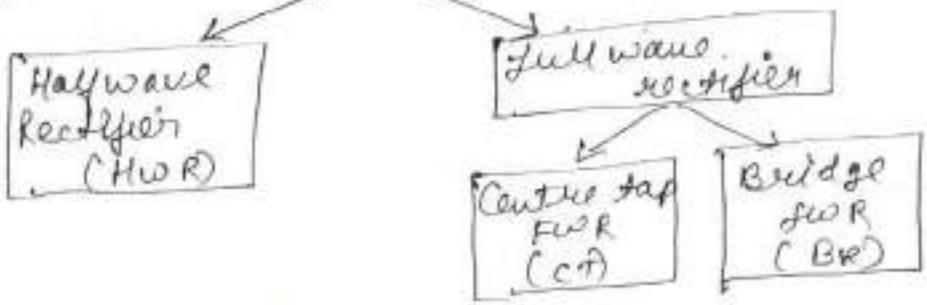
electronics 7/Dec/2022

(Diode Rectifiers)

① As a rectifier
② As a clipper
③ As a clamper
④ zener diode is a shunt regulator

#(Diode as a rectifier)#

- A rectifier is a circuit which is used to convert AC to Pulsating DC. There are 2 types of rectifiers

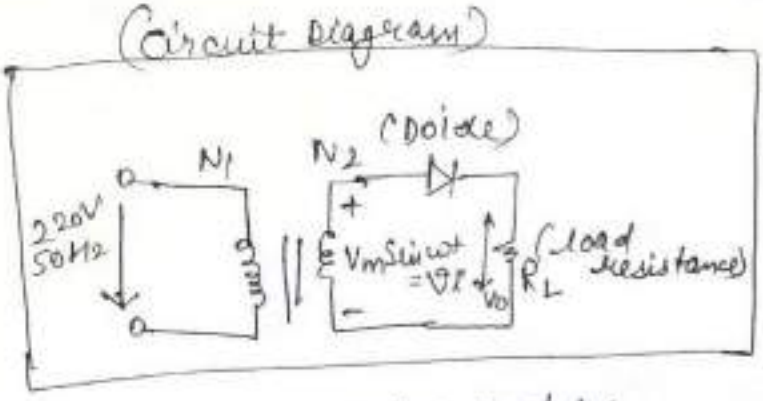


Halfwave Rectifier (HWR):-

The process of removing 1 half of the input signal to establish a (DC) level is called as HWRectification.

* Circuit Diagram *

(Circuit Diagram)



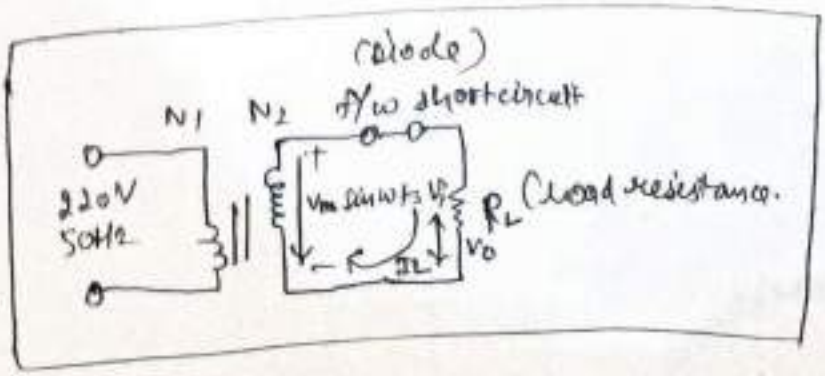
Working

- There is a transformer at the input of the circuit which provides 2 purpose for.

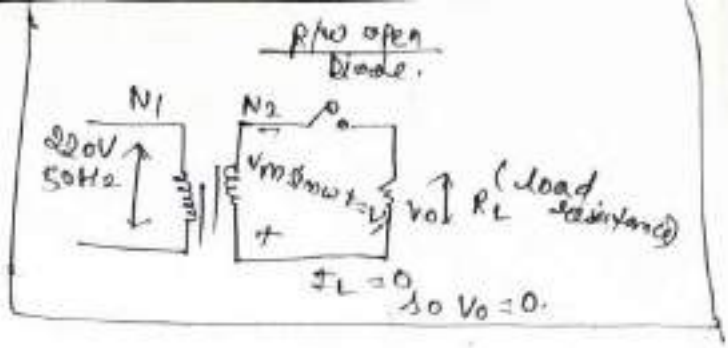
1) step up & step down.
2) Isolation

- primary winding is connected to the power mains and AC voltage is induced across the 2nd winding which is given by $V_I = V_m \sin\omega t$. here V_m = peak voltage.

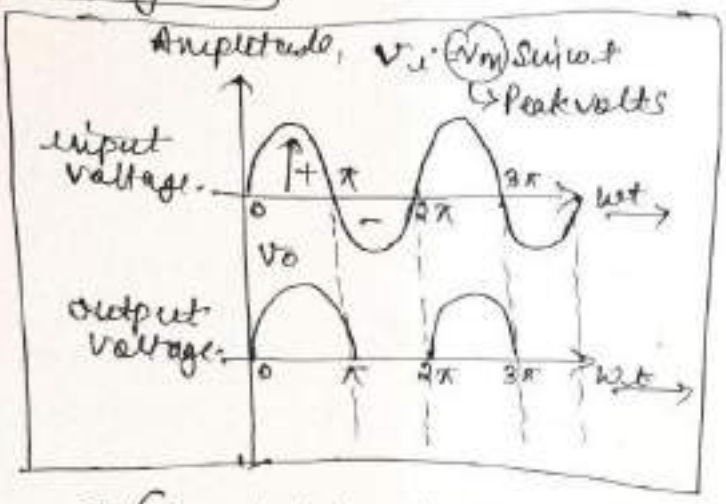
- during the half cycle of input voltage the diode is forward biased so short circuit & conducts. Current I_L flows through resistor R_L.



* During the half cycle of V_{inp} diode is reversed biased so open circuit thus it will not conduct and o/p voltage across R_L will be zero



* Waveforms :-

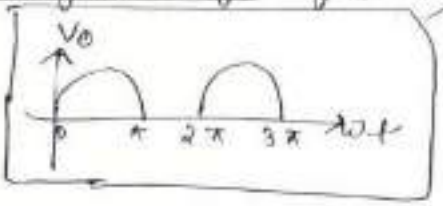


$$\boxed{P/V_{HWR} = V_m}$$

Peak inverse voltage from half wave rectifier = V_m.

(Calculation for DC voltage or Average Voltage of HWR)

$$V_o = \begin{cases} V_m \sin\omega t & 0 \le \omega \le \pi \\ 0 & \pi < \omega \le 2\pi \end{cases}$$



Base → 0 to 2π = 2π

Area :-

$$\int_0^{\pi} (V_m \sin\omega t)\, d\omega t + \int_{\pi}^{2\pi} 0 \cdot d(\omega t)$$

$$V_m [-\cos\omega t]_0^{\pi} + 0$$

$$V_m [-\cos\pi - (-\cos 0)]$$

$$V_m [-(-1) - (-1)] = 2V_m$$

$I_L = 0$ $\quad V_{dc} = \dfrac{\text{Area}}{\text{Base}}$ $\quad$ learn it

so $V_o = 0$ = $\boxed{V_{dc\,HWR} = \dfrac{2V_m}{2\pi} = \dfrac{V_m}{\pi}}$

Similarly average or DC current for HWR is given by.

$$\boxed{I_{dc\,(HWR)} = I_{avg} = \frac{I_m}{\pi}}$$

Note :- If diode has internal dynamic resistance (r_d) in that case $\boxed{V_{dc} = \dfrac{V_m}{\pi(1 + \frac{r_d}{R_L})}}$

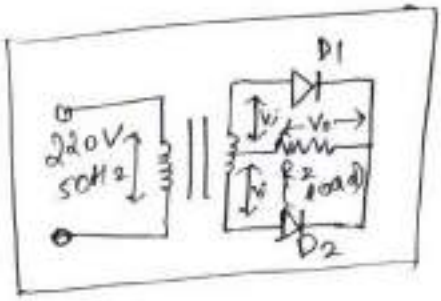
electronics 08/Dec/2022

(Full Wave Rectifier)

Its a type of rectifier which utilises both the half cycle of AC input voltage. Those are of 2 types:-

① Centre tap FWR

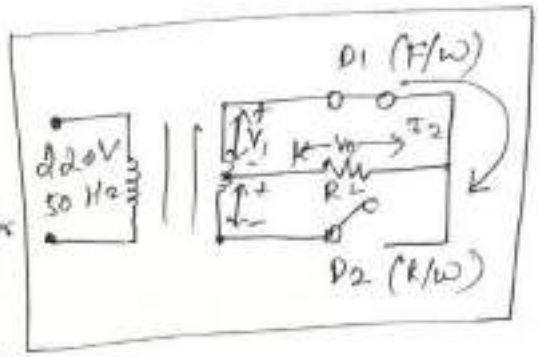
• It uses two diodes D_1 & D_2 which are connected to centre tap winding of the transformer.



(Working Principle)

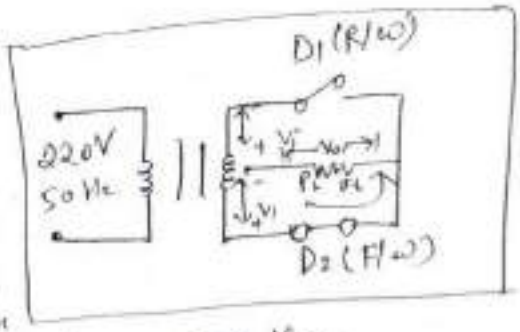
•) During the half:-

During the half cycle of input voltage diode D_2 is forward bias so, short circuit & conducts & the diode D_2 is reverse biased so open circuit & not conducts. A current I_L flows through the load resistor R_L producing an O/P voltage V_o.

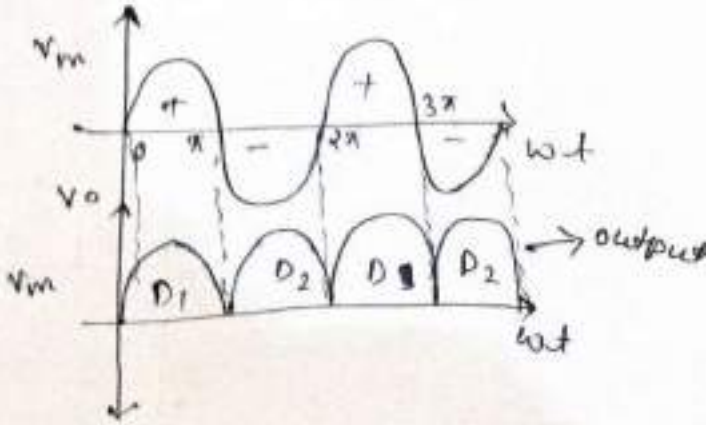


•) During the half cycle

During the half cycle of input voltage diode D_1 is reverse biased so open circuit and diode D_2 forward biased so short circuit. Thus a current I_L flows through the load resistor R_L producing O/P voltage V_o.

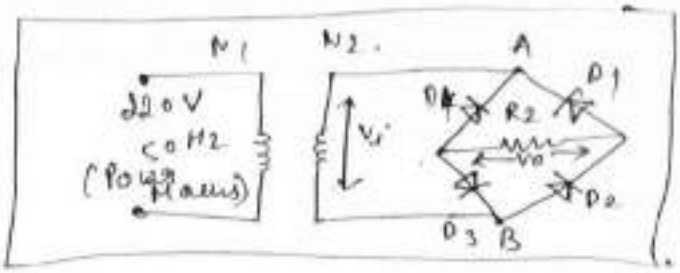


Peak voltage input of (CTFWR) = 2Vm.



② Bridge Rectifier

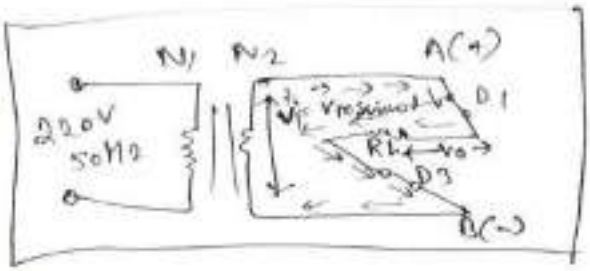
- it uses four diodes which are connected across the secondary winding of the transformer.



Working Principle :-

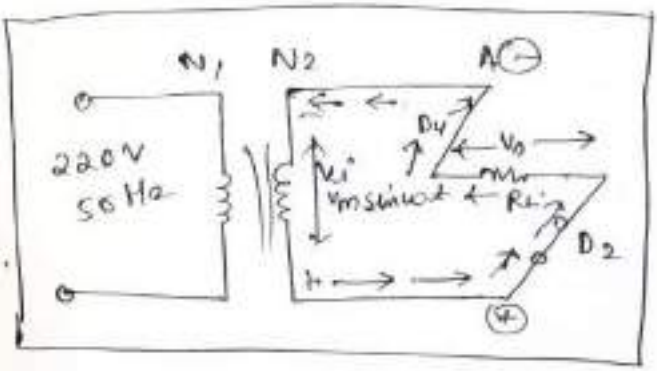
•) During the +ve half

During +ve half cycle diode D_1 & D_3 are forward biased, so they conducts. Therefore the output V_o developed across the load.

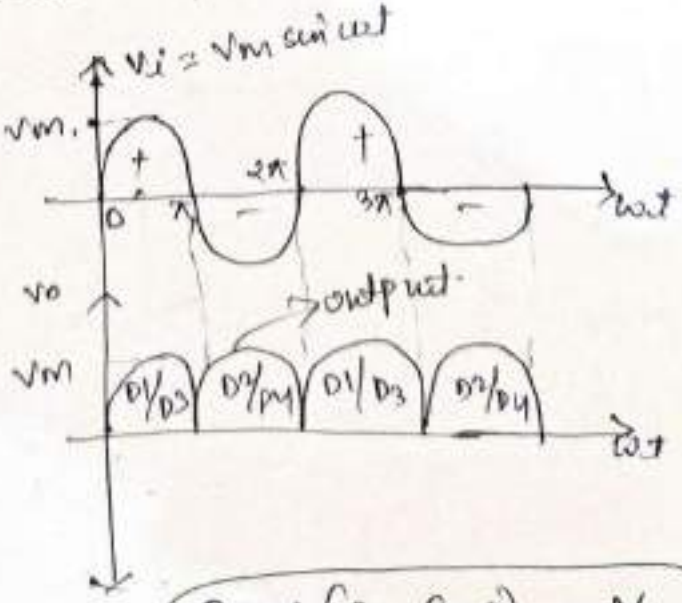


•) During -ve half

During -ve half cycle diode D_2 & D_4 are forward biased so they conducts and produces output across load resistor (R_L).



Waveforms



PIV (B.fwR) = V_m

(Advantage of Bridge Rectifier over Centre tap rectifiers)

- Bridge rectifiers does not require centre tap secondary winding.
- Each diode in (CTR) must have a (PIV) rating of 2Vm hence they are costly.

(Disadvantage of Bridge rectifier) # 09/Dec/2022

- It requires four diode.

$$V_o = \begin{cases} V_m \sin\omega t & 0 \le \omega t \le \pi \\ -V_m \sin\omega t & \pi \le \omega t \le 2\pi \end{cases}$$

$$V_{dc} = \frac{\text{Area}}{\text{Base}} = \int_0^{2\pi} V_o \cdot d(\omega t)$$

$$\text{Area} = \int_0^{\pi} V_m \sin\omega t \, d\omega t - \int_{\pi}^{2\pi} V_m \sin\omega t \, d\omega t.$$

$$= V_m[-\cos\omega t]_0^{\pi} - V_m[-\cos\omega t]_{\pi}^{2\pi}$$

$$= V_m[1+1] + [1+]$$

$$= \boxed{4V_m}$$

$$V_{dc} = \frac{\text{Area}}{\text{Base}} = \frac{4V_m}{2\pi} = \frac{2V_m}{\pi}$$

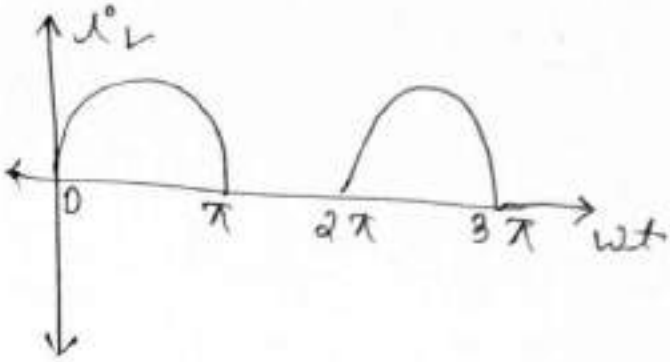
$$V_{dc}\,(FWR) = 0.636\,V_m.$$

$$\boxed{I_{dc}\,(FWR) = \frac{2I_m}{\pi}}$$

Ripple factor :- We can say that a unidirectional fluctuating waveforms has an average or DC value over which AC components of different frequencies are super imposed. These undesired AC components are called Ripple

#1 Ripple factor for HWR

$$i_L = \begin{cases} I_m \sin\omega t & 0 \le \omega t \le \pi \\ 0 & \pi < \omega t \le 2\pi \end{cases}$$



$$I_{rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_L^2 \, d(\omega t)}$$

$$I_{rms\,(HWR)} = \sqrt{\frac{1}{2\pi}\left[\int_0^{\pi} I_m^2 \sin^2\omega t \, d(\omega t) + \int_{\pi}^{2\pi} 0 \cdot d(\omega t)\right]}$$

$$I_{rms\,(HWR)} = \sqrt{\frac{1}{2\pi} I_m^2 \left[\int_0^{\pi}\left(1 - \frac{\cos 2\omega t}{2}\right) d(\omega t) + 0\right]}$$

$$= \sqrt{\frac{I_m^2}{4\pi}\left[(\omega t)_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)\right]_0^{\pi}}$$

$$= \sqrt{\frac{I_m^2}{4\pi}\left[\pi - \left(\sin 2\frac{\pi}{2} - \sin 0\right)\right]}$$

$$= \sqrt{\frac{I^2}{4\pi}\left[\pi - (0 - 0)\right]}$$

$$= \sqrt{\frac{I^2_m}{4\cancel{\pi}}\cancel{\pi}}$$

for HWR $\quad I_{dc} = \frac{I_m}{\pi}$

$$r_{(HWR)} = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1}$$

$$r_{(HWR)} = 1.21$$

Note:- Thus we can see that the ripple current exceeds the DC current this shows that half wave rectifier is a poor converter of AC to DC.

* Ripple factor is a measure of purity of DC o/p of a rectifier & its given by :-

$$r = \frac{\text{Rms value of AC components of o/p voltage}}{\text{dc component of o/p voltage}}$$

$$r = \frac{V_{ac}(rms)}{V_{dc}} = \frac{I_{ac}(rms)}{I_{dc}}$$

As we know rms value of total value is given by.

$$I_{rms} = \sqrt{(I_{dc})^2 + (I_{dc})^2_{rms}}$$

$$I^2_{rms} = I_{dc}^2 + I_{ac}^2 (rms)$$

$$\boxed{\text{Divided by } I^2_{dc}}$$

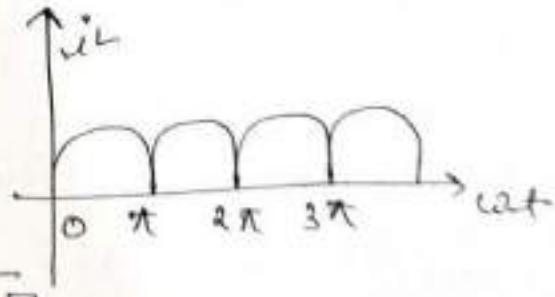
$$\left(\frac{I_{rms}}{I_{dc}}\right)^2 = 1 + \left(\frac{I_{ac}(rms)}{I_{dc}}\right)^2$$

$$\left(\frac{I_{ac}(rms)}{I_{dc}}\right)^2 = r^2 = \left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1$$

$$r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

(Ripple factor for full wave rectifier)

$$i_L = \{I_m \sin\omega t \quad 0 \le \omega t \le \pi\}$$



$$I_{rms}\ (FWR) = \sqrt{\frac{1}{\pi}\int_0^{\pi} i_L^2 \, d(\omega t)}$$

$$I_{rms}\ (FWR) = \sqrt{\frac{1}{\pi}\left[\int_0^{\pi} I_m^2 \sin^2\omega t \, d(\omega t)\right]}$$

$$I_{rms}\ (FWR) = \sqrt{\frac{1}{\pi} \cdot I_m^2 \left[\int_0^{\pi} \left(1 - \frac{\cos 2\omega t}{2}\right) d(\omega t)\right]}$$

$$= \sqrt{\frac{I_m^2}{2\pi}\left[(\omega t)_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]}$$

09/Dec/2022

$$= \sqrt{\frac{I_m^2}{2\pi}\left[\pi - 0 - \left(\frac{\sin 2\pi}{2} - \frac{\sin 0}{2}\right)\right]}$$

$$= \sqrt{\frac{I_m^2}{2\pi} \times \pi}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$
(FWR)

$$I_{dc} = \frac{2 I_m}{\pi}$$
(FWR)

$$r = \sqrt{\left(\frac{I_m/\sqrt{2}}{2 I_m/\pi}\right)^2 - 1}$$

$$r_{(FWR)} = 0.482$$

∴ This is a good converter of AC into DC

Rectification efficiency (η)

It tells us what percentage of total input AC power is converted into useful DC output power.

It's defined.

$$\boxed{\eta = \frac{\text{dc Power delivered to load}}{\text{AC power from secondary winding}}}$$

$$\boxed{\eta = \frac{P_{dc}}{P_{ac}}}$$

12/Dec/2022

* rectification efficiency for (FWR)

$$P_{dc} = I_{dc}^2 \cdot R_L$$

$$P_{ac} = I_{rms}^2 (r_d + R_L)$$

diode resistance

load resistance

$$= \left(\frac{I_m^2}{2}\right)(r_d + r_L)$$

$$\eta_{FWR} = \frac{40.6}{1 + \frac{r_d}{r_L}} \%$$

electronics 12/Dec/2022

* rectification efficiency for FWR.

$$P_{dc} = I_{dc}^2 * R_L$$
$$= \left(\frac{2I_m}{\pi}\right)^2 * R_L$$

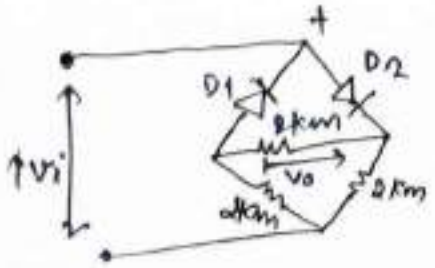
$$P_{ac} = I_{rms}^2 * (r_d + r_L)$$
$$= \left(I_m/\sqrt{2}\right)^2 * (r_d + r_L)$$

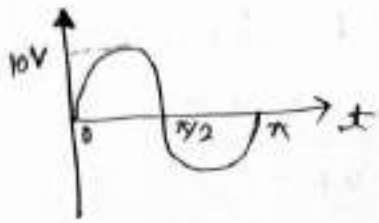
$$\eta_{FWR} = \frac{81.2}{1 + \frac{r_d}{r_L}} \%$$

(comparision b/w rectifiers)

Parameters.	HWR.	FWR. CT	Bridge.
No of diodes	1	2	4
η	1.21	0.482	0.482
I_{dc}	I_m/π	$2I_m/\pi$	$2I_m/\pi$
I_{rms}	$I_m/2$	$I_m/\sqrt{2}$	$I_m/\sqrt{2}$.
Peak Voltage.	V_m	V_m	V_m.
PIV	V_m	$2V_m$	V_m.
η	$\frac{40.6}{1+\frac{r_d}{r_L}}$		$\frac{81.2}{1+\frac{r_d}{r_L}}$.

Q. for given circuit draw o/p waveform and also calculate output DC level and PIV reqd for each diode?





12/Dec/2022

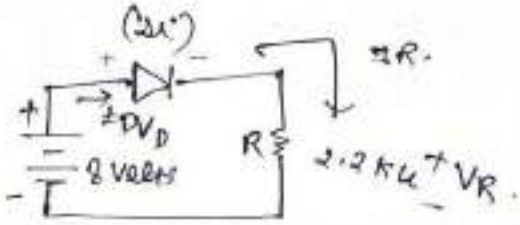
$I = \frac{10}{2k + 2k}$ $\quad V_o = 2k * I = 5$ volts

$V_{dc} = \frac{2V_m}{\pi} = \frac{2 \times 5}{\pi} = 3.18$ volt

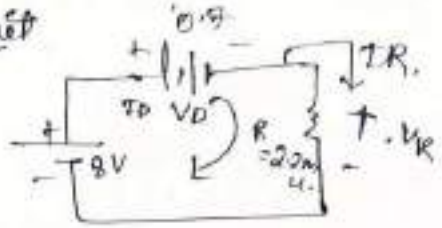
$\boxed{PIV = V_m = 5 \text{ volt}}$

(Diode series Configuration)

$\boxed{V_D, \; V_R, \; I_D}$



∴ Equivalent circuit when diode is on condition..



$V_D = 0.7$ Volt

$+E - 0.7 - V_R = 0$

$8 - 0.7 - V_R = 0$

$V_R = 7.3$ volt

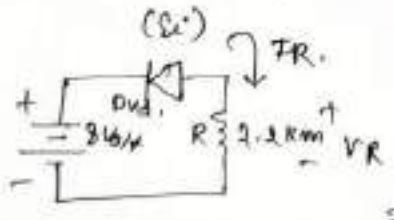
$I_D = I_R$

$I_R = \frac{V_R}{R} = \frac{7.3}{2.2 \times 10^3} = 3.32 \times 10^{-3}$ Amp

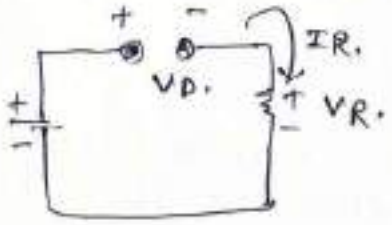
Ans.

$\boxed{\text{Reverse Diode} = \text{off diode}}$

Q2:-



=



$V_D = 8$ volt.

$I_D = 0$ Amp. $= I_R$.

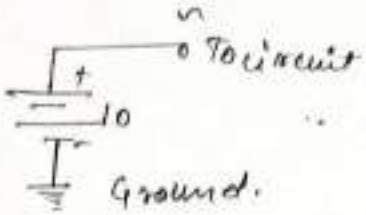
$V_R = R * I_R$

$V_R = 0$

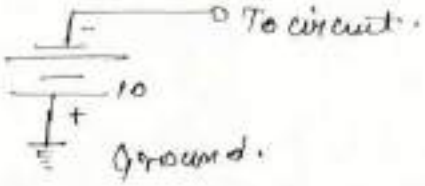
Electronics (13/Dec/2022)

Source notations

- +10 volt

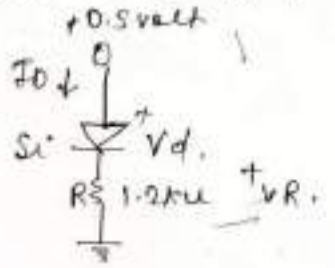


- -10 volt



Q:- Calculate V_D, V_R, I_D.

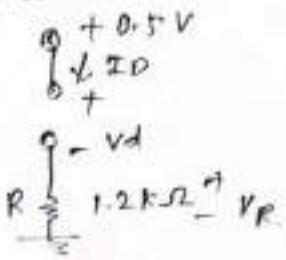
Ans:



Potential kam hai 0.7 se isliye diode off hai.

* Applied volt is insufficient to turn the diode ON, so diode is off

Resulting circuit



$V_D = 0.5$ volt.

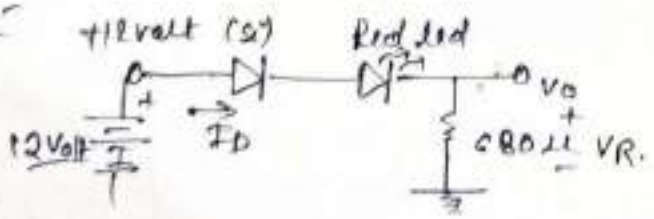
$I_D = 0$

$V_{R_1} = I_R * R$

$= I_D * R$

$\boxed{V_R = 0}$

Q:-



$V_0 = ?$

$I_D = ?$

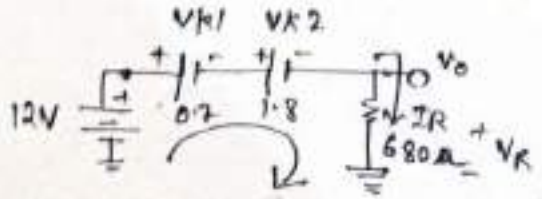
given =

$V_{K_1} = 0.7$ volt.

$V_{K_2} = 1.8$ Volt.

Applied Potential = 12V

Ans



KVL = Kirchoff voltage law.

Applying KVL.

$+12 - V_{K_1} - V_{K_2} - V_0 = 0$

$V_0 = 12 - 0.7 - 1.8$

$= 9.5$ Volts.

electronics 13/Dec/2022

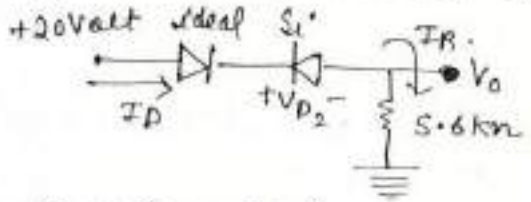
$$12 - 0.7 - 1.8 + I_R = 0$$
$$12 - 2.5 + I_R = 0$$
$$9.5 + I_R = 0$$
$$I_R = 9.5 \text{ Volts}$$

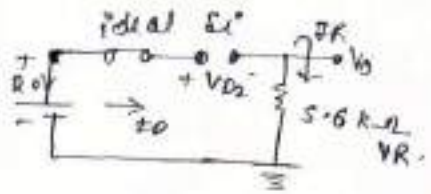
I_D = current in Diode.
I_R = same current in Resistance.
open circuit = $I = 0$
Potential hoskta hai.

$I_D = I_R$

$$I_R = \frac{V_R}{R} = \frac{V_R}{R} = \frac{9.5}{680} = \boxed{13.97 \text{ mAmp}} \text{ Ans}$$

Q:- for given circuit calculate I_D, V_{D2}, V_0 ?





Ans = $I_D = 0$ (open ckt)

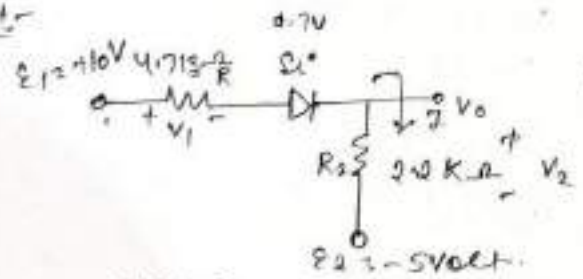
$I_R = \frac{V_R}{R}$

$V_{D_2} = 20$ volt

Here $V_0 = V_R = I_R * R$
$= 0 * R$.

$\boxed{V_0 = 0}$

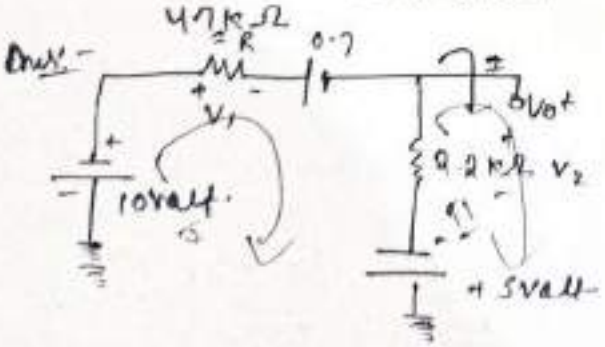
(VVIMP)
Q:-



Q. Calculate I, V_1, V_2, V_0 ?

Same ground nhi hai isliye.
$\boxed{V_2 \neq V_0}$

Ans:-



~~$I = 2.21$ mAmp.~~
~~$V_1 = 4.7 \times 2.21$~~
~~$= 9.462$~~
~~$V_2 = 2.21 \times 2.2$~~
~~$= 4.862$~~

$$\begin{array}{r} 2.21 \\ \times 2.2 \\ \hline 442 \\ 42 \\ \hline 4.862 \end{array}$$

$$I = \frac{10 - 0.7 + 5}{4.7k\Omega + 2.2k\Omega} \quad \left(\frac{V_{eq}}{R_{equivalent}}\right) = I = 2.07 \text{ mAmp}$$

Electronics 13/Dec/2022

$V_1 = I \times R$ $\quad$ $V_2 = I \times R$

$V_1 = 2.07 \times 4.7$ $\quad$ $V_2 = 2.07 \times 2.2$

$= 9.729$ Volt $\quad$ $= 4.554$ Volt

$V_0 = ?$ Apply KVL in II loop.

$-E_2 + V_2 - V_0 = 0$

$V_0 = V_2 - E_2$

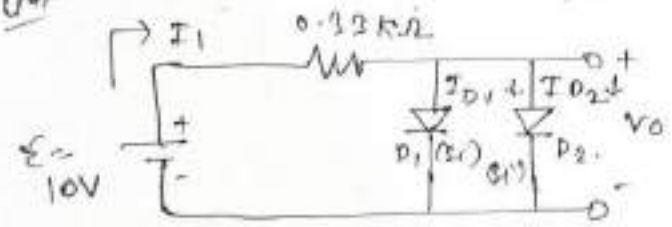
$= 4.55 - 5$

$\Rightarrow -\boxed{0.45 \text{ volt}}$

(Parallel & Series diode configurations)

14/Dec/2022

Q#



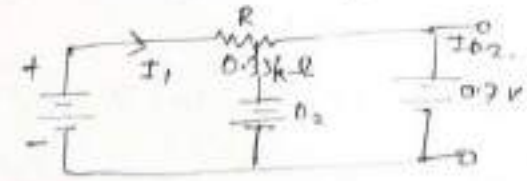
$I_{D_1} = I_{D_2}$

$V_0 = 0.7V$

Ans:- $V_0 = 0.7V$

$I_L = \frac{E - V_0}{R} = \frac{10 - 0.7}{0.33 \times 10^3} = \boxed{28.18 \text{ mA}}$

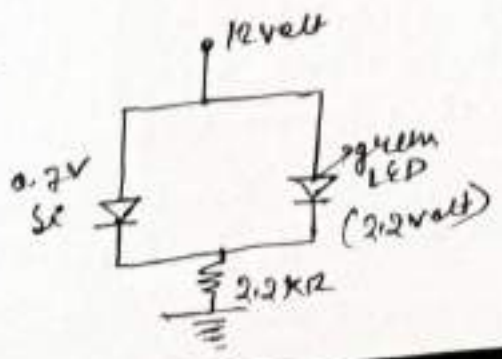
$I_{D_1} = I_{D_2} = \frac{I_1}{2} = \frac{28.18}{2} = 14.09$ mA



(Parallel & series configuration) (15/Dec/2022)

calculate V_0?

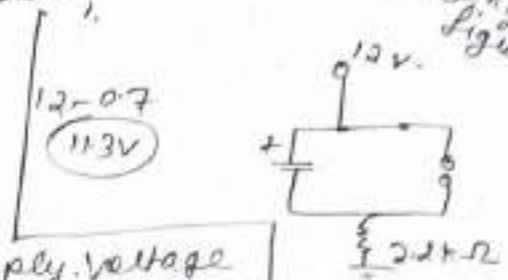
Q1



15/Dec/2022.

Calculate V_o for the given circuit?

Resulting figure



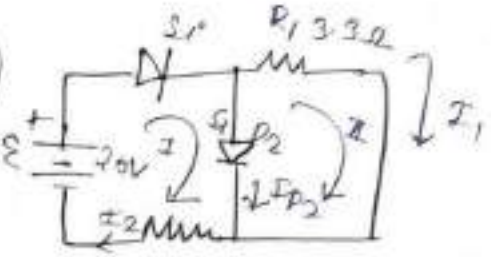
Ans:- As we know the voltage must be same accross parallel elements. There is a period of built up of the supply voltage from zero to 12 volt when supply voltage from 0 to 12 when supply volt reaches 0.7V Si diode turns on maintains the level of 0.7 volt the result is that the voltage across green led will never rise above 0.7V & will remain in open circuit.

Q2:- Calculate I_1, I_2, I_{D_2}?

Ans:- $I_1 = \frac{0.7}{R_1} = \frac{0.7}{3.3\times10^3} = 0.212$ mAmp

$20V - 0.7 - 0.7 - I_2 \times 5.6\times10^3 = 0$

$I_2 = 3.3mA$



KVL In Loop I

$I_2 = \frac{\varepsilon - 0.7 - 0.7}{R_2} = \frac{20-1.4}{5.6\times10^3} = 3.3$ mAmp

KCL at Point A

$I_2 = I_{D_2} + I_1$

$I_{D_2} = I_2 - I_1 =$ 3.1 mAmp

#(Breakdown Mechanism)#

There are 2 types of Breakdowns.

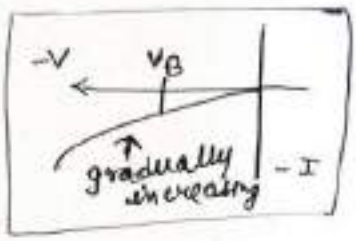
Avalanche Breakdown	Zener Breakdown
• In case of this Breakdown the increased electric field increase the velocity of minority charge carriers.	• where reverse bias increases the electric field at the junction also increases high (E) causes covalent bonds to break.
• These high energy carriers break covalent bond. thereby generating more carriers.	• Thus a large number of carriers are generated causing a brg.

15/Dec/2022.

Avalanche Breakdown

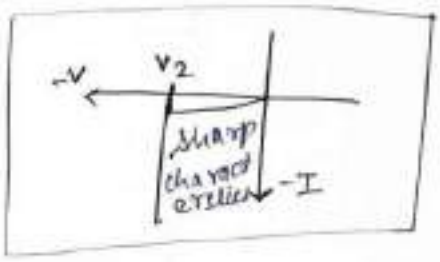
Thus a change in reaction is established.

- creating a large no of carriers this BD is called Avalanche BD.



Zener breakdown

current to flow. Thus this is called as zener breakdown.

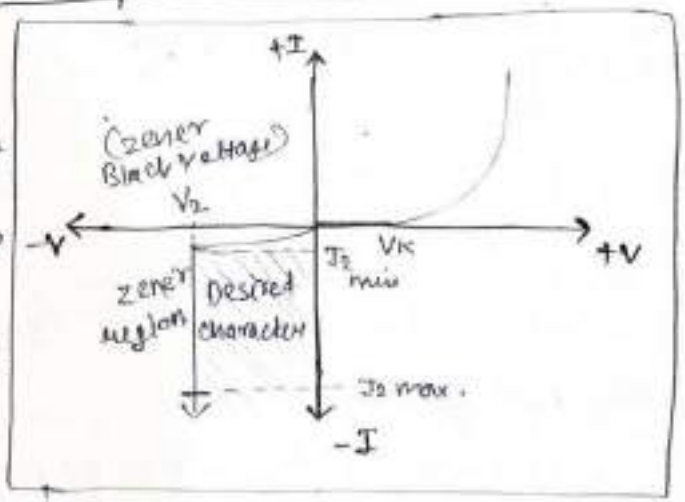


(Zener Diode)

its a reverse biased heavily doped P-N junction Diode which operates in zener Breakdown region.

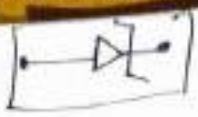
(VI curve of zener Diode)

- forward curve is almost identical to forward characteristics of ordinary P-N junction diode
- Reverse curve as we increase reverse voltage initially a small reverse saturating current will flow due to minority charge carriers.



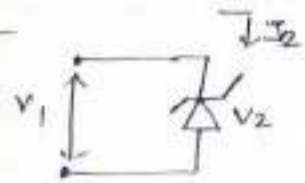
- At a certain value of R/r voltage reverse current will increase sharply this voltage is known as zener BD voltage (V_Z)
- After BD the voltage across zener diode remains constant (V_Z) any increase in the source voltage will result in increasing reverse zener current.

(Symbol of zener diode)

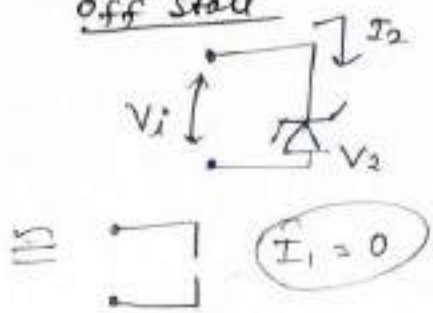


ON state

$V_i \geq V_2$



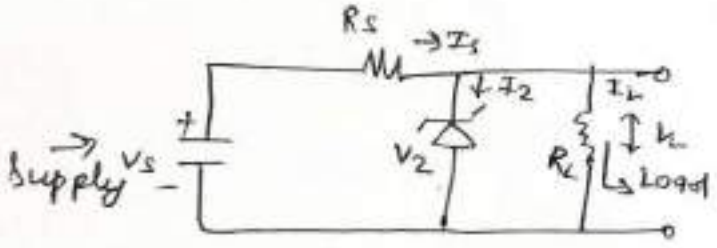
Off state



(Application of zener diode)

- Voltage regulator.
- Meter protection usage.
- As a clipper
- As a fixed reference Voltage.

(Zener diode as a shunt regulator:-) # 16/Dec/2022



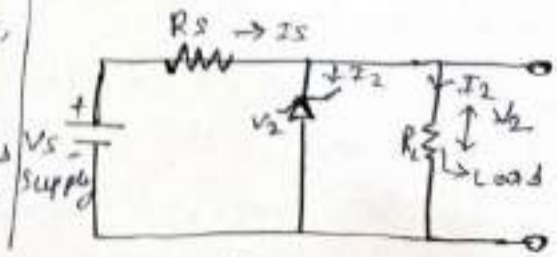
$I_S = I_2 + I_L$

$V_L = I_L * R_L$

This circuit is called as shunt regulator because zener diode is connected parallel with load. The resistance R_S is then connected to limit the current in the circuit. The regulated Voltage is obtained across the load resistance (R_L).

Working Principle:-

Case1:- when supply voltage is variable:-



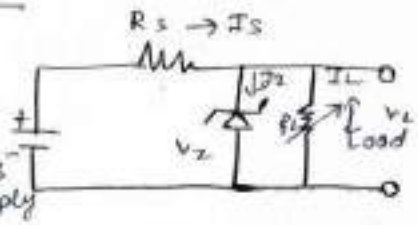
when we increase supply voltage, supply current also increases hence to maintain the current eq^n ($I_S = I_2 + I_L$). Zener increases its current similarly, when we decrease supply voltage (V_S) supply current (I_S) also decreased. But (I_L) is constant hence to maintain the current eq^n. zener decreases its current.

$V_L = I_L * R_L = \text{constant}$ ($\because R_L$ is constant so I_L also constant)

$I_s = I_L + I_Z$ → changes.
(changes) ↳ (∵ Vs changes) ↓ constant

$V_s \uparrow$	$I_s \uparrow$	$I_Z \uparrow$	(I_L const)
$V_s \downarrow$	$I_s \downarrow$	$I_Z \downarrow$	(I_L const)

case 2:- when load (R_L) is Variable:-



when we increase load resistance, the load current decrease but the supply current (I_s) is constant hence to maintain the equation ($I_s = I_L + I_Z$) zener increase its current similarly, when the load resistance decrease, the load current increases hence to maintain the eq^n zener decreases its current

$V_L = I_L * R_L$ = constant
(R_L → variable)

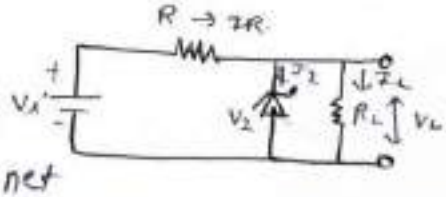
($R_L \uparrow$ $I_L \downarrow$)
($R_L \downarrow$ $I_L \uparrow$)

$I_s = I_L + I_Z$
const, changes.

($R_L \uparrow$) ($I_L \downarrow$) ($I_Z \uparrow$)
($R_L \downarrow$) ($I_L \uparrow$) ($I_Z \downarrow$)

* Zener Diode Numericals:-

case 1: when V_i & R_L fixed.



(step 1) Determine state of zener diode by remove it from the net work and calculate the voltage across resulting open circuit.

$$V = \frac{V_i}{R + R_2} \times R_1$$

* if $V \geq V_Z$ (ON)
$V_L = V_Z$

* if $V < V_Z$ (off)
$V_L = V$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L}$$

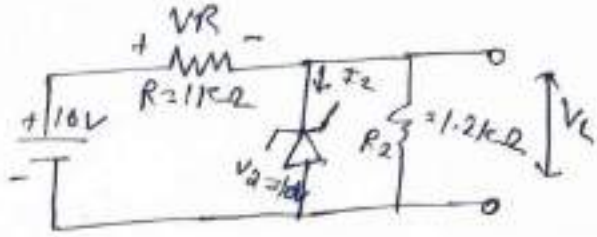
$I_R = \frac{V_R}{R} = \frac{V_i' - V_L}{R} = \frac{V_i' - V_2}{R}$

$I_2 = I_R - I_L$

$\boxed{P_2 = V_2 I_2}$

Ques # Determine V_L, V_R, I_2, P_2 ?

Ans:



$V_L = \frac{V_i'}{R + R_L} \times R_L$

$= \frac{16 \times 1.2 \times 10^3}{(1+1.2)10^3} = 8.73V$

$\because V < V_2$ so diode is off

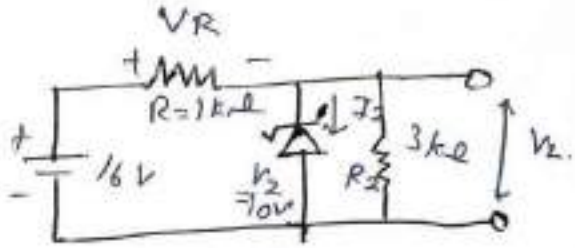
$I_2 = 0$, $V_L = V = 8.73$ volts

$V_R = V_1' - V_L = 16 - 8.73 = 7.23V$

$\boxed{P_2 = V_2 I_2 = 0W}$

Ques # Determine V_1, V_R, I_2, P_2 ?

Ans



$V = \frac{V_i'}{R + R_L} \times R_L = \frac{16 \times 3 \times 10^3}{(1+3) \times 10^3}$

$= 12$ volt

$\because V > V_2$ so diode is ON

$V_L = V_2 = 10$ volt

$I_L = \frac{V_L}{R_L} = \frac{V_2}{R_2} = \frac{10}{3 \times 10^3} = 3.33$ mAmp

$I_R = \frac{V_R}{R} = \frac{V_i' - V_L}{R} = \frac{V_i' - V_2}{R} = \frac{16 - 10}{1 \times 10^3} = 6$ mAmp.

$I_2 = I_R - I_L$

$= 6mA - 3.33mA = 2.67mA$

$P_2 = V_2 I_2 = (10 * 2.67)$ mW

$= 26.7$ mW

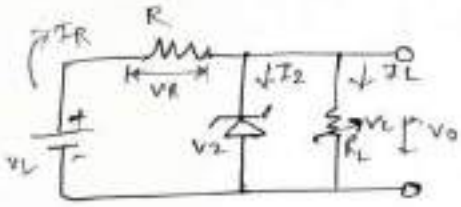
electronics 19/Dec/2022

Case-2:- fixed V_i, variable R_L:-

$R_L = min \rightarrow I_L max$
$R_L max \rightarrow I_L min$

V_i fixed I_R fixed.

$I_R = I_L + I_Z$
fixed change change.



$V_o = V_L = R_L * I_L$
R_L ↓ I_L ↑ R_L ↑ I_L ↓

• To determine the minimum load resistance to turn the zener diode on · simply calculate the value of R_L that will result in $V_L = V_Z$

diode is on condition. $V_L = V_Z$

$V_o = V_L = V_Z = IR_L$.

$V_Z = \frac{V_i}{R + R_{L min}} * R_{L min}$

$R_{L min} = \frac{RV_Z}{V_i - V_Z}$

$I_{L max} = \frac{V_L}{R_{L min}} = \frac{V_Z}{R_{L min}}$

$V_R = V_i - V_C = V_i - V_Z$

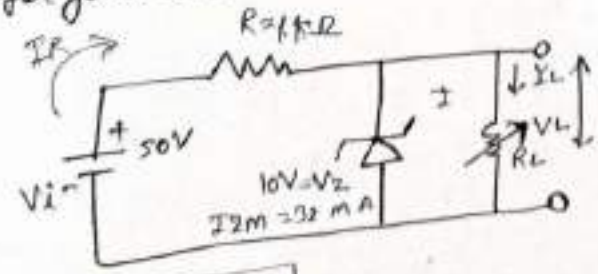
$I_R = \frac{V_R}{R_1}$

$\therefore I_R = I_{Z max} + I_{L min}$

$I_{L min} = I_R - I_{Z max}$

$R_{L max} = \frac{V_L}{I_{L min}} = \frac{V_Z}{I_{L min}}$

1. for given circuit determine range of R_L?



$I_L = \frac{V_L}{R_L}$

electronics 19/Dec/2022

- $R_{L\,min} = \frac{R V_2}{V_i - V_2} = \frac{1\times10^3 \times 10}{50-10} = 250\,\Omega$

- $I_{L\,max} = \frac{V_L}{R_{L\,min}} = \frac{V_2}{R_{L\,min}} = \frac{10}{250} = 40\,mA.$

- $\frac{V_R}{R_1} = I_R = \frac{50-10}{1\times10^3} = 40\,mAmp$

- $I_{L\,min} = I_R - I_{L\,max}. = (40-32)\,mA = 8\,mAmp.$

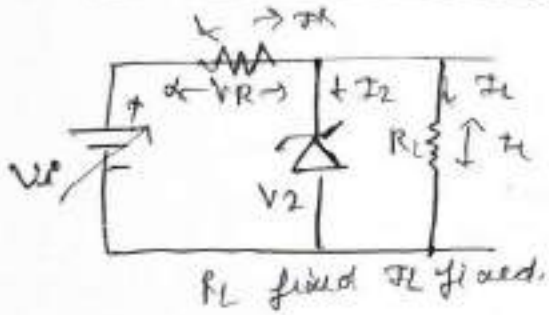
- $R_{L\,max} = \frac{V_L}{I_{L\,min}} = \frac{V_2}{I_{L\,min}} = \frac{10}{8} = 1.25\,k\Omega$

Calculate Max Power Dissipation $= (P_2)$

$P_{2\,max} = V_2\, I_{2\,max} = (10\times32)\,mW$
$= 320\,mWatts$

case 3

fixed R_L, variable V_i



$I_R = I_L + I_2$
change fixed change.

$V_i \uparrow \Rightarrow I_R \uparrow \Rightarrow I_2 \uparrow$
(keeping I_L const)

$V_i \downarrow \Rightarrow I_R \downarrow \Rightarrow I_2 \downarrow$
(keeping I_L const)

for fixed values of R_L the voltage V_i must be sufficient to turn the zener diode on. The minimum turn on voltage:

$\boxed{V_i = V_i\,min}$ is determined by:

$\boxed{\text{diode is on condition}}$

$V_L = V_2$

$V_0 = V_L = V_2 = I R_L$

$V_2 = \frac{V_i\,min}{R+R} \times R_L.$

$V_i\,min = \frac{(R_L + R)V_2}{R_L}$

$I_{R\,max} = I_{2u} + I_L$

$I_L = \frac{V_L}{R_L} = \frac{V_2}{R_L}.$

$V_i\,max = V_{R\,max} = V_{R\,max} + V_2$
$= I_{R\,max} \times R + V_2)$

electronics 19/Dec/2022

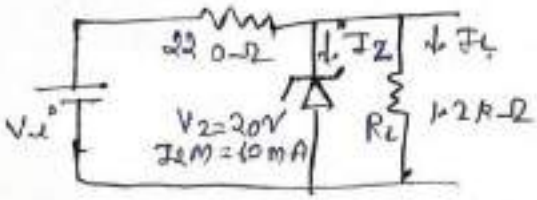
$$I_{R\,max} = I_{ZM} + I_L$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L}$$

$$V_i\,max = V_{R\,max} + V_Z$$

$$V_i\,max = I_{R\,max} \times R + V_Z$$

Q. for given determine range of V_i that will maintain the diode in on state?



$$V_i\,min = \frac{(R_L + R)V_Z}{R_L}$$

$$= \left(\frac{1.2\times10^3 + 220}{1.2\times10^3}\right)20$$

$$= 23.67\,\text{volt}$$

$$I_L = \frac{V_Z}{R_L} = \frac{20}{1.2\times10^3} = 16.67\,mA$$

$$I_{R\,max} = I_{ZM} + I_L = 76.76\,mAmp$$

$60mA + 16.67$

$$V_i\,max = I_{R\,max} \times R + V_Z$$

$$(76.767 \times 220) + 20 = 36.87\,\text{Volts}$$

(Clippers) # 20/Dec/2022

A clipper is a circuit with which the waveform is shaped by removing or clipping a portion of the applied input signal waveform without distorting the remaining part.

Types:-

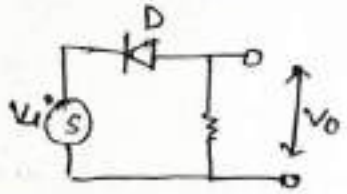
- +ve clipper
- -ve clipper
- Biased (+ve, -ve)
- combinational.

20 Dec - 2022.

(Positive Clippers)

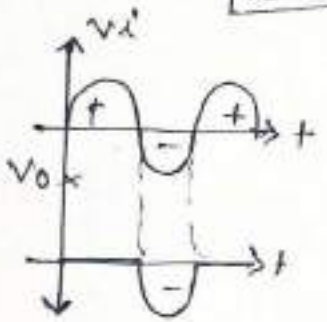
removes the +ve half cycle of the input voltage waveform

series

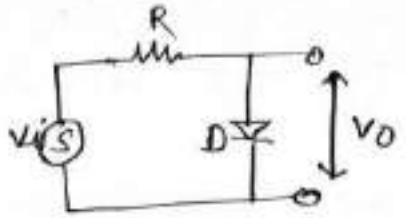


+ve half:-
diode gets Reverse biased
open circuit.
$I = 0$ $V_o = I * R = 0$

-ve half
diode gets forward, short circuit, I flows.
$\boxed{V_o = V_i}$

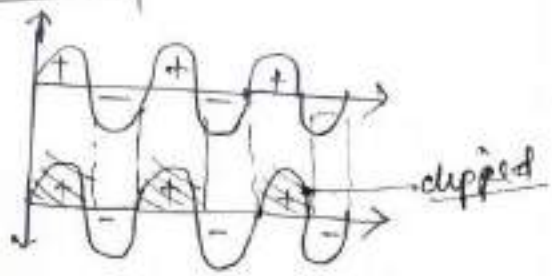


shunt



+ve half
diode f/w, short ckt
$\boxed{V_o = 0}$ (voltage across short = 0)

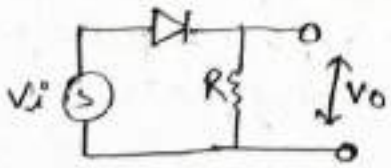
-ve half.
diode R/w, open circuit, I flows
$\boxed{V_o = V_i}$



(negative clippers)

removes -ve half cycle of the input voltage waveform

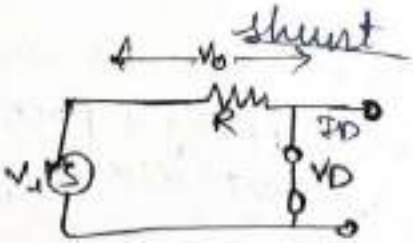
series



+ve half:
diode f/w, short ckt,
I flows
$\boxed{V_o = V_i}$

-ve half = diode R/w, open ckt
$I = 0$ $\boxed{V_o = 0}$

shunt

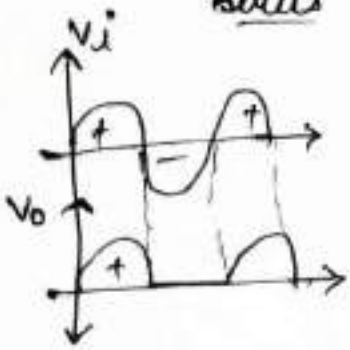


+ve half = R/w diode, open ckt
$\boxed{V_o = V_i}$ I flows.

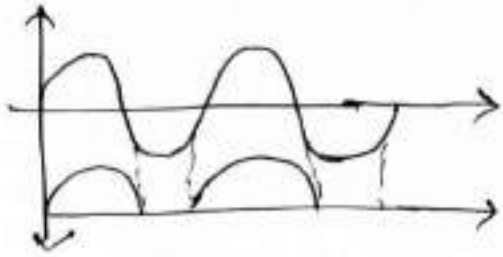
-ve half =
f/w diode, short ckt,
Voltage across short ckt will be zero, so $\boxed{V_o = 0}$

Electronics 20 Dec 2022

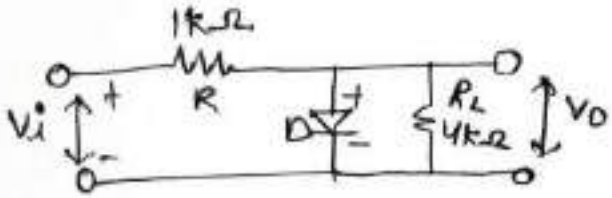
Series

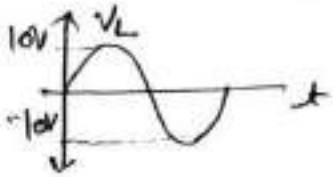


Shunt



+ve clippers





Q. determine using the given circuit?

Ans - $\boxed{\text{+ve half}}$ diode gets forward bias, short ckt

$\boxed{V_o = 0V}$

$\boxed{\text{-ve half}}$ diode get Rev bias, open ckt.

$V_o = -8V$

$V_o = I * R_L$

$= \frac{-10}{1+4} k\Omega * 4 \times 10^3$

$\boxed{V_o = -8V}$

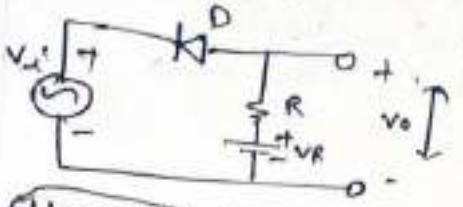
(Biased clippers)

- It used to remove a small portion of the +-ve half cycle of the input signal voltage.
- Biased means that the adjustment of clipping level is achieved by adding a biasing voltage in series with the diode or resistor.

(Biased the clipper)

21/Dec/2022

Series



(+ve half) →

$V_i < V_R$

diode f/w, short

$V_o = V_i$

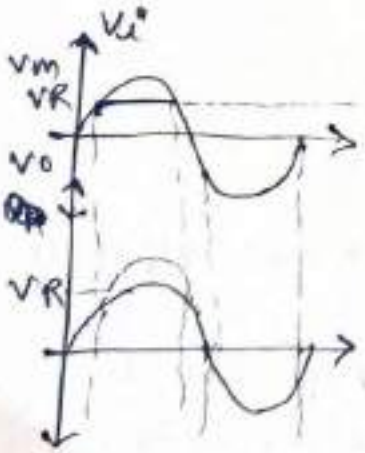
$\therefore V_i - V_\gamma + V_\gamma$

$V_i > V_R$, Reverse Diode, open ckt

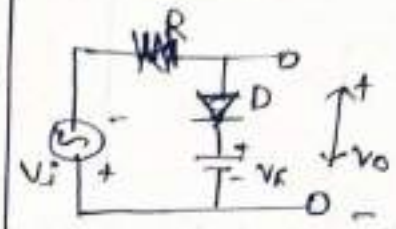
$V_o = V_R$

(-ve half) → diode is f/w biased, short ckt

$V_o = V_i$



Shunt

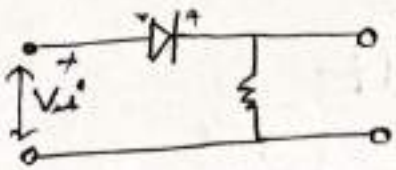


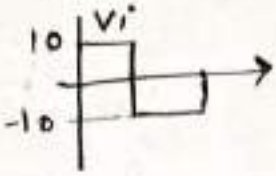
+ve half = f/w; short

$V_i < V_R$,

21/Dec/22 Electronics

Q:-



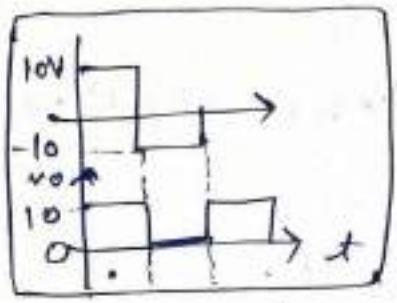


Ans:- (+ve half) = Diode f/w, short ckt

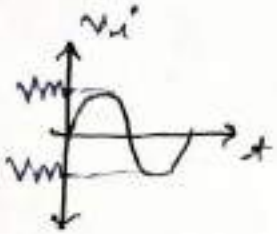
$V_o = V_i$

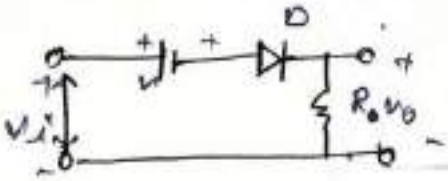
(-ve half) = Diode R/w, open ckt

$I_D = 0$ $V_o = 0$



Q:-



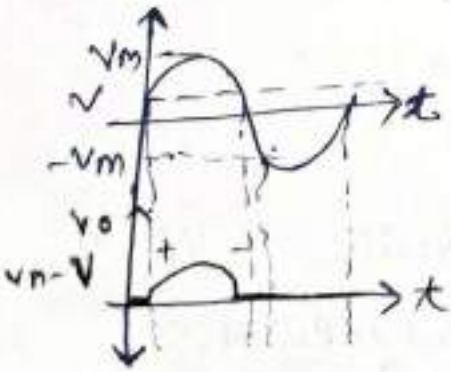


Transition Point: $V_i \leq V$

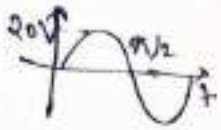
Q. Determine transition voltage that switch the diode from off to on state?

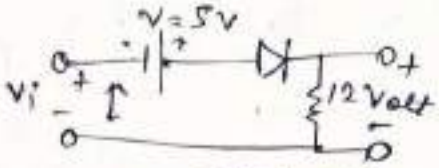
Ans: Transition Point $V_i - V \geq 0$ $[V_i \geq V]$ ON. short diode. $V_i - V - V_o = 0$ $V_o = V_i - V$

$[V_{omax} = V_m - V]$



Q For given circuit give o/p ?



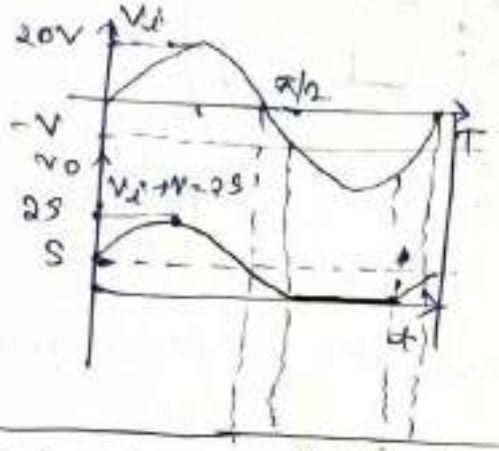


Ans:- Transition point = [redacted]

[redacted] $V_i + V \geq 0$

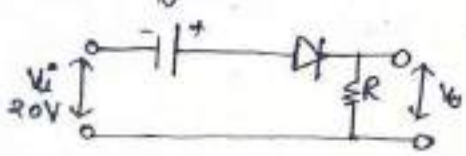
$\boxed{V_o = V_i + V}$ $\boxed{V_i \geq -V}$ diode ON

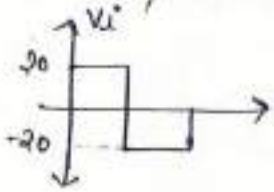
V_o max = 20 + 5 = 25 volt.



22/Dec/2022 Q.) for the given ckt draw o/p waveform ?

[redacted]





V=5

$V_i = \pm 20$

Sol^n:- +ve half:- forward, short ckt

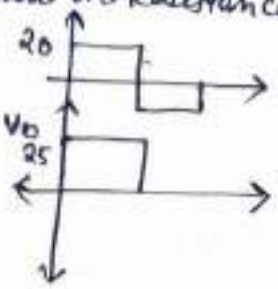
$V_o = 20 + V$

$20 + 5 = 25$ Volts

-ve half:- reverse, open circuit $V_i = -10$

diode open zero current to Resistance

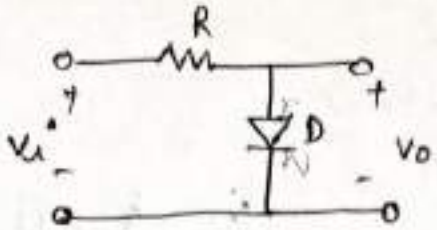
$V_o = 0$

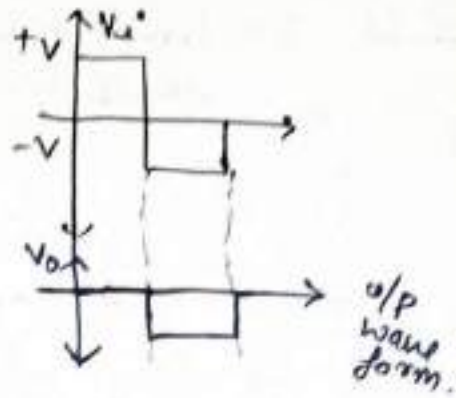


22-Dec-2022

Electronics

Q:2





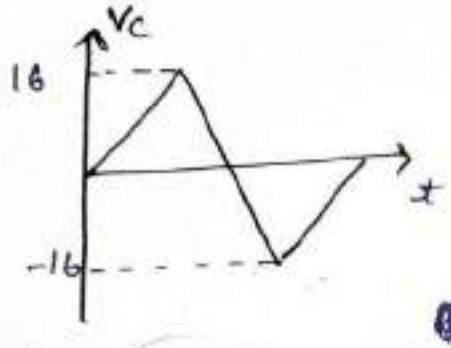
Ans:- +ve half :- forward biased short

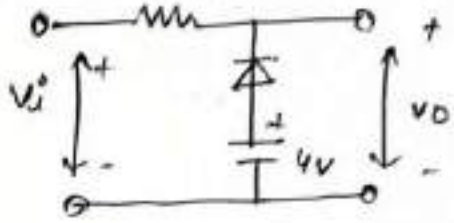
$V_o = 0$

-ve half = reverse, open

$\boxed{V_o = +V_i}$

Q3:





Sol^n:- +ve half cycle:- forward bias, short ckt

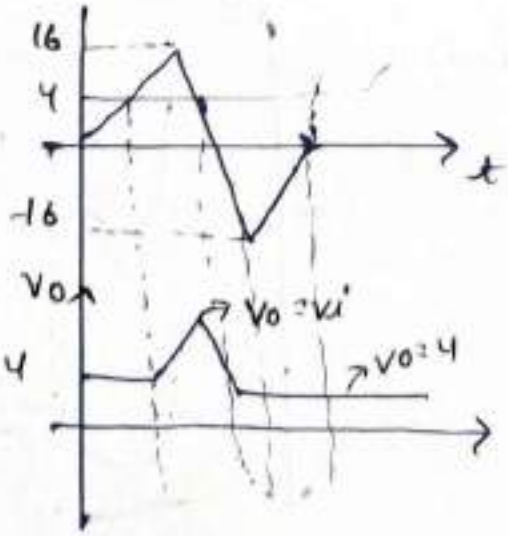
$\boxed{V_i + V \geq 0}$ $\boxed{V_i \geq 4}$ transition level

$\boxed{V_i + 4 \geq 0}$

Transition level when diode is ON

$\boxed{V_o = 4 \text{ Volt}}$

[$V_i > 4$, off, open
$V_o = V_i$]



Q: Previous Question same with Silicon diode?

Ans:

Transitional level = 3.3V

the half - forward, short

$v_i + 0.7 + 4$

$v_i - 3.3 = 0$

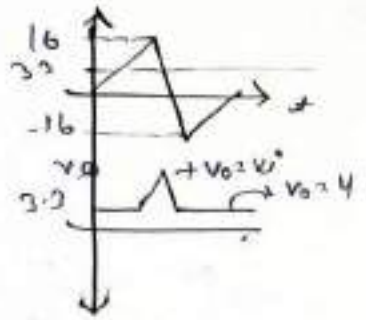
$\boxed{v_i \leq 3.3}$

[$v_i > 3.3$, off, open]

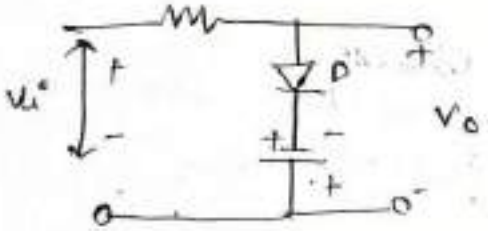
$\boxed{v_o = v_i}$

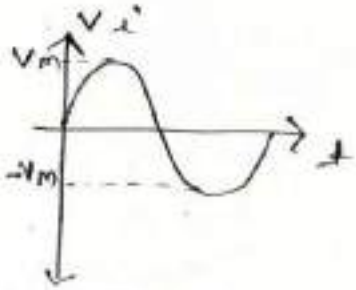
Transition level diode ON state

$V_o = 3.3$



Q:





Ans:-

$v_i > -V$, $\boxed{\text{diode on}}$

$V_o = -V$

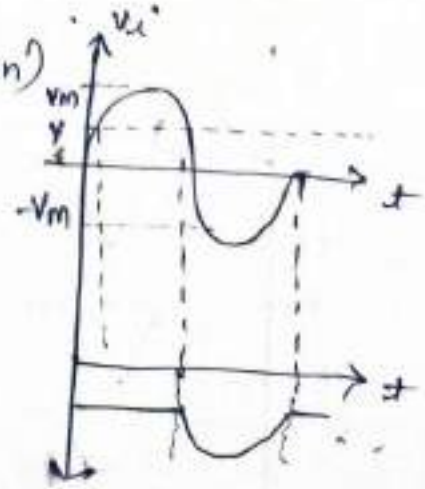
Transition:- $v_i + V \geq 0$ (diode on)

$v_i \geq -V$

$\boxed{V_o = -V}$

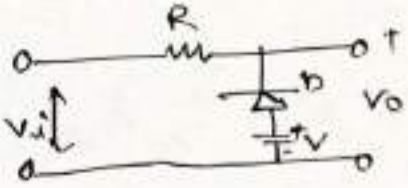
when $v_i < -V$, (diode off)

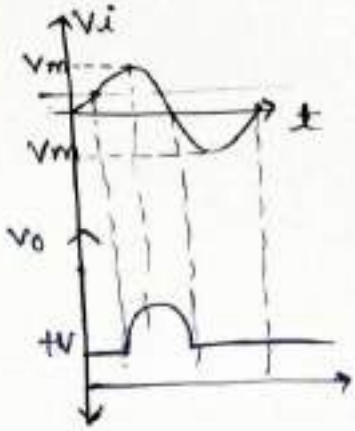
$\boxed{V_o = v_i}$



22/Dec/2021. electronics

Q.





$V_i - V \le 0$

$V_i = V$

Transition $\boxed{V_i \le V}$ diode ON

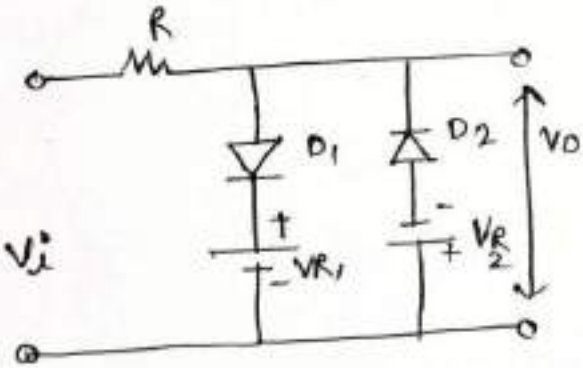
$V_i > V$, off diode

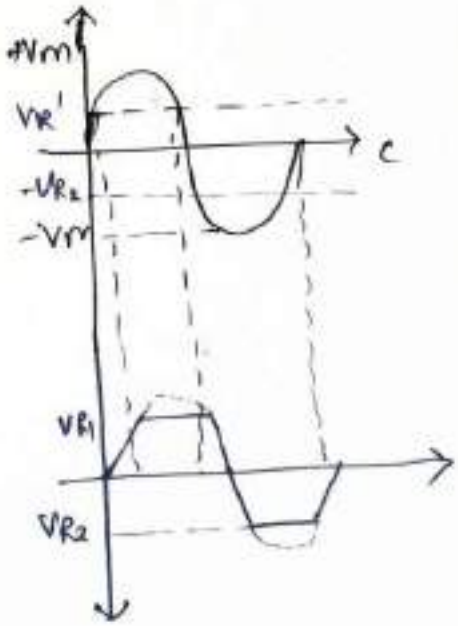
$(V_o = +V)$ $V_o = V_i$

(Combinational clippers)

its a combination of biased the & biased -ve clipper

Q:1





- Transition level =

$\boxed{\text{+ve half}}$:

D_1 = forward, short

$\boxed{V_i - V_{R1} > 0}$

$\boxed{V_0 = V_{R1}}$

$\boxed{\text{-ve half}}$ D_2 = forward, short.

$-V_i + V_{R2} < 0$

$\boxed{V_0 = V_{R2}(-)}$

$V_i < V_{R2}$

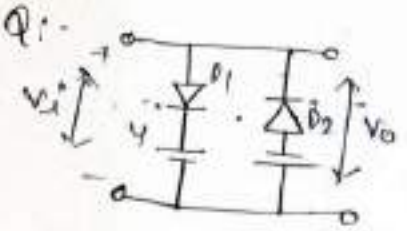
$V_0 = -V_{R2}$

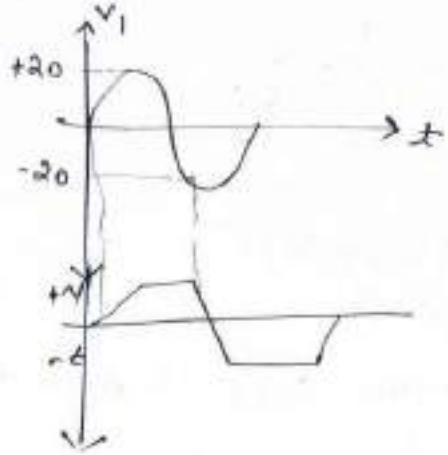
$V_i > V_{R2}$

$V_0 = V_i$

23/12/2022 (Electronics)

Q:-





Ans:-

+ve half: $D_1 = ON$ forward Short ckt

$\boxed{V_i - 4 > 0}$

$V_o = 4$

-ve half: $D_2 = ON$ reverse bias open ckt

$\boxed{V_i + 6 < 0}$

$V_i < -6$

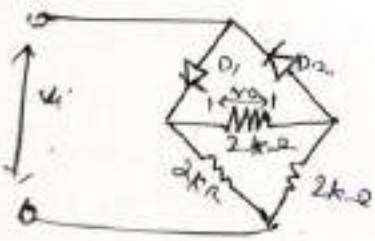
$V_o = -6$

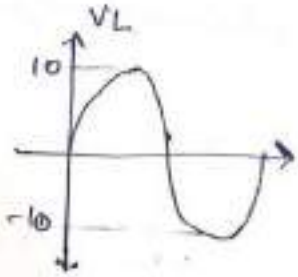
$\boxed{\text{const} = V_L = I_L * R_L}$

$\boxed{I_R = I_2 \uparrow + I_L \downarrow}$

$\boxed{R_L \uparrow \quad I_L \downarrow \quad I_2 \uparrow}$

Q:





Ans: $\frac{10}{2+2} \times 2 = 5$

$V_{dc} = \frac{2V_m}{\pi}$

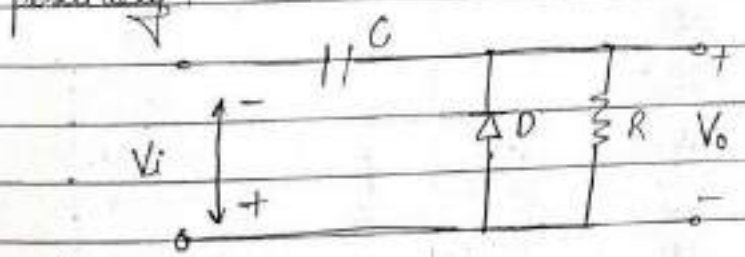
$\boxed{PIV = V_m = 5}$

Diode as a Clampers

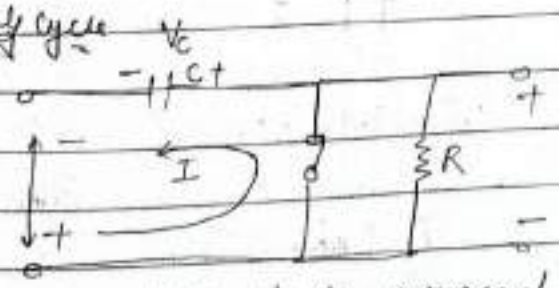
A clamper is a network constructed of a diode, as resistor and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signals.
Means clamping circuit shifts or clamp a signal to a different DC levels.
There are of three type
1) Positive clamper.
2) Negative Clamper.
3) Biased Clamper.

Positive Clamper

It is a circuit which clamps a input signal waveforms positively.



-ve half cycle



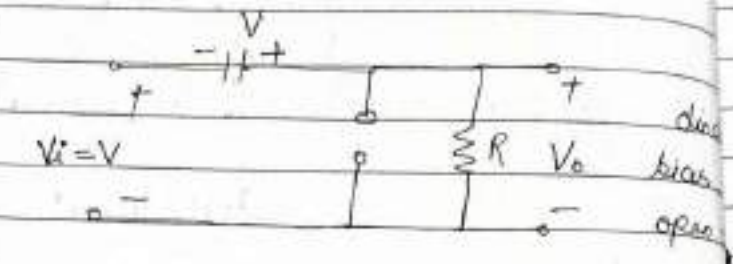
During -ve half cycle diode forward bias so short circuit and capacitor charges upto V volt due to short circuit across diode
[$V_o = 0$] (short circuit)

KVL

$-V + V_c = 0$

$[V_c = V]$

+ve half cycle

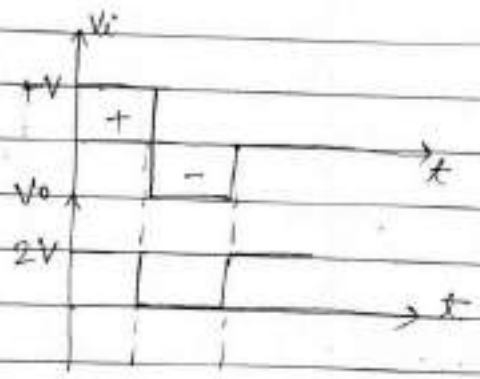


$V_i + V - V_o = 0$

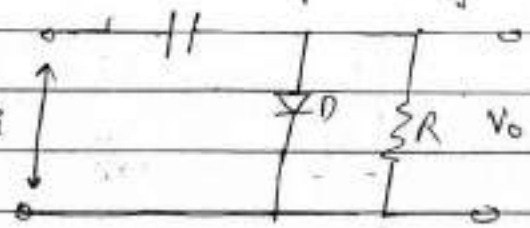
$V_i + V = V_o$

$V_o = 2V$

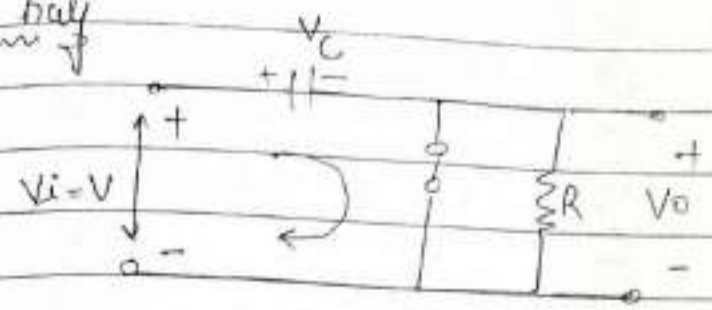
Wave form



Negative Clamper It is a circuit which clamps the input signal waveform negatively



+ve half



Diode is forward, short circuit

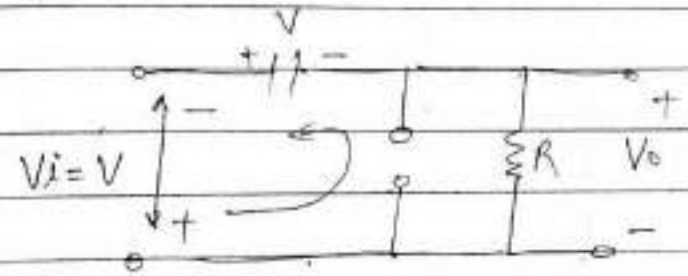
$V_o = 0$ (short circuit)

KVL

$V - V_C = 0$

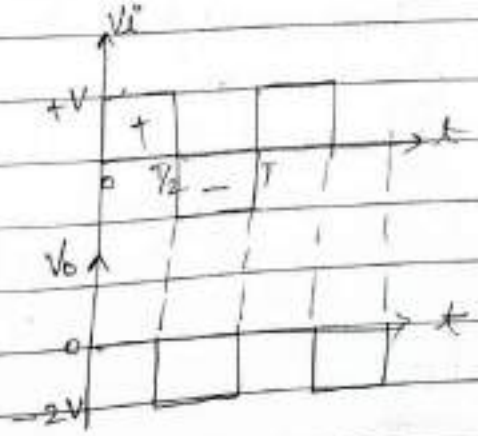
$[V_C = 0]$

-ve half cycle



$-V - V - V_o = 0$

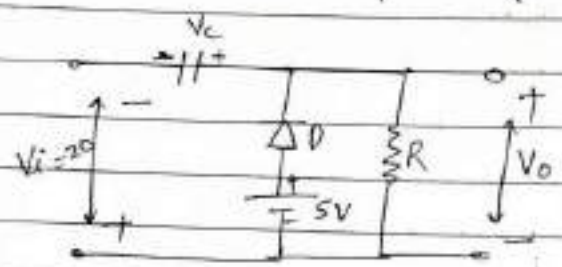
$V_o = 2V$



Biased Clampers

In case of biased clampers, clamping may be done at any voltage level other than zero, using DC sources.

Ques) Draw output waveforms for given circuit.



-ve half diode is F/W biased, short circuit

$V_o = 5V$ (short circuit)

$-20 + V_c - 5 = 0$

$-20 - 5 = -V_c$

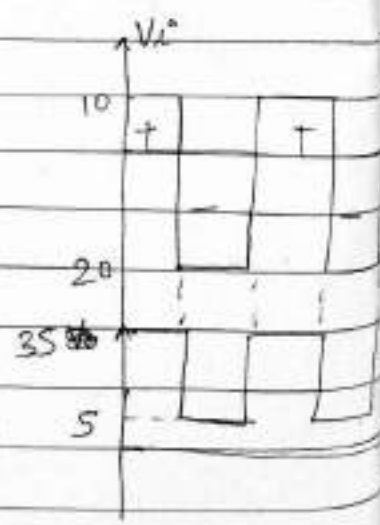
$25 = V_c$

$V_c = 25$ volts

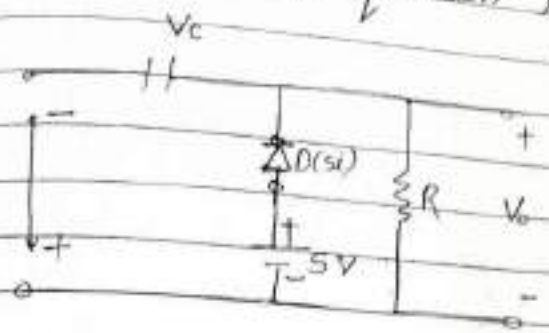
+ve half

$10 + 25 - V_o = 0$

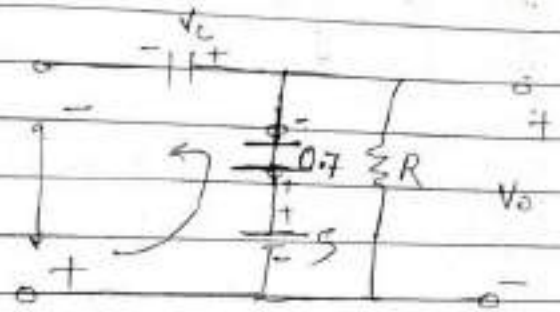
$V_o = 35$



Repeat the previous question using silicon diode



-ve half cycle.



KVL

$$5 - 0.7 - V_o = 0$$

$$V_o = 5 - 0.7$$

$$= 4.3\,V$$

~~+ve half cycle~~

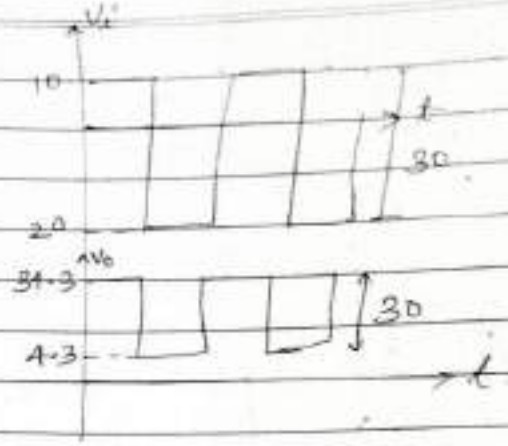
$$-20 + V_c + 0.7 + 5 = 0$$

$$V_c = 24.3 \text{ Ans}$$

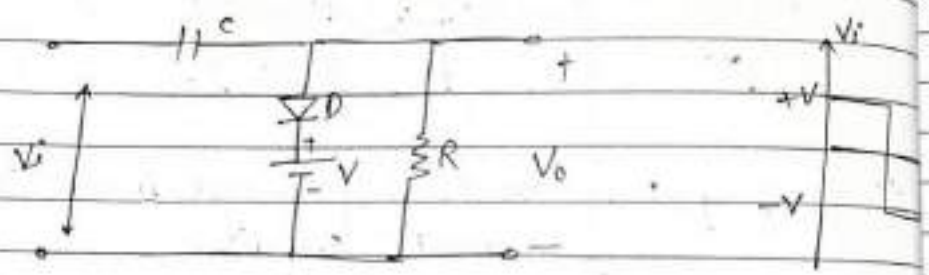
+ve half

$$10 + 24.3 - V_o = 0$$

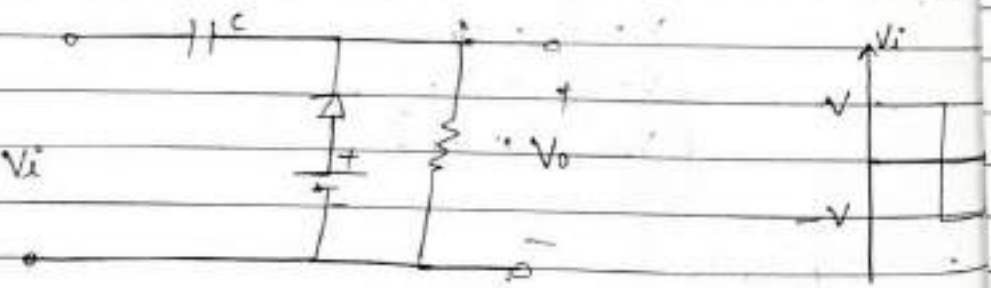
$$[V_o = 34.3]$$



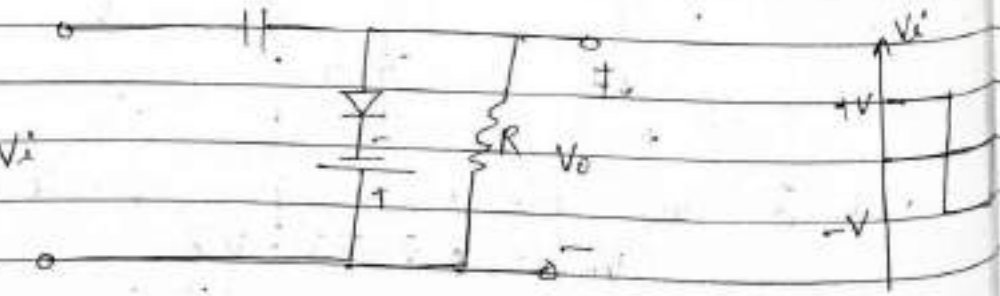
Ques)



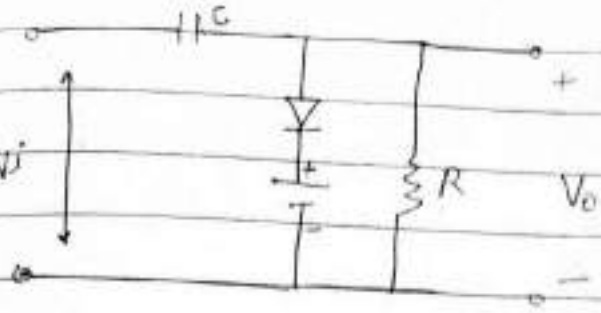
Q-2)

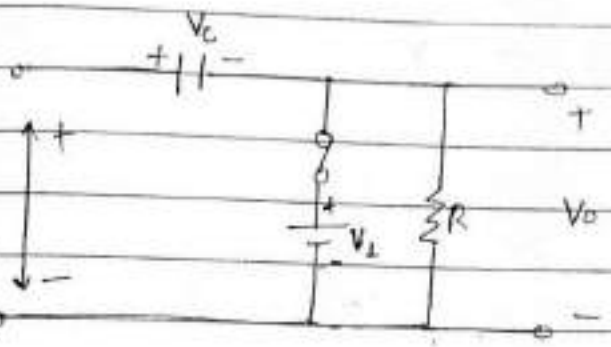


Q-3)



Q-4) Change V_i in Q2





+ve half cycle, diode is forward bias so short circuit.

$[V_o = V_1]$

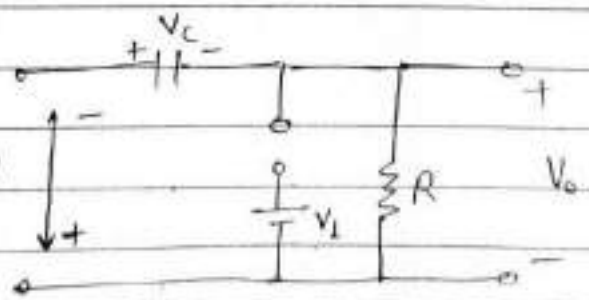
Apply KVL,

$$V - V_c - V_1 = 0$$

$$V - V_o = V_c$$

$$[V_c = V - V_1]$$

-ve half cycle



diode is reverse biased, so open circuit.

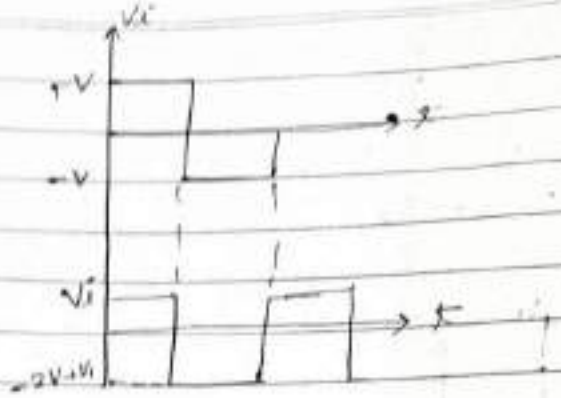
$$V_o = V - (V_1 - V)$$

$$V_o = -2V + V_1$$

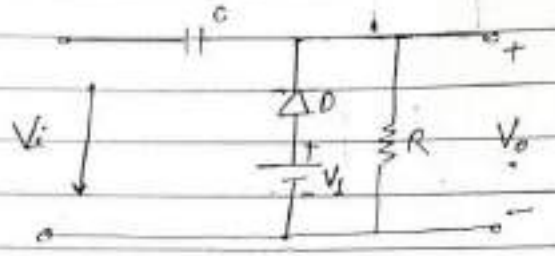
~~Applying KVL, $-V_i - V_c = 0$~~

~~$[V_c = V_i + V_1]$~~

~~$[V_c = V_1 + V_1]$~~

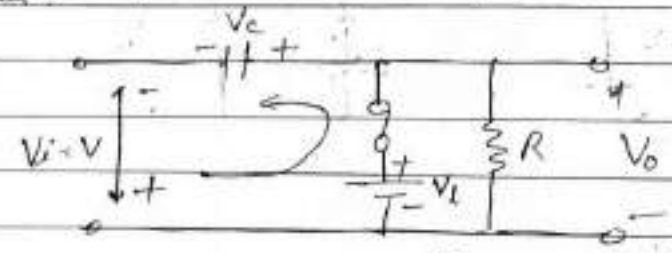


Q-2)



During -ve half cycle, diode is forward bias, so circuit

Vs-3)



Apply KCL, $-V + V_C - V_1 = 0$

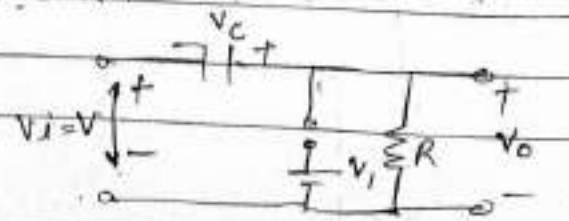
$[\cancel{V_0 = V + V_1}]$

$V_C = V + V_1$

$[V_C = V + V_1]$

$[V_0 = V_1]$ Ans

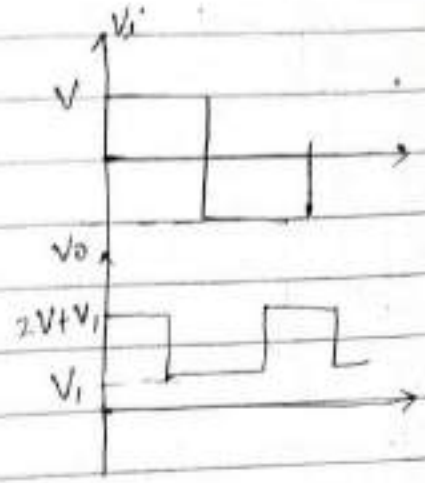
During +ve half cycle, diode is reverse biase so circuit



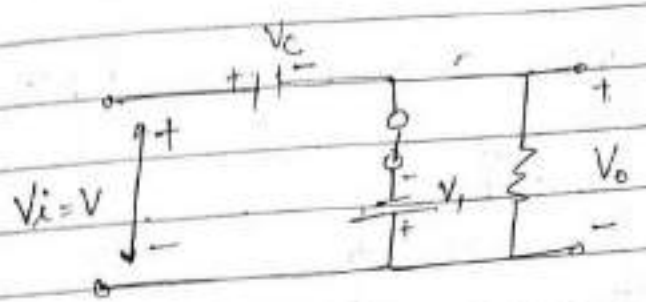
Diode is R/W, so open circuit

$V + V_1 + V - V_1 = 0$

$V_o = 2V + V_1$



Ans-3)



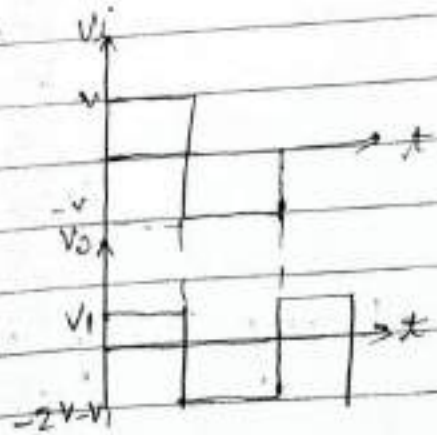
+ve half,

Diode F/W, short

$V_o = -V_1$

$V - V_c + V_1 = 0$

$V_c = V_o + V_1$



-ve half,

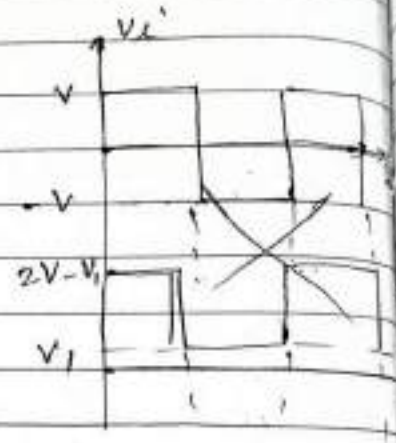
Diode R/W, open

$-V - V_1 - V - V_o = 0$

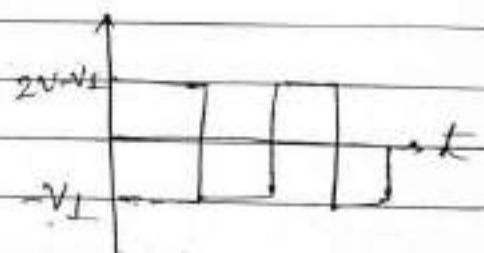
$V_o = -(2V + V_1)$

Ans 4)

For −ve half
Diode F/W, short
$[V_o = -V_1]$
$-V + V_c + V_1 = 0$
$V_c = V - V_1$



for +ve half
diode R/W, open
$V + V - V_1 = V_o$
$[V_o = 2V - V_1]$



Voltage Multiplier

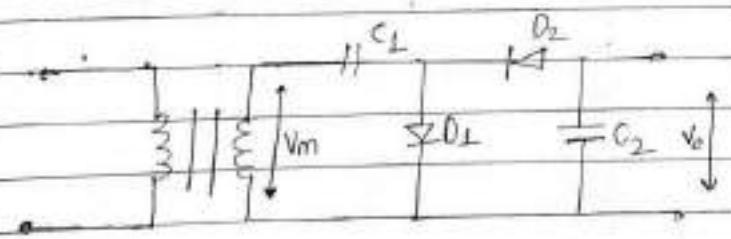
A voltage multiplier is a circuit which produces an output DC voltage where values is multiple of peak input voltage (2Vm, 3Vm, 4Vm ...)

It can be classified as:

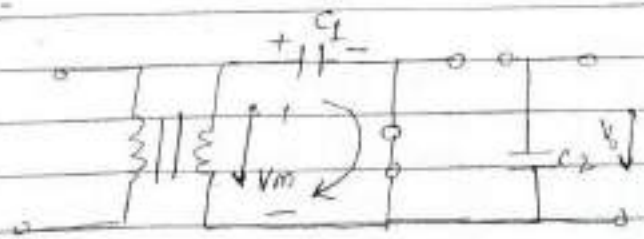
1) Voltage Doubler
   - Half Wave
   - Full wave

2) Voltage Tripler
3) Voltage Quadrupler

H.W. Voltage Doubler



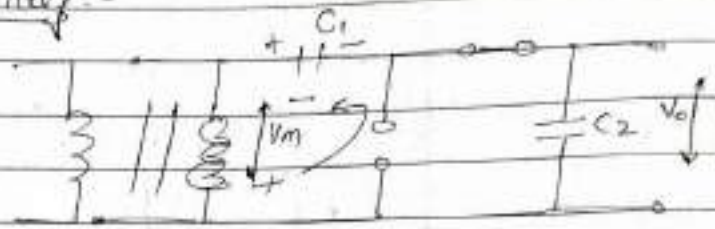
Working + Body :-



Diode D_1 conducts and D_2 is cutoff. Capacitor C_1 charges upto V_m volt.

$[V_o = 0]$

During -ve half:-

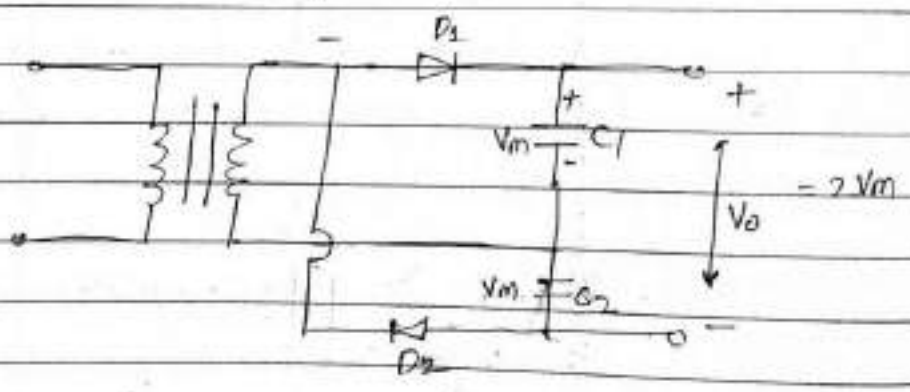


$[V_o = 2V_m]$

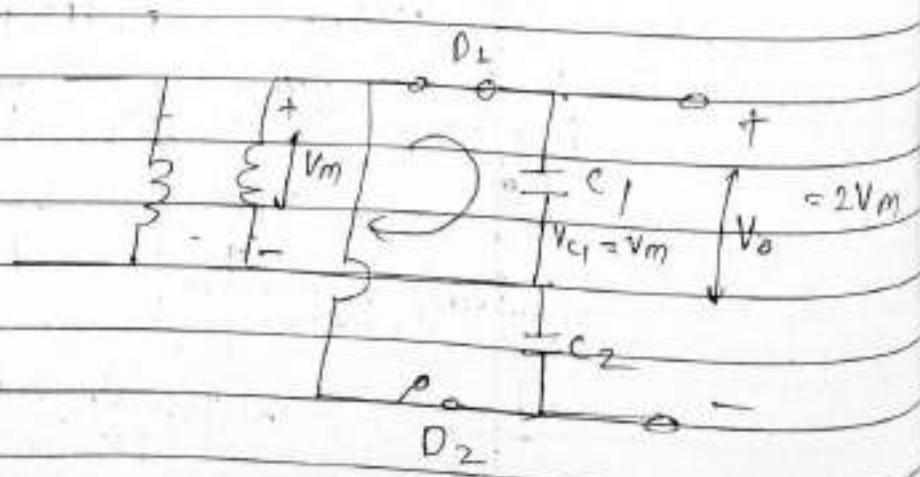
Diode D_1 ~~Vm~~ is cutoff and D_2 conducts charges the capacitor upto $2V_m$ volts.

On the next positive half cycle diode D_2 is non conducting and capacitor C_2 discharge through the load $(2V_m)$ V.

Full Wave Voltage Doubler

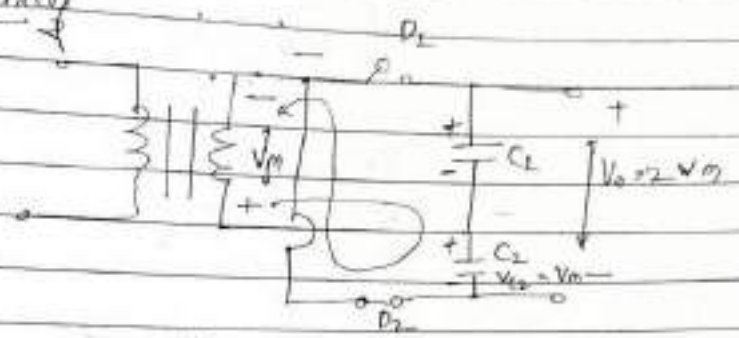


+ve half



During +ve half cycle diode D_1 is forward biased and D_2 is reverse biased. Now capacitor C_1 will charge to the maximum value of input signal.

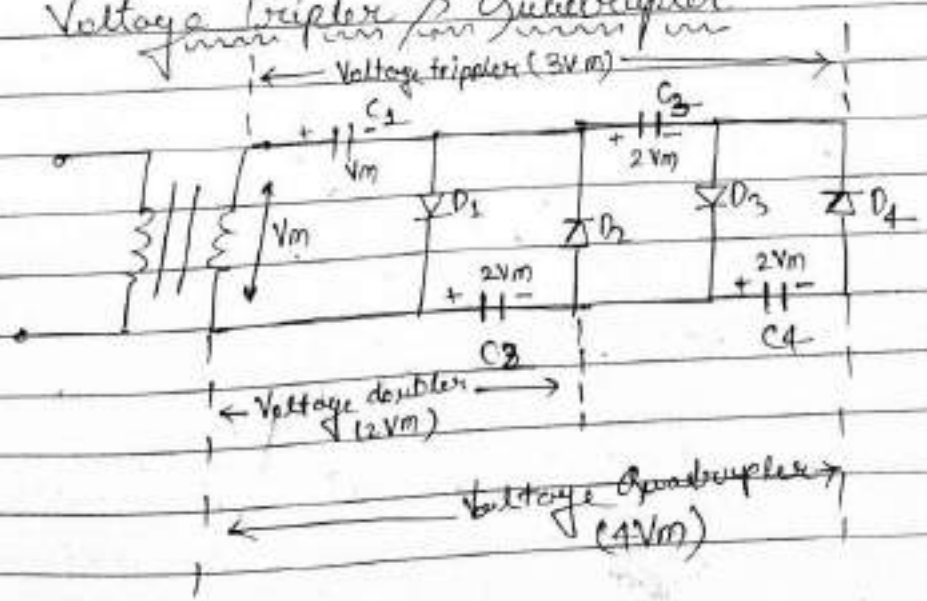
During -ve half



$[V_o = 2V_m]$

During -ve half cycle diode D_1 will be reverse biased and D_2 is forward bias now capacitor C_2 will charge to the peak value of input signal so the output across capacitor C_1 & C_2 will be twice of the maximum value.

Voltage Tripler & Quadrupler



During +ve half cycle :- Diode D_1 becomes forward biased and capacitor C_1 will charge the peak value of input signal.

During -ve half cycle diode D_2 is forward biased and capacitor C_2 will charge twice of peak value.

During second +ve half cycle Diode D_1 & D_3 are forward biased. Now, capacitor C_3 will charge to twice of maximum value.

During second -ve half cycle diode D_2 and D_4 are will be forward biased and capacitor C_4 will charge to twice of maximum value.

So, if we take output across capacitor C_2, it would be a voltage doubler.
If we take output from C_1 & C_3 it would be a voltage tripler similarly if we take output across C_2 & C_4 it would be a voltage quadrupler.

Special Purpose Diodes

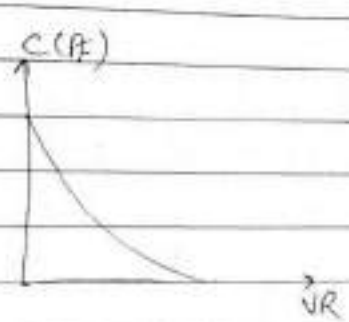
1) Varactor Diodes:- The term varactor is a short form a variable reactor which refers to the variable capacitance of R/V biased junction.

Operation & Characteristics

There mode of operations depends on its capacitance

that exist at the p-n junction when the current is reverse biased. under this condition diode behaves as a capacitance with the junction itself acting as a dielectric between the two conducting materials. The width of depletion layer depends on applied bias and capacitance is inversely proportional to the width of this layer.

C-V Curve

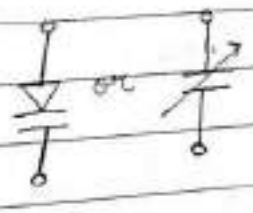


$$C_T = \frac{\epsilon A}{W}$$

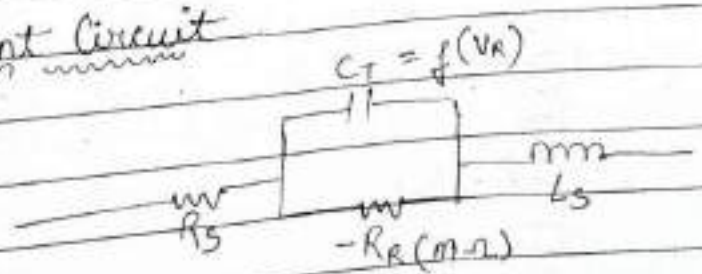
ϵ = permitivity
W = width of depletion layer
A = Area

$V_R \uparrow \; W \uparrow \; C_T \downarrow$

Symbol



Equivalent Circuit



R_S = series resistance due to connecting leads

L_S = Series inductance
R_R = Reverse resistance
C_T = Transition capacitance

Construction :- GaAs (Gallium Arsenide)

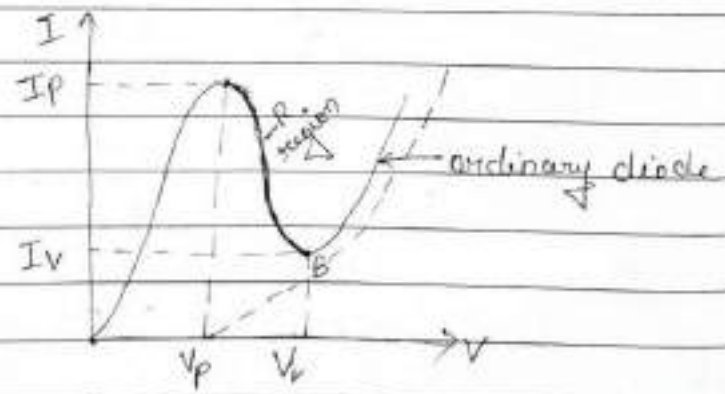
Applications

i) For microwave frequency multiplication
ii) Pulse generation
iii) In switching networks.
iv) In tuning networks
v) In active filters.

2) Tunnel Diode

is a specially made p-n junction device which contains negative resistance in forward biased characteristics. it has extremely heavy doping.

V-I curve



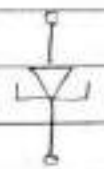
A = Peak Point

I_p :- peak current	I_V = ~~Voltage~~ Valley current	V_V = valley volt
V_p - peak voltage	B = valley point	

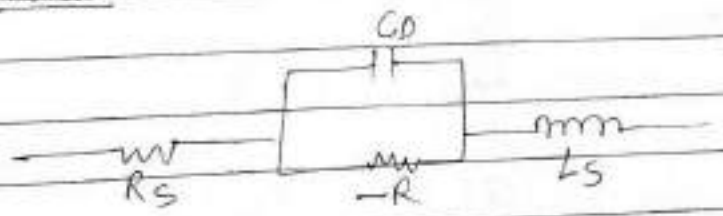
It is seen that at first forward current rises sharply as voltage is applied.

The interesting portion of curve begins at the point A. This is the voltage peak as the forward bias is increased above this point, the forward current drops and continues to decrease until point B is reached. This is the valley voltage.
At point B the current starts to increase once again and characteristics resembles like an ordinary diode.

Circuit Symbol :-



Equivalent circuit



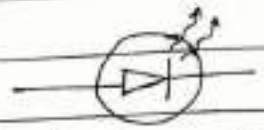
C_D - Diffusion capacitance due to F/W biased
$-R$ = reverse resistance.

Construction :- mixture of gallium arsenied and germanium.

Application:

i) For oscillators
ii) Pulse generation
iii) In switching networks.
iv) In tunning networks.
v) In Amplifiers.

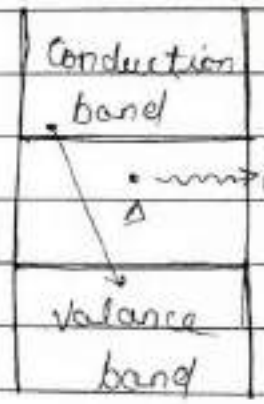
Light Emitting Diode (LED)



A diode which emits light when forward biased is called light emitting diode.

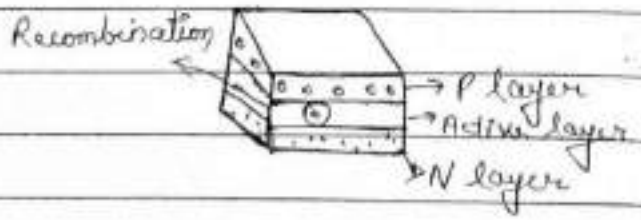
Working Principle

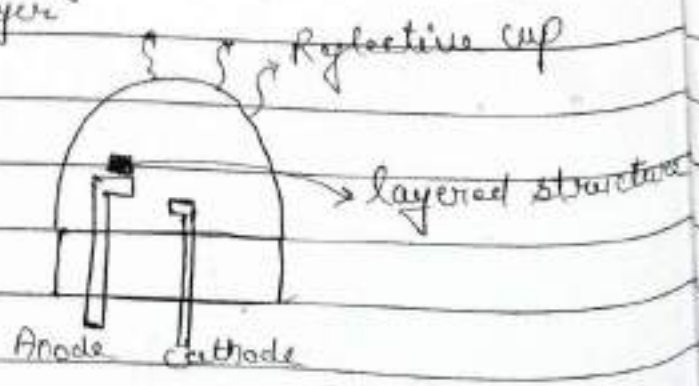
Symbol:-



Mixture:- GaAs & P.

Construction

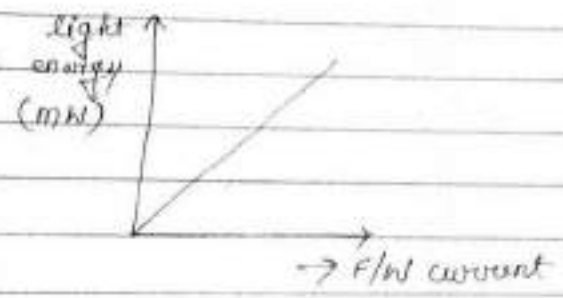




In LED three semiconductor layers on the substrate are used in between P-type and N-type region there exist a region called active, which is responsible for the emission of light.

This layered structure is placed in reflected up so that light gets reflected towards desired direction.

Output Curve



Applications

i) In seven segment display.
ii) In optical devices.
iii) In electronics circuit.

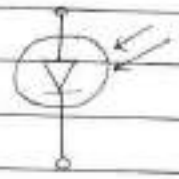
Advantages of LEDs

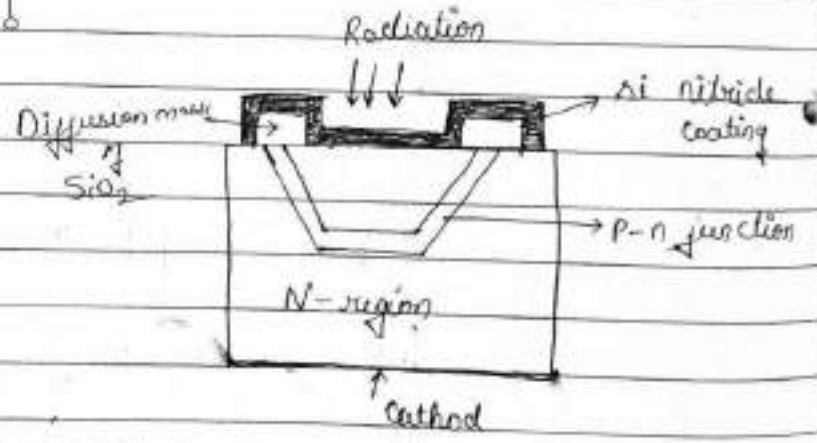
i) Small in size
ii) Fast operating device
iii) Light in weight
iv) Available in various colours.
v) Long life.
vi) Cheap

Photo diode

its a semiconductor device that converts light into an electrical current, the current is generated when photons are absorbed in photo diode

Symbol:-





When a photon of sufficient energy strikes the diode it creates an electron hole pair, this mechanism called as innere photoelectric effect. These electrons & holes start flowing in opposite direction to each other and current starts flowing in the device.

P-n junction of device is placed inside a glass material this is done in order to allow the light energy to pass through it as only junction is exposed to radiation.

Photo diode operates in two modes

i) Photo voltic mode :- This is also called zero bias mode because no external reverse potential is provided to device, however flow of minority carriers will take place when device is exposed to light.

ii) Photo Conductive mode :- When a certain reverse potential is applied to device then it would behave as photoconductive device. Here an increase in depletion width is seen with corresponding change in reverse potential.

Characteristics Curve

Dark Current : a very small current flows through the device in absence of light is known as dark current.

02/Jan/2023

Unit-2 (Transistors)

(Transistors)

- BJT (Bipolar Junction Transistor) — (current control) — (Bipolar)
  - NPN
  - PNP
- FET (unipolar) (field effect Transistor) — (voltage controlled)
  - JFET (junction FET)
    - N chanel JFET
    - P chanel JFET
  - MOSFET (metal oxide SC FET)
    - Depletion type MOSFET
      - N chanel
      - P chanel
    - Enhance MOSFET
      - N chanel
      - P chanel

(BJT) (Bipolar Junction Transistor)

BJT is a three layer semiconductor device consisting of either two (n) & one (P) type layer of semiconductor material or 2P and 1 N type layer of material.

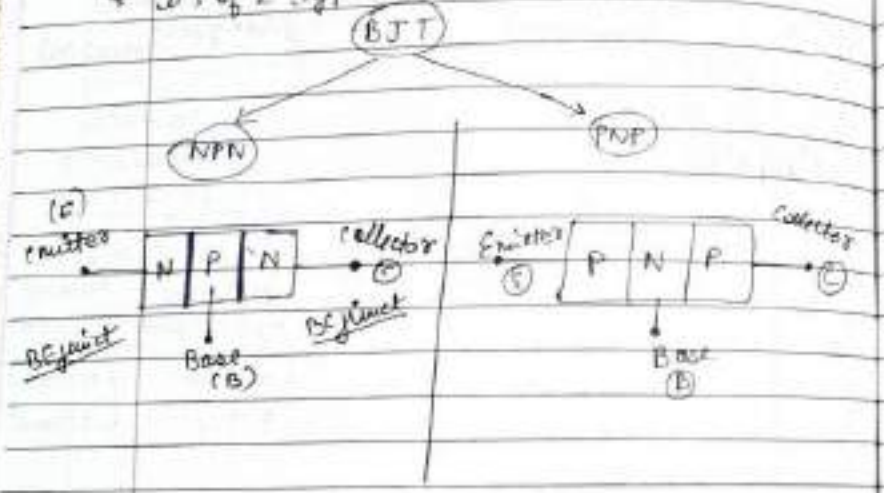
* BJT has 2 PN junctions:-

(i) Base emitter junction (BE)

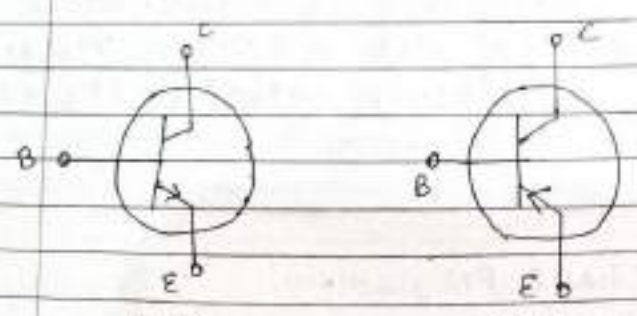
(ii) Base collector junction (BC)

- Its operation depends on flow of both majority and minority charge carriers hence its named bipolar.

* It's of 2 types :-



(Symbols for circuit)



(Construction) # (BJT Structure)

It have 3 layers E, B, C :-

(1) Emitter :- The region which emit charge carriers to next two regions is known as emitter region. the doping level of this region is always very large.

(2) Base :- The middle region is known as Base and the doping level of this region is always very small and width of this layer is very thin.

(3) Collector :- The region which collects charge carriers emitted from (E) is called (C) the doping level of this layer is more than Base but less than (E).
The (C) is made physically larger as compared to (E) because its req'd to dissipate more Δ

Electrical Profile
* doping Profile :- (E > C > B)
* Area Profile :- (C > E > B)

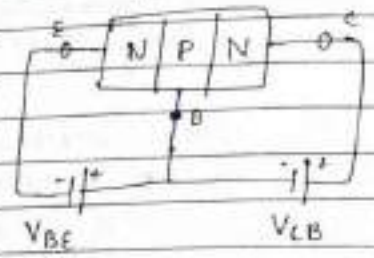
* Note :- NPN are preferred as compared to PNP because electron mobility is high as compared to holes

(Modes of BJT or Biasing of BJT)

(1) Active Mode (Amplifier)

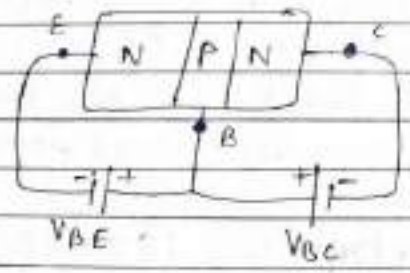
1st junction = f/w
2nd junction = R/w

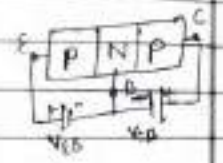
PNP
sign reverse



(2) Saturation (ON switch)

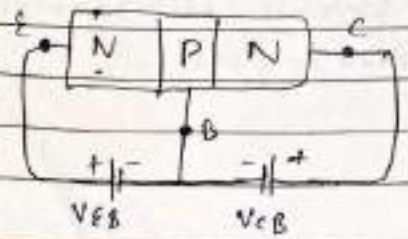
Both junction f/w.





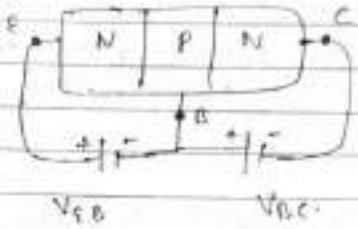
(3) Cut off (off switch)

Both junction R/w.



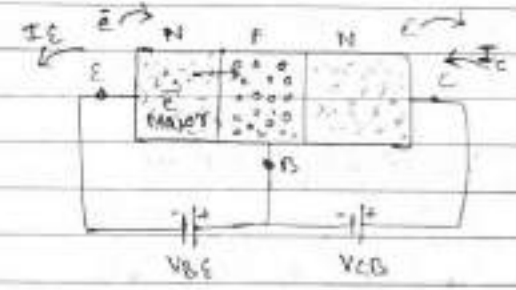
(4) Inactive (Not used)

1st junction = R/w
2nd junction = f/w



(Working of NPN)

$I_E = I_B + I_C$



* Connect BJT in active mode, the (e) is connected to (-ve) terminal of battery hence the (-ve) charge of battery repels the free (e) in n type materials. So the current flows from emitter terminal (I_E) is outward and known as emitter current. Similarly the current flows from base's terminal is known as base current (I_B) and direction is inside the transistor.

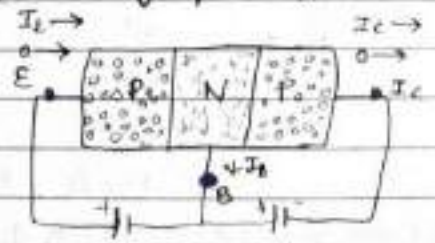
The (C) terminal is connected to (+ve) terminal of battery, so (+ve) charge of battery attracts the free e^- in collector region, so they start moving away from the junction hence the current flow from this terminal is known as collector current (I_C) the direction of (I_C) is inside the transistor.

BJT current Equation is given by:-

$$\boxed{I_E = I_B + I_C}$$

Note:- Due to this Eqn (BJT) is known as current controlled device.

(Working of PNP)



Connect BJT in active mode. The emitter terminal is connected to the (+ve) terminal of the V_{BE} battery hence the +ve charge of battery repels the holes in P-type material so the current flow from emitter terminal is inwards & known as emitter current.

- Similarly the current flow from base terminal is known as Base current (I_B) & direction of this current is outside that transistor.
- The collector terminal is connected to the -ve terminal of battery so the -ve charge of battery attracts the free holes in collector region so they start having away from the junction hence the current flow this terminal is called as collector current (I_C) & direction of this current as outside the transistor

* BJT current eq: is given by.

$$I_E = I_B + I_C$$

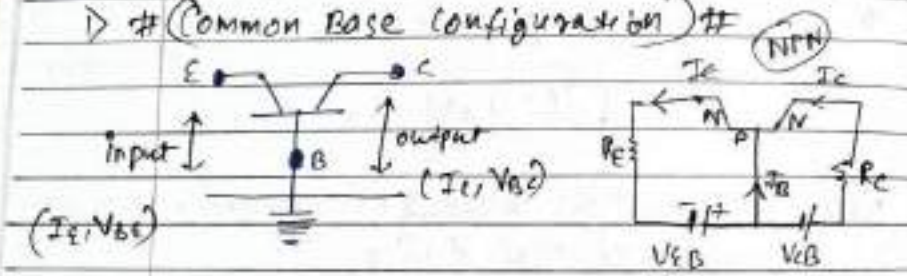
Note:- Due to this working BJT is known as current control device.

:- (Transistor Configuration) :-

The terminal which is used for both input & output is common pin. Leaving the common pin, one pin used for input and another for o/p.

* There are 3 types :-
  1. common Base (CB)
  2. common emitter (CE)
  3. common collector (CC)

▷ # (Common Base Configuration)



* Here emitter pin is input pin & collector pin is o/p pin.
* Current gain parameter for CB configuration is alpha (α) which is given by.

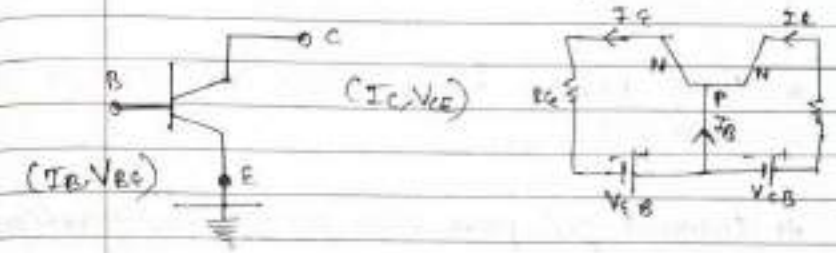
$$\alpha = \frac{\text{o/p current}}{\text{i/p current}} \Rightarrow \alpha = \frac{I_C}{I_E} \quad (\alpha < 1)$$

α, β, γ are unitless

:- (Properties of α) :-

- Always less than 1
- The range for α is from (0.95 to 0.99)

2> # (Common Emitter Configuration)



* Here base is i/p pin and collector is o/p pin this configuration is maximum used, because of high current gain parameter.
* for CE configuration current gain parameter is

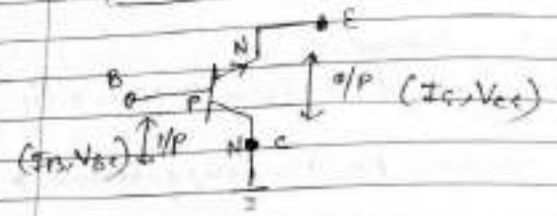
$$\beta = \frac{I_C}{I_B}$$

:- (Properties of β) :-

- β is greater than one.
- The range is kept (20-250)

Generally not used due to loading effect (increase load)

3) # (Common collector configuration) #



* Here Base is i/p pin and emitter is o/p pin

Current gain parameter for CC configuration

$$\boxed{\gamma = \frac{I_E}{I_B} >>> 1}$$

(Relation b/w Alpha (α) & Beta (β))

$\boxed{I_E = I_B + I_C}$ Divide both side by I_C.

$$\boxed{\begin{aligned} \gamma &= I_E/I_B \\ \beta &= I_C/I_B \\ \alpha &= I_C/I_E \end{aligned}}$$

* $\frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$

* $\frac{1}{\alpha} = \frac{1}{\beta} + 1$

* $\alpha = \frac{\beta}{1+\beta}$, $\beta = \frac{\alpha}{1-\alpha}$

(Relation b/w α, β & γ)

$I_E = I_B + I_C$ (multiply by I_C & $\div$ by I_C)

$\gamma = \frac{I_E}{I_B}$

$\gamma = \frac{I_E}{I_B} \times \frac{I_C}{I_C}$

$\gamma = \beta/\alpha$

* (Transistor characteristics) *

1) # Input characteristics curve. #

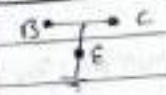
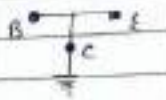
It's a curve b/w input voltage & input current for different values of o/p voltage

2) # o/p characteristics curve. #

It's a curve b/w o/p voltage & o/p current for different value of input current

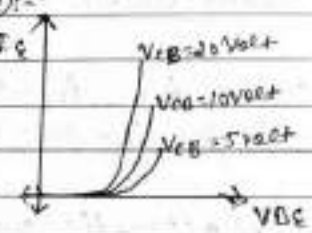
# Configuration		i/p curve	o/p curve
① CB Config.	E, C, B	I_E v/s V_{BE} for different V_{CB}	I_C v/s V_{CB} for different values of I_E

Active = Pn junction f/w
dusra R/w

Configuration	I/P curve	O/P curve
(2) CE 	I_B vs V_{BE} for different values of V_{CE}	I_C v/s V_{CE} for different I_B
(3) CC 	I_B v/s V_{BC} for different V_{CE}	I_E v/s V_{CE} for different I_B.

(Characteristics curves for) # Common Base configuration.

* (Input curve):-



1). Its a plot b/w V_{BE} & I_E for different values of V_{BC}.

2). Input curve is similar to forward curve of diode because BE junction is f/w biased.

3). Initially conduction is 0, after the barrier potential the emitter current (I_E) increases Rapidly with small increase in base emitter voltage (V_{BE})

R/w bias (↑) Dlayer (↑)
Note More increase of DL in Base due to less doping in it. #

4). It can be observed that there is increase in emitter current (I_E) with increasing V_{BC} this is due to Early effect

* Early effect :- there is change in width of Dlayer region in the Base under R/w bias condition this is known as Early effect.

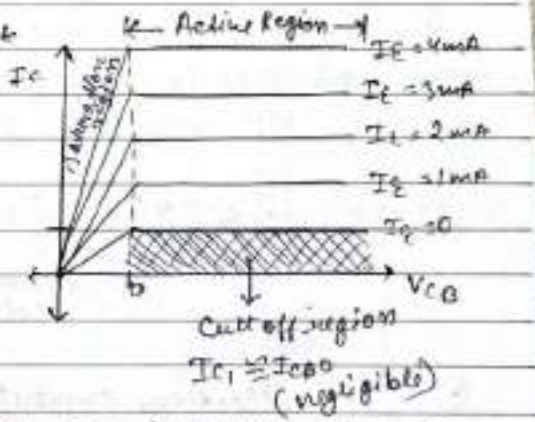
{ V_{BC} ↑, R/w ↑, DL (↑), Base width (↓) }
I_B (↓) I_E (↑)

4/Jan/2023

5). Dynamic I/p resistance is given by:-

$$r_i = \frac{\Delta V_{BE}}{\Delta I_E}\Big|_{\text{constant } V_{BC}}$$

* (Output curve) :-



- It is a curve b/w V_{BC} & I_C for diff values of I_E.
- There are few observations:-

(i) As I_E increases, I_C also increases thus I_C depends on input current (I_E). Hence I/P (↑) controls O/P current that's why BJT is current controlled device.

Q. Why BJT is current controlled

(ii) I_C doesn't depend on collector voltage and remains almost constant.

(iii) Dynamic o/p resistance is given by:-

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C} \Big/ \text{constant } (I_E)$$

- There are 3 segments in the curve:-
  1) Active region
  2) Saturation region
  3) cutoff region.

1) (Active region):- Here (BE) junction is f/w biased and (BC) junction is R/w biased.

- In this region $[I_C \cong I_E]$ and transistor works as an amplifier.

  o/p current is given by

$$[I_C = \alpha I_E + I_{CBO}]$$

(collector to Base R/w current when emitter open.)

- The collection current (I_C) is almost constant and independent of V_{BC}.

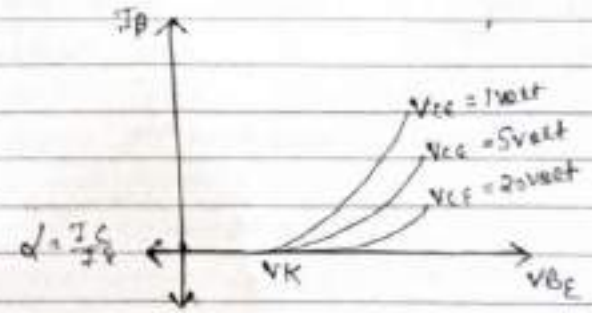
2) (Saturation region):-

- Here BE junction & BC junction is f/w biased.
- The saturation region is that region of curve which is to the left of $[V_{CB} = 0]$
- As the voltage (V_{CB}) ↑, I_C ↑.
- Here I_C is independent of (I_E).
- In saturation mode transistor works as a close switch.

3) (Cutoff region):-

- Here BE and BC junction is R/w biased.
- The region below the curve ($I_E = 0$) is known as cutoff region.
- Here $[I_C = I_{CBO}]$ which is negligible.
- In cutoff region transistor is used as an open switch.

(Characteristics curve for CE configuration)



$V = IR$

V_{CE} (↑), R/W (↑), depletion (↑), effective width (↓), diffusion (↑), I_E (↑), I_B (↓)
Early effect

- 1) It is a plot V_{CE} and I_B for different values of V_{CE}.
- 2) Because I/P junction is F/W biased, so O/P characteristics resembles a family of F/W bias diode curves.
- 3) initially current is zero due to barrier potential after free potential current increases rapidly.
- 4) As V_{CE} (↑) I_B decreases due to early effect.

(EE) # Due to reduced base width conc^n of charge carriers increases in base, causes more diffusions of e^- from n type emitter to p type base that increases (I_C) but decreases (I_B) due to reduced width.
Defined

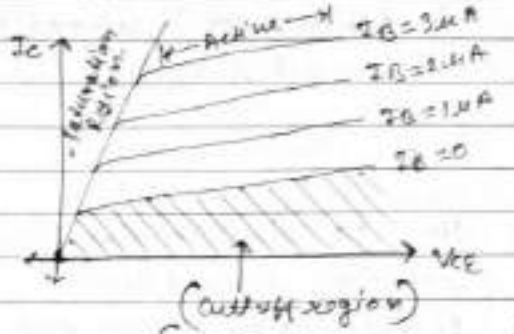
- 5) Dynamic input resistance =

$$\boxed{r_i = \frac{\Delta V_{BE}}{\Delta I_B} \Big/ \text{constant } V_{CE}}$$

output = majority + minority

$\beta = \frac{I_C}{I_B}$ — constant current

(output curve)



$$\left\{ I_C \leq I_{CEO} = (1+\beta)\, I_{CBO} \right\}$$

05/JAN/2023

* It's a plot b/w V_{CE} and I_C for different values of I_B, observations are:-

(i) Collector current (I_C) increases as (I_B) (↑).

$$\boxed{I_C = \beta I_B + I_{CEO}}$$

I_C: o/p current (To yeh batata); I_B: input current (ye bata)

- here (I_B) controls (I_C) so it's a controlled by current device.

(ii) change in V_{CE} causes little change in I_C for constant I_B.

(iii) Dynamic o/p resistance is given by:-

$$\left(r_o = \frac{\Delta V_{CE}}{\Delta I_C} \right) \Big/ \text{constant } I_B.$$

Active = 1st Junct^n f/w 2nd R/w
Saturation = both f/w
cutoff = both R/w

curve has 3 sections:-
(i) Active region
2) saturation region
3) cutoff region.

(i) (Active region)

1) Here BE junction f/w biased & CE junction R/w biased.
2) In this region curves are approximately horizontal & equally spaced.
3) As V_{CE} increases I_C also increases in small amount.
4) I_C depends on I_B.
5) Transistors works as an amplifier.

(ii) (saturation region)

1) Both junctions (BE, CE) are f/w biased.
2) Here I_C depends on V_{CE} and independent of I_B.
3) if V_{CE} is reduced to a small value then CE junction becomes f/w biased. since BE is already f/w biased. transistor operates in saturation region and works as a closed switch.

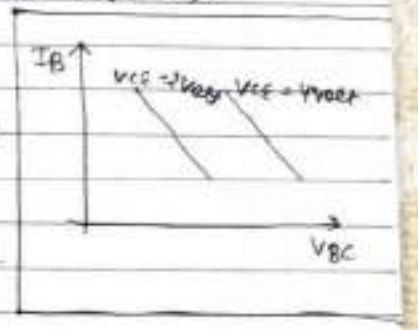
Common Base, emitter are inp

(iii) (cutoff region)

1) Both junctions (BE, CE) are reverse biased.
2) The region below the curve ($I_B = 0$) is the cutoff region.
3) Here ($I_C = I_{CEO}$) which is negligible and due to minority charge carriers.
4) Transistor works as an open switch.

(Common collector configuration)

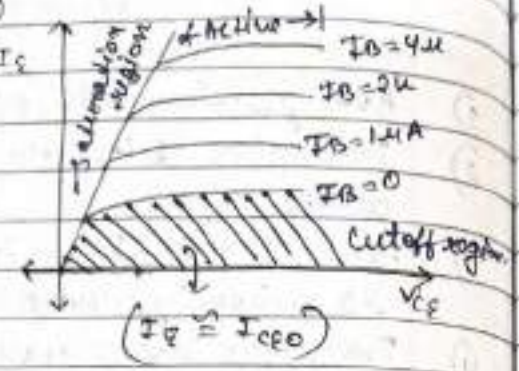
& (input curve) (I_B Vs V_{BC} diff V_{CE})



1) → its a plot b/w I_B & V_{BC} for different values of V_{CE}
2) → its similar to R/w VI curve of a P-N junction diode.
3) → when V_{BC} increases I_B decreases.
4) → V_{BC} is largely determined by V_{EC} value

$V_{EC} = V_{EB} + V_{BC}$
$V_{EB} = V_{EC} - V_{BC}$
(V_{BC} ↑) (V_{EB} ↓) so (I_B ↓)

* (output curve)



$\gamma = \frac{I_C}{I_B}$

$\boxed{I_C = \gamma I_B + I_{CEO}}$

- it is a curve between I_C & V_{CE} with different values of (I_B)
- it is similar to output curve of collector & emitter configuration (CE)
- Emitter Current (I_C) increases as (I_B) increase.
- Total current

  I_C = majorcomponent + minority component

  $I_C = \beta I_B + I_{CEO}$
- Here I_C controls I_B, so its a current controlled device.
- Change in V_{CE} causes little changes in I_C for constant I_B
- Here curve has 3 regions : 1) Active 2) Saturated 3) cutoff.

* **Active Region:-** 1) Here BC is f/w biased CE is R/w biased.
  2) Curves are approx horizontal and equal spaced.
  3) As V_{CE} increases I_C also increases in small amount
  4) Transistors work as Amplifier.

* **Saturation region:-** (1) Both region BC & CE are f/w biased.
  (2) Here I_C depends on V_{CE} and independent of I_B.
  (3) Transistor work as closed switch.

* **Cutoff region:-**
  1) Both junction BC and CE are in Reverse Biased condition.
  2) Here $I_C \cong I_{CEO}$ which is negligible due to minority component
  3) Transistors works as an open switch here.

(Relation b/w α & γ)

- As we know:-

$$\boxed{I_E = I_B + I_C}$$

- Divide by I_E both sides:-

$$\frac{I_E}{I_E} = \frac{I_B}{I_E} + \frac{I_C}{I_E}$$

$$1 = \frac{1}{\gamma} + \alpha$$

$$\boxed{\gamma = \frac{1}{1-\alpha}}$$

$\alpha = I_C / I_E$
$\beta = I_C / I_B$
$\gamma = I_E / I_B$

(Relation b/w β & γ)

- As we know

$$I_E = I_B + I_C$$

Divide by I_B both sides.

$$\frac{I_E}{I_B} = \frac{I_B}{I_B} + \frac{I_C}{I_B}$$

$$\boxed{\gamma = 1 + \beta}$$

(current relation in BJT)

(i) (for common base configuration):-

As we know $(I_E = I_B + I_C)$

$$I_C = \underbrace{\alpha I_E}_{f/w} + \underbrace{I_{CBO}}_{R/w}$$

$$\alpha = \frac{I_C - I_{CBO}}{I_E}$$ — nearly negligible

so $\boxed{\alpha \cong \frac{I_C}{I_E}}$

(ii) (for common emitter configuration):-

As we know BJT eqn.

$$(I_E = I_B + I_C) \quad \text{—①}$$

∵ and for CE configuration.

$$I_C = \underbrace{\alpha I_E}_{f/w} + \underbrace{I_{CBO}}_{R/w} \quad \text{—②}$$

* In CE configuration o/p current is I_C & i/p current is I_E so replace I_B from eqn ①

$$I_C = \alpha (I_B + I_C) + I_{CB}$$

$$I_C = \alpha I_B + \alpha I_C + I_{CBO}$$
$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$
$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}$$

$$\therefore \quad \frac{\alpha}{1-\alpha} = \beta$$

$$\frac{1}{1-\alpha} = 1+\beta$$

$$I_C = \beta I_B + (1+\beta) I_{CBO} \quad \cong I_{CEO}$$

$$I_C = \beta I_B + I_{CEO}$$

$$\left[\therefore \; I_{CEO} = (1+\beta) I_{CBO}\right]$$

So we have:-

Exactly:- $\left(\beta = \frac{I_C - I_{CEO}}{I_B}\right)$ negligible nearly.

Nearly:- $\left(\beta \cong \frac{I_C}{I_B}\right)$

(iii) (for common collector configuration)

As we know BJT current Eq^n is given by

$$I_E = I_B + I_C \quad \text{—①}$$

and for CE configuration

$$I_C = \beta I_B + I_{CEO}$$

* In CC configuration O/p current is (I_E) & I/p current is (I_B) so replace I_C from equation① in equation②

$$I_E - I_B = \beta I_B + I_{CEO}$$
$$I_E = (1+\beta) I_B + I_{CEO}$$

$$\boxed{I_E = \gamma I_B + I_{CEO}}$$

$$\gamma = \frac{I_E - I_{CEO}}{I_B} \qquad \left(\gamma \cong \frac{I_E}{I_B}\right)$$

Q:- In a BJT circuit (I_C) = 10 mA (α) = 0.98, calculate I_B & I_E?

Ans:- $\alpha = \frac{I_C}{I_E}$

$$0.98 = \frac{I_C}{I_E} \quad : \quad I_E = \frac{1000}{98} = 10.2040$$

$$I_E = 10.204$$

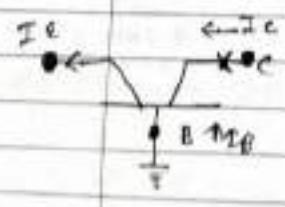
$$I_E = I_B + I_C$$
$$10.204 = I_B + 10$$
$$I_B = 0.204 \text{ mA}$$

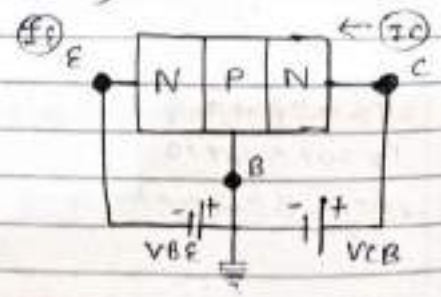
(comparison of different configurations)

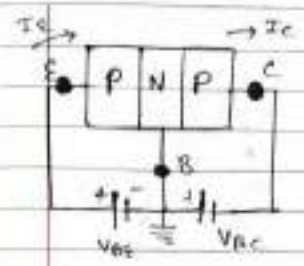
characteristics	CB	CE (IMPORTANT)	CC
① current gain (A_I)	$\alpha < 1$	β (high = 100)	high (γ = 100)
② voltage gain (A_V)	medium (150)	high (400)	less than unity.
③ power gain (A_P)	medium (150)	Very high (40000)	low (100)
④ input resistance (r_i)	low	medium	very high
⑤ output resistance (r_o)	very high	medium	low
⑥ Application.	for high frequency	for Audio frequency	for impedance frequency

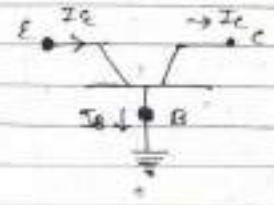
(circuits for different configurations)

(i) (CB configurations.)

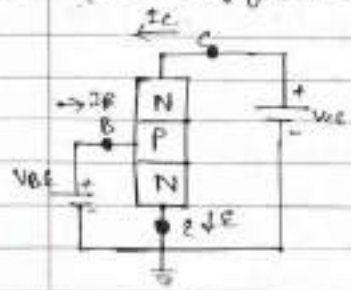


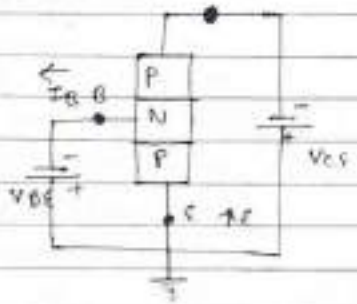


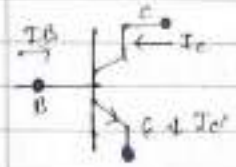


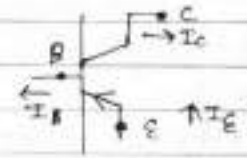


(ii) (CE configurations)

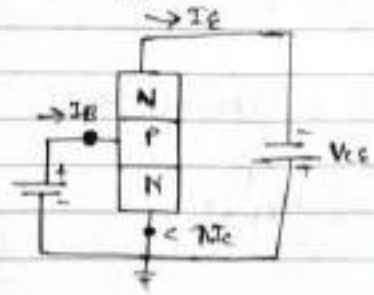


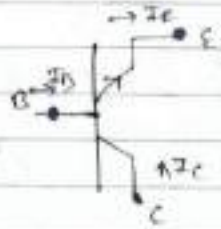


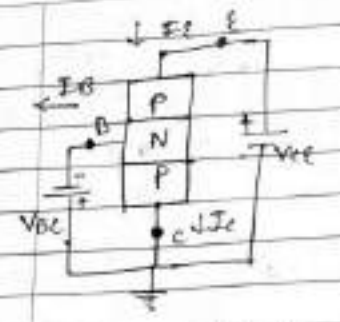


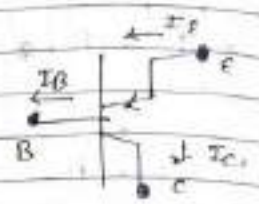


(iii) (CC configurations)









(voltage controlled device)

(field effect transistor (FET))

The name "field effect" is derived from the fact that the current flow in the device is controlled by an electric field setup by an externally applied voltage. Hence its voltage controlled device.

- It is a unipolar device here current is due to only one type of charge carrier either free (−) [n channel device] or holes [P channel device]

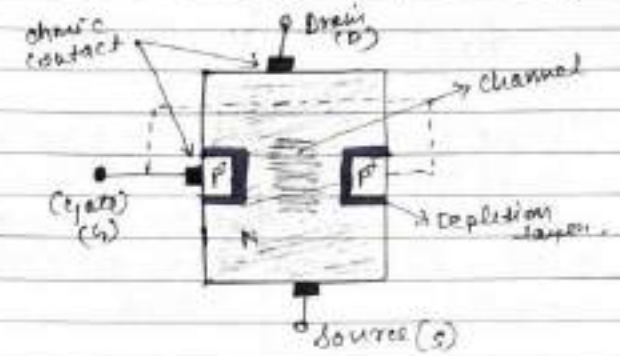
- fet is of 2 types :-
  (i) Jfet (ii) Mosfet.

(i) JFET = there is 2 types of Jfet.

N channel — P channel.

(Heavy doping is shown by + charge)
N channel - N as bulk materials.
Position of battery devices (SLD)

(construction of N channel Jfet)



1). It has a bar of 'N' type silicon material, the terminals at the 2 ends of this bars are called drain & source.

2). Heavily doped 'P' regions are formed on 2 sides of this bar designated as P⊕

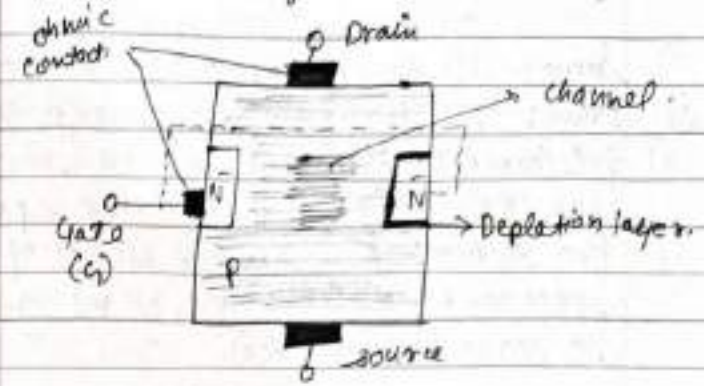
3). These 2 P regions are internally connected to a common terminal called gate (G).

4). The region of N material b/w 2 opposite P⊕ region is called as channel.

Difference b/w :-

BJT	FET
• This is a current controlled device means the i/p current controls the o/p current.	• This is a voltage controlled device means voltage at the gate controls the drain current.
• This is a Bipolar device, means current flows due to both e^- & holes.	• This is a unipolar device means current flows either due to e^- or holes.
• Current flows through junction.	• Current flow through channel.
• Switching speed is less.	• Switching speed is high.
• More Noisy operation.	• Less noisy operation
• I/p impedance is low	• I/p impedance is high.
• less temp stable.	• more temp stable.
• large size.	• smaller than BJT.

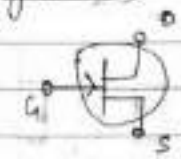
Construction of P channel JFet



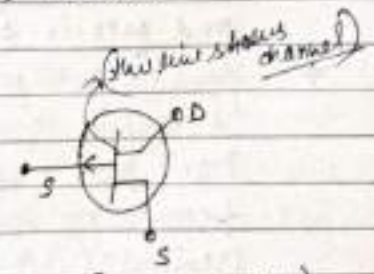
- It has slab/bar P-type silicon material. The terminals at the 2 ends of this base are called drain & source.
- Heavily doped n-region are formed on two sides of this bar designated as N^-. There are 2 N-region are internally connected to common terminal called gate.
- The region of P- material b/w 2 opposite N-region is called as channel.

16/JAN/23

Symbols



(N-CH JFet)



(P-CH JFet)

(Pinchoff :- condition. V_{DS} when happens combines at drain side)

(Structure of JFet)

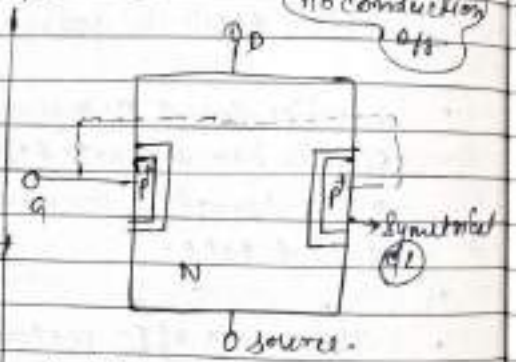
1) Source :- Its the origin of charge carrier.
2) Drain :- Its drains away the charge carrier
3) Gate/channel :- The charge carriers in the bar have to pass through the space b/w two (n^+, p^+) region. Width of this space can be controlled by changing gate to source voltage (V_{GS})

Mark (4) ## (Working of N-channel JFET) # VVIMP

(Case 1) :- No biasing is applied :-

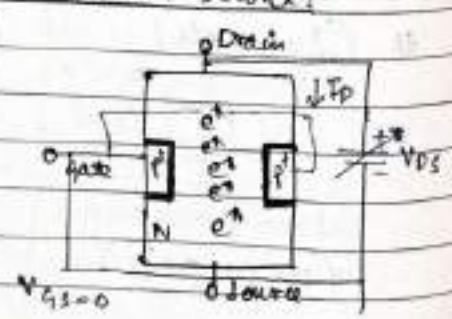
$I_D = 0$ no conduction

* When no bias is applied both Depletion regions are symmetrical and drain current (I_D) = 0



(Case 2) :- When the voltage Applied to Drain wrt source and gate is shorted with source :-

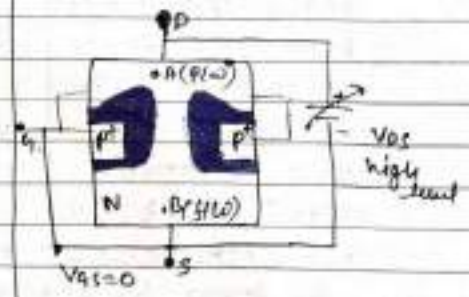
* When the voltage is applied to Drain free e⁻ moves from source to Drain, so (I_D) flows through the channel from Drain to Source



- When you'll increase voltage in case (2) increase in (I_D).
- B/w (A) DL (A)

(Case 3) :- When V_{DS} is further increased :-

- When V_{DS} is further increased Depletion region expands, DL region width is more at drain end (A) as compare to source end (B).

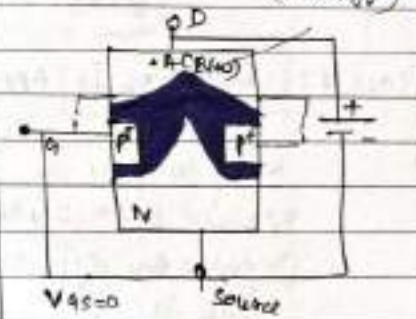


- The channel becomes very narrow at point (A). In this case as V_{DS} increases (I_D) also increases

VVIMP

(Case 4) :- Pinch off condition :-

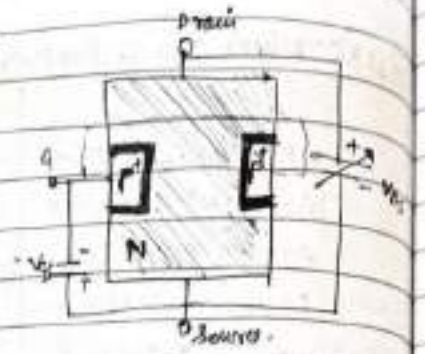
- If the voltage V_{DS} is increased further. A condition comes when the 2 depletion region meet at a point near the drain end.
- And the channel is pinched off.



- The minimum value of V_{DS} at which pinchoff occurs is called pinchoff voltage (V_P). Now if V_{DS} is increased beyond (V_P), (I_D) remains constant, and the maximum saturated current is denoted as (I_{DSS}) (Drain to source current with gate shorted by source) ($V_{GS}=0$)

Case 5:- (Effect of V_{GS})

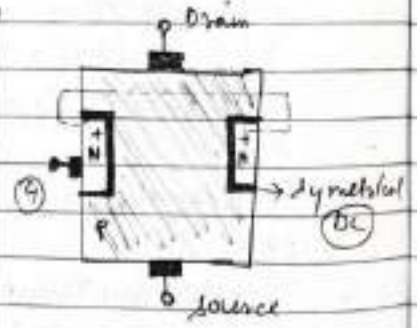
- Applying -ve voltage at V_{GS} depletion region becomes more deeper compared to V_{GS} is equal to zero. hence I_D (Drain current) will be lower as compare to $V_{GS} = 0$ and pinchoff occurs for lower levels of V_{DS}.
- The value of V_{GS} at which $[I_D = 0]$ is called as V_{GS} of Parameter and device is turned off.



(Working of P-channel JFet):-

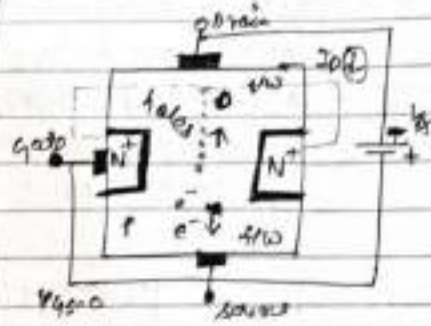
Case 1: No Bias is Applied:-

when No Bias is applied both depletion regions are symmetrical & (I_D is = 0)



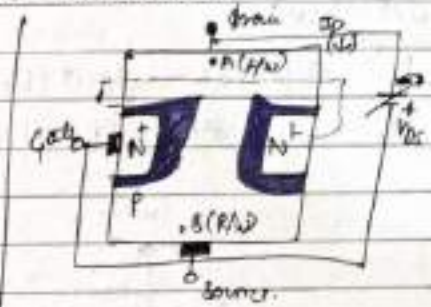
case 2: When the voltage is applied to Drain wrt to source & gate is shorted with source:-

- when the voltage is Applied to Drain free holes move from drain to source so drain current flows through the channel from D to S.



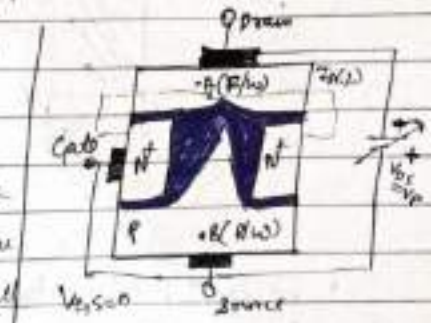
case 3: when V_{DS} is further increased:-

when V_{DS} is further increased depletion region expand. DR is more at Drain end A. as compare to source end B.



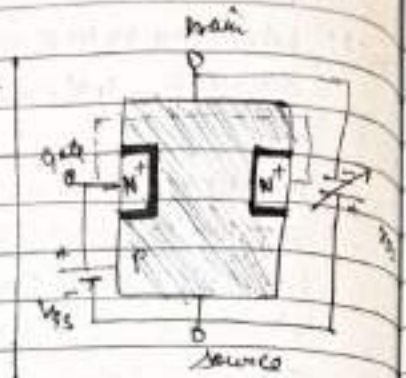
case 4: Pinch off condition.

- If the V_{DS} is increased further a condition comes when the two depletion region meet at a point A near the drain. and the channel is pinched off.



Case 5:- (Effect of V_{GS})

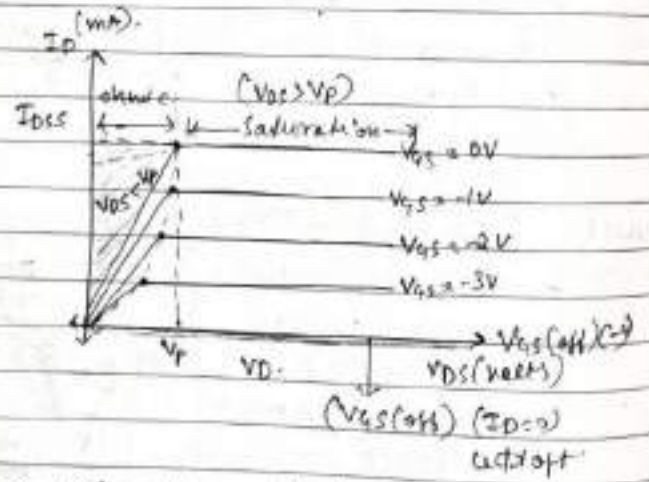
Applying the voltage at V_{GS}, I_D will be lower as compare to $V_{GS}=0$ and the pinch off occurs for lower V_{DS} (voltage Drain to source)



$V_{GS} = V_{GS(off)}$ = the value of V_{GS} at which $I_D = 0$

MARK (P) IMPORTANT

(Jfet output characteristics curve) OR (DRAIN O/P CURVE) # [N-channel]



- it is a plot between I_D & V_{DS} for different values of V_{GS}.
- Curve has 3 sections (ohmic, saturation, cutoff region).

(i) ohmic Region:- • Region left to parabola locus is ohmic region.

- here V_{DS} is less than V_P. ($V_{DS} < V_P$)
- In this region Jfet is used as ~~an amplifier~~ voltage controlled resistor.
- In this region I_D depends on V_{DS}.

(ii) Saturation Region:- • Region right to parabola locus is saturation region here ($V_{DS} > V_P$).

Why voltage controlled?

- In this region Jfet is used as an amplifier
- In this region I_D depends input voltage V_{GS} hence voltage controlled device.
- Hence I_D is independent of V_{DS} & (I_D = const).

(iii) Cutoff region:- • In this region V_{GS} is equal to V_{GS} off and the curve is on the horizontal axis.

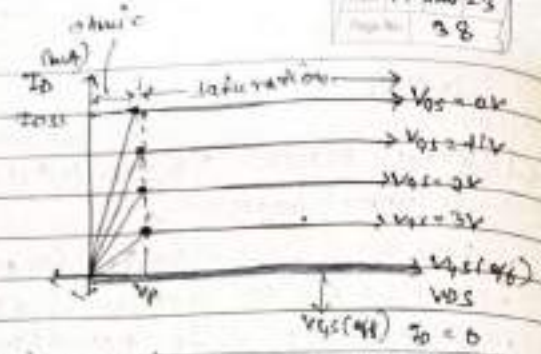
- for all values of V_{DS}, ($I_D = 0$).
- Jfet is used as open switch

(Jfet output characteristics curve) # [P-channel].

1.) it is a plot b/w I_D and V_{DS} for the different values of V_{GS}.

2.) Curve has 3 sections:-

(i) ohmic (ii) saturation (iii) cutoff region.



(i) Ohmic region:- Region left to parabola locus is ohmic region, (V_{DS} is less than V_P)

- In this region JFet is used voltage controlled resistor.
- In this region I_D depends on V_{DS}.

(ii) Saturation region:- • Region right to the parabola locus is saturation region here ($V_{DS} > V_P$).

- In this region JFet is used as an amplifier.
- In this region I_D depends input voltage V_{GS}. hence voltage controlled device.
- Here I_D is independent of V_{DS} and I_D is constant.

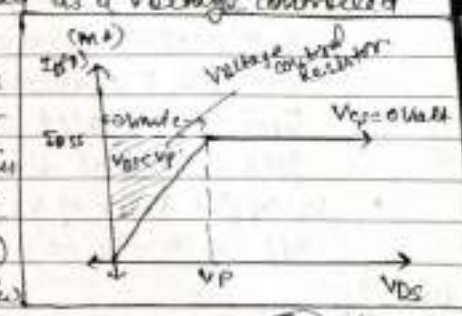
(iii) Cutoff region:- • In this region V_{GS} is equal to $V_{GS}(off)$ and the curve is on horizontal axis.

- for all values of V_{DS}, Drain current (I_D) is equal to zero ($I_D=0$)

- JFet is used as an open switch.

Imp Q: How JFet is used as a voltage controlled resistance?

Ans:- • JFet can be used as a variable resistor whose resistance is controlled by gate source voltage (V_{GS}) thus resistance b/w drain and source is controlled by (V_{GS}) in ohmic region - from the curve for ($V_{DS} < V_P$) V_{GS} becomes more (-ve) slope begins to be more horizontal which increases resistance level.



$$r_d = \frac{r_0}{\left(1-\frac{V_{GS}}{V_{GS}(off)}\right)^2}$$

- here (r_0) = JFet resistance with $V_{GS}=0$.

(r_d) = JFet resistance b/w D & S for a particular V_{GS}

(Shockley's eqn for JFet)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

- It gives relationship b/w input voltage (V_{GS}) and output current (I_D) ⇒ (Drain current b/w D & S terminal)
- I_{DSS} = Saturated current b/w D & S with gate terminal shorted with source ($V_{GS}=0$)
- $V_{GS(off)}$ = value of V_{GS} to turn the device off i.e ⇒ ($I_D = 0$)

MARK (8) IMPORTANT

(Transfer Characteristics (curve) :-
or Transconductor Curve.
for (N channel JFet) :-

1). It's a plot between I_D & V_{GS} for constant value of V_{DS}.

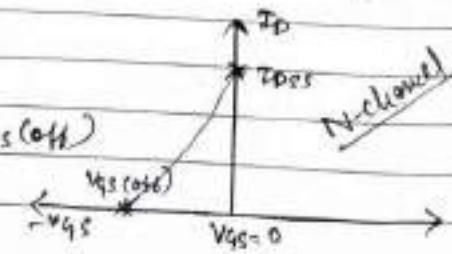
2). from shockley eqn: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$

* case (1) $V_{GS} = 0$, calculate I_D?

($I_D = I_{DSS}$)

* case (2) $V_{GS} = V_{GS(off)}$

($I_D = 0$)

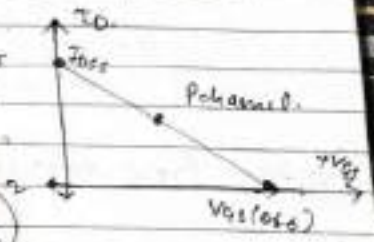


* case (3) = $V_{GS} = \frac{V_{GS(off)}}{2}$ (Non-linear)

($I_D = \frac{I_{DSS}}{4}$)

(Transfer Curve for P-channel JFet)

it's a plot b/w I_D and V_{GS} for constant value of V_{DS}.



from shockley's eqn

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

- case 1 = $V_{GS} = 0$ ($I_D = I_{DSS}$)
- case 2 = $V_{GS} = V_{GS(off)}$ ($I_D = 0$)
- case 3 = $V_{GS} = \frac{I_{DSS}}{2}$ ($I_D = \frac{I_{DSS}}{4}$)

[JFET Parameters]

(i) DC, Drain resistance = $R_D = \frac{V_{DS}}{I_D}$

(ii) AC, Drain resistance / Dynamic Resistance

$r_d = \frac{\Delta V_{DS}}{\Delta I_D}$ (constant V_{GS})

IMPORTANT

(iii) Trans conductance (g_m):-

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$

[(ohm)$^{-1}$ or Ω^{-1} (mho / siemens)]

(iv) Amplification factor (μ):-

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$

or [$\mu = g_m \times r_d$]

Question Prove that $\left[g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)\right]$?

mark (5) learn

Ans:-

Using Shockley's Equation:-

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

(differentiating wrt V_{GS})

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2 \times I_{DSS}}{V_{GS(off)}}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$$

$$g_{mo} = \frac{-2 I_{DSS}}{V_{GS(off)}}$$

mark (5) learn

Metal oxide Semiconductor

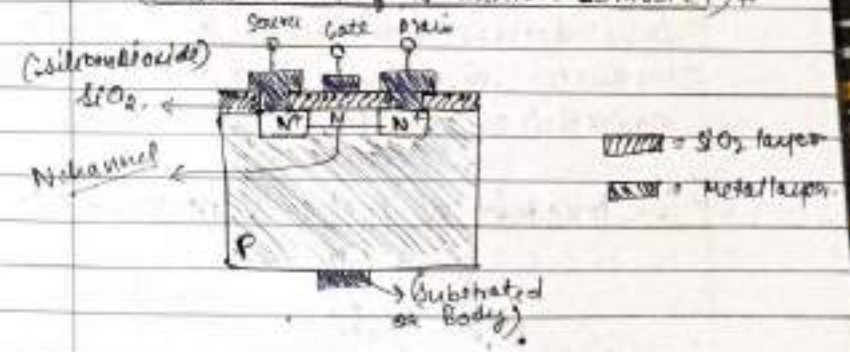
[MOSFET] # (IGFET)

- A mosfet differs from jfet in the sense that its gate terminal is electrically insulated from its gate channel. for this reason a mosfet is also known as Insulated Gate feild effect Transistor (IGFET).
- Due to insulation of Gate it input impedance is extremely high.

* (Types) *

- (Depletion MOSFET)
  - N Channel
  - P channel
- (Enhancement MOSFET)
  - N Channel
  - P channel

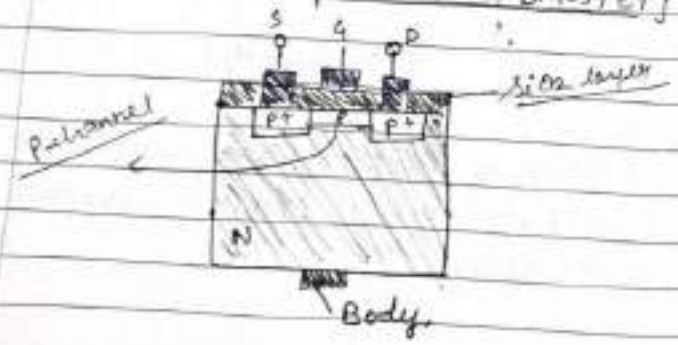
(Construction of N channel DMOSFET)



* A block of P type silicon forms the body or substrate which provides support to the device.

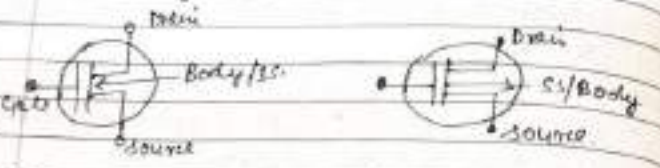
- 2 heavily doped type(N) regions are created in this P type substrate
- B/w 2 (N^+) regions there is lightly doped N type region which makes channel.
- A thin layer of silicon dioxide is deposited along the surface.
- Drain or source (metal contact at 2(N^+) regions forms drain & source of the device).
- Metal deposited on SiO_2 layer opposite to channel (gate terminal) is made by it.
- While going from gate to channel we come across metal oxide and semi-conductor in the sequence that why we named it as mosfet.

Construction of P-channel MOSFET :-



- A block of N type silicon forms the body or substrate which provides supports to the device.
- 2 heavily doped P type regions are created in this N type substrate.
- B/w 2(P^+) regions there is lightly doped P type region which makes channel.
- A thin layer of silicon dioxide is deposited along the surface.
- Metal contact at 2(P^+) regions forms drain source of the device
- Metal deposited on SiO_2 layer opposite to channel (gate terminal) is made by it.
- While going from gate to channel we come across metal oxide and semiconductor in the sequence that why are named it as mosfet.

DMOSfet E MOSfet

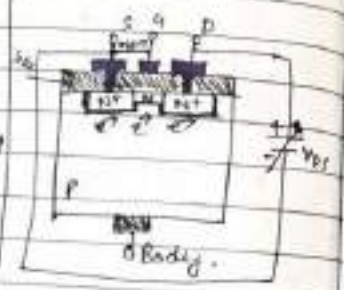


(N-channel DMOSfet) (P-channel DMOSfet)

[Working of N-channel DMOSfet]

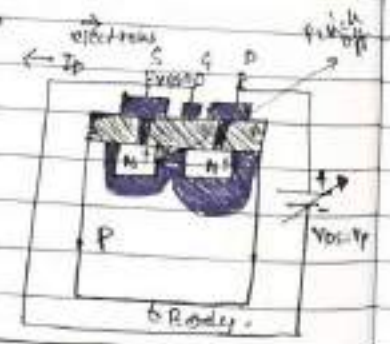
CASE I: $V_{GS} = 0$ & V_{DS} is applied.

* when the gate is shorted with source ($V_{GS} = 0$) and V_{DS} applied on increasing V_{DS}, I_D (↑) linearly.
* Symetric depletion layer forms here.



CASE 2: Pinchoff Condition :-

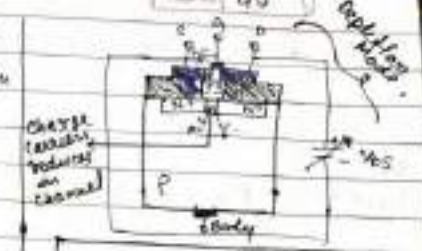
* As V_{DS} increases the channel becomes narrow at the drain and & V_{DS} reaches to pinch off Voltage the current becomes constant (I_{DSS}) and channel gets pinched off.



$V_{GS} = 0$ ($V_G = V_S$) source & gate shorted hai.

CASE 3:- When V_{GS} is -ve :-

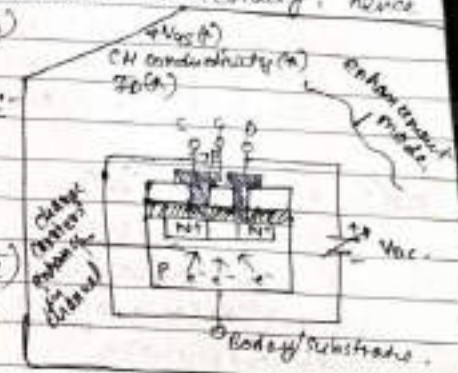
when V_{GS} is less than zero, an electric field is induced which repels the majority charge carriers (for e) away from the channel thus depletion of free e from channel that reduces conductivity. hence drain current (I_D)



$-V_{GS}$ (↑) = conducting (↓) = I_D (↓)

CASE 4: When V_{GS} is +ve :-

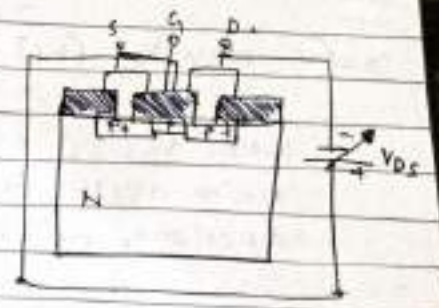
when ($V_{GS} > 0$) an electric field is induced which attracts electrons (e) into channel from P-type substrate. which increases, conductivity of channel so as a result I_D increases.



(Working - Pchannel DMOSfet)

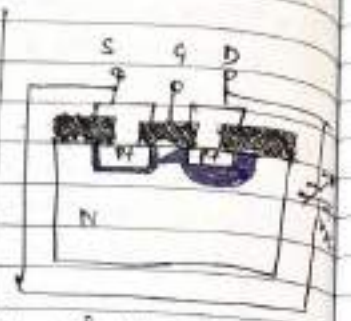
CASE I $V_{GS} = 0$
V_{DS} is applied.

* Symetric depletion will be formed.



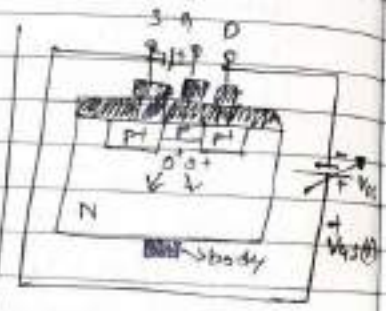
where the gate is shorted with source ($V_{GS}=0$) and V_{DS} is applied on increasing V_{DS}, I_D increasing linearly.

case (2) Pinchoff condition :-



As the V_{DS} (+) channel become narrower drain end & V_{DS} reaches to pinch off voltage the current becomes constant (I_{DSS}) and channel gets pinched off

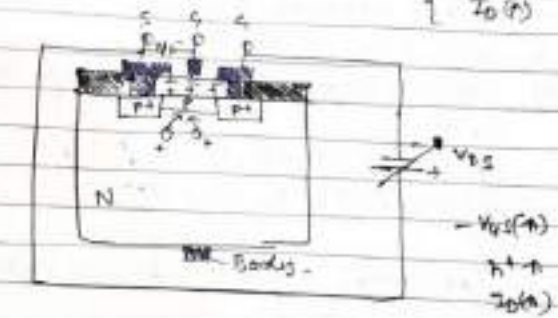
case (3) when V_{GS} is (+ve) :-



when $V_{GS}>0$, electric field is induced which repels holes away from the channel thus depletion of holes from channel that reduces conductivity of channel so as a result Drain current (I_D) decreases.

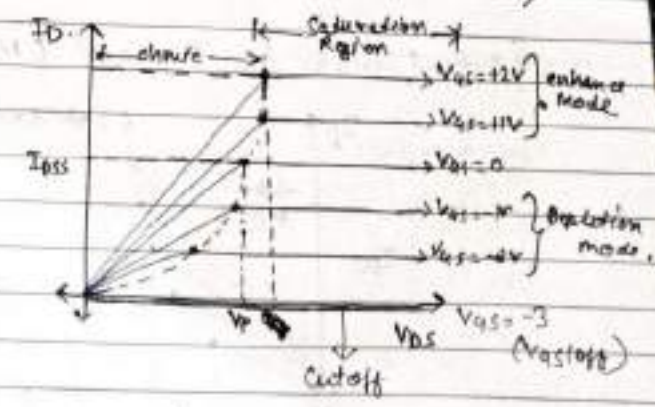
case (4) when V_{GS} (-ve) (negative) :-

when $V_{GS}<0$, an electric field is induced which attracts holes into channel thus depletion of holes of channel, so as a result Drain current I_D increases. $\left\{ \begin{array}{l} -V_{GS}(+) \\ \text{(conductivity ↑)} \\ I_D(+) \end{array} \right.$



-: (Output curve for N channel DMOSFET) :-

O/P curve OR DRAIN CURVE.



- it is a plot b/w V_{DS} & I_D for different values of V_{GS} the characteristics are same as for N-

channel JFET with only difference that in DMOSFET the curves are for both the +ve values of V_{GS}.

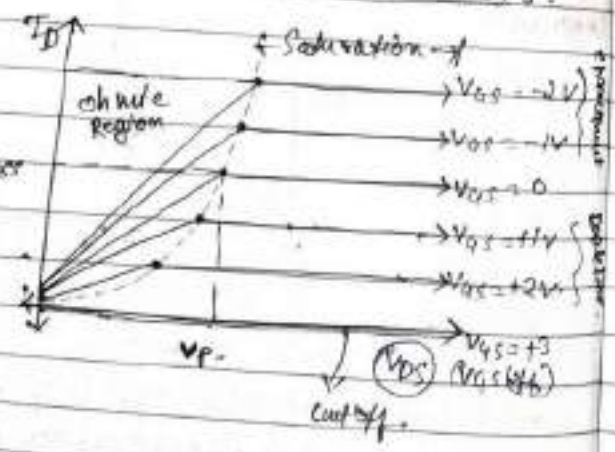
- Curve has 3 regions.

(i) ohmic region:- • region left to parabola locus.
- I_D depends on V_{DS}.
- As V_{DS} (↑) I_D also (↑)

(ii) Saturation region:- region right to parabola locus.
- I_D dependence over V_{DS} is nomore but it depends on V_{GS}.
- I_D is constant.

(iii) Cut off region:- • when $V_{GS} = V_{GS(off)}$, $I_D = 0$

:{Output curve for P-channel DMOSFET}:-



(1) It's a plot b/w I_D & V_{DS} for different values of V_{GS}. The characteristics are same as P-channel JFET as only difference that in DMOSFET the curves are for both the +ve values of V_{GS}

Figure has 3 regions:-

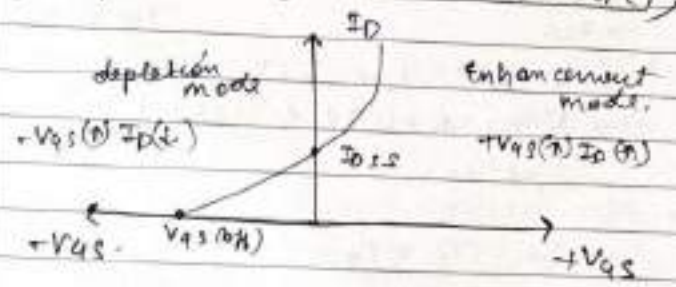
* ohmic region: • region left to parabola locus.
- It's I_D depends on V_{DS}
- As V_{DS} increases I_D also increases.

* Saturation region: • region to parabola locus
- I_D independent on V_{DS} and depend on V_{GS}.
- I_D remains constant.

* Cut off:- • when $V_{GS} = V_{GS}(off)$, $I_D = 0$
- region exist on horizontal axis.

20/JAN/2023

:(Transfer Curve for N-channel DMOSFET):-



$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

- it's a plot b/w I_D & V_{GS} for constant values of V_{DS} according to shockley's eqn.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$

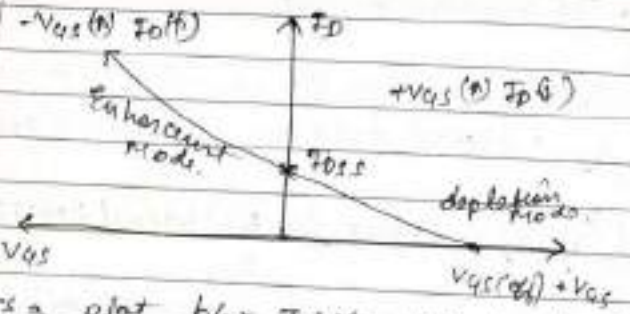
(i) $V_{GS}=0$; $I_D = I_{DSS}$

(ii) $V_{GS} = V_{GS(off)}$ (-ve) ; $I_D = 0$

$+V_{GS} \rightarrow$ Enhancement

$-V_{GS} \rightarrow$ Depletion mode.

Transfer Curve for P channel DMOSFET :-



- it's a plot b/w I_D & V_{GS} for constant values of V_{DS} according to shockley's equation.

$$I_D = I_{DSS}\left(\frac{1-V_{GS}}{V_{GS(off)}}\right)^2$$

$I_D = I_{DSS}$

channel ki depletion DMOSFET
Dmode / Emode.
Done ho kaam krta hai

EMOSFET → channel physically Absent.

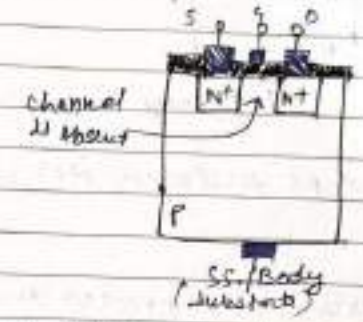
$+V_{GS} \rightarrow$ Depletion Mode, $-V_{GS} \rightarrow$ Enhancement mode.

Enhancement MOSFET :-

There are 2 types of EMOSFET :-

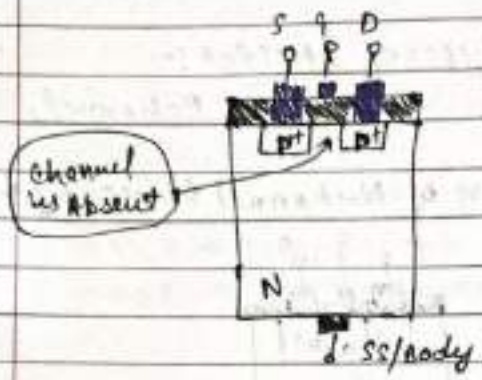
1) N channel 2) P channel.

[Construction of N-channel EMOSFET] :-



- A slab of P type semiconductor is used as SS/Body
- the drain and source terminals are connected to the (N^+) doped regions through metal contact.
- CHANNEL IS PHYSICALLY ABSENT HERE!
- SiO_2 layer is present which isolates gate terminals from the substrate.
- The construction is very similar to that of depletion type of mosfet the only difference is that channel is absent

(Construction of P-channel EMOSFET)



1) • A slab of N type semiconductor is used as SS/Body.

2) • Drain & source are connected to (P+) regions through metal contact.

3) • CHANNEL IS ABSENT HERE.

4) • SiO_2 layers insulates metals (gate terminal) from N type substrate/Body.

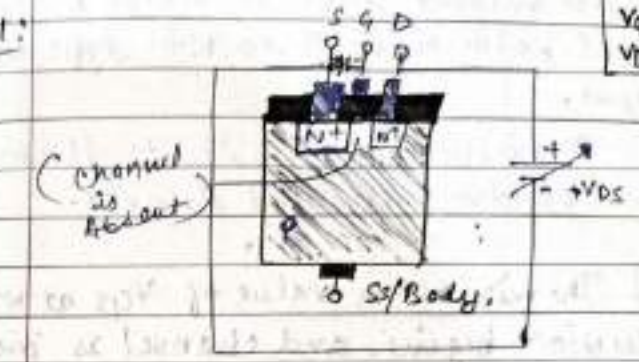
5) • The construction is very similar to that of (DMOSFET) the only difference is that channel is absent here.

D → R/W
S → S/W

(Working of N-CH. EMOSFET)

case1:

$V_{GS} = 0$
V_{DS} applied
$I_D = 0$

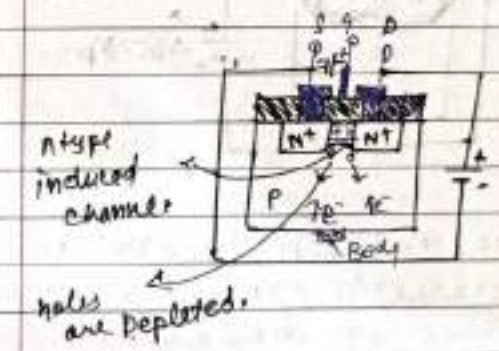


* If $V_{GS} = 0$ and (+ve) voltage is applied b/w drain & source then due to absence of N type channel I_D will be zero.

case2: if $V_{GS} > 0$ (+ve value)

V_{th} = Threshold voltage

$+V_{GS}$
Channel creates.



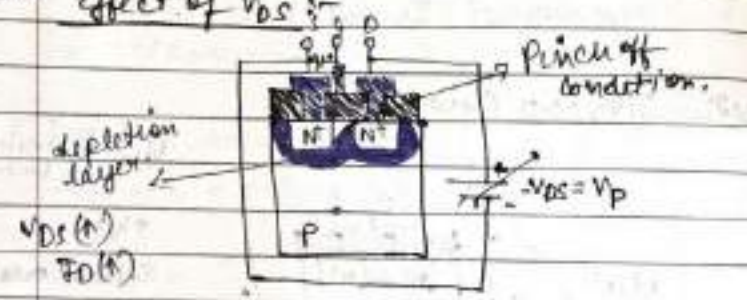
When V_{GS} = +ve, positive terminal of Gate will repel holes present in p type substrate. and e⁻ from p type substrate will be attracted towards gate terminal. and gather near the surface of SiO_2 layer.

As V_{GS} increases e^- concentration increases to such amount that it creates N-type channel which connects to (N+) type doped regions.

- Now Drain Current (I_D) starts flowing through the induced channel.

- (V_{th}:) The minimum value of V_{GS} at which conduction begins and channel is induced is known as threshold Voltage (V_{TH}) for EMOSFET.

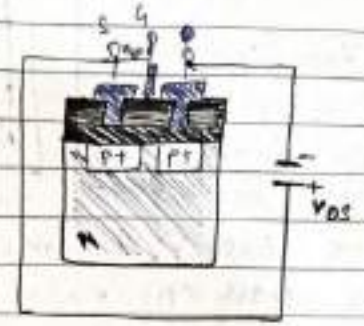
Case3: Effect of V_{DS} :-



* if ($V_{GS} > V_{th}$) and capped constant and V_{DS} increasing gradually the induced channel becomes narrow at drain end.

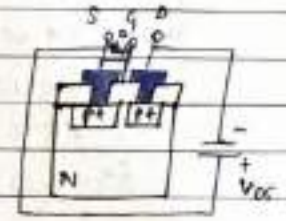
* if (V_{DS}) increases the channel width will be reduced to a point of pinch off and a saturation condition will be established & current (I_D) becomes constant.

(Working of P-CH EMOSFET)



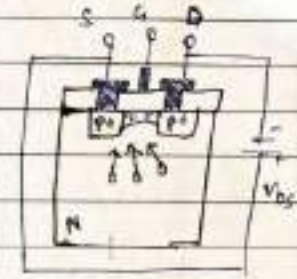
Case1: when $V_{GS} = 0$

if $V_{GS} = 0$ & -ve voltage is applied b/w drain & source then due to the absence of P-type channel. I_D will be zero.



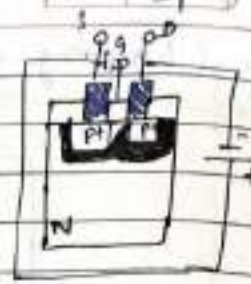
Case2: when (-ve) V_{GS} applied

when V_{GS} is (-ve), (-ve) terminal of Gate will repel i-present in n^- type substrate & holes from n-type substrate will be attracted towards gate terminal & gather near the surface of SiO_2 layer.



- As (-ve) V_{GS} increases holes concentration increases to such amount that it creates p-type channel which connects two p^+ type doped region.
- Now drain current starts flowing through the induced channel.
- The minimum value of (-ve) V_{GS} at which conduction begins & channel is induced known as (V_{TH}) for EMOSFET.

case ③ Effect of V_{DS}:-

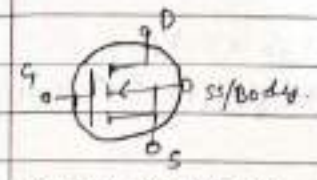


* If $V_{DS} > V_{TH}$ (threshold voltage) & kept constant & if V_{DS} increases gradually the induced channel becomes narrower at the drain (D) end.

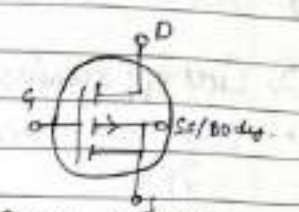
* if V_{DS} increases the channel width will be reduced to a point at which pinch off occurs, saturation condition will be established & current (I_D) becomes constant.

* V_{GS} doesn't exist on zero.

:- (Symbols) :-



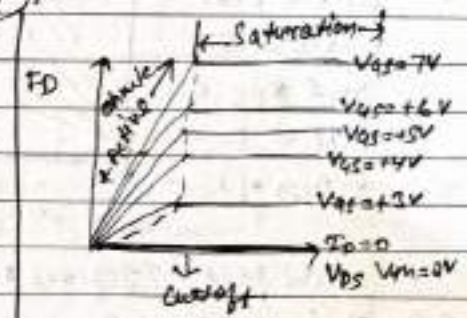
N-CH-EMOSFET.



P-CH-EMOSFET.

:- (Output curve / Drain curve for N-channel EMOSFET) :-

- It's a plot b/w I_D & V_{DS} for Diff values of V_{GS}.
- Concept of V_{GS} (Threshold voltage)



- Curve consists of 3 sections :-
  1) ohmic 2) cutoff 3) saturation.

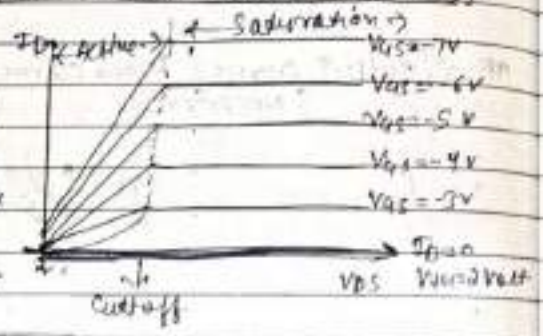
1) ohmic region :- • Region left to parabola locus
   - I_D depends on V_{DS}.
   - ⊗
2) Saturation region :- • Region right to parabola locus
   - I_D is independent of V_{DS}, but depends on V_{GS}.

Here current remains constant

③ Cut off region:- ($V_{GS} <= V_{TH}$)

- here $V_{GS} <= V_{TH}$ and for this section $I_D = 0$.

{Output curve / Drain Curve (P-CH- EMOSFET)}:-



- it's a plot between I_D and V_{DS} for Different values of V_{GS}.

- curve have 3 regions:-

(1) Ohmic region:- • Region left to the parabola in the given curve.

- it depends on V_{DS}.

(2) Saturation region:- • Region right to parabola is called saturation region.

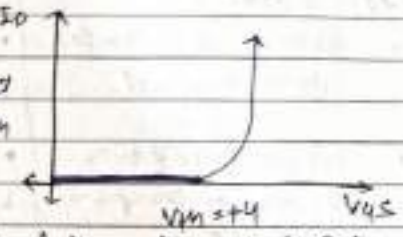
- I_D is independent on V_{DS}, but depends on V_{GS}. here current I_D remains constant

Transconductance = $\frac{1}{\text{resistance}}$ = ohm^{-1}

(3) Cutoff region:- $V_{GS} \le V_{TH}$, $I_D = 0$

- region exists on horizontal axis

{Transfer curve for N-channel EMOSFET}:-

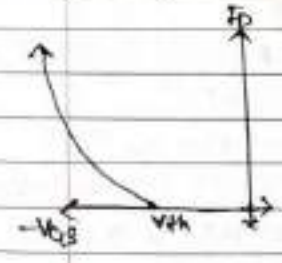


- it's a plot b/w I_D and V_{GS} for constant V_{TH} and for [$V_{GS} < V_{TH}$ $I_D = 0$]

Note:- This device doesn't follow Shockley's Eqn. it follows similar square law relationship

$$\boxed{I_D = k(V_{GS} - V_{TH})^2}$$

{Transfer Curve for P-channel EMOSFET}#



- it's a plot b/w drain current (I_D) and V_{GS} for constant (V_{TH}) Threshold voltage. for $V_{GS} < V_{TH}$, Drain Current (I_D) = 0.

Note:- This device doesn't follow shockley's equation

- it follows similar square law relationship

Same Question

Diff b/w ① Jfet/Mosfet.
② EMOSfet/DMOSfet.

$$I_D = k(V_{GS} - V_{TH})^2$$

Q: Difference b/w (Jfet, Mosfet)

(i)

(Jfet)	(Mosfet)
• Gate is not insulated from channel	• Gate is insulated from channel.
• input impedance is low on compare of MOSFet.	• Input impedence is higher than Jfet.
• operates in depletion mode	• operates in both Depletion and enhancement mode.

(ii)

(EMOSfet)	(DMOSfet)
• Physical channel is absent.	• physical channel is present.
• operates only in enhancement mode.	• operates in both depletion & enhancement
• It is normally on mode.	• normally an off device.

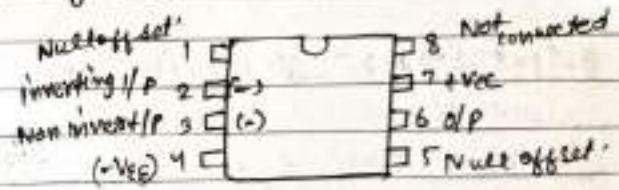
UNIT-3 (OP-AMP)

(Unit-3) (Operational Amplifier) 741 (Op-Amp)

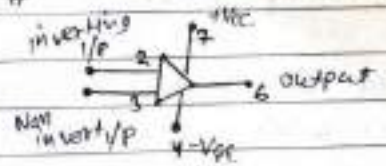
Q. what do you mean by op-Amp. why is it so?

Ans: it can perform diff types of arithmetic operation, like Add, subtract, integrate, differentiate etc. On signals applied to I/P that's why it is called op Amp.
It's called Amplifier due to its Amplifying characteristics.

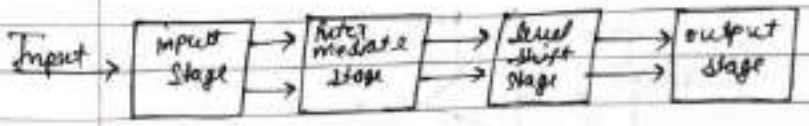
(PIN diagram)



(Symbol)



:- (Block Diagram) :-



① **Input Stage:** – It provides most of the voltage gain of amplifier & also establish input resistance of Op-Amp.

- It is a dual input balance o/p circuit.

② **Intermediate Stage:** – It increases overall gain of the op-Amp.

- It is a dual input unbalanced o/p circuit.

③ **Level Shifting Stage:** – It shifts the DC level to 0V wrt ground.

- Ammeter follower constant current source

④ **Output Stage:** – It provides low output resistance.

- Complimentary symmetry push pull amplifier.

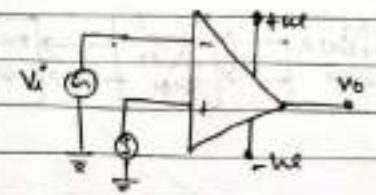
Imp

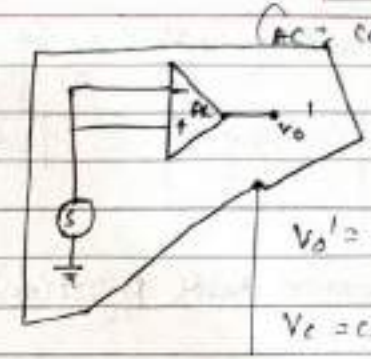
(Mode of Operation of An Op-Amp)

There are two modes of operations

1) common mode 2) Differential mode

1) (#) (Common Mode) #





$\frac{V_1+V_2}{2} = V_c$

(common Mode input)

V_o' = common mode o/p

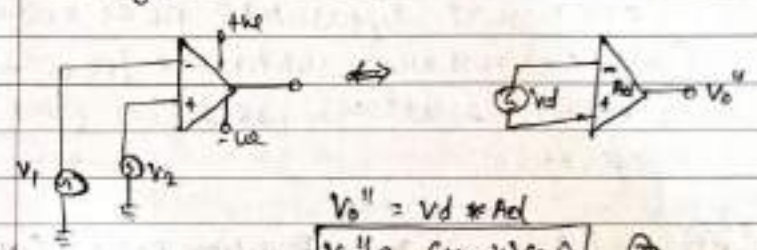
V_c = common mode input.

Ac = common Mode gain

$V_1+V_2/2$

$[V_o' = V_c * A_c]$ — ①

② # (Differential Mode) #



$V_o'' = V_d * A_d$

$\boxed{V_o'' = (V_2 - V_1)(A_d)}$ — ②

V_d = diff input $(V_2 - V_1)$

A_D = diff mode gain.

* Since op-Amp work in both mode simultaneously resultant output of op-Amp will be.

$\boxed{V_o = V_o' + V_o''}$

$V_o = V_o' + V_o''$

$V_o = V_c A_c + V_d A_d$.

$$V_0 = V_d A_d \left[1 + \frac{V_c}{V_d} \cdot \frac{A_c}{A_d} \right] \quad \text{--- (3)}$$

Here, $\boxed{V_c = \frac{V_1 + V_2}{2}}$ $\boxed{V_d = V_2 - V_1}$

(common Mode Rejection)

- In common mode operation error of both input signal will be added up to form common input voltage (V_c).
- It will result the output with more error wrt differential mode operation. (where errors are subtracted from each other), that why we reject (CMR) operations.

VIMP Mark (5)

(Common Mode Rejection Ratio) (CMRR)

CMRR is the ratio of Differential mode voltage gain (A_d) and common mode voltage gain (A_c)

$$\boxed{CMRR = \frac{A_d}{A_c}}$$

For ideal op-Amp,
CMRR = ∞
(1) $A_c = 0$

$\boxed{\text{ideal OP-Amp. } A_c = 0, \; CMRR = \infty}$

* CMRR in Decibels :- $= 20 \log_{10} (CMRR)$

$= 20 \log_{10} (A_d / A_c)$

So from eqn (3) we have :-

VIMP

$$\boxed{V_0 = A_d V_d \left[1 + \frac{1}{CMRR} \times \frac{V_c}{V_d} \right]}$$

Here, A_d = differential Mode gain
V_d = differential input → $(V_2 - V_1)$
V_c = common mode input → $\left(\frac{V_1 + V_2}{2}\right)$

25/Jan/2023

Q.1) Two input signal of 240 mV & 180 mV are now applied to an op Amp having differential mode voltage gain and CMRR as 10^6 & 120 dB respectively. Find o/p voltage of op Amp?

Ans:- $CMRR(dB) = 20 \log_{10} (CMRR)$
$120 = 20 \log_{10} (CMRR)$
$6 = \log_{10} (CMRR)$

$V_1 = 240 mV$
$V_2 = 180 mV$
$A_d = 10^6$
$CMRR = 120 dB$

$CMRR = 10^6$

$V_c = \frac{V_1 + V_2}{2} = \frac{(240+180)}{2} mV = 210 mV$

$V_d = V_1 - V_2 = (240 - 180) mV = 60 mV$

$V_0 = A_d V_d \left[1 + \frac{1}{CMRR} \times \frac{V_c}{V_d} \right]$

$V_0 = 10^6 \times 60 \times 10^{-3} \left[1 + \frac{1}{10^6} \times \frac{210}{60} \right] = 60000.21$ Volts.

Ques:2 Determine the output Voltage for Input voltage of:-

$V_{i_1} = 150\,\mu V$

$V_{i_2} = 140\,\mu V$, The amplifier has diff gain of 4000 & the value of CMRR is:-

(a) 10^2 (b) 10^5

Ans:- $V_d = 150 - 140 = 10\,\mu V$

$V_c = \frac{150+140}{2} = 145\,\mu V$

(CMRR = 10^2)

case:- (a)

$V_0 = 4000 \times 10 \times 10^{-6} \left[1 + \frac{1}{10^2} \times \frac{145}{10}\right]$

$= 45.8 \times 10^{-3}$

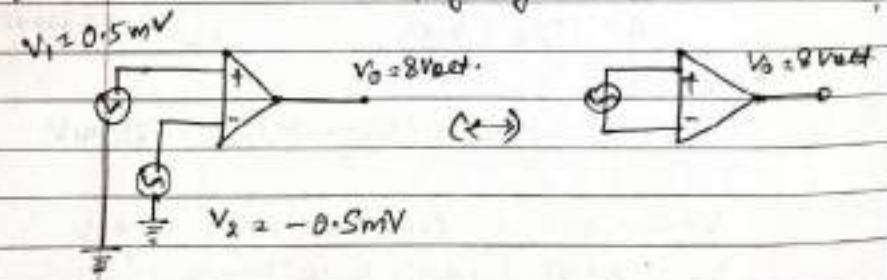
$= (45.8\,mVolt)$

case:- (b)

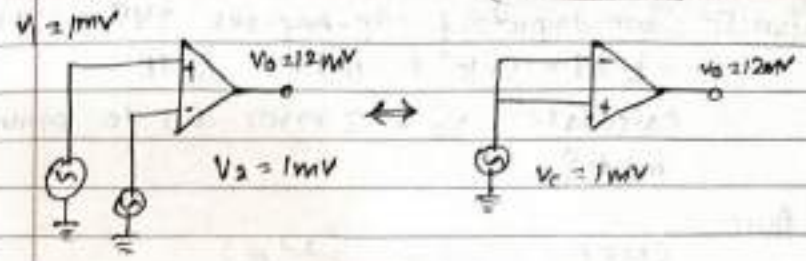
$V_0 = 4000 \times 10 \times 10^{-6} \left[1 + \frac{1}{10^5} \times \frac{145}{10}\right]$

$= (40.0006\ m\ Volt)$

Ques.3:- Calculate CMRR for given circuit measure?



(Common Mode)



Sol:- $A_d = \frac{8}{1 \times 10^{-3}} = 8 \times 10^{+3}$

$A_c = \frac{V_0}{V_c} = \frac{12 \times 10^{-3}}{1 \times 10^{-3}} = 12$

$CMRR = \frac{A_d}{A_c} = \frac{8000}{12} = 666.667 = 666.7$

$(CMRR)\,dB = 20 \log_{10} (666.7)$
$= 56.48\,dB$

Ques 4:- find the output voltage of an Op-Amp where differential gain is 10^3 common mode rejection ratio is 1000 & input voltage are $10\,\mu V$ & $20\,\mu V$

Ans:- $A_d = 10^3$, CMRR = 1000

$V_1 = 20\,\mu V$, $V_2 = 10\,\mu V$

$V_c = \frac{20+10}{2} = \frac{30}{2} = 15\,\mu V$

$V_d = 20 - 10 = 10\,\mu V$

$V_0 = 10^3 \times 10 \times 10^{-6} \left[1 + \frac{1}{10^3} \times \frac{15}{10}\right]$

$(V_0 = 2.538\ Volts)$

Ques:5:- Two inputs of op-Amp are 745 μV, 740 μV & $A_d = 5\times10^5$ & CMRR = 80 dB calculate V_o & % error due to common mode?

Ans:-

$$CMRR = 20\log_{10}\left(A_d/A_c\right)$$

$$= 20\log_{10}\left(5\times10^5/A_c\right)$$

$$4 = \log_{10} CMRR \cdot \left(\frac{5\times10^5}{A_c}\right)$$

$$10^4 = \frac{5\times10^5}{A_c}$$

$$\boxed{A_c = 50}$$

$$V_d = V_1 - V_2 = 5\,\mu V$$

$$V_c = \frac{V_1+V_2}{2} = 742.5\ \mu V$$

$$V_o = A_d V_d + A_c V_c$$

$$V_o = \left[5\times10^5\times5\times10^{-6}\right] + \left[A_c 742.5\times10^{-6}\right]$$

$$V_o = \left[5\times10^5\times5\times10^{-6}\right] + \left(50\times742.5\times10^{-6}\right)$$

$$V_o = 2.53 \text{ volts}$$

$$\%\ \text{error} = \frac{A_c V_c}{V_o}\times100$$

$$= \frac{50\times742.5\times100}{2.53} = \frac{0.037\times100}{2.53}$$

$$= 1.46\%$$

(i) (Slew Rate) (SR)

Maximum rate of change in o/p voltage is defined as slew rate.

$$\boxed{S.R = \left.\frac{dV_o}{dt}\right|_{max.} \qquad \text{unit} = \text{volt}/\mu\text{sec}}$$

(ii) for ideal op Amp $S.R = \infty$

* Band Width:- it is known as range of frequency & for ideal op Amp is ∞.

23/01/2023

(iii) Offset Voltage:- (ideal op Amp me zero)

There are 2 types of offset voltage.
1) output offset voltage (V_{OOC})
2) input offset voltage (V_{IOC})

1) (Output offset Voltage)
A very small amount of voltage occurs at output (Due to internal leakage current) even there is no input signal, this voltage is known as output offset voltage.

* for ideal op Amp:- $V_{OOC} = \text{zero}$

* in ideal op amp: $R_i = \infty$, $R_o = 0$ to prevent loading effect.

$R = \infty$, ckt = open.

op amp = $I = 0$

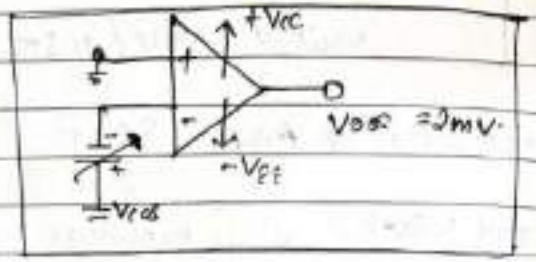
Hard water
• [illegible]

Soft water
• [illegible]

(iii) Input offset voltage (V_{IOS}).

To nullify an output offset voltage, a reverse amount of voltage is applied to input this voltage is known as (V_{IOS}).

* for ideal op amp = $V_{IOS} = 2 \times 40$



(Power supply rejection ratio)
* (PSRR) *

* It is a degree of dependence of output on the change in power supply voltage.

* it is ratio of change in I/p offset voltage to the change in supply voltage.

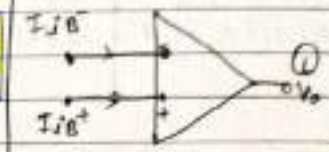
$$PSRR = \frac{\Delta V_{IOS}}{\Delta V}$$

* for ideal op amp = $PSRR = 0$

(Bias current compensation)

(i) Input Bias current :-

$$I_{iB} = \frac{I_{iB}^- + I_{iB}^+}{2}$$



* it is defined as algebraic mean of both input currents

* for ideal op amp :-

$$I_{iB}^- = I_{iB}^+ = 0$$

$$I_{iB} = 0$$

input Bias current

(ii) Offset current :- difference of both currents.

$$I_{IOS} = |I_{iB}^+ - I_{iB}^-|$$

VIMP Part B

(ideal op amp characteristics)

	Characteristics	Symbol	Ideal value	Practical value
1	Voltage gain	A_v	∞	2×10^5
2	I/p impedance	R_i, Z_i	∞	$2\ M\Omega$
3	o/p impedance	R_o, Z_o	0	$75\ \Omega$
4	CMRRatio	CMRR	∞	90dB
5	Slew rate	S.R	∞	0.5V/micro sec
6	Band width.	BW	∞	1MHz

* Difference of V_1 & V_2 is Amplified by Op Amp.

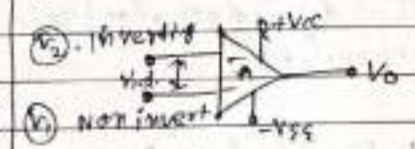
	Characteristics	Symbol	Ideal value	Practical value
(7)	Power supply Rejection ratio	PSRR	0	150 μV/V (micro volt)
(8)	Offset voltage	V_{OOS}	0	2 mV
(9)	Offset current	I_{iOS}	0	6 nA (nano Amp)

(Concept of OP Amp)

Not for 17-2

$V_o = A\,V_{id}$.

$V_o = A(V_1 - V_2)$



* Op Amp has 2 input terminals.
(i) (-ve) = inverting i/p terminal.
(ii) (+ve) = non-inverting i/p terminal.

* Inverting means output with a phase shift of 180°

* Non-inverting means output with a zero phase shift.

* Op Amp Amplifies the difference between voltages applied non-inverting input & inverting input if its gain is (A) o/p is given by:-

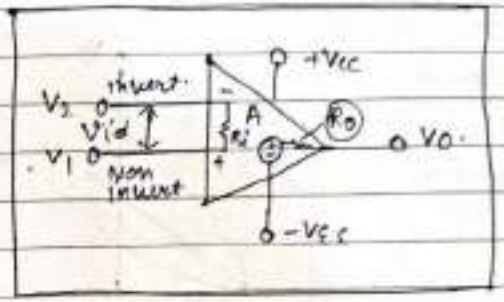
$V_o = A \cdot V_{id}$

$V_o = A(V_1 - V_2)$

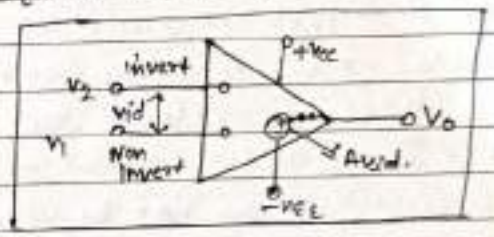
(Practical op Amp)

* VVIP important for 15-2

(Equivalent ckt of op Amp) # Mark (6)



(Equivalent ckt for ideal op Amp)



$V_o = A(V_{id}) \Rightarrow A(V_i - V_{ii})$

$R_i = \infty$ (replaced by open ckt)

$R_o = 0$ (Replaced by short ckt).

30 JAN 2023

Q. Difference between open loop and closed loop configuration?

Ans: close loop mean there is a feedback connection b/w input & output open loop mean there is no feedback connection b/w Input & O/p.

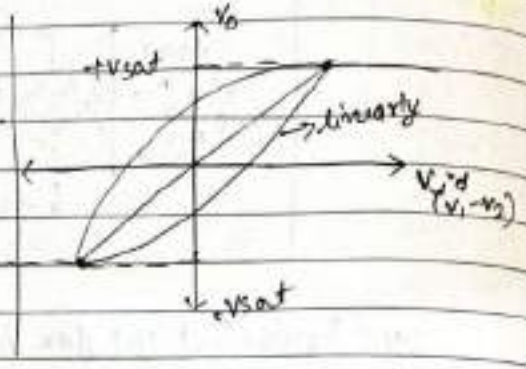
(limitation/drawback of open loop configuration)

$V_o = A v_{id}$

$= A(V_1 - V_2)$

A = open loop gain

$= \infty$



It's gain is so high that its too unstable to be useful here A (open loop gain) is very large for voltage level slightly greater than 0 the output is driven into saturation so can not be used in linear applications.

VIMP

(closed loop op-Amp configuration)

There are three types of configuration:-

(i) inverting Amplifier configuration.

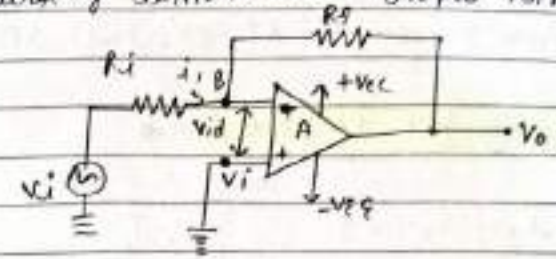
(ii) Non-inverting Amplifier configuration.

(iii) Differential Amplifier configuration.

(i) (Inverting Amplifier Configuration)

→ Here input is applied at inverting (-ve) terminal & non-inverting (+ve) terminal is ground.

→ There is a feedback connection b/w the inverting terminal and output terminal.



→ for op-Amp we know that

$V_o = A v_{id}$

$V_o = A(V_1 - V_2)$

* for ideal op-Amp

$A = \infty = \frac{V_o}{V_1 - V_2}$

$V_1 - V_2 = 0$ → (virtual short condition) (IMP)

$(V_1 - V_2) = 0$ eq

from eq ① as potential difference is zero b/w the 2 terminals thus a virtual short circuit exist b/w the 2 i/p terminals.

* from circuit $V_1 = 0$ (Terminal is grounded)

so from eq ①, we have (IMP)

$(V_1 = V_2 = 0)$ → ② → (virtual ground condition)

Virtual ground means that the terminal is not connected to the ground actually even then the voltage at terminal is 0

* (Apply KCL at node B) *

$i_1 = i_2 + i_3$ $(\because i_2 = 0$

$i_1 = i_3$ (op-Amp doesn't draw any current)

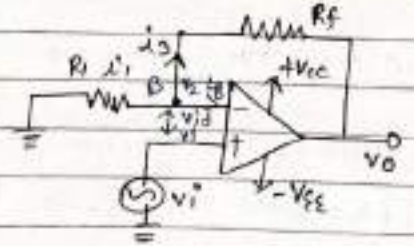
$$i_1 = \boxed{\frac{V_1 - V_2}{R_1} = \frac{V_2 - V_0}{R_f}} = i_3$$

As we know $V_2 = 0$:-

$$\boxed{V_0 = -R_f \frac{V_i}{R_1}} \qquad \boxed{\text{gain} = -\frac{R_f}{R_1}}$$

Thus inverting gain $= -\frac{R_f}{R_i}$ (-ve) sign means that opt is inverted.

(ii) (Non-inverting Amplifier Configuration)



Here input is applied at non inverting (+ve) terminal & inverting terminal is grounded through feedback.

$$V_0 = \underset{\text{open loop gain}}{A} \underset{\text{differential input}}{V_{id}}$$
$$= A(V_1 - V_2)$$

for ideal op-Amp.

$$A = \infty = \frac{V_0}{V_1 - V_2}$$

$V_1 - V_2 = 0$

$$\boxed{V_1 = V_2} \text{ — (1)}$$

Virtual short cond^n.

from circuit

$V_1 = V_i$

so from eq^n (1) we have.

$$\boxed{V_1 = V_2 = V_i} \text{ — (2) eq}^n.$$

Apply KCL at node B.

$i_1 = i_2 + i_3$ $(\because i_2 = 0$, op Amp does not draw current)

$i_1 = i_3$

$$\frac{0 - V_2}{R_1} = \frac{V_2 - V_0}{R_f}$$

Here $V_2 = V_i$ from eq^n (2)

$$\Rightarrow \frac{-V_i}{R_1} = \frac{V_i - V_0}{R_f}$$

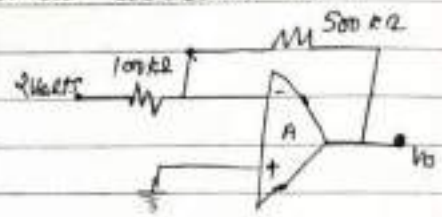
$$\Rightarrow \frac{-V_i}{R_1} = \frac{V_i}{R_f} - \frac{V_0}{R_f}$$

$$\frac{V_o}{R_f} = \frac{V_i R_f + V_i R_1}{R_1 R_f}$$

$$V_o = \frac{V_i (R_1 + R_f)}{R_1}$$

$$\boxed{V_o = \left(1 + \frac{R_f}{R_1}\right) V_i} \qquad \boxed{\text{gain} = 1 + \frac{R_f}{R}}$$

Q:- for given circuit calculate V_o.



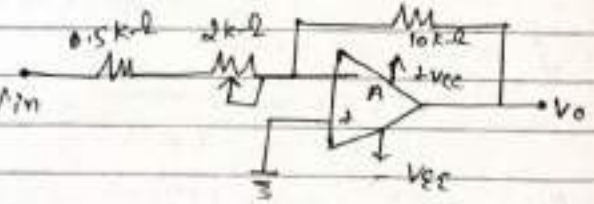
Ans

circuit is inverting :-

$$V_o = \frac{-R_f V_i}{R_1} = \frac{-500 \times 2}{100} = -10 \text{ Volts.}$$

Q:- Calculate Range of gain :-

Ans



Ans

Case I

$R_1 = 0.5\,k\Omega + 0\,k\Omega = 0.5\,k\Omega$

$R_f = 10\,k\Omega$

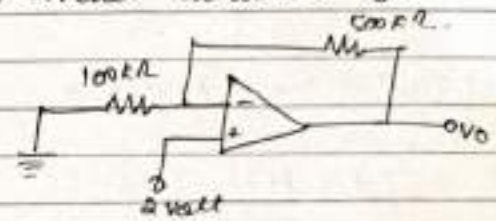
$$\text{Gain} = \frac{-10}{0.5} = -20$$

$R_1 = 0.5\,k\Omega + 2\,k\Omega = 2.5\,k\Omega$, $R_f = 10\,k\Omega$

$$\text{Gain} = \frac{-10}{2.5} = -4$$

Range = -4 to -20 Volts.

Q:- for given circuit calculate V_o.



Ans Case ①

$R_f = 500\,k\Omega$, $R_1 = 100\,k\Omega$

$$V_o = \left(1 + \frac{500}{100} \times 2\right)$$

$$= \frac{600}{100} \times 2 = 12 \text{ Volt}$$

Case ② By KCL

$V_1 = V_2$, $V_1 = V_2 = 2$ Volt.

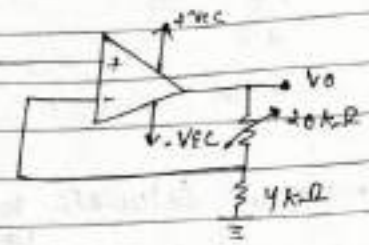
$i_1 = i_2$

$$\frac{0 - V_2}{100} = \frac{V_2 - V_o}{500.5} \qquad \therefore \boxed{V_2 = 2}$$

$$-10 = 2 - V_o$$

$$\boxed{+12 = +V_o}$$

Q:- calculate range of gain



Ans= circuit is non-inverting.

case (I)

$$R_f = 1 + \frac{20}{4} = 6$$

$$R_f = 1 + \frac{0}{4} = 1$$

Range = 1 – 6 volts

By KCL

$$V_1 = V_2$$

$$V_1 = V_2 = V_{in} \quad , \; i_1 = i_2$$

$$\frac{0 - V_2}{R_1} = \frac{V_2 - V_0}{R_f}$$

Maximum	Minimum
$\frac{0 - V_{in}}{4k\Omega} = \frac{V_{in} - V_0}{20k\Omega}$	$\frac{0 - V_{in}}{4k\Omega} = \frac{V_{in} - V_0}{0k\Omega}$
$-20V_{in} = 4V_{in} - 4V_0$	$4V_{in} = 4V_0$
$-24V_{in} = -4V_0$	$1V_{in} = V_0$
$6V_{in} = V_0$	
gain = 6	gain = 1

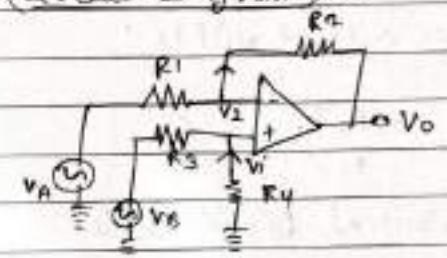
Range = 1 to 6 Volts.

VVIMP # [Differential Amplifier Configuration] #

→ A differential amplifier is a circuit which amplifies the difference between two voltages.

→ for differential amplifier voltages are applied at both input terminals.

* (Circuit Diagram) *

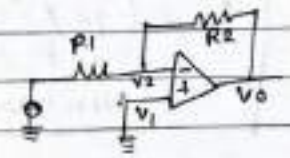


Now using superposition theorem to analyse the circuit.

CASE I : Assume $V_B = 0$.

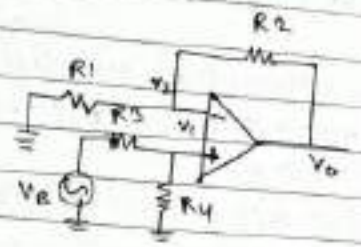
In this case circuit works as inverting amplifier so output component will be

$$V_0 = -\frac{R_2}{R_1} V_A$$



(Case II) :- Assume $V_A = 0$

In this case circuit works as non-inverting amplifier with an additional voltage divider circuit.



* In this case output will be :-

$$V_{o_2} = \left(1 + \frac{R_2}{R_1}\right) V_1 \quad \text{--- (2)}$$

using potential Divider rule.

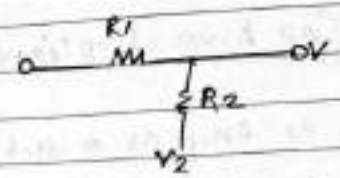
$$V_1 = \frac{V_B R_4 + 0 \cdot R_3}{R_3 + R_4} = \frac{V_B R_4}{R_3 + R_4}$$

\# from eq^n (2) $V_{o_2} = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4 V_B}{R_3 + R_4}\right)$

so the total o/p will be:-

$V_o = V_{o_1} + V_{o_2}$

$$\boxed{V_o = \underbrace{\left(1 + \frac{R_2}{R_1}\right)\left(\frac{V_B R_4}{R_3 + R_2}\right)}_{\text{Non inverting}} - \underbrace{\frac{R_2}{R_1} V_A}_{\text{Inverting}}}$$



$$V = \frac{V_1 R_2 + V_2 R_1}{R_1 + R_2}$$

Now using Voltage Divider rule

$$V_1 = \frac{V_B R_4 + 0 \cdot R_3}{R_3 + R_4}$$

$$V_1 = \frac{V_B \cdot R_4}{R_3 + R_4}$$

from eq (2).

$$V_{o_2} = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{V_B \cdot R_4}{R_3 + R_4}\right)$$

total outputs

$V_o = V_{o_1} + V_{o_2}$

$$V_o = \underbrace{\left(1 + \frac{R_2}{R_1}\right)\left(\frac{V_B \cdot R_4}{R_3 + R_1}\right)}_{\text{Non invert}}^{2} - \underbrace{\frac{R_2}{R_1} \cdot V_A}_{\text{inverting}}$$

$$V_o = (1 + R)\left(\frac{V_B \cdot R}{2 \cdot R}\right) - V_A$$

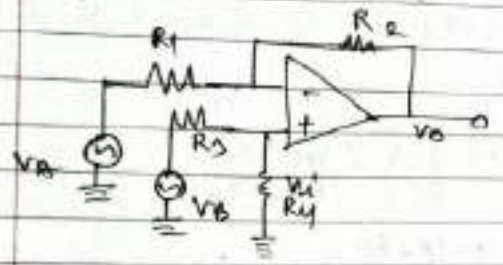
$$\boxed{V_o = V_B - V_A}$$

* Branch i_2 se jyada par potential divider nhi lagayege.

(I) * (Op Amp Applications) *

(a) **Op Amp as a subtractor** :- A subtractor is a circuit which subtracts 1 Volt from another voltage.

- A difference amplifier can be converted into a subtractor if all the 4 resistors (R_1, R_2, R_3, R_4) are same



using superposition concept.

Case ① (Assume $V_b = 0$)
inverting Amp.

$$V_{o1} = -\frac{R}{R} V_a = -V_a \quad \text{—①}$$

Case ② (Assume $V_a = 0$)
Non-inverting Amp.

$$V_{o2} = (1 + R/R) V_1 \quad \text{—②}$$

$V_1 = ?$ using KCL at (+ve) terminal
$I_1 + I_2 = 0$

+ve terminal = $i_1 + i_2 = 0$
-ve terminal =

$$\frac{V_b - V_1}{R} + \frac{0 - V_1}{R} = 0$$

on calculating :-

we get :→ $V_1 = V_b/2$

* Put value of V_1 in eqn ②

$$V_{o2} = (1+1) \times \frac{V_b}{2} = V_b$$

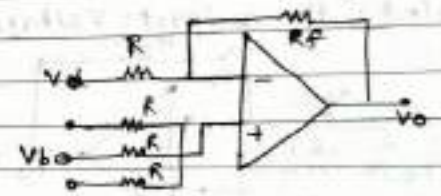
Total output

$$V_o = V_{o1} + V_{o2} = V_b - V_a.$$

∴ circuit behaves as a Subtractor.

Q:- Calculate output voltage for given circuit

VIMP



Ans:-

Case ① = Inverting Response of the ckt.

$$V_{o1} = -\frac{R_f}{R} V_d \quad \text{—①}$$

Case ② = Non inverting response of the ckt

$$V_{o2} = \left(1 + \frac{R_f}{R}\right) V_1$$

$V_1 = ?$

$I_1 + I_2 + I_3 = 0$

$$\frac{V_a - V_1}{R} + \frac{V_b - V_1}{R} + \frac{V_c - V_1}{R} = 0$$

$$V_1 = \frac{V_a + V_b + V_c}{3}$$

$$V_{o2} = \left(1 + \frac{R_f}{R}\right)\left(\frac{V_a + V_b + V_c}{3}\right)$$

Total o/p

$$V_o = V_{o1} + V_{o2}$$

$$= \boxed{-\frac{R_f}{R} V_i + \left(1 + \frac{R_f}{R}\right)\left(\frac{V_a + V_b + V_c}{3}\right)}$$

Q:- Calculate the output voltage for given

Ans:-

$I_1 = I_2$

$$\frac{0 - V_2}{3k\Omega} = \frac{V_2 + V_o}{15k\Omega} \qquad V_2 = V_1$$

$$V_o = \left(1 + \frac{R_f}{12}\right) V_i$$

$$= \left(1 + \frac{15k}{3k}\right) V_i$$

$V_1 = ?$

$$\frac{10 - V_1}{6k\Omega} + \frac{-8 - V_1}{2k\Omega} = 0$$

$V_1 = ?$ $(-7/2)$

* Now put value of V_1 in

$(6)(-7/2)$

$$\boxed{V_o = -21}$$

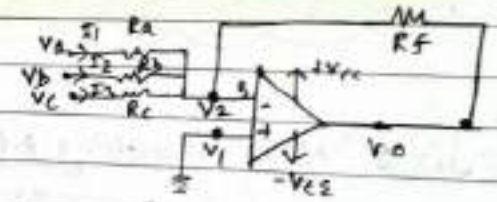
3rd Appl.

(b) (Op Amp as a adder / summing Amplifier / Summer)

An adder is a circuit whose output is equal to the sum of applied input voltages. There are two types of adder.

(i) Inverting Adder. (ii) Non-inverting Adder.

(Inverting Adder)



As we know for ideal op-Amp

$V_o = A V_{id}$.

$V_o = A(V_1 - V_2)$

Ideally.

$A = \infty = V_o / V_1 - V_2$

$V_1 - V_2 = 0$ (virtual short cond^n)

Here $v_1 = 0$

from eqn (1)

$\boxed{v_1 = v_2 = 0}$ → virtual ground condition

(KCL at Node B)

$I_1 + I_2 + I_3 = I_4$

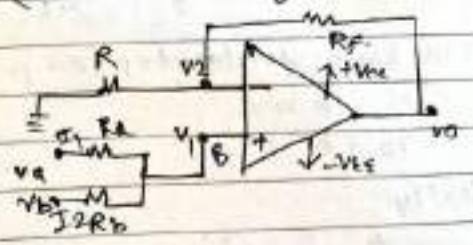
$$\frac{V_a - V_B}{R_a} + \frac{V_b - V_B}{R_b} + \frac{V_c - V_B}{R_c} = \frac{V_B - V_o}{R_f}$$

$\boxed{V_B = 0}$

$$\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c} = \frac{-V_o}{R_f}$$

$$V_o = -R_f\left[\frac{V_a}{R_a} + \frac{V_b}{R_b} + \frac{V_c}{R_c}\right]$$

(ii) # (Non inverting Adder) #



As we know for ideal op-Amp

$V_o = A V_{id}$.

$V_o = A(V_1 - V_2)$

ideally,

$A = \infty = \frac{V_o}{V_1 - V_2}$

$V_1 - V_2 = 0$

$V_1 = V_2$ → virtual short condition. (1) eqn.

This is not inverting configuration so O/P will be.

$$V_o = \left(1 + \frac{R_f}{R}\right) V_1$$

(KCL at Node B)

$I_1 + I_2 = 0$

$$\frac{V_a - V_1}{R_a} + \frac{V_b - V_1}{R_b} = 0$$

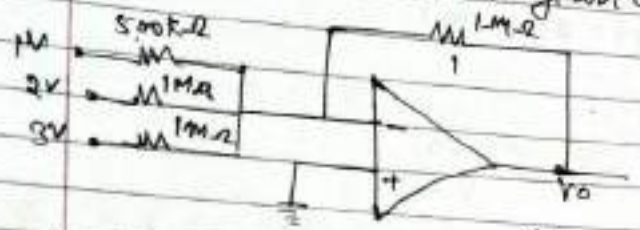
$$V_1 = \frac{V_a R_b + V_b R_a}{R_a + R_b}$$

So. Now from eqn (2)

$$\boxed{V_o = \left(\frac{1 + R_f}{R}\right)\left(\frac{V_a R_b + V_b R_a}{R_a + R_b}\right)}$$

$1M\Omega$ = 1mega ohm $\rightarrow 10^6$

Q:- (Calculate o/p voltage for given ckt)



(Inverting Adder)

Ans:- $V_0 = -R_f\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]$

$V_0 = -1M\Omega\left[\frac{1V}{500k\Omega} + \frac{2V}{1M\Omega} + \frac{3V}{1M\Omega}\right]$

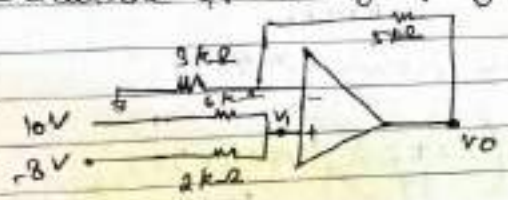
$V_0 = -10^6\left[\frac{1}{500\times10^3} + \frac{2}{1\times10^6} + \frac{3}{1\times10^6}\right]$

On solving we get:

$= -7$ volt

02/feb/2023

Q:- (calculate o/p voltage for given ckt)



Ans on pg-89

Current at $R = \frac{0-V_0}{R}$

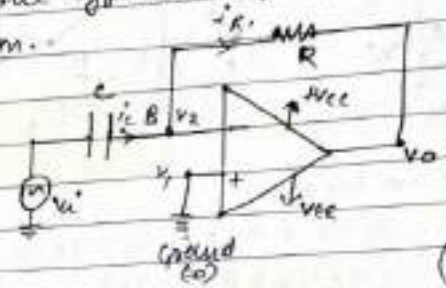
$V_1 - V_2$ = Subtractor.

$A_1V_1 - A_2V_2$ = differential.

1st APP^n

(c) (Op Amp differentiator):-

It is a circuit in which the o/p voltage waveform is the differential of input voltage waveform.



Derivation

* As we know:

$V_0 = AV_{id}$

$V_0 = A(V_1 - V_2)$

(for ideal op Amp)

$(V_1 = V_2)$

$V_1 = 0$

$V_2 = 0$

$A = \infty = \frac{V_0}{V_1 - V_2}$

$V_1 = V_2$ = (Virtual Short condition)

Here $V_1 = 0$

so $V_1 = V_2 = 0$ [virtual ground condition]

Applying KCL at node B:-

$i_C = i_R$

$C\frac{dv_c}{dt} = C\frac{d}{dt}(V_i - V_2) = \frac{V_2 - V_0}{R}$ $[\because V_2 = 0]$

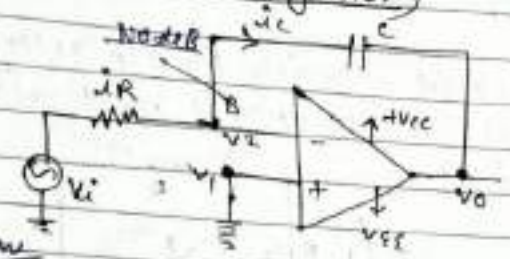
$C\,d/dt(V_i) = -V_0/R$.

$V_0 = -RC\,d/dt(V_i)$

Imp Appn

capacitor is in feedback.

#(d) (Op amp as a integrator)



Derivation

As we know

$V_0 = A V_1' d$

$V_0 = A(V_1 - V_2)$

for ideal op Amp.

$A = \infty = \frac{V_0}{V_1 - V_2}$

$\boxed{V_1 = V_2}$ (virtual short cond^n)

Same in all cases of op Amp

Here $V_i' = 0$

so $V_1 = V_2 = 0$ (virtual ground)

(Applying KCL at node B)

$i_R = i_C$

$$\frac{V_i' - V_2}{R} = C\frac{dV_c}{dt}$$

$$\frac{V_i' - V_2}{R} = C\frac{d}{dt}(V_2 - V_0) \quad (V_2 = 0)$$

gain $= \frac{dP}{1/P}$

$$\frac{V_i}{R} = +C\frac{d}{dt}(-V_0)$$

$$\boxed{\frac{-V_i}{RC} = \frac{d}{dt}(V_0)}$$

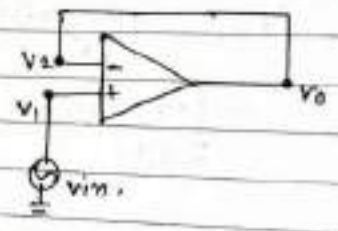
integrating both sides.

$$\boxed{-\frac{1}{RC}\int V_i\, dt = V_0}$$ Ans

(VIMP)

Appn #(e) (Op amp as Unity gain Amplifier) OR (Voltage follower) OR (Buffer Amplifier)

This circuit is called follower of voltage because the o/p voltage is equal to the input voltage and gain of the circuit is one (unity).



#① According to virtual short condition.

$V_1 = V_2$.

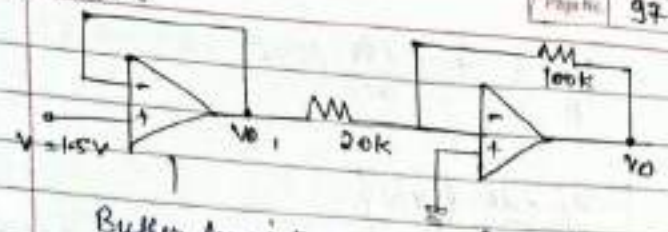
#② Here $V_1 = V_{in}$ — ①

$V_2 = V_0$ — ②

$\boxed{V_{in} = V_0}$

#③ gain $= \frac{V_0}{V_{in}} = 1$

Q: Solve it



Buffer Amplifier: Inverting Amplifier

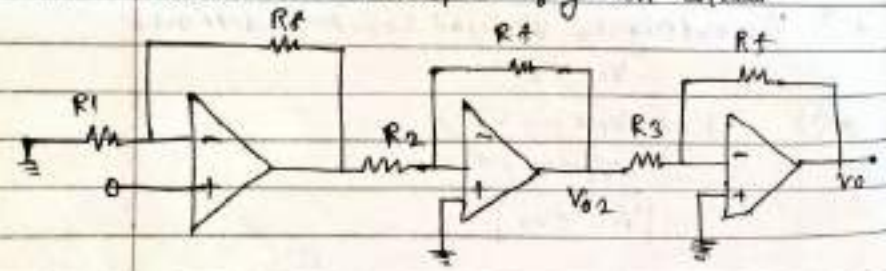
① $V_{o1} = V = 1.5V$ (As $V_{in} = V_o$)

② # [from inverting Amplifier]

$$V_o = -\frac{R_f}{R_1} v_{in} \text{ (Inverting)}$$

$$-\frac{100k}{20k} V_{o1} = \frac{-100k}{20k} \times 1.5 = -7.5 \text{ Volt}$$

Q: Calculate the output of given circuit?



Ans:- $V_o = -\frac{R_f V_{o2}}{R_3}$

$\Rightarrow \left(-\frac{R_f}{R_2}\right) V_{o1}$

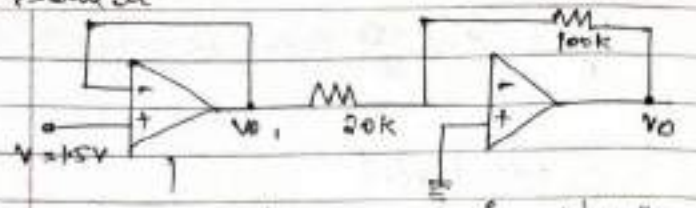
$\Rightarrow \left(-\frac{R_f}{R_1} V_1\right)$

$V_o = -\left[\frac{R_f}{R_3}\right]\left[\frac{R_f}{R_2}\right]\left[\frac{R_f}{R_1}\right] V_1$

$V_o = 1.78$ Volt.

Solve it

Q:



Buffer Amplifier: Inverting Amplifier

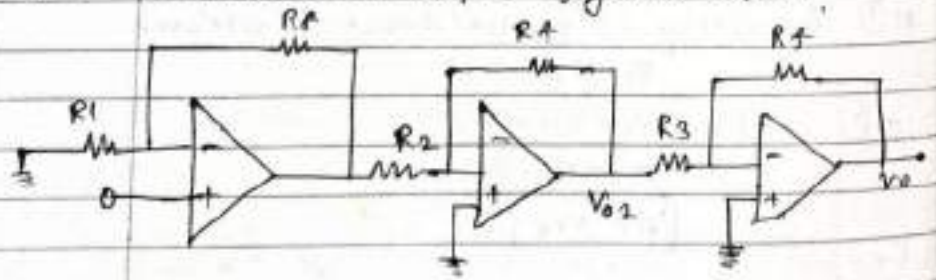
① $V_{o1} = V = 1.5V$ (As $V_{in} = V_o$)

② # [from inverting Amplifier]

$V_o = -\frac{R_f}{R_1} v_{in}$ (Inverting)

$-\frac{100k}{20k} V_{o1} = \frac{-100k}{20k} 1.5 = -7.5$ Volt

Q: Calculate the output of given circuit?



Ans:- $V_o = -\frac{R_f}{R_3} V_{o2}$

$\Rightarrow \left(-\frac{R_f}{R_2}\right) V_{o1}$

$\Rightarrow \left(-\frac{R_f}{R_1} V_1\right)$

$V_o = -\left[\frac{R_f}{R_3}\right]\left[\frac{R_f}{R_2}\right]\left[\frac{R_f}{R_1}\right] V_1$

$= \frac{470}{33} \times \frac{470}{33}\left[1 + \frac{470}{4.3}\right] \times 80$

$= \frac{470}{33} \times \frac{470}{33} \times \frac{474.3}{4.3} \times 80$

$= 14.24 \times 14.24 \times 110.30 \times 80$

$= 1789309.54$ μV

1.78V Ans

02/feb/2023

Slew rate Based.

$SR = \frac{dv_o}{dt}\Big|_{max}$

$f_{max} = \frac{SR}{2\pi V_m}$

$SR = V_m \omega_{max}$

$SR = V_m 2\pi f_{max}$

$V_m \times \omega [\cos]_{max}$

Q:- An op Amp has slew rate 15V/micro sec then calculate its full power bandwidth for a peak voltage of 10.

formula used

$$f_{max} = \frac{SR}{2\pi V_m}$$

Ans:

$$f_{max} = \frac{15}{2 * 3.14 \times 10 \times 10^{-6}}$$

$$238.7 \times 10^{3} Hz$$ Ans.

Q:- for an op Amp input offset current (I_{io}) is 20nA while input bias (I_{iB}) = 60nA calculate values of two input bias current?

Ans: $I_{ios} = 20nA = I_{b1} - I_{b2}$

$I_{iB} = 120nA = I_{b1} + I_{b2}$ $\left(\frac{I_{b1}+I_{b2}}{2}\right)$

$I_{b1} = 120nA - I_{b2}$

$120nA - I_{b2} - I_{b2} = 20nA$.

$100nA = 2I_{b2}$

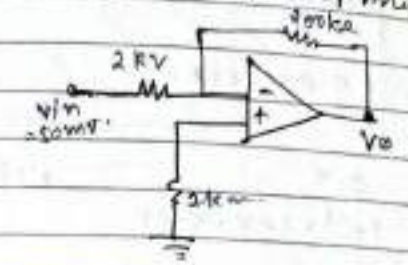
$50nA = I_{b2}$

$20nA = I_{b1} - 50nA$

$20nA + 50nA = I_{b1}$

$I_{b1} = 70nA$

Q:- for input of 50mV in given ckt determine the maximum frequency that may be used when the slew rate of an op Amp is 0.4V/μs.



Ans:

$$V_0 = \frac{-R_f}{R_1} V_{inp}$$

$$= \frac{-200k}{2k} * 50mV$$

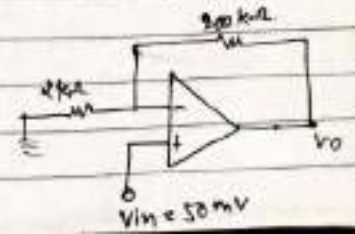
$V_0 = -5V$ ckt

$|V_0| = 5$

$$f_{max} = \frac{S.R}{2\pi (V_m)} = \frac{0.4}{10^{-6} \times 2 \times \pi \times 5}$$

$$= 12.73 \times 10^{3} Hz$$

Q: Determine Maximum freq for given ckt if SR = 0.4V/μsec



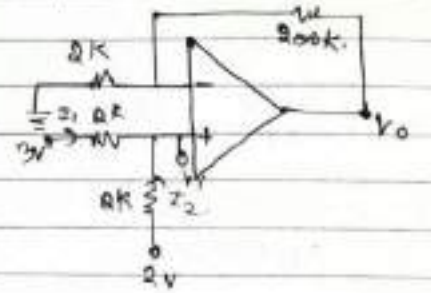
Ans:- $V_o = \left(1 + \frac{R_f}{R_1}\right) V_{inp}$

$= \left(1 + \frac{200}{2}\right) \times 50 \times 10^{-3}$

$V_o = 5.05$ volt.

$SR = \frac{0.4}{10^{-6} \times 2 \times \pi \times 5.05} = 12.606 \times 10^{3}$ Hz.

Q: Calculate output voltage for given circuit?



Ans:-

$V_o = \left(1 + \frac{R_f}{R_1}\right) V_{inp}$

$= \left(1 + \frac{200k}{2k}\right) V_1$

$= (1 + 100) 2.5$

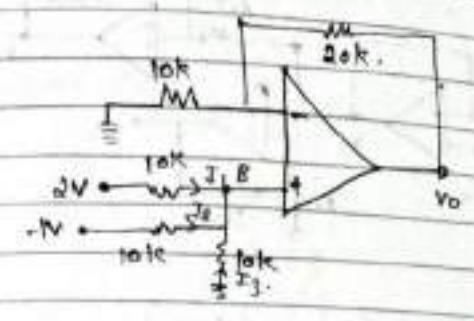
$= 252.5$ Volts

$I_1 + I_2 = 0$

$\frac{3 - V_1}{2k} + \frac{2 - V_1}{2k}$

$V_1 = 2.5$ volt

Q: Calculate V_o for given circuit?



Ans:- Non inverting Adder.

$V_o = \left(1 + \frac{R_f}{R_1}\right) V_{inp}$

$V_o = \left(1 + \frac{20k}{10k}\right) V_1$

$V_1 = ?$

Apply KCL at Node B:-

$I_1 + I_2 + I_3 = 0$

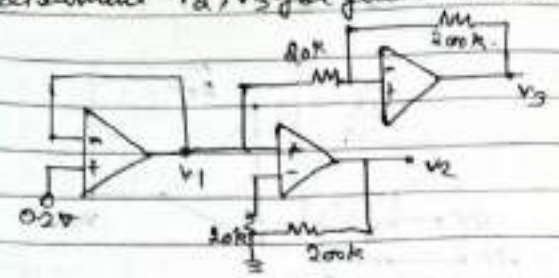
$\frac{2 - V_1}{10k} + \frac{-1 - V_1}{10k} + \frac{0 - V_1}{10k} = 0$

$V_1 = 1/3$ volts

$V_o = \left(1 + \frac{20k}{10k}\right) 1/3$

$V_o = 1$ volt

Q: Determine V_2, V_3 for given circuit?



Ans:

$V_1 = 0.2V$ (Buffered Amp)

$V_2 = ?$ (non-inverting)

$V_2 = \left(1 + \frac{250k}{20k}\right) 0.2 = 2.2$ volt

$V_3 = ?$ (Inverting)

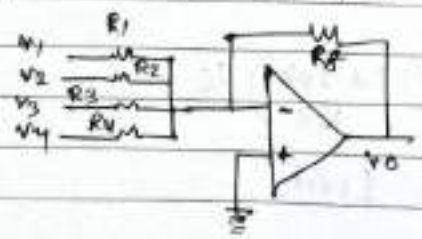
$V_3 = \frac{200k}{20k} * 0.2$

$= -2$ volts.

$V_2 = 2.2$ Volt, $V_3 = -2$ volt

Q: Design an op Amp with the op Amp.

$V_0 = -3V_1 + 2V_2 - 5V_3 + V_4$ —— ①



Ans:

$$V_0 = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3 + \frac{R_f}{R_4}V_4\right] \quad ②$$

on equating ① & ②

$\frac{R_f}{R_1} = 3$, $\frac{R_f}{R_2} = 2$, $\frac{R_f}{R_3} = 5$,

$\frac{R_f}{R_4} = 1$

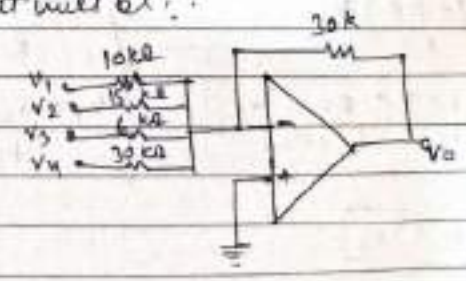
$R_1 = \frac{R_f}{3} = 30/3 = k\Omega = 10$

$R_2 = R_f/2 = 30/2 = 15k\Omega$

$R_3 = R_f/5 = 30/5 = 6k\Omega$

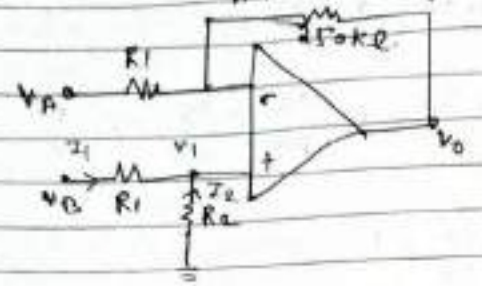
$R_4 = R_f/1 = 30/1 = 30k\Omega$

* So circuit will be:



Q:- find the value of R_1 & R_2 for the output to be :-

$V_0 = -5V_A + 3V_B$ for given ckt.



Ans:

$V_{o/p} = -\frac{R_f}{R_1} V_{input}$

$V_0 = \frac{-250k}{R_1} \times V_A$

Non inverting

$V_0 = \left(1+\frac{250k}{R_1}\right) \times V_1$

$V_0 = \left(1+\frac{R_f}{R_1}\right) V_1$

$\left(1+\frac{R_f}{R_1}\right)\left(\frac{R_2}{R_1+R_2}\right) V_B$

$\left(1+\frac{R_f}{R_1}\right) V_1$

Apply KCL

$I_1 + I_2 = 0$

$\frac{V_B - V_1}{R_1} + \frac{0 - V_1}{R_2} = 0$

$V_1 = \frac{V_B R_2}{R_1 + R_2}$

$V_0 = V_{o1} + V_{o2}$

$V_0 = -5V_A + 3V_B$

$= -5 = \frac{-250k}{R_1}$

$= R_1 = 50k\Omega$

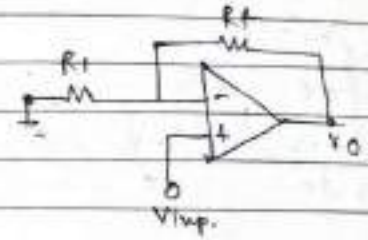
$\left(1+\frac{R_f}{R_1}\right)\left(\frac{R_2}{R_1+R_2}\right) = 3$

$\left(1+\frac{250k}{50k}\right)\left(\frac{R_2}{50k+R_2}\right) = 3$

$R_2 = 50k$

Q: Design a non-inverting amplifier that is capable of providing a voltage gain of 15. Assume ideal op amp and resistances used should not exceed $30k\Omega$?

Ans:-



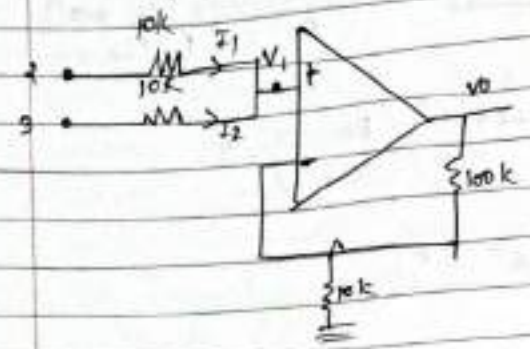
gain $= \left(1+\frac{R_f}{R_1}\right) = 15$

$\frac{R_f}{R_1} = 14$

let $R_f = 30k\Omega$

$R_1 = \frac{R_f}{14} = \frac{30k}{14} = 2.1k\Omega$

Q.



Ans:- Non-inverting

$$V_0 = \left(1+\frac{R_f}{R_1}\right)V_1$$

$$V_0 = \left(1+\frac{100}{10}\right)V_1$$

$V_1 = ?$

$$I_1 + I_2 = 0$$

$$\frac{2-V_1}{10} + \frac{3-V_1}{10} = 0$$

$$\frac{2}{10} - \frac{V_1}{10} + \frac{3}{10} - \frac{V_1}{10} = 0$$

$$\frac{-2V_1}{10} = \frac{5}{10}$$

$$V_1 = 5/2$$

$$V_0 = (1+10)\times 5/2$$

$$= 55/2\,V = 27.5V$$

(Op amp as a comparator):-

① comparator may be defined as a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input & produces either a high or low o/p voltage depending upon which input is higher.

② comparator output has 2 voltage level either high or low it is not linearly proportional to input voltage.

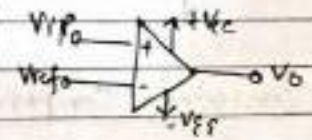
③ op-amp in an open loop configuration or sometimes a the feedback configuration can be used as a comparator.

There are 2 types of comparator.

1) Non inverting comparator -

$V_{in} > V_{ref}$, $V_0 = +V_{sat}$

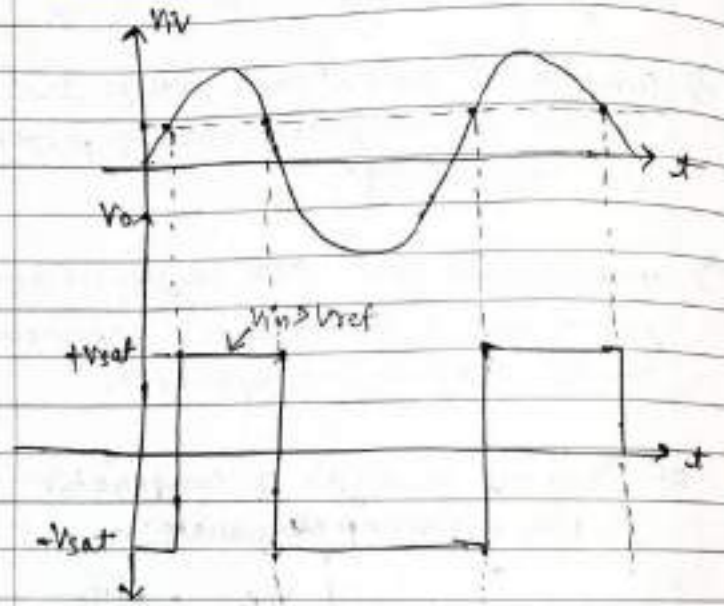
$V_{in} < V_{ref}$, $V_0 = -V_{sat}$



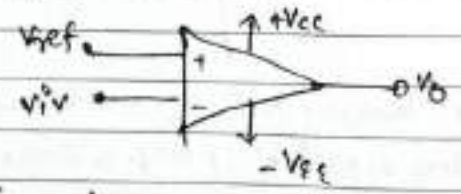
Here a known reference voltage is applied at inverting input of op amp & time varying signal V_{in} is applied is at non-inverting of an op-amp since V_{in} applied at the

terminal circuit is called as non-inverting comparator.

The open loop gain of the op-Amp is very large so with a small input voltage, the op-amp will go into saturation & the output V will be either +Vsat or -Vsat.



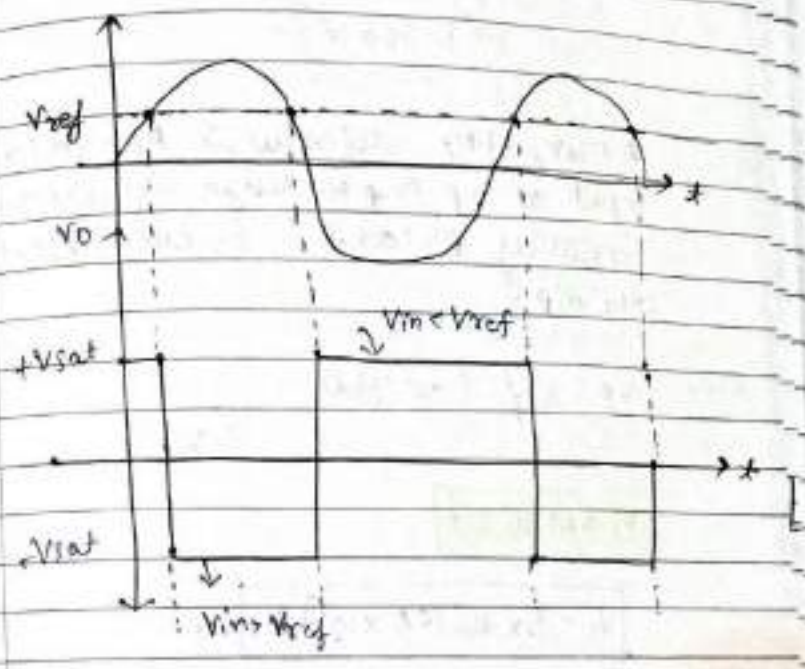
d) Inverting Comparator.



Vin > Vref ; Vo = -Vsat

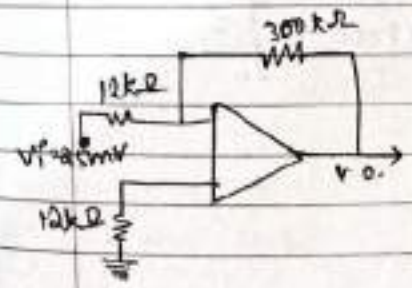
Vin < Vref ; Vo = +Vsat.

Here reference voltage is applied to non-inverting input & signal voltage is applied to inverting terminal of op-Amp.



Q: Calculate A_{cl}, Zi, Zo
closed loop gain, I/P impedance, o/p impedance.

Given:
$R_o = 75\Omega$
$A = 300k$



① $A_{cl} = \left|\frac{-R_f}{R_1}\right|$

$A_{cl} = \left|\frac{-300k}{12}\right| = |-25| = 25$

$A_{cl} = \frac{1}{\beta}$

(1) $Z' = R_1 = 1\Omega$

$Z_0 = \frac{Z_0}{1+AB} = \frac{75}{1+300\times\frac{1}{25}} \times 10^{3}$

$= 5.76\times10^{-3}$

Q:- A 5mV, 1kHz sin wave is Applied at input of op-Amp to design integrator circuit if $R = 100k\Omega$, $C = 1\mu F$, Calculate the o/p?

Ans:- $V_0 = \frac{-1}{RC}\int V_i(t)\,dt$

$\Rightarrow V_i = ?$

$V_i = V_m \sin\omega t$

$V_i = 5\times\sin(2\pi\times10^{3})t$ mV.

$V_0 = \frac{-1}{100\times10^{3}\times1\times10^{-6}}\left[\int_0^t 5\sin(2000\pi)t\,dt\right]$

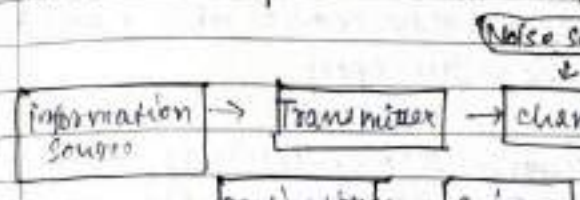
$V_0 = \frac{-50}{2000\pi}\left[-\cos 2000\pi t\right]_0^t$

UNIT-5 (COMMUNICATION SYSTEMS)

Unit-5 (communication System)

Communication refers to transmission of information from one place to another place.

Element of communication system:-
OR
Block Diagram of communication system.
OR
fundamental of communication System.



Main elements of communication System are:-

(i) Information source	(iv) Noise source
(ii) Transmitter	(v) Reciever
(iii) channel	(vi) Destination

(i) Information Source:- The message signal comes from the information source it will be in non-electrical form which will be then converted into electrical form by using transducer.

Transducer:- it's a device which converts the energy from one form to another form.

(ii) Transmitter:- it's a collection of electronic circuits design to convert the information into a signal suitable for transmission over a given communication medium.

(iii) Channel:- it's the medium by which electronic signal is transmitted from one place to another place it can be of conducting wire coaxial cable a pair optical fibre & free space.

(iv) Reciever:- it's a collection of electronic circuits design to convert the signal back to the original information. it consists of amplifier, detector, mixer & oscillator.

(v) Noise:- it is random undesirable electric energy that enters in the communication system through channel. IMPORTANT

(vi) Destination:- the destination block recieves the message signal it process the message signal to recollect the information present in it.

$\lambda = c/f$ $(f \uparrow \lambda \downarrow)$
$\lambda \propto 1/f$

(Modulation & Demodulation)#

modulation is a process in which some parameters of carrier wave. such as (Amplitude, Frequency, Phase) is varied in accordance with the modulating signal.

- At the recieving end message signal and the carrier signal are separated from the modulated signal by the process of demodulation

- Base Band signal
- Modulating signal
- information signal
- Audio signal.

} low frequency signals.

- carrier signal / Radio signal } High freq signals

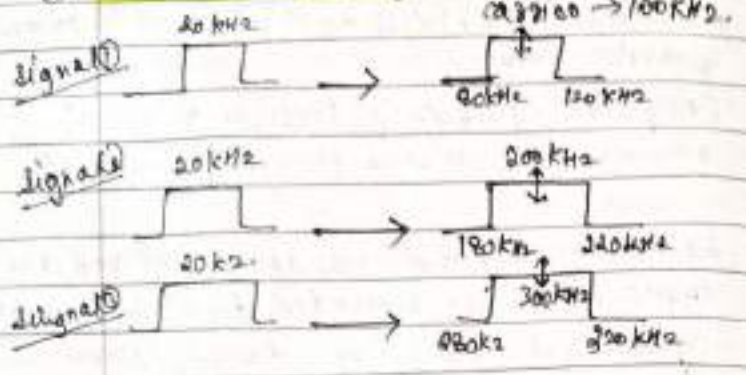
[(carrier signal + Modulating Signal
↓
Modulated signal)]

(Need of modulation)#

(1) reduces the height of antenna. the height of antenna is a function of wavelength. (λ) & we know that ($\lambda = c/f$) therefore ($\lambda \propto 1/f$)

when f increases, λ ($\downarrow$) thus antenna height reduces as well as cost reduces

② **Avoid mixing of signal.**



* if sound signals are transmitted without modulation by more than one transmitter then all the signal mixes in same frequency domain. so they get mixed together and receiver cannot separate them from each other.

* if each sound signal is used to modulate a different carrier then they will occupy different frequency slots. thus **Modulation Avoids mixing of signals.**

③ **Increases the range of communication:**

* At low frequencies radiation is poor and signal gets highly attenuated (Degraded) / distorted. Modulation increases the freq of signal & thus increases the distance over which the signal can be transmitted.

④ **Allows multiplexing of signals.**

Modulation permits multiplexing [means transmission of 2 or more signals simultaneous over the same channel]

⑤ **Allows Adjustment in the Bandwidth:**

Bandwidth of a modulated signal (carrier + Base) can be made flexible by using modulation.

⑥ **Improves quality of reception:-**

using modulation we can reduce the effect of noise.

[Amplitude Modulation]

When the amplitude of carrier signal gets changed with respect to ($\omega_m t$) Instaneous value of Base Band or massive of Base Band or msg signal is called Amplitude modulation.

Now consider modulting signal (V_m) and carrier signal (V_c), which is given by

eq ① $V_m = V_m \sin \omega_m t$

Eq ② $V_c = V_c \sin \omega_c t$.

Here V_c is peak value of carrier.

* V_m is peak value of modulating / Info signal

* ω_c = carrier frequency
* ω_m = modulating frequency
* v_m = instantaneous Amplitude of modulating signal.
* v_c = instantaneous amp of carrier signal.

{ Expression for Amplitude modulated (Am) signal }

⇒ As we know information signal is given by. $\boxed{V_m = V_m \sin \omega_m t}$ — (1)

and carrier signal is given by $\boxed{v_c = V_c \sin \omega_c t}$ — (2)

Amplitude modulated signal is given by.

$$\boxed{v_{am} = V_{AM} \sin \omega_c t} \quad — (3)$$

* Now from defination Peak amplitude of Am wave will be:

$$\boxed{V_{AM} = V_c + V_m}$$

$$\boxed{V_{AM} = V_c + V_m \sin \omega_m t}$$

from Eq^n (3) $\boxed{v_{am} = (V_c + V_m \sin \omega_m t) \sin \omega_c t}$ — (4)

As we know modulation index is given by

$$m = \frac{V_m}{V_c}$$

$$\Rightarrow \boxed{V_m = mV_c}$$

$$v_{AM} = (V_c + mV_c \sin \omega_m t) \sin \omega_c t$$

$$\boxed{v_{AM} = V_c \sin \omega_c t + mV_c \sin \omega_m t \sin \omega_c t}$$

$\because 2 \sin(A \sin B) = \cos(A-B) - \cos(A+B)$

$$\boxed{v_{AM} = \underbrace{V_c \sin \omega_c t}_{\text{carrier } f_c} + \underbrace{\frac{mV_c}{2} \cos(\omega_c - \omega_m) t}_{\text{lower side Band (LSB) } (f_c - f_m)} - \underbrace{\frac{mV_c}{2} \cos(\omega_c + \omega_m) t}_{\text{upper side Band (USB)}}}$$

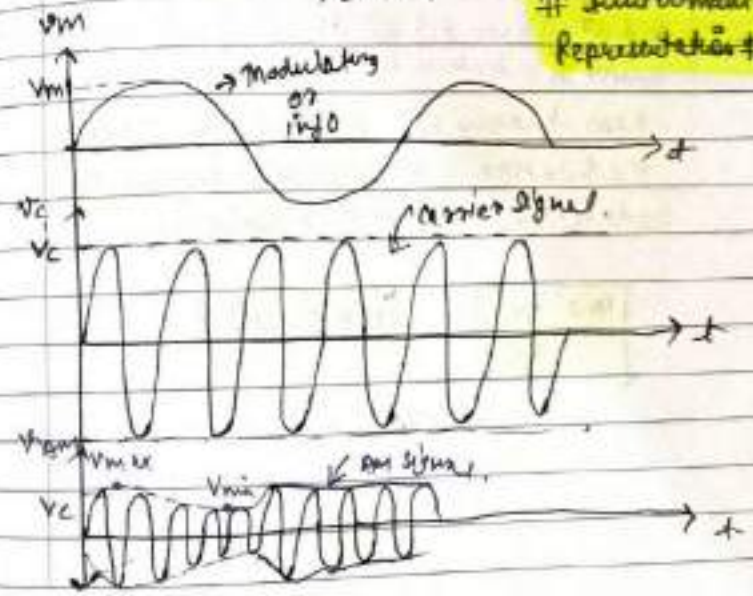
Final Form eqn

upper side Band (USB)

⇓

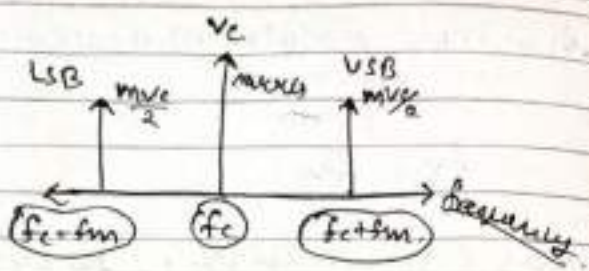
$f_c + f_m$

Time Domain Representation



Bandwidth = frequency of range.

#



(Bandwidth of AM)

Maximum frequency − Minimum freq

$$(f_c + f_m) - (f_c - f_m) = 2 f_m$$

IMPORTANT

(Modulation Index)

• The relationship b/w amplitudes of modulating & carrier signal is important and it's expressed in terms of there ratio which is known as modulation index. It also known as modulation factor, modulation coefficient, degree of modulation, depth of modulation.

$$\boxed{m = \frac{V_m}{V_c}} \qquad \boxed{m = 0 \text{ to } 1}$$

* $V_{max} = V_c + V_m$
* $V_{min} = V_c - V_m$

* $V_c = \frac{V_{max} + V_{min}}{2}$

* $V_m = \frac{V_{max} - V_{min}}{2}$

$$\boxed{m = \frac{V_m}{V_c} = \frac{V_{max} - V_{min}}{V_{max} + V_{min}}}$$

IMP

: (Power relations in AM wave) :-

Total power in amplitude modulating wave

$$P_t = P_c + P_{LSB} + P_{USB}$$

$$P_t = \frac{V^2_{carrier}}{R} + \frac{V^2_{LSB}}{R} + \frac{V^2_{USB}}{R}$$

$\boxed{V_{rms} = V_{peak}/\sqrt{2}}$ formula used :-

$$P_t = \frac{(V_c/\sqrt{2})^2}{R} + \frac{(mV_c/2/\sqrt{2})^2}{R} + \frac{(mV_c/2/\sqrt{2})^2}{R}$$

$$P_t = \frac{V_c^2}{2R} + \frac{m^2V^2}{8R} + \frac{m^2V_c^2}{8R}$$

$$P_t = \frac{V_c^2}{2R} + \frac{V_c^2}{2R} \cdot \frac{m^2}{4} + \frac{V_c^2}{2R} \cdot \frac{m^2}{4}$$

$$\boxed{P_t = P_c + \underbrace{P_c \, m^2/4}_{LSB} + \underbrace{P_c \, m^2/4}_{USB}}$$

IMPORTANT

$P_t = P_c\left(1+\frac{m^2}{2}\right)$

P_t = Total Power
P_c = carrier Power
m = modulation index
(PC)

Q1):- A 400 Watt carrier is modulated to a calculate total power in the modulated wave?

Ans:-

$P_c = 400$ watt

$m = \frac{75}{100} = 0.75$

$P_t = 400\left(1+\frac{(0.75)^2}{2}\right)$

$= 400(1+0.28125)$

$400 + 112.5$

$= 512.5$

Q2: A broadcast radio transmitter radiates 10 kW when the modulation percentage is 60%. how of this is carrier power?

$P_t = P_c(1+m^2/2)$

$10 = P_c(1+(6)^2/2)$

$10 = P_c(1+\frac{36}{2})$

$P_c = \frac{10}{1.18} = 8.47$ KW

$P_t = P_c\left(1+\frac{m^2}{2}\right)$ LSB+USB = $P_c m^2/2$

LSB = $P_c m^2/4$ USB = $P_c m^2/4$

(Current Relations in AM waves)

$P = I^2R$

$I_t = I_c\sqrt{1+m^2/2}$

Total current — Carrier current

Q3: The Antenna Current of an AM transmitter is 8 Amperes only when the carrier is sent? but it increases to 8.9 Amperes when the carrier is modulated find the % modulation? Determine the antenna current when the % of modulation changes to 0.8?

Ans. given $I_t = 8.93$
$I_c = 8$
(a) m = ?

$m = \sqrt{2\left[\left(\frac{I_t}{I_c}\right)^2-1\right]}$

$m = \sqrt{2\left[\left(\frac{8.93}{8}\right)^2-1\right]} = 0.701 = 70.1\%$

(b) $m = 0.8$
$I_c = 8$
$I_t = I_c\sqrt{1+m^2/2}$

$I_t = 8\sqrt{1+\frac{(0.8)^2}{2}}$

$I_t = 9.19$ amp

Short Notes

Important

- $$\boxed{V_{AM} = V_c\left[1 + m\sin\omega_m t\right]\sin\omega_c t}$$

- $$V_{AM} = \underbrace{V_c\sin\omega_c t}_{\text{carrier}} + \underbrace{\frac{mV_c}{2}\cos(\omega_c - \omega_m)t}_{LSB} - \underbrace{\frac{mV_c}{2}\cos(\omega_c + \omega_m)t}_{USB}$$

- $$P_t = \underbrace{\frac{V_c^2}{2R}}_{\text{Carrier Power}} + \underbrace{\frac{m^2V_c^2}{8R}}_{\text{LSB Power}} + \underbrace{\frac{m^2V_c^2}{8R}}_{\text{USB Power}}$$

- Total Power $(P_t) = \underbrace{P_c}_{\text{carrier}} + \underbrace{\boxed{P_c\frac{m^2}{2}}}_{\text{(Power of 2 side Bands)}}$

- $$P_t = P_c + \underbrace{P_c\frac{m^2}{4}}_{\text{LSB Power}} + \underbrace{P_c\frac{m^2}{4}}_{\text{USB Power}}$$

IMPORTANT

(Modulation by Several SineWaves)

(Total modulation index) $m_t = \sqrt{m_1^2 + m_2^2 + m_3^2 + \cdots}$

$$P_t = P_c\left(1 + \frac{m_t^2}{2}\right)$$

m_1 = mod^n index of 1st carrier wave
m_2 = " " 2nd carrier wave.

IMPORTANT

Q.4 A transmitter radiates 9kW with the carrier unmodulated (P_c). and 10.125kW when the carrier is modulated. calculate the modulation index. If another sine wave is simultaneously transmitted with modulation index 0.4, determine the total radiated power.

Ans:- $P_t = P_c\left(1 + \frac{m^2}{2}\right)$

$$\sqrt{2\left(\frac{P_t}{P_c} - 1\right)} = m = \sqrt{2\left(\frac{10.125}{9} - 1\right)} = 0.50$$

$m_1 = 0.5$
$m_2 = 0.4$.

$$m_t = \sqrt{(0.5)^2 + (0.4)^2} = 0.64$$

$$\boxed{P_t = P_c\left(1 + \frac{m_t^2}{2}\right)}$$

$$= 9\left(1 + \frac{(0.64)^2}{2}\right) kW$$

$= 10.84$ kW Ans:-

Q5. The antenna current of an AM transmitter, modulated to a depth of 40% by audio sine wave is eleventh Ampere, it increases to 12 Amp as a result of simultaneous modulation by another sine wave what is the modulation

due to this 2nd wave?

Ans = $m_1 = 0.4$ (0.4/100)

$m_2 = ?$

$I_c = ?$ → 10.58 Ans.

$I_t = 11$ Amp

$I_t = I_c\sqrt{1+m^2/2}$

$11 = I_c\sqrt{1+\frac{(0.40)^2}{2}}$

$I_c = 10.58$ Amp.

* Case (2)

$I_t = 12$ Amp

$I_c = 10.58$

$m_1 = 0.40$

$m_2 = ?$

$I_t = I_c\sqrt{1+\frac{m_t^2}{2}}$

$12 = 10.58\sqrt{1+\frac{m_t^2}{2}}$

$m_t = (1.13)^2 = 1 + \frac{m_t^2}{2}$

$= 0.757$

$m_2 ?$

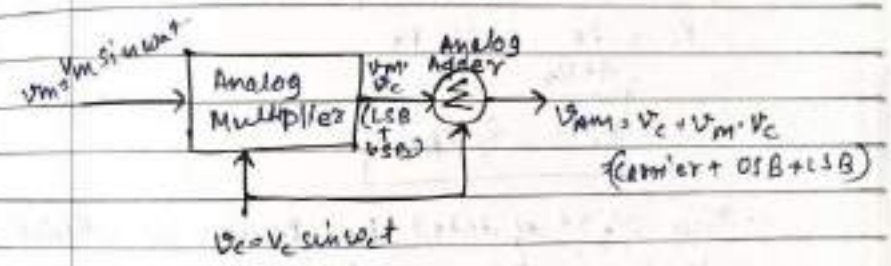
$m_t = \sqrt{m_1^2 + m_2^2}$

$0.757 = \sqrt{(0.40)^2 + m_2^2}$

$m_2 = 0.643$

(Amplitude Modulated wave Generation Techniques)

Que: Complete Am Wave (carrier + LSB + USB) Generation.



- Am wave can be generated using analog multiplier and adder.
- The o/p of the multiplier is given by

$$v_m \cdot v_c = \frac{mV_c}{2}\cos(\omega_c - \omega_m)t - \frac{mV_c}{2}\cos(\omega_c + \omega_m)t$$

- Now by adding carrier with the help of adder we can generate complete AM wave which is given by:-

$$v_{AM} = V_c \sin\omega_c t + \frac{mV_c}{2}\cos(\omega_c - \omega_m)t - \frac{mV_c}{2}\cos(\omega_c + \omega_m)t$$

(Case 2) <u>Double side Band (suppressed carrier) DSBSC</u>

Power for complete AM signal is given by $\boxed{P_t = P_c(1 + m^2/2)}$ ① $\boxed{P_c = \frac{P_t}{(1 + m^2/2)}}$ ②

for 100% modulation ($m = 1$)

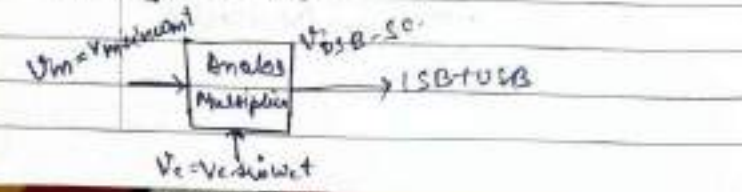
$$P_c = \frac{P_t}{1 + 1/2} = 2/3\, P_t$$

$$\boxed{P_c = \frac{2}{3} P_{AM}}$$

- Thus $2/3^{rd}$ of total AM Power is utilised for carrier transmission which doesn't carry any information so a significant saving in power can be achieved by removing carrier before transmission this technique is known as DSBSC.

08/Feb/2023

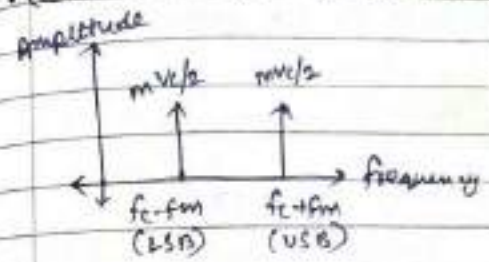
(Generation)



- output of Multiplier will be DSB-SC signal.

$$V_{DSB-SC} = \frac{mV_c}{2}\cos(\omega_c - \omega_m)t - \frac{mV_c}{2}\cos(\omega_c + \omega_m)t$$

∴ (DSB-SC frequency Spectrum):-



<u>Bandwidth</u>

BW of DSB-SC

$(f_c + f_m) - (f_c - f_m)$

$= 2 f_m$

(Power Relation in DSB-SC)

$$P_{DSB-SC} = \left(\frac{mV_c/2}{\sqrt{2}}\right)^2 + \left(\frac{mV_c/2}{\sqrt{2}}\right)^2$$

$$P_{DSB-SC} = \frac{m^2 V_c^2}{8R} + \frac{m^2 V_c^2}{8R}$$

$$P_{DSB-SC} = P_c\frac{m^2}{4} + P_c\frac{m^2}{4} = \boxed{P_c\frac{m^2}{2}}$$

Q6. A 400W carrier is amplitude modulated to the depth of 100%, calculate total power in case of AM and DSBSC technique, how much power saving is achieved for DSBSC?

Ans:- given

$P_c = 400\ W$

$m = 100\% = 1$

$P_{AM} = P_c(1 + m^2/2)$

$= 400(1 + 1/2) = 600$ watts.

$P_{DSBSC} = \frac{m^2}{2} P_c$

$= 400 \times \frac{(1)^2}{2} = 200$ watts.

Power Saving = $P_{AM} - P_{DBSC}$

$= 600\ W - 200\ W$

$= 400\ W$

Q 9 A DSBSC transmitter 1kW when the modulation '%' is 60%, how much of carrier power is required if we want to transmit the same message by AM transmitter?

given.

Ans:- $P_{DSBSC} = 1kW$

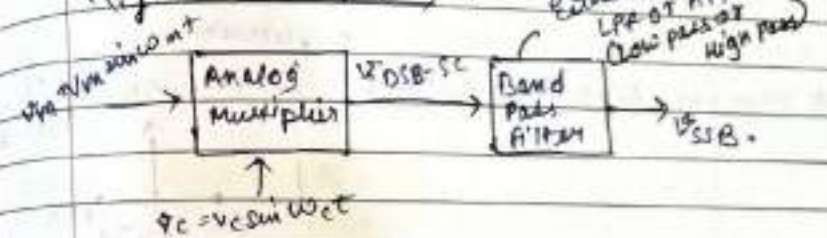
$m = 60\% = 0.60$

$P_c = \frac{P_{DSBSC}}{m^2} \times 2 = \frac{1 \times 2}{(0.60)^2} = 556\ kW$

Single Sideband (suppressed carrier) (SSB)

- The Bandwidth requirement of DSBSC is still same as that of AM ($2f_m$).
- Hence saving bandwidth can be achieved by suppressing or removing one of the sideband the technique is known as single side band technique.

(Generation of SSB)



(Output of the multiplier is given by:) # (USB)

- $v_{DSB-SC} = \frac{m v_c}{2} \cos(\omega_c - \omega_m) t - \frac{m v_c}{2} \cos(\omega_c + \omega_m) t$.

LSB (1)

- Now for generation for SSB the DSBSC signal is passed through Band Pass filter.

i) if filter is LPF (low Pass filter) with critical frequency (f_c)

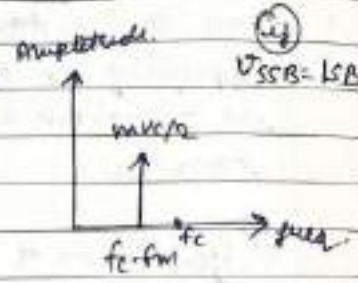
i) $V_{SSB} = LSB$

if filter is HPF of carrier frequency. fc

$V_{SSB} = V_{SB}$.

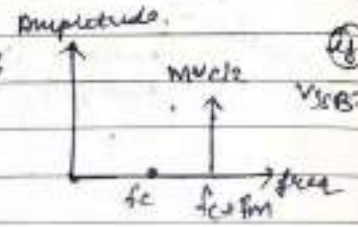
(frequency spectrum of SSB)

when use low pass filter:



$V_{SSB} = LSB$

when use High pass filter:



$V_{SSB} = U_{SB}$

(Power relations in SSB)

$$P_{SSB} = \frac{(mV_c/2/\sqrt{2})^2}{R} \Rightarrow \frac{m^2 V_c^2}{8R}$$

$$\Rightarrow \underbrace{\frac{V_c^2}{2R}}_{P_c} \frac{m^2}{4} = P_c m^2/4$$

Q8. An SSB Transmitter radiates 0.5kW when the modulation % is 60%. how much of carrier power is reqd by the transmitter?

Ans: given:

$P_{SSB} = 0.5kW$

$m = 60\% = 0.6$

$P_c = ?$

$P_{SSB} = P_c m^2/4$

$0.5 = P_c \cdot \frac{(0.60)^2}{4}$

$P_c = \frac{4 \times (0.5)}{(0.60)^2}$ kW

$P_c = 5.56kW$

Q7. Calculate the % power saving when the carrier & one of the side Band are suppressed in Am wave modulated to a depth of 100%?

Ans: $P_{SSB} = \frac{P_c m^2}{4}$

$P_{SSB} = \frac{P_c (1)^2}{4}$

$P_{SSB} = \frac{P_c}{4} = 0.25 P_c$

$P_{AM} = P_c\left(1 + \frac{m^2}{2}\right)$

$P_{AM} = P_c\left(1 + \frac{(1)^2}{2}\right)$

$1.5 P_c$

% Power saving: $\frac{\text{saving}}{P_{AM}} \times 100\%$

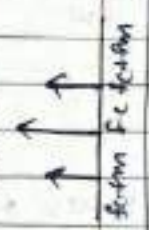
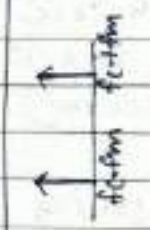
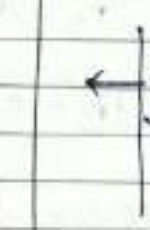
$= \frac{P_{AM} - P_{SSB}}{P_{AM}} \times 100\% = \frac{1.5 - 0.25}{1.5} \times 100$

83.3%

Mark (4)

MOST IMPORTANT

COMPARE ALL TECHNIQUES

Name	Generation	Equation	Power	Spectrum	Band width
① AM		$V_c \sin\omega_c t + \frac{mV_c}{2}\cos(\omega_c-\omega_m)t - \frac{mV_c}{2}\cos(\omega_c+\omega_m)t$	$P_t\left(1+\frac{m^2}{2}\right)$		2 fm
② DSBSC		$\frac{mV_c}{2}\cos(\omega_c-\omega_m)t - \frac{mV_c}{2}\cos(\omega_c+\omega_m)t$	$P_t\, m^2/2$		2 fm
③ SSBSC		LPF $\frac{mV_c}{2}\cos(\omega_c-\omega_m)t$ HPF $\frac{mV_c}{2}\cos(\omega_c+\omega_m)t$	$P_t\frac{m^2}{4}$		fm

Learn this table for sure! Most Important to Pass!

Amplitude demodulation

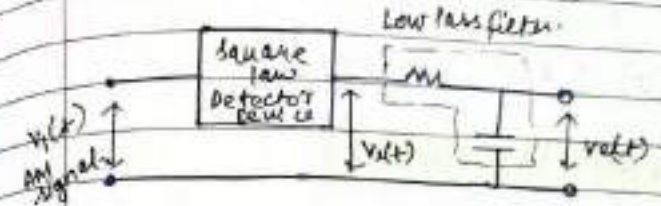
(OR) Amplitude detection].

There are 2 types of techniques:-

(1) square law detector.

(2) envelope law detector.

(i) [Square law Detector]



* It consists of a square law device which is a non-linear device and low pass R-C filter as shown in figure.

(Operation & Analysis)

The output of the square law device is non linear & expressed as $v_2(t) = a v_1(t) + b v_1^2(t)$ — ①

input of square law detector is AM signal which is given by $V_1(t) = V_c[1+m\sin\omega_m t]\sin\omega_c t$ — ②

simplified eq^n ② = $v_1(t) = V_c[1+m.x(t)]\sin\omega_c t$ — ③

$x(t) \rightarrow$ message signal.

from eq^n ① & ②

$$V_2(t) = a\left[V_c(1+m\,x(t))\sin\omega_c t\right] + bV_c^2\sin^2\omega_c t\,(1+m_a x(t))^2$$

$\Rightarrow \; a v_c \sin\omega_c t\,(1+m x(t)) + \frac{b v_c^2}{2}(1-\cos 2\omega_c t)\cdot$

$\cdot\left[1+m^2 x^2(t)+2m x(t)\right]$

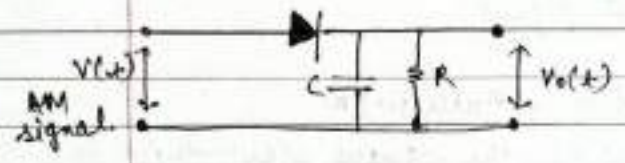
$\Rightarrow \; a v_c \sin\omega_c t\,(1+m x(t)) + \frac{b v_c^2}{2}\left[1+m^2 x^2(t)+2m x(t)\right]$

$- \frac{b v_c^2}{2}\cos 2\omega_c t\left[1+m^2 x^2(t)+2m x(t)\right]$

$\Rightarrow \; \left[V_0(t) = \frac{b v_c^2}{2} + 2m x(t)\right]$

$\Rightarrow \; \boxed{V_0(t) = b V_c^2\, m x(t)}$

(ii) [Envelope detector] #



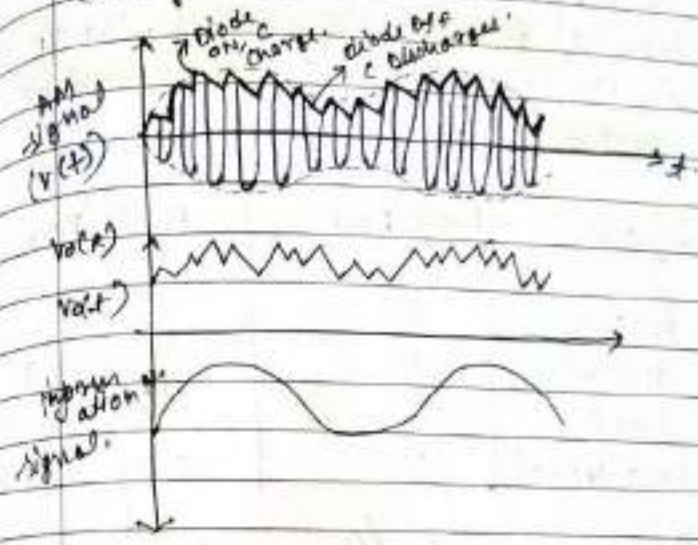
An envelope detector an output signal that follows the envelope of the input AM signal.

(Working Principle)

The standard AM signal is applied as an input to the detector (Demodulator).
During the cycle diode becomes forward biased, charging of capacitor takes place during the cycle diode becomes reverse biased, capacitor discharges through resistor

The discharging process continues until the next (+ve) half cycle repeats.

(Waveforms) :-



reception.

xxx — xxx

Electromagnetic spectrum and typical applications :→

As the name indicates, an electromagnetic (EM) wave is a signal made of oscillating electric and magnetic fields.

The entire range of frequencies that the EM wave can produce oscillations is termed as Electromagnetic spectrum.

EM spectrum classified, in terms of different freq. ranges and corresponding wavelength ranges and typical application.

$1KHz = 10^3 Hz$, $1MHz = 10^6 Hz$, $1GHz = 10^9 Hz$, $1THz = 10^{12} Hz$, $1mm = 10^{-3} m$, $1\mu m = 10^{-6} m$.

frequency (f) range	wavelength (λ) range	EM Spectrum Nomenclature	Applications.
30 - 300 Hz.	$10^7 - 10^6$ m	extremely low freq. (ELF)	Power line communication
0.3 - 3 kHz.	$10^6 - 10^5$ m	Voice freq. (VF)	Face to face speech comm^n intercom.
3 - 30 kHz	$10^5 - 10^4$ m	Very low freq. (VLF)	Submarine communication
30 - 300 kHz	$10^4 - 10^3$ m	Low freq. (LF)	Marine comm^n.
0.3 - 3 MHz	$10^3 - 10^2$ m	Medium freq. (MF)	AM Broadcasting.
3 - 30 MHz	$10^2 - 10^1$ m	High freq. (HF)	Landline telephony.
30 - 300 MHz	$10^1 - 10^0$ m	Very high freq. (VHF)	FM Broadcasting.
0.3 - 3 GHz	$10^0 - 10^{-1}$ m	Ultra high freq (UHF)	TV
3 - 30 GHz	$10^{-1} - 10^{-2}$ m	Super high freq. (SHF)	Microwave oven, Radar
30 - 300 GHz	$10^{-2} - 10^{-3}$ m	Extremely high freq (EHF)	Satellite comm^n, Radar.
0.3 - 3 THz	0.1 - 1 mm	Experimental	For all new explorations.
43 - 430 THz	7 - 0.7 μm	Infrared	LED, Laser
430 - 750 THz	0.7 - 0.4 μm	Visible light	optical communication.
750 - 3000 THz	0.4 - 0.1 μm	Ultraviolet	Medical applications.
> 3000 THz	< 0.1 μm	X-Rays, gamma Rays, cosmic Rays	Medical applications.

Scanned with CamScanner

radio frequency (RF) waves. The EM waves oscillate, they are sinusoidal and their frequency is measured in Hz. The frequency of EM signal can be very low or it can be extremely high. This entire range of frequencies of EM waves is called as **Electromagnetic spectrum***.

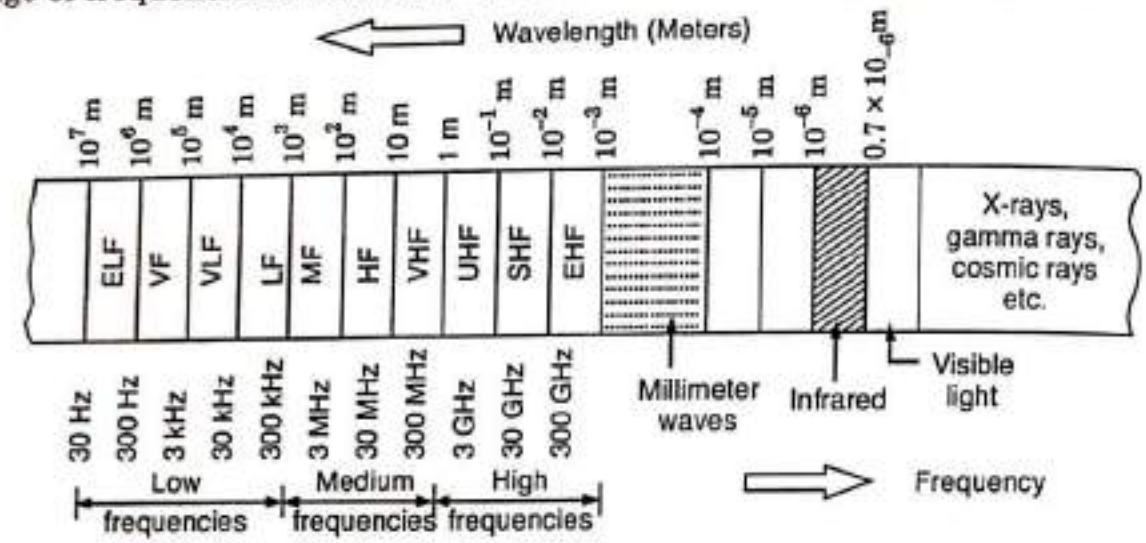


Fig. 9.26. Illustration of complete electromagnetic (EM) spectrum

The electromagnetic spectrum consists of signals such as 50 Hz line frequency and voice signals at the lower end. The radio frequencies which are used for the two way communication reside at the center of the EM spectrum. These frequencies are used for the applications such as radio of T.V. broadcasting as well. The infrared and visible light are at the upper end of the EM spectrum. Figure 9.26 shows the entire electromagnetic spectrum**.

Here, it may be noted that the short forms used in the EM spectrum of figure 9.26 have the detailed meanings as depicted in Table 9.3.

TABLE 9.3. Segments of the electromagnetic spectrum

S.No.	Name	Frequency	Wavelength
1.	Extremely low frequency (ELF)	30-300 Hz	10^7 to 10^6 m
2.	Voice frequecies (VF)	300-3000 Hz	10^6 to 10^5 m
3.	Very low frequencies (VLF)	3-30 kHz	10^5 to 10^4 m
4.	Low frequencies (LF)	30-300 kHz	10^4 to 10^3 m
5.	Medium frequencies (MF)	300 kHz-3 MHz	10^3 to 10^2 m
6.	High frequencies (HF)	3-30 MHz	10^2 to 10 m
7.	Very high frequencies (VHF)	30-300 MHz	10 to 1 m
8.	Ultra high frequencies (UHF)	300 MHz-3GHz	1 to 10^{-1} m
9.	Super high frequencies (SHF)	3-30 GHz	10^{-1} to 10^{-2} m
10.	Extremely high frequencies (EHF)	30-300 GHz	10^{-2} to 10^{-3} m
11.	Infrared	—	0.7 to 10 μm
12.	Visible light	—	0.4 μm to 0..8 μm

* The electromagnetic spectrum is that range of frequencies from approximately 30 Hz to visible light over which electronic communications take place.

** The greatest portion of the spectrum covers radio waves, which are oscillating electric and magnetic fields that radiate for long distances.

Scanned with CamScanner

Introduction to wireless Communication:-

Wireless communication involves the transmission of information over a distance without the help of wires, cables or any other form of electrical conductors.

Features of Wireless Communication:-

* Long range of communication:- The transmitted distance can be anywhere b/w a few meters (for eg. TV remote) and thousand of kilometer (for eg. radio communication).
* It can be used for cellular telephony, ~~wireless~~ wireless access to internet, wireless home networking and so on.
* Other eg. GPS units, garadge ~~door~~ door openers, wireless computer mice etc.

Wireless Advantage:-

It involves transfer of information without any physical connection b/w two or more points. It has several advantages; the most important ones are discussed below:-

a. Cost effectiveness :- It dont require elaborate physical infrastructure or maintenance practices. Hence the cost is reduced.

b Flexibility:- It enables people to communicate regardless of their location i.e. it is not necessary to be in an

Scanned with CamScanner

office or same telephone booth in order to receive or pass message.

c Convenience:- These devices are easy to user, wherever they are. There is no need to physically connect anything in order to receive or pass messages.

d. Speed:- The N/w connectivity or the accessibility were much improved in accuracy and speed.

e. Accessibility:- It helps easy accessibility as remote areas where ground lines can't be properly laid, are being easily connected to network.

f. Constant Connectivity: It also ensure that people can respond to every ~~[illegible]~~ relatively quickly.

~~Cellular Communication~~ :-

Limitation :-

a. Interference:- As wireless communication system used open space as the medium for transmitting signal so there is a huge chance that radio signal from one wireless communication system or network might interfere with other signals.

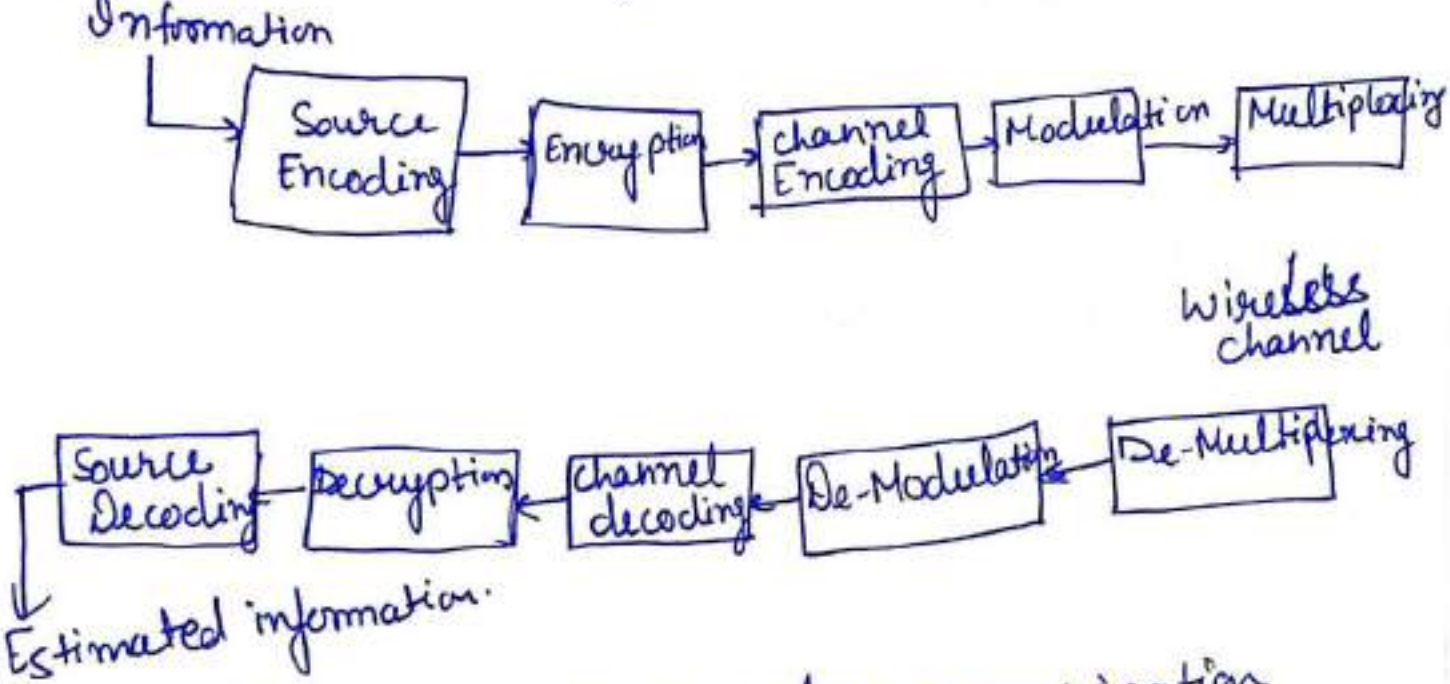
b. Security:- Since the signal are transmitted in open space, it is possible that an intruder can intercep the signal and copy sensitive information.

c. Health Concerns:- Continuous exposure to any types of radiation can be hazardous. Even it is advisable to avoid any Rf radiation to maximum.

Scanned with CamScanner

Basic Elements of a wireless Communication System:-

The following image shows the block diagram of wireless communication system.

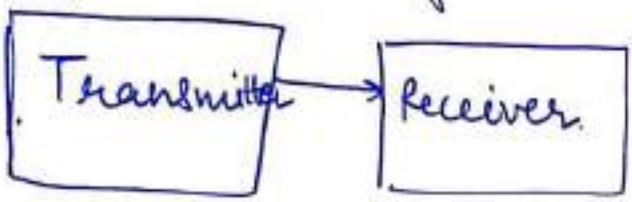


* Some of the important wireless communication system are:
* Television and Radio Broadcasting
* Satellite Communication
* Radar
* Mobile Telephone system
* Global positioning system.
* Infrared communication
* WLAN (Wi-Fi)
* Bluetooth
* ZigBee
* Paging
* Cordless phone
* RFID

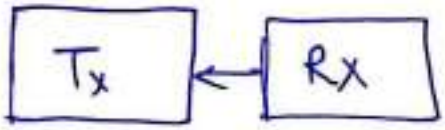
Scanned with CamScanner

Wireless systems can be classified as:-

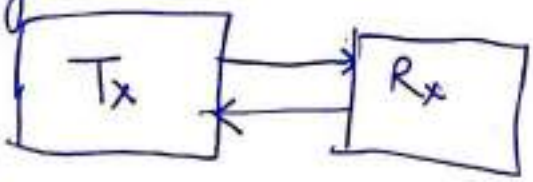
(i) Simplex:- It is only a one way communication.



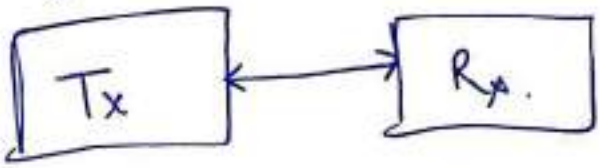
or



(ii) Half duplex:- Two way communication but one way at a time



(iii) Full Duplex:- Two way communication simultaneously.



<u>Cellular Communication</u>:- It is a form of communication technology that enables the use of mobile phones.

* Mobile phone is bidirectional radio that works in full duplex mode.
* Cellular communication is based on the geographical division of the communication coverage area into cells and within cells.

Scanned with CamScanner

~~Wireless Communication Standards:-~~

~~TIA (Telecommunication Industry Association):-~~

~~With accre~~

Cellular Communication Standards :-

1G Technology:- It refers to the first generation of wireless communication where analog signals were used to transmit data. It was introduced in the US in early 1980s and designed exclusively for voice communication. Some charactristics of 1G communication are :-

* Speeds upto 2.4kbps
* Poor voice quality
* Large phones with limited battery life.
* No data security

2G Technology :- It refers to the second generation of mobile telephony which used digital signals for the first time. It was launched in Finland in 1991 and used GSM technology. Some prominent charactristics of 2G communication are:-

* Data speed upto 64 kbps
* Text and multimedia messagin possible
* Better quality than 1G

When GPRS technology was introduced, it enabled web-browing, e-mail services and fast upload/download speeds. 2G with GPRS is also reffered as 2.5G, a step short of next mobile generation.

3G Technology :- Third generation (3G) of mobile telephony began with start of new milennium and offered major advancement over previous generations. Some of the charactristics of this generation are

* Data speeds of 144kbps to 2Mbps
* High speed web browsing
* Running web base applications like video conferencing, multimedia e-mails etc.

Scanned with CamScanner

* FM Radio Service :- It gives high-fidelity audio
* fast and easy transfer of audio and video files.
* 3D Gaming

Some limitations of 3G technology :-

* Expensive mobile phones
* High infrastructure costs like licensing fees and mobile towers.
* Trained personal required for infrastructure setup

The intermediate generation 3.5G grouped together dissimilar mobile telephony and data technologies and paved way for next generation of mobile communication.

4G Technology :- keeping the trend of a new mobile generation every decade, fourth generation (4G) of mobile communication was introduced in 2011. Its major characteristics are:-

* Speed of 100Mbps to 1Gbps
* Mobile Web access
* High definition mobile TV
* cloud computing
* IP telephony.

5G Technology :- Goals for future 5G include significantly faster speeds (a minimum of 1Gbps and perhapes upto 10Gbps) plus lower power requirements to better support huge numbers of new Internet of Things (IoT) devices. It will have capabilities to provide faster dialing speeds, multi media device connectivity, higher data speeds etc.

* There was a few advancement made within 2G Spectrum such as GSM, GPRS and EDGE.

GSM : Short for Global system for Mobile communication :.

* It enabled voice communication at 30-35kbps
* It was being used as mobile phone connectivity and popularity.

Scanned with CamScanner

GPRS:- General Packet Radio Service:- It gives higher data speeds upto 110kbps.

EDGE:- Enhanced data rates for GSM Evolution:-
↳ It was known as 2.9G or 3G.
↳ It offered high speed of 135kbps.

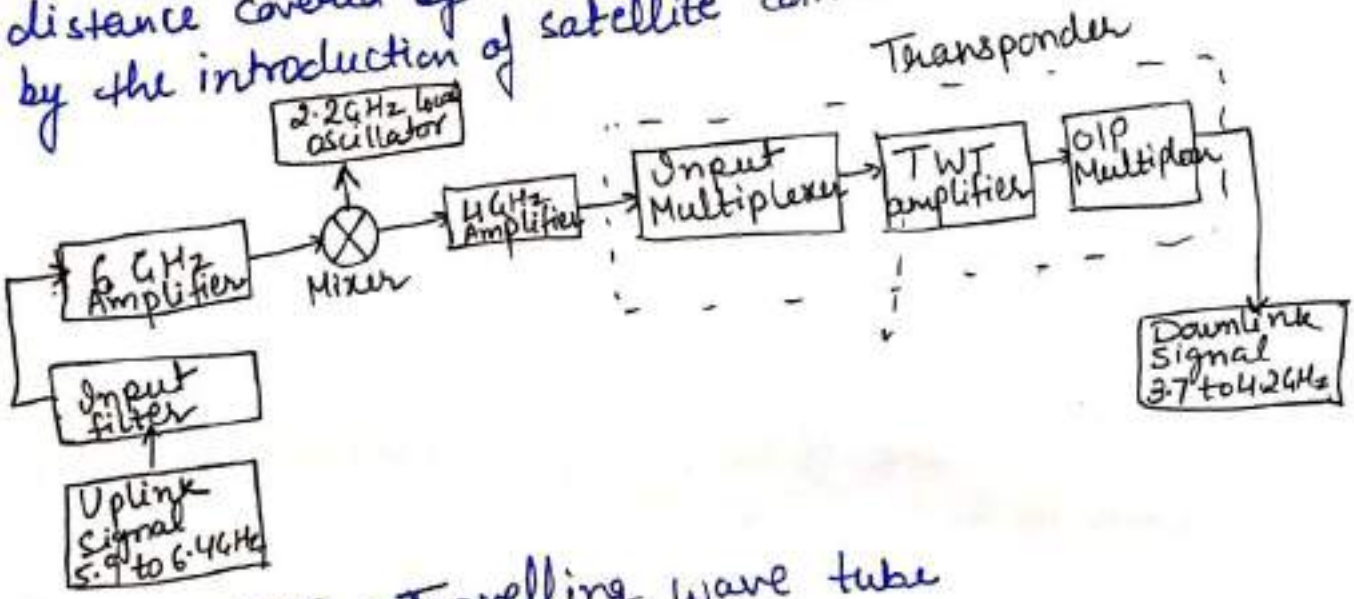
Scanned with CamScanner

Satellite Communication:- It is the method of transporting information from one place to another using a communication satellite in orbit around the earth.

* A communication satellite is an artificial satellite that transmits the signal via a transponder by creating a channel b/w the transmitter and receiver located at different locations on the earth.

Elements of Satellite Communication:

Need for Satellite Communication:- Ground wave propagation and Skywave propagation are the two ways in which communication takes place for a certain distance. The maximum distance covered by them is 1500 km and this was overcome by the introduction of satellite communication.



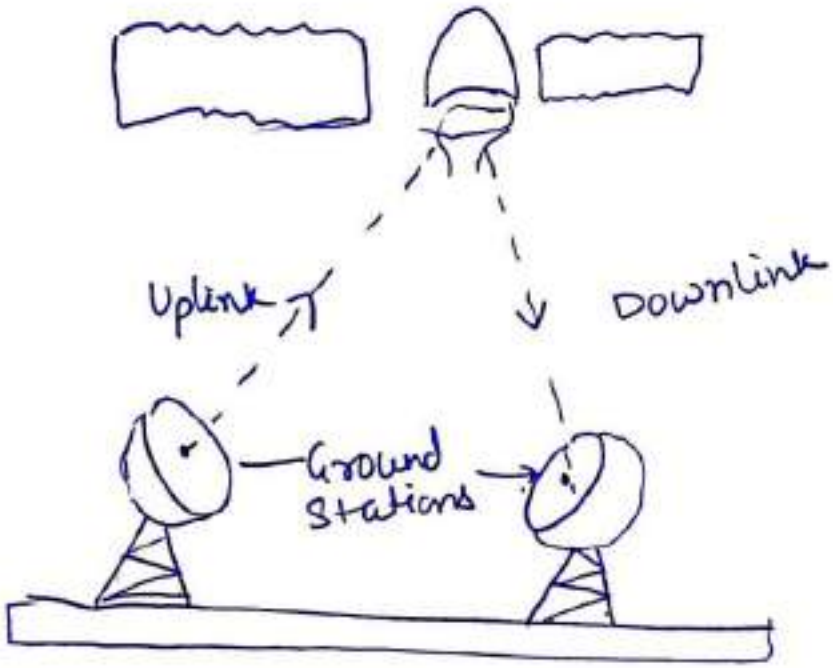
TWT → Travelling wave tube

How Satellite Communication works?

There are three stages that are involved which explain the working of satellite communication. These are:-

* Uplink
* Transponders
* Downlink

Scanned with CamScanner



for eg. Signals from a television

* In the first stage, the signal from the television broadcast ~~are~~ is beamed upto satellite from the ground station on the earth. This process is known as uplink.
* In second stage transponders such as radio receivers, amplifiers and transmitters. These transponders are used for boosting the incoming signal and to change their freq. so that outgoing signals are not altered.
* The final stage involves a downlink in which data is sent to ~~an~~ the other end of receiver on the earth.
* Note that usually there is one uplink and multiple down-links.

Scanned with CamScanner

Satellite Communications in India:-

Indian National Satellite (INSAT) system is one of the largest domestic communication system that is placed in the geo-stational orbit. There are more than 200 transponders in the INSAT system and are used for various purposes such as telecommunications, weather forecasting, disaster warning, search and rescue operations and satellite news gathering. Few satellites are listed below:-

Satellite Name	Launch date	Application
GSAT-30	Jan 17, 2020	Communication
GSAT-31	Feb 06, 2020	Communication
GSAT-15	Nov 11, 2015	Communication & Navigation
GSAT-10	Sep 29, 2012	Communication and Navigation
INSAT-3A	Apr 10, 2003	Communication, climate and environment
KALPANA-1	Sep 12, 2002	Communication, climate and environment

Advantage of Satellite Communication

* Installation of circuits are easy.
* The elasticity of these circuits is excellent
* With the help of satellite communication, every corner of earth can be covered.
* The user fully controls the network.

Disadvantage:-

1. Initial expenditure is high.
2. There are chance of blockage of frequencies
3. Propagation and interference.

Applications:- Telephone, Digital camera, Amateur radio, Military, ~~tab~~ television, radio broadcasting, Internet access, disaster management.

Scanned with CamScanner

RADAR :- It stands for radio Detection and Ranging system

* It is an electromagnetic system which is used to detect the location and distance of an object from the point where the RADAR is placed.
* It works by radiating energy into space and monitoring the echo or reflected signal from the objects. It
* It operates in UHF and microwave range.

Basic idea of RADAR:-

* It consists of a transmitter which produces an electromagnetic signal which is radiated into space by antenna.
* When Signal strikes the object it gets reflected or reradiated in many directions
* This reflected or echo signal is received by the radar antenna which delivers it to the receiver, where it is processed to determine geographical statistics of the object.
* The range is determined by the signal to travel from the RADAR to target and back.
* The target's location is measured in angle from the direction of maximum amplitude echo signal, the antenna points to.
* To measure range and location of moving object Doppler effect is used.

Scanned with CamScanner

(Unit-4)

(DIGITAL ELECTRONICS)

* Number Systems *

- Digital circuits operates with binary Number (only 2 states).
- The o/p of circuit is either low (0) OR high (1) for the logic system. The o/p is low (1) or high (0) for -ve logic system.

# System	Radix/Base	Digits/Range
1) Binary	2	0, 1
2) decimal	10	0, 1, 2 --- 9
3) octal	8	0, 1, 2, 3, --- 7
4) Hexa-decimal	16	0, 1, 2 -- 9, A B C ... F

(No of symbol = x) / (Range 0, → x-1)

Note: 1) for any radix (R) range will be zero to (r-1)
2) Each digit is called as Bit.
3) Group of 4 Bits is called as Nibble.
4) Group of 8 Bits is called as 1 Byte.

(1) Decimal Number system :-
(Base is 10, range zero to nine)

[Decimal to Binary Conversion]

•) its obtained by ÷ the decimal no by 2 until remainder is zero or one is obtained

MSB = Most significant Bit

•) Binary no is obtained by taking the remainder after each division in the reverse order.

ⓐ $(2)_{10} = (10)_2$

2	2	1
	0	0

ⓑ $(53)_{10} \Rightarrow (110101)_2$

2	53	1 → LSB
2	26	0
2	13	0
2	6	1
2	3	0
2	1	1 → MSB

ⓒ $(0.625)_{10} = (1010\quad)_2$

0.18 × 2 = 0.360 0
0.360 × 2 = 0.720 0
0.720 × 2 = 1.440 1
0.440 × 2 = 0.880 0

2	18	0
2	9	1
2	4	0
2	2	0
	1	

ⓓ $(41)_{10} = (101001)_2$

2	41	1
2	20	0
2	10	0
2	5	1
2	2	0
	1	

ⓔ $(18.18)_{10}$ $(10010.0010)_2$

(Decimal to Octal)

1) $(214)_{10} = (326)_8$

8	214	6
8	26	2
8	3	

2) $(214.56)_{10} = (326.4365)_8$

$0.56 \times 8 = 4.48$ (4)
$0.48 \times 8 = 3.84$ (3)
$0.84 \times 8 = 6.72$ (6)
$0.72 \times 8 = 5.76$ (5)

3) $(783.38)_{10} = (1417.3024)_8$

8	783	
8	97	7
8	12	1
	1	4
	1	

$0.38 \times 8 = 3.04$ (3)
$0.04 \times 8 = 0.32$ (0)
$0.32 \times 8 = 2.56$ (2)
$0.56 \times 8 = 4.48$ (4)

(Decimal to Hexadecimal)

① $(15)_{10} = (F)_{16}$

16	15

② $(987)_{10} = (3DB)_{16}$

16	987	
16	61	B (11)
	3	D (13)
	3	

③ $(357.35)_{10} = (165.599)_{16}$

$0.35 \times 16 = 5.6$ (5)
$0.6 \times 16 = 9.6$ (9)
$0.6 \times 16 = 9.6$ (9)

16	357	
16	22	5
16	1	6
	1	

Note: Decimal to any radix conversion
(i) D

(ii) The no is obtained by taking the division

for fractional part multiply the decimal No by radix are continuously recording a carry in the integer position each time. carries in forward order gives the required radix No.

(Conversion of any radix into equivalent radix number)

$(a_5 a_4 a_3 a_2 a_1 a_0 . a_{-1} a_{-2} a_{-3})_r = (\ )_{10}$

↓

$(a_4 r^4 + a_3 r^3 + a_2 r^2 + a_1 r^1 + a_0 \times r^0 . a_{-1} r^{-1} + a_{-2} r^{-2} + a_{-3} r^{-3} \ldots)_{10}$

0 1 2 3 4 5 6 7 8 9 A B C D E F

$(260)_{10} = (198)_{12}$

12	260	
12	21	8
12	1	9
		1

(Binary to Decimal)

$(11011)_2 = (\ )_{10}$

$1\times2^4 + 1\times2^3 + 0\times2^2 + 1\times2^1 + 1\times2^0 = (27)_{10}$

$(10.10)_2 = (\ )_{10}$

$1\times2^4 + 0\times2^3 + 1\times2^2 + 1\times2^1 + 0\times2^0 + 1\times2^{-1} + 0\times2^{-2}$

(Hexadecimal) to Decimal):-

$(B6SF)_{16} = (\ )_{10}$

116515

$11\times16^3 + 6\times16^2 + 5\times16^1 + 15\times16^0$

$= (46687)_{10}$

(Octal to Decimal)

(i) $(630.4)_8 = (?)_{10}$

$6\times8^2 + 3\times8^1 + 0\times8^0 . 4\times8^{-1} = (408.5)_{10}$

(ii) $(123.4)_8 = (?)_{10}$

$1\times8^2 + 2\times8^1 + 3\times8^0 . 4\times8^{-1}$

$83 \times 1/2 = (83.5)_{10}$

(iii) $(153.513)_{10} = (?)_8$.

8	153	1
8	19	3
	2	2
	1	

(231)

$0.513\times8 = 4.104$ (4)

$0.104\times8 = 0.832$ (0)

$0.832\times8 = 6.656$ (6)

$0.656\times8 = 5.248$ (5)

$(231.4065)_8$

(iv) $(56026.6875)_{10} \rightarrow (?)_{16}$

10/feb/2023

{Octal no system (radix = 8)}

Decimal	octal No	Equivalent Binary
0	0	001
1	1	001
2	2	010
3	3	011
4	4	100
5	5	101
6	6	110
7	7	111
8		

{Binary to Octal}

⇒ $(1011\ 000\ 110\ 011 . 111\ 0000\ 011)_2 = (?)_8$

$(2\ 6\ 1\ 5\ 3\ 7\ 4\ 0\ 6)_8$

⇒ $(111\ 011\ 000\ 101 . 000\ 001)_2$ → base 2 to 16 → add bits

-: (Hexadecimal Number System):-

decimal no	hexadecimal	equivalent binary
0	0	0000
1	1	0001
2	2	0010
3	3	0011
4	4	0100
5	5	0101

decimal no	hexadecimal	equivalent binary
6	6	0110
7	7	0111
8	8	1000
9	9	1001
10	A	1010
11	B	1011
12	C	1100
13	D	1101
14	E	1110
15	F	1111

Q) $(2C6B.F2)_{16} = (?)_2$

$(0010\ 1100\ 0110\ 1011 . 1111\ 0010)_2$

Q) $(001\ 011\ 001 . 001\ 0010)_2 = (?)_{16}$

$(0\ B\ 9 . 24)_{16}$

* {hexadecimal to Octal & octal to hexadecimal conversion}:

Q: $(64CD)_{16} = (?)_8$

$[0110\ 0100\ 1100\ 1101]$

equivalent octal → $(0\ 6\ 2\ 3\ 1\ 0\ 5)_8$

Q: $(5071)_2 = (?)_{16}$

$[101\ 000\ 111\ 001]$

$(A\ 3\ 9)_{16}$

imp Q: $(637)_9 = (?)_5$.

$(637)_9 = (?)_{10}$ $\Rightarrow 6\times9^2 + 3\times9^1 + 7\times9^0$

$(\text{known})_{10} = (?)_5$ $\Rightarrow (520)_{10}$

5	520	0
5	104	4
5	20	0
	4	4

$(4040)_5$ Ans.

vimp

Q: $(193)_x = (623)_8$.

$1\times x^2 + 9\times x^1 + 3\times x^0 = 6\times8^2 + 2\times8^1 + 3\times8^0$

$x^2 + 9x + 3 = 384 + 16 + 3$

$x^2 + 9x + 3 = 403$

$x^2 + 9x - 400 = 0$

$\boxed{x = 16}$

[Binary Arithmetic]

1) Binary Addition :-

	Sum	carry
0+0	0	0
0+1	1	0
1+0	1	0
1+1	0	1

2) Binary Subtraction :-

	difference	Borrow
0 − 0	0	0
0 − 1	1	1
1 − 0	1	0
1 − 1	0	0

Q: Add $(28)_{10}$ $(15)_{10}$

$(28)_{10} = (11100)_2$

$(15)_{10} = (1111)_2$

$(43)_{10}$ $(101011)_2$

2	28	0
2	14	0
2	7	1
2	3	1
	1	

Q Subtract :-

$$\begin{array}{r} 1\,1\,0\,1\,1 \\ -\,1\,0\,1\,1\,0 \\ \hline 0\,0\,1\,0\,0 \end{array}$$

Imp Q subtract $(29)_{10}$ from $(38)_{10}$ in binary Arithmetic

$(29)_{10} = (11101)$

$(38)_{10} = (100110)$

$$\begin{array}{r} 100110 \\ -\;11101 \\ \hline 01001 \end{array}$$

2	29	1
2	14	0
2	7	1
2	3	1
	1	

2	38	0
2	19	1
2	9	1
2	4	0
2	2	0
	1	1

Compliment :- compliments are used in digital computer to represent negative number & simplify the substraction. it is also used for logical manipulation.

for any radix r there are two compliments

Binary < 1st compliment, 2nd compliment

radix < r^{th} comp, $r-1$ comp

Binary (2) < 1st com, 2st com

decimal (10) < 10th, 9th

octal (8) < 8th, 7th

Hexa (16) < 16th, 15th

(1S Compliment)

it results when we changed all ones to zero & all zeroes to one in binary No

Q:- find 1^{s} compliment of $(1010011)_2$
$= (0101100)_2$

(2's compliments)

it results when we add 1 to the 1^{s} compliment of a binary no.

2^{s} complement = 1^{s} complement + 1

Q: find 2^{s} complement of no $(1010011)_2$

Take 1^{s} complement	1^{s} compliment → (0101100)
0 → 1	+ 1
1 → 0	0101101

Binary substraction using 1^{s} & 2^{s} compliment

[Binary substraction using 1^{s} compliment]

→ if a binary digit $(B)_2$ is substracted from $B(A)_2$ then the following steps are followed.

1) find 1^{s} compliment of the number to be substract → B
2) Add 'A' with 1^{s} complement of B by using binary operation.
3) if final carry (1) is generated then the result will be +ve & carry will be added bit to the result.
4) if No carry goes (final) generated the result will be a (-ve) no then take 1^{s} complement for final result.

Q: Subtract $(1011)_2$ (B) from $(0100)_2$ (A) using 1^s complement

$+(-B)$ $(-B) \rightarrow 1^{s}$ complement

$$\begin{array}{r} 0100 \\ +\ 0100 \\ \hline 1000 \end{array}$$

No carry means take 1^s complement.

final answer: $\boxed{-0111}$ Ans

Q: Subtract $(4)_{10}$ from $(9)_{10}$ using 1^s complement

$$\begin{array}{r} 1001 \\ +\ 1011 \\ \hline (1)\ 1100 \end{array}$$

$+1$

$0100 =$

2	4	0
2	2	0
	1	1

carry available → (+ve) and carry add +1.

$$\begin{array}{r} 0100 \\ +\ 1 \\ \hline 0101 \end{array}$$ Ans

2	9	1
2	4	0
2	2	0
	1	1

1001

{Binary Subtraction using 2^s complement}:

If a no $(B)_2$ is subtracted from $(A)_2$ then following steps are to be followed to perform subtraction using 2^s complement.

① → Take 2^s complement of no to be subtracted i.e implies $(B)_2$

② → Add $(A)_2$ with 2^s complement of $(B)_2$ using binary addition

③ if final carry is 1 then result be (+ve) & discard the carry.

④ if final carry is 0 then result be (-ve) & take 2^s complement of the result to get desired solⁿ.

Q: $(9)_{10} - (5)_{10}$ perform using 2^s complement.

$$\begin{array}{r} 1001 \\ 0101 \\ \hline 1010 \end{array}$$

(1001)

2	9	1
2	4	0
2	2	0
	1	1

1^s complement 1010

$+1$

1011

2	5	1
2	2	0
	1	

1001

$$\begin{array}{r} 1001 \\ +\ 1011 \\ \hline \boxed{1}\ 0100 \end{array}$$

·101

0100 — 4

$\cdot \rightarrow$ AND
$+ \rightarrow$ OR
$\bar{\cdot} \rightarrow$ NAND

Boolean Algebra.

It is a system of mathematical logic.

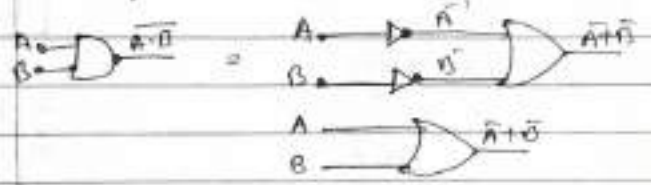
① **Duality theorem** : It is an important property of boolean algebra. It states that in a 2 valued boolean algebra the dual of an algebric expression can be obtained by interchanging OR & AND operators and by replacing 1^s by 0^s & 0^s by 1^s.

∴ (Demorgan's theorem) :-

Demorgan suggested two theorems:

$$\boxed{\overline{AB} = \bar{A}+\bar{B}} \quad \text{— eq ①}$$

- The compliment of a product is equal to the sum of the compliments.



(NAND ⟷ Bubbled OR)

$$\boxed{\overline{A+B} = \bar{A}\cdot\bar{B}} \quad \text{— eq ②}$$

- Compliment of a sum is equal to product of the compliment

(NOR) ⟷ Bubbled AND)

Q: Simplify the following Eq^n :-

(i) $Y = \overline{(\overline{AB}+\bar{A}+AB)}$

Ans: $= (\bar{A}+\bar{B}+\bar{A}+AB)$ $\quad (\because \overline{AB} = \bar{A}+\bar{B})$

$Y = (\bar{A}+\bar{B}+AB)$

$= \bar{\bar{A}}\cdot\bar{\bar{B}}\cdot\overline{AB}$

$= A\cdot B\cdot(\bar{A}+\bar{B})$

$= A\bar{A}B + AB\bar{B} \quad = 0+0 = 0$

Postulates	(a)	(b)
• Identity elements	$A+0=A$	$A\cdot 1 = A$
•	$A+\bar{A}=1$	$A\cdot\bar{A}=0$
• Commutative	$A+B=B+A$	$AB=BA$
• Distributive	$A(B+C)=AB+AC$	$A+BC=(A+B)(A+C)$
Theorem ①	$A+A=A$	$A\cdot A=A$
Theorem ②	$A+1=1$	$A\cdot 0=0$
Theorem ③ (Involution)	$\bar{\bar{A}}=A$	
Theorem ④ (Absorption)	$A+AB=A$	$A(A+B)=A$
Theorem ⑤	$A+\bar{A}B=A+B$	$A\cdot(\bar{A}+B)=AB$
Theorem ⑥ (Associative)	$A+(B+C)=(A+B)+C$	$A(BC)=(AB)C$
Demorgan	$\overline{A+B}=\bar{A}\cdot\bar{B}$	$\overline{AB}=\bar{A}+\bar{B}$

Q: Minimise given boolean Expression:

$$Y = AB+\overline{AC}+A\bar{B}C(AB+C)$$

Ans:- $Y = AB+\bar{A}+\bar{C}+A\bar{B}C(AB+C) \quad \because \overline{AC}=\bar{A}+\bar{C}$

$= AB+\bar{A}+\bar{C}+\underbrace{A\bar{B}CAB}_{(B\bar{B}=0)}+A\bar{B}C$

$= \underbrace{AB+\bar{A}}_{(A+\bar{A}B=A+B)}+\bar{C}+A\bar{B}C$

$\Rightarrow B + \bar{A} + \bar{C} + A\bar{B}C$

$= B + \bar{C} + A + \bar{B}C$

$= B + C + \bar{C} = B + 1 = 1$

Q: $\bar{A}B\bar{C}D + \bar{A}BCD + ABD$

$\bar{A}BD(\bar{C} + C) + ABD$

$\bar{A}BD + ABD$

$BD(\bar{A} + A)$

BD.

{Logic Gates}:-

The electronic or digital circuits which have ability to make logical decisions by producing output under certain input conditions are known as logic gates.

* (Types of logic gates) *

Basic gates	universal	Special Purpose
① AND	① NOR	① EXOR/XOR
② OR	② NAND	② X-NOR.
③ NOT		

① NOT Gate:- • The logic circuit which perform NOT.

- NOT operator represents logical inversion or complement. (NOT operator is denoted by bar over the variable to be inverted.

13/Feb/2023

* Symbol:- (NOT Gate)

(input) A —▷o— $\bar{A}$ (output)

Truth Table:

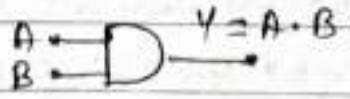
A table that list all the posible combination of the input variables & corresponding op is known as truth table

(Input)	(output)
0	1
1	0

* Boolean Expression:- $Y = \bar{A}$

(2) AND Gate:- It performs 'and' operations here AND respresents logical multiplication its denoted by '.' b/w variables to be multiplied

* Symbol:- (AND GATE)



Truth table.

input		output
0	0	0
0	1	0
1	0	0
1	1	1

Boolean Expⁿ:- $Y = A \cdot B$.

(3) OR Gate:- it performs 'OR' operations which is logical addition $(1+1)=1$, its denoted by '+' sign b/w the variables to be added.

Symbol:-

Boolean Expⁿ:- $Y = A+B$

Truth Table:-

Input		output
A	B	
0	1	1
0	0	0
1	0	1
1	1	1

(Universal Gates)

1) NAND Gates: The term 'NAND' can be splitted as 'AND-NOT' which means that NAND operation can be implemented with the combination of AND gate & NOT gate.

NAND is also known as 'Universal gate' because all the gates can be implemented using NAND gates

Symbol:-

Truth table:-

Input		output
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

(2) NOR Gates:- The term 'NOR' can be splitted as 'NOT-OR' gate which means that NOR operation can be implemented with the combination of OR gate & NOT gate. its also a known as 'universal gate as all the gates can be implemented using NOR gates.

Symbol:-

Truthtable:-

Input		output
A	B	$Y = A+B$
0	0	1
0	1	0
1	0	0
1	1	0

Boolean Expⁿ:-

$Y = \overline{A + B}$

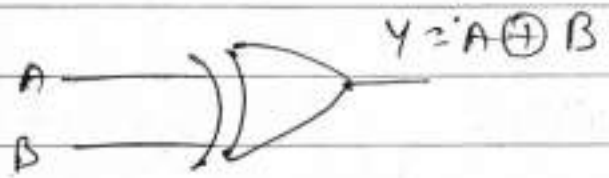
(Special purpose Gates)

Ex-OR / X-OR:

- The exclusive OR gate is abbreviated as XOR, it performs XOR operations which is denoted by ⊕ b/w input variable.

Note:- When both input are same (A = B) then o/p is low otherwise high.

Symbol:-



(Truth table)

Input		Output
(a)	(b)	
0	0	0
0	1	1
1	0	1
1	1	0

* Boolean Expression:

$$Y = A \oplus B.$$

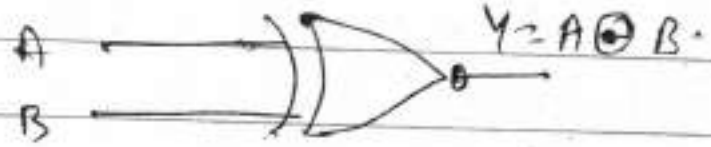
exclusive

(2) EX-NOR / X-NOR gate

The exclusive NOR gate is abbreviated as XNOR. XNOR gate is equivalent to XOR gate followed by NOT gate.

Note:- when both inputs are same the o/p will be high otherwise low.

Symbol:-



Truth table

Input		Output
A	B	
0	0	1
0	1	0
1	0	0
1	1	1

Boolean Expression.

$$Y = A \odot B$$

(Boolean Expressions)

Boolean Expressions are constructed by connecting Boolean constants & variables with the Boolean operations

14/feb — $f(A,B,C,D) = AB + CD = Y$.

Boolean function is described by algebraic expression called Boolean Expression which consists of binary variables & logical symbols its of two types.

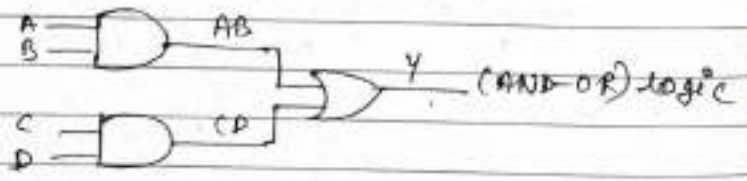
1) POS forms
2) SOP forms

1) (SOP Forms) (Sum of Products)

This form expression contains two or more "AND" terms all together (ORed)

$f(A,B,C,D) = \underbrace{AB}_{\text{Product}} + \overbrace{CD}^{\text{Product}}$ } Logical implementation

-: {Hardware implementation}:-



2) (POS forms) (Product of sum)

This form expression contains 2 or more 'OR'

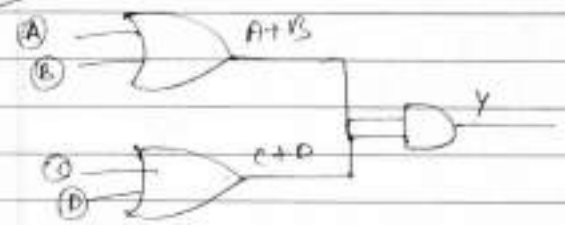
terms ended together.

function Ex:

$$f(A,B,C,D) = \underbrace{(A+B)}_{\text{sum term}} \overset{\text{AND}}{\cdot} \underbrace{(C+D)}_{\text{sum term}}$$

Logical implementation

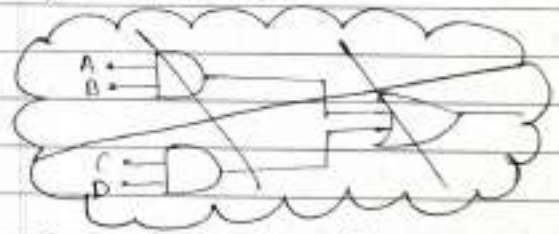
Hardware IMPLEMENT

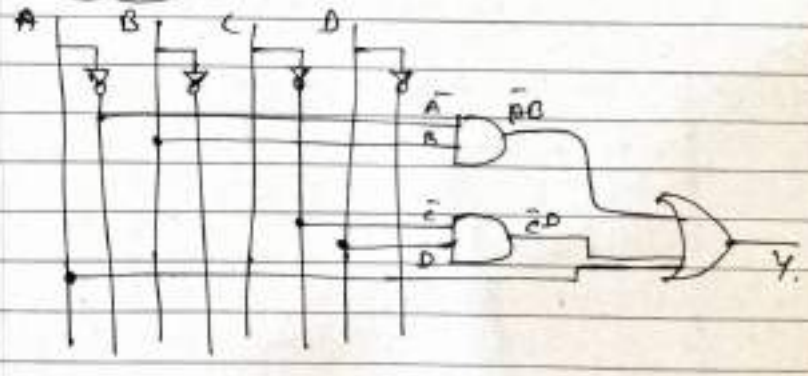


(OR-AND) logic

Q: implement the given Expression using basic gates (NOT, AND, OR)?

(i) $f = \bar{A}B + \bar{C}D + A$





Most IMP

:- {Standard/Canonical SOP & POS forms} :-

1.> Generally the SOP & POS expression does not contains all the variables.

2.> if each term of (SOP) & (POS) expression contains all the variables / literals then its called canonical or standard form.

(Conversion of SOP into Standard SOP) # (canonical SOP / minterm form) other name

Step ①:- find the missing literal in each product term (if any).

Step ②:- AND each product term by 'ORing' the literal and its compliment.

Q:- Convert the given expression in Standard SOP form ?

(i) $f(A,B,C) = AC + AB + BC$

B missing, C missing, A missing.

$= AC(B+\bar{B}) + AB(C+\bar{C}) + BC(A+\bar{A})$

Ans:- $= [ABC + A\bar{B}C + ABC + AB\bar{C} + BCA + BC\bar{A}]$

repeated terms kio ek bar likho bss.

$[ABC + A\bar{B}C + AB\bar{C} + \bar{A}BC]$

(POS standard/ canonical form/MAX term form)

Step① : find the missing variable in each sum term (if any)

Step② : OR each sum term by ANDing the literal and its compliment.

Q. Convert the given expression in standard POS form :

$$f(A, B, C) = (A+B)(B+C)(A+C)$$

C missed. A missed B missed

Ans :

$$(A+B+C\bar{C}) \cdot (A\bar{A}+B+C) \cdot (A+B\bar{B}+C)$$

$$\Rightarrow (A+B+C)(A+B+\bar{C}) \cdot (A+B+C)(\bar{A}+B+C) \cdot (A+B+C) \cdot (A+\bar{B}+C)$$ Ans

Q. $f(ABC) = A + BC + ABC$ (into SOP)

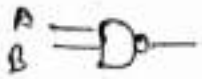
BC missing A ×

$$A(B+\bar{B})(C+\bar{C}) + BC(A+\bar{A}) + ABC$$

$$ABC + A\bar{B}C + A\bar{B}\bar{C} + ABC + \bar{A}BC + ABC$$

$$= ABC + A\bar{B}\bar{C} + \bar{A}BC$$ Ans

✓ = same term.



14/feb/2023
163

IMPORTANT

(AND OR) (SOP)
+ ·

{NAND-NAND IMPLEMENTATION}

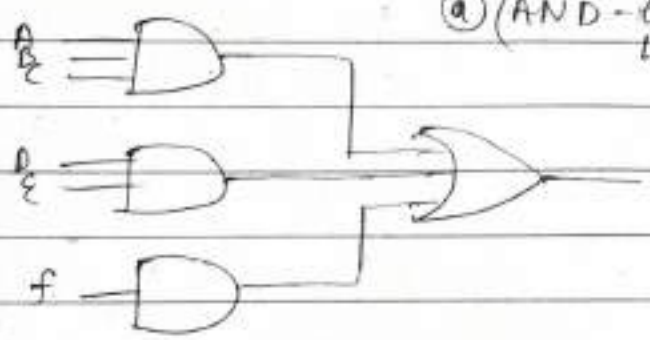
for NAND-NAND the function should be in SOP form.

Q:- Simplify the given boolean function using NAND-NAND logic? [AND-OR Logic]
$(Y = ABC + DE + F)$

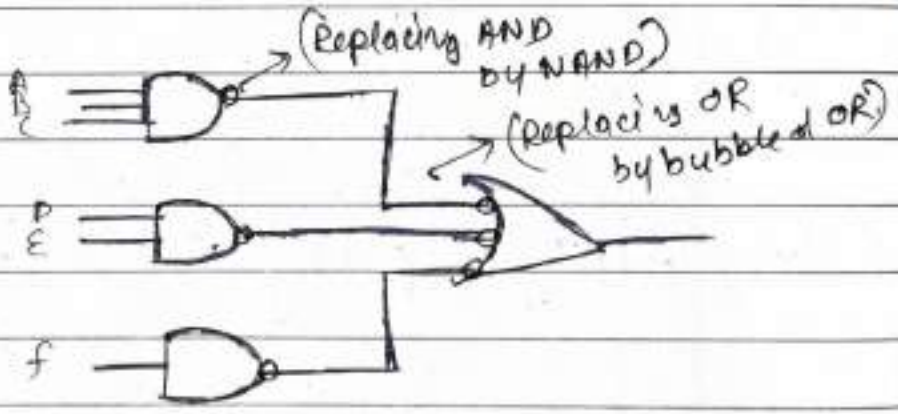
Ans:

Stage ① :

ⓐ (AND-OR LOGIC)



ⓑ AND-OR logic.

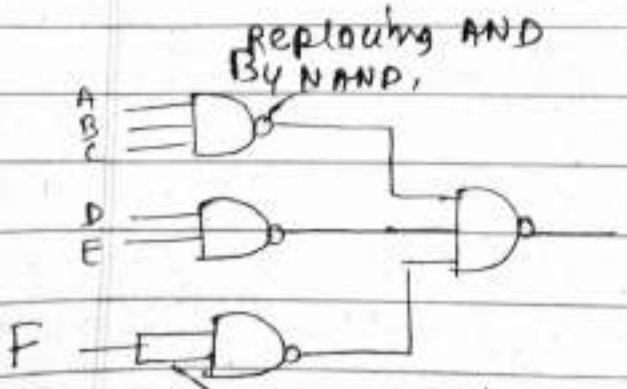


* (By demorgan's theorem).

$\overline{A \cdot B} = \bar{A} + \bar{B}$

NAND = Bubbled OR.

Demorgan



$A \cdot B$ = AND $\quad \bar{A} \cdot \bar{B}$ = Bubbled AND

$\overline{A \cdot B}$ = NAND

15/Feb/2023
164

A/c Demorgan $\boxed{\text{NOR = Bubbled AND}}$

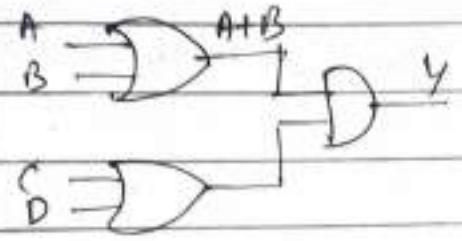
{NOR - NOR IMPLEMENTATION}

for NOR-NOR implementation function must be in POS form.

Q. Implement given expression using NOR-NOR logic?

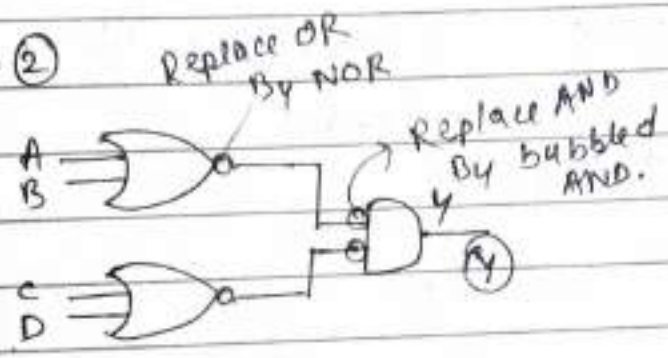
$$Y = (A+B) \cdot (C+D) \rightarrow \text{POS}$$

Ans: Step ① = Release using basic gate.



[OR-AND logic]

Step ②



OR)

* By Demorgan's.

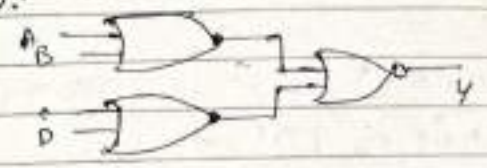
$\overline{A+B} = \bar{A} \cdot \bar{B}$

NOR = Bubbled AND

NOR-NOR → POS
NAND-NAND → SOP

15/feb/2023
165

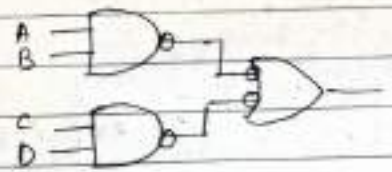
step③:-



Q:- Realise using Boolean Expression.

$F = AB + CD$ (SOP)

ⓐ NAND-NAND.



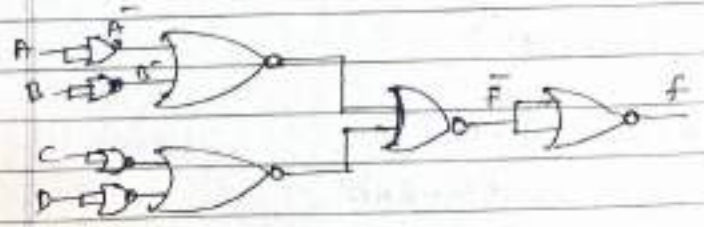
By Demorgan's
Bubbled OR = NAND

ⓑ NOR-NOR $f = AB + CD$ - SOP.

using Demorgan.

$\bar{F} = \overline{AB+CD}$

$\bar{f} = (\bar{A}+\bar{B}) \cdot (\bar{C}+\bar{D})$ → POS.

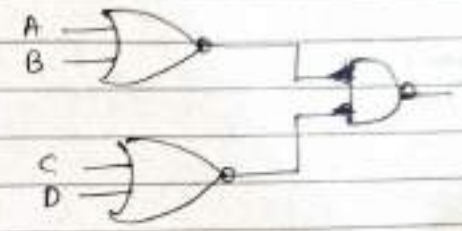


15/feb/2023
166

Q Realise the given function using NAND NAND, NOR, NOR logic.

$F = (A+B) \cdot (C+D)$ ← POS

Ans:- NOR-NOR Logic.



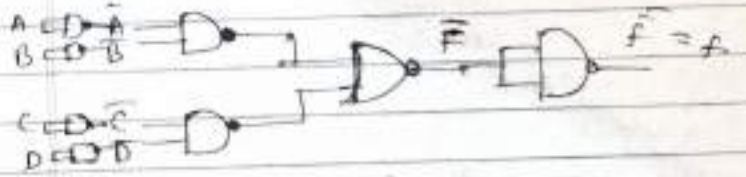
NAND-NAND logic.

$f = (A+B) \cdot (C+D)$ - POS

using Demorgan's

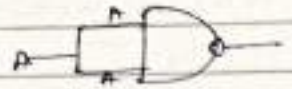
$\bar{f} = \overline{(A+B) \cdot (C+D)}$

$(\bar{A}\bar{B}) + (\bar{C}\bar{D})$ ← SOP



Q (realise all the gates from NAND gates)

(1) NOT gate.



$A \longrightarrow \bar{A}$

$\overline{A \cdot A}$

$= \bar{A}$

(2) AND gate.

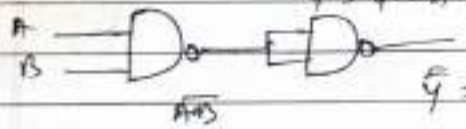
$\overline{A \cdot B} = AB$

$Y = A \cdot B$

$\bar{Y} = \overline{A \cdot B}$

$\bar{Y} = ?$

$Y = \bar{\bar{Y}} = A \cdot B$



$\bar{Y} = \overline{\overline{A \cdot B}} = A \cdot B$.

(3) OR Gate:

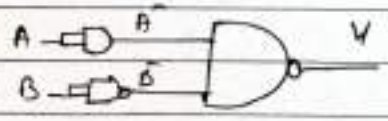
$Y = A + B$

using Demorgan's : $\bar{Y} = \overline{A + B}$

$Y = (\bar{A} \cdot \bar{B})$

$Y = \bar{\bar{Y}} = \overline{\bar{A} \cdot \bar{B}}$

$Y = A \cdot B$



(4) NOR Gate.

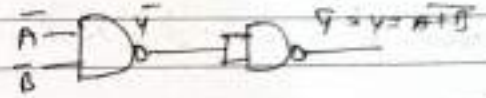
$Y = (\overline{A + B})$

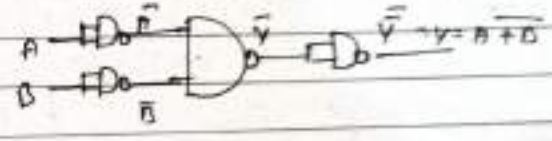
using Demorgans.

$Y = \bar{A} \cdot \bar{B}$ AND

$\bar{Y} = \overline{\bar{A} \cdot \bar{B}}$ NAND

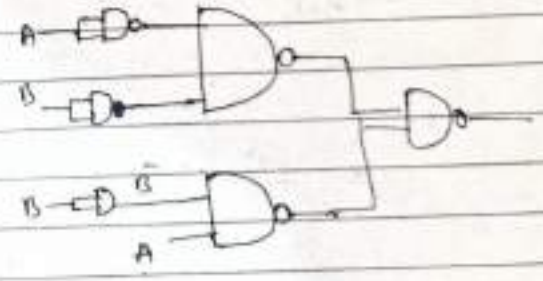
$\bar{\bar{Y}} = \overline{\overline{\bar{A} \cdot \bar{B}}} = Y$





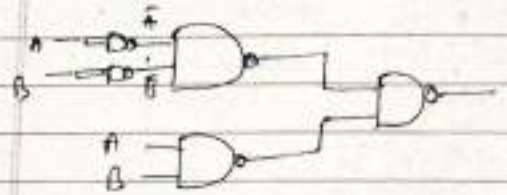
(5) XOR Gate:

$Y = (\bar{A}B + \bar{B}A)$ → SOP



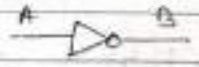
(6) X-NOR.

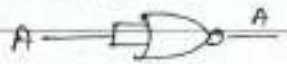
$Y = \bar{A}\cdot\bar{B} + AB$. SOP.



Q. # (Realise all gates using NOR) #

(1) NOT Gate:-





$\bar{A}+A$
$= \bar{A}$

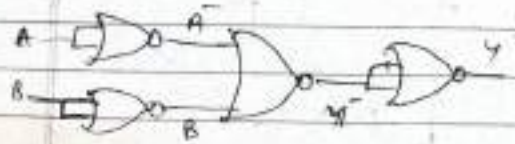
(2) AND $Y = A\cdot B$

Apply Demorgan.

$\bar{Y} = \overline{A\cdot B}$

$\bar{Y} = \bar{A}+\bar{B}$

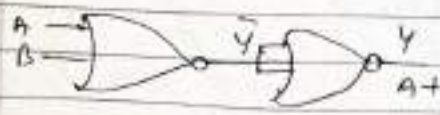
$\bar{\bar{Y}} = Y = \overline{\bar{A}+\bar{B}}$



(3) OR Gate $Y = A+B$.

$\bar{Y} = \overline{A+B}$ } NOT

$\bar{\bar{Y}} = \overline{\overline{A+B}}$ } NOR



$A+B = Y$

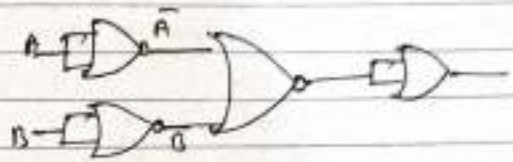
(4) NAND gate

$Y = \overline{A\cdot B}$

$Y = \bar{A}+\bar{B}$

$\bar{Y} = \overline{\bar{A}+\bar{B}}$

$\bar{\bar{Y}} = \overline{\overline{\bar{A}+\bar{B}}}$ } NOT NOR



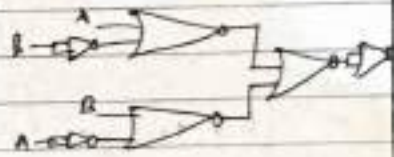
(5) EX-OR.

$Y = \bar{A}\cdot B + \bar{B}A$

$\bar{Y} = \overline{\bar{A}B + \bar{B}A}$

$\bar{\bar{Y}} = \overline{(\bar{A}+B)\cdot(\bar{B}+A)}$

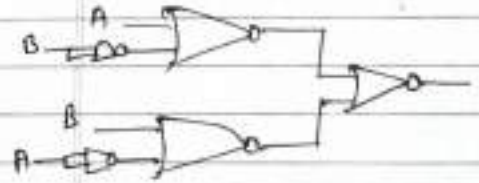
$\bar{\bar{Y}} = \overline{(\bar{A}+B)} + \overline{(\bar{B}+A)}$



(6) EX-NOR.

$Y = \bar{A}B + \bar{B}A$

$Y = (A+B)\cdot(B+\bar{A})$



M - Notations (Minterms & Maxterms)

Minterms :- Each individual term in standard SOP form is called minterms.

→ In this case complement term is represented by 0 and non-complement term is by 1.

→ It is denoted by (m). & given by the expression $Y = \Sigma m(\ )$.

Q. $f(A,B,C,D) = \bar{A}BCD + A\bar{B}\bar{C}D$.

0111 1001

$f = \Sigma m(7,9)$

Maxterms :- Each individual term in the standard POS form is called maxterm.

→ The complement is represented by 1 & non-complement term by 0.

→ This is denoted by (M) & given by the expression $Y = \pi M(\ )$.

Q. $f(A,B,C,D) = (\bar{A}+B+C+D) \cdot (\bar{A}+\bar{B}+C+D)$

(1000) (1100)

8 12

$Y = \pi M(8,12)$

Note :- Minterm & Maxterms are complementary to each other.

$F(A,B,C,D) = \Sigma m(0,2,6,7,13)$ ← complementary to each other.

↳ SOP

⇓ Same fun^n.

⇓ POS ?

$f(A,B,C,D) = \pi M(1,3,4,5,8,9,10,11,12,14,15)$

Variable.	Minterms.	Maxterms.
A B C	m_i	M_i
0 0 0	$\bar{A}\bar{B}\bar{C} = m_0$	$A+B+C = M_0$
0 0 1	$\bar{A}\bar{B}C = m_1$	$A+B+\bar{C} = M_1$
0 1 0	$\bar{A}B\bar{C} = m_2$	$A+\bar{B}+C = M_2$
0 1 1	$\bar{A}BC = m_3$	$A+\bar{B}+\bar{C} = M_3$
1 0 0	$A\bar{B}\bar{C} = m_4$	$\bar{A}+B+C = M_4$
1 0 1	$A\bar{B}C = m_5$	$\bar{A}+B+\bar{C} = M_5$
1 1 0	$AB\bar{C} = m_6$	$\bar{A}+\bar{B}+C = M_6$
1 1 1	$ABC = m_7$	$\bar{A}+\bar{B}+\bar{C} = M_7$

~~# (KMAP) #~~ ~~(Karnaugh (K) Map)~~ :-

Q. Express given boolean expression as a sum of min terms & product of max terms?

$F = A + \bar{B}C$ SOP

↓ ↓

BC mins A mins

$(A(B+\bar{B})(C+\bar{C}) + (A+\bar{A})\bar{B}C$

$ABC + AB\bar{C} + \bar{A}BC + A\bar{B}C$

(111) (110) (001) (101)

Jaha bar hai value = 0
wice versa = 1

16/Feb/2023.
173

$ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC + \bar{A}\bar{B}C$

(111) (110) (101) (100) (101) (001)

7 6 5 4 5 1

$\Sigma m(1,4,5,6,7)$

$F = A + \bar{B}C$

$(A + B\bar{B} + C\bar{C}) + (A\bar{A} + \bar{B}\bar{C})$

$[(A+B) \cdot (A+\bar{B})]$

$(A+B+C)(A+B+\bar{C})(A+\bar{B}+C)(A+\bar{B}+\bar{C})$

$[A+\bar{B}+C][A+\bar{B}+\bar{C}]$

$[A+B+C][A+\bar{B}+C]$

$\pi M(2,3,0)$.

* (KMAP) *

- The KMAP is a graphical representation that provides a systematic method to simplify the boolean Expression.

- The simplified expression produced by KMAP is always in one of the forms can be SOP form & can be POS form.

- The requirement of Number of cells is equal to 2^n (n = no of variables).

* In a KMAP minterms are marked by 1's & maxterms are marked by 0's.

(2 Variable KMAP)

$n=2$ cells = 4.

A \ B	$\bar{B}$ 0	B 1
$\bar{A}$ 0	0	1
A 1	2	3.

(3 Variable KMAP)

$n=3$, cells = 8.

(SOP Minterm Representation)

A \ BC	00	01	11	10
0	0	1	3	2
1	4	5	7	6

A \ BC	00	01	11	10
0	$\bar{A}\bar{B}\bar{C}$	$\bar{A}\bar{B}C$	$\bar{A}BC$	$\bar{A}B\bar{C}$
1	$A\bar{B}\bar{C}$	$A\bar{B}C$	ABC	$AB\bar{C}$

POS (Maxterm Representation)

A \ BC	00	01	11	10
0	$A+B+C$	$A+B+\bar{C}$	$A+\bar{B}+\bar{C}$	$A+\bar{B}+C$
1	$\bar{A}+B+C$	$\bar{A}+B+\bar{C}$	$\bar{A}+\bar{B}+\bar{C}$	$\bar{A}+\bar{B}+C$

4 Variable KMAP

AB \ CD	00	01	11	10
00	0	1	3	2
	4	5	7	6
	12	13	11	10
	8	9	10	14

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

(Pairing / grouping of cells)

1. Pair (2 ones)
2. quad (4 ones)
3. Octet (8 ones)

[Simplify the given function using KMAP?]

$f(A,B) = \Sigma(1,2,3)$ (By KMAP)

A \ B	0	1
0		1
1	1	1

$f = A+B$

(By Boolean Algebra)

$f = 01, 10, 11$

$\bar{A}B + A\bar{B} + AB$

$\bar{A}B + A(B+\bar{B})$

$\bar{A}B + A$

$(\bar{A}+A)(B+A)$

$1 \cdot (B+A)$.

(Simplify using KMAP).

$f(x,y,z) = \Sigma(2,3,4,5)$

x \ yz	00	01	11	10
0			1	1
1	1	1		

$\bar{x}y$

$x\bar{y}$

$f = x\bar{y} + \bar{x}y$.

Q. Simplify the given expression using KMAP
$f(x,y,z) = \Sigma(3,4,6,7)$

$x \backslash yz$	00	01	11	10
0	0	1	3	2
1	4	5	7	6

Q. Simplify
$f(x,y,z) = \Sigma(0,2,4,5,6)$

$x \backslash yz$	00	01	11	10
0	1			1
1	1	1		1

$\bar{z}$

$x\bar{y}$

Pair

Quad

$f = x\bar{y} + \bar{z}$

Q. Simplify
$f(x,y,z) = \Sigma(0,2,4,5)$

$x \backslash yz$	00	01	11	10
0	1			1
1	1	1		

$\bar{x}\bar{z}$

$x\bar{y}$

$f = x\bar{y} + \bar{x}\bar{z}$

Q. $f(x,y,z) = \Sigma(0,1,2,3,5)$

$x \backslash yz$	00	01	11	10
0	1	1	1	1
1		1		

Quad $\bar{x}$

$\bar{y}z$

$f = \bar{x} + \bar{y}z$ Ans.

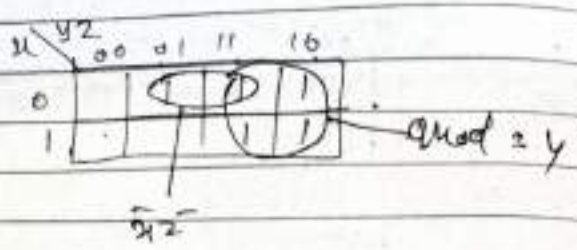
Q:- $f(x,y,z) = \Sigma(1,2,3,7)$

$x \backslash yz$	00	01	11	10
0		1	1	1
1			1	

3 Pairs.

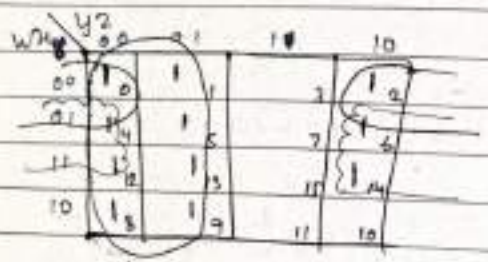
$\Rightarrow f = \bar{x}z + \bar{x}y + yz$

Q. $f(x,y,z) = \{(1,2,3,6,7)$



$= \bar{x} + yz$

Q: $f(w,x,y,z)$.
$= \Sigma(0,1,2,4,5,6,8,9,12,13,14)$



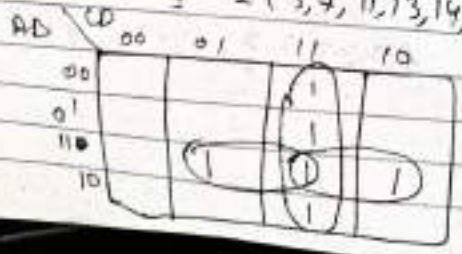
octet

2 Quads.

1 octet 2 Quads

$f = \bar{y} + x\bar{z} + \bar{w}\bar{z}$

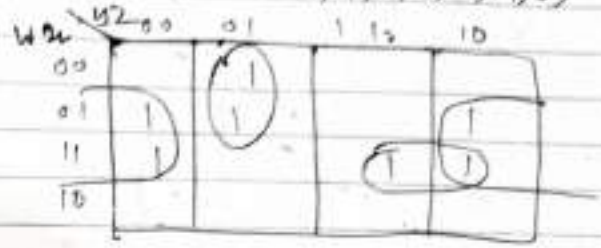
Q: $f(A,B,C,D)$
$= \Sigma(3,7,11,13,14,15)$



2 Quad
2 Paired

$f = CD + ABC + ABD$.

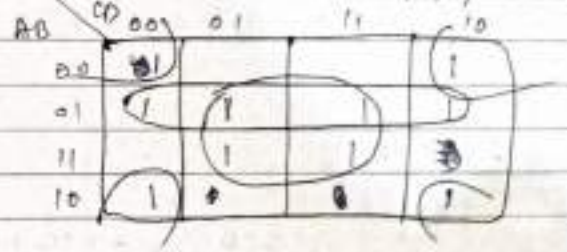
Q: $f(w,x,y,z) = \Sigma(1,4,5,6,13,14,15)$



2 Pair, 1 Quad.

$f = \bar{w}\bar{y}z + wxy + xz$

Q: $f(A,B,C,D) = \Sigma(0,2,4,5,6,7,8,10,13,15)$



$BD + \bar{B}\bar{D} + \bar{A}B$
OR
$BD + \bar{B}\bar{D} + \bar{A}D$

Both Are Soln.

17/feb/2023
183

Q. $f(ABCD) = \Sigma(0,2,3,5,7,8,9,10,11,13,15)$

AB \ CD	00	01	10	11
00	1		1	1
01		1	1	
10		1	1	
11	1	1	1	1

4 Quads.

Possible Outcomes.

$BD + \bar{B}\bar{D} + CD + AD$

$BD + \bar{B}\bar{D} + CD + A\bar{B}$

$BD + \bar{B}\bar{D} + \bar{B}C + AD$

$BD + \bar{B}\bar{D} + \bar{B}C + A\bar{B}$

Q. $f(ABCD)$

$= \bar{A}\bar{B}\bar{C} + \bar{B}C\bar{D} + \bar{A}BC\bar{D} + A\bar{B}\bar{C}$

0001 0010 0110 1001

0000 1010 1000

AB \ CD	00	01	11	10
00	1	1		1
01				1
11				
10	1	1		

2 Quads. 1 Pair

Σ = minterm. (Fill by 1)

Π = maxterm (Fill by 0)

17/feb/2023
184

$(\bar{B}\bar{D} + \bar{B}\bar{C} + \bar{A}C\bar{D})$ Ans

Q. Simplify using KMAP. (POS) Maxterm

$F(ABCD) = \Pi[1,3,5,7,12,13,14,15]$

AB \ CD	00	01	10	10
00		0	0	
01		0	0	
11	0	0	0	0
10				

$F = (A+\bar{D}) \cdot (\bar{A}+\bar{D})$

Maxterm.

Q. $f(ABCD) = \Pi(1,3,6,9,11,12,14)$

AB \ CD	00	01	10	10
00		0	0	
01				0
11	0			0
10		0	0	

2 Quad, 2 Pair.

$(\bar{B}D) + (B + D)$

$(\bar{B}+\bar{D}) \cdot (\bar{A}+\bar{B}+\bar{D}) \cdot (\bar{B}+\bar{C}+D)$

(IMPORTANT)

Q Simplify the given boolean function using KMAP

(i) SOP form (ii) POS form.

$f(ABCD) = \Sigma(0,1,2,5,8,9,10)$

AB \ CD	00	01	11	10
00	1	1		1
01		1		
11				
10	1	1		1

1 Quad 2 Pair.

$\bar{B}\bar{D} + \bar{B}\bar{C} + \bar{A}\bar{C}D$

(ii) POS.

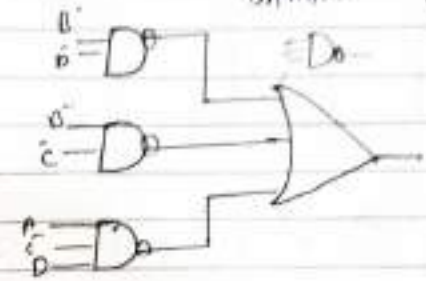
$f(ABCD) = \pi(3,4,6,7,11,12,13,14,15)$

AB \ CD	00	01	11	10
00			0	
01	0		0	0
11	0	0	0	0
10			0	

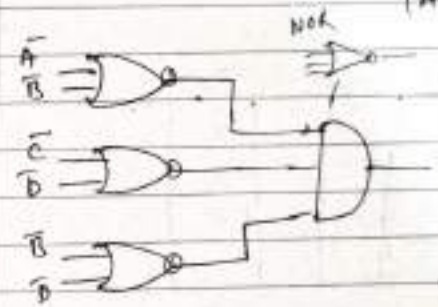
$(\bar{A}+\bar{B})\cdot(\bar{C}+\bar{D})\cdot(\bar{B}+D)$

(iii) Draw basic logic gates...

on NAND $\bar{B}\bar{D} + \bar{B}\bar{C} + \bar{A}\bar{C}D$.



$(\bar{A}+\bar{B})(\bar{C}+\bar{D})(\bar{B}+D)$



(KMAP using Don't care condition)

Note: Don't care conditions are filled by cross (-x)

Q (Simplify the given expression using KMAP)?

$f(w,x,y,z) = \Sigma(1,3,7,11,15)$
$d(w,x,y,z) = \Sigma(0,2,5)$

17/Feb/2024
187

(a) SOP

wx \ yz	00	01	11	10
00	x	1	1	x
01		x	1	
11			1	
10			1	

Ans1 $(\bar{w}\bar{x}+y)$

$(yz+\bar{w}z)$ Ans2

$(y+z)\cdot(w+\bar{z})$

(b) POS.

wx \ yz	00	01	11	10
00	x			x
01	0	x		0
11	0	0		0
10	0	0		0

$f = z\cdot(\bar{w}+y)$ Ans

Q. Solve the function using KMAP?

$f(ABCD) = \Sigma(0,6,8,13,14) + d(2,4,10)$

AB \ CD				
	1			x
	x			1
		1		1
	1			x

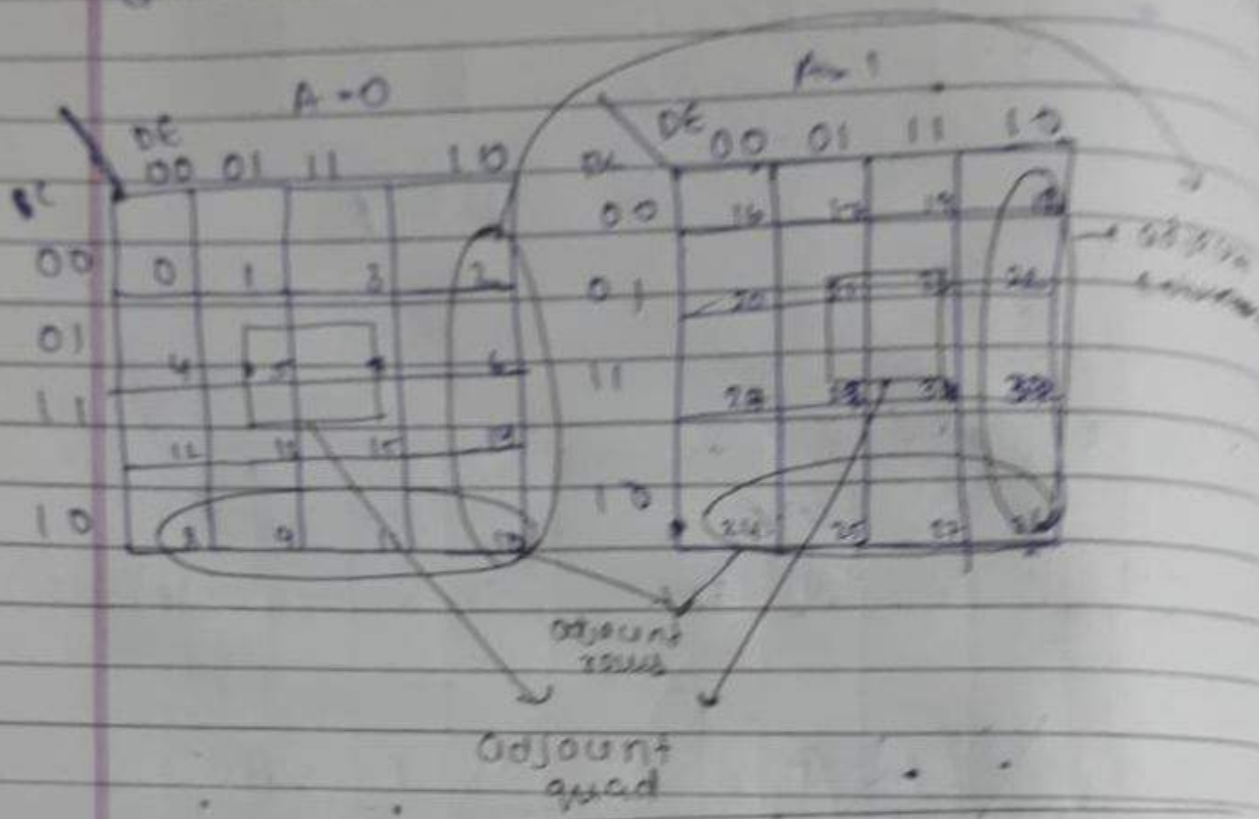
2 Quad 1 single

$\bar{B}\bar{D}+C\bar{D}+AB\bar{C}$

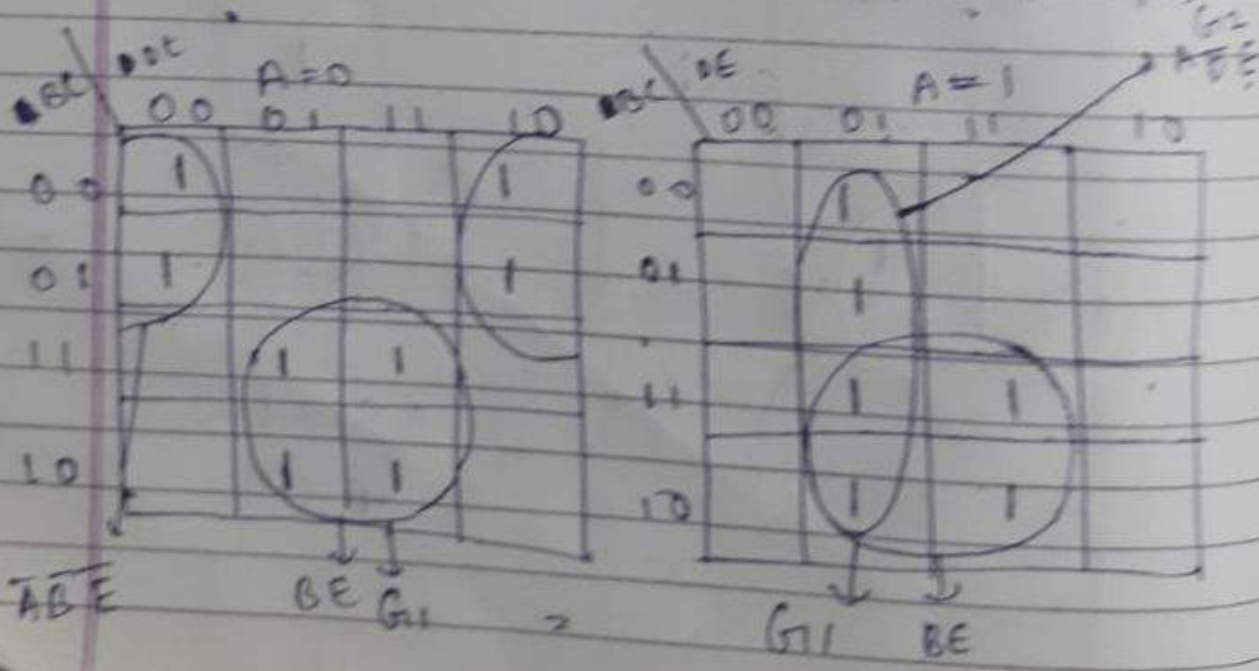
→ 5 variable K map :

$n = 5$ (no of variables)

$2^n = 2^5 = 32$ (no of cells)

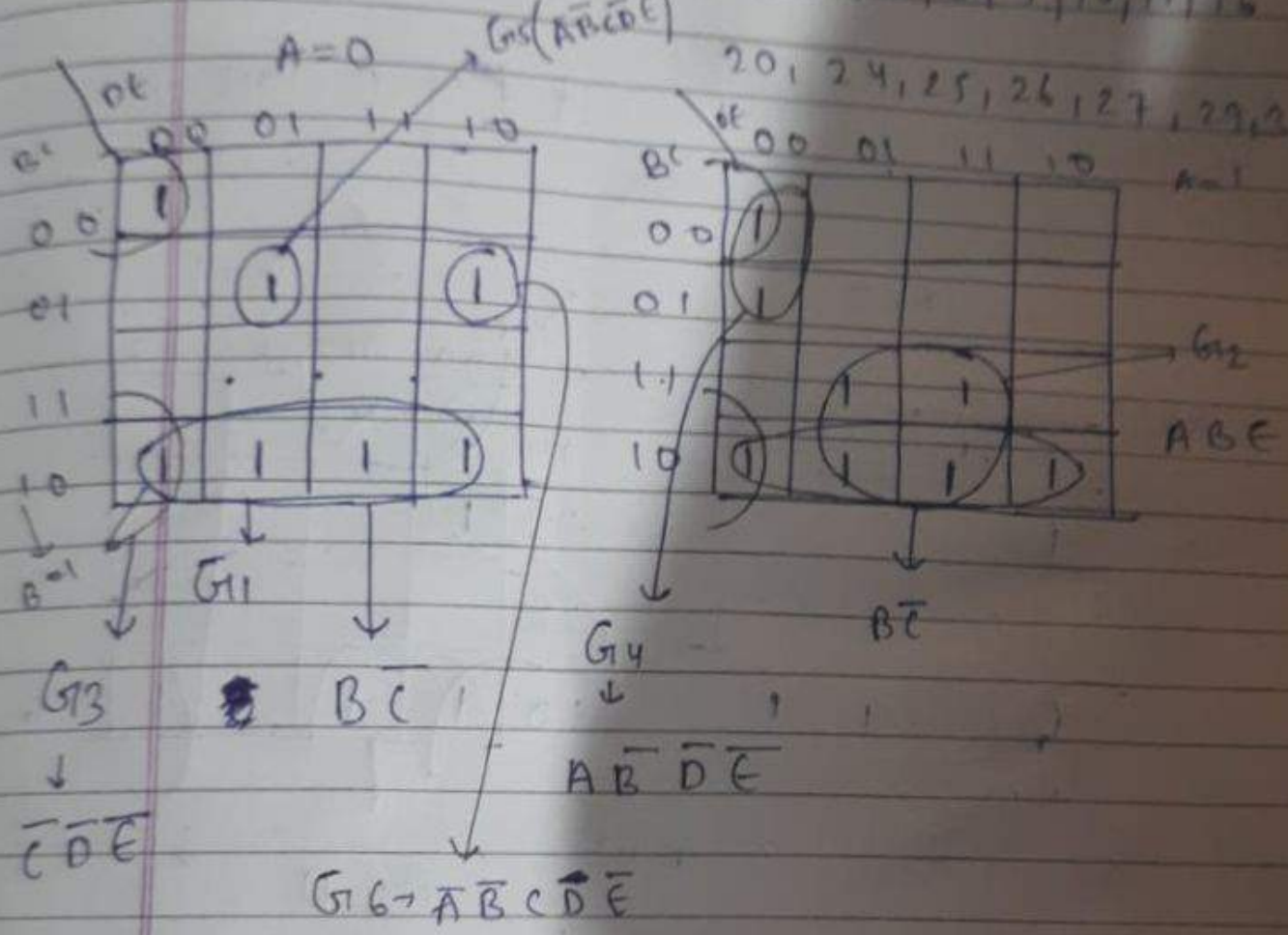


Q- $F(ABCDE) = \Sigma(0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 29, 31)$



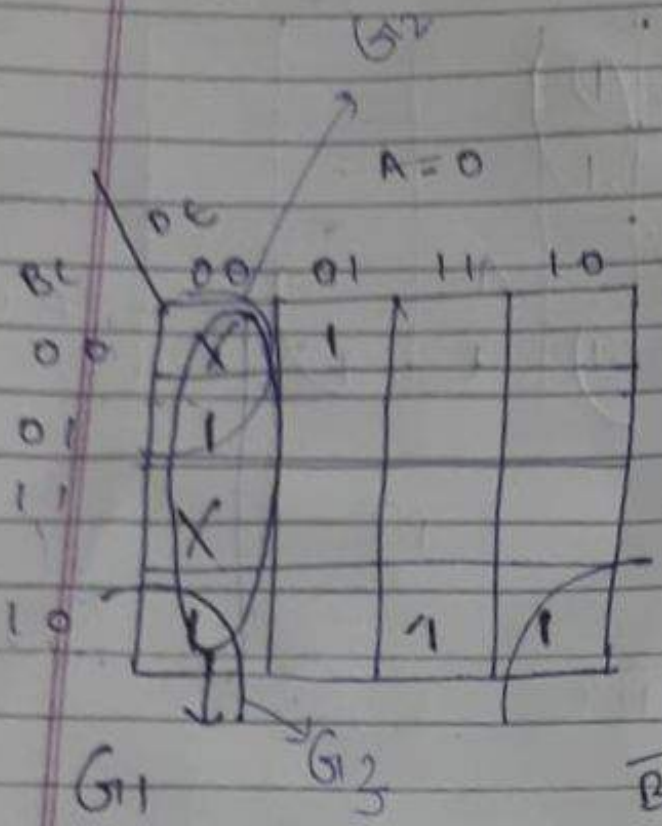
$= A\bar{D}E + \bar{A}\bar{B}\bar{E} + BE$

Q- $f(ABCDE) = \Sigma(0, 5, 6, 8, 9, 10, 11, 16, 20, 24, 25, 26, 27, 29, 31)$



→ $f = B\bar{C} + ABE + \bar{C}\bar{D}\bar{E} + A\bar{B}\bar{D}E + \bar{A}\bar{B}C\bar{D}E + \bar{A}\bar{B}CD\bar{E}$

Q- $F(ABCDE) = \Sigma(1,4,8,10,11,20,22,24,25,26) + d(0,12,16,17)$



$G_1 \rightarrow \overline{A}\,\overline{D}\,\overline{E}$

G_2: $\overline{A}\,\overline{B}\,\overline{E} +$

G_1: $\overline{B}\,\overline{C}\,\overline{D} +$

f_2: $B\overline{C}\,\overline{E} + \overline{A}B\overline{C}D + A\overline{B}\,\overline{C}\,\overline{E} + A\overline{C}\,\overline{D} +$

16 8 4 2 1
0 0 0 0
1 1 1 1

Page:
Date: / /

2^6

6 Variable K-Map :

→ $n = 6$

→ cells $= 2^6 = 64$ $(0 \rightarrow 63)$ counting

CD \ EF	$\bar{A}\bar{B}$ 00	01	10	11
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

CD \ EF	$\bar{A} \cdot B$ 00	01	10	11
	16	17	19	18
	20	21	23	22
	28	29	31	30
	24	25	27	26

CD \ EF	$A\bar{B}$
	32 33 35 34
	36 37 39 38
	44 45 47 46
	40 41 43 42

CD \ EF	$A \cdot B$
	48 49 51 50
	52 53 55 54
	60 61 63 62
	56 57 59 58

Imp K-MAP using don't care condition :-

Note : Don't care conditions are filled by X

Date / /
Page No.

Q Simplify the Given expression using K Map.

(a) SOP Form

$F(w,x,y,z) = \Sigma(1,3,7,11,15)$

$d(w,x,y,z) = \Sigma(0,2,5)$.

wx \ yz	00	01	11	10
00	X	1	1	X
01		X	1	
11			1	
10			1	

$f = yz + \bar{w}\bar{x}$

(b) POS form.

$F(w,x,y,z) = \pi(0,2,4,5,6,8,9,10,12,13,14)$

$d(wxyz) = \pi(0,2,5)$

wx \ yz	00	01	11	10
00	X			X
01	0	X		0
11	0	0		0
10	0	0		0

$f = (\bar{w}+y)\cdot(z)$.

Q Solve the function using K Map.

$F(ABCD) = \Sigma(0,6,8,13,14) + d(2,4,10)$

AB \ CD	00	01	11	10
00	1			X
01	X			1
11		1		1
10	1			X

$f = \bar{B}\bar{D} + \bar{C}\bar{D} + AB\bar{C}D$

5 Variable K-Map.

$n = 5$ (variables) $2^n = 2^5 = 32$ (No. of cells).

A = 0

BC \ DE	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

A = 1

BC \ DE	00	01	11	10
00	16	17	19	18
01	20	21	23	22
11	28	29	31	30
10	24	25	27	26

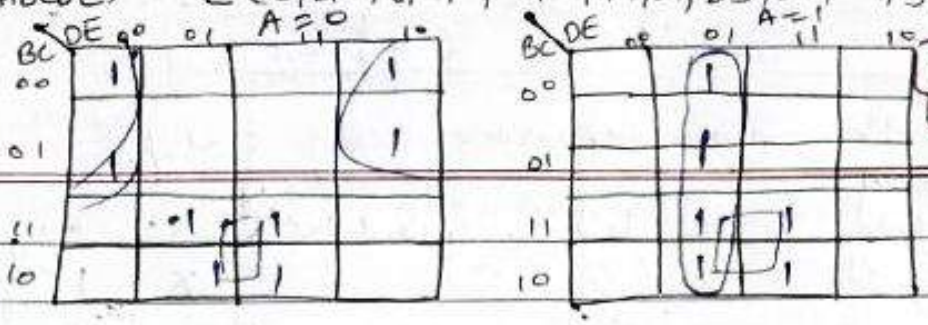
Adjacent column

Adjacent cell.

Adjacent group

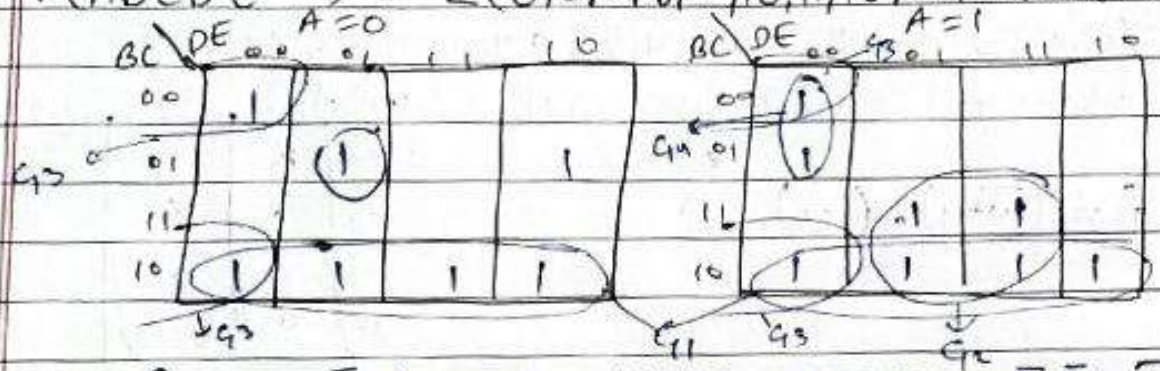
Adjacent Row

Q $F(ABCDE) = \Sigma(0,2,4,6,9,11,13,15,17,21,25,27,29,31)$



$$F = BE + A\bar{D}E + \bar{A}\bar{B}\bar{E}$$

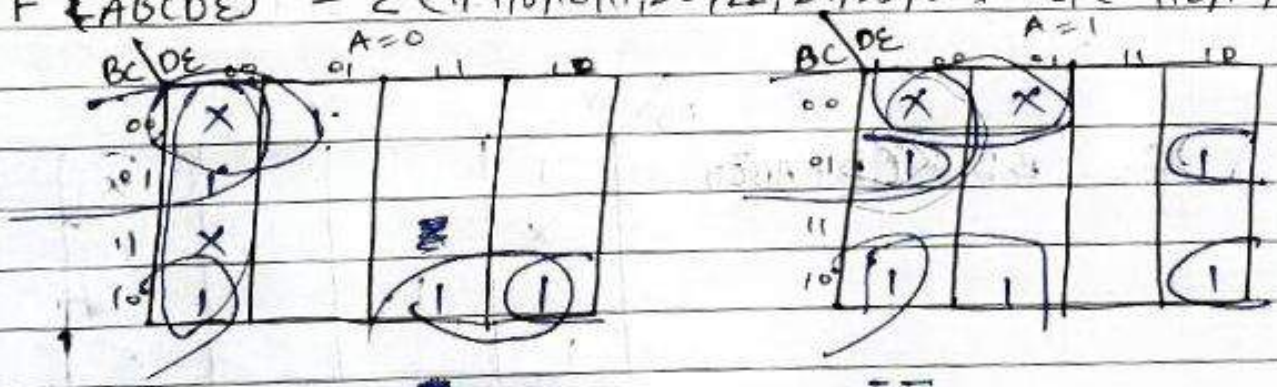
Q $F(ABCDE) = \Sigma(0,5,6,8,9,10,11,16,20,24,25,26,27,29,31)$



$$f = B\bar{C} + ABE + \bar{C}\bar{D}\bar{E} + A\bar{B}\bar{D}\bar{E} + \bar{A}\bar{B}C\bar{D}E + \bar{A}\bar{B}CD\bar{E}$$

~~fix variable~~

Q $F(ABCDE) = \Sigma(1,4,8,10,11,20,22,24,25,26) + d(0,12,16,17)$



$$\cancel{F = \bar{A}\bar{B}\bar{D}\bar{E} + \bar{B}\bar{C}\bar{E}} + A\bar{C}\bar{D}$$
$$\cancel{+ \bar{A}\bar{B}\bar{C}\bar{D}E + \bar{A}B\bar{C}D + A\bar{B}CD\bar{E}}$$

$$\boxed{F = \bar{B}\bar{C}\bar{D} + \bar{A}\bar{D}\bar{E} + B\bar{C}\bar{E} + \bar{A}B\bar{C}D + A\bar{C}\bar{D} + A\bar{B}C\bar{E}}$$

Date ___/___/___
Page No. _____

6 Variable K Map.

$n = 6$

$2^6 = 64$ cells $(0 \rightarrow 63)$.

$\bar{A}\bar{B}$

CD \ EF			
0	1	3	2
4	5	7	6
12	13	15	14
8	9	11	10

$\bar{A}B$

CD \ EF			
16	17	19	18
20	21	23	22
28	29	31	30
24	25	27	26

$A\bar{B}$

CD \ EF			
32	33	35	34
36	37	39	38
44	45	47	46
40	41	43	42

AB

CD \ EF			
48	49	51	50
52	53	55	54
60	61	63	62
56	57	59	58