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| **18EES101J-BASIC ELECTRICAL AND ELECTRONICS ENGINEERING (LAB)** |
| **RECORD**  **SEMESTER I**    **ACADEMIC YEAR: 2020-21**  **NAME : *Tambe Utkarsh Yashwant.***  **REG. NO. : *RA2011027010166***  C:\Users\System 1\Desktop\11.png  **DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING**  **FACULTY OF ENGINEERING & TECHNOLOGY**  **SRM INSTITUTE OF SCIENCE AND TECHNOLOGY**  (Formerly SRM University, Under section 3 of UGC Act, 1956)  **S.R.M. NAGAR, KATTANKULATHUR – 603 203**  **KANCHEEPURAM DISTRICT** |



**SRM Institute of Science and Technology**

(Deemed to be University)

**S.R.M. NAGAR, KATTANKULATHUR -603 203**

**KANCHEEPURAM DISTRICT**

**BONAFIDE CERTIFICATE**

**Register No : *RA2011027010166***

Certified to be the bonafide record of work done by *Tambe Utkarsh Yashwant* of *Computer Science & Engineering department*, B.Techdegree course in the Practical of 18EES101J Basic Electrical and Electronics Engineering in **SRM IST, Kattankulathur** during the academic year 2018-2019. **Lab in-charge**

**Date: Year Co-ordinator**

Submitted for end semester examination held in\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Lab, SRMIST**,** Kattankulathur**.**

**Date: Examiner-1 Examiner-2**

**LIST OF EXPERIMENTS**

1. Verification of Kirchhoff’s laws

2. Verification of All Theorems (Thevenin’s theorem, Norton’s theorem, Maximum power transfer theorem)

3. Transient analysis of RL an RC series circuits

4. Load test on single phase transformer

5. Demo of DC/AC machines & Parts

6. Types of wiring (fluorescent lamp wiring, staircase wiring)

7. Characteristics of semiconductor devices (PN junction, Zener diode, BJT)

8. Wave shaping circuits (Half and full wave rectifier, clipper)

9. Displacement measurement using LVDT and pressure measurement using Strain gauge

10. Verification and interpretation of Logic Gates.

11. Reduction of Boolean expression using K-map

12. Study of modulation and demodulation techniques.

**INDEX**

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| --- | --- | --- | --- |
| **Sl. No.** | **Name of the Experiment** | **Marks (50)** | **Signature**  **of the Staff** |
| 1 | Verification of Kirchhoff’s laws |  |  |
| 2 | Verification of All Theorems  (Thevenin’s theorem, Norton’s theorem, Maximum power transfer theorem) |  |  |
| 3 | Transient analysis of RL an RC series circuits |  |  |
| 4 | Load test on single phase transformer |  |  |
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DEPT. OF ELECTRICAL & ELECTRONICS ENGINEERING

SRM INSTITUTE OF SCIENCE AND TECHNOLOGY, Kattankulathur – 603 203

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| --- |
| Title of Experiment : **7. Characteristics of semiconductor devices**  **(a) PN junction diode, (b) Zener diode, (c)BJT** |
| Name of the candidate : *Tambe Utkarsh Yashwant*.  Register Number : *RA2011027010166*  Date of Experiment : *22nd October, 2020* |

|  |  |  |  |
| --- | --- | --- | --- |
| Sl.  No. | Marks Split up | Maximum marks  (50) | Marks obtained |
| 1 | Pre-Lab questions | 5 |  |
| 2 | Preparation of observation | 15 |  |
| 3 | Execution of experiment | 15 |  |
| 4 | Calculation / Evaluation of Result | 10 |  |
| 5 | Post-Lab questions | 5 |  |
| **Total** | | **50** |  |

**Staff Signature**

**PRE-LAB QUESTIONS**

**1. What are intrinsic and extrinsic semiconductors?**

**Ans :** *The pure form of the semiconductor is known as the intrinsic semiconductor and the semiconductor in which intentionally impurities is added for making it conductive is known as the extrinsic semiconductor. The conductivity of the intrinsic semiconductor becomes zero at room temperature while the extrinsic semiconductor is very less conductive at room temperature.*

**2. Give examples for Trivalent and Pentavalent impurity.**

**Ans : i. *Pentavalent* -** *Antimony, Arsenic & Phosphorus.*

**ii. *Trivalent* -** *Boron, Aluminium & Gallium.*

**3. What is the need for Zener diode?**

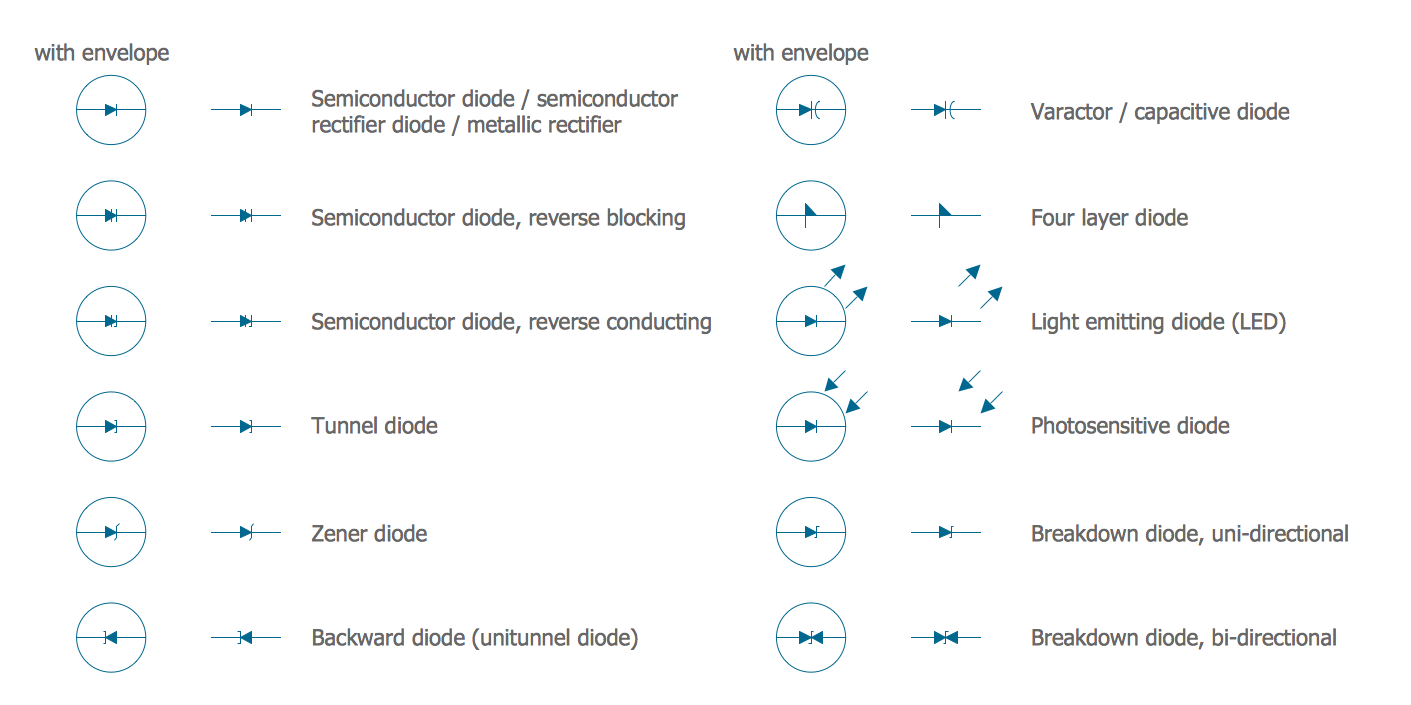
**Ans : *Zener diodes*** *are used for voltage regulation, as reference elements, surge suppressors, and in switching applications and clipper circuits. Voltage regulator. The load voltage equals breakdown voltage VZ of the diode.*

**4. What is voltage regulation and mention its significance?**

**Ans :** *Voltage regulation is the measure of how well a power transformer can maintain constant secondary voltage given a constant primary voltage and wide variance in load current. The lower the percentage (closer to zero), the more stable the secondary voltage and the better the regulation it will provide.*

**5. Give the different types of semiconductor devices with symbols.**

**Ans :**



|  |  |
| --- | --- |
| **Experiment No. 7 a)**  **Date :** *22/10/2020* | **CHARACTERISTICS OF PN JUNCTION DIODE** |

**Aim:**

To study the characteristics of PN Junction diode under forward and reverse bias conditions.

**Apparatus Required: Components Required:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Sr. No.** | **Name** | **Range** | **Qty** |  | **Sr. No.** | **Name** | **Range** | **Qty** |
| 1 | R.P.S. | (0-30) V | 1 | 1 | Diode | IN4001 | 1 |
| 2 | Ammeter | (0–30) mA | 1 | 2 | Resistor | 1kΩ | 1 |
| (0-500) µA | 1 | 3 | Bread Board | - | 1 |
| 3 | Voltmeter | (0-1) V | 1 | 4 | connecting Wires | - | Req |
| (0-10) V | 1 |

**Theory:**

A PN junction diode is a two terminal semiconducting device. It conducts only in one direction (only on forward biasing).

**Forward Bias**

On forward biasing, initially no current flows due to barrier potential. As the applied potential exceeds the barrier potential the charge carriers gain sufficient energy to cross the potential barrier and hence enter the other region. The holes, which are majority carriers in the P-region, become minority carriers on entering the N-regions, and electrons which are the majority carriers in the N-region, become minority carriers on entering the P-region. This injection of minority carriers results in the current flow, opposite to the direction of electron movement.

**Reverse Bias**

On reverse biasing, the majority charge carriers are attracted towards the terminals due to the applied potential resulting in the widening of the depletion region. Since the charge carriers are pushed towards the terminals no current flows in the device due to majority charge carriers. There will be some current in the device due to the thermally generated minority carriers. The generation of such carriers is independent of the applied potential and hence the current is constant for all increasing reverse potential. This current is referred to as Reverse Saturation Current (IO) and it increases with temperature. When the applied reverse voltage is increased beyond the certain limit, it results in breakdown. During breakdown, the diode current increases tremendously.

**Procedure:**

**Forward Bias**

1. Connect the circuit as per the diagram.
2. Vary the applied voltage V in steps of 0.1V.
3. Note down the corresponding Ammeter readings I.
4. Plot a graph between V & I

**Observations:**

1. Find the d.c (static) resistance = V/I.
2. Find the a.c (dynamic) resistance r = δV / δI (**r = ΔV/ΔI) = **.
3. Find the forward voltage drop [Hint: it is equal to 0.7 for Si and 0.3 for Ge]

**Reverse Bias**

1. Connect the circuit as per the diagram.
2. Vary the applied voltage V in steps of 1.0V.
3. Note down the corresponding Ammeter readings I.
4. Plot a graph between V & I
5. Find the dynamic resistance **r = δV / δI.**

**Formula for Reverse Saturation Current (IO):**

**Io = ∂I/[exp(∂V/ηVT)]-1**

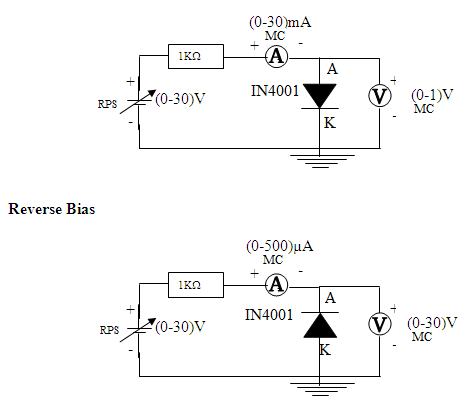
Where VT  is the voltage equivalent of Temperature = kT/q

‘k’ is Boltzmann’s constant, ‘q’ is the charge of the electron and ‘T’ is the temperature in degrees Kelvin.

η =1 for Silicon and 2 for Germanium

**Circuit Diagram:**

Forward Bias

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**Specification for 1N4001: Silicon Diode**

Peak Inverse Voltage: 50V

Idc = 1A.

Maximum forward voltage drop at 1 Amp is 1.1 volts

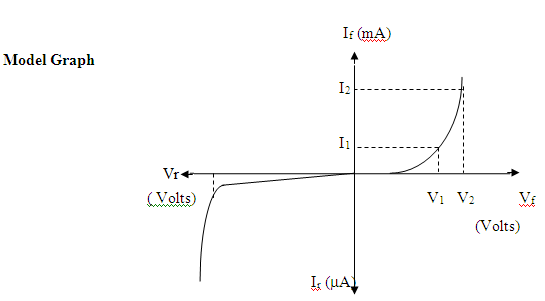
Maximum reverse current at 50 volts is 5μA

|  |  |  |
| --- | --- | --- |
| **Sr. No.** | **Voltage**  **(In Volts)** | **Current**  **(In mA)** |
| *1.* | *0.6096* | *0.39* |
| *2.* | *0.6408* | *1.36* |
| *3.* | *0.6545* | *2.35* |
| *4.* | *0.6698* | *4.33* |
| *5.* | *0.6793* | *6.32* |
| *6.* | *0.6889* | *9.31* |
| *7.* | *0.6959* | *12.3* |
| *8.* | *0.7029* | *16.3* |
| *9.* | *0.7084* | *20.29* |
| *10.* | *0.7139* | *25.29* |

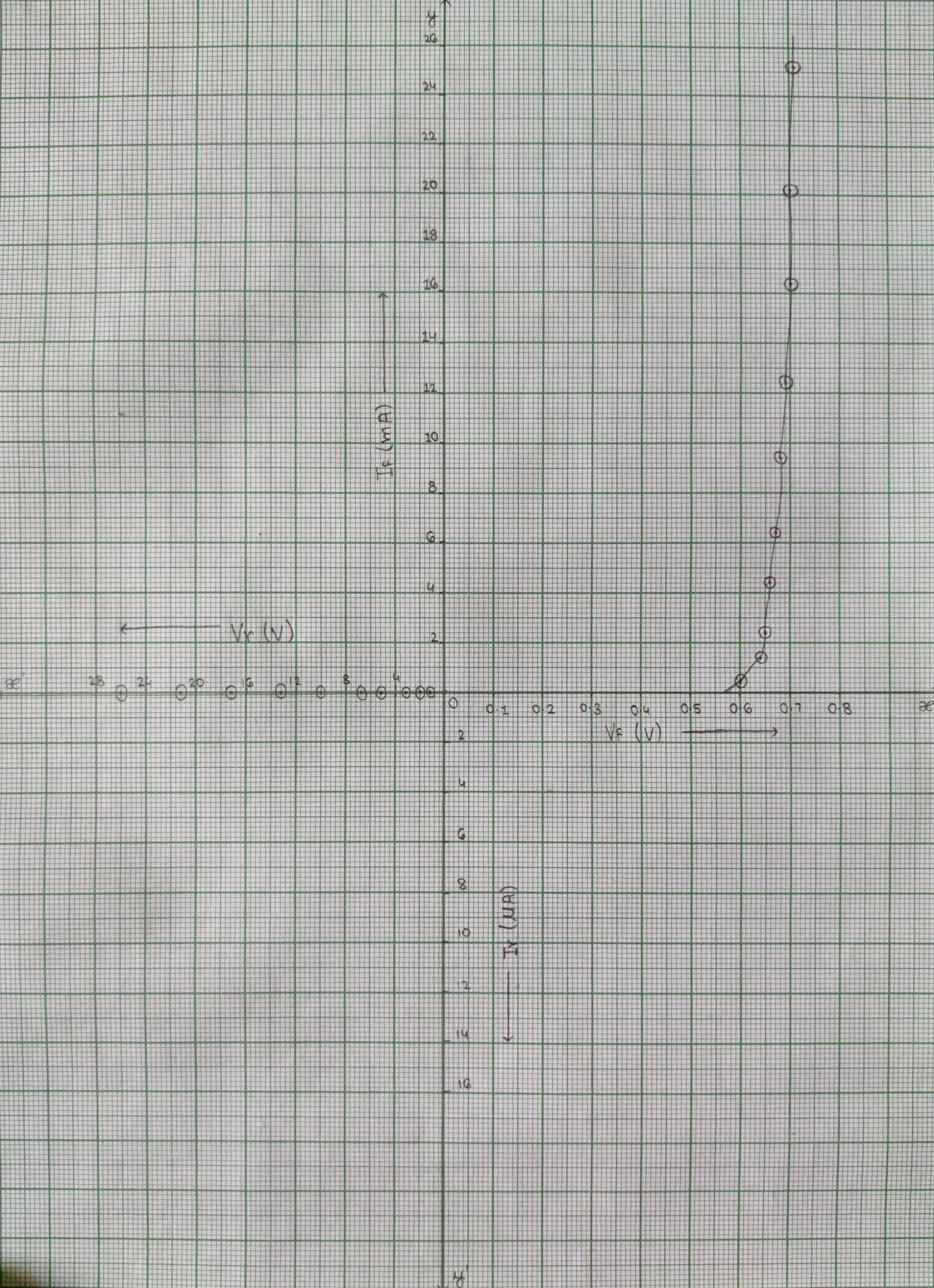
**Tabular Column:**

**Forward Bias Reverse Bias**

|  |  |  |
| --- | --- | --- |
| **Sr. No.** | **Voltage**  **(In Volts)** | **Current**  **(In μA)** |
| *1.* | *1* | *0* |
| *2.* | *2* | *0* |
| *3.* | *3* | *0* |
| *4.* | *5* | *0* |
| *5.* | *7* | *0* |
| *6.* | *10* | *0* |
| *7.* | *13* | *0* |
| *8.* | *17* | *0* |
| *9.* | *21* | *0* |
| *10.* | *26* | *0* |

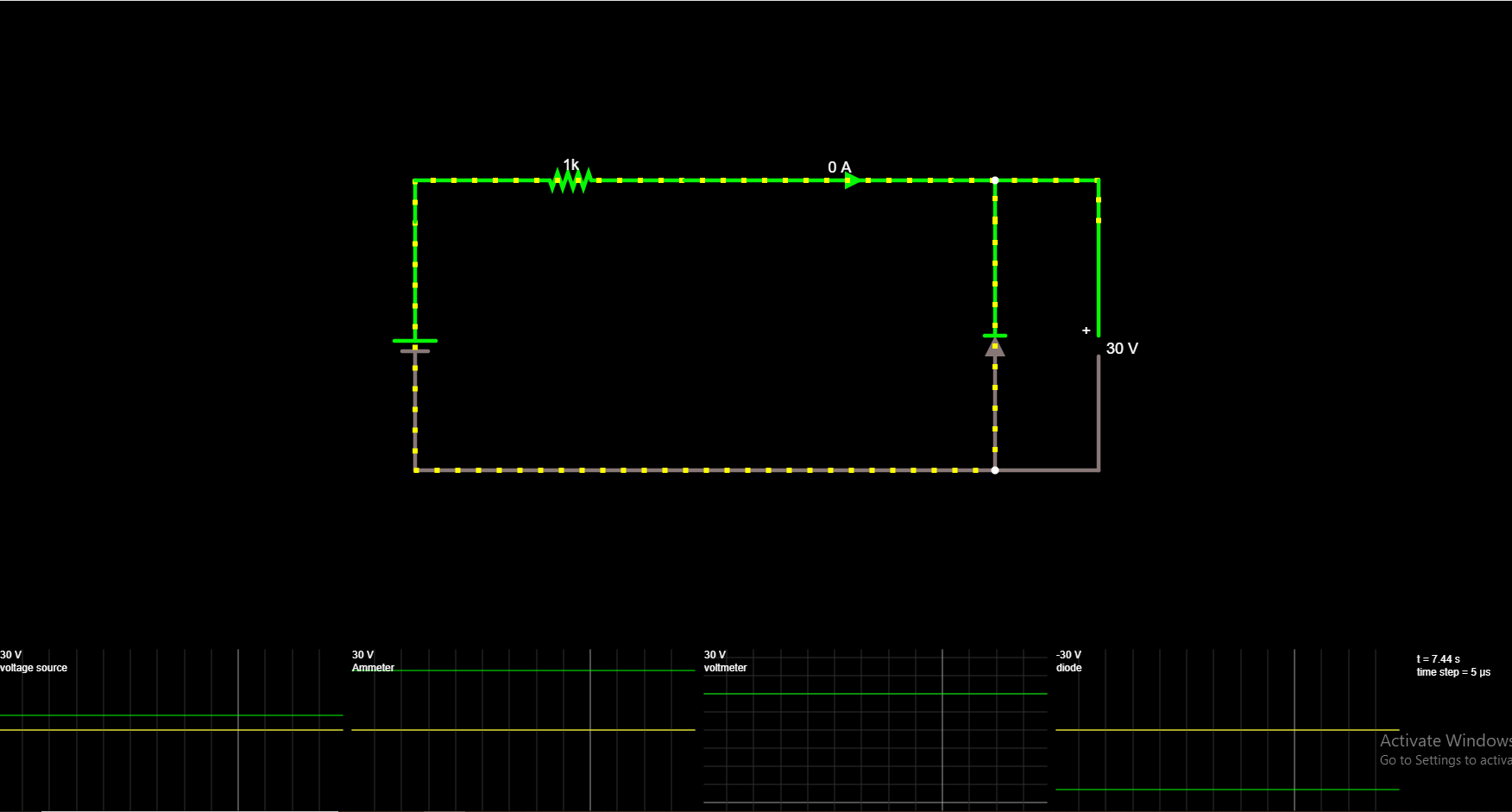


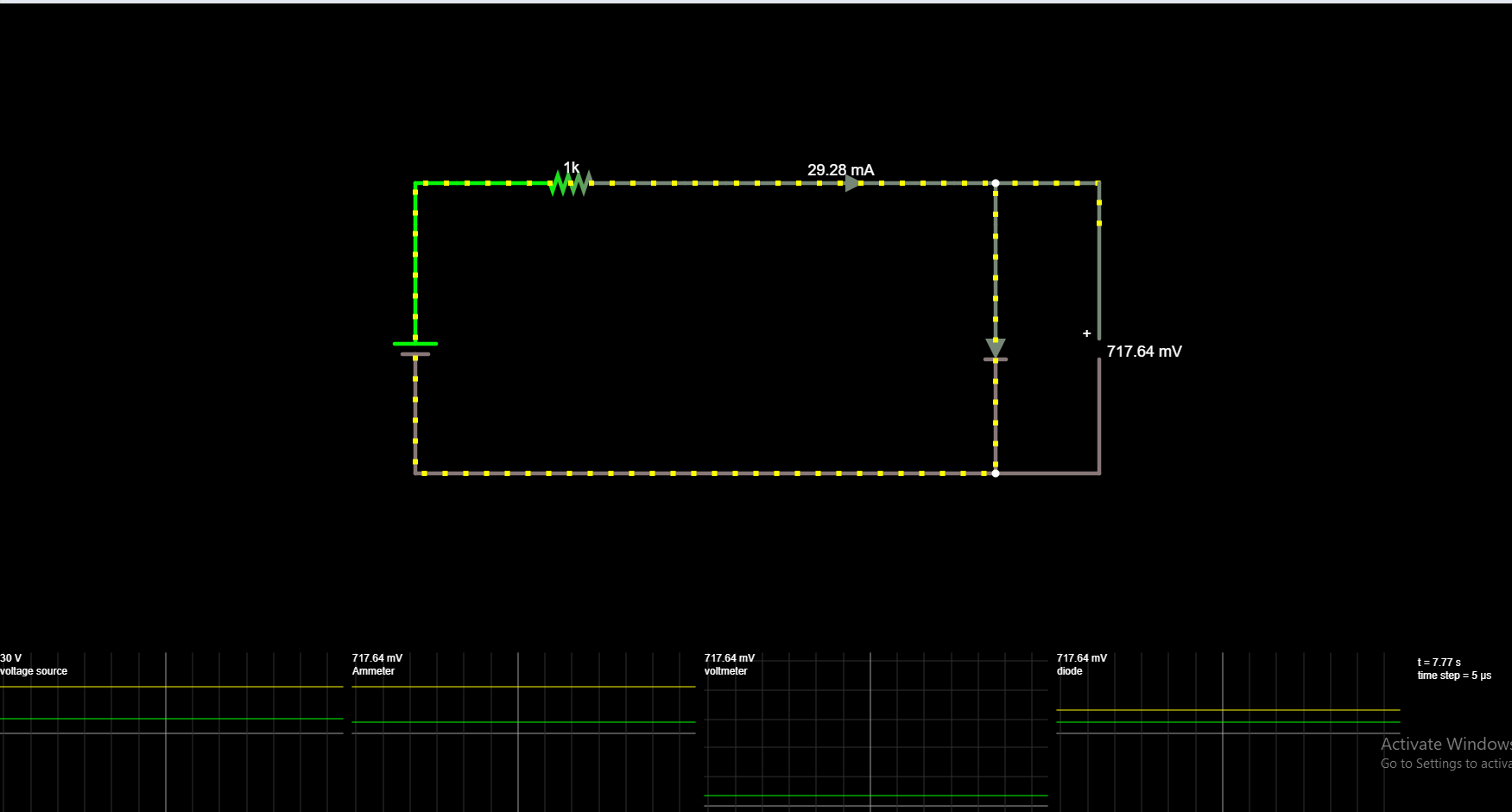
**Graph:**



**Result:** *Thus, the characteristics of P-N Junction diode under forward and reverse bias conditions are studied.*

***Screenshots of E-Circuits with Forward & Reverse biased P-N Junction Diode.***





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| **Experiment No. 7 b)**  **Date :** *22/10/2020* | **CHARACTERISTICS OF ZENER DIODE** |

**Aim:**

To find the forward and reverse bias characteristics of a given Zener diode.

**Apparatus Required: Components Required:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Sr. No.** | **Name** | **Range** | **Qty** |  | **Sr. No.** | **Name** | **Range** | **Qty** |
| 1 | R.P.S | (0-30)V | 1s | 1 | Zener diode | FZ5.1 | 1 |
| 2 | Ammeter | (0–30)mA | 2 | 2 | Resistor | 1KΩ | 1 |
| 3 | Bread Board | - | 1 |
| 3 | Voltmeter | (0–10)V | 1 | 4 | Wires | - | Req |
| (0–1)V | 1 |

**Theory:**

A properly doped crystal diode, which has a sharp breakdown voltage, is known as Zener diode.

**Forward Bias**

On forward biasing, initially no current flows due to barrier potential. As the applied potential increases, it exceeds the barrier potential at one value and the charge carriers gain sufficient energy to cross the potential barrier and enter the other region. the holes ,which are majority carriers in p-region, become minority carriers on entering the N-regions and electrons, which are the majority carriers in the N-regions become minority carriers on entering the P-region. This injection of minority carriers results current, opposite to the direction of electron movement.

**Reverse Bias**

When the reverse bias is applied, due to majority carriers small amount of current (ie) reverse saturation current flows across the junction. As the reverse bias is increased to breakdown voltage, sudden rise in current takes place due to Zener effect.

**Zener Effect**

Normally, PN junction of Zener Diode is heavily doped. Due to heavy doping the depletion layer will be narrow. When the reverse bias is increased the potential across the depletion layer is more. This exerts a force on the electrons in the outermost shell. Because of this force the electrons are pulled away from the parent nuclei and become free electrons. This ionization, which occurs due to electrostatic force of attraction, is known as Zener effect. It results in large number of free carriers, which in turn increases the reverse saturation current

**Procedure:**

**Forward Bias**

1. Connect the circuit as per the circuit diagram.

2. Vary the power supply in such a way that the readings are taken in steps of 0.1V in the voltmeter till the needle of power supply shows 30V.

3. Note down the corresponding ammeter readings.

4. Plot the graph : V (vs) I.

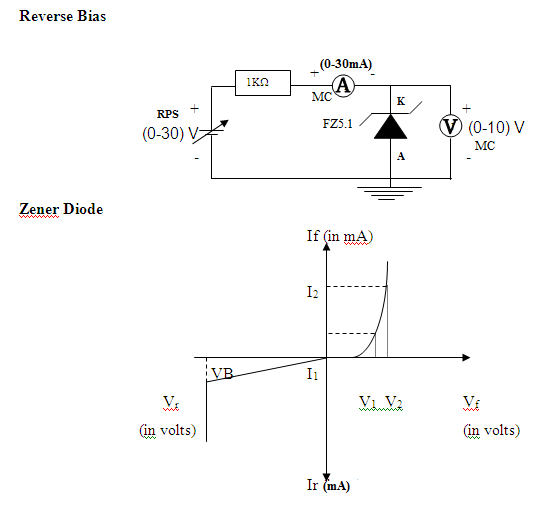
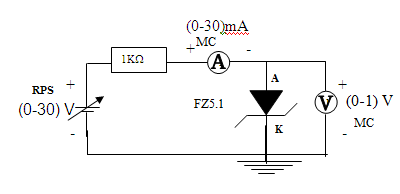
5. Find the dynamic resistance **r = δV / δI.**

**Reverse Bias**

1. Connect the circuit as per the diagram.
2. Vary the power supply in such a way that the readings are taken in steps of 0.1V in the voltmeter till the needle of power supply shows 30V.
3. Note down the corresponding Ammeter readings I.
4. Plot a graph between V & I
5. Find the dynamic resistance **r = δV / δI.**
6. Find the reverse voltage Vr at Iz=20

**Circuit Diagram:**

Forward Bias

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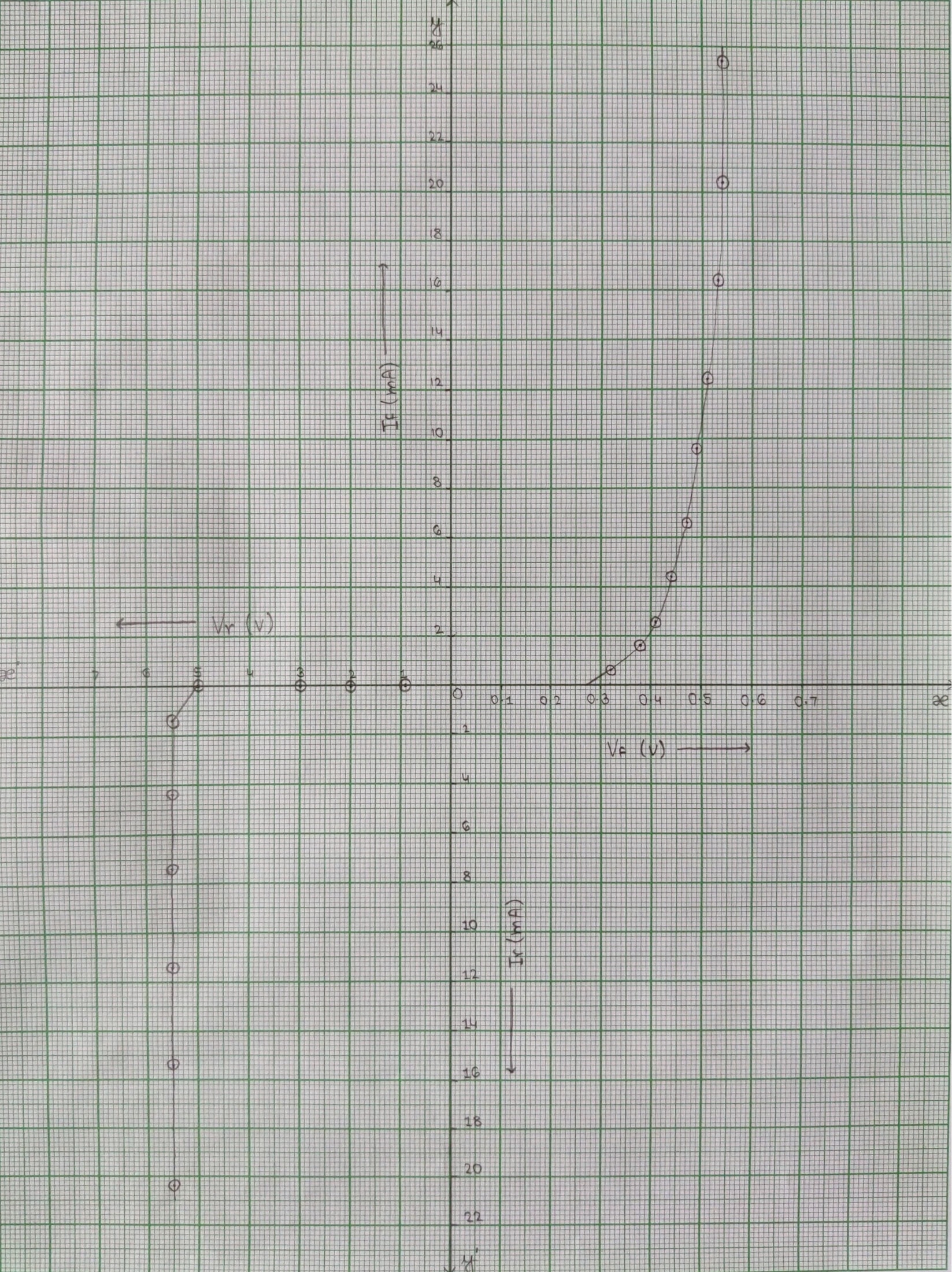
**Tabular Column:**

**Forward Bias Reverse Bias**

|  |  |  |
| --- | --- | --- |
| **Sr. No.** | **Voltage**  **(In Volts)** | **Current**  **(In mA)** |
| *1.* | *0.3244* | *0.67* |
| *2.* | *0.3818* | *1.62* |
| *3.* | *0.4127* | *2.59* |
| *4.* | *0.4499* | *4.55* |
| *5.* | *0.4737* | *6.53* |
| *6.* | *0.4985* | *9.50* |
| *7.* | *0.5165* | *12.48* |
| *8.* | *0.5347* | *16.47* |
| *9.* | *0.5491* | *20.45* |
| *10.* | *0.5465* | *25.44* |

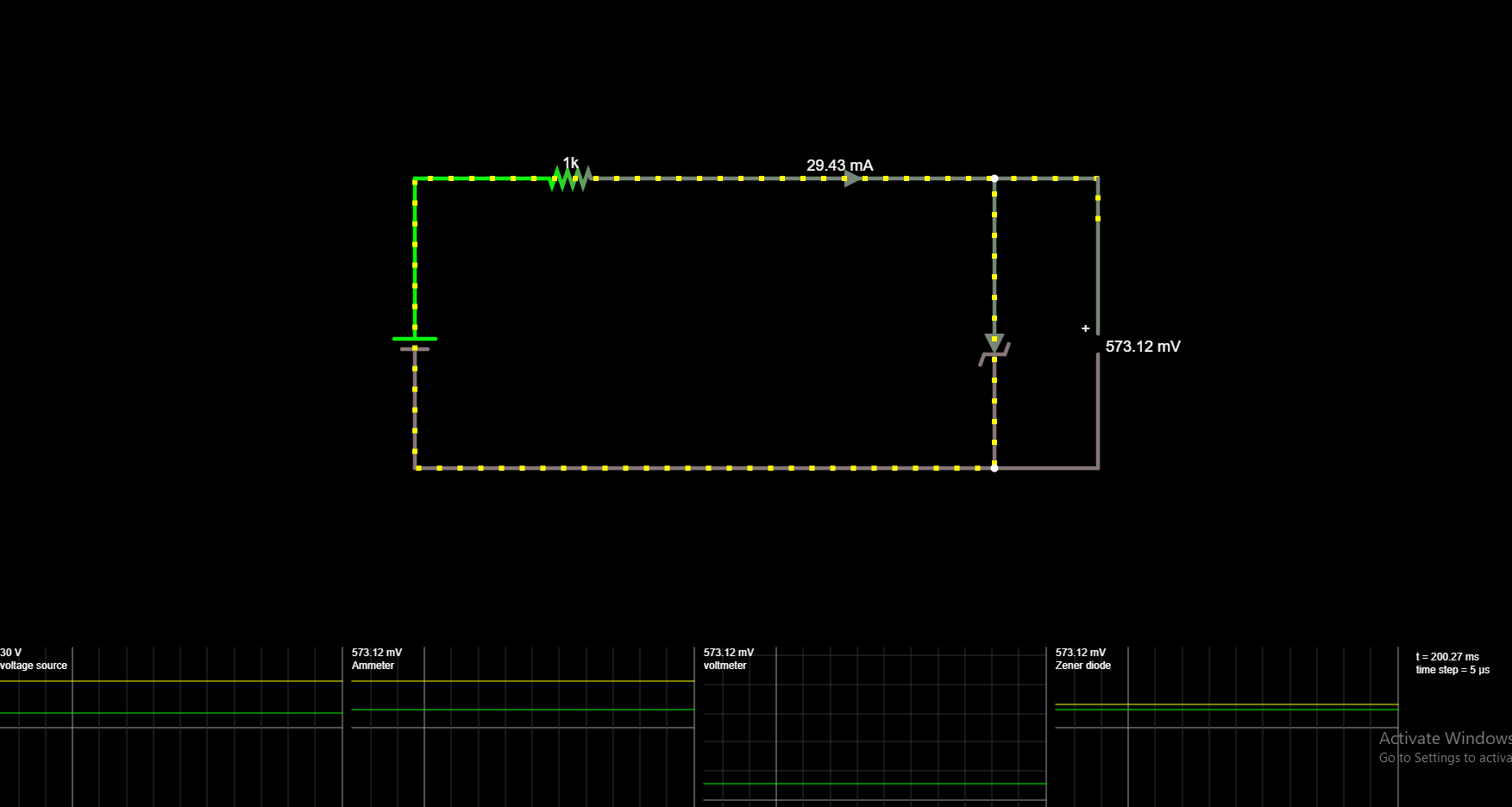
|  |  |  |
| --- | --- | --- |
| **Sr. No.** | **Voltage**  **(In Volts)** | **Current**  **(In mA)** |
| *1.* | *0.99* | *0.0050* |
| *2.* | *2.00* | *0.0050* |
| *3.* | *3.00* | *0.0050* |
| *4.* | *4.99* | *0.0055* |
| *5.* | *5.52* | *1.48* |
| *6.* | *5.59* | *4.41* |
| *7.* | *5.63* | *7.37* |
| *8.* | *5.65* | *11.35* |
| *9.* | *5.67* | *15.33* |
| *10.* | *5.69* | *20.31* |

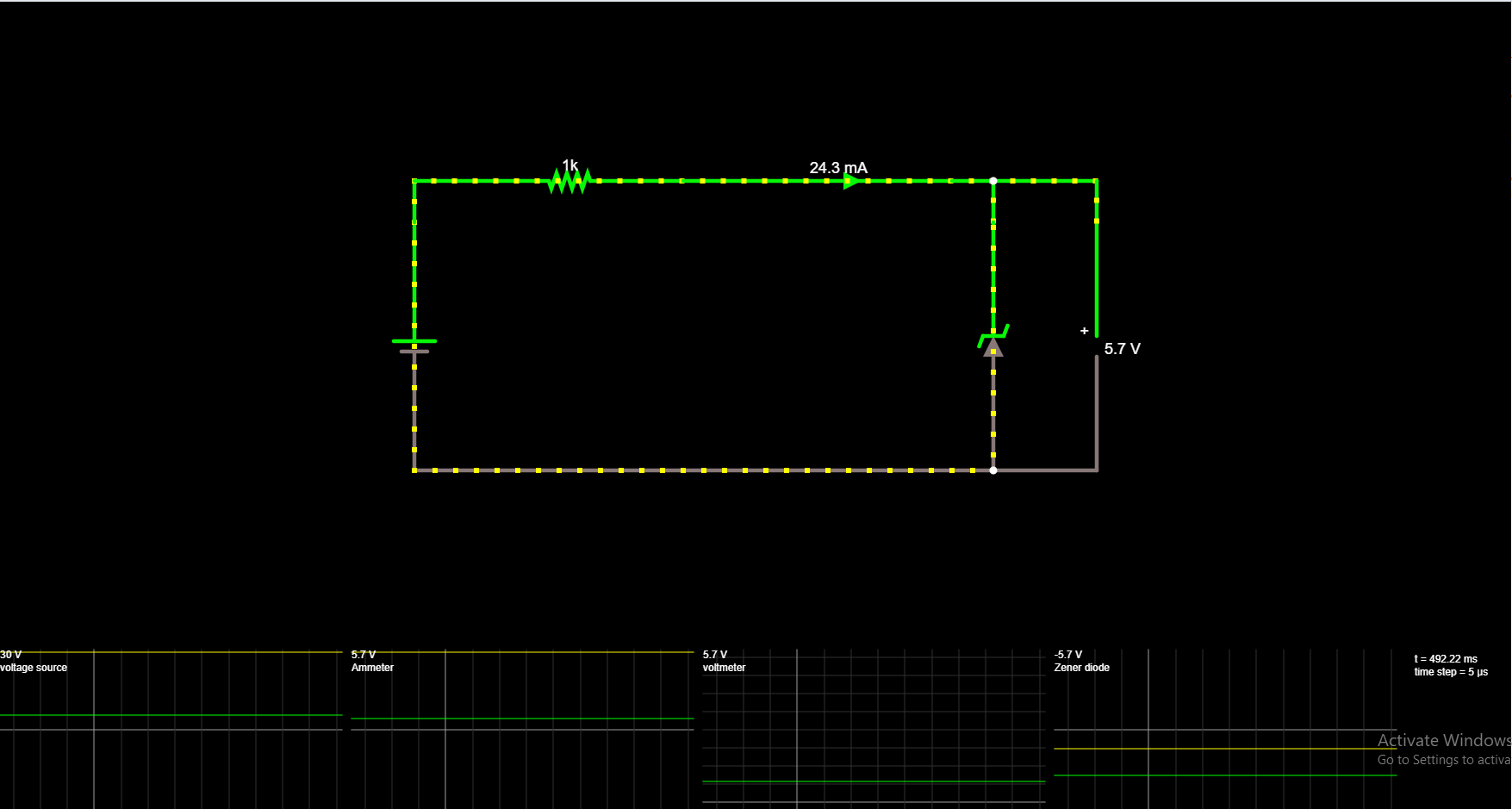
**Graph:**



**Result:** *Thus, the characteristics of Zener diode under forward and reverse bias conditions are studied.*

***Screenshots of E-Circuits with Forward & Reverse biased Zener Diode.***





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| **Experiment No. 7 c)**  **Date :** *22/10/2020* | **CHARACTERISTICS OF BJT (CE CONFIGURATION)** |

**Aim:**

To plot the transistor (BJT) characteristics of CE configuration.

**Apparatus Required: Components Required:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Sr. No.** | **Name** | **Range** | **Qty** |  | **Sr. No.** | **Name** | **Range** | **Qty** |
| 1 | R.P.S | (0-30)V | 2 | 1 | Transistor | BC 107 | 1 |
| 2 | Ammeter | (0–30) mA  MC | 1 | 2 | Resistor | 10 KΩ | 1 |
| (0–250) µA  MC | 1 | Resistor | 1 KΩ | 1 |
| 3 | Voltmeter | (0–30)V  MC | 1 | 3 | Bread Board |  | 1 |
| (0–1)V  MC | 1 | 4 | Wires |  |  |

**Theory:**

A BJT is a three terminal two – junction semiconductor device in which the conduction is due to both the charge carrier. Hence it is a bipolar device. BJT is classified into two types – NPN & PNP. A NPN transistor consists of two N types in between which a layer of P is sandwiched. The transistor consists of three terminal emitter, collector and base. The emitter layer is the source of the charge carriers and it is heavily doped with a moderate cross sectional area. The collector collects the charge carries and hence moderate doping and large cross sectional area. The base region acts a path for the movement of the charge carriers. In order to reduce the recombination of holes and electrons the base region is lightly doped and is of hollow cross sectional area. Normally the transistor operates with the EB junction forward biased.

**Procedure:**

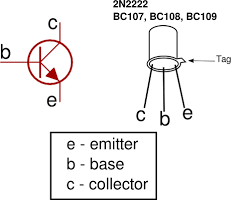
**Input Characteristics**

1. Connect the circuit as per the circuit diagram.
2. Set VCE, vary VBE in regular interval of steps and note down the corresponding IB reading. Repeat the above procedure for different values of VCE.
3. Plot the graph: VBE vs IB for a constant VCE.

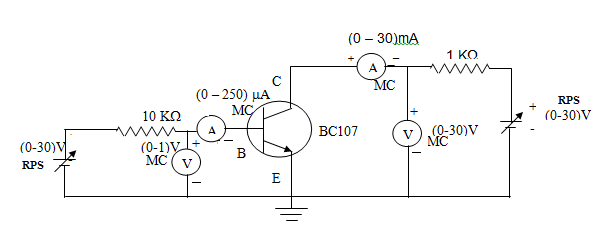
**Output Characteristics**

1. Connect the circuit as per the circuit diagram.
2. Set IB, Vary VCE in regular interval of steps and note down the corresponding IC reading. Repeat the above procedure for different values of IB.
3. Plot the graph: VCE vs IC for a constant IB.

**Pin Diagram:**

****

**Circuit Diagram:**

** Model Graph:**

**Input Characteristics Output Characteristics**

VCE = 0V

VCE = 5V

IB

µA

mA

VBE(V)

VCE(V)

0

0

IB=60μA

IB=40μA

IB=20μA

IC

**Tabular Column:**

**Input Characteristics**

|  |  |  |  |
| --- | --- | --- | --- |
| **VCE = 0 V** | | **VCE = 5V** | |
| **VBE (V)** | **IB (μA)** | **VBE (V)** | **IB (μA)** |
| *1* | *48.31* | *1* | *39.01* |
| *2* | *145.55* | *2* | *138.34* |
| *3* | *244.25* | *3* | *238.24* |
| *5* | *442.76* | *5* | *438.05* |
| *7* | *641.84* | *7* | *637.89* |
| *10* | *940.88* | *10* | *937.65* |
| *13* | *1240* | *13* | *1240* |
| *17* | *1640* | *17* | *1640* |
| *21* | *2040* | *21* | *2040* |
| *26* | *2540* | *26* | *2540* |

**Output Characteristics**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **IB=20μA** | | **IB=40μA** | | **IB=60μA** | |
| **VCE (V)** | **IC (mA)** | **VCE (V)** | **IC (mA)** | **VCE (V)** | **IC (mA)** |
| *1* | *0.877* | *1* | *0.924* | *1* | *0.938* |
| *2* | *1.16* | *2* | *1.89* | *2* | *1.91* |
| *3* | *1.16* | *3* | *2.84* | *3* | *2.90* |
| *5* | *1.16* | *5* | *3.09* | *5* | *4.83* |
| *7* | *1.16* | *7* | *3.09* | *7* | *5.07* |
| *10* | *1.16* | *10* | *3.09* | *10* | *5.07* |
| *13* | *1.16* | *13* | *3.09* | *13* | *5.07* |
| *17* | *1.16* | *17* | *3.09* | *17* | *5.07* |
| *21* | *1.16* | *21* | *3.09* | *21* | *5.07* |
| *26* | *1.16* | *26* | *3.09* | *26* | *5.07* |

**Graph:**

**1. Input Characteristics**

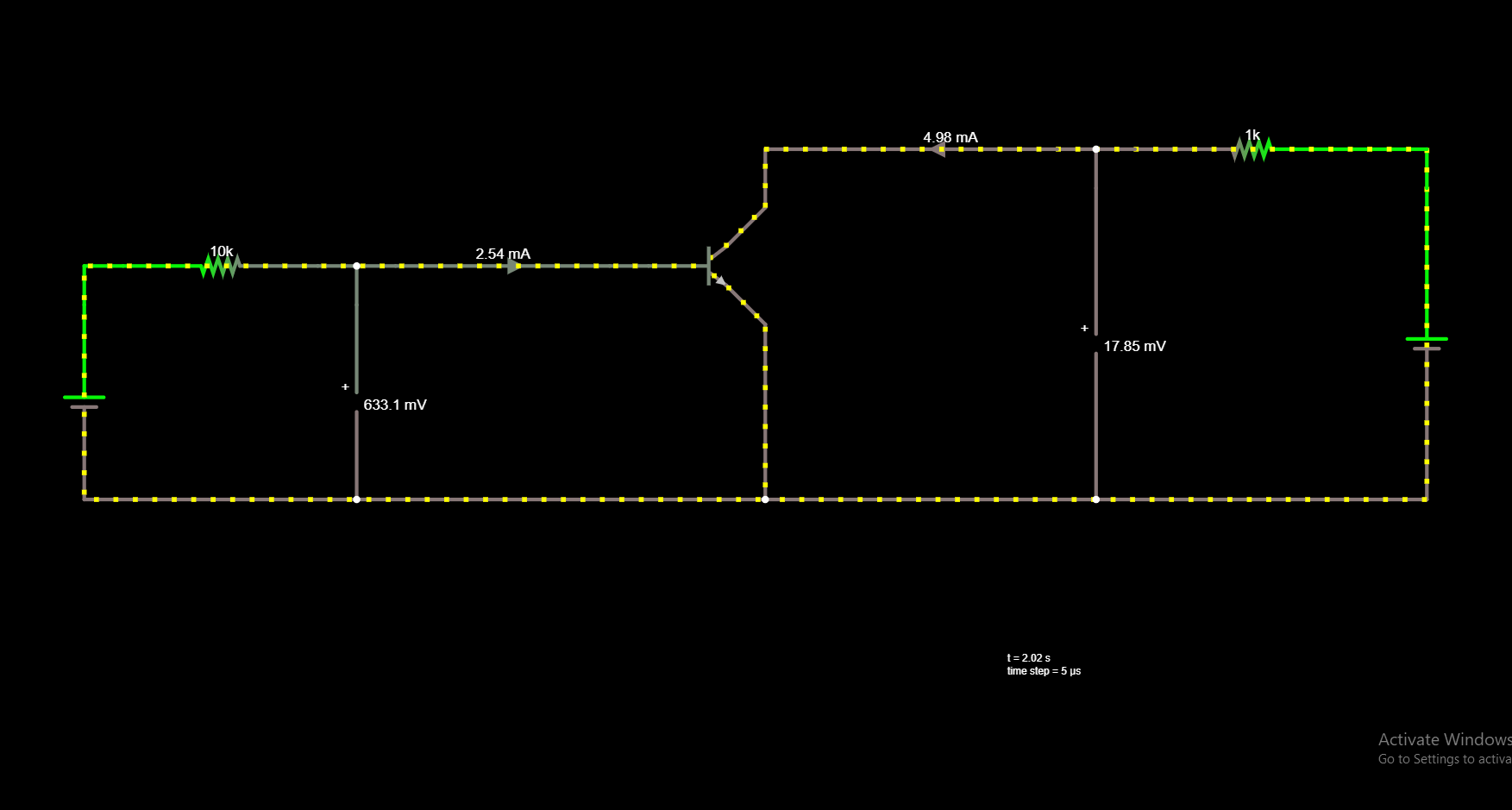
**2. Output Characteristics**





**Result:** *Thus, the input & output characteristics of BJT with CE configuration are studied.*

***Screenshots of E-Circuits with BJT with CE Configuration.***



**POST-LAB QUESTIONS**

**1. What is Punch through voltage?**

**Ans :** *The reverse-bias voltage applied to the drain terminal that results in significant drain-to-source current even though the transistor is biased in its off state.*

***NOTE :-*** *Punch-through is differentiated from junction breakdown in that the current path is from drain to source instead of from drain to substrate, as is the case for junction breakdown.*

**2. What is early effect?**

**Ans :** *The* ***Early effect****, named after its discoverer* ***James M. Early****, is the variation in the effective width of the base in a* ***bipolar junction transistor (BJT)*** *due to a variation in the applied base-to-collector voltage. A greater reverse bias across the collector–base junction, for example, increases the collector–base depletion width, thereby decreasing the width of the charge carrier portion of the base.*

**3. State maximum rating of transistor.**

**Ans :** *The rating for maximum collector-emitter voltage VCE can be thought of as the maximum voltage it can withstand while in cutoff mode (no base current). This rating is of particular importance when using a bipolar transistor as a switch. A typical value for a small signal transistor is* ***60 to 80 V****. In power transistors, this could range to* ***1000 V****.*

**4. What is leakage current and mention its range?**

**Ans : *A leakage current*** *is an electric current in an unwanted conductive path under normal operating conditions. If the conductors are separated by a material with a small conductivity rather than a perfect dielectric, then a small leakage current flows directly between them. A leakage current is an electric current in an unwanted conductive path under normal operating conditions.*

*Its range is :- Usually, the level of this leakage current is from about* ***10mA to some 100mA****, depending on the size of electrical system.*

**5. What is base – width modulation?**

**Ans : *Early effect*** *or* ***base width modulation*** *:- The early effect is the variation in the width of the base in a bipolar transistor due to a variation in the applied base-to-collector voltage. For example, a greater reverse bias across the collector- base junction increases the collector-base depletion width.*