

EE414 Introduction to Analog Integrated Circuits

Term Project Final Report

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Abstract

This document is the final report of the term project of the *Introduction to Analog Integrated Circuits* (EE 414). In this project, a low dropout voltage regulator is designed according to the requirements given. As band-gap voltage reference circuitry, a PTAT (*Proportional-to-Absolute Temperature*) generator with a temperature compensation stage at the end is adopted. As error amplifier, a telescopic amplifier topology is adopted. Whole design is simulated via *Cadence*.

Keywords – PTAT, Temperature Coefficient, PSRR, Line Regulation, MOS, Reference

1 Introduction

Low Dropout (LDO) Voltage Regulators are linear DC regulators that maintains regulation when there is a small fraction between the output voltage and the supply voltage (1). Some advantages of the LDO regulators can be summarized as the absence of switching noise, smaller device size and design simplicity. The main disadvantage of the LDO regulators is the power dissipation across the regulation device (2).

The device contains just three elements: a band-gap reference, an error amplifier, a pass element. The device has four pins: V_{in} , V_{out} , ADJUST and GND. ADJUST pin allows user to adjust the output according to the reference voltage (see Fig. 1).

The working principle of LDO voltage regulator (see Fig. 1) can be summarized as follows:

- Output voltage (V_{out}) is sampled from feedback network, and a portion of it (V_{fb}) is given to input of error amplifier.
- The other input of error amplifier (V_{ref}) is taken from voltage reference circuitry
- The error amplifier compares these two inputs.

- If the $V_{ref} > V_{fb}$, output of the error amplifier (V_g) will become low, and pass transistor will become open. Therefore, V_{out} is fed by supply and increase.

- If the $V_{fb} > V_{ref}$, output of the error amplifier (V_g) will become high, and pass transistor will become close. Therefore, there will be no path between supply and output which leads V_{out} to decrease.

- Since these operations keep continuing in a loop, stable output can be obtained.

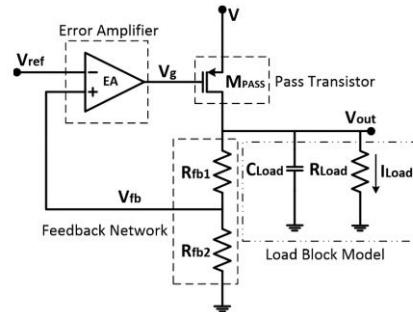


Figure 1: Block diagram for a simple LDO Voltage Regulator

2 Design

In this project, the device consists of two main parts: BGR and Error Amplifier. An ideal regulator has an output independent from load, temperature and supply. In this part, the device are tried to be idealized as much as possible according to the specifications given.

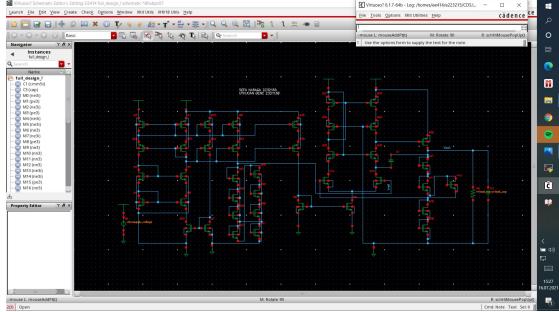


Figure 2: Device Design for $V_{ref} = 600\text{mV}$

2.1 Requirements

2.1.1 Overall Device Requirements

- Maximum Power Dissipation: $\leq 1\mu\text{W}$
- Maximum Output Current: $50\ \mu\text{A}$
- Output Voltage Change w/ Temp: $\leq 10\ \text{mV}$
- Line Regulation: $\leq 5\ \text{mV}$
- Load Regulation: $\leq 1\ \text{mV}$
- Output Voltage, V_{out} : $1.5\ \text{V}$

2.1.2 BGR Circuitry Requirements

- Variation w/ Temp: $\leq 1\%$ of V_{ref}
- Variation w/ Supply Voltage: $\leq 1\%$ of V_{ref}
- PSRR: $\leq -80\ \text{dB}$
- Supply Current: $10\ \text{nA} \leq I_{V_{DD}} \leq 75\ \text{nA}$

2.2 Band-gap Voltage Reference Circuitry

According to the literature research executed before, the band-gap reference topology is based on an article, *Design and implementation of a μW CMOS voltage reference circuit based on thermal compensation of V_{gs}* . The decision is made due to the supply voltage range and simplicity of the circuitry (3).

The reference circuitry consists of three subdivisions: Start-up, Resistor-less Beta Multiplier, and Temperature Compensation (3).

2.2.1 Start-Up

The start-up subdivision (RC time constant circuit) includes two PMOS transistors and a capacitor. The first PMOS (Ms1 in Fig. 3) is used in linear region; hence the resistance value of the time constant is obtained. The capacitance value is chosen as $0.6\ \text{pF}$. The second PMOS transistor, Ms2, provides an initial current pulse until the RC time constant circuitry shuts Ms2 down (3).

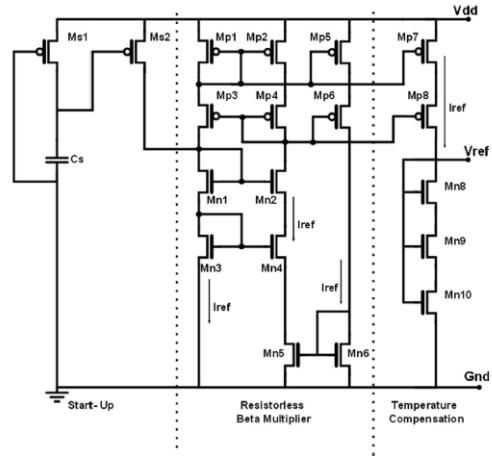


Figure 3: Band-Gap Reference topology preferred for this project (3)

2.2.2 Resistor-less Beta Multiplier

The main purpose of this subdivision is to generate a current that is independent from the supply voltage. In order to achieve that, the reference current, I_{ref} is tried to be a function of transistor parameters only. In addition to that, cascode transistor arrangement (see Fig. 3) is adopted to increase PSRR and to minimize the channel-length modulation effect on I_{ref} (3).

Before starting the derivation, the operation regions of the NMOS transistors should be explained. The NMOS transistors, Mn3 and Mn4 are operating in subthreshold region. Mn5 is in deep - triode region with strong inversion. Mn6 is diode connected; hence it operates in strong saturation region. Since the PMOS transistors are in current mirror configuration, the drain currents flowing on each branch is equal to I_{ref} (5).

Drain currents of Mn5 and Mn6 can be expressed as

$$I_{D5} = S_5 \cdot K_n \cdot (V_{gs5} - V_{thn}) \cdot V_{ds5} \quad (1)$$

$$I_{D6} = S_6 \cdot \frac{K_n}{2} \cdot (V_{gs6} - V_{thn})^2 \quad (2)$$

where K_n is the transconductance parameter, S_i is the aspect ratio of i^{th} transistor, V_{gs} and V_{ds} voltages are gate-to-source and drain-to-source voltages respectively. Since I_{D5} and I_{D6} are equal to each other and named as I_{ref} . By using (1) and (2), reference current can be expressed as

$$I_{ref} = 2 \cdot \frac{S_5^2}{S_6} \cdot K_n \cdot V_{ds5}^2 \quad (3)$$

Considering the loop formed around Mn3, Mn4 and Mn5 (see Fig. 3), Kirchhoff's Voltage Law (KVL) can be applied by using the gate-to-source and drain-to-source voltages. The equation for gate-to-source voltage of Mn3 becomes

$$V_{gs3} = V_{gs4} + V_{ds5} \quad (4)$$

In addition to that, a subthreshold saturation drain current, where the drain current of Mn3 is equal to the reference current, equation can be written as follows

$$I_{ref} = I_{D0} \cdot S_3 \cdot e^{\frac{(V_{gs3} - V_{thn})}{\eta \cdot V_T}} \quad (5)$$

where I_{D0} is the saturation current (5). Since Mn4 operates in subthreshold, (5) can be adapted for I_{D4} , too. From (5), both V_{gs3} and V_{gs4} can be obtained as in following form

$$V_{gs3} = V_{thn} + \eta \cdot V_T \cdot \ln\left(\frac{I_{ref}}{I_{D0} \cdot S_3}\right) \quad (6)$$

By using (4) and (6), V_{ds5} can be expressed as

$$V_{ds5} = \eta \cdot V_T \cdot \ln\left(\frac{S_4}{S_3}\right) \quad (7)$$

By using (7) in (1), the reference current can be finalized as

$$I_{ref} = 2 \cdot \frac{S_5^2}{S_6} \cdot K_n \cdot \eta^2 \cdot V_t^2 \cdot [\ln\left(\frac{S_4}{S_3}\right)]^2 \quad (8)$$

To remark an important point here, I_{ref} is not a function of supply voltage, V_{DD} . On contrary, it is a function of transconductance parameter (K_n), transistors' aspect ratios (S_i) and thermal voltage (V_T). Its dependence on thermal voltage explains the PTAT behavior of this subdivision.

2.2.3 Temperature Compensation

The generated reference current (I_{ref}) is mirrored to the output stage of the BGR circuitry via PMOS transistors, Mp7 and Mp8 (see Fig. 3). One of the main purposes of this subdivision is converting the mirrored current to an output voltage. This voltage is the reference voltage, V_{ref} .

A KVL equation can be written considering the loop formed by NMOS transistors (Mn8, Mn9, Mn10) stack (see Fig. 3). The output voltage becomes

$$V_{ref} = V_{ds8} + V_{ds9} + V_{ds10} \quad (9)$$

It can be noticed that the transistor, Mn8, is diode connected. Hence, it is in strong saturation region.

The drain-to-source voltage of Mn8 can be written as

$$V_{ds8} = V_{gs8} = V_{thn} + \sqrt{\frac{2 \cdot I_{ref}}{S_8 \cdot K_n}} \quad (10)$$

Also from the Figure 3, it can be noticed that

$$V_{gs10} = V_{ref} \quad (11)$$

The drain-to-source voltage of the Mn9 can be rearranged as

$$V_{gs9} = V_{ref} - V_{ds10} = V_{ds8} + V_{ds9} \quad (12)$$

The NMOS transistors, Mn9 and Mn10 are in linear region. The drain current expression for Mn9 is

$$I_{D9} = S_9 \cdot K_n \cdot [(V_{gs9} - V_{thn}) \cdot V_{ds9} - \frac{V_{ds9}^2}{2}] \quad (13)$$

$$I_{D9} = I_{D10} = I_{ref} \quad (14)$$

By inserting (10) into (12), and then inserting the new equation into (13), a quadratic equation is obtained.

$$V_{ds9}^2 + (2 \cdot \sqrt{\frac{2 \cdot I_{ref}}{S_9 \cdot K_n}}) \cdot V_{ds9} - 2 \cdot \frac{I_{ref}}{S_9 \cdot K_n} = 0 \quad (15)$$

Another quadratic equation for Mn10 can be derived by using a similar approach used in (15)

$$V_{ds10}^2 + (2,828 \cdot \sqrt{\frac{2 \cdot I_{ref}}{S_{10} \cdot K_n}}) \cdot V_{ds10} - 2 \cdot \frac{I_{ref}}{S_{10} \cdot K_n} = 0 \quad (16)$$

Solving these quadratic equations, (15) and (16), yields

$$V_{ds9} = 0,414 \cdot \sqrt{\frac{2 \cdot I_{ref}}{S_9 \cdot K_n}} \quad (17)$$

$$V_{ds10} = 0,586 \cdot \sqrt{\frac{2 \cdot I_{ref}}{S_{10} \cdot K_n}} \quad (18)$$

By inserting (10), (17) and (18) into (9), the output voltage can be expressed as

$$V_{ref} = V_{thn8} + \chi_s \sqrt{\frac{2 \cdot I_{ref}}{K_n}} \quad (19)$$

where χ_s stands for

$$\chi_s = \sqrt{\frac{1}{S_8}} + 0,414 \cdot \sqrt{\frac{1}{S_9}} + 0,586 \cdot \sqrt{\frac{1}{S_{10}}} \quad (20)$$

The reference current is converted into a reference voltage. However, the temperature dependency of the output voltage should be investigated. The first order temperature dependence of the threshold voltage is expressed as

$$V_{thn}(T) = V_{thn}(T_0) - \kappa_n \cdot (T - T_0) \quad (21)$$

where T is the temperature in question, T_0 is the absolute temperature, and κ_n is the Temperature Coefficient (TC) of the threshold voltage of the NMOS transistor. κ_n is derived as

$$\kappa_n = \left| \frac{\phi_{ms}}{T} + \frac{2\phi_F}{T} + \frac{\gamma(N_s, t_0x, W, L)}{\sqrt{2\phi_F + V_0 + |V_{SB}|}} \right| \quad (22)$$

By substituting (8), (20) and (21) into 19, the output voltage is arranged as

$$V_{ref} = [V_{thn}(T_0) - \kappa_n \cdot (T - T_0)]_a + [\chi_s \cdot \frac{S_5}{\sqrt{S_6}} \cdot \eta \cdot V_T \cdot \ln(\frac{S_4}{S_3})]_b \quad (23)$$

The first part, a , is function of the V_{thn} , and it decreases with the increasing temperature. However, the second part, b , is function of the thermal voltage, V_T , and increases with increasing temperature. If (23) is differentiated with respect to temperature, TC of the reference voltage is obtained as

$$\frac{\partial V_{ref}}{\partial T} = -\kappa_n + [\chi_s \cdot \frac{S_5}{\sqrt{S_6}} \cdot \eta \cdot V_T \cdot \frac{K}{q} \cdot \ln(\frac{S_4}{S_3})] \quad (24)$$

According to the result obtained in (24), desired temperature compensation can be obtained by adjusting device geometry and the temperature coefficient of the threshold voltage with respect to each other.

2.3 Error Amplifier

Error amplifier takes output of band-gap voltage reference and feedback network as its inputs, and compare them. Therefore, the sensitivity of error amplifier is important. In order to achieve better sensitivity, gain should be increased. For the design, telescopic amplifier whose schematic is given in figure 4 is used. Also, the gain of telescopic amplifier is given in (25).

$$A_v = g_{m_{N1,2}} R_o \quad (25)$$

where

$$R_o = [(g_{m_{N9}} r_{oN9} r_{oN2}) // (g_{m_{P4}} r_{oP4} r_{oP6})] \quad (26)$$

As the aspect ratios of the transistors increases, the gain also increases, however output voltage

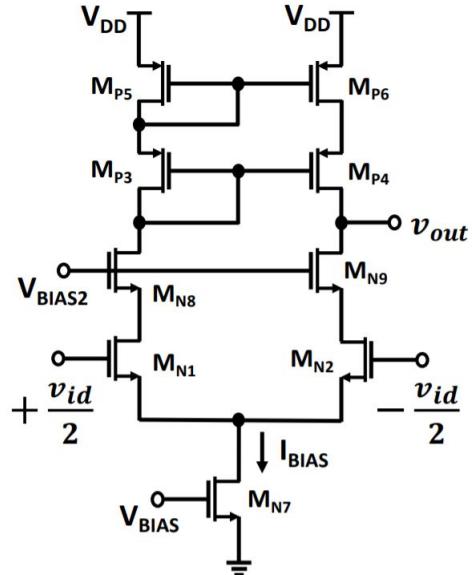


Figure 4: Error Amplifier [6]

swing decreases. So, the aspect ratios are determined to maximize gain while having enough output voltage swing to open and close the pass transistor.

2.4 Pass Transistor

Pass transistor is used as a switch between supply voltage, and output voltage. When it is open, it allows the supply voltage to feed output voltage. On the other hand, when it is closed, there will be no path between supply and output voltage. In the design PMOS transistor is used as pass transistor.

2.5 Feedback Network

Feedback network is used to take a portion of output voltage as an input of error amplifier. If resis-

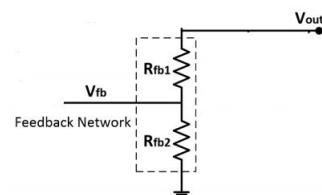


Figure 5: Feedback Network

tive feedback is used as it is given in figure 5 , the output voltage can be calculated by using (27).

$$V_{out} = (1 + \frac{R_{fb1}}{R_{fb2}}) * V_{ref} \quad (27)$$

In the design, depletion type NMOS transistor whose gate and drain are short-circuited is used

as resistor. Since using different aspect ratios cause strong temperature sensitivity, identical NMOSs are used and deserved ratio is obtained by changing the number of NMOSs.

2.6 Design Modifications

In overall circuitry, some design modifications are made in order to satisfy the requirements given. Most of these modifications belong to the band-gap reference circuitry. The modifications done are listed below with their justifications.

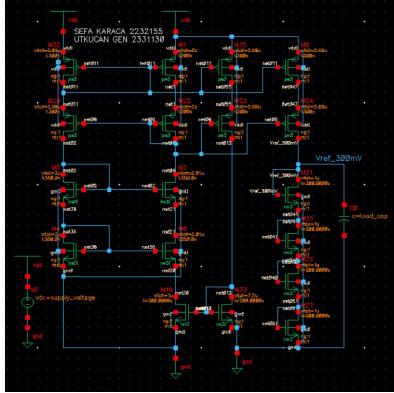


Figure 6: Modified Reference Circuitry for $V_{ref} = 300mV$

- Start - up subdivision in BGR circuitry is eliminated in order to reduce the supply current of the reference circuitry (see Fig. 6).
- Mn5 in Figure 3 is selected as Depletion Mode NMOS in order to keep Mn5 in linear region always (see Fig. 6).
- Mn8, Mn9, Mn10 are diode connected and they are selected as Depletion Mode NMOS to construct a resistive structure with a positive TC (see Fig. 6).
- Aspect ratios of Mp1 and Mp3, Mp2 and Mp4, Mp5 and Mp6, Mp7 and Mp8 are selected equal since they are cascade structure. This cascade structure reduce the supply voltage dependency.
- Aspect ratios of Mp1, Mp3, Mp5, Mp6, Mp7 and Mp8 are selected equal since they all used as current mirror(to copy current). This ratio is selected as small as possible to reduce power consumption. Also, this reference current is used to bias error amplifier, so it is adjusted to be in nA scale. In addition, this

ratio and the aspect ratios of Mn8, Mn9 and Mn10 are adjusted in iterative manner in order to suppress temperature dependency.

- Aspect ratio of Mn5 is selected as high as possible to achieve high resistance value in order to decrease current, so the power consumption.
- Aspect ratios of Mn3 and Mn4 are chosen as slightly different than each other. During the application of iterative method, it is observed that the supply voltage dependence increases with the increasing aspect ratio difference (note that S_3 is taken as constant). In addition to that, a slight difference between the aspect ratios yielded better line regulation than the same aspect ratio case.
- A slight difference is introduced between the aspect ratios of Mn1 and Mn2 too due to the same reason stated previously.

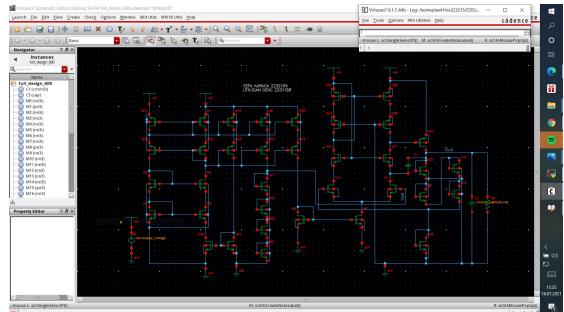


Figure 7: Device Design for $V_{ref} = 300mV$

3 Test Results

Since there are two different requirements categories, tests conducted for the reference circuitry and the overall device are examined under different sections. Test results for the 300 mV and 600 mV cases are examined under the same sections.

3.1 Band-Gap Reference Circuitry

3.1.1 Power Supply Rejection Ratio (PSRR)

In order to obtain PSRR values, AC magnitude of 1 V is given the supply voltage, and AC analysis is applied. As expected, as the frequency increases, PSRR value becomes worse. The results for typical and corner simulations for 300 mV and 600 mV band-gap reference circuits are given below.

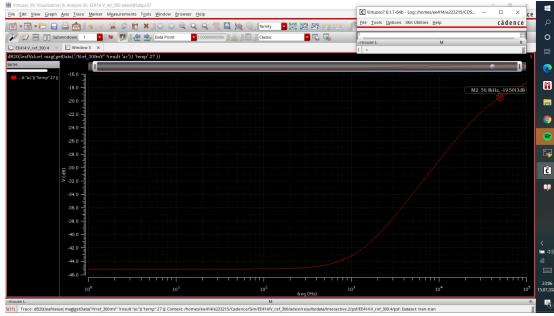


Figure 8: PSRR, Typical Simulation ($V_{ref} = 300mV$)

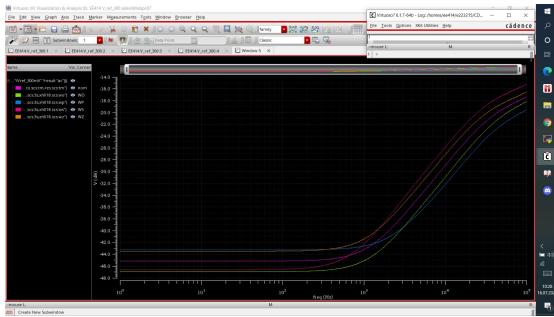


Figure 9: PSRR, Corner Simulation ($V_{ref} = 300mV$)

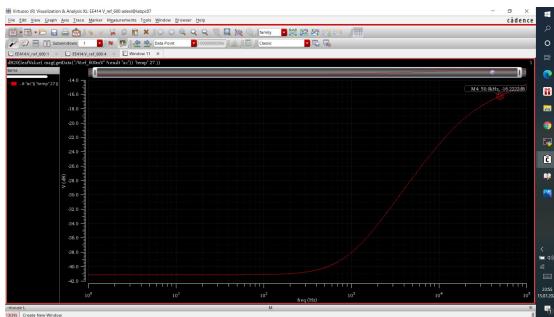


Figure 10: PSRR, Typical Simulation ($V_{ref} = 600mV$)

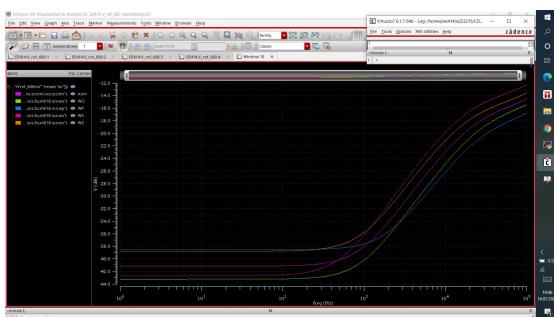


Figure 11: PSRR, Corner Simulation ($V_{ref} = 600mV$)

3.1.2 Variation w/ Temperature

The temperature dependency results of output of band-gap reference voltage circuits are given below.

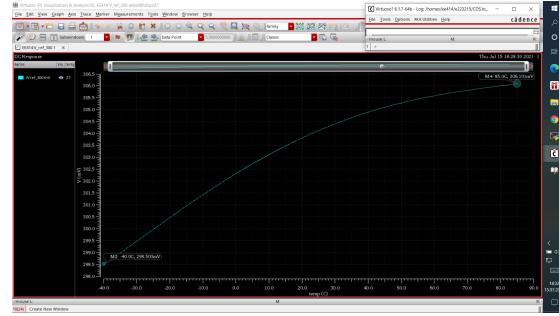


Figure 12: V_{ref} vs. T ($V_{ref} = 300mV, V_{DD} = 3.3V$)

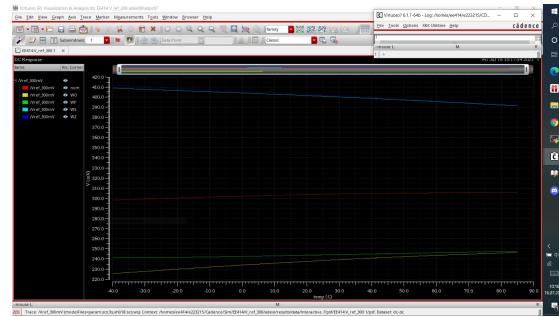


Figure 13: V_{ref} vs. T ($V_{ref} = 300mV$, Corner Simulation)

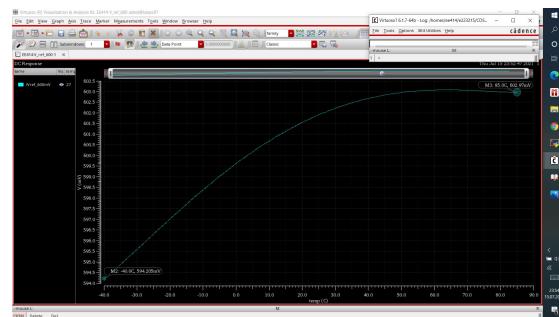


Figure 14: V_{ref} vs. T ($V_{ref} = 600mV, V_{DD} = 3.3V$)

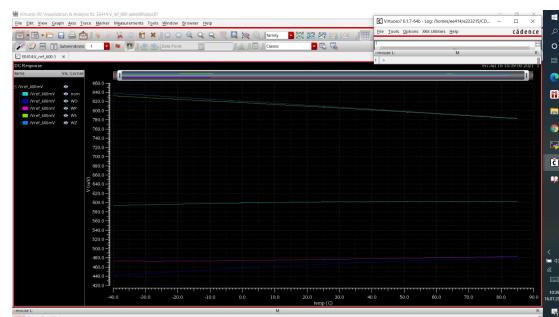


Figure 15: V_{ref} vs. T ($V_{ref} = 600mV$, Corner Simulation)

3.1.3 Variation w/ Supply Voltage

The supply voltage dependency results of output of band-gap reference circuits for different temperature values are given below.

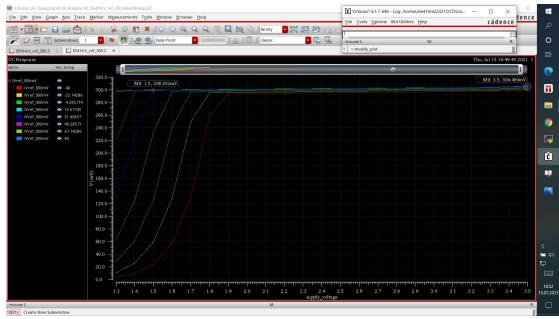


Figure 16: V_{ref} vs. V_{DD} ($V_{ref} = 300mV$)

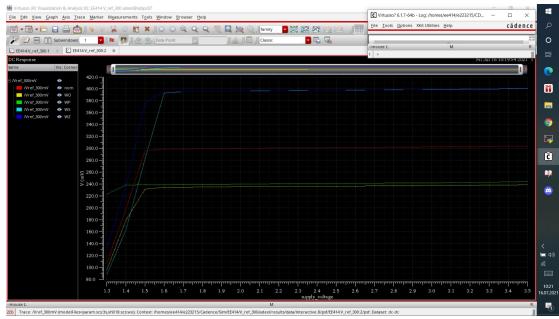


Figure 17: V_{ref} vs. V_{DD} , Corner Simulation ($V_{ref} = 300mV$)

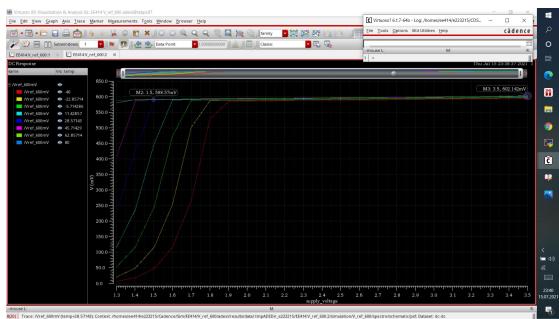


Figure 18: V_{ref} vs. V_{DD} ($V_{ref} = 600mV$)

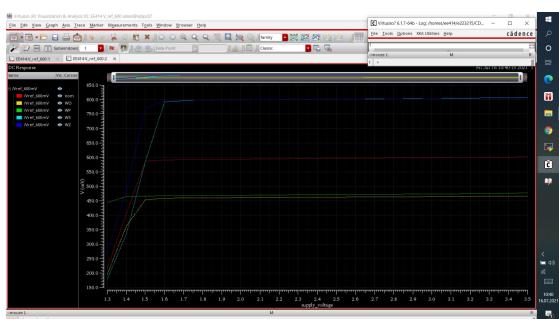


Figure 19: V_{ref} vs. V_{DD} , Corner Simulation ($V_{ref} = 600mV$)

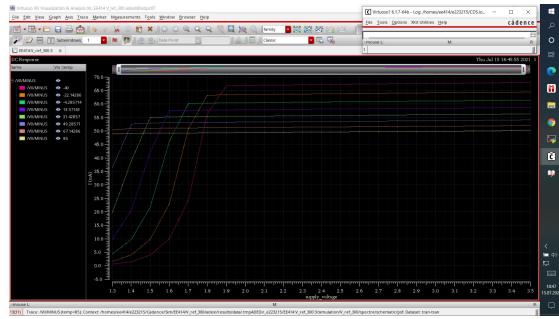


Figure 20: $I_{V_{DD}}$ vs. V_{DD} ($V_{ref} = 300mV$)

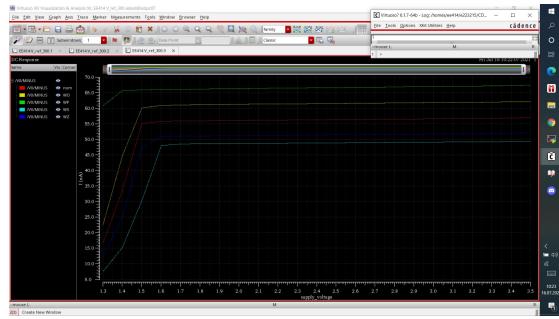


Figure 21: $I_{V_{DD}}$ vs. V_{DD} , Corner Simulation ($V_{ref} = 300mV$)

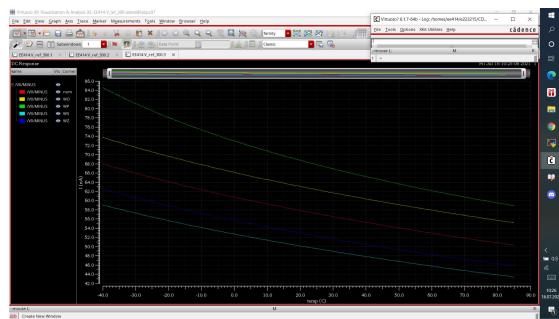


Figure 22: $I_{V_{DD}}$ vs. T , Corner Simulation ($V_{ref} = 300mV$)

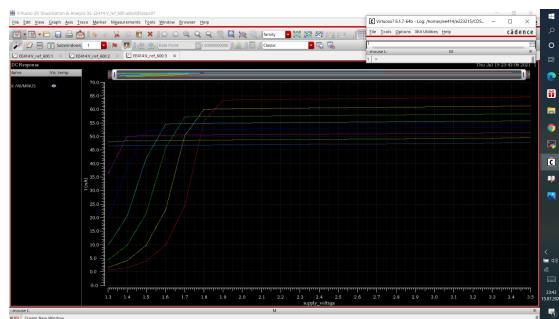


Figure 23: $I_{V_{DD}}$ vs. V_{DD} ($V_{ref} = 600mV$)

3.1.4 Supply Current

The supply voltage and temperature dependency results of supply current of reference circuits are given below.

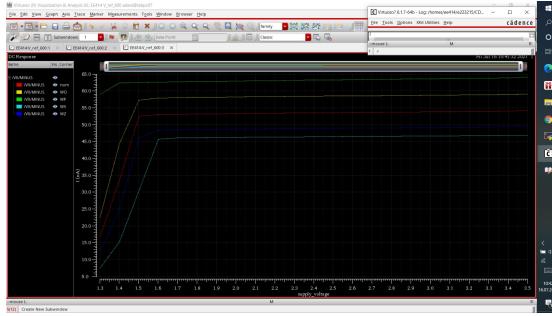


Figure 24: $I_{V_{DD}}$ vs. T , Corner Simulation ($V_{ref} = 600mV$)

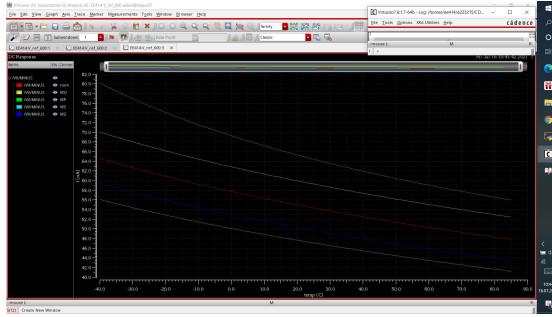


Figure 25: $I_{V_{DD}}$ vs. T , Corner Simulation ($V_{ref} = 600mV$)

3.2 Overall Circuitry

3.2.1 Output Voltage Consistency

Output voltages values of LDO voltage regulator for different temperatures and supply voltages are given below.

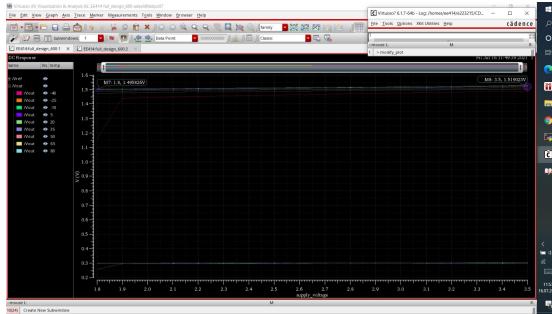


Figure 26: V_{out} vs. T & V_{DD} ($V_{ref} = 300mV$)



Figure 27: V_{out} vs. T & V_{DD} ($V_{ref} = 600mV$)

3.2.2 Power Dissipation

Power dissipation values of LDO voltage regulator at $V_{DD} = 3.5V$ and $T = 23\text{degree}$ are given below.

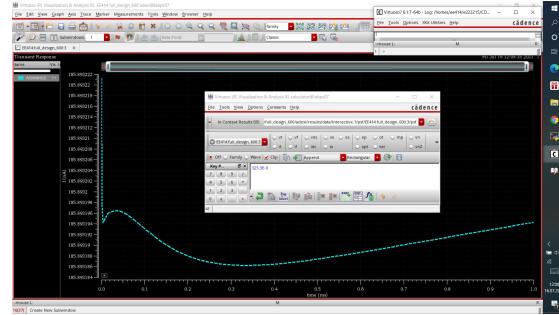


Figure 28: Power Consumption of the device ($v_{ref} = 300mV$)

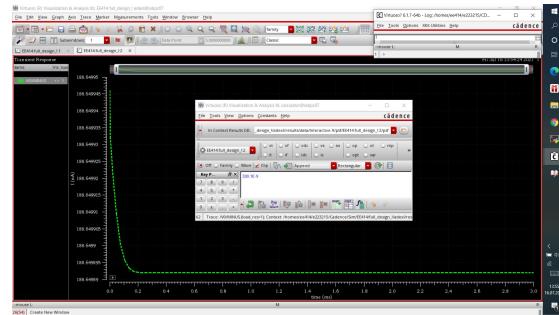


Figure 29: Power Consumption of the device ($v_{ref} = 600mV$)

3.2.3 Variation w/ Temperature @ No Load

Temperature dependency of LDO voltage regulator for different supply voltages are given below.

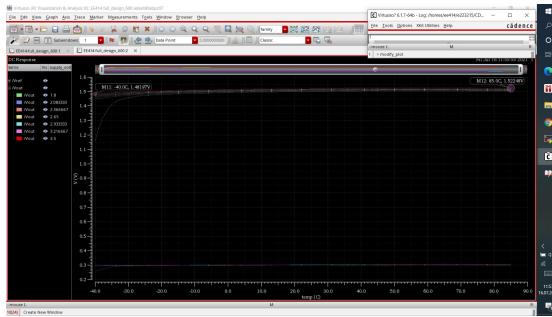


Figure 30: V_{ref} vs. T ($V_{ref} = 300mV$)

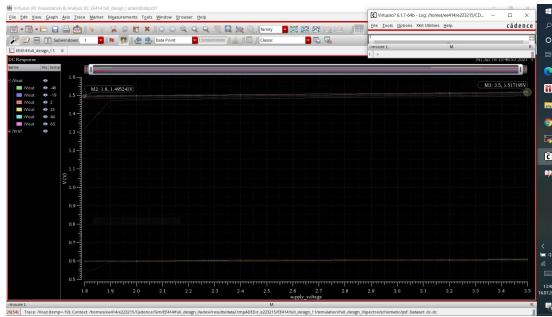


Figure 31: V_{ref} vs. T ($V_{ref} = 600mV$)

3.2.4 Line Regulation @ No Load

Supply voltage dependency of LDO voltage regulator for different temperatures are given below.



Figure 32: V_{ref} vs. V_{DD} ($V_{ref} = 300mV$)



Figure 33: V_{ref} vs. V_{DD} ($V_{ref} = 600mV$)

3.2.5 Load Regulation

Load dependency of LDO voltage regulator for different temperatures and supply voltages are given below.

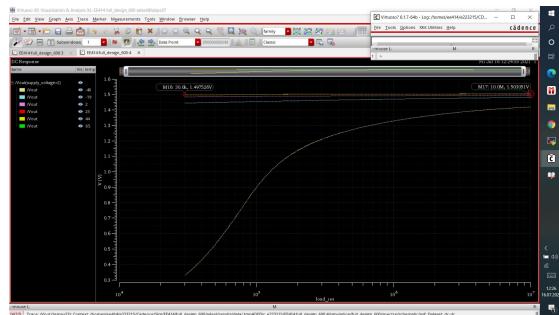


Figure 34: R_{load} vs. T ($V_{ref} = 300mV$)

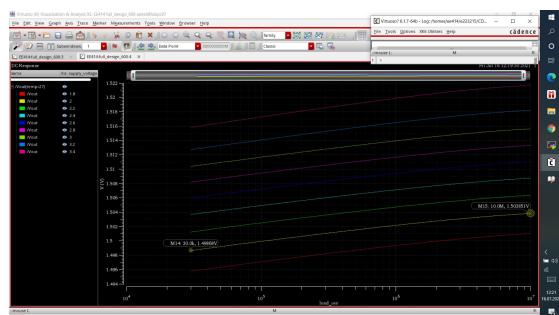


Figure 35: R_{load} vs. V_{DD} ($V_{ref} = 300mV$)

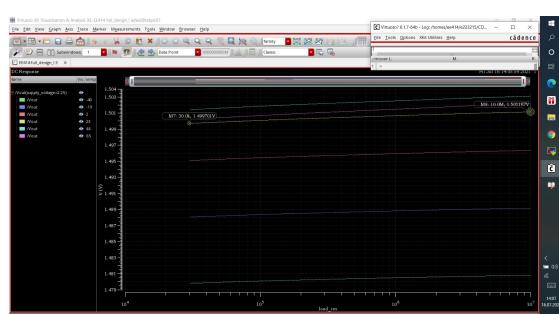


Figure 36: R_{load} vs. T ($V_{ref} = 300mV$)

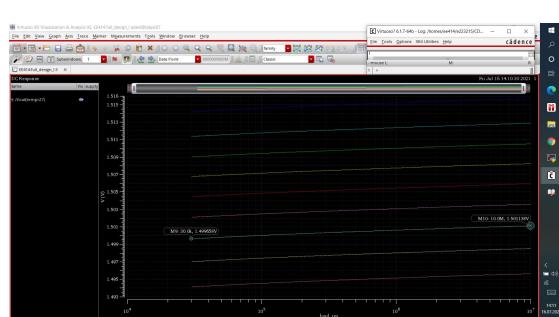


Figure 37: R_{load} vs. V_{DD} ($V_{ref} = 600mV$)

4 Discussions

For $V_{ref} = 300mV$, circuit operates in the desired region under every temperature greater than -25°C . Between -40°C and -25°C , circuit operates in the desired region when the supply voltage is greater than 2 Volts. In another saying, at the lower boundary of the supply voltage range, circuit needs an environment hotter than -25°C . The same situation is valid for $V_{ref} = 600mV$.

The measured PSRR (-46 dB) is lower than the required value ($\leq 80 \text{ dB}$).

Load regulation when $V_{ref} = 600mV$ is slightly higher than the required value. The measured value is $\sim 1.47mV$ whereas the required value is less than $1mV$. However, load regulation drastically increases when the reference voltage drops to $300mV$. For $V_{ref} = 300mV$, the load regulation is measured as $\sim 5.3mV$. When the behavior of the load regulation under different temperature and supply voltages is examined, the load regulation stays nearly constant in every case when the reference voltage is $600mV$. However, the load regulation is inversely proportional to the temperature when the reference voltage is $300mV$. In another saying, the load regulation gets better as the temperature increases. In addition to that, when $V_{ref} = 300mV$ and $T = -40^{\circ}\text{C}$, the output voltage behavior is non-linear (see Fig. 34). PSRR value and the load regulation can be enhanced by cascading another PMOS branch (3); however, this solution may cause supply current to increase. Hence, lower PSRR worse load regulation are preferred to higher supply current. Also, this solution may lead output voltage swing to decrease, or increase in the minimum supply voltage.

Overall power consumption of the device satisfies the requirements for both reference voltages ($325.3nW$ w/ $V_{ref} = 300mV$ & $330.1nW$ w/ $V_{ref} = 600mV$).

The undesired reference voltages obtained in the Corner Simulations is due to the design adopted by the authors. Since the branch current is forced to be changed abruptly, the resistance seen from the output due to the NMOS stack changes. Moreover, this NMOS stack is responsible for the conversion of the branch current into the reference voltage. Hence, the reference voltage exceeds the desired level.

The circuit can be said *Temperature Invariant* when V_{DD} exceeds $1.9V$.

5 Conclusions

There are various band-gap reference topologies can be used for an LDO regulator; however, only all-MOS configurations were allowed for this project. Despite the impression that this restriction made, there are many different all-MOS BGR topologies, too. For this project, a topology among fifteen is selected to become a milestone. At the end, the selected topology became modified by the authors according to the requirements given.

The error amplifier topology is selected as a telescopic amplifier. At the end of the amplifier, a feedback is ensured via a pass element.

In this project, resistor and BJT usage are prohibited. Therefore, MOS transistors in linear region are used as resistors. For temperature compensation, diode connected NMOS transistors are used to give V_{be} reference since BJT usage is not permitted.

At the end, the device satisfies the requirements except Power Supply Rejection Ratio (PSRR). Further proposals and analyses are made in the *Discussions* section.

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