Techniques for Static Detection of Data-Races in OpenMP Programs



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Problem Statement

Software Bugs



"Bug" or "Glitch" or "Anomaly" or "Defect" is the incorrectness in software behaviour.

"Bug" word is popularized by Grace Hopper when she traced a problem in the Harvard Mark II system to a Moth trapped in the system.



Major Incidents due to Software Bugs



Bugs can result in "Fault"/"Error" or "Failure"/"Crash".

Major Incidents due to Software Bugs



Bugs can result in "Fault"/"Error" or "Failure"/"Crash".









- Ariane Flight V88 Explosion
- Mariner 1 Launch Failure
- Therac-25 Radiation Therapy Accident (lives lost)
- Northeast Blackout of 2003
- Heathrow Terminal 5 Opening Blunder (500 flights cancelled)

Problem Statement

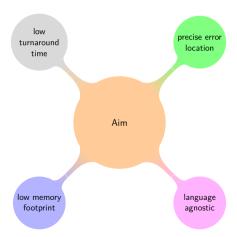


Provide a solution to the problem of statically detecting data-races in shared-memory parallel programs.

Problem Statement



Provide a solution to the problem of statically detecting data-races in shared-memory parallel programs.

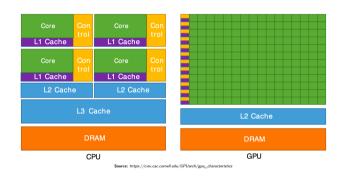


Shared-Memory Systems & Parallel Programming



Parallel Programming Models

- Shared Memory
- Message Passing
- Partitioned Global Address Space (PGAS)



Shared-Memory Programming Languages: Cilk, Cilk Plus, C++11, C#, CUDA, Java, OpenMP, Threading Building Blocks, etc.

OpenMP Parallel Programming



Open Multi-Processing (OpenMP) is a framework for C, C++ and FORTRAN programs to enable shared-memory parallel programming on a multi-threaded system.

OpenMP **Supports**:

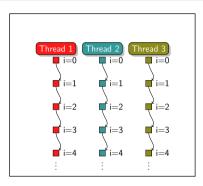
- Single Program Multiple Data (SMPD) programming model
- Single Instruction Multiple Data (SIMD) programming model
- Divide-and-conquer paradigm with tasks
- Data environment for shared-memory consistency
- Mutual exclusion and atomicity
- Implicit and explicit synchronization

OpenMP is portable across architectures from different vendors. (e.g. CPU, GPU, and FPGA [Mayer et al., 2019])

OpenMP Execution Model: parallel construct



OpenMP parallel construct

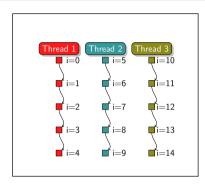


OpenMP thread execution model for parallel construct

OpenMP Execution Model: parallel for construct



OpenMP worksharing for construct



OpenMP thread execution model for parallel for construct

What is a Data-Race?



DRB013: Example with data-race due to improper synchronization

Definition (Data-Race)

An execution of a concurrent program is said to have a data-race when

- two threads access the same memory location,
- accesses are not protected by a mutual exclusion mechanism (e.g., locks),
- the order of the two accesses is non-deterministic,
- one of these accesses is a write.



Missing data sharing clauses

```
#pragma omp parallel for \
private (temp,i,j)

for (i = 0; i < len; i++)

for (j = 0; j < len; j++){
    temp = u[i][j];
    sum = sum + temp * temp;
}</pre>
```

DRB021: OpenMP Worksharing construct with data-race



- Missing data sharing clauses
- Loop carried dependences

```
1 for (i = 0; i < n; i++) {
2 #pragma omp parallel for
3 for (j = 1; j < m; j++) {
4          b[i][j] = b[i][j-1];
5     }
6 }</pre>
```

DRB038: Example with Loop Carried Dependence



- Missing data sharing clauses
- Loop carried dependences
- SIMD races

```
1 #pragma omp simd
2 for (int i = 0; i < len-1; i++){
3     a[i+1] = a[i] + b[i];
4 }</pre>
```

DRB024: Example with SIMD data-race



- Missing data sharing clauses
- Loop carried dependences
- SIMD races
- Synchronization issues

DRB013: Example with data-race due to improper synchronization



- Missing data sharing clauses
- Loop carried dependences
- SIMD races
- Synchronization issues
- Control flow dependent on number of threads

Control flow dependent on number of threads

Proposed Solutions for Race Detection



- Using Polyhedral Dependence Analysis
- Using May-Happen-in-Parallel (MHP) Analysis

Race Detection using Polyhedral Dependence Analysis







1 for (i = 0; i < m; i++) {
2 #pragma omp parallel for</pre>

for (j = 1; j < n; j++) {



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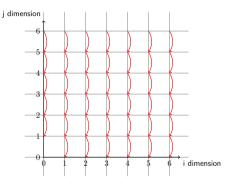






```
1  for (int i = 0; i < m; i++) {
2  #pragma omp parallel for
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6  }</pre>
```

Example with Loop Carried Dependence



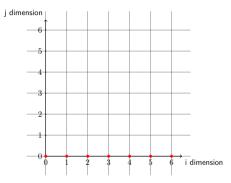
Dependence Polyhedra

Technique 1: Race Detection using Polyhedral Dependences



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1  for (int i = 0; i < m; i++) {
2  #pragma omp parallel for
3   for (int j = 1; j < n; j++) {
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5   }
6 }</pre>
```

Example with Loop Carried Dependence



Projection of the Dependence Polyhedra on i-dimension

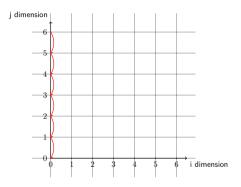
Zero magnitude of the projections on a dimension signifies that the dimension is parallel.

Technique 1: Race Detection using Polyhedral Dependences



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1  for (int i = 0; i < m; i++) {
2  #pragma omp parallel for
3   for (int j = 1; j < n; j++) {
4    b[i][j] = b[i][j-1];
5   }
6  }</pre>
```

Example with Loop Carried Dependence



Projection of the Dependence Polyhedra on j-dimension

Non-zero magnitude of the projections on a dimension signifies that the dimension is not parallel.

Overcoming Limitations of the Polyhedral Framework



• Limited scope of the Polyhedral framework (less coverage).

```
void f1(int* q) {
   *q += 1;
   // None-affine code
}

int main() {
   int i = 0;
   #pragma omp parallel
   { f1(&i); }
}
```

Non-affine program

Overcoming Limitations of the Polyhedral Framework



- Limited scope of the Polyhedral framework (less coverage).
- Cannot handle inter SCoP (Static Control Parts) dependences.

```
void f1(int* q) {
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}
```

Non-affine program

DRB013: Example with data-race due to improper synchronization

Overcoming Limitations of the Polyhedral Framework



- Limited scope of the Polyhedral framework (less coverage). Use Dependence Testing
- Cannot handle inter SCoP (Static Control Parts) dependences. Use MHP Analysis

```
void f1(int* q) {
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   // None-affine code
}

int main() {
   int i = 0;
   #pragma omp parallel
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Non-affine program

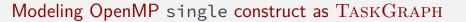
DRB013: Example with data-race due to improper synchronization

Race Detection using May-Happen-in-Parallel Analysis

Technique 2: Overview



- Perform Phase Interval Analysis (PIA) in the Monotone framework [Kildall, 1973]
 - Construct a TASKGRAPH for the OpenMP constructs
 - Compute Phase Intervals ([lb, ub]) for each basic block
- Perform May-Happen-in-Parallel (MHP) analysis using the Phase Intervals
 - Compute MHP sets for each basic block
- Use MHP sets to detect data-races statically





```
1 #pragma omp parallel
     // S1
4 #pragma omp single
    // S2
  } // implicit barrier
     // S3
9 #pragma omp single
11
    // S4
 } // implicit barrier
   // S5
13
```

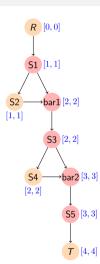
Multiple OpenMP single constructs

Modeling OpenMP single construct as TASKGRAPH



```
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      // S2
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9 #pragma omp single
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       // S4
     } // implicit barrier
     // S5
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```

Multiple OpenMP single constructs



 ${\rm TASKGRAPH}$ for the OpenMP single construct annotated with phase intervals.





```
1 #pragma omp parallel
      // S1
4 #pragma omp master
        // S2
      // S3
9 #pragma omp master
        // S4
      // S5
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```

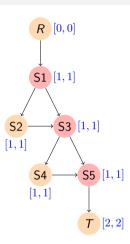
Multiple OpenMP master constructs

Modeling OpenMP master construct as TASKGRAPH



```
1 #pragma omp parallel
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4 #pragma omp master
        // S2
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         S5
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```

Multiple OpenMP master constructs



 ${\rm TASKGRAPH}$ for the OpenMP master construct annotated with phase intervals.



Definition (Reduced TASKGRAPH)

A reduced TaskGraph $G = \langle V, E, R, T \rangle$ consists of:

- ullet the vertex set V of implicit and explicit tasks.
- the edge set $E \subseteq V \times V$ contains directed edges.
- a special vertex R for the root of the graph.
- ullet a special sentinel vertex T that represents the termination of all the tasks.

Modeling OpenMP constructs for Phase Interval Analysis (PIA)



Definition (Phase)

A phase, represented by a positive integer $p \in \mathbb{N}^+ \cup \infty$, is the execution number of an instance of the nodes in the TASKGRAPH.

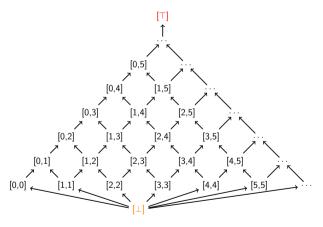
A program can execute in phases due to:

- the presence of barriers
- upon entry to a parallel region
- upon exit from a parallel region.



Lattice : $(I, \sqsubseteq, \sqcup, \sqcap)$ is a lattice over an interval domain I.

Top element: $T = [0, \infty]$. Bot element: \bot .

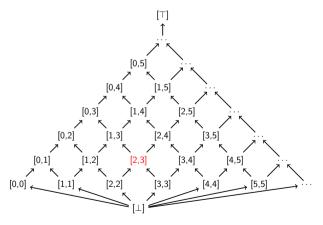


Interval Lattice for PIA



Lattice : $(I, \sqsubseteq, \sqcup, \sqcap)$ is a lattice over an interval domain I.

Interval (PI): $[Ib, ub] \in I$, where Ib is lower bound & ub is upper bound.

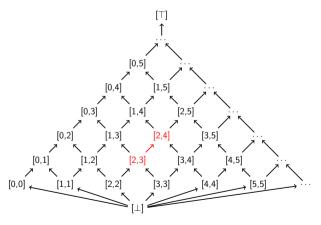


Interval Lattice for PIA



Lattice : $(I, \sqsubseteq, \sqcup, \sqcap)$ is a lattice over an interval domain I.

Partial Order (\sqsubseteq) : $[lb_1, ub_1] \sqsubseteq [lb_2, ub_2] \iff lb_2 \le lb_1 \le ub_1 \le ub_2$.

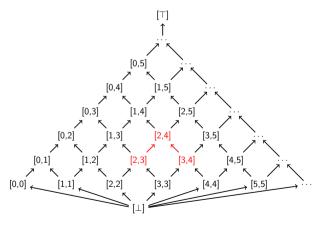


Interval Lattice for PIA



Lattice : $(I, \sqsubseteq, \sqcup, \sqcap)$ is a lattice over an interval domain I.

Join Operation (\sqcup): $[lb_1, ub_1] \sqcup [lb_2, ub_2] \Longrightarrow [\min(lb_1, lb_2), \max(ub_1, ub_2)].$

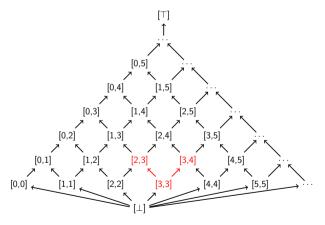


Interval Lattice for PIA



Lattice : $(I, \sqsubseteq, \sqcup, \sqcap)$ is a lattice over an interval domain I.

Meet Operation (\sqcap) : $[lb_1, ub_1] \sqcap [lb_2, ub_2] \implies [\max(lb_1, lb_2), \min(ub_1, ub_2)].$



Interval Lattice for PIA

Phase Interval Analysis



Data flow Equation for Phase Interval Analysis for a node $S \in G$ is defined as:

$$PI_{in}[S] = \bigsqcup_{p \in pred[S]} PI_{out}[p]$$

where the confluence operator is the join operation (\sqcup), p is an immediate predecessor node of S, and pred[S] is the set of all the immediate predecessor nodes of $S \in G$.

Phase Interval Analysis



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where the confluence operator is the join operation (\sqcup), p is an immediate predecessor node of S, and pred[S] is the set of all the immediate predecessor nodes of $S \in G$.

Transfer Function is defined as:

$$PI_{out}(S) = f(PI_{in}(S)) = \begin{cases} PI_{in}(S), & \text{Identity function, if } S \\ & \text{does not have a barrier.} \\ PI_{in}(S) + [1,1], & \text{otherwise.} \end{cases}$$

The binary operator + is defined as $[lb_1, ub_1] + [lb_2, ub_2] = [lb_1 + lb_2, ub_1 + ub_2].$

Phase Interval Analysis: Termination Guarantee



Widening is defined as:

$$[\mathit{Ib}_1, \mathit{ub}_1] \nabla_{[\mathit{Ibt}, \mathit{ubt}]}[\mathit{Ib}_2, \mathit{ub}_2] = \begin{cases} \left[\mathit{Ibt}, \mathit{ubt} \right] & \text{if } \mathit{ub}_1 < \mathit{ub}_2 \\ \left[\mathit{Ibt}, \mathit{ub}_1 \right] & \text{otherwise} \end{cases} \\ \left\{ \begin{bmatrix} \mathit{Ib}_1, \mathit{ub}_1 \right] & \text{if } \mathit{ub}_1 < \mathit{ub}_2 \\ \left[\mathit{Ib}_1, \mathit{ub}_1 \right] & \text{if } \mathit{ub}_1 < \mathit{ub}_2 \\ \left[\mathit{Ib}_1, \mathit{ub}_1 \right] & \text{otherwise} \end{cases} \\ \text{otherwise} \end{cases}$$

where *lbt* and *ubt* are widening thresholds.

Phase Interval Analysis: Termination Guarantee



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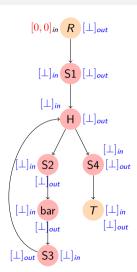
where *lbt* and *ubt* are widening thresholds.

For a loop header H and loop trip count TC, widening is applied as:

$$PI_{\mathit{in}}(H) = \begin{cases} PI_{\mathit{in}}^0(H) \sqcup (PI_{\mathit{in}}^0(H) + (\mathit{TC} * (PI_{\mathit{in}}^0(H) \Delta PI_{\mathit{in}}^1(H)))) & \text{if the trip count } \mathit{TC} \text{ is known} \\ PI_{\mathit{in}}^0(H) \nabla_{[0,\infty]} PI_{\mathit{in}}^1(H) & \text{otherwise} \end{cases}$$

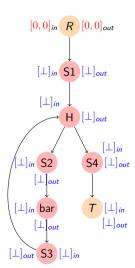
where difference (Δ) : $[lb_1, ub_1]\Delta[lb_2, ub_2] \implies [lb_2 - lb_1, ub_2 - ub_1]$.





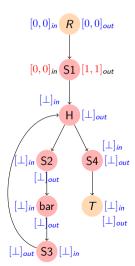


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1 #pragma omp parallel
2  {
3     // S1
4     for (int i = 0; i < 100; i++) {
5         // S2
6 #pragma omp barrier
7         // S3
8     }
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```



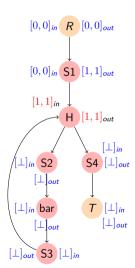


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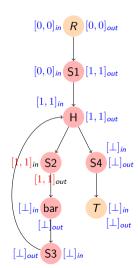


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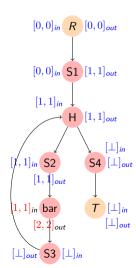


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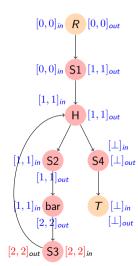


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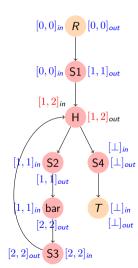


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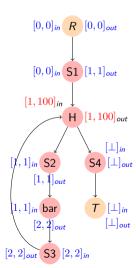


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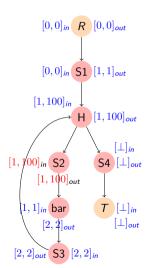




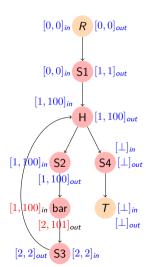
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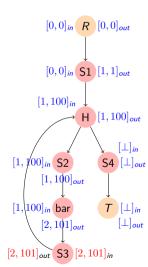




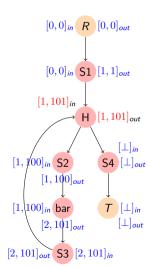






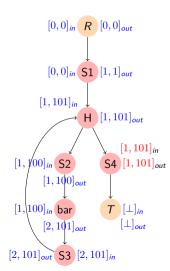






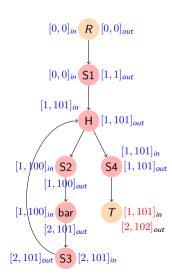


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Technique 2: May-Happen-in-Parallel (MHP) Analysis



Given: TASKGRAPH and Phase Intervals.

Question: Can the two statements S1 and S2 be executed in parallel?

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Given: TASKGRAPH and Phase Intervals. Question: Can the two statements S1 and S2 be executed in parallel?

```
1 #pragma omp parallel shared(b, error)
2 {
3 #pragma omp for nowait
4    for(i = 0; i < len; i++)
5     a[i] = b + a[i] * 5; //S1
6 #pragma omp single
7    error = a[9] + 1; //S2
8 }</pre>
```

Answer: Instances of two nodes $u, v \in G$ may run in parallel if and only if $PI[u] \cap PI[v]$. Here the binary operator \bigcap on the phase intervals $PI_1 = [Ib_1, ub_1]$ and $PI_2 = [Ib_2, ub_2]$ is:

$$PI_1 \bigcap PI_2 = egin{cases} true, & \mathit{lb}_1 \leq \mathit{ub}_2 \leq \mathit{ub}_1 \lor \\ & \mathit{lb}_2 \leq \mathit{ub}_1 \leq \mathit{ub}_2 \\ \mathit{false}, & \mathsf{otherwise}. \end{cases}$$

Implementation Details

Implementation Details



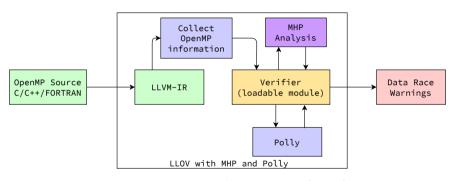
Designed and implemented a static data-race checker, LLOV, in the LLVM compiler framework.

LLOV:

- is based on the intermediate representation of LLVM (LLVM-IR)
- uses polyhedral dependence analysis
- uses May-Happen-in-Parallel analysis
- can handle OpenMP programs in C/C++/FORTRAN
- also can conservatively state when a program is data-race free

LLOV: Architecture





Flow Diagram of LLVM OpenMP Verifier (LLOV)

LLOV: Reconstructing pragmas from IR



```
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```

```
Directive: OMP Parallel
 Variables:
   Private: %.omp.ub = alloca i32, align 4
   Private: %.omp.lb = alloca i32, align 4
   Shared: i32* %i
   Shared: i32* %len
   Firstprivate: i64 %vla
   Shared: i32* %a
   Shared: i32* %h
   Shared: i32* %error
   Private: %.omp.stride = alloca i32, align 4
   Private: %.omp.is last = alloca i32, align 4
 Child Directives:
 1: Directive:
                  OMP_Workshare_Loop
   Schedule type: Static Schedule (auto-chunked)
 2: Directive:
                  OMP Workshare single
 3: Directive:
                   OMP Barrier
```

In-memory representation of a directive.

LLOV: Reconstructing pragmas from IR



```
1 #pragma omp parallel shared(b, error)
2 {
3 #pragma omp for nowait
4     for(i = 0; i < len; i++)
5     a[i] = b + a[i]*5;
6 #pragma omp single
7     error = a[9] + 1;
8 }</pre>
```

```
Directive: OMP Parallel
 Variables:
   Private: %.omp.ub = alloca i32, align 4
   Private: %.omp.lb = alloca i32, align 4
   Shared: i32* %i
   Shared: i32* %len
   Firstprivate: i64 %vla
   Shared: i32* %a
   Shared: i32* %h
   Shared: i32* %error
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   Schedule type : Static Schedule (auto-chunked)
 2: Directive: OMP Workshare single
 3: Directive:
                   OMP Barrier
```

```
<Directive> ::= <Dtvpe> [ <Sched> ] { <Var> } { <Directive> }
<Dtype>
            ::= parallel | for | simd
                  workshare | sections
                  section | single | master
                  critical | atomic
                  target | distribute
            ::= <Vtvpe> val
<Var>
<Vtvpe>
            ::= private | firstprivate
                  lastprivate | threadprivate
                  shared | reduction
<Sched>
            ::= [ <modifier> ] [ ordered ] <Stype> <chunk>
<modifier>
            ::= monotonic | nonmonotonic
<Stype>
            ::= static | dvnamic
                | guided | auto | runtime
<chunk>
            ::= <non-negative integer>
```

Data-Race Reporting in LLOV (Goal 1)



Data-Race: The source memory access MA₁ (in basic block u) and sink memory access MA₂ (in basic block v) of a data dependence may potentially race if $PI[u] \cap PI[v]$.

Error reporting: LLOV highlights the source location of the race condition.

Experimental Evaluation

Evaluation



We evaluate our work on two metrics:

- Compare Performance with seeded benchmarks
- Measure Scalability with real world applications

Experimental Setup



Benchmarks

- DataRaceBench C/C++ v1.3.2 [Verma et al., 2020] to evaluate performance
 - 172 Kernels, 83 kernels with data-races, 89 kernels without any data-race
- 22 ECP Proxy application to evaluate scalability (1 million LOC)
- DataRaceBench FORTRAN [Kukreja et al., 2019]

Experimental Setup



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 - 172 Kernels, 83 kernels with data-races, 89 kernels without any data-race
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System Specifications

System: Two Intel Xeon E5-2697 v4 @ $2.30\mbox{GHz}$ processors

OS: 64 bit Ubuntu 20.04.2 LTS Server

Kernel: Linux kernel version 5.4.0-71-generic

Threads: $72 (2 \times 36)$ hardware threads

Memory: 128GB

OpenMP library: LLVM OpenMP runtime v5.0.1 (libomp5)

Other Race Detection Tools



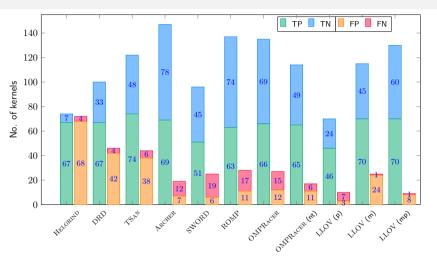
Race detection tools with the version numbers and flags used for comparison. Dynamic tool, Static tool.

Tools	Version	Flags	OpenMP	Compiler
HELGRIND [Valgrind-project, 2007b]	3.15.0	-tool=helgrind	gomp	gcc 9.3
VALGRIND DRD [Valgrind-project, 2007a]	3.15.0	-tool=drd -check-stack-var=yes	gomp	gcc 9.3
TSAN-LLVM [Serebryany et al., 2011]	12.0.1	ignore_noninstrumented_modules=1	lomp	clang 12.0
ARCHER [Atzeni et al., 2016]	5b37681	ignore_noninstrumented_modules=1	lomp	clang 6.0
SWORD [Atzeni et al., 2018]	7a08f3c	-analysis-tool=sword-race-analysis	lomp	clang 7.1
ROMP [Gu and Mellor-Crummey, 2018]	v2.0		gomp	gcc 9.3
OMPRACER [Swain et al., 2020]	0.1.1	-no-filter -silent -nolimit	lomp	clang 9.0
LLOV (WITH POLLY)	v0.3	openmp-verify-use-llvm-da=false	lomp	clang 12.0
LLOV (WITH MHP)	v0.3	openmp-verify-use-polly-da=false	lomp	clang 12.0
LLOV (WITH MHP & POLLY)	v0.3	-Xclang -disable-O0-optnone	lomp	clang 12.0

Unavailable tools: $\underline{OMPVERIFY}$ [Basupalli et al., 2011], $\underline{POLYOMP}$ [Chatarasi et al., 2016], and \underline{DRACO} [Ye et al., 2018].

Performance: DataRaceBench v1.3.2 Results





Tools (nt for without tasks, p for Polly, m for MHP, mp for MHP and Polly)

Maximum number of races reported by different tools in DataRaceBench v1.3.2

Performance: DataRaceBench v1.3.2 Statistics



Precision, Recall, and Accuracy of the tools on DataRaceBench v1.3.2

Tools	Precision	Recall	Accuracy	F1 Score	Diagnostic Odds Ratio
HELGRIND	0.50	0.94	0.51	0.65	1.72
Valgrind DRD	0.61	0.94	0.68	0.74	13.16
TSAN-LLVM	0.66	0.93	0.73	0.77	15.58
Archer	0.91	0.85	0.89	0.88	64.07
SWORD	0.89	0.73	0.79	0.80	20.13
ROMP	0.85	0.79	0.83	0.82	24.93
OMPRACER	0.85	0.81	0.83	0.83	25.30
OMPRACER (notasks)	0.86	0.92	0.87	0.88	48.26
LLOV (WITH POLLY)	0.94	0.87	0.88	0.90	52.57
LLOV (WITH MHP)	0.74	0.99	0.82	0.85	131.25
LLOV (WITH MHP & POLLY)	0.90	0.99	0.94	0.94	525.00

Scalability Analysis on million LOC



22 Miscellaneous Benchmarks used for Scalability Analysis

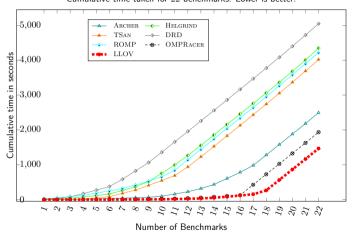
Benchmark	Domain	KLOC	Benchmark	Domain	KLOC
AMG	Parallel Algebraic Multigrid Solver	64.9	NBody	Parallel N-body Simulation	0.4
CoMD	Molecular Dynamics Simulation	6.1	openmp-tutorial	SC OpenMP Tutorial	10.4
COVID-SIM	COVID-19 Transmission Dynamics	19.0	OpenMP-Microbench	OpenMP Performance Benchmarking	1.0
LCALS	Livermore Loops	6.6	ParallelResearchKernels	Parallel Architectures	106.2
LULESH	Shock Hydrodynamics	5.5	QuickSilver	Monte Carlo Particle Transport	10.0
miniAMR	Adaptive Mesh Refinement	17.7	Rodinia	Parallel Computing Benchmark Suite	186.4
miniBUDE	Molecular Docking	9.5	RSBench	Monte Carlo Neutron Transport	6.0
miniFE	Finite Element	297.8	sw4lite	Geodynamics	54.2
miniQMC	Quantum Monte Carlo Simulation	31.9	Sundials	Nonlinear ODE Solver	186.9
miniVite	Louvain Method for Community Detection	2.4	TriangleCounting	Parallel Triangle Counting	0.8
NAS-Parallel	Performance of Parallel Supercomputers	15.9	XSBench	Monte Carlo Neutron Transport	6.7

Combined total of 1 million lines of code.

Scalability Analysis: Runtime (Goal 2)



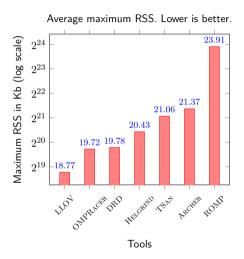




Cactus plot of different race detection tools on 22 miscellaneous benchmarks.

Scalability Analysis: Memory Footprint (Goal 3)





Average maximum resident set size (RSS) of the tools across all the 22 miscellaneous benchmarks

DataRaceBench FORTRAN (Goal 4)



An implementation of DataRaceBench C/C++v1.2 [Liao et al., 2017] in FORTRAN 95.

- \bullet Demonstrate LLOV is language agnostic
- Created DataRaceBench FORTRAN
 - Converted 92 (out of 116) C/C++ kernels
- Open-sourced the benchmark [Kukreja et al., 2019]

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 $^{^{1}}$ Earlier version of LLOV. FORTRAN frontend (FLANG) generating LLVM-IR is replaced by a new frontend (F18) that does not yet generate LLVM-IR.

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An implementation of DataRaceBench C/C++ v1.2 [Liao et al., 2017] in FORTRAN 95.

- Demonstrate LLOV is language agnostic
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- Open-sourced the benchmark [Kukreja et al., 2019]

Maximum number of races reported by different tools in DataRaceBench FORTRAN

Tools	Race	: Yes	Race	: No	Coverage/92	
10015	TP	FN	TN	FP	Coverage/92	
HELGRIND	46	6	4	36	92	
Valgrind DRD	45	7	21	19	92	
LLOV v0.2 ¹	36	7	19	5	67	

¹Earlier version of LLOV. FORTRAN frontend (FLANG) generating LLVM-IR is replaced by a new frontend (F18) that does not yet generate LLVM-IR.

OpenMP v4.5 Pragma Handling Status



Comparison of OpenMP pragma handling by OpenMP aware tools.(Y for Yes, N for No)

OpenMP Pragma	LLOV	OMPRACER	OMPVERIFY	POLYOMP	DRACO	SWORD	Archer	ROMP
#pragma omp parallel	Υ	Υ	Υ	Υ	Υ	Υ	Υ	Υ
#pragma omp for	Υ	Υ	Υ	Y	Y	Y	Υ	Υ
#pragma omp parallel for	Υ	Υ	Υ	Y	Y	Y	Υ	Υ
#pragma omp critical	Υ	Υ	N	N	N	Y	Υ	Υ
#pragma omp atomic	Υ	Υ	N	N	N	Υ	Υ	Υ
#pragma omp master	Υ	Υ	N	Υ	N	Υ	Υ	Υ
#pragma omp single	Υ	Υ	N	Υ	N	Υ	Υ	Υ
#pragma omp simd	Υ	Υ	N	N	Υ	N	N	N
#pragma omp parallel for simd	Υ	Υ	N	N	Υ	N	N	N
#pragma omp parallel sections	Υ	N	N	N	N	Υ	Υ	Υ
#pragma omp sections	Υ	N	N	N	N	Υ	Υ	Υ
#pragma omp threadprivate	Υ	Υ	N	N	N	N	Υ	Υ
#pragma omp ordered	Υ	N	N	N	N	N	Υ	Υ
#pragma omp distribute	Υ	Υ	N	N	N	N	Υ	Υ
#pragma omp task	N	N	N	N	N	N	Υ	Υ
#pragma omp taskgroup	N	N	N	N	N	N	Υ	Υ
#pragma omp taskloop	N	N	N	N	N	N	Υ	Υ
#pragma omp taskwait	N	N	N	N	N	N	Υ	Υ
#pragma omp barrier	Υ	Υ	N	Y	N	Υ	Υ	Υ
#pragma omp teams	Υ	Υ	N	N	N	N	N	N
#pragma omp target	Υ	Υ	N	N	N	N	N	N

Summary



We proposed and implemented a fast, static data-race checker for shared-memory parallel programs using

- Polyhedral Dependence Analysis
- May-Happen-in-Parallel (MHP) Analysis

Summary



We proposed and implemented a fast, static data-race checker for shared-memory parallel programs using

- Polyhedral Dependence Analysis
- May-Happen-in-Parallel (MHP) Analysis

Observations

- Using only precise dependence analysis results in low coverage but high precision
- Using only MHP analysis results in more coverage but less precision

Conclusion

• Combination of precise dependence analysis and MHP analysis results in high precision, high accuracy, and better coverage

Future Directions



Handling explicit tasks in OpenMP

Support tasking constructs: task, taskloop, taskgroup, and taskwait.

None of the static techniques support tasking. (Open Problem).

MLIR based LLOV

Use OpenMP dialect of MLIR in place of LLVM-IR.

PIA for Optimization

PIA for C++ threads and pthreds will be interesting, and will expose classic compiler optimizations on shared-memory parallel programs.

List of Publications



Utpal Bora, Santanu Das, Pankaj Kukreja, Saurabh Joshi, Ramakrishna Upadrasta, and Sanjay Rajopadhye. 2020. "LLOV: A Fast Static Data-Race Checker for OpenMP Programs." ACM Trans. Archit. Code Optim. 17, 4, Article 35 (December 2020), 26 pages. DOI:https://doi.org/10.1145/3418597

- Utpal Bora, Shraiysh Vaishay, Saurabh Joshi and Ramakrishna Upadrasta, "OpenMP aware MHP
 Analysis for Improved Static Data-Race Detection", 2021 IEEE/ACM 7th Workshop on the LLVM
 Compiler Infrastructure in HPC (LLVM-HPC), 2021, pp. 1-11, doi: 10.1109/LLVMHPC54804.2021.00006
- Shalini Jain, Utpal Bora, Prateek Kumar, Vaibhav B. Sinha, Suresh Purini and Ramakrishna Upadrasta, "An analysis of executable size reduction by LLVM passes." CSI Transactions on ICT 7, 105110 (2019). doi: 10.1007/s40012-019-00248-5

Thank you for your time! Questions?

LLOV is freely available for download.

Link: https://github.com/utpalbora/llov

Blog: https://compilers.cse.iith.ac.in/projects/llov/



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Thank You!!

References I





Atzeni, S., Gopalakrishnan, G., Rakamarić, Z., Ahn, D. H., Laguna, I., Schulz, M., Lee, G. L., Protze, J., and Müller, M. S. (2016).

ARCHER: effectively spotting data races in large openmp applications.

In 2016 IEEE International Parallel and Distributed Processing Symposium, IPDPS 2016, Chicago, IL, USA, May 23-27, 2016, pages 53–62. IEEE Computer Society.



Atzeni, S., Gopalakrishnan, G., Rakamarić, Z., Laguna, I., Lee, G. L., and Ahn, D. H. (2018).

SWORD: A bounded memory-overhead detector of openmp data races in production runs.

In 2018 IEEE International Parallel and Distributed Processing Symposium, IPDPS 2018, Vancouver, BC, Canada, May 21-25, 2018, pages 845–854. IEEE Computer Society.



Basupalli, V., Yuki, T., Rajopadhye, S., Morvan, A., Derrien, S., Quinton, P., and Wonnacott, D. (2011).

ompverify: Polyhedral analysis for the openmp programmer.

In Chapman, B. M., Gropp, W. D., Kumaran, K., and Müller, M. S., editors, OpenMP in the Petascale Era - 7th International Workshop on OpenMP, WOMP 2011, Chicago, IL, USA, June 13-15, 2011. Proceedings, volume 6665 of Lecture Notes in Computer Science, pages 37–53, Berlin, Heidelberg, Springer Berlin Heidelberg.



Chatarasi, P., Shirako, J., Kong, M., and Sarkar, V. (2016).

An extended polyhedral model for SPMD programs and its use in static data race detection.

In Ding, C., Criswell, J., and Wu, P., editors, Languages and Compilers for Parallel Computing - 29th International Workshop, LCPC 2016, Rochester, NY, USA, September 28-30, 2016, Revised Papers, volume 10136 of Lecture Notes in Computer Science, pages 106–120. Springer.



Gu, Y. and Mellor-Crummey, J. (2018).

Dynamic data race detection for openmp programs.

In Proceedings of the International Conference for High Performance Computing, Networking, Storage, and Analysis, SC '18. IEEE Press.

References II





Kildall, G. A. (1973).

A unified approach to global program optimization.

In Proceedings of the 1st Annual ACM SIGACT-SIGPLAN Symposium on Principles of Programming Languages, POPL '73, page 194206, New York, NY, USA. Association for Computing Machinery.



Kukreja, P., Shukla, H., and Bora, U. (2019).

DataRaceBench FORTRAN.

https://github.com/IITH-Compilers/drb_fortran.

[Online; accessed 19-October-2019].



Liao, C., Lin, P.-H., Asplund, J., Schordan, M., and Karlin, I. (2017).

Dataracebench: A benchmark suite for systematic evaluation of data race detection tools.

In Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, SC '17, pages 11:1–11:14, New York, NY, USA, ACM.



Mayer, F., Knaust, M., and Philippsen, M. (2019).

Openmp on fpgas—a survey.

In Fan, X., de Supinski, B. R., Sinnen, O., and Giacaman, N., editors, *OpenMP: Conquering the Full Hardware Spectrum*, pages 94–108, Cham. Springer International Publishing.



Serebryany, K., Potapenko, A., Iskhodzhanov, T., and Vyukov, D. (2011).

Dynamic race detection with Ilym compiler.

In Proceedings of the Second International Conference on Runtime Verification, RV'11, pages 110-114, Berlin, Heidelberg. Springer-Verlag.



Swain, B., Li, Y., Liu, P., Laguna, I., Georgakoudis, G., and Huang, J. (2020).

OMPRacer: A Scalable and Precise Static Race Detector for OpenMP Programs.

In Proceedings of the International Conference for High Performance Computing, Networking, Storage and Analysis, SC '20. IEEE Press.

References III





Valgrind-project (2007a).

DRD: a thread error detector.

http://valgrind.org/docs/manual/drd-manual.html. [Online: accessed 08-May-2019].



Valgrind-project (2007b).

Helgrind: a thread error detector.

http://valgrind.org/docs/manual/hg-manual.html.

[Online: accessed 08-May-2019].



Verma, G., Shi, Y., Liao, C., Chapman, B., and Yan, Y. (2020).

Enhancing dataracebench for evaluating data race detection tools.

In 2020 IEEE/ACM 4th International Workshop on Software Correctness for HPC Applications (Correctness), pages 20–30.



Ye, F., Schordan, M., Liao, C., Lin, P., Karlin, I., and Sarkar, V. (2018).

Using polyhedral analysis to verify openmp applications are data race free.

In Laguna, I. and Rubio-González, C., editors, 2nd IEEE/ACM International Workshop on Software Correctness for HPC Applications, CORRECTNESS@SC 2018, Dallas, TX, USA, November 12, 2018, pages 42–50. IEEE.

Extra Slides!

Contributions



- Implemented a fast, static, and language agnostic OpenMP data-race checker
- Demonstrated use of Pohyhedral dependences and MHP in data-race detection
- Proposed and Formalized OpenMP aware MHP Analysis using Phase Interval Analysis
- Created DataRaceBench FORTRAN, an annotated benchmark of data-races in FORTRAN
- Visualization of TASKGRAPH for better developer productivity

Data-Races in Miscellaneous Benchmarks



Number of Data-Races reported by various tools in 22 Miscellaneous Benchmarks

Benchmark	KLOC	LLOV	Tsan	Archer	OMPRACER	ROMP	Helgrind	DRD
AMG	64.9	644	536	97	2489	9520	1000	1000
CoMD	6.1	22	71	0	12	0	367	129
COVID-SIM	19.0	331	2	0	0	0	350	0
LCALS	6.6	18	0	0	0	0	0	0
LULESH	5.5	126	71	0	139	0	1000	648
miniAMR	17.7	7693	0	250	539	146644	159	106
miniBUDE	9.5	0	1	0	0	0	131	57
miniFE	297.8	0	177	0	2	0	743	332
miniQMC	31.9	593	90	0	0	0	193	143
miniVite	2.4	5	66	0	68	14048	393	218
NAS-Parallel	15.9	219	17	84	8	0	73	10
NBody	0.4	18	99	0	4	0	133	140
openmp-tutorial	10.4	4	462	1	1	0	203	24
OpenMP-Microbench	1.0	0	46	2	0	0	335	19
ParallelResearchKernels	106.2	31	13	31	4165	36840	105	33
QuickSilver	10.0	0	48	33	7	0	128	2
Rodinia	186.4	55	166	3590	33	2231871	206	121
RSBench	6.0	0	4	0	0	0	13	0
sw4lite	54.2	42	895	0	0	0	112	112
Sundials	186.9	59	13	64	0	0	164	78
TriangleCounting	0.8	11	100	1	0	0	576	273
XSBench	6.7	0	6	0	0	0	23	0

LLOV: PIA Algorithm I



```
1: Input: TaskGraph G
2: Output: Phase Intervals PI
 3: Data: worklist.
4: function PIA(G)
        worklist.add(G.root)
 5:
        for all n \in G do
 6.
            PI_{out}[n] \leftarrow \bot

    init to bot

            if n has barrier then worklist.add(n) end if
8:
        end for
9:
        PI_{in}[G.root] \leftarrow [0,0]
10:
11:
        while !worklist.empty() do
            n \leftarrow \text{worklist.pop()}
12:
            PI_{in}[n] \leftarrow | | PI_{out}[p]
13:

⊳ join

                        p \in pred[n]
```

LLOV: PIA Algorithm II



```
if n is loop header then
14:
                 PI_{out}[n] \leftarrow w(PI_{in}[n])
15:
             end if
16:
             PI_{out}[n] \leftarrow f(PI_{in}[n])
17:
             if PI_{out}[n] \neq PI_{in}[n] then
18:
                 for all s \in successor(n) do
19:
                      worklist.add(s)
20:
                  end for
21:
             end if
22:
        end while
23.
        return Plout
24:
25: end function
```

▷ transfer

Data-race detection literature



Race detection literature (minimalistic)

Published	Title	Year
TOCS	Eraser: A dynamic data race detector for multithreaded programs	1997
SOSP	RacerX: Effective, Static Detection of Race Conditions and Deadlocks	2003
POPL	Conditional must not aliasing for static race detection	2007
PPoPP	May-happen-in-parallel analysis of X10 program	2007
ESEC-FSE	RELAY: static race detection on millions of lines of code	2007
WBIA	ThreadSanitizer data race detection in practice	2009
IWOMP	ompVerify: Polyhedral Analysis for the OpenMP Programmer	2011
TOPLAS	LOCKSMITH: Practical static race detection for C	2011
LCPC	An extended polyhedral model for SPMD programs and its use in static data race detection	2016
IPDPS	ARCHER: effectively spotting data races in large OpenMP applications	2016
IPDPS	SWORD: A Bounded Memory-Overhead Detector of OpenMP Data Races in Production Runs	2018
Correctness	Using Polyhedral Analysis to Verify OpenMP Applications are Data Race Free	2018
SC	Dynamic Data Race Detection for OpenMP Programs	2018
OOPSLA	RacerD: Compositional Static Race Detection	2018
IWOMP	OMPSan: Static Verification of OpenMPs Data Mapping Constructs	2019
SC	OMPRacer: A Scalable and Precise Static Race Detector for OpenMP Programs	2020
TACO	LLOV: A Fast Static Data-Race Checker for OpenMP Programs	2020



```
#pragma omp parallel shared(a) private(i)
{
    #pragma omp master
    a = 0;

    #pragma omp for reduction(+:a)
    for (i=0; i<10; i++){
        a = a + i;
    }

#pragma omp single
printf("Sum is %d\n", a);
}</pre>
```

DRB140: Example of the only FN case for LLOV



```
#pragma omp parallel
for(int i=0; i<N;i++){
    #pragma omp for
    for(int i=0; i<C; i++){
        temp[i] = b[i] + c[i];
}

#pragma omp for
for(int i=C-1; i>=0; i--){
    b[i] = temp[i] * a;
}
```

DRB159: PIA is not precise due to conservative analysis

Terminology I



- True Positive (TP): If the evaluation tool correctly detects a data-race present in the kernel it is a True Positive test result. A higher number of true positives represents a better tool.
- True Negative (TN): If the benchmark does not contain a race and the tool declares it as race-free, then it is a true negative case. A higher number of true negatives represents a better tool.
- False Positives (FP): If the benchmark does not contain any race, but the tool reports a race condition, it is a false positive. False Positives should be as low as possible.
- False Negatives (FN): False Negative test result is obtained when the tool fails to detect a known race in the benchmark. These are the cases that are missed by the tool. A lower number of false negatives are desirable.

Terminology II



• **Precision :** Precision is the measure of closeness of the outcomes of prediction. Thus, a higher value of precision represents that the tool will more often than not identify a race condition when it exists.

$$Precision = \frac{TP}{TP + FP}$$

• **Recall :** Recall gives the total number of cases detected out of the maximum data-races present. A higher recall value means that there are less chances that a data-race is missed by the tool. It is also called true positive rate (TPR).

$$Recall = \frac{TP}{TP + FN}$$

 Accuracy: Accuracy gives the chances of correct reports out of all the reports, as the name suggests. A higher value of accuracy is always desired and gives overall measure of the efficacy of the tool.

$$Accuracy = \frac{TP + TN}{TP + FP + TN + FN}$$

Terminology III



• F1 Score: The harmonic mean of precision and recall is called the F1 score. An F1 score of 1 can be achieved in the best case when both precision and recall are perfect. The worst case F1 score is 0 when either precision or recall is 0.

$$F1$$
 Score = $2 * \frac{Precision * Recall}{Precision + Recall}$

• Diagnostic odds ratio (DOR): It is the ratio of the positive likelihood ratio (LR+) to the negative likelihood ratio (LR-).

$$DOR = \frac{LR+}{LR-}$$
 where,

Positive Likelihood Ratio $(LR+) = \frac{TPR}{FPR}$,

Negative Likelihood Ratio $(LR-) = \frac{FNR}{TNIR}$,

True Positive Rate $(TPR) = \frac{TP}{TP + FN}$, False Positive Rate $(FPR) = \frac{FP}{FP + TN}$,

False Negative Rate $(FNR) = \frac{FN}{FN + TP}$ and

True Negative Rare $(TNR) = \frac{TN}{TN + FR}$

Terminology IV



DOR is the measure of the ratio of the odds of race detection being positive given that the test case has a data-race, to the odds of race detection being positive given the test case does not have a race.