ECE/CS 552 Fall 2024: Guidelines for Final Project Report

Due date: December 16, 2024, 11:59pm on Canvas

The report should document the work done throughout the three phases, but with heavy emphasis on phase 3. The project report should include the following parts:

1) **Overview:** A brief description and an introduction to your project design. Include a top-level block diagram that shows your module hierarchy.
2) **Responsibility/Task Breakdown:** Include a brief table describing the work performed (with percentages if applicable) by each member of the group, for each phase of the project.
3) **Special features:** Report any special features, any particular effort you have made to optimize the design, and any major problems you encountered in implementing the design.
4) **Completeness:** A statement indicating whether or not your design meets all the requirements specified for phase 1, phase 2, and phase 3. The test programs are short enough where you should be able to hand-calculate what the results should be, and ensure your processor traces match. Make sure to note any missing features or non-functional aspects of your design.
5) **Testing:** A description of the methodology you used to test the correctness of your design. Block level? Full-chip? Mixture of both? Further, what known corner-cases did you test related to arithmetic, forwarding, or stalling?
6) **Results:** A summary of your simulation results for all of the phase3 test programs, which includes the log and trace files. Note that test lists in each phase are not identical. Please include a table that shows the outcome (correct/incorrect) and cycle count for each program. Include a discussion of any incorrect outcomes, explaining where the source of the problem lies. Include a simulation waveform image for each program showing the key signals (minimum the trace signals, and mux selects).
7) **Extra credit synthesis**: If you synthesized your design, clearly state the cycle time you reached, as well as results (outcome and cycle count) for each test case. You can include these in the table from step 5 in separate columns.
8) **Extra credit features:** If you implemented any extra credit features, you must include parts 2-5 above for each feature, including a description of the test cases that you created to verify the correctness of, and demonstrate the advantages of, the optimizations you added.
9) **Verilog Files:** In addition, you should submit all your Verilog files as well as output files for each test case (for the base required phase 3, as well as for any altered versions you created for extra credit).