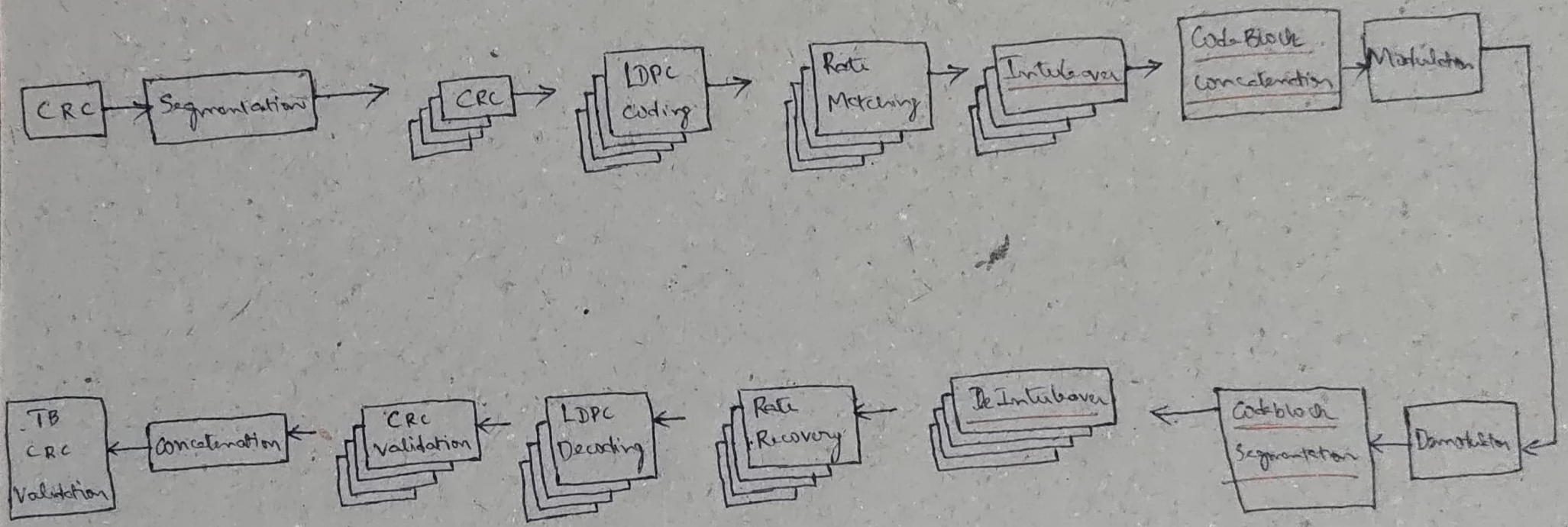
5G Transceiver Chain till Code block Concatenation



① Each rate matched code blocks is interleaved using row-column interleaver.

Rate matching output with length E

Row-column Interleaver (Writing)

$M(=2) \times E/M$,

$M = 2, 4, 6, 8$

Row-column Interleaver (reading)

Interleaver Output

② De-interleave them by reading them appropriately.

⇒ 01001100 01010011

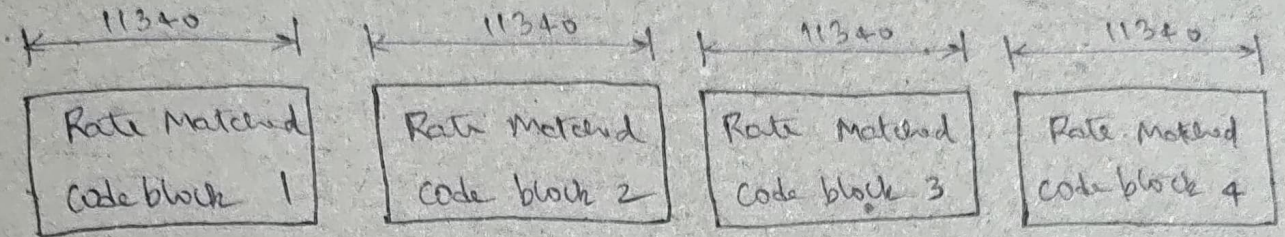
Pseudo code of interleaving. (Sec. 5.4.2.2 of 38.212)

- Row size depends on modulation order – avoid burst errors
- Bits output of Rate Matcher are denoted as $e_0, e_1, e_2, e_3, \ldots, e_{(E-1)}$
- Bits output of interleaver are denoted as $f_0, f_1, f_2, \ldots, f_{(E-1)}$

```
for j = 0 to E / Q_m - 1
    for i = 0 to Q_m - 1
        f_{i+j·Q_m} = e_{i·E/Q_m + j} ;
    end for
end for
```

Concatenation of code blocks

- Rate matched code blocks are sequentially concatenated when $C > 1$



- Rate Matcher output is four code blocks of length 11340 bits
- Total rate matched output bits $11340 \times 4 = 45360$
- Recall total output bits allowed to transmit

$$G = N_{PRB} \times RE \times Q_m = 70 \times 162 \times 4 = 45360$$

- Input and Output bit sequence for the code block concatenation are

f_{rj} for $r = 0, \ldots, (C-1)$ and $j = 0, \ldots, (E_r - 1)$

g_k for $k = 0, \ldots, (G-1)$

Pseudo Code of code block Concatenation (Sec. 5.5 of 38.212)

Set $k = 0$ and $r = 0$

while $r < C$

  Set $j = 0$

  while $j < E_r$

    $g_k = f_{rj}$

    $k = k + 1$

    $j = j + 1$

  end while

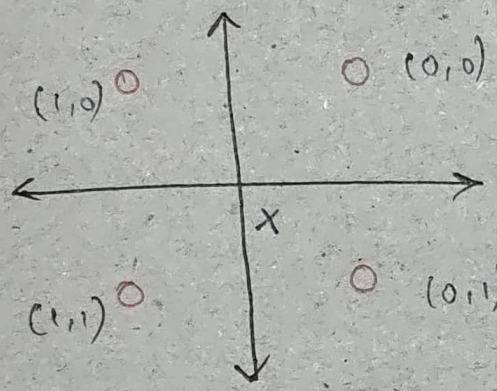
  $r = r + 1$

end while

Modulation / Demodulation (Sec. 5.1 of 38.211)

- 5G NR allows 4/16/64/256-QAM modulation
- Demodulator detects bits from 4/16/64/256-QAM modulated symbols.
- LDPC decoder works on the demodulated bits and not symbols.
  - Not practical to design decoder for different modulation schemes.

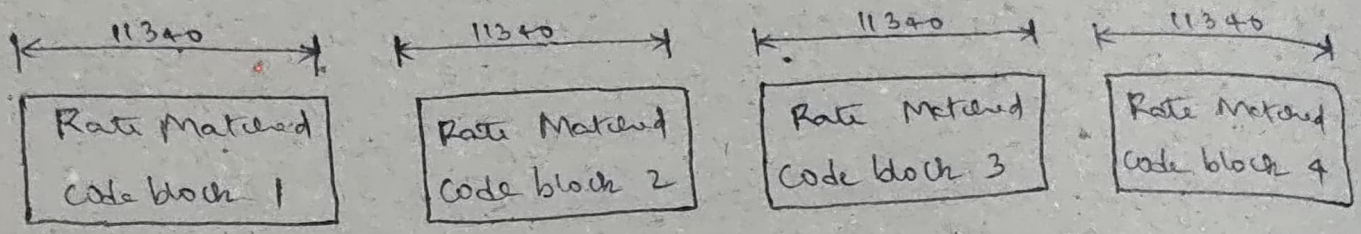
Receiver processing – QPSK demodulation



- Apply the nearest distance detection rule
- Threshold the equalized symbols to the nearest symbol
- Demap the symbols into bits.

Receiver Processing — Code block Segmentation

- Code block Concatenation (Recap)
- Rate matched code blocks are sequentially concatenated when number of code blocks $C > 1$



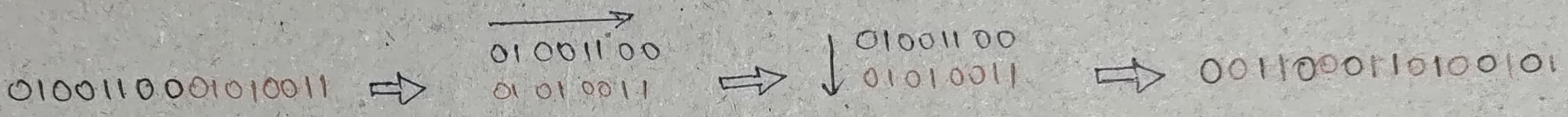
- Length of concatenated output

  $11340 \times 4 = 45360$

- code block Segmentation output is four code blocks of length 11340 bits.
- Total output bits $= 11340 \times 4 = 45360$

De-interleaving of Code blocks

⊙ Each rate matched codeblock is interleaved using row-column interleaver.



Rate Matching Output with length E

Row-column Interleaver (Writing)

Row-column Interleaver (Reading)

Interleaver Output

$M (=2) \times E/M$,

$M = 2, 4, 6, 8$

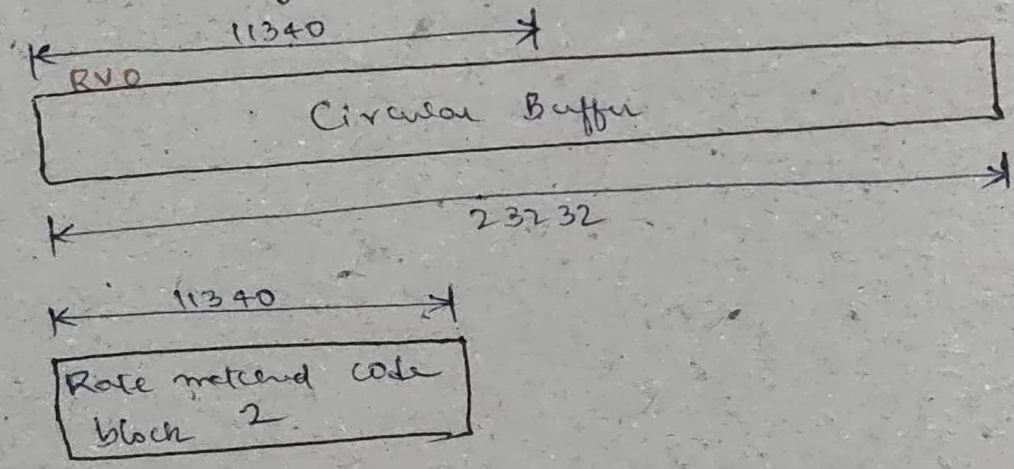
⊙ De-interleave them by reading them appropriately.

Receiver processing – Rate recovery principles

- **Rate matching**
  - Puncturing / repeating bits to match the allocated resources.
- **Rate recovery**
  - LDPC decoder works only for code rate of $\frac{1}{3}$. Code rate should be reverted back to $\frac{1}{3}$.
  - Zeros are inserted in place of punctured bits
  - Repeated bits are combined

5G receiver processing – rate recovery

- Rate recovery of code blocks. Eg: Second code block



- Write bits starting from RV0.
  Write neutral information for bits punctured at transmitter
- Feed rate recovered data to LDPC decoder.
  Validate CRC of each code block.