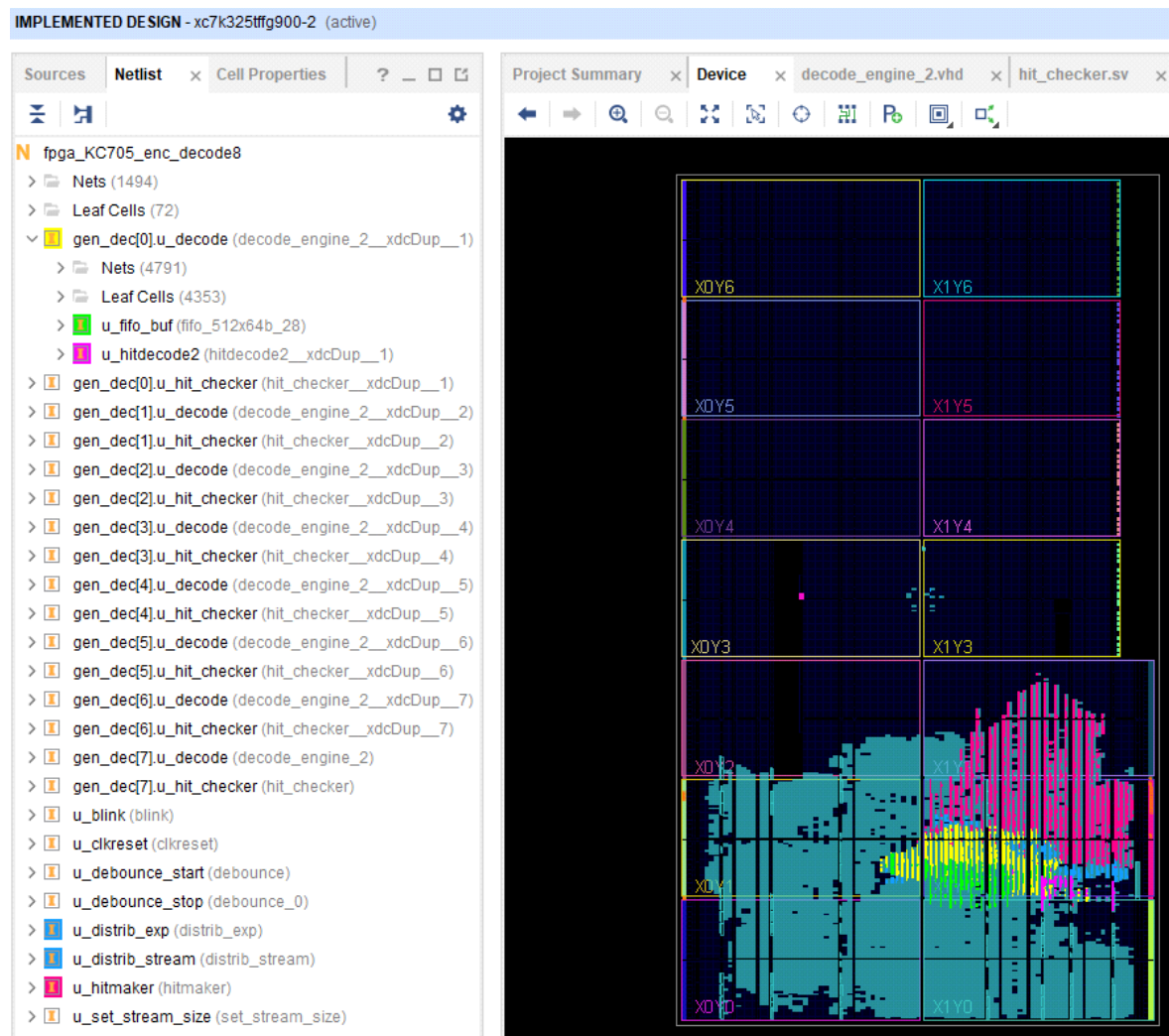


FPGA KC705 8-channel Decoder Usage

Wednesday, February 16, 2022 4:01 PM



Kintex7 xc7k325 device on KC705 board. Entire device

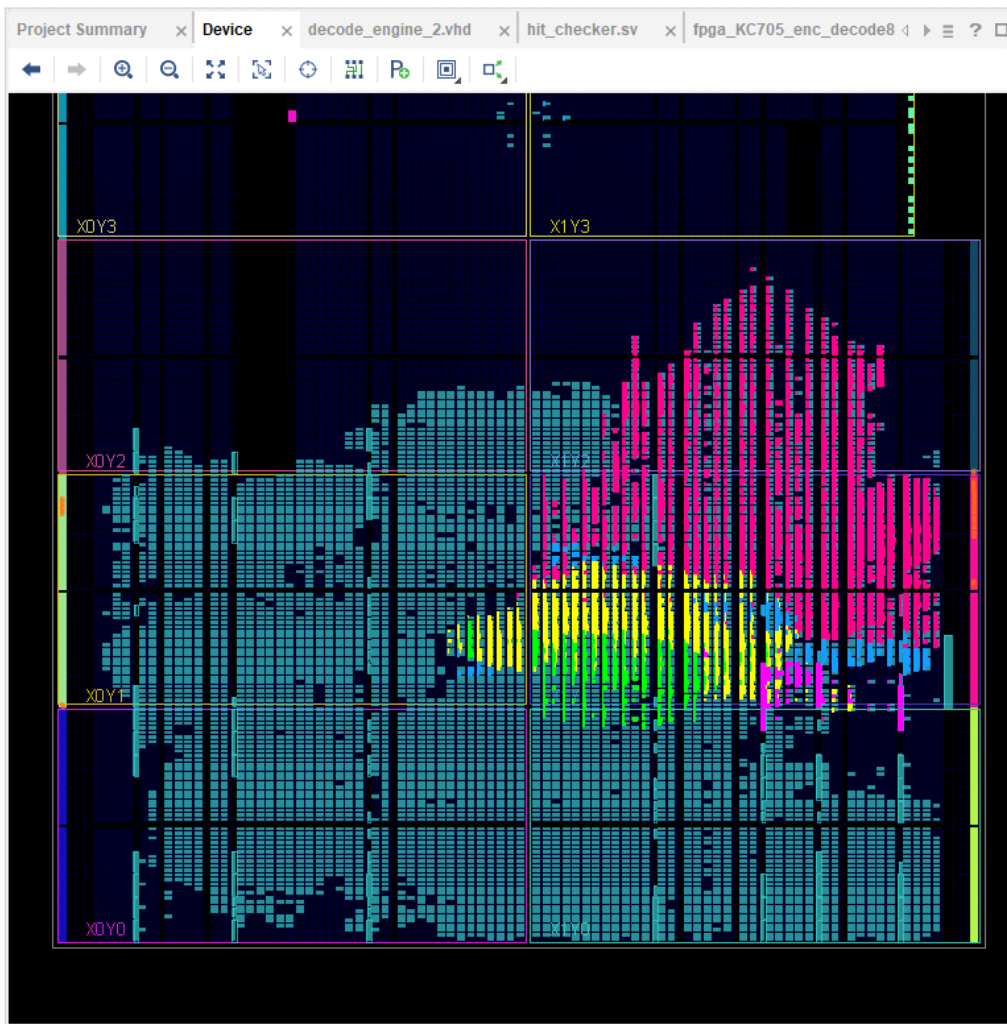
KEY:

- Red - Hitmaker. Generates test data
- Yellow - Decoder channel, One hit decoded every 8 clock cycles.
- Green - FIFO buffer 512x64b (32Kbits). Input stream buffer for 1 decoder. Currently distrib RAM, will move to 1 32K block RAM.
- Purple - Hitdecode ROM. Used by one decoder. Only used once every 8 cycles. Could be shared by 8 decoders but might not be worth the effort.
- Light Blue - Blocks to distribute encoded data to decoders and expected decoded data to a 'checker' block.
- Remaining logic. Other 7 decoders/ROM/FIFOs and 8 'checker' blocks.

Sources **Netlist** **Cell Properties** ? _ □

fpga_KC705_enc_decode8

- > Nets (1494)
- > Leaf Cells (72)
- ▼ **gen_dec[0].u_decode (decode_engine_2__xdcDup__1)**
 - > Nets (4791)
 - > Leaf Cells (4353)
 - > **u_fifo_buf (fifo_512x64b_28)**
 - > **u_hitdecode2 (hitdecode2__xdcDup__1)**
- > **gen_dec[0].u_hit_checker (hit_checker__xdcDup__1)**
- > **gen_dec[1].u_decode (decode_engine_2__xdcDup__2)**
- > **gen_dec[1].u_hit_checker (hit_checker__xdcDup__2)**
- > **gen_dec[2].u_decode (decode_engine_2__xdcDup__3)**
- > **gen_dec[2].u_hit_checker (hit_checker__xdcDup__3)**
- > **gen_dec[3].u_decode (decode_engine_2__xdcDup__4)**
- > **gen_dec[3].u_hit_checker (hit_checker__xdcDup__4)**
- > **gen_dec[4].u_decode (decode_engine_2__xdcDup__5)**
- > **gen_dec[4].u_hit_checker (hit_checker__xdcDup__5)**
- > **gen_dec[5].u_decode (decode_engine_2__xdcDup__6)**
- > **gen_dec[5].u_hit_checker (hit_checker__xdcDup__6)**
- > **gen_dec[6].u_decode (decode_engine_2__xdcDup__7)**
- > **gen_dec[6].u_hit_checker (hit_checker__xdcDup__7)**
- > **gen_dec[7].u_decode (decode_engine_2)**
- > **gen_dec[7].u_hit_checker (hit_checker)**
- > **u_blink (blink)**
- > **u_clkreset (clkreset)**
- > **u_debounce_start (debounce)**
- > **u_debounce_stop (debounce_0)**
- > **u_distrib_exp (distrib_exp)**
- > **u_distrib_stream (distrib_stream)**
- > **u_hitmaker (hitmaker)**
- > **u_set_stream_size (set_stream_size)**



Kintex7 xc7k325 device on KC705 board. Zoom in on lower half of device

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```

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| Tool Version : Vivado v.2018.2 (win64) Build 2258646 Thu Jun 14 20:03:12 MDT 2018
| Date        : Wed Feb 16 11:57:59 2022
| Host       : RATBAG running 64-bit major release (build 9200)
| Command    : report_utilization -file fpga_KC705_enc_decode8_utilization_placed.rpt -pb fpga_KC705_enc_decode8
utilization_placed.pb
| Design     : fpga_KC705_enc_decode8
| Device     : 7k325tffg900-2
| Design State : Fully Placed
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```

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs	48798	0	203800	23.94
LUT as Logic	38959	0	203800	19.12
LUT as Memory	9839	0	64000	15.37
LUT as Distributed RAM	9812	0		
LUT as Shift Register	27	0		
Slice Registers	14561	0	407600	3.57
Register as Flip Flop	14561	0	407600	3.57
Register as Latch	0	0	407600	0.00
F7 Muxes	3031	0	101900	2.97
F8 Muxes	340	0	50950	0.67

3. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	79	0	445	17.75
RAMB36/FIFO*	56	0	445	12.58
RAMB36E1 only	56			
RAMB18	46	0	890	5.17
RAMB18E1 only	46			

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

4. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	840	0.00

6. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	2	0	32	6.25
BUFIO	0	0	40	0.00
MMCME2_ADV	1	0	10	10.00
PLLE2_ADV	0	0	10	0.00
BUFMRCE	0	0	20	0.00
BUFHCE	0	0	168	0.00
BUFR	0	0	40	0.00

10. Instantiated Netlists

Ref Name	Used
fifo_chk_512x32b	36
rom_hitdecode	8
clkgen_200to160	1