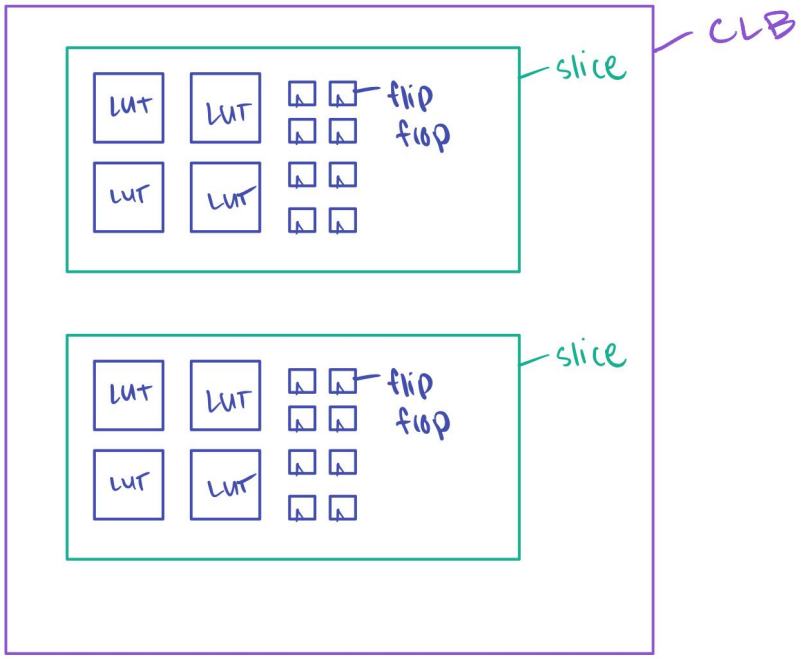
Virtex7 Features

UNIVERSITY of WASHINGTON

Configurable Logic Blocks



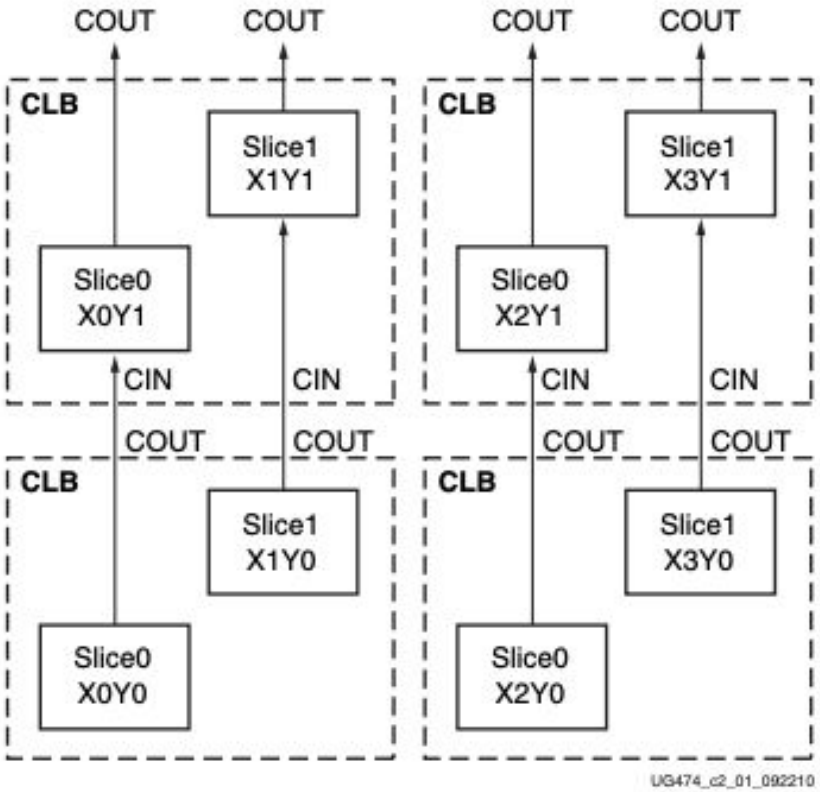


Figure 2-2: **Row and Column Relationship between CLBs and Slice**

Lookup Table

- 6-input, 2-output
  - 6-input with 1 output
  - two 5-input LUTs with separate outputs
- Some can also be
  - Distributed 64-bit RAM
  - 32-bit shift registers
- Dedicated carry logic for quick arithmetic

DSP Slices

- 3600 DSP Slices
- Pre-adder
- 25 x 18 multiplier
  - Two's complement
- 48-bit accumulator
  - Up/Down counter
- 48-bit-wide Pattern Detector
  - Use with logic unit for 96-bit logic functions

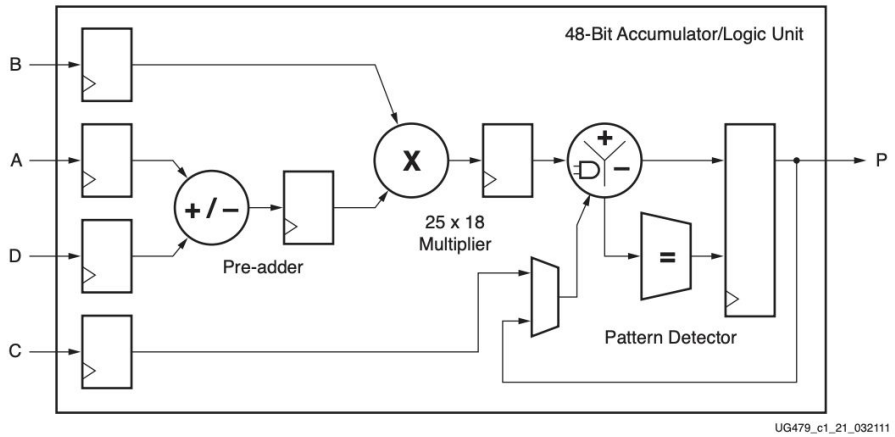
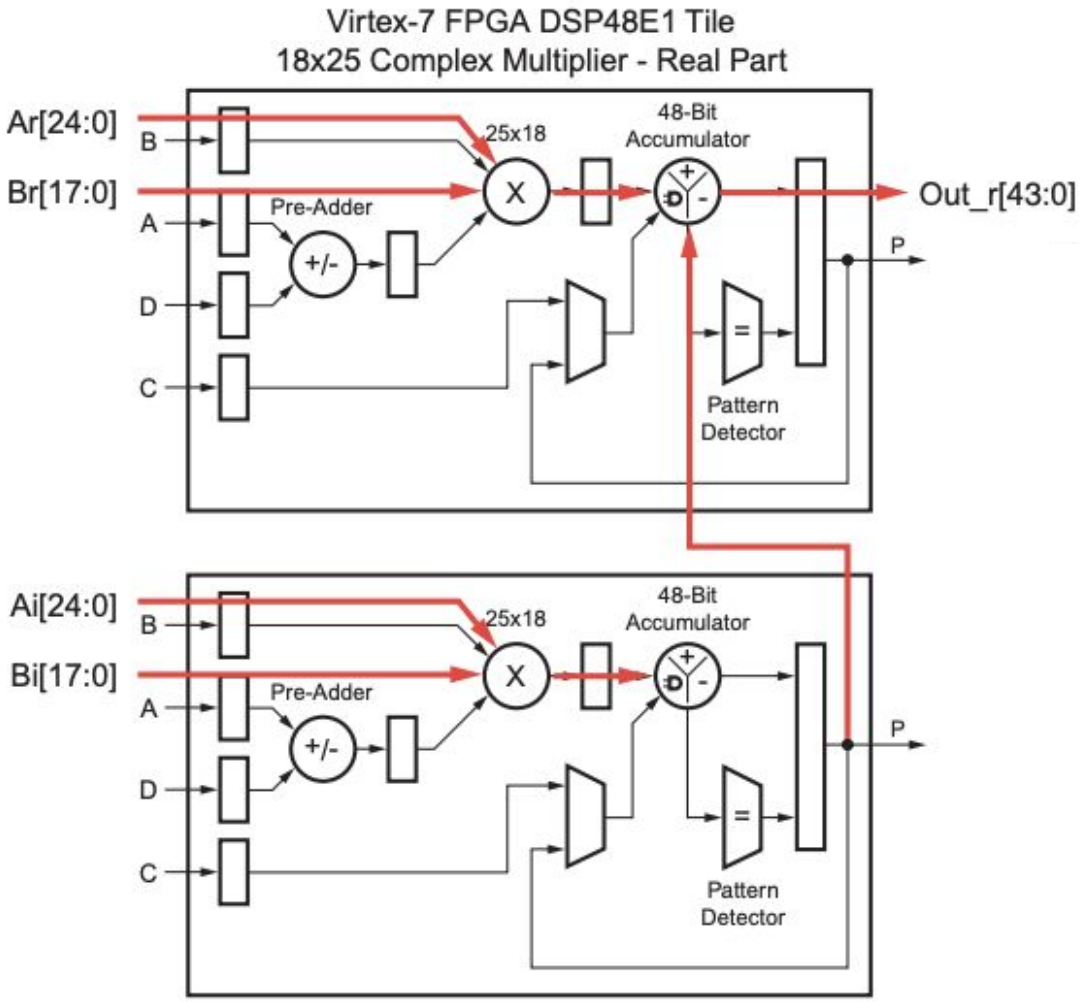


Figure 1-1: **Basic DSP48E1 Slice Functionality**

out_r = (ar*br) - (ai*bi)



Block RAM

- 1,470 per device
- Each stores 36 Kb
  - Can be cascaded for deeper memory (64K x1)
- Synchronous Write & Read
- Dual port
  - Programmable data width
  - Port width up to 72
  - Possible port configurations:
    - 32K x 1, 16K x 2, 8K x 4, … , 512 x 72
  - Simple Dual-Port (SDP)
    - 1 read-only port, 1 write-only
  - True dual-port
    - Write or Read from either or both ports
- FIFO support
- Built in error correction

Summary of features

- # of Logic Cells: 693,120
- Logic Blocks:
  - Slices: 108,300
    - 4 LUTs & 8 flip-flops
  - Some slices can use LUTs as distributed RAM
    - Max Distributed RAM: 10,888
- DSP Slices: 3,600
- Block RAM Blocks (36 Kb):
  - 1,470

Table 1-4: **Virtex-7 FPGA CLB Resources**

Device	Slices[1]	SLICEL	SLICEM	6-input LUTs	Distributed RAM (Kb)	Shift Register (Kb)	Flip-Flops
7V585T	91,050	63,300	27,750	364,200	6,938	3,469	728,400
7V2000T	305,400	219,200	86,200	1,221,600	21,550	10,775	2,443,200
7VX330T	51,000	33,450	17,550	204,000	4,388	2,194	408,000
7VX415T	64,400	38,300	26,100	257,600	6,525	3,263	515,200
7VX485T	75,900	43,200	32,700	303,600	8,175	4,088	607,200
7VX550T	86,600[2]	51,700	34,900	346,400	8,725	4,363	692,800
7VX690T	108,300	64,750	43,550	433,200	10,888	5,444	866,400

7VX690T	Total per device	Columns per device	Number per column
DSP48E1	3,600	18	200
Block RAM	1,470	15	100

- https://www.xilinx.com/support/documentation/data_sheets/ds180_7Series_Overview.pdf
- https://www.xilinx.com/support/documentation/white_papers/wp406-DSP-Design-Productivity.pdf
- https://www.xilinx.com/support/documentation/user_guides/ug479_7Series_DSP48E1.pdf
- https://www.xilinx.com/support/documentation/user_guides/ug473_7Series_Memory_Resources.pdf
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