

FMC216 high pin count FMC DAC

16-channel 16-bit DAC – 312.5 Msps

The FMC216 is a sixteen-channel DAC FMC Daughter Card which is fully compliant with the VITA 57.1-2008 standard. The FMC216 provides sixteen 16-Bit D/A channels with sample rates up to 312.5Msps (2.5Gsps with x8 interpolation). The sample clock can be sourced from an internal clock source (optionally locked to an external reference) or an externally supplied sample clock. A trigger input for customized sampling control is also available. The FMC216 uses an FMC HPC (high-pin count) connector, front panel I/O,

and is conduction cooled capable. The design is based on Texas Instrument's DAC39J84 quad channel 16-bit DAC with JESD204B signaling. The analog output is DC coupled with programmable DC offset correction. The FMC216 allows flexible control on sampling frequency and on board circuitry through serial a communication bus. Furthermore the card is equipped with power supply and temperature monitoring and offers several powerdown modes to switch off unused functions or protect the card from overheating.

FEATURES:

- 16 channel 16-bit 312.5Msps D/A conversion
- Conduction cooled compatible
- ANSI/VITA 57.1-2010 compliant
- Based on DAC39J84
- 1.65V to 3.3V VADJ operation
- Single ended DC coupled outputs
- Programmable DC offset correction
- Flexible clock tree enables
 - External or Internal clock
 - External clock output
 - External or internal reference
- HPC (High-Pin Count) 400 pins connector
- Samtec QSE front panel connector mates with QTE series and EQCD and EQRF cable assemblies with SMA connectors
- MIL-I-46058c conformal coating (optional)

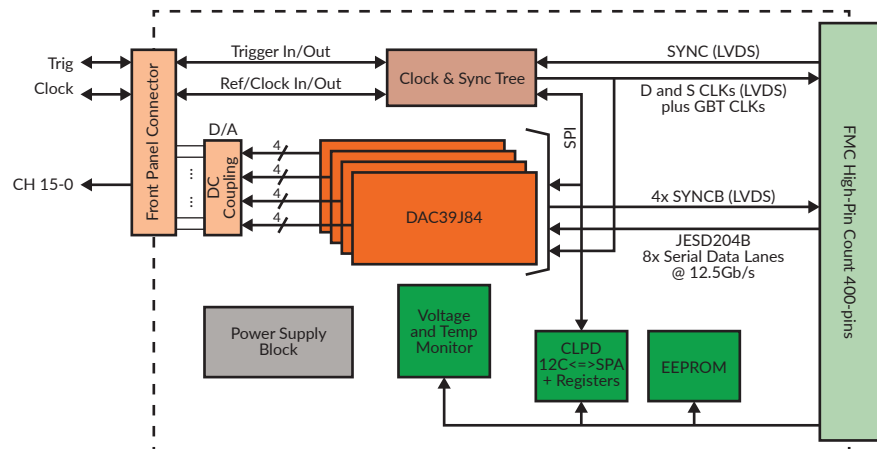
ANSI/VITA 47	Air-cooled		Conduction-cooled	
	EAC4	EAC6	ECC1	ECC4
Operating temperature	0C to +55C	-40C to +70C	0C to +55C	-40C to +85C
Storage temperature	-40C to +85C	-50C to +100C	-40C to +85C	-55C to +105C
Humidity	95%	95%	95%	95%
Operating vibration	5Hz to 100Hz PSD = 0.04g ² /Hz 100 Hz to 1000 Hz PSD = 0.04 gs ² /Hz 1000 Hz to 2000 Hz PSD decreasing at 6 dB/octave	5Hz to 100H PSD = 0.04g ² /Hz 100 Hz to 1000 Hz PSD = 0.04 gs ² /Hz 1000 Hz to 2000 Hz PSD decreasing at 6 dB/octave	5 Hz to 100 Hz PSD increasing at 3 dB/octave 100 Hz to 1000 Hz PSD = 0.1 g ² /Hz 1000 Hz to 2000 Hz PSD decreasing at 6 dB/octave	5 Hz to 100 Hz PSD increasing at 3 dB/octave 100 Hz to 1000 Hz PSD = 0.1 g ² /Hz 1000 Hz to 2000 Hz PSD decreasing at 6 dB/octave
Operating shock	20g, 11 millisecond, half-sine or 20g, 11 millisecond, terminal sawtooth shock pulses in all three axes	20g, 11 millisecond, half-sine or 20g, 11 millisecond, terminal sawtooth shock pulses in all three axes	40g, 11 millisecond shock half-sine or 40g, 11 millisecond, terminal sawtooth shock pulses in all three axes	40g, 11 millisecond shock half-sine or 40g, 11 millisecond, terminal sawtooth shock pulses in all three axes
Operating altitude	-1500 ft to 60,000 ft (with airflow)	-1500 ft to 60,000 ft (with airflow)	-1500 ft to 60,000 ft	-1500 ft to 60,000 ft
Conformal coating	Optional	Optional	Optional	Optional

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Main characteristics

Analog Outputs	
Number of channels	16
Channel resolution	16-bit
Output voltage range	2.0Vpp DC Coupled into 50Ω
Output impedance	50Ω
Analog output bandwidth	DC Coupled - 120 MHz
Digital Sample Rate	312.5 MS/sec maximum data rate for each DAC, but this is limited by JESD204B channel bandwidth width. With 8x interpolation, DAC output rate can be as high as 2500 MS/Sec.
External Clock/Reference Input	
Input Level	0.35Vpp to 3.1Vpp (-5 to +13.5dBm)
Input impedance	50Ω (AC coupled)
Input range	800mVpp typical
External Clock/Reference Output	
Output Level	650 mVpp into 50Ω typical. at 100MHz
External Trigger Input	
Format	LVTTL/LVCMOS Logic '0' --> max 0.8V / Logic '1' --> min 2.0V
Frequency range	Up to 125 MHz
External Trigger Output	
Output Level	3.3V CMOS 1.65V into 50Ω typical
DAC Input	
Data width	JESD204B 8 pairs
Data Format	Offset binary or 2's complement (default)

Block diagram



Specifications

Application

- High channel count applications
- Software defined radio (SDR)
- RADAR/SONAR
- Wireless communication receivers
- Medical equipment
- Aerospace and test measurement Instruments

Support

- User manual
- Performance guide
- Reference Firmware design (VHDL) with Stellar IP framework and AXI bus support
- Reference Xilinx Vivado project for multiple FPGA boards

AS9100 Certified

Ordering information

Talk to us about your algorithmic requirements, Abaco Systems is a full-service firmware and software development house. We are a specialist at high performance FFT and Video Processing. Check with us, we may have IP Cores that meet requirements for your application, right off the shelf.



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