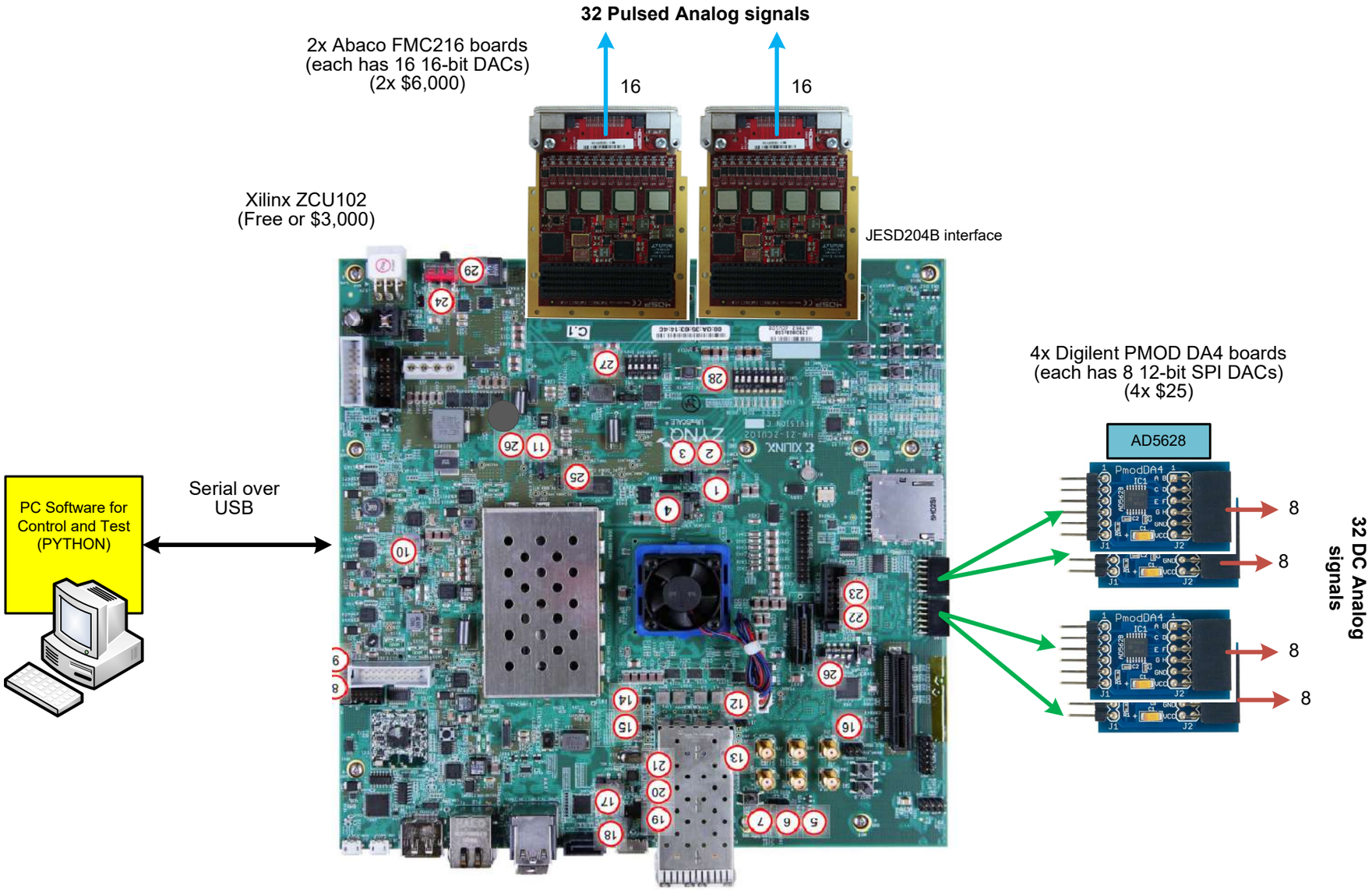
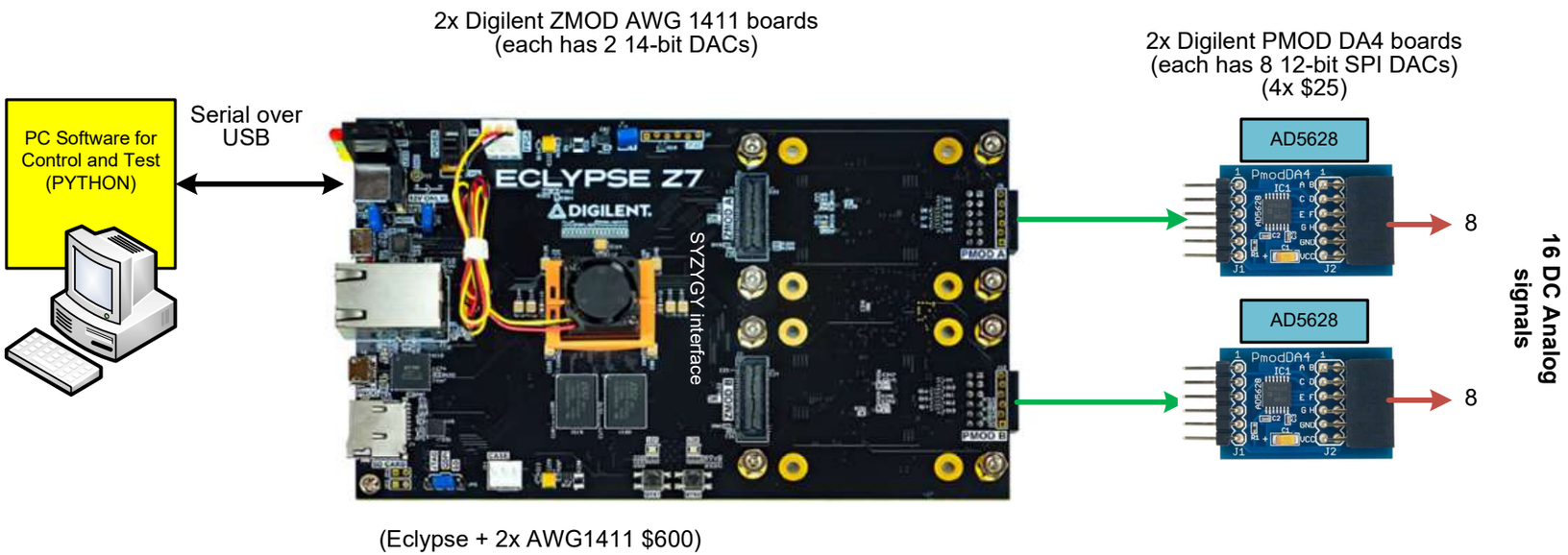
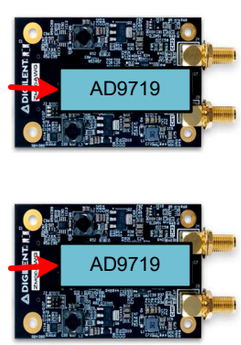
Xilinx ZCU102 + 2x Abaco FMC216 + 4x PMOD DA4
32 DC 12-bit, 32 Pulse 16-bit analog

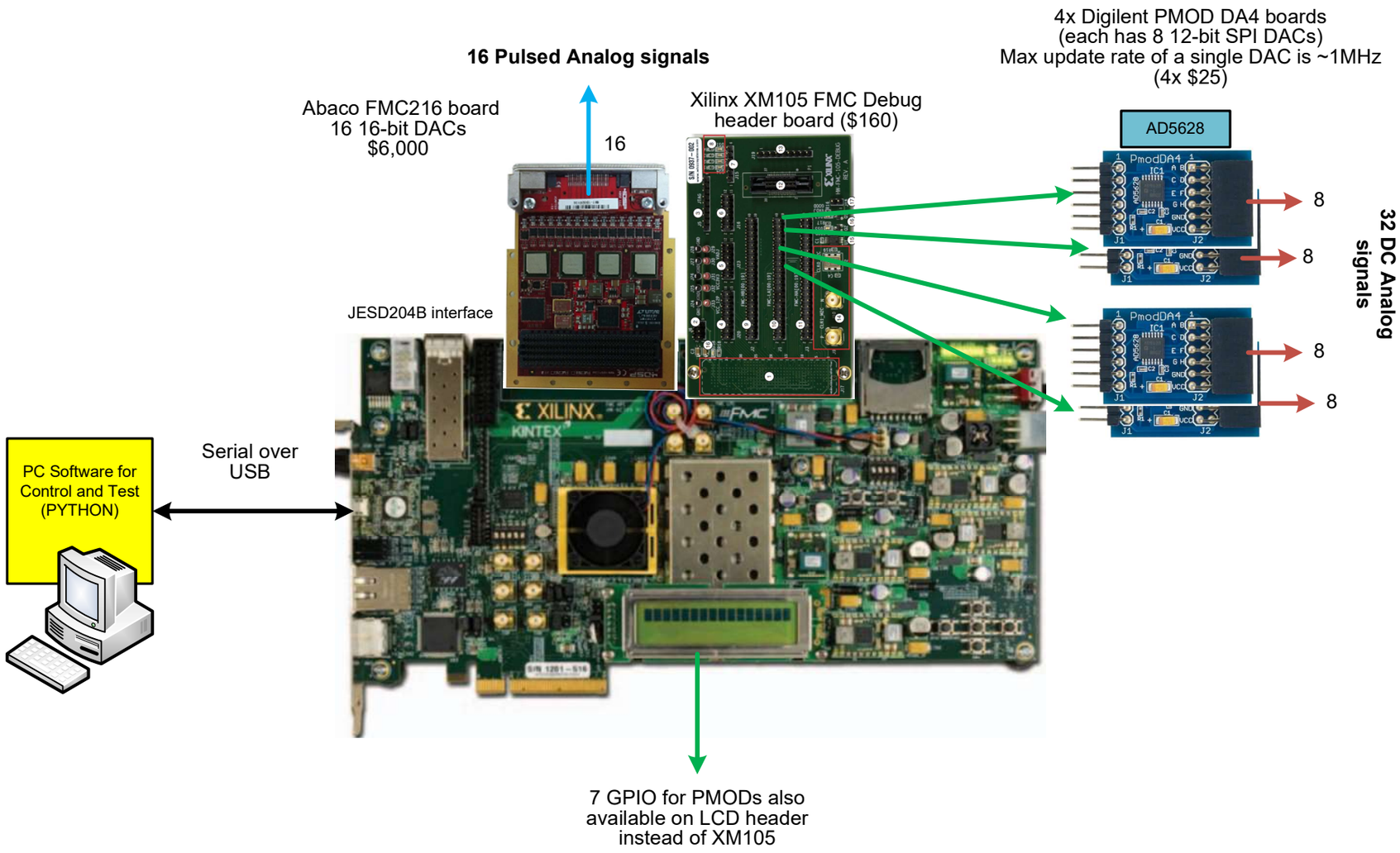


Eclypse Z7 + 2x AWG1411 + 2x PMOD DA4
16 DC 12-bit, (Optional 4 Pulse 14-bit analog)
(Prototype System)

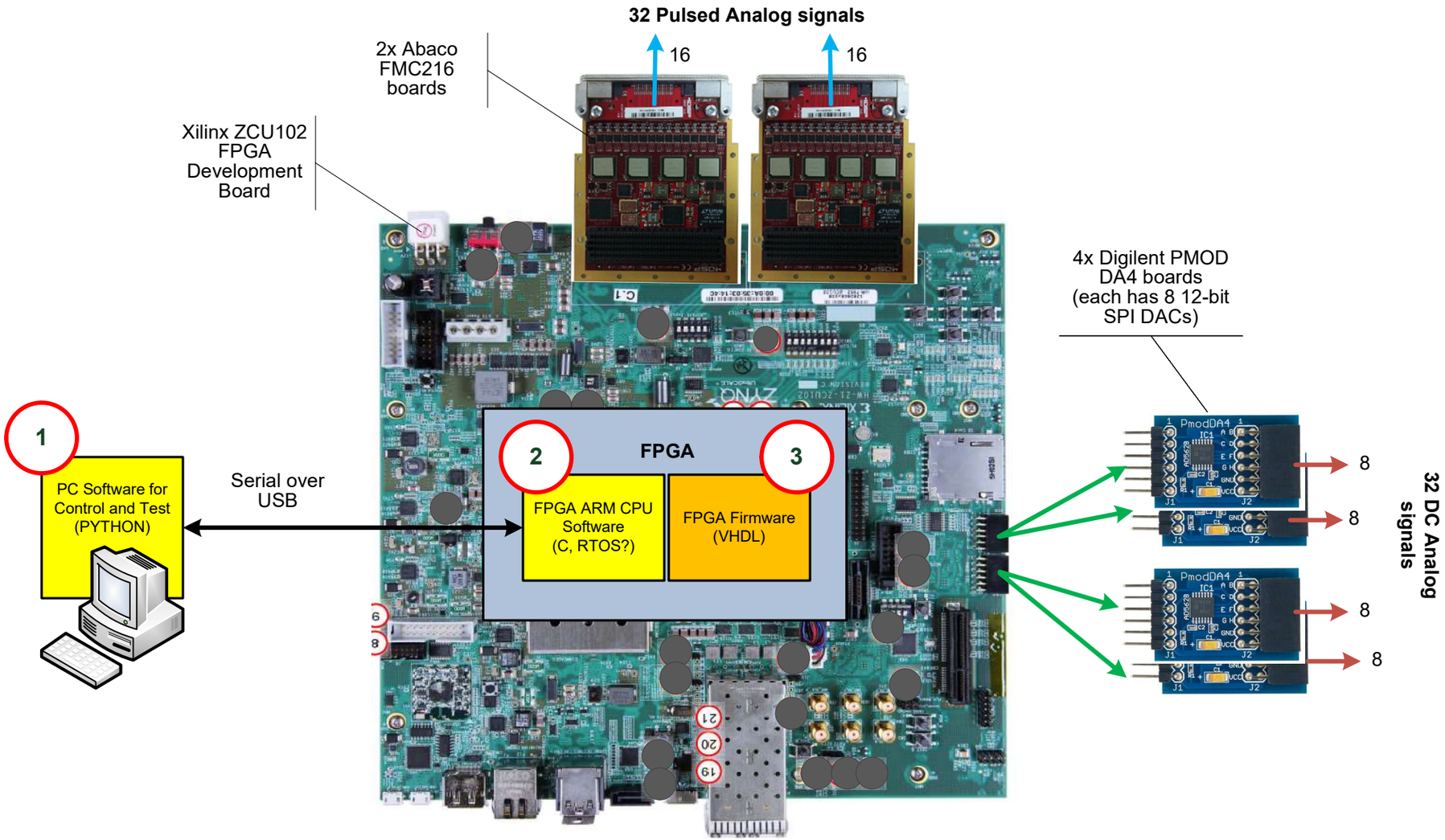




(Backup) Xilinx KC705 + 1x Abaco FMC216 + 4x PMOD DA4
32 DC 12-bit, 16 Pulse 16-bit analog



Laser Control Project Components



1. PC Software for Control and Test (PYTHON, Tk for GUI) Communicates with FPGA ARM CPU over 115,200 bps serial link.
2. FPGA ARM CPU (PS) Software (C, RTOS?) Developed in Vitis environment. Controls and monitors JESD blocks, Interprets commands from PC interface. Programs PL RAM tables etc.
3. FPGA Firmware. (VHDL/SystemVerilog) Custom logic connected to PS through AXI-lite interface. Contains DC inteface channels, Pulse generators and JESD IP blocks.

Things you need to know

Project goal is to construct a pulse generator for controlling quantum computer elements

1. Xilinx (AMD) UltraScale+ FPGA data sheets. ZCU102 Development board user manual.

2. VHDL.

3. Vivado 2022.1 and Modelsim. Create project and bitfile to blink LED. Simulate then make bitfile to test.

4. Version Control with Github. Inspect existing code. Run simulations.

5. Initial use of a serial to parallel (cpuint) block in the FPGA to receive read/write commands.

6. Replacement by UART in hard CPU in the ZCU102 board.

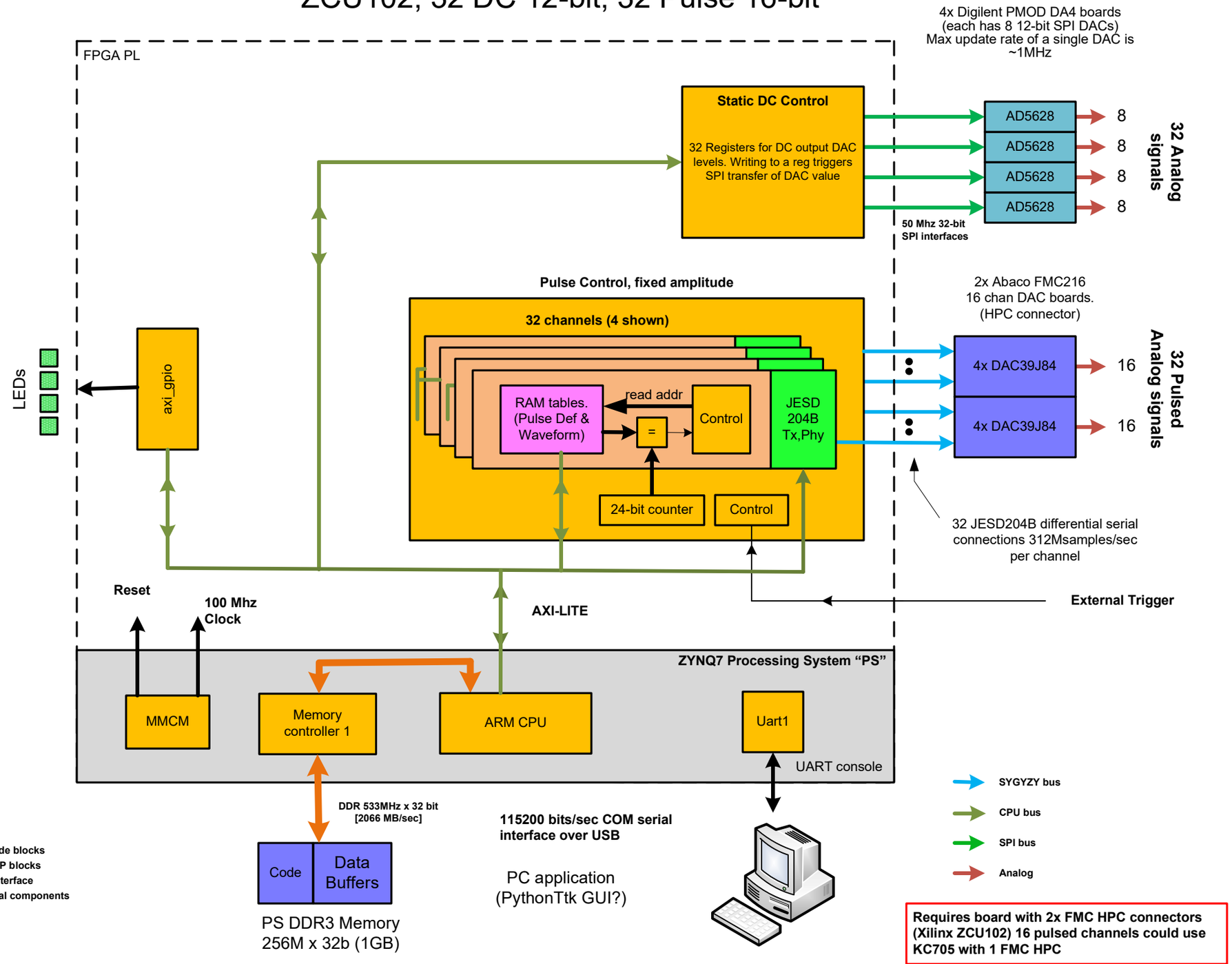
7. Use of Python/Tkinter to create a user interface to control the system.

8. The use of the JESD serial interface standard to transfer data, at high speed, to 32 16-bit DACs. 64 signals replace 512 parallel data lines. JESD documents, Abaco FMC216 manual

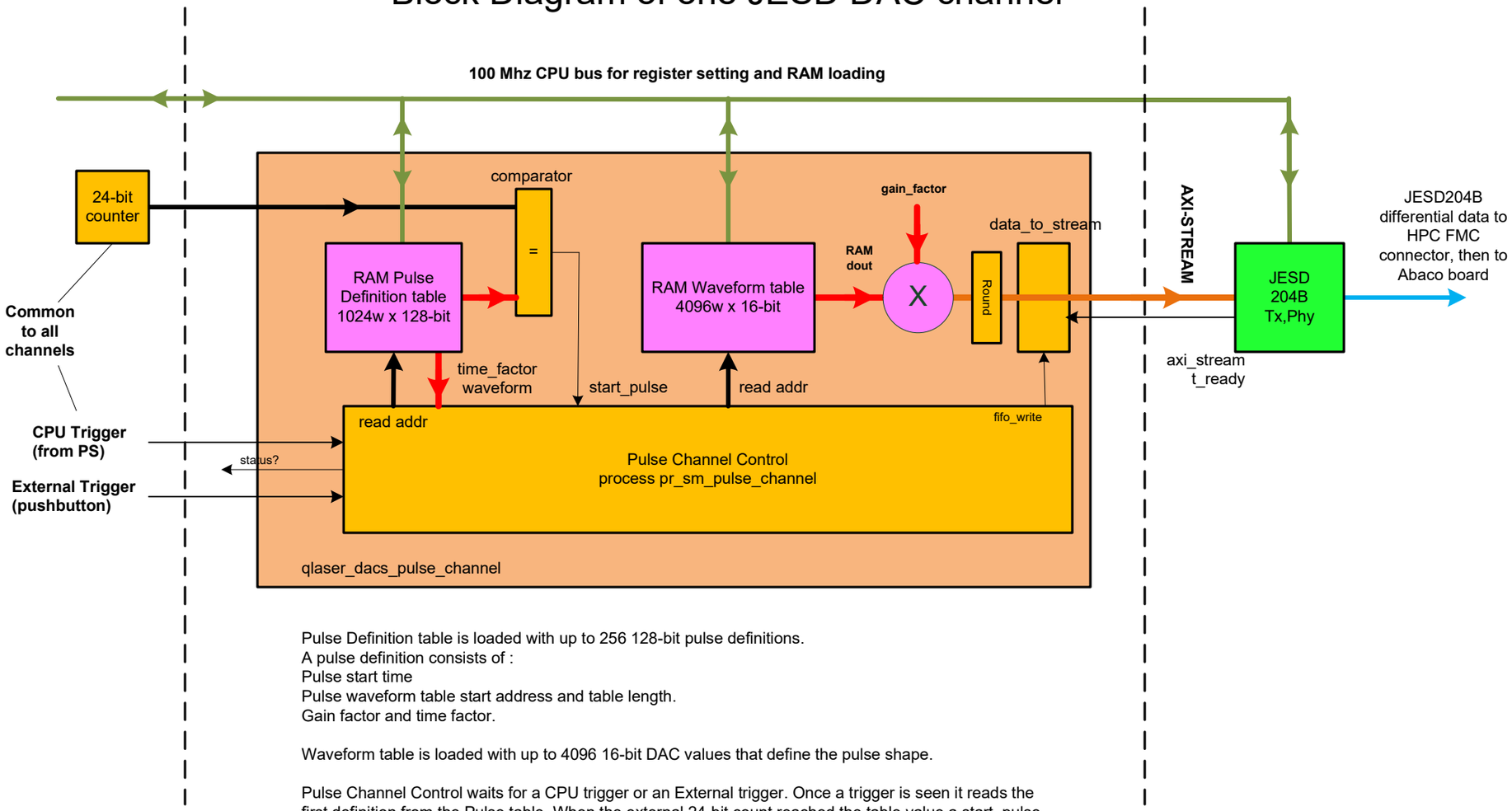
9. The use of the I2C bus to program DACs and Clock generators on FMC216 boards. Embedded C programming. Xilinx IP manual, TRM. Datasheets for DAC and Clock generator.

10. The use of software running on the FPGA PS CPU to perform initial setup and interpret higher level commands instead of sending detailed register read/write commands serially from the PC.

Laser Control FPGA Block Diagram
ZCU102, 32 DC 12-bit, 32 Pulse 16-bit



Laser Control FPGA
Block Diagram of one JESD DAC channel



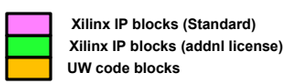
Pulse Definition table is loaded with up to 256 128-bit pulse definitions.
A pulse definition consists of :
Pulse start time
Pulse waveform table start address and table length.
Gain factor and time factor.

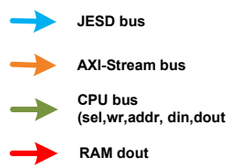
Waveform table is loaded with up to 4096 16-bit DAC values that define the pulse shape.

Pulse Channel Control waits for a CPU trigger or an External trigger. Once a trigger is seen it reads the first definition from the Pulse table. When the external 24-bit count reached the table value a start_pulse is generated and the controller then reads the requested waveform table using the start address and time factor from the definition table. The waveform table output is scaled by the gain factor and converted into an AXI stream and sent to the JESD Transmit block.

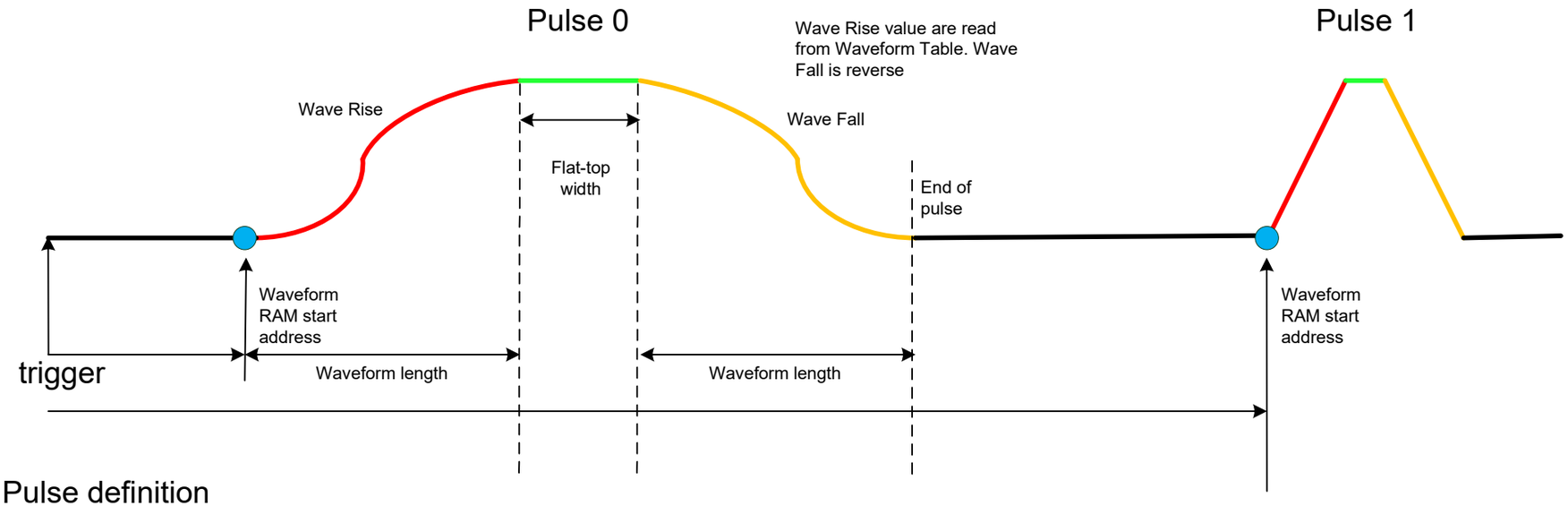
The read address of the Pulse definition table is incremented and the Controller waits for the next start_pulse to the output the next pulse.

The data_to_stream block uses a FIFO to buffer the waveform data and supplies AXI-stream data to the JESD block. The JESD block could apply ‘backpressure’ using the axi_s bus tready signal to pause the data.

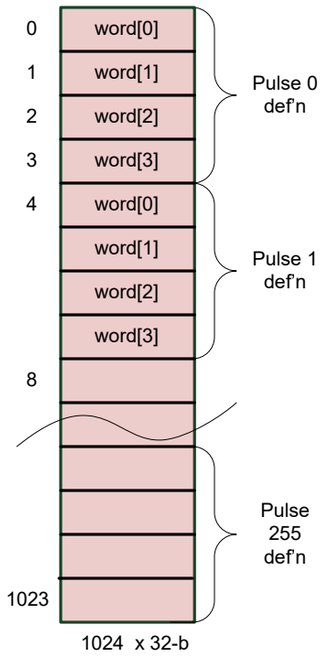




Pulse Definition for JESD DAC channel



Pulse definition RAM



Fields of a pulse definition table entry

Entry word 0 :	doutb[23: 0]	: pulse start time
Entry word 1 :	doutb[11: 0]	: waveform start address [11:0]
	doutb[25:16]	: waveform length [9:0]
Entry word 2 :	doutb[15: 0]	: gain scale factor
	doutb[31:16]	: address scale factor
Entry word 3 :	doutb[16: 0]	: pulse flat top length in clock cycles