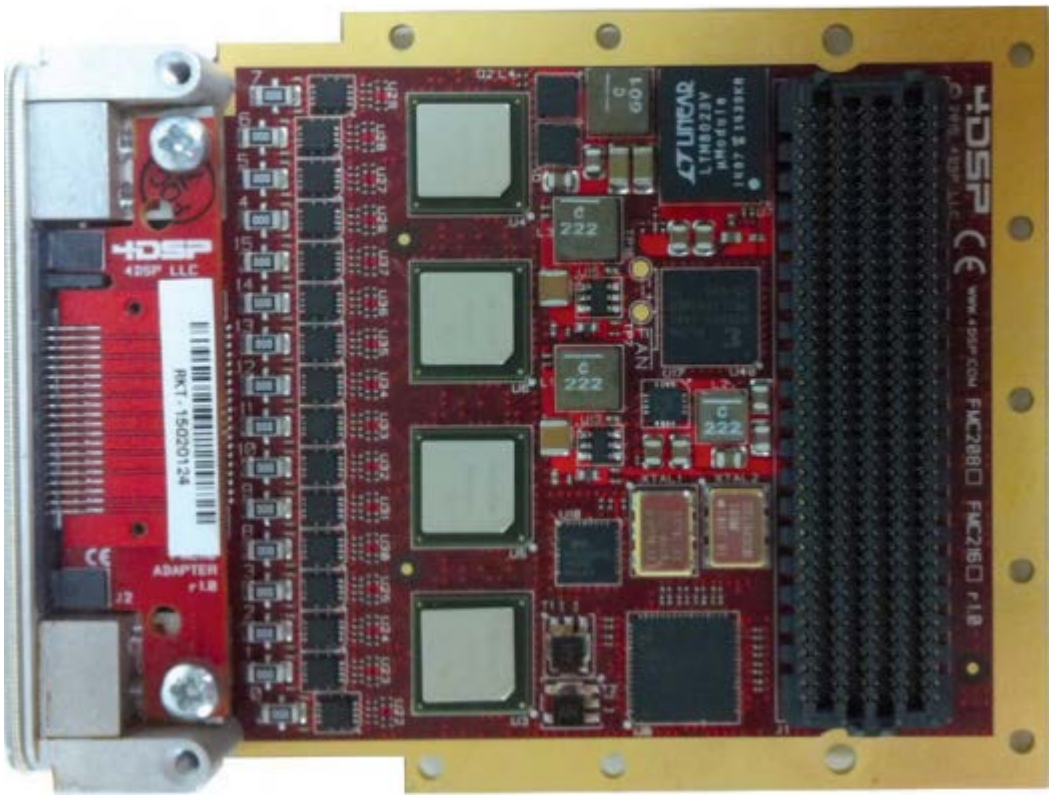
FMC216

User Manual



Abaco Systems, USA.

Support Portal

Revision History

Date	Revision	Revision
2016-04-06	Initial release	r1.0
2016-04-12	Corrected errors and added signals to Table 14 Clarified general description in section 2	r1.1

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1 Acronyms and related documents

1.1 Acronyms

DDR	Double Data Rate
DDS	Direct Digital Synthesis
DSP	Digital Signal Processing
EEPROM	Electrically Erasable Programmable ROM
FBGA	Fineline Ball Grid Array
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
JTAG	Join Test Action Group
LDO	Low Dropout
LED	Light Emitting Diode
LSB	Least Significant Bit(s)
LVDS	Low Voltage Differential Signaling
LVPECL	Low Voltage Positive Emitter Coupled Logic
LVTTL	Low Voltage Transistor Logic level
MGT	Multi-Gigabit Transceiver
MSB	Most Significant Bit(s)
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PLL	Phase Locked Loop
PMC	PCI Mezzanine Card
PSRR	Power Supply Rejection Ratio
QDR	Quadruple Data rate
SDRAM	Synchronous Dynamic Random Access memory
SRAM	Synchronous Random Access memory
TTL	Transistor Logic level
XMC	PCIe Mezzanine card

Table 1: Glossary

1.2 Related Documents

- FPGA Mezzanine Card (FMC) standard ANSI/VITA 57.1-2010
- Datasheet DAC39J84, TI - Digital to Analog Converter
- Datasheet LMK04828, TI - PLL and Clock Generator
- Datasheet AD7291BCPZ Analog Devices 8-Ch I^2C SAR ADC
- JESD204B Specification, JEDEC Standard No. 204B.01

2 General Description

The FMC216 is a 16-channel Digital-to-Analog FMC daughter card. The board provides 16 analog output channels at a 16-bit resolution and a maximum output rate of 2.8 GSPS with a data rate of 175MSPS interpolated by 16, or an output rate of 625 MSPS with a maximum data rate of 312.5MSPS interpolated by 2. (The FMC216 must be operated with a minimum interpolation of 2) Clocking can be from an internal clock source (optionally locked to an external reference) or an externally supplied sample clock. Additionally, the FMC216 includes a trigger input and trigger output to customize sampling control. The FMC216 daughter card is mechanically and electrically compliant to FMC standard (ANSI/VITA 57.1-2010).

The FMC216 has been designed with the ability to stack directly beneath a Abaco FMC116. This Abaco FMC stacked technology enables to have 16 outputs and 16 inputs from a single FMC HPC site; for stacked configurations consult Abaco sales and support for more information. The factory default configuration is the FMC module directly connected directly to an HPC mezzanine connector with no stacking connector included.

The FMC216 is based on the DAC39J84, quad channel 16-bit 2.8Gsps DAC from Texas Instruments. The analog signal outputs are DC coupled and connected to the front panel Samtec connector.

The FMC216 allows flexible control on sampling frequency through an I^2C serial communication channel. Furthermore, the card is equipped with power supply and temperature monitoring and offers several power-down modes to switch off unused functions.

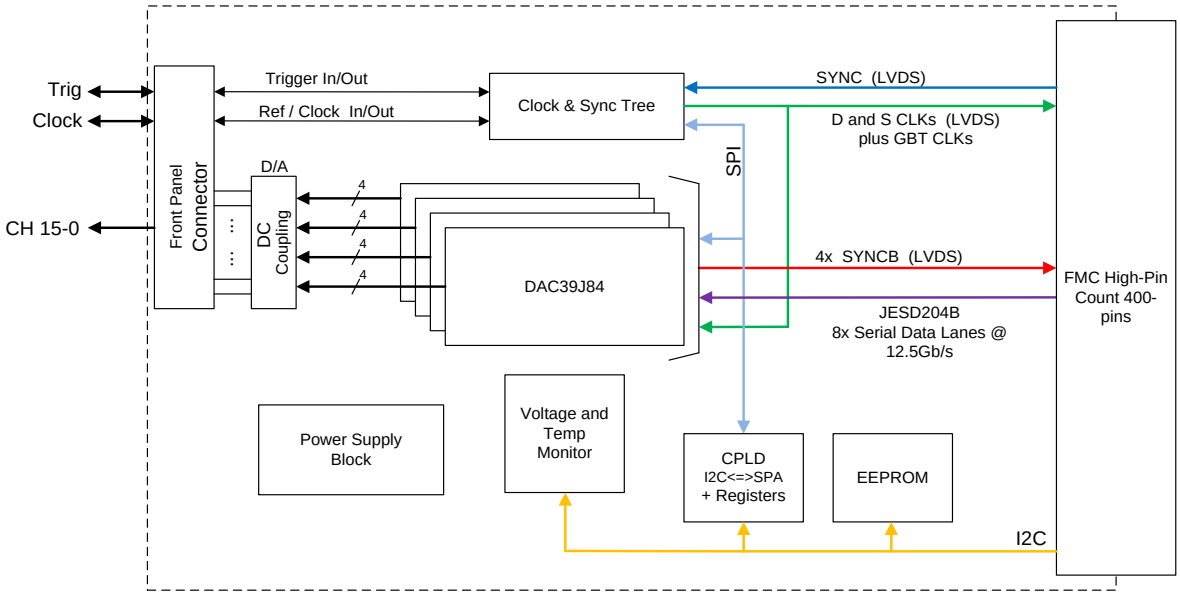


Figure 1: FMC216 Block Diagram

A reduced version of the FMC216, the FMC208 is available and offers 8 DAC channels instead of 16.

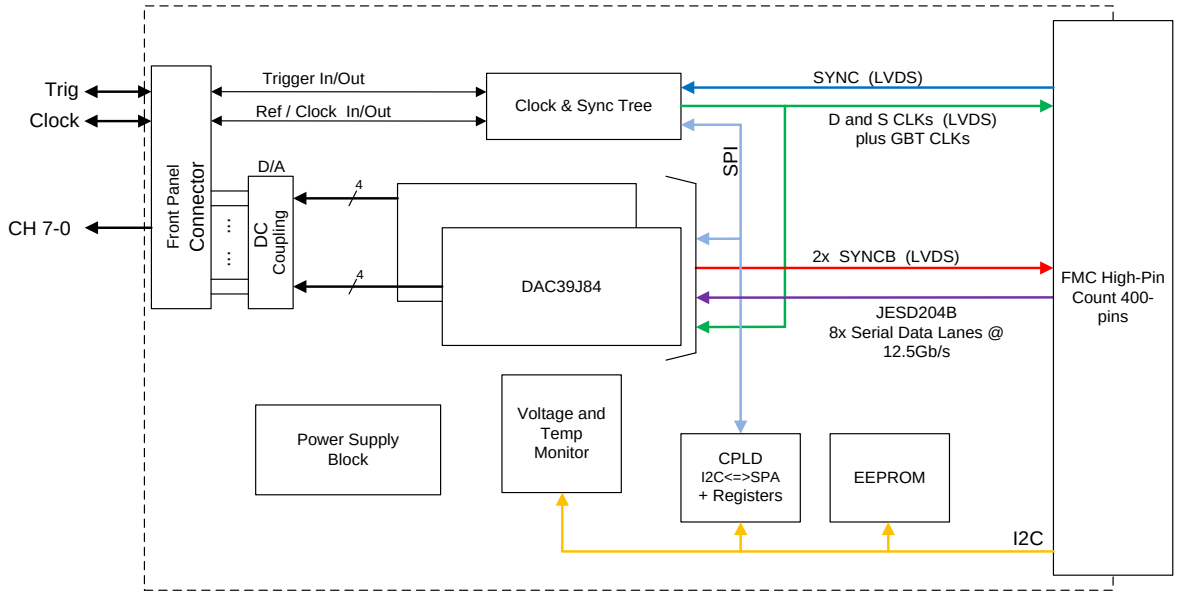


Figure 2: FMC208 Block Diagram

2.1 Installation and Handling Instructions

- Prevent electrostatic discharges by observing ESD precautions when handling the card.
- Do not flex the card and do not exceed the maximum torque specification on the coax connectors.
- The FMC216 daughter card must be installed on a carrier card compliant to the FMC standard.
- The FMC carrier card must support the high-pin count connector (400-pins)
- The carrier card can support VADJ/VIO_B voltage range of 1.65V to 3.3V, but typically VADJ will be 1.8V or 2.5V for LVDS operation.

3 Design

3.1 Physical Specifications

3.1.1 Board Dimensions

The FMC216 card complies with the FMC standard known as ANSI/VITA 57.1. The card is a single width conduction cooled mezzanine module (with region 1 and front panel I/O). The front connector allows access to 20 I/O signals. The stacking height is 10mm; the maximum component height on the bottom layer is 1.3mm.

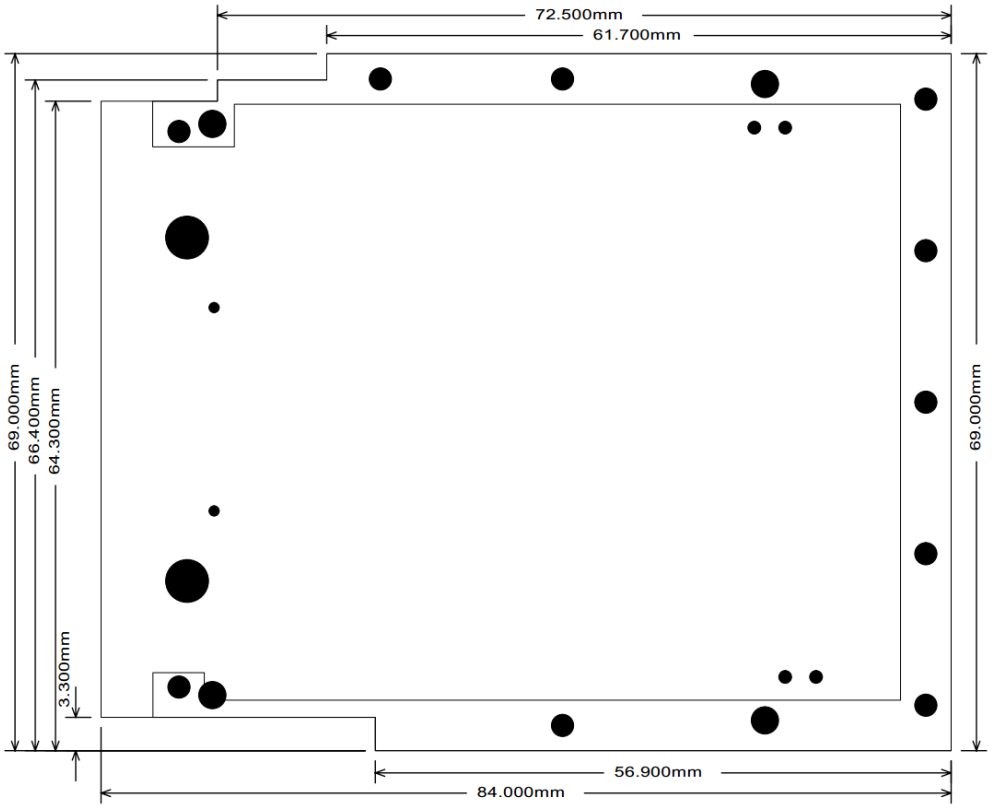
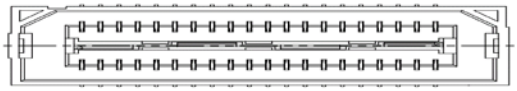


Figure 3: FMC216 dimensions

3.1.2 Front Analog I/O Connector

The front panel of the FMC216 contains a SAMTEC (QSE-020-01-F-D-A-K) socket for all analog signals. The socket has provision for up to 20 shielded I/O signals. The mating connector houses individual SMA tipped coaxial cables for each DAC channel, clock, and trigger signal.



Side 1		Cable		Side 2		Cable
Pin	**Signal**	**Label**		**Pin**	**Signal**	**Label**
1	CH 08	CH09		2	GND	
3	GND			4	CH 09	CH10
5	CH 10	CH11		6	GND	
7	GND			8	CH 11	CH12
9	CH 04	CH05		10	GND	
11	GND			12	CH 05	CH06
13	CH 06	CH07		14	GND	
15	GND			16	CH 07	CH08
17	CH 00	CH01		18	GND	
19	GND			20	CH 01	CH02
21	CH 02	CH03		22	GND	
23	GND			24	CH 03	CH04
25	CH 12*	CH13		26	GND	
27	GND			28	CH 13*	CH14
29	CH 14*	CH15		30	GND	
31	GND			32	CH 15*	CH16
33	GND			34	GND	
35	CLOCK IN	CI		36	GND	
37	GND			38	TRIGGER IN	TI
39	CLOCK OUT	CO		40	TRIGGER OUT	TO

Table 2: Analog I/O Connector Pinout

A small adapter PCB is mounted on the FMC216 as shown in **Figure 4** below. This functions as a right angle adapter through the bezel allowing connection of an external cable such as the SMA breakout cable shown in **Figure 5** below.

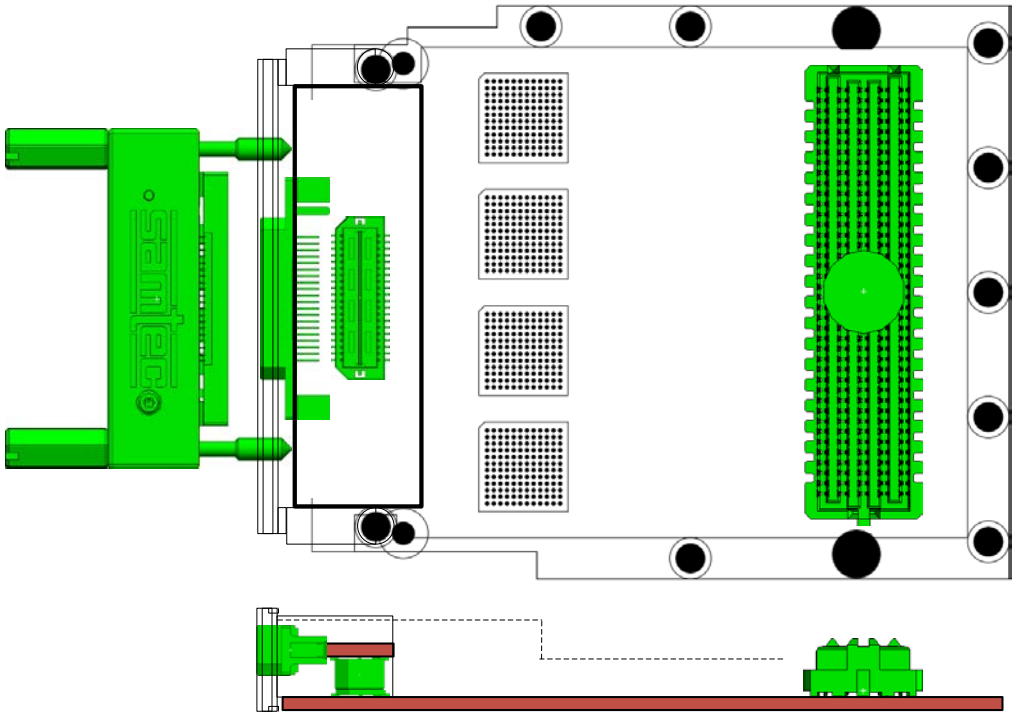


Figure 4: FMC216 with Adapter PCB

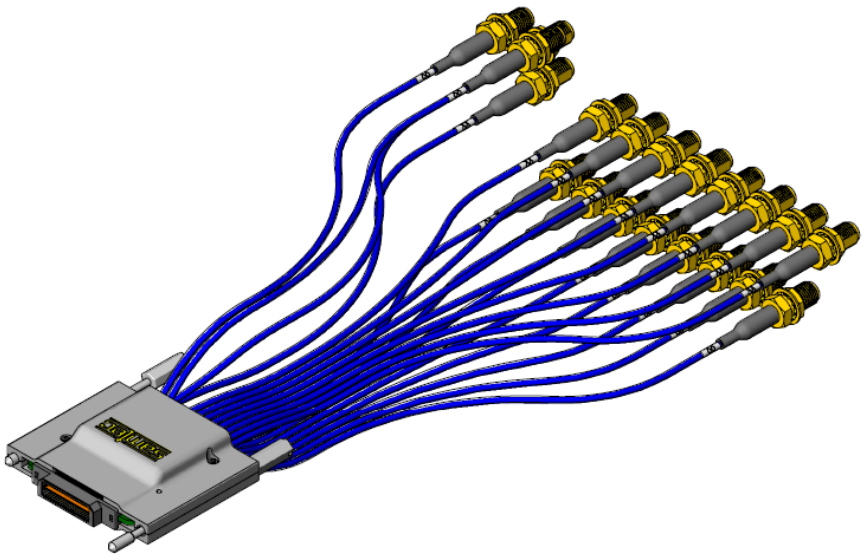


Figure 5: SMA Breakout Cable

3.2 Electrical Specifications

Each DAC device use JESD204B subclass 1 coded differential pairs connected to the GBT pins on the FMC connector to transfer sample data. There are normally 0.5 lanes (8 lanes available for 16 DAC channels) available per DAC channel. Control signals operate in LVCMOS/LVDS mode. A VADJ range of 1.65V to 3.3V is supported. The voltage on the VIO_B pins will follow the voltage on VADJ. CLK pins are required to be LVDS by the FMC standard. CLK0 and CLK1 are not used, but are passed thru for stacked operation. CLK2 is connected to a spare DCLK output of the clock tree. CLK3 is connected to a spare SCLK output of the clock tree.

3.2.1 EEPROM

The FMC216 card carries a 2kbit EEPROM (M24C02-WDW) which is accessible from the carrier card through the I^2C bus. The EEPROM is powered by 3P3VAUX. The standby current is only 0.01µA when SCL and SDA are kept at 3P3VAUX level. On-board pull-up resistors allow these signals to be left floating. The EEPROM is read-only and contains IPMI information of the FMC as defined in ANSI/VITA 57.1-2010.

3.2.2 FMC Mezzanine Connector

Both the recommendations from AV57.1 **Table 3**, and the potential for use in a stacked situation have been taken into account. The high-pin count connector is required for operation of the FMC216.

- The JESD204B DAC data pairs are mapped to DP[0..7]_C2M_[P/N].
- The reference clocks for the gigabit lanes are mapped to GBTCLK[0..1]_M2C_[P/N].
- The reference clock for the FPGA logic is mapped to CLK2_BIDIR_[P/N].
- The SYSREF clock for the FPGA logic is mapped to CLK3_BIDIR_[P/N].
- Other signals are mapped to LA bank starting at index 0.

	# LVDS Clock Pairs	# LVDS Data Pairs	# GBT Clock Pairs	# GBT Data Pairs C2M	# GBT Data Pairs M2C
CLK0 – **N/C**					
CLK1 – **N/C**					
CLK2 **– LVDS Ref CLOCK**	1				
CLK3 **– LVDS SYSREF**	1				
GBTCLK0 – **REF CLK**			1		
GBTCLK1 – **REF CLK**			1		
Trigger in		1			
Trigger Out (single ended)		.5			
Sync in		1			
DAC0 (FMC216 or FMC208)					
JESD204B lanes				FMC216: 2 FMC208: 4	
SYNCB[P/N]		1			
DAC1					

(FMC216 or FMC208)						
	JESD204B lanes				FMC216: 2 FMC208: 4	
	SYNCB[P/N]		1			
DAC2 **(FMC216 only)**						
	JESD204B lanes				FMC216: 2 FMC208: N/A	
	SYNCB[P/N]		1			
DAC3 **(FMC216 only)**						
	JESD204B lanes				FMC216: 2 FMC208: N/A	
	SYNCB[P/N]		1			
CPLD Auxiliary Control I/O: (Configured as 4 SE nets)			2			
Clock Tree SYNC (single ended)			.5			
# Total Pairs		2	9	2	8*	0

Table 3: LPC/HPC Signal Utilization

*Depending on the number of available GBT pairs on the carrier card (4 or 8), the FMC216 DACs will have 1 or 2 GBT pairs per DAC device connected on the FMC216 (4 DACs). For the FMC208 (2 DACs), 2 or 4 GPT pairs will be connected per DAC.

3.2.3 FMC Carrier Connector

All FMC pins not used by the FMC216 will be passed through to the carrier connector, for example, for stacking a FMC116, to prevent I^2C bus conflicts, the global address signals GA0 and GA1 can be read by the CPLD thru the I^2C bus and a translated version can be output to the carrier connector from the CPLD. Detailed pin descriptions and be found in section 10.1 Appendix A. The routing of the GBTCLK signals are shown in **Figure 6**.

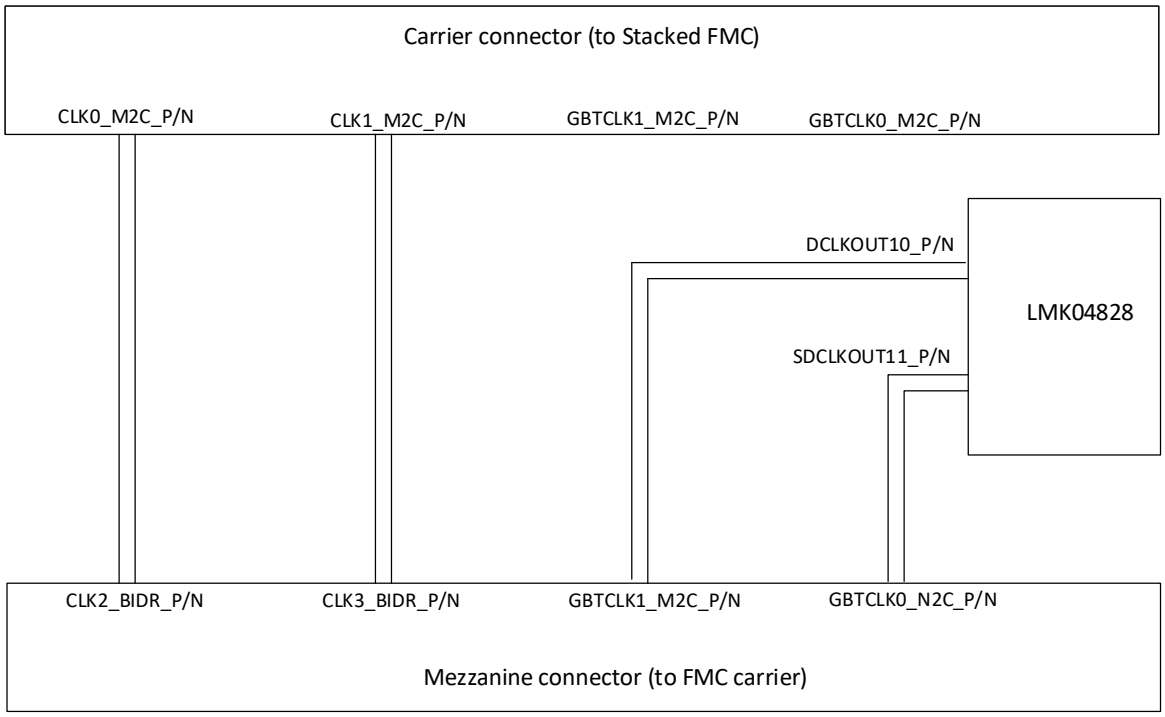


Figure 6: GBTCLK[0/1]_M2C_[P/N] Connections

3.2.4 JTAG Chain

The CPLD device is included in the JTAG chain accessible from the FMC connection in its default configuration. The user should **NOT** reprogram or erase the CPLD.

In a stacked environment the TDI pin will be decoupled from the TDO pin by the PRST_M2C_L signal coming from the bottom connector. TRST#, TCK, TMS, TDI and TDO are directly connected between top to bottom connector on the FMC216.

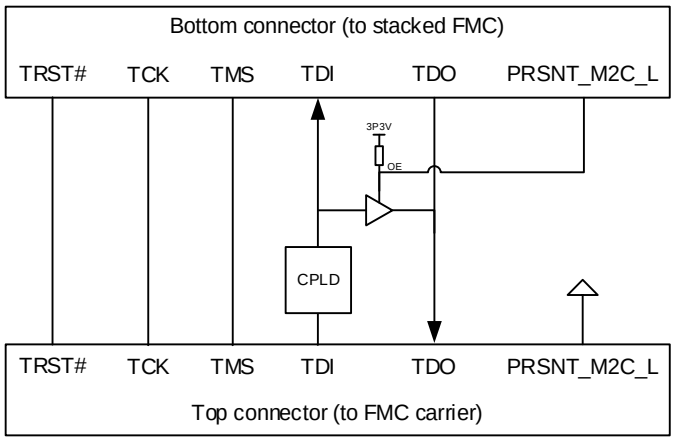


Figure 7: JTAG Connection

3.3 Main Characteristics

Analog Outputs at 258MSPS 8 X Interpolation	
Number of channels	16 (CH0-CH15 for FMC216);

	8 (CH0-CH7 for FMC208);
Channel resolution	16-bit
Output voltage range	2.0Vpp DC Coupled into 50Ω (+10dBm)
Output impedance	50Ω
Crosstalk	-50dBFS typical at 30 MHz -40dBFS typical at 50MHz -30dBFS typical at 100MHz
Analog output bandwidth	DC Coupled -1.0dB typical at 80MHz -1.7dB typical at 103MHz (.8 Nyquist @ 258MSPS) -3.0dB typical at 120MHz
DAC Output Sample Rate	625 MSPS for a maximum input rate of 312.5MSPS interpolate = 2 1250 MSPS for a maximum input rate of 312.5MSPS interpolate = 4 2.5 GSPS for a maximum input rate of 312.5MSPS interpolate = 8 2.8 GSPS for a maximum input rate of 175MSPS interpolate = 16 **Note**: The FMC216 requires a minimum interpolation of 2
SFDR	-50dBFS typical
Harmonics	F2 -50dBFS typical F3 -50dBFS typical F4 -70dBFS typical F5 -70dBFS typical
DAC Input	
Data width	JESD204B 4 or 8-pairs
Data Format	Offset binary or 2's complement(default)
Sampling Frequency Range	up to 312.5Msps. This may be further limited by JESD204B channel bandwidth.
External Clock/Reference Input	
Input level	External Reference 0.35Vpp to 3.1Vpp (-5 to +13.5dBm) +10dBm Typical, It is recommended to operate close to the maximum input amplitude
Input impedance	50Ω (AC coupled)
Frequency range	10 to 700MHz (transformer limited)
External Clock/Reference Output	
Output level	650mVp-p into 50 ohms typical at 100MHz 500mVp-p into 50ohms typical at 625MHz
External Trigger Input	
Format	LVTLL/LVCMOS

	Default Threshold Voltage 1.25Vdc Logic '0' → max 0.8V / Logic '1' → min 2.0V
Frequency range	Up to 125 MHz LVCMOS
External Trigger Output	
Output level	3.3V CMOS with 50Ω source termination. 1.65V into 50Ω typical. Toggle rate 250MHz typical, with VAD >= 1.8Vdc Toggle rate 160MHz typical, with VADJ < 1.8Vdc

Table 4 : FMC216 daughter card main characteristics

3.4 Analog Channels

3.4.1 DC Coupling

The FMC216 utilizes DC coupled outputs based on the AD8000 current feedback operational amplifier for the current to voltage conversion.

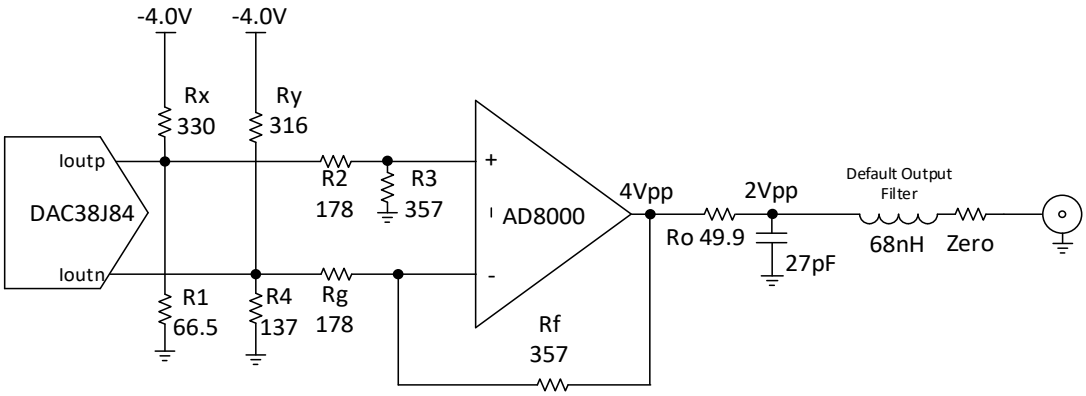


Figure 8: DC coupled output assembly

The AD8000 was chosen for its high bandwidth, and excellent distortion and noise characteristics. It also has the ability to be put into sleep mode to conserve power when not required.

The values listed in the representative schematic shown in **Figure 8** were chosen to allow each side of the DAC current output to swing close to the positive limits of the compliance voltage with a DAC output current of 0 to 20mA. The DAC compliance voltage range is -0.5V to 0.6V. With the values chosen, each side of the DAC output swings approximately from -0.45 to 0.55Vdc. The full scale output amplitude is set to a nominal 2Vp-p (+10dBM).

3.4.1 Output Filters

The default factory configuration for the FMC216 shown in **Figure 8** above is DC coupled and provides harmonic suppression of about 50 dBFS. The typical frequency response of the factory default configuration is shown in below in **Figure 9**.

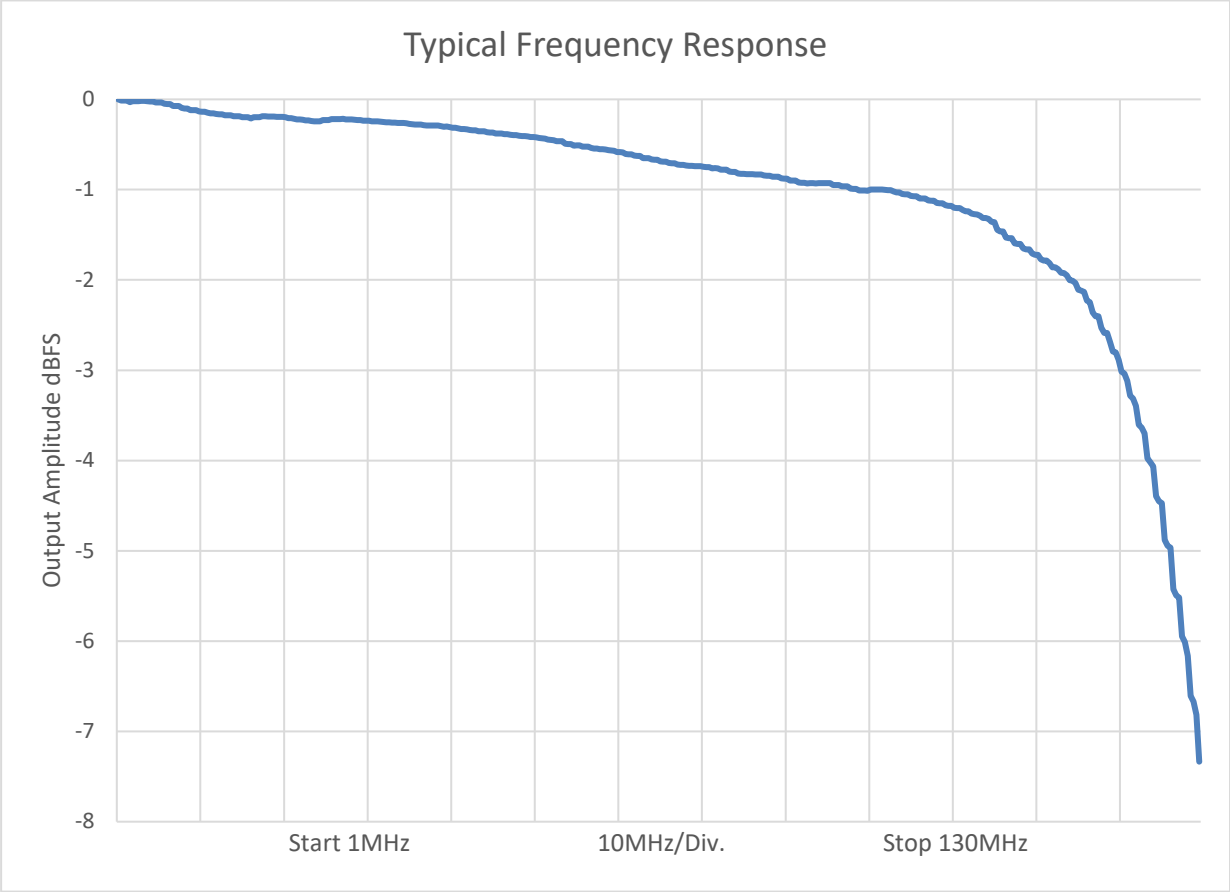


Figure 9: Output Frequency Response

3.5 External Trigger / Synchronization Input

The trigger input circuitry uses an ON Semiconductor NB6N11S 'Any-Level' input buffer to support LVTTL/LVCMOS and similar input standards. The single ended input is DC coupled with an input impedance of approximately 2kΩ and a threshold of 1.25V.

One output of the trigger buffer is routed to the FPGA via the FMC connector while the other output is routed to the trigger multiplexer to support the synchronization circuit. The trigger input can be used as sync input, synchronizing local converters, or synchronizing multiple cards. See section 3.6.

3.5.1 External Trigger Output

The trigger output on the front I/O connector can provide a trigger signal directly from the FPGA.

The Single Ended CMOS Trigger output signal from the FPGA (TRIGGER_OUT) is level translated from VADJ and buffered to 3.3V CMOS with an SN74AVC2T245RSWR. A 49.9 Ohm series resistor in the output path allows the gate to cleanly drive 50 Ohm cables.

For VADJ voltages below 1.8V the typical maximum toggle frequency is ~160MHz.

For VADJ voltages above 1.8V the typical maximum toggle frequency is ~250MHz

Like any other pin that can toggle, keeping the FPGA TRIGGER_OUT pin static when not using this function will help reduce noise that otherwise might be coupled into the RF outputs.

3.6 Multi-Channel Synchronization

Since the converters are subclass 1 JESD204B devices, they support synchronization across the channels. Frame and LMFC clocks are generated inside the devices and are used to properly align the phase of the serial data. The phases of the frame and multi-frame clocks are determined by the frame alignment step for JESD204B link initialization. Frame alignment takes place on the rising edge of the SYSREF signal. The LMK04828B is used to generate device clocks and SYSREF signals and guaranty proper setup and hold time between those.

The external trigger input can also be utilized to generate synchronous SYSREF events across multiple FMC216 boards. The synchronization pulse is also routed to the FPGA.

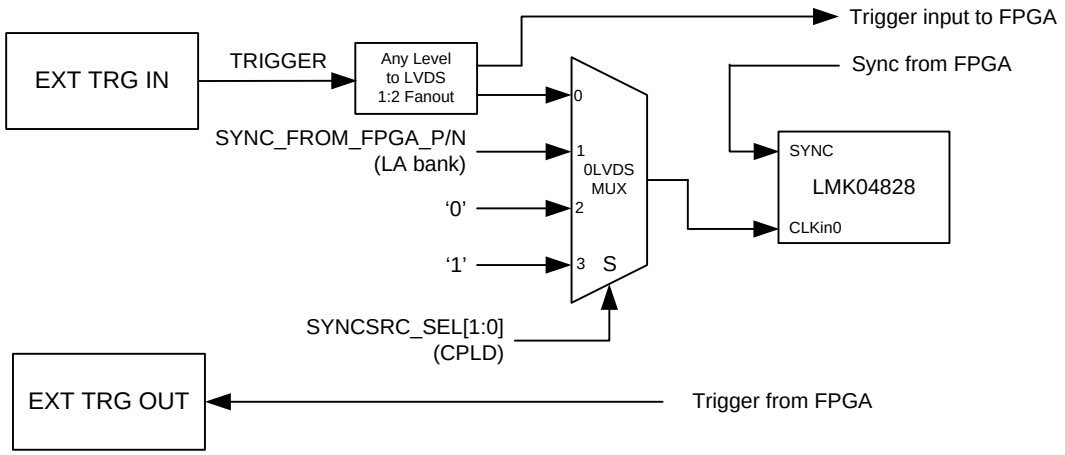


Figure 10: Synchronization Topology

For synchronization to work across multiple cards, the cards need to be supplied with synchronized clock or reference signals. In addition, an external synchronization signal is required. Match the cable length between the clock/sync generator and each FMC216. The clock generator needs to be able to tune the phase relationship between the clock and sync signal to satisfy the setup/hold timing requirements.

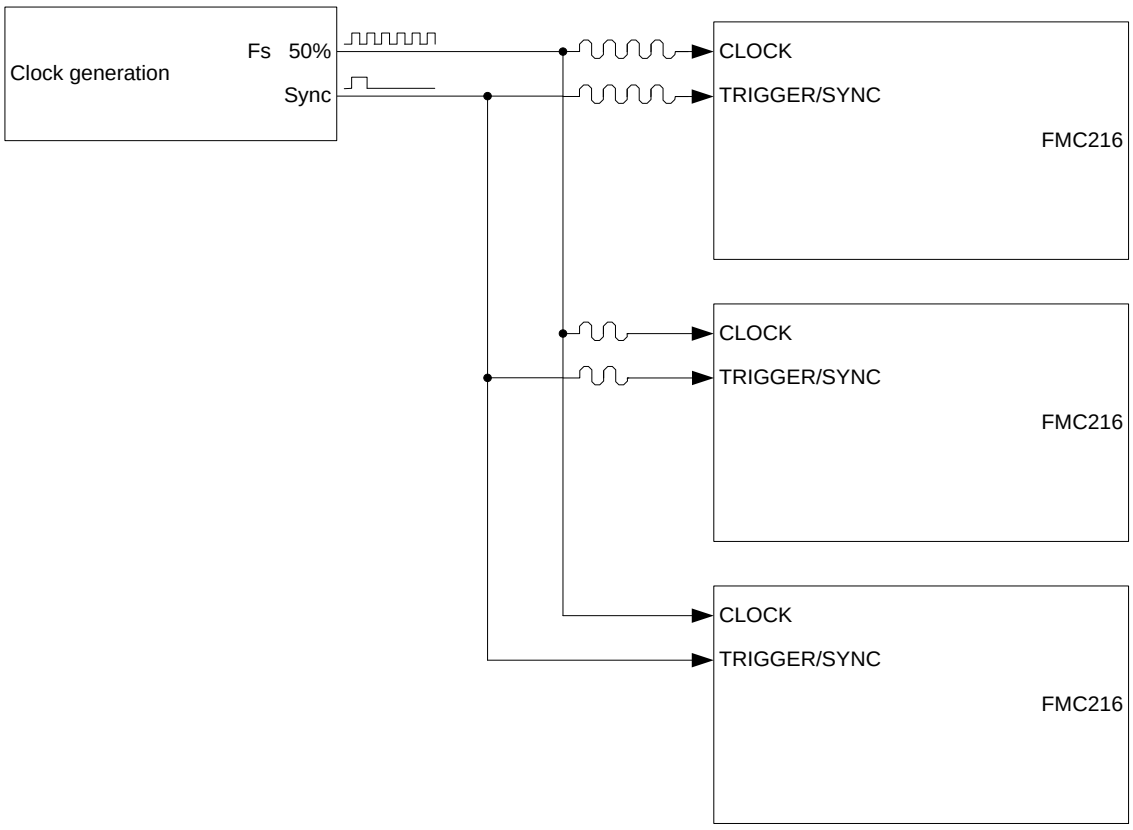


Figure 11: Synchronizing Multiple Cards

3.6.1 Trigger Input Multiplexer

As shown in **Figure 10** above, the trigger source is selected by a 4:1 LVDS multiplexer / buffer, based on the state of CPLD control signals SYNCSRC_SEL0_3.3, and SYNCSRC_SEL1_3.3, the multiplexer selects 1 of 4 possible signals.

An I^2C write to CPLD register 3, bits 4 and 5 determines the state of the multiplexer as shown in **Table 5** below.

State	SYNCSRC_SEL1_3.3 CPLD Register 3, Bit 4	SYNCSRC_SEL0_3.3 CLPD Register 3, Bit 5	Signal on LMK CLKin0
0	0	0	External Trigger Input
1	0	1	FPGA_SYNC_OUT
2	1	0	Logic 0
3	1	1	Logic 1

Table 5: Trigger Multiplexer States

To generate a software trigger from the application (asynchronous), the initial multiplexer state should be 2 placing the trigger signal at a logic 0 state. To initiate a trigger, changing the state to 3, and then back to 2 writing will result in a positive trigger pulse. For synchronous trigger operations it is recommended to set the SYNCSRC_SEL bits to static values and toggle the trigger exclusively from the External Trigger Input of FPGA_SYNC_OUT.

3.7 Clock tree

3.7.1 External Clock Input

The clock input on the front I/O connector is connected to CLKin1 of the LMK04828B, this input can be programed as the external reference to PLL1, the external VCO input to the Clock Distribution Path, or if not being used, turned off. For further details, refer to the LMK04828 data sheet and/or Abaco reference designs.

To minimize potential noise, it is strongly recommended to turn this input off when it is not being used.

3.7.2 External Clock Output

The 50 Ohm singled ended clock output on the front I/O connector is connected to LMK04828B 100 ohm differential DCLKOUT12 output thru a 2:1 impedance matching transformer. The typical output amplitude verses frequency is shown in **Figure 12** below.

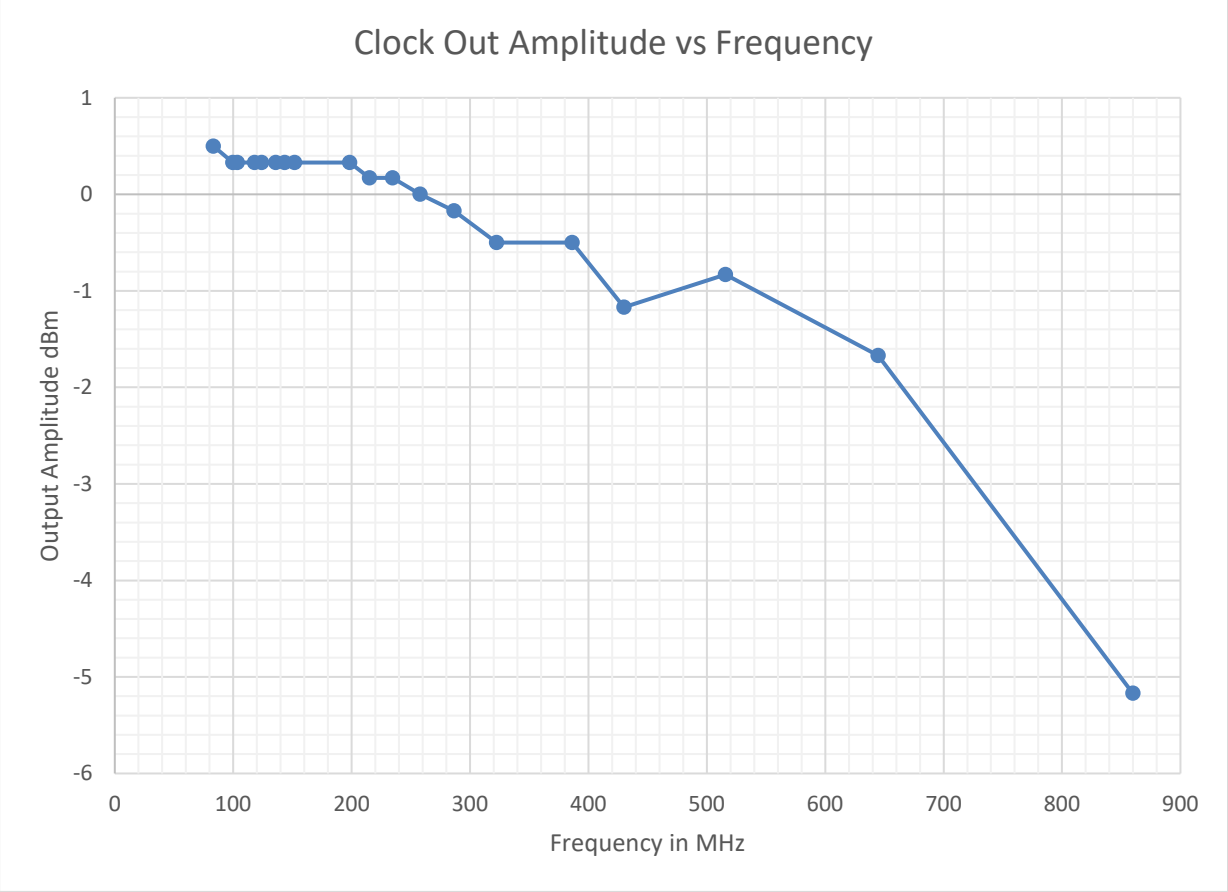


Figure 12: Typical Clock Output Amplitude vs. Frequency

In general, the external clock output can be programed via LMK04828 registers 0x130, 0x131, 0x133, 0x134, 0x136, and 0x137.To enable the output, LMK register 0x137 bit 0 should be set, to disable the output bit 0 should be cleared. Selecting an output driver in register 0x137 other than LVDS will result in less than optimal results. For detailed configuration information, refer to the LMK04828 datasheet.

Note: when not using the external clock output is it strongly recommended to turn off the output via LMK04828 Register 0x147 Bit 0 to minimize any interference that might couple into the RF outputs.

Note: when the internal clock is enabled and there is no need for an external reference, it is strongly recommended to leave the external clock input disconnected to prevent interference with the internal clock.

3.7.3 Architecture

The FMC216 card offers a clock architecture that combines flexibility and high performance. Components have been chosen in order to minimize jitter and phase noise to reduce

degradation of the data conversion performance. The user may choose to use an external sampling clock or an internal sampling clock.

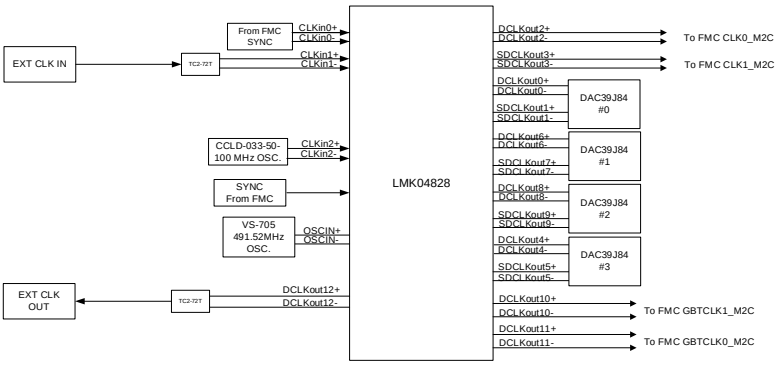


Figure 13: Clock Tree Architecture

TI's LMK04828B Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner is the base of the clock tree. Internally to the LMK04828B, there are two Integer-N PLLs. There are three different configurations of the clocking architecture:

1. Internal clock with internal 100 MHz reference oscillator,

   PLL1 locks the 491.52 MHz VCXO to internal 100MHz reference oscillator. PLL2 provides frequency multiply function.

2. Internal clock with external reference

   PLL1 locks the 491.52 MHz VCXO to an external reference clock source. PLL2 provides frequency multiplication.

   Note: in this mode the internal 100MHz Reference oscillator should be powered down to reduce possible noise and interference.

   Note: the 100MHz internal reference oscillator can be turned off by an I^2C write to CPLD register 1 clearing bit 0, This clears signal OSC100_EN_3.3 to a logic low turning off the oscillator.

3. External clock

   Neither of the internal PLLs are used. The external input signal is directly used by the LMK04828 as the source for the clock distribution section.

   Note: In this mode both the Internal 100MHz reference and 491.52MHZ VCXO should be powered down to reduce possible noise and interference. To power off both oscillators an I^2C Write to CPLD Register 1, clearing Bit 0 and Bit1. This clears signals OSC100_EN_3.3, and OSC491_EN_3.3 to a logic low turning off both oscillators.

The master clock signal, whether generated by PLL2 or an external clock, drives the root of the clock distribution system. Clocking is then fed to the master SYSREF divider and each of the 7 DCLK outputs through independent dividers.

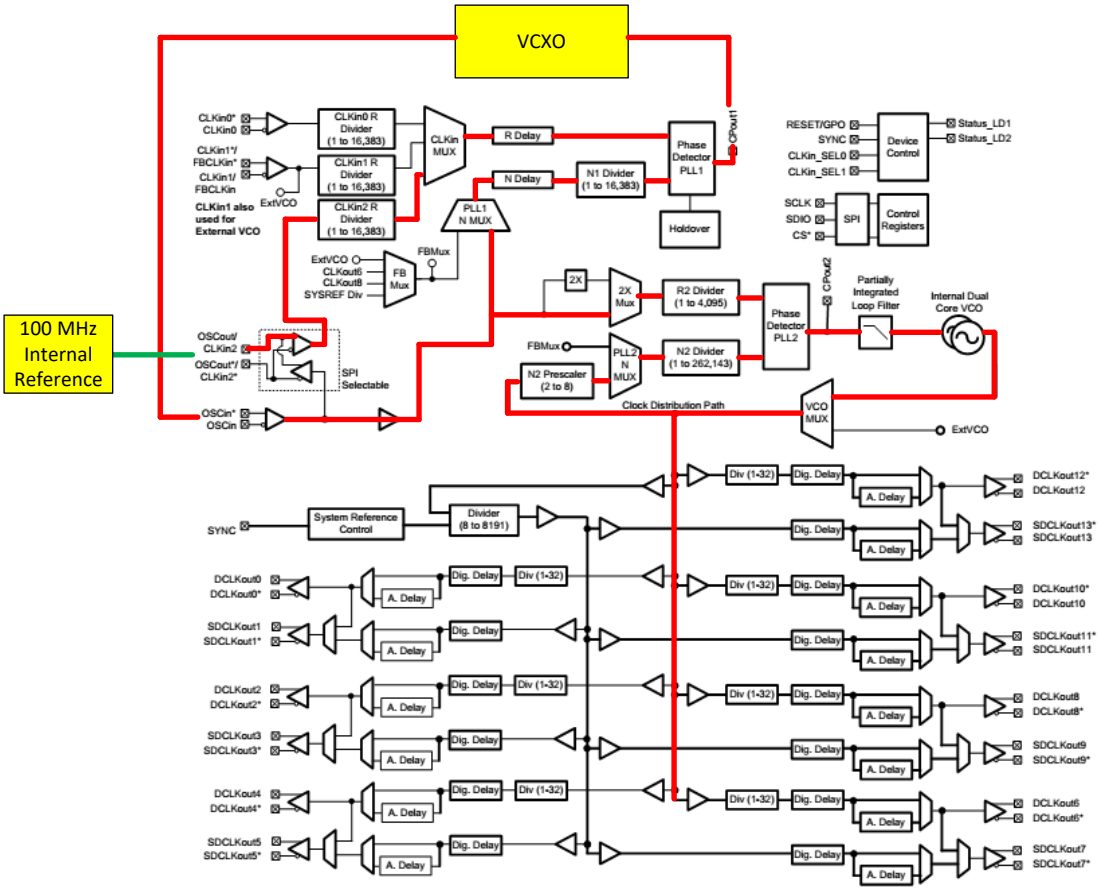


Figure 14: Internal clock with internal 100 MHz reference (Ref XTAL locked)

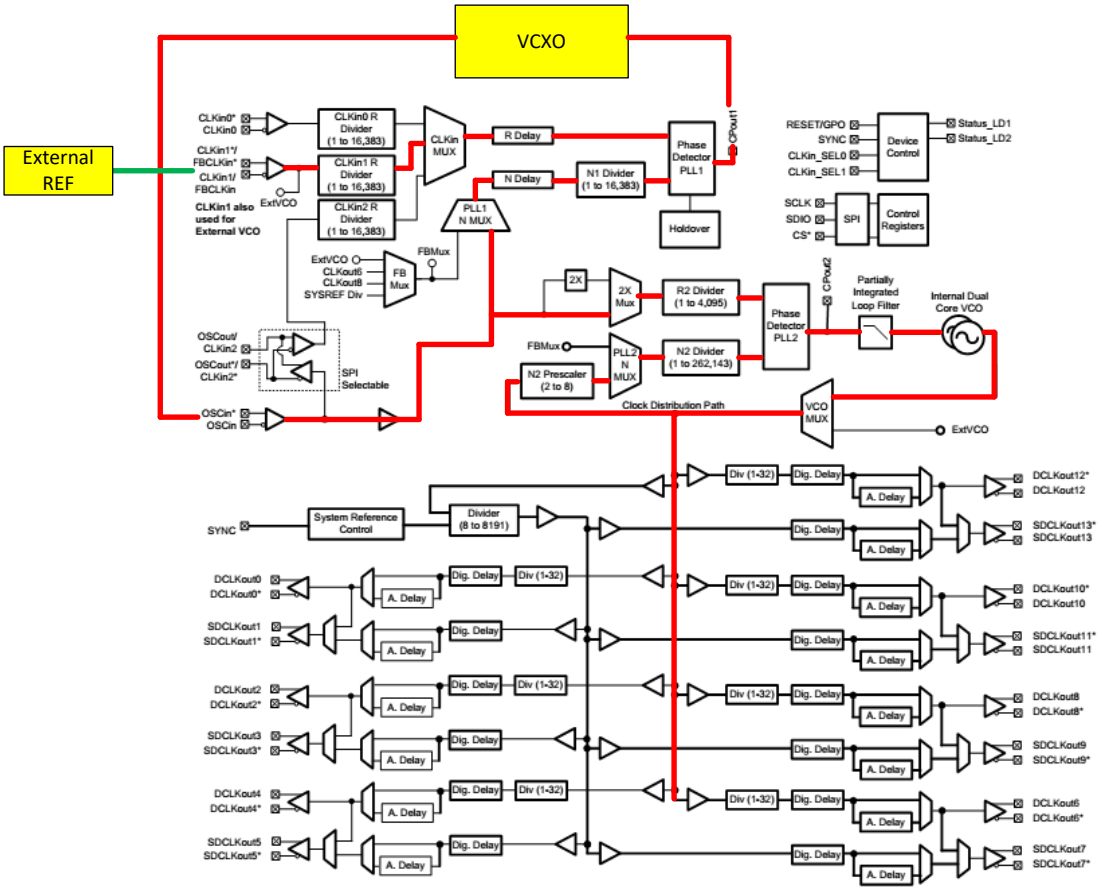


Figure 15: Internal clock with external reference (Ref XTAL locked)

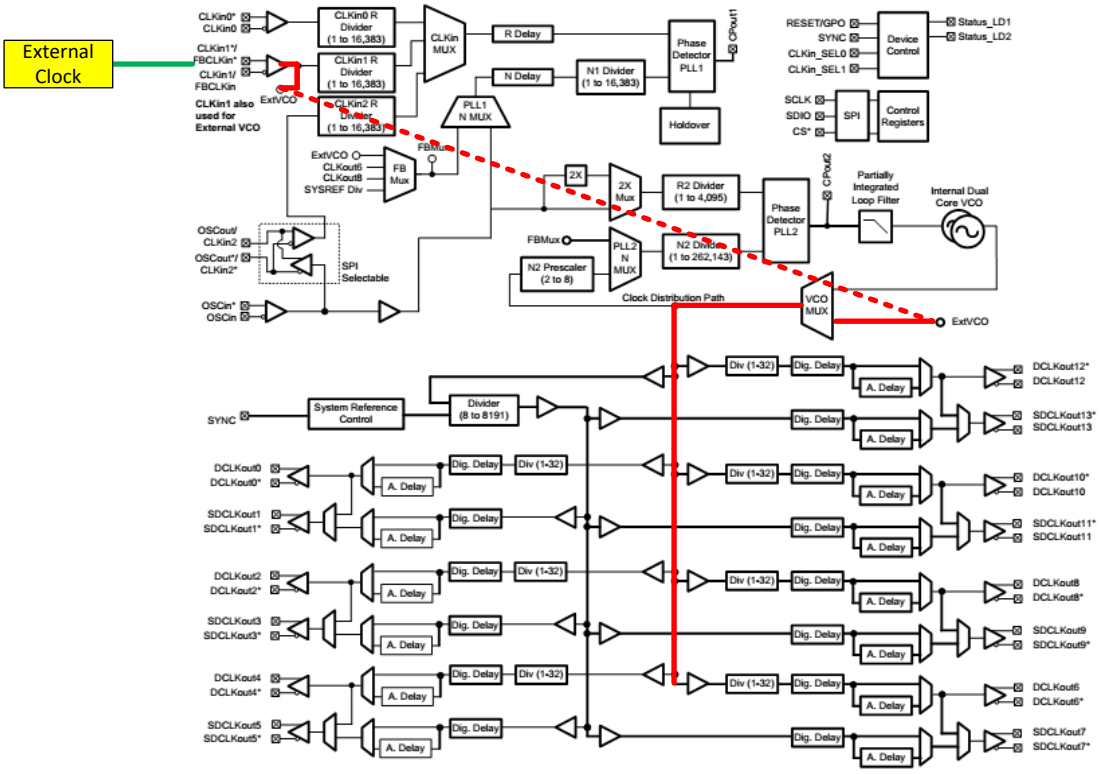


Figure 16: External clock

3.7.4 PLL Design

The PLL functionality of the LMK04828B is used to operate from an internal sampling clock. This enables flexibility in frequency selection while maintaining high performance.

The default loop filter for PLL1 is designed for a phase detector frequency of 80kHz. This was chosen to allow a default external reference input frequency of 10MHz.

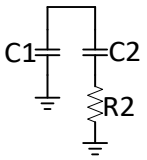


Figure 17: PLL1 loop filter design

Reference	Value	Device Size
C1	120nF	0402
C2	4700nF	0402
R2	10k	0402

Table 6: PLL 1 loop filter component values

The default loop filter for PLL2 is designed for a phase detector frequency of 160kHz.

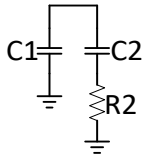


Figure 18: PLL2 loop filter design

Reference	Value	Device Size
C1	0.027nF	0402
C2	2.7nF	0402
R2	14.7k	0402

Table 7: PLL 2 loop filter component values

3.7.5 Clock Ranges

The available clock ranges with the above architecture and phase detector frequencies are shown in **Table 8** below. Note that the DAC39J84 does not allow Interpolation of 1 in the LMFS = 2441 configuration.

Device and, lane configuration	Min Fdata (MSPS)	Max Fdata (MSPS)	Min Fdac (MSPS)	Max Fdac (MSPS)
FMC216, LMFS = 2441 Interpolation = 4	50	312.5	100	625
FMC216, LMFS = 2441 Interpolation = 4	25	312.5	100	1250
FMC216, LMFS = 2441 Interpolation = 8	19.53125	312.5	156.25	2500
FMC216, LMFS = 2441 Interpolation =16	19.53125	175	312.5	2800
FMC208, LMFS = 4421 Interpolation = 1	100	625	100	625
FMC208, LMFS = 4421 Interpolation = 2	50	625	100	1250
FMC208, LMFS = 4421 Interpolation = 4	39.0625	625	156.25	2500
FMC208, LMFS = 4421 Interpolation = 8	39.0625	350	312.5	2800

Table 8: DAC Clock Ranges

The GBT routing required to support this as shown in **Figure 19** below. This configuration maximizes the available DACs based on the number of available lanes

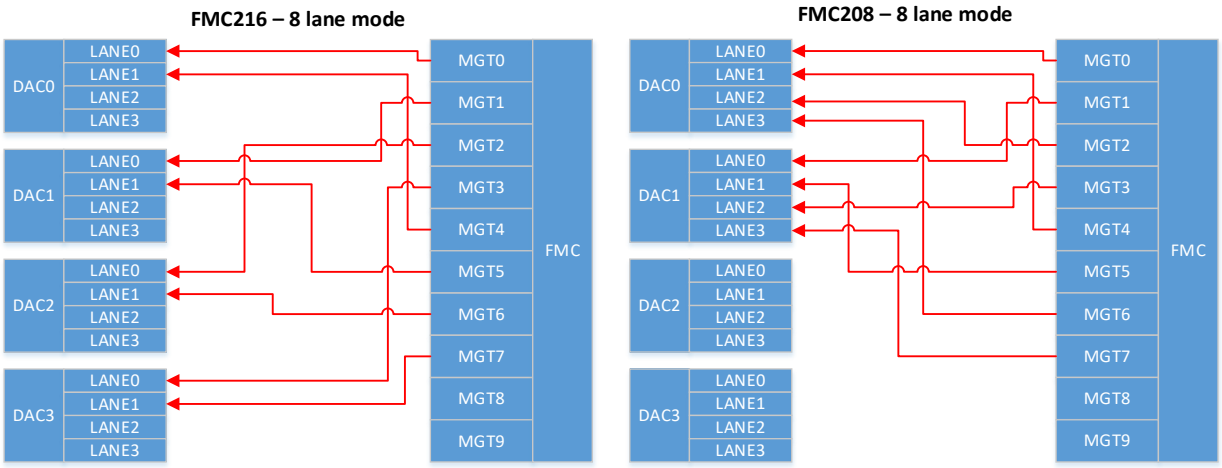


Figure 19: GBT Lane Routing

3.7.6 JESD204B Default Setup

The default DAC input sample rate is 312.5 MSPS. When interpolated by 4, this leads to an output sample rate of 1250 MSPS.

For proper operation of the DAC, the following setup is used:

L = 2
M = 4
F = 4
S = 1
K = 32

This requires a SYSREF signal to be 9.7656 MHz with a divide value of 256 internal to the LMK04828 (assuming a PLL2 frequency of 2.5 GHz).

3.8 Power Supply

Power is supplied to the FMC216 card through the FMC connector. The pin current rating is 2.7A, but the overall maximum for each supply is limited according to **Table 9** below.

Voltage	# Pins	Max Amps	Max Watt
+3.3V	4	3 A	10 W
+12V	2	1 A	12 W
VADJ (+1.8V / +2.5V)	4	4 A	10 W
VIO_B (VADJ)	2	1.15 A	2.3 W

Table 9: FMC standard power specification

The power provided by the carrier card can be very noisy. Special care is taken with the power supply generation on the FMC216 card to minimize the effect of power supply noise on clock generation and data conversion.

Power plane	Typical	Maximum
VADJ	1 mA	1 mA
3P3V	2600 mA	3300 mA
12P0V	900 mA	1200 mA
3P3VAUX (Operating) 3P3VAUX (Standby)	0.1 mA 0.01 µA	3 mA 1 µA

Table 10: Typical / Maximum current drawn from FMC216

3.9 Level Translation

The FMC216 has a several signals that are single ended that are connected to the FMC connector. The bidirectional CPLD control signals are translated to VADJ by a TXB0304RUTR and the remaining signals are translated to VADJ by an SN74AVC2T245RSWR.

3.10 CPLD Interface

A CPLD is implemented on the board to control the FMC216 through a minimal amount of connections on the FMC connector. This allows for a maximum number of connections that may be passed through to other cards in a stacked configuration.

The FMC216 is controlled from the carrier hardware through the I^2C communication bus. The CPLD accepts commands from the I^2C communications bus and performs other local functions including

- Distribute SPI access from the carrier hardware to the local devices
- Control the power state of local devices
- Control the trigger multiplexer
- Collect local status signals and store them in a register (register 4) which can be accessed from the carrier hardware.

- Drive a user defined LED (typically local power good)

3.10.1 CPLD Simplified Block Diagram

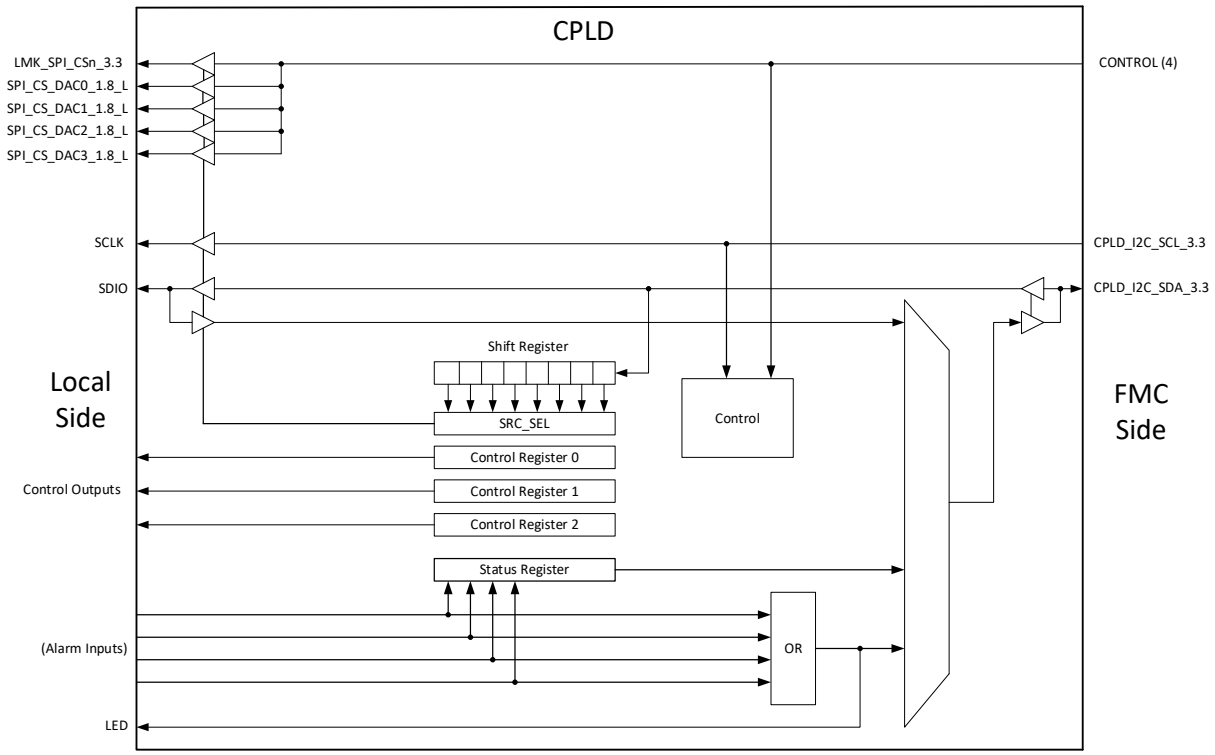


Figure 20: Simplified CPLD Block Diagram

4 Controlling the FMC216

Control of the FMC216 is accomplished via commands sent over the I²C bus, a good knowledge of the internal structure and communication protocols of relevant on-board devices is required.

For detailed information it is recommended to refer to the datasheets mentioned in the related documents section of this document.

Examining the code in the BSP / Fmc216APP will also give some good insight in how this is achieved. In addition, Abaco may be contacted for support (www.4dsp.com).

4.1 I²C Devices

The devices shown in **Table 11** are directly connected to the I²C bus, The EEPROM is powered by VAUX and can be read any time whereas the other peripherals require the board to be fully powered.

Device	I2C Address	GA1	GA0	Address Binary	Address Hex
M24C02 (EEPROM)	10100XX	0 0 1 1	0 1 0 1	1010000 1010010 1010001 1010011	0x50 0x52 0x51 0x53
AD7291 (Voltage Monitor)	010XXXX*	0 0 1 1	0 1 0 1	0101111 0101100 0100011 0100000	0x2F 0x2C 0x23 0x20
CPLD (Board Control)	00111XX	0 0 1 1	0 1 0 1	0011100 0011101 0011110 0011111	0x1C 0x1D 0x1E 0x1F

Table 11: I²C slave addresses

Note: On the FMC216 the AD7291's address line GA0 is connected to AS0 and GA1 is connected to AS1.

4.2 Controlling the CPLD

The CPLD is controlled by commands issued over the I²C bus, there are also 4 user defined control lines from the FPGA not presently implemented. The register map for the CPLD is shown below in **Table 12** below. Access to these registers is the same as any other I²C peripheral. **Note: for clarity, this manual will identify CPLD registers by their physical I²C address in the CPLD, along with any associated functionality.**

Function or Signal Name if applicable	Register Address		Description
	0x00		**Register 0 (command input)**
	W	Bit 0	Write '1' initiates a 32-bit SPI cycle to the LMK04828 Clock Generator
	W	Bit 1	Write '1' initiates a 32-bit SPI cycle to DAC0 DAC39J84 (Ch. 0-3)
	W	Bit 2	Write '1' initiates a 32-bit SPI cycle to DAC1 DAC39J84 (Ch. 4-7)
	W	Bit 3	Write '1' initiates a 32-bit SPI cycle to DAC2 DAC39J84 (Ch. 8-11)
	W	Bit 4	Write '1' initiates a 32-bit SPI cycle to DAC3 DAC39J84. (Ch. 12-15)
	W	Bit 5	Reserved for future use, write '0's.
	W	Bit 6	Reserved for future use, write '0's.
	W	Bit 7	Reserved for future use, write '0's.
	0x01		**Register 1 (control outputs)**
OSC100_EN_3.3	R/W	Bit 0	'0' disables internal 100MHz Reference Oscillator '1' Enables internal 100MHz PLL1 Reference Oscillator
OSC491_EN_3.3	R/W	Bit 1	'0' Disables Internal 491.52MHz VCXO PLL2 Reference Oscillator '1' Enables Internal 491.52MHz VCXO PLL2 Reference Oscillator
RESET_DACS_1.8_L	R/W	Bit 2	'0' Assert all 4 DAC39J84 Reset Lines '1' Normal Operation
LMK_RESET_3.3	R/W	Bit 3	'0' Normal Operation LMK04828 Clock Chip '1' Assert CLK reset (AD9517)
LMK_CLKIN_SEL_0_3.3	R	Bit 4	State of LMK04828 CLKin0_Sel Pin, Write has no effect
LMK_CLKIN_SEL_1_3.3	R	Bit 5	State of LMK04828 CLKin1_Sel Pin, Write has no effect
Reserved	R/W	Bits 6-7	Reserved write only '00'
	0x02		**Register 2 (control outputs)**
CH0-3_ENABLE_3.3	R/W	Bit 0	'0' Disables output amplifiers for DAC3 Channels 0,1,2, and 3 '1' Enables output amplifiers for DAC3 Channels 0,1,2, and 3
CH4-7_ENABLE_3.3	R/W	Bit 1	'0' Disables output amplifiers for DAC3 Channels 4,5,6, and 7 '1' Enables output amplifiers for DAC3 Channels 4,5,6, and 7
CH8-11_ENABLE_3.3	R/W	Bit 2	'0' Disables output amplifiers for DAC3 Channels 8,9,10, and 11 '1' Enables output amplifiers for DAC3 Channels 8,9,10, and 11
CH12-15_ENABLE_3.3	R/W	Bit 3	'0' Disables output amplifiers for DAC3 Channels 12,13,14, and 15 '1' Enables output amplifiers for DAC3 Channels 12,13,14, and 15
DAC0_SLP_1.8 (Ch. 0-3)	R/W	Bit 4	'0' DAC0 Normal Operation '1' Places DAC0 in Sleep Mode
DAC1_SLP_1.8 (Ch. 4-7)	R/W	Bit 5	'0' DAC1 Normal Operation '1' Places DAC1 in Sleep Mode

DAC2_SLP_1.8 (Ch. 8-11)	R/W	Bit 6	'0' DAC2 Normal Operation '1' Places DAC2 in Sleep Mode
DAC3_SLP_1.8 (Ch. 12-15)	R/W	Bit 7	''0' DAC3 Normal Operation '1' Places DAC3 in Sleep Mode
	0x03		**Register 3 (control outputs)**
DAC0_TXEN_1.8	R/W	Bit 0	'0' Disables DAC0 Outputs (outputs set to midscale) '1' Enables DAC0 Outputs (Channels 0,1,2, and 3)
DAC1_TXEN_1.8	R/W	Bit 1	'0' Disables DAC1 Outputs (outputs set to midscale) '1' Enables DAC1 Outputs (Channels 4,5,6, and 7)
DAC2_TXEN_1.8	R/W	Bit 2	'0' Disables DAC2 Outputs (outputs set to midscale) '1' Enables DAC2 Outputs (Channels 8,9,10, and 11)
DAC3_TXEN_1.8	R/W	Bit 3	'0' Disables DAC3 Outputs (outputs set to midscale) '1' Enables DAC3 Outputs (Channels 12,13,14, and 15)
SYNCSRC_SEL0_3.3	R/W	Bit 4	These lines control the SYNC son LMK CLKin0 P/N '0' Selects External Trigger input as SYNC Source '1' Selects FPGA FPGA_SYNC_OUT_P, LA01P/N as SYNC Source '2' Sets SYNC signal to logic 1 '3' Clears SYNC signal to logic 0
SYNCSRC_SEL1_3.3	R/W	Bit 5	
GA0_CC_OUT_3.3	R/W	Bit 6	These bits drive the GA0 and GA1 Signals on the optional carrier connector, they should be remapped to prevent I^2C bus conflicts
GA1_CC_OUT_3.3	R/W	Bit 7	
	0x04		**Register 4 (status)**
DAC0_ALM_1.8	R	Bit 0	DAC0 ALARM output signal
DAC1_ALM_1.8	R	Bit 1	DAC1 ALARM output signal
DAC2_ALM_1.8	R	Bit 2	DAC2 ALARM output signal
DAC3_ALM_1.8	R	Bit 3	DAC3 ALARM output signal
PMTR_ALM_3.3_L	R	Bit 4	State of AD7291 'ALERT' output pin
GA0_MOD_IN_3.3	R	Bit 5	state of Host FPGA FMC Signal GA0
GA1_MOD_IN_3.3	R	Bit 6	state of Host FPGA FMC Signal GA1
reg_control(0)	R	Bit 7	Reserved
	0x05		**Register 5 (CPLD Firmware Version)**
	R	Bits 0-15	Reading this location will return a 16bit word representing CPLD Firmware Version, A value of 0x0010 is the initial release.
	0x06		**Register 6 (SPI Command, Last Byte to Send)**
	R/W	Bits 0-7	Write bits 7-0 of the SPI command here
	0x07		**Register 7 (SPI Command, Third Byte to Send)**
	R/W	Bits 8-15	Write bits 15-8 of the SPI command here
	0x08		**Register 8 (SPI Command, Second Byte to Send)**
	R/W	Bits 16-23	Write bits 23-16 of the SPI command here
	0x09		**Register 9 (SPI Command, First Byte to Send)**
	R/W	Bits	Write bits 31-24 of the SPI command here

		24-31	
	0x0A		**Reserved**
	0x0b		**Reserved**
	0x0C		**Reserved**
	0x0D		**Reserved**
	0x0E		**SPI Read-back Register Upper 8 bits**
	R	Bits 8-15	This register is the upper 8bits (15-8) of the response from the last SPI read command that was sent
	0x0F		**SPI Read-back Register Lower 8 bits**
	R	Bits 0-7	This register is the lower 8bits (7-0) of the response from the last SPI read command that was sent

Table 12: CPLD Register Map

4.3 Controlling the Clock Tree

4.3.1 General Guidelines

Apart from enabling the onboard reference oscillators, and the trigger circuitry, the whole clock tree is controlled by programming the LMK04828B device via SPI thru the CPLD's I^2C serial interface. The following guidelines should be taken into account:

The internal oscillators should be disabled if not required. This includes both the 491.52 MHz VCSO and the 100 MHz XTAL oscillator. (bit_0 and bit_1 of CPLD register 1.)

1. Before programming the device, and with a clock applied, strobe the LMK_RESET_3.3 line from low, to high, to low again to insure the part is in a known state. (bit_3 CPLD register 1).
2. It is recommended to disable the unused clock outputs on the LMK04828B.
3. It is recommended to disable PLL functions and VCO input on the LMK04828B when an external sampling clock is applied.
4. When the internal clock is used the PLL functions need to be enabled. The recommended phase detector frequency is 100MHz. The recommended VCO frequency is 2500MHz. In case the internal reference is used the reference divider should be set to 1. The VCO divider is set to 25.
5. Other phase detector frequencies may be used, but stability of the PLL is not guaranteed in all cases.
6. TI notes that sending SPI commands while the PLLs are locked may degrade phase noise performance, the I^2C / SPI bus should remain static as much as possible during normal operation.

4.3.2 LMK04828 Clock Tree SPI Communication

Communication with the LMK04828 Clock generator IC via the CPLD and I^2C bus.

Based on the desired clock source, configure bit 0 (OSC100_EN_3.3) and Bit1 (OSC491_EN_3.3) of CPLD register 1

Based on the Trigger / Sync requirements, configure bit 4 and bit 5 of CPLD register 3 (SYNCSRC_SEL0_3.3 and SYNCSRC_SEL1_3.3)

Per the TI data sheet, the LMK04828 communicates with 24bit words across the SPI bus, to send an SPI bus command to the device, the control word is padded with an extra 8 bits. The resulting 32bit word is mapped as shown below in **Figure 21**.

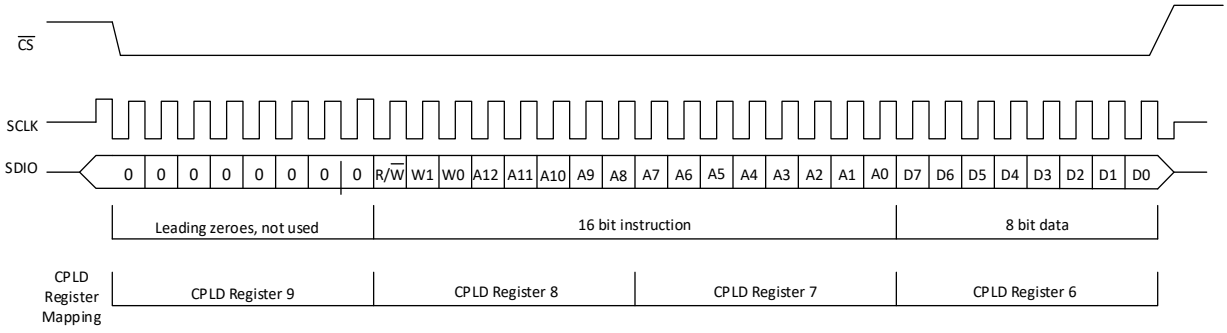


Figure 21: LMK04828 SPI Transaction

The I^2C register transactions to the CPLD listed in sections 4.3.3 and 4.3.4 describe the operation. Note that the extra 8 bits get shifted out of the device and are of no consequence to the operation.

4.3.3 LMK04828 SPI Write Register Command Sequence:

To write an LMK04828 register the R/W bit in the SPI command must be ‘0’.
Write the first byte to send (dummy byte 0x00) to CPLD Register 9
Write the second byte to send, bits R/W thru A8 to CPLD Register 8
Write the third byte to send, bits A7 thru A0 to CPLD register 7
Write the last byte to send, D7 thru D0 to CPLD Register 6
Write an 0x01 to the CPLD register 0, to Initiate a SPI bus write of the message

4.3.4 LMK04828 SPI Read Register Command Sequence:

To write an LMK04828 register the R/W bit in the SPI command must be ‘1’.
Write the first byte (dummy byte 0x00) to send, to CPLD Register 9
Write the second byte to send, bits R/W thru A8 to CPLD Register 8
Write the third byte to send, bits A7 thru A0 to CPLD register 7
Write the last byte to send, D7 thru D0 to CPLD Register 6 (data = don’t care)
Write an 0x01 to the CPLD register 0, to Initiate a SPI bus write of the message
The result of the read operation can be read out of CPLD Register 0x0F,

4.4 Controlling the DACs

There are four Texas Instruments DAC39J84 Quad Channel, 16-Bit 2.8 GSPS DACS on the board (two on the FMC208). The DAC hardware Reset, Sleep, and TX_Enable lines along with 4 banks of output amplifiers are directly controlled by the CPLD via I^2C commands. Everything else is controlled by programming the Four DAC39J84 DACs via SPI thru the CPLD's I^2C serial interface. The following guidelines should be taken into account:

4.4.1 General Guidelines for Controlling the DACs

Controlling the DAC enables advanced control of the conversion process. The DAC39J84 can be programmed through a serial communication interface to change the input format or using advanced settings among which gain control, offset correction, and several power down modes.

1) **Important:** to maintain the phase matching between all 16 channels on the board DAC outputs A and C were inverted to keep the transmission lines matched. In order to maintain the phase relationship on all outputs the polarity of channels A and C need to be inverted. This is accomplished by setting bits 7,6,5,4 of DAC register 0x01 to 1010 on all 4 DAC39J84 devices.
2) The DAC39J84 has an on-chip low-jitter phase-locked loop (PLL). The PLL loop filter is brought out for future use, but this feature is not currently supported.
3) The DAC39J84 includes an output multiplexer before the digital to analog converters that allows any signal channel D0-D3 to be routed to any DAC A-D. See pathx_out_sel in the datasheet for details on how to configure the cross-bar switches.
4) The DAC39J84 provides an optional mechanism to protect an external power amplifier (PA) in cases when the signal power shows some abnormality. In the PA protection mechanism, the signal power is monitored by maintaining a sliding window accumulation of the last N samples. N is selectable to be 64 or 128. The average amplitude of the input signal is computed by dividing the accumulated value by the number of samples in the delay-line (N). The result is then compared against a programmable threshold value. If the threshold is violated, the delayed input signal is divided by a programmable value, to form a scaled down version of the input signal. The PA protection circuit is disabled in the default configuration.
5) All receive channels include a 12-bit counter for accumulating pattern verification errors. The counter increments once for every cycle that the TESTFAIL bit is detected. The counter will not increment when it is at its maximum value. This can be used to get a measure of the bit error rate.
6) All receive channels provide features which facilitate mapping the received data eye or extracting a symbol response. The process of transforming this data into a map of the eye or a symbol response must be performed externally, typically in software.
7) The DAC incorporates a temperature sensor block which monitors the temperature by measuring the voltage across 2 transistors. The voltage is converted to an 8-bit digital word using a successive approximation (SAR) analog to digital conversion process. The result is scaled, limited, and formatted as a twos complement value representing the temperature in degrees Celsius. The sampling is controlled by the SPI serial interface. If the temperature sensor is enabled, a conversion takes place each time the serial port is written or read. The temperature sensor is enabled even when the device is in sleep mode.
8) The DAC includes a flexible set of alarm monitoring that can be used to alert of a possible malfunction scenario. All of the alarm events can be accessed either through the SPI register and/or through the ALARM pin. The 4 individual DAC alarm pins are

mapped to the CPLD register 4 bits 0-3). Once an alarm is set, the corresponding alarm bit must be reset through the serial interface to allow further testing.

9) It is strongly recommended that any system design ensure that there is sufficient airflow to keep all four DAC temperatures within acceptable limits.

4.4.2 DAC39J84 DAC SPI Communication

Per the TI data sheet, the DAC39J84 communicates with 32bit words across the SPI bus, to send an SPI bus command to the device we pad the control word with an extra 8 bits, map the bits as shown in **Figure 22** below, and the perform the following I^2C register transactions to the CPLD. Note that the extra 8 bits get shifted out of the device and are of no consequence to the operation.

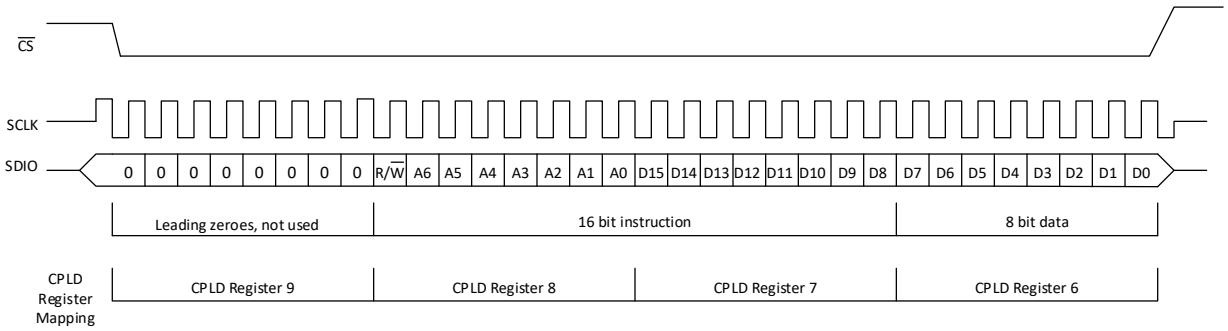


Figure 22: DAC39J84 SPI Transaction

4.4.3 DAC39J84 SPI Write Register Command Sequence:

To write an DAC39J84 register the R/W bit in the SPI command must be '0'.
Write the first byte to send, (dummy byte 0x00) to CPLD Register 9
Write the second byte to send, bits R/W thru A0 to CPLD Register 8
Write the third byte of the message, bits D15 thru D8 to CPLD register 7
Write the last byte of the message, D7 thru D0 to CPLD Register 6
Write an 0x02 (for DAC0) to the CPLD Register 0, to Initiate a SPI bus write of the message

4.4.4 DAC39J84 SPI Read Register Command Sequence:

To write an DAC39J84 register the R/W bit in the SPI command must be '1'.
Write the first byte to send, (dummy byte 0x00) to CPLD Register 9
Write the second byte to send, bits R/W thru A0 to CPLD Register 8
Write the third byte to send, bits D15 thru D8 to CPLD register 7
Write the last byte to send, D7 thru D0 to CPLD Register 6 (data = don't care)
Write an 0x02 (for DAC0) to the CPLD Register 0 to Initiate a SPI bus write of the message
The result of the read operation can be read out of CPLD Register 0x0F,

4.4.5 DAC Output Amplifier Control

The four TI DAC39J84 16bit DACs on the FMC216 each have a dedicated Analog Devices AD8000 output amplifier on each channel that can be powered down in banks of 4. The amplifiers are controlled via bits 0-3 in CPLD register 2 as described in **Table 12.** An I^2C write to CPLD register 2 setting the associated bit to 1 will turn on the four amplifiers while clearing the bit will turn off the four amplifiers.

4.4.6 DAC Sleep Signal

The four TI DAC39J84 16bit DACs on the FMC216, have their hardware sleep pin mapped to CPLD register 2 bits 4-7 as described in **Table 12**. An I^2C write to CPLD register 2 clearing an associated bit to 0 will enable the specified DAC while setting the bit to a 1 will power down the DAC.

4.4.7 DAC Reset Signal

All four TI DAC39J84 16bit DACs on the FMC216 have their hardware reset pin mapped to CPLD register 1 bit 2 as described in **Table 12.**

The normal state of this bits is a logic 1, on power-up, prior to programing the DACs, an I^2C write to CPLD register 1 clearing bit 2 to a 0, followed by another I^2C write to CPLD register 1 setting bit 2 back to a 1 will reset all of the DACs and place their registers in a known state.

4.4.8 DAC TX Enable Pins

The four TI DAC39J84 16bit DACs on the FMC216, have their hardware sleep pin mapped to CPLD register 3 bits 0-3 as described in **Table 12**. An I^2C write to CPLD register 3 setting the associated a bit to 1 will enable the specified DAC while clearing the bit to zero will disable all four of the DACs outputs and set them to midscale (0Vdc).

4.5 Guidelines for Onboard Monitoring

The FMC216 includes an AD7291 connected to the I^2C bus for monitoring several power supply voltages as well as temperature. The device can be programmed and read out through the I^2C bus.

1) At power-up, the firmware should write a ‘1’ to the Reset bit in the Command Register to initialize the part to a known state.
2) Resistive dividers are used to scale the monitored voltages to a range acceptable to the AD7291, the measured values must be multiplied by a constant to get the actual analog level (see **Table 13**). The monitor reference voltage is 2.50V, giving an input range 0-2.50V.
3) To avoid the possibility of introducing noise on the RF output it is recommended to program the minimum and maximum thresholds in the AD7291 and only read from the device when the interrupt line is asserted.

Parameter:	Voltage	Formula
Channel 0	+0.9V_ANALOG (DACS 0&2)	ADC0 * 0.00061 (2.50V FS)
Channel 1	+0.9V_ANALOG (DACS 1&3)	ADC1 * 0.00061 (2.50V FS)

Channel 2	+1.8V_ANALOG	ADC2 * 0.00061 (2.50V FS)
Channel 3	+3.3V_ANALOG	ADC3 * 0.001221 (5.0V FS)
Channel 4	VADJ	ADC4 * 0.001221 (5.0V FS)
Channel 5	+4.0V_ANALOG	ADC5 * 0.001221 (5.0V FS)
Channel 6	+12V_DIGITAL (FMC_CONN)	ADC6 * 0.003663 (15V FS)
Channel 7	-4.0V_ANALOG	((4096 – (ADC7 +488)) *1.8335 (6.6V FS)
Temperature	(internally generated)	Positive temp ADC/4 Negative temp (4096 –ADC)/4

Table 13: Temperature and Voltage Parameters

5 Environment

5.1 Temperature

Operating temperature

- -40˚C to +85˚C (Industrial)

Storage temperature:

- -40˚C to +120˚C

5.2 Monitoring

The AD7291 device may be used to monitor the voltage on the different power rails as well as the temperature. It is recommended that the carrier card and/or host software uses the power-down features in the devices in the case the temperature is too high. Normal operations can resume once the temperature is within the operating conditions boundaries. It is strongly recommended that any system design ensure that there is sufficient airflow to keep all four DAC temperatures within acceptable limits.

5.3 Cooling

Two different types of cooling will be available for the FMC216.

5.3.1 Convection Cooling

The air flow provided by the chassis fans that the FMC216 is enclosed in must dissipate the heat generated by the on board components. A minimum airflow of 300 LFM is recommended.

For standalone operations (such as on a Xilinx development kit), it is highly recommended to blow air across the FMC and ensure that the temperature of the devices is within the allowed range. Abaco's warranty does not cover boards on which the maximum allowed temperature has been exceeded.

5.3.2 Conduction Cooling

In demanding environments, the ambient temperature inside a chassis could be close to the operating temperature defined in this document. It is very likely that in these conditions the junction temperature of power consuming devices will exceed the operating conditions recommended by the devices manufacturers (mostly +85˚C). Consult the factory for the availability of cooling options for the board.

6 Safety

This module presents no hazard to the user.

7 EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system. This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the system.

8 Ordering Information

Please See: http://www.4dsp.com/FMC216.php

And http://www.4dsp.com/FMC208.php

9 Warranty

	Hardware	*Software/Firmware*
Basic Warranty (included)	1 Year from Date of Shipment	90 Days from Date of Shipment
Extended Warranty (optional)	2 Years from Date of Shipment	1 Year from Date of Shipment

10 Appendices

10.1 Appendix A: FMC216 mezzanine and carrier connector pin-out table

Table Notes:

- All power and ground pins are connected to their common nets for on both mezzanine and carrier connectors for stacked operation
- All pins not explicitly noted in the table are passed through between the mezzanine and carrier connectors for stacked operation
- Mezzanine (module) connector exclusive pins are notes in **RED**
- Carrier connector exclusive pins are noted in **BLUE**
- Common (pass through pins) are noted in **GREEN**
- Mezzanine signals remapped to Carrier Connector for stacked operation are in **VIOLET**

AV57.1	Pin	FMC216 Signal	Direction	I/O Standard	Notes
CLK0_M2C_P	H4	LLMK_DCLKOUT_2_P	Out	LVDS	D-Clock
CLK0_M2C_N	H5	LLMK_DCLKOUT_2_N	Out	LVDS	D-Clock
CLK1_M2C_P	G2	LLMK_SDCLKOUT_3_P	Out	LVDS	S-Clock
CLK1_M2C_N	G3	LLMK_SDCLKOUT_3_P	Out	LVDS	S-Clock
GBTCLK0_M2C_P	D4	LMK_SDCLK11_M2C_TO_FPGA_P	Out	LVDS	S-Clock
GBTCLK0_M2C_P	D5	LMK_SDCLK11_M2C_TO_FPGA_N	Out	LVDS	S-Clock
GBTCLK1_M2C_P	B20	LMK_DCLK10_M2C_TO_FPGA_P	Out	LVDS	DCLKOUT10_P is routed to the FPGA GBTCLK1_M2C_P
GBTCLK1_M2C_P	B21	LMK_DCLK10_M2C_TO_FPGA_N	Out	LVDS	DCLKOUT10_N is routed to the FPGA GBTCLK1_M2C_N
DP0_C2M_P	C2	DP0_C2M_P	In	CML	DAC0_LANE0_P
DP0_C2M_N	C3	DP0_C2M_N	In	CML	DAC0_LANE0_N
DP1_C2M_P	A22	DP1_C2M_P	In	CML	DAC1_LANE0_P
DP1_C2M_N	A23	DP1_C2M_N	In	CML	DAC1_LANE0_N
DP2_C2M_P	A26	DP2_C2M_P	In	CML	DAC2_LANE0_P DAC0_LANE2_P (FMC208 only)
DP2_C2M_N	A27	DP2_C2M_N	In	CML	DAC2_LANE0_N DAC0_LANE2_N (FMC208 only)
DP3_C2M_P	A30	DP3_C2M_P	In	CML	DAC3_LANE0_P DAC1_LANE2_P (FMC208 only)
DP3_C2M_N	A31	DP3_C2M_N	In	CML	DAC3_LANE0_N DAC1_LANE2_N (FMC208 only)
DP4_C2M_P	A34	DP4_C2M_P	In	CML	DAC0_LANE1_P
DP4_C2M_N	A35	DP4_C2M_N	In	CML	DAC0_LANE1_N
DP5_C2M_P	A38	DP5_C2M_P	In	CML	DAC1_LANE1_P
DP5_C2M_N	A39	DP5_C2M_N	In	CML	DAC1_LANE1_N
DP6_C2M_P	B36	DP6_C2M_P	In	CML	DAC2_LANE1_P DAC0_LANE3_P (FMC208 only)
DP6_C2M_N	B37	DP6_C2M_N	In	CML	DAC2_LANE1_N DAC0_LANE3_N (FMC208 only)
DP7_C2M_P	B32	DP7_C2M_P	In	CML	DAC3_LANE1_P DAC1_LANE3_P (FMC208 only)
DP7_C2M_N	B33	DP7_C2M_N	In	CML	DAC3_LANE1_N DAC1_LANE3_N (FMC208 only)
LA00_P_CC	G6	BUF_EXT_TRIG_TO_FPGA_P	Out	LVDS	From external trigger to FPGA
LA00_N_CC	G7	BUF_EXT_TRIG_TO_FPGA_N	Out	LVDS	From external trigger to FPGA
LA01_P_CC	D8	FPGA_SYNC_OUT_P	In	LVDS	From FPGA to clock tree trigger
LA01_N_CC	D9	FPGA _SYNC_OUT_N	In	LVDS	From FPGA to clock tree trigger
LA02_P	H7	DAC0_SYNC_P	Out	LVDS	Synchronization request to FPGA

LA02_N	H8	DAC0_SYNC_N	Out	LVDS	Synchronization request to FPGA
LA03_P	G9	DAC1_SYNC_P	Out	LVDS	Synchronization request to FPGA
LA03_N	G10	DAC1_SYNC_N	Out	LVDS	Synchronization request to FPGA
LA04_P	H10	DAC3_SYNC_P	Out	LVDS	Synchronization request to FPGA
LA04_N	H11	DAC3_SYNC_N	Out	LVDS	Synchronization request to FPGA
LA05_P	D11	DAC2_SYNC_P	Out	LVDS	Synchronization request to FPGA
LA05_N	D12	DAC2_SYNC_N	Out	LVDS	Synchronization request to FPGA
LA06_P	C10	FMC_CPLD_CTRL0_VADJ	I/O	LVCMOS	CPLD Control Signal
LA06_N	C11	FMC_CPLD_CTRL1_VADJ	I/O	LVCMOS	CPLD Control Signal
LA07_P	H13	FMC_CPLD_CTRL2_VADJ	I/O	LVCMOS	CPLD Control Signal
LA07_N	H14	FMC_CPLD_CTRL3_VADJ	I/O	LVCMOS	CPLD Control Signal
LA08_P	G12	TRIGGER_OUT	In	LVCMOS	External Trigger output from FPGA
LA08_N	G13	FPGA_SYNC_OUT_TO_LMK	In	LVCMOS	SYNC from FPGA, connects to SYNC/SYSREF_REQ of LMK
GA0	C34	GA0_MOD_IN_3.3	In	LVCMOS	Card Global Address 0 from mezzanine connector
GA1	D35	GA1_MOD_IN_3.3	In	LVCMOS	Card Global Address 1 from mezzanine connector
GA0	C34	GA0_CC_OUT_3.3	Out	LVCMOS	Card Global Address 0 from CPLD to carrier connector
GA1	D35	GA1_CC_OUT_3.3	Out	LVCMOS	Card Global Address 1 from CPLD to carrier connector
TSRT_L	D34	TRST_L	Input	LVTTL	JTAG Reset in, (also passed through)
TCK	D29	TCK	In	LVTTL	JTAG Clock in, (also passed through)
TMS	D33	TMS	In	LVTTL	JTAG Test Mode Select (also passed through)
TDI	D30	TDI	In	LVTTL	JTAG Data in (also passed through)
TDO	D31	TDO	Out	LVTTL	JTAG Data Out (also passed through)
PRSNT_M2C_L	H2	PRSNT_M2C_L	Out	Ground	Tied to GND (FM216 is present)
PRSNT_M2C_L	H2	PRSNT_M2C_CC_L	In	LVCMOS	Indicates that a stacked card is present (from carrier connector to CPLD)
PG_M2C	F1	PG_M2C	Out	Open Drain	Indicate FMC216 power good status to carrier (4.7K pullup to 3.3V)
PG_C2M	D1	PG_C2M	Out	CMOS	Indicates that Carrier power is OK
I2C_SCL	C30	I2C_SCL	In	CMOS	I^2C Bus Clock (also passed through)
I2C_SDA	C31	I2C_SDA	I/O	Open Drain	I^2C Bus Data (also passed through)
RES0	B40	RES0	n/a	n/a	Passed thru no connection
CLK_DIR	B1	CLK_DIR	Out	CMOS*	Driven by mezzanine, *pop option to tie high or low

CLK2_BIDR_P	H4	CLK0_M2C_P	I/O	LVDS	remapped signal for stacked operation
CLK2_BIDR_N	H5	CLK0_M2C_N	I/O	LVDS	remapped signal for stacked operation
CLK3_BIDR_P	G2	CLK1_M2C_P	I/O	LVDS	remapped signal for stacked operation
CLK3_BIDR_N	G3	CLK1_M2C_N	I/O	LVDS	remapped signal for stacked operation
HA17_P_CC	G6	LA00_P_CC	I/O	LVDS	remapped signal for stacked operation
HA17_N_CC	G7	LA00_N_CC	I/O	LVDS	remapped signal for stacked operation
HA18_P	D8	LA01_P_CC	I/O	LVDS	remapped signal for stacked operation
HA18_N	D9	LA01_N_CC	I/O	LVDS	remapped signal for stacked operation
HA10_P	H7	LA02_P	I/O	LVDS	remapped signal for stacked operation
HA10_N	H8	LA02_N	I/O	LVDS	remapped signal for stacked operation
HA11_P	G9	LA03_P	I/O	LVDS	remapped signal for stacked operation
HA11_N	G10	LA03_N	I/O	LVDS	remapped signal for stacked operation
HA12_P	H10	LA04_P	I/O	LVDS	remapped signal for stacked operation
HA12_N	H11	LA04_N	I/O	LVDS	remapped signal for stacked operation
HA13_P	D11	LA05_P	I/O	LVDS	remapped signal for stacked operation
HA13_N	D12	LA05_N	I/O	LVDS	remapped signal for stacked operation
HA14_P	C10	LA06_P	I/O	LVDS	remapped signal for stacked operation
HA14_N	C11	LA06_N	I/O	LVDS	remapped signal for stacked operation
HA15_P	H13	LA07_P	I/O	LVDS	remapped signal for stacked operation
HA15_N	H14	LA07_N	I/O	LVDS	remapped signal for stacked operation
HA16_P	G12	LA08_P	I/O	LVDS	remapped signal for stacked operation
HA16_N	G13	LA08_N	I/O	LVDS	remapped signal for stacked operation

Table 14: FMC Connector Pinout