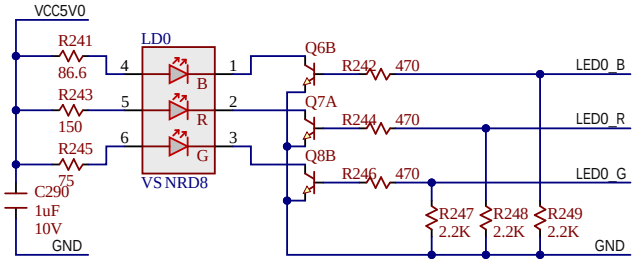
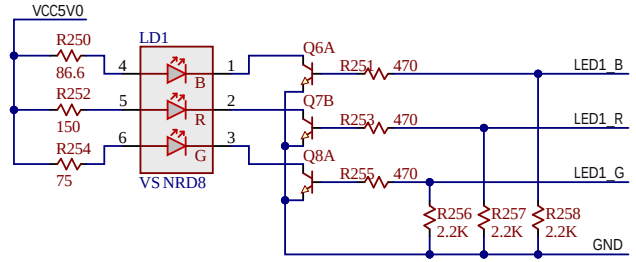
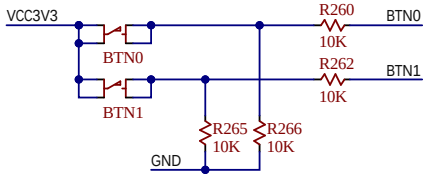
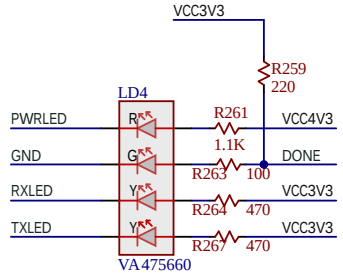
Sheet	Circuit
1.	LEDs, Buttons
2.	PMOD Ports
3.	SYZYGY Ports
4.	Ethernet and SD Card
5.	USB OTG
6.	FPGA Configuration
7.	DDR and MIO Banks
8.	FPGA Banks
9.	FPGA Power
10.	DDR3L Memory
11.	DDR3L Termination
12.	Platform MCU
13.	Power Regulation
14.	Power Regulation
15.	Power Regulation and Sequencer









Foot
F1
Foot
F2

Title	Eclypse Z7
Rev	B.2
Circuit	LEDs, Buttons
Doc#	500-393
Engineer	MTA
Author	GMA
Date	10/28/2020
Sheet#	1 out of 15

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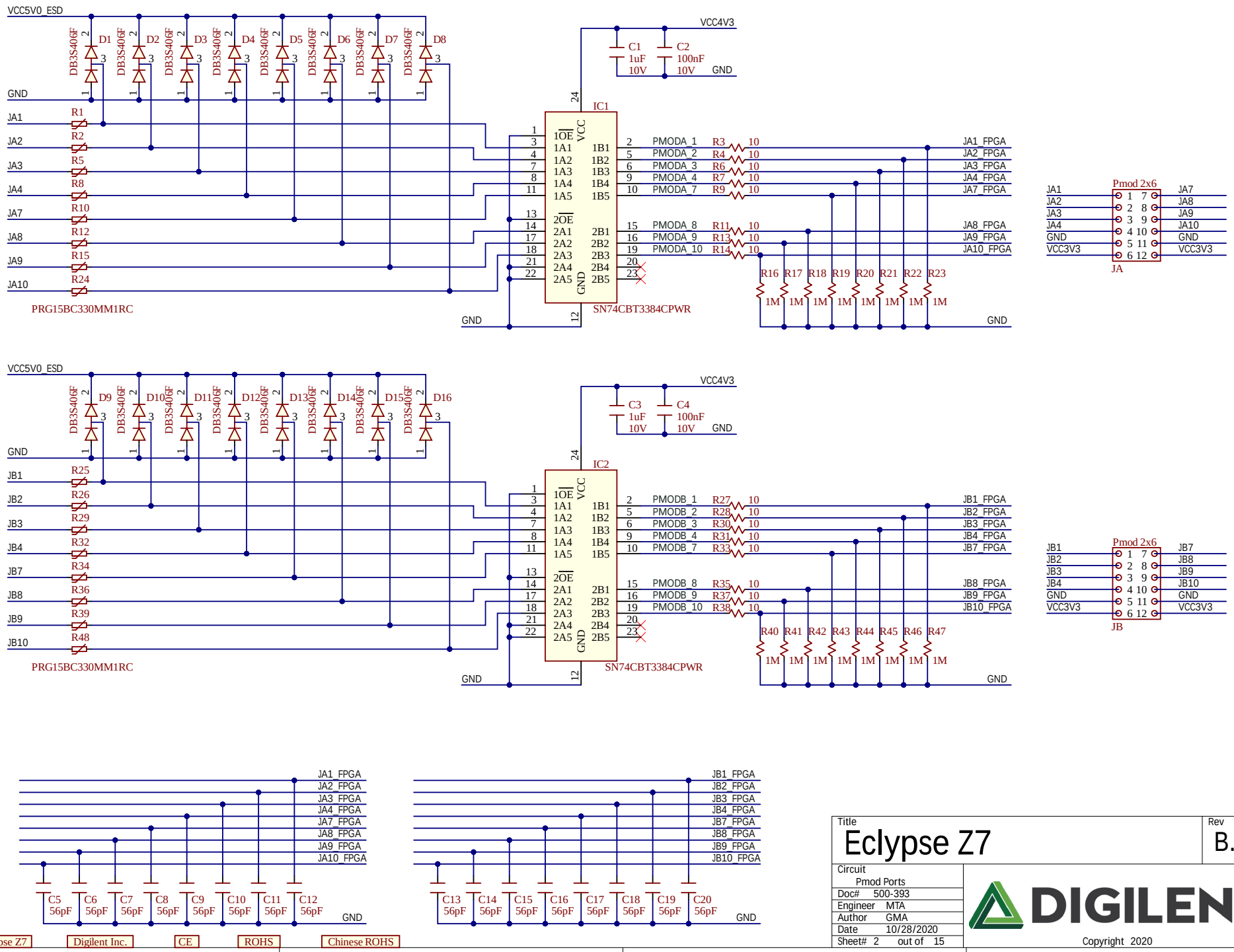
VCC5V0_ESD
DB3S406F
D1
D2
D3
D4
D5
D6
D7
D8
GND
JA1
JA2
JA3
JA4
JA7
JA8
JA9
JA10
R1
R2
R5
R8
R10
R12
R15
R24
PRG15BC330MM1RC
VCC4V3
C1
1uF
10V
C2
100nF
10V
GND
IC1
SN74CBT3384CPWR
PMODA_1
PMODA_2
PMODA_3
PMODA_4
PMODA_7
PMODA_8
PMODA_9
PMODA_10
R3
R4
R6
R7
R9
R11
R13
R14
10
JA1_FPGA
JA2_FPGA
JA3_FPGA
JA4_FPGA
JA7_FPGA
JA8_FPGA
JA9_FPGA
JA10_FPGA
R16
R17
R18
R19
R20
R21
R22
R23
1M
Pmod 2x6
JA
VCC3V3
D9
D10
D11
D12
D13
D14
D15
D16
JB1
JB2
JB3
JB4
JB7
JB8
JB9
JB10
R25
R26
R29
R32
R34
R36
R39
R48
C3
C4
IC2
PMODB_1
PMODB_2
PMODB_3
PMODB_4
PMODB_7
PMODB_8
PMODB_9
PMODB_10
R27
R28
R30
R31
R33
R35
R37
R38
JB1_FPGA
JB2_FPGA
JB3_FPGA
JB4_FPGA
JB7_FPGA
JB8_FPGA
JB9_FPGA
JB10_FPGA
R40
R41
R42
R43
R44
R45
R46
R47
JB
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
56pF
Eclypse Z7
Digilent Inc.
CE
ROHS
Chinese ROHS
Title
Eclypse Z7
Rev
B.2
Circuit
Pmod Ports
Doc# 500-393
Engineer MTA
Author GMA
Date 10/28/2020
Sheet# 2 out of 15
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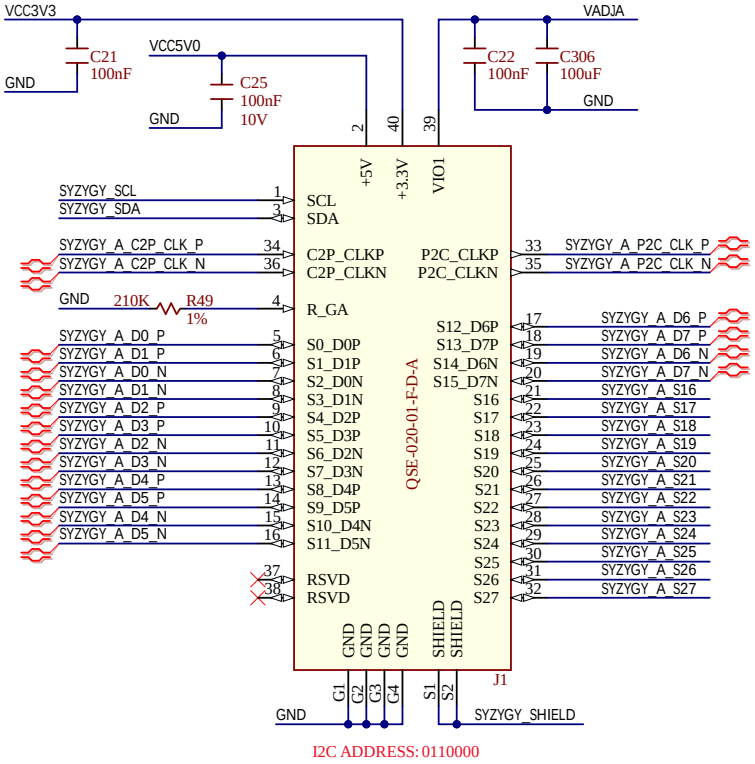
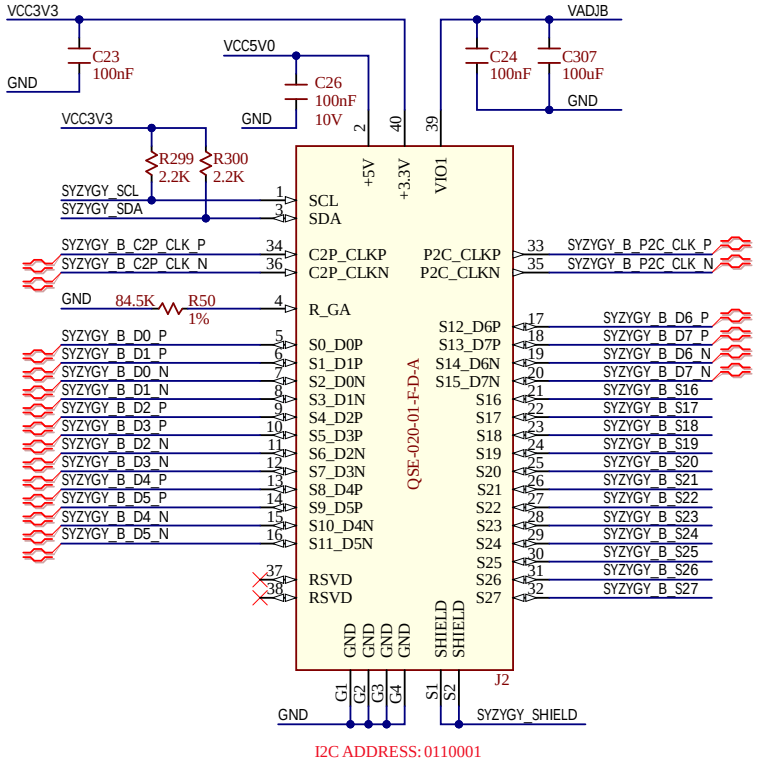
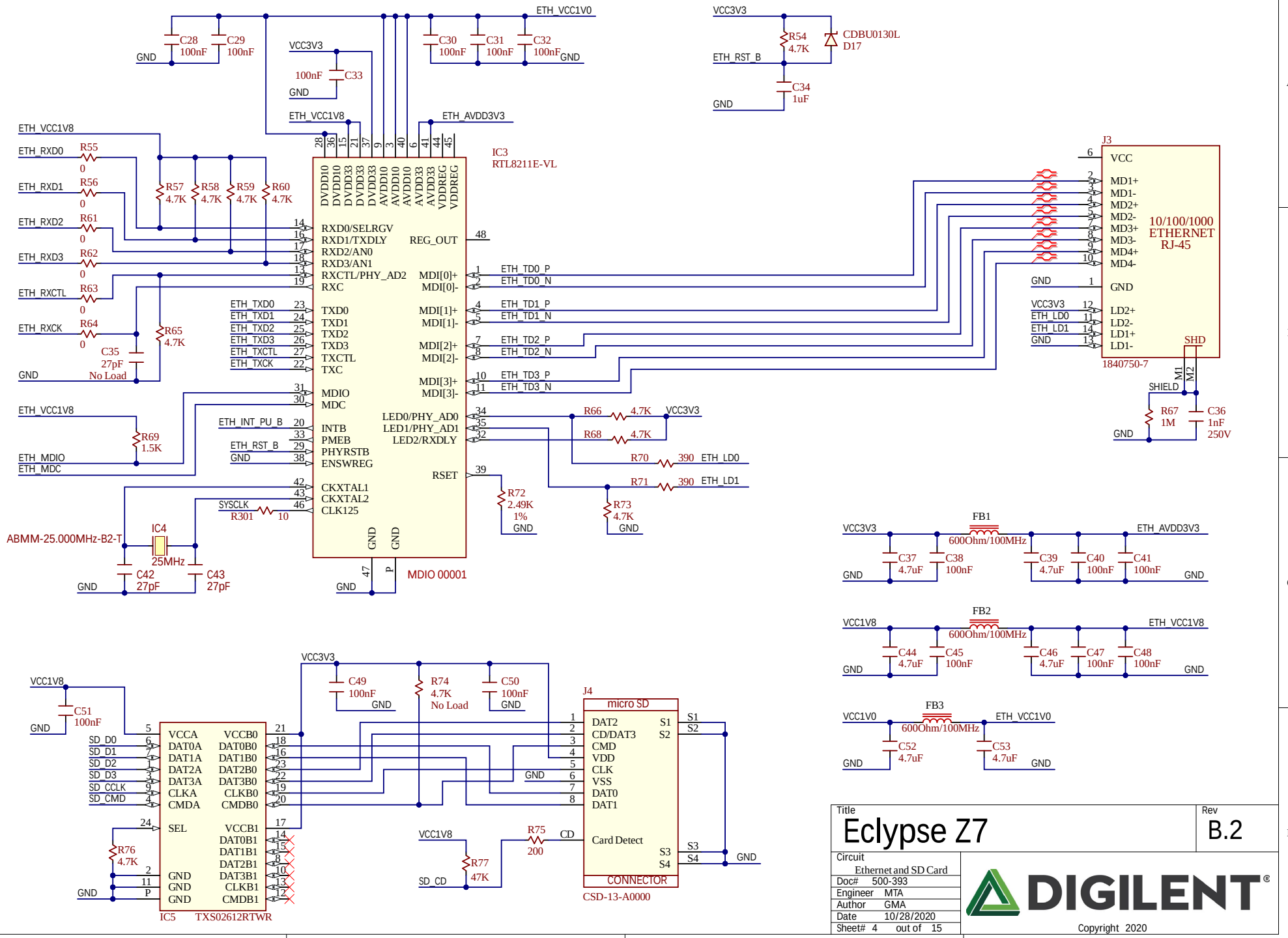


I2C ADDRESS: 0110000



I2C ADDRESS: 0110001

Title	Eclypse Z7
Rev	B.2
Circuit	SYZYGY Ports
Doc#	500-393
Engineer	MTA
Author	GMA
Date	10/28/2020
Sheet#	3 out of 15


ETH_VCC1V0
C28 100nF
C29 100nF
C30 100nF
C31 100nF
C32 100nF
GND
VCC3V3
C33 100nF
VCC3V3
R54 4.7K
CDBU0130L
D17
ETH_RST_B
C34 1uF
ETH_VCC1V8
ETH_AVDD3V3
IC3
RTL8211E-VL
DVDD10
DVDD33
AVDD10
AVDD33
VDDREG
RXD0/SELRGV
RXD1/TXDLY
RXD2/AN0
RXD3/AN1
RXCTL/PHY_AD2
RXC
REG_OUT
MDI[0]+
MDI[0]-
MDI[1]+
MDI[1]-
MDI[2]+
MDI[2]-
MDI[3]+
MDI[3]-
TXD0
TXD1
TXD2
TXD3
TXCTL
TXC
MDIO
MDC
LED0/PHY_AD0
LED1/PHY_AD1
LED2/RXDLY
INTB
PMEB
PHYRSTB
ENSWREG
RSET
CKXTAL1
CKXTAL2
CLK125
ETH_RXD0
ETH_RXD1
ETH_RXD2
ETH_RXD3
ETH_RXCTL
ETH_RXCK
R55 0
R56 0
R61 0
R62 0
R63 0
R64 0
R57 4.7K
R58 4.7K
R59 4.7K
R60 4.7K
R65 4.7K
C35 27pF No Load
ETH_TXD0
ETH_TXD1
ETH_TXD2
ETH_TXD3
ETH_TXCTL
ETH_TXCK
ETH_TD0_P
ETH_TD0_N
ETH_TD1_P
ETH_TD1_N
ETH_TD2_P
ETH_TD2_N
ETH_TD3_P
ETH_TD3_N
ETH_INT_PU_B
ETH_RST_B
ETH_MDIO
ETH_MDC
R69 1.5K
R66 4.7K
R68 4.7K
R70 390 ETH_LD0
R71 390 ETH_LD1
R72 2.49K 1%
R73 4.7K
SYSCLK
R301 10
IC4
ABMM-25.000MHz-B2-T
25MHz
C42 27pF
C43 27pF
MDIO 00001
J3
10/100/1000 ETHERNET RJ-45
1840750-7
VCC
MD1+
MD1-
MD2+
MD2-
MD3+
MD3-
MD4+
MD4-
GND
LD2+
LD2-
LD1+
LD1-
SHD
SHIELD
M1
M2
R67 1M
C36 1nF 250V
FB1
600Ohm/100MHz
C37 4.7uF
C38 100nF
C39 4.7uF
C40 100nF
C41 100nF
FB2
C44 4.7uF
C45 100nF
C46 4.7uF
C47 100nF
C48 100nF
FB3
C52 4.7uF
C53 4.7uF
C51 100nF
C49 100nF
R74 4.7K No Load
C50 100nF
IC5
TXS02612RTWR
VCCA
VCCB0
DAT0A
DAT0B0
DAT1A
DAT1B0
DAT2A
DAT2B0
DAT3A
DAT3B0
CLKA
CLKB0
CMDA
CMDB0
SEL
VCCB1
DAT0B1
DAT1B1
DAT2B1
DAT3B1
CLKB1
CMDB1
SD_D0
SD_D1
SD_D2
SD_D3
SD_CCLK
SD_CMD
R76 4.7K
J4
micro SD
DAT2
CD/DAT3
CMD
VDD
CLK
VSS
DAT0
DAT1
Card Detect
S1
S2
S3
S4
CONNECTOR
CSD-13-A0000
R75 200
CD
R77 47K
SD_CD
Title
Eclypse Z7
Rev
B.2
Circuit
Ethernet and SD Card
Doc# 500-393
Engineer MTA
Author GMA
Date 10/28/2020
Sheet# 4 out of 15
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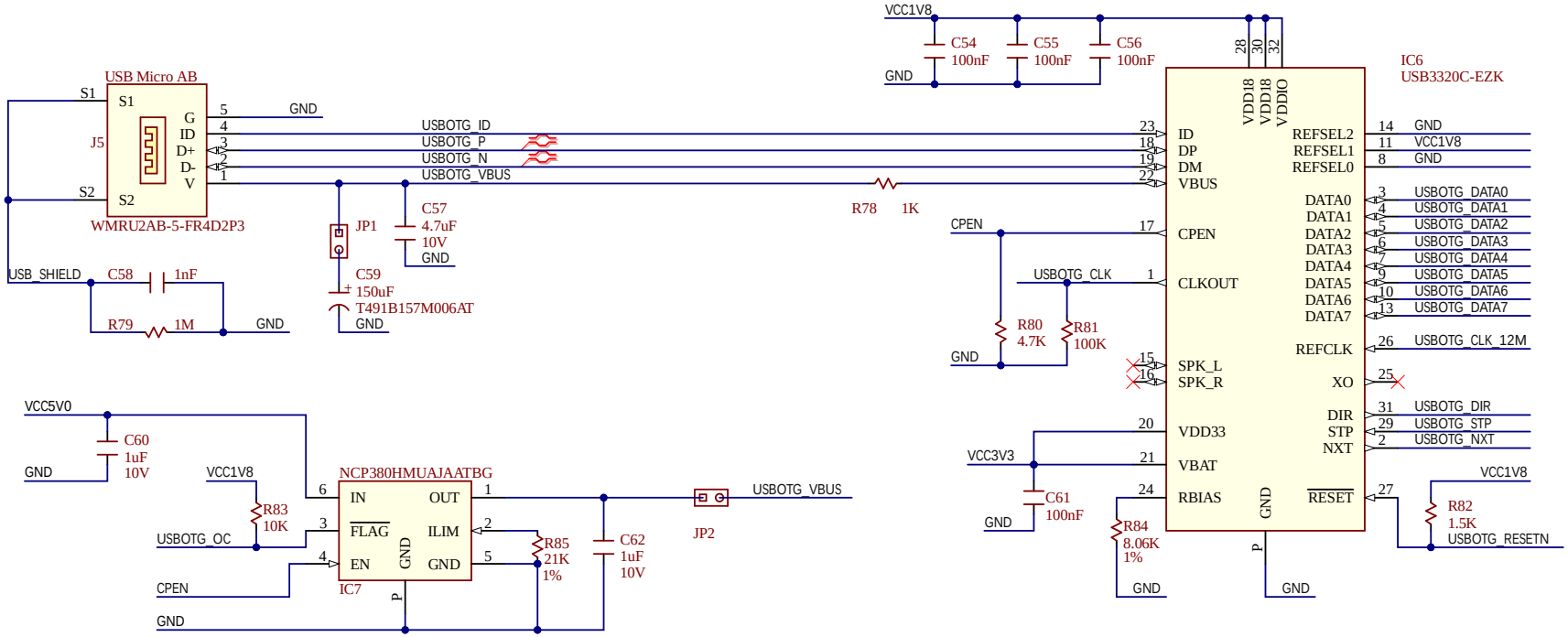
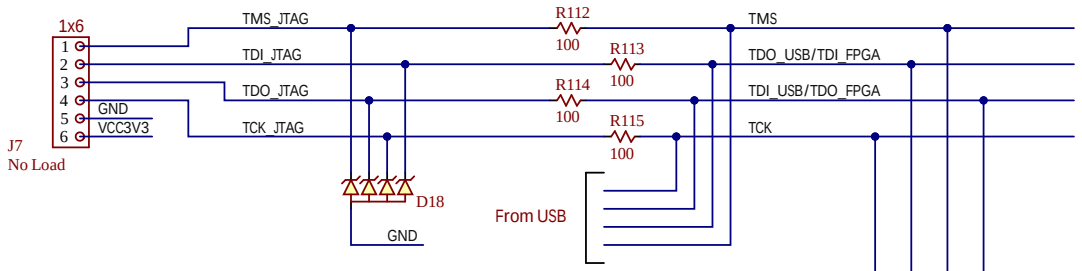
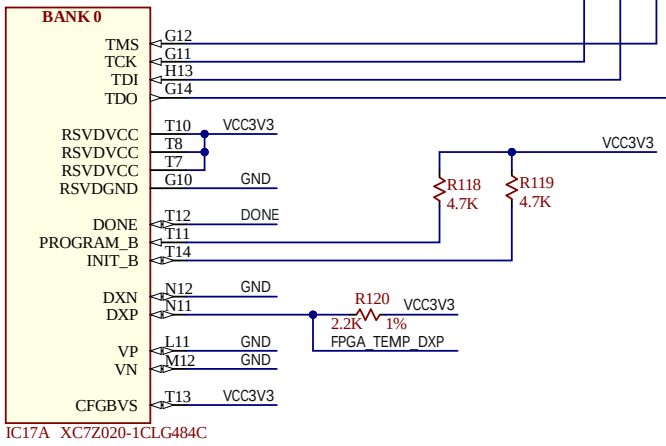
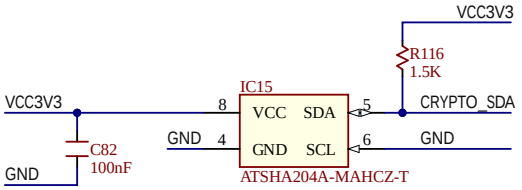
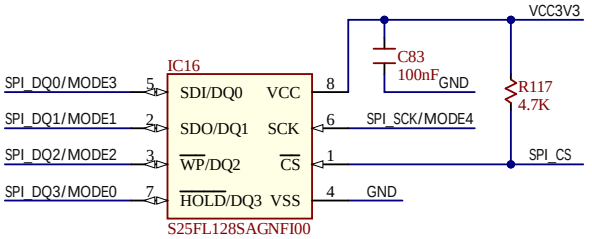


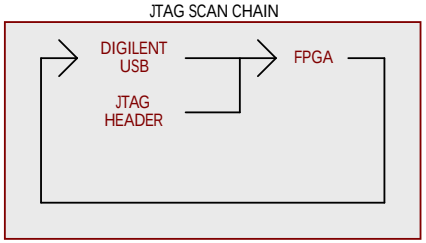
Title	Eclypse Z7
Rev	B.2
Circuit	UST OTG
Doc#	500-393
Engineer	MTA
Author	GMA
Date	10/28/2020
Sheet#	5 out of 15



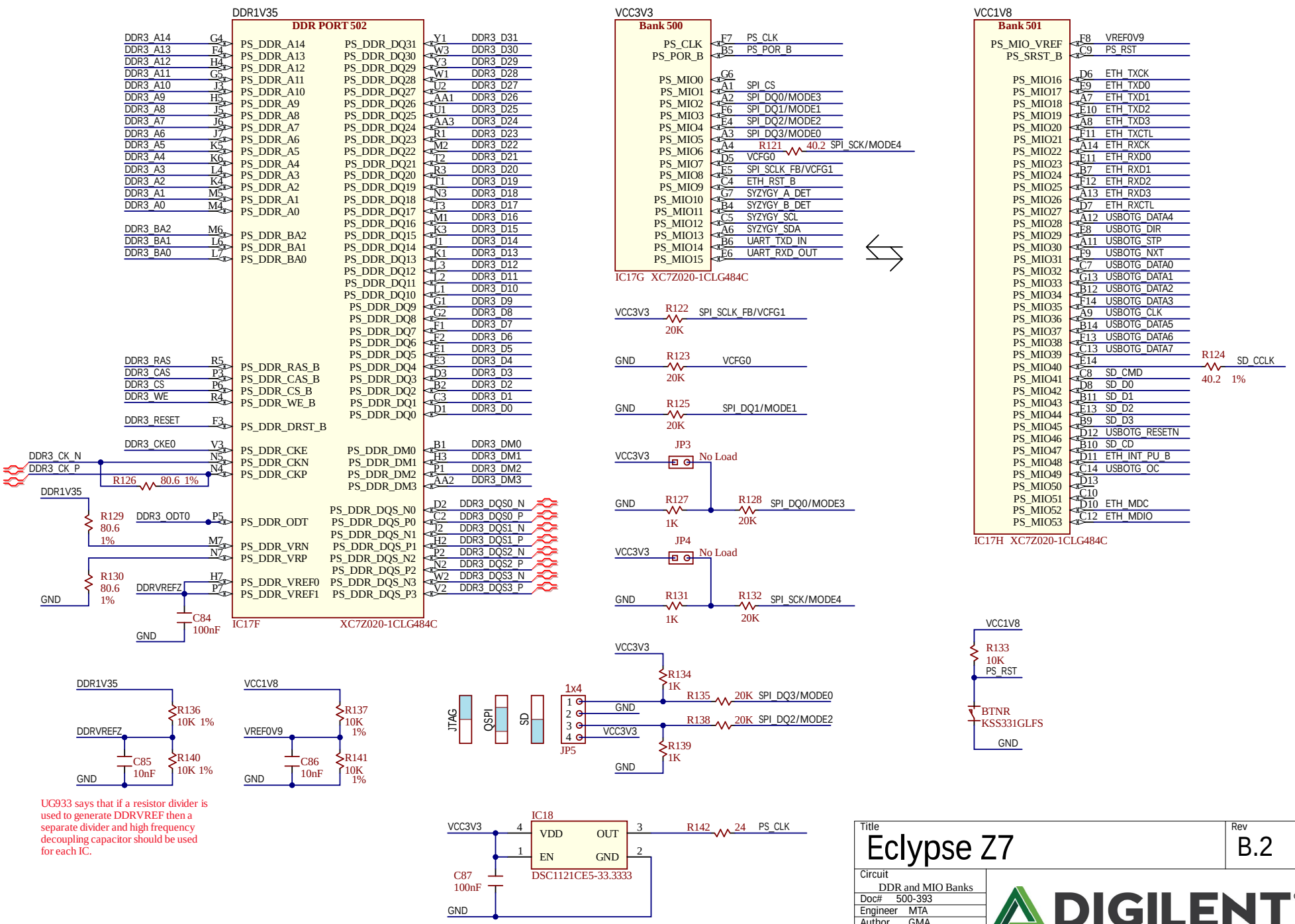








Title	Eclypse Z7
Rev	B.2
Circuit	FPGA Configuration
Doc#	500-393
Engineer	MTA
Author	GMA
Date	10/28/2020
Sheet#	6 out of 15


DDR1V35
DDR PORT 502
DDR3_A14 G4
DDR3_A13 F4
DDR3_A12 H4
DDR3_A11 G5
DDR3_A10 J3
DDR3_A9 H5
DDR3_A8 J5
DDR3_A7 J6
DDR3_A6 J7
DDR3_A5 K5
DDR3_A4 K6
DDR3_A3 L4
DDR3_A2 K4
DDR3_A1 M5
DDR3_A0 M4
DDR3_BA2 M6
DDR3_BA1 L6
DDR3_BA0 L7
DDR3_RAS R5
DDR3_CAS P3
DDR3_CS P6
DDR3_WE R4
DDR3_RESET F3
DDR3_CKE0 V3
DDR3_CK_N N5
DDR3_CK_P N4
PS_DDR_A14
PS_DDR_A13
PS_DDR_A12
PS_DDR_A11
PS_DDR_A10
PS_DDR_A9
PS_DDR_A8
PS_DDR_A7
PS_DDR_A6
PS_DDR_A5
PS_DDR_A4
PS_DDR_A3
PS_DDR_A2
PS_DDR_A1
PS_DDR_A0
PS_DDR_BA2
PS_DDR_BA1
PS_DDR_BA0
PS_DDR_RAS_B
PS_DDR_CAS_B
PS_DDR_CS_B
PS_DDR_WE_B
PS_DDR_DRST_B
PS_DDR_CKE
PS_DDR_CKN
PS_DDR_CKP
PS_DDR_ODT
PS_DDR_VRN
PS_DDR_VRP
PS_DDR_VREF0
PS_DDR_VREF1
PS_DDR_DQ31 Y1 DDR3_D31
PS_DDR_DQ30 W3 DDR3_D30
PS_DDR_DQ29 Y3 DDR3_D29
PS_DDR_DQ28 W1 DDR3_D28
PS_DDR_DQ27 U2 DDR3_D27
PS_DDR_DQ26 AA1 DDR3_D26
PS_DDR_DQ25 U1 DDR3_D25
PS_DDR_DQ24 AA3 DDR3_D24
PS_DDR_DQ23 R1 DDR3_D23
PS_DDR_DQ22 M2 DDR3_D22
PS_DDR_DQ21 T2 DDR3_D21
PS_DDR_DQ20 R3 DDR3_D20
PS_DDR_DQ19 T1 DDR3_D19
PS_DDR_DQ18 N3 DDR3_D18
PS_DDR_DQ17 T3 DDR3_D17
PS_DDR_DQ16 M1 DDR3_D16
PS_DDR_DQ15 K3 DDR3_D15
PS_DDR_DQ14 J1 DDR3_D14
PS_DDR_DQ13 K1 DDR3_D13
PS_DDR_DQ12 L3 DDR3_D12
PS_DDR_DQ11 L2 DDR3_D11
PS_DDR_DQ10 L1 DDR3_D10
PS_DDR_DQ9 G1 DDR3_D9
PS_DDR_DQ8 G2 DDR3_D8
PS_DDR_DQ7 F1 DDR3_D7
PS_DDR_DQ6 F2 DDR3_D6
PS_DDR_DQ5 E1 DDR3_D5
PS_DDR_DQ4 E3 DDR3_D4
PS_DDR_DQ3 D3 DDR3_D3
PS_DDR_DQ2 B2 DDR3_D2
PS_DDR_DQ1 C3 DDR3_D1
PS_DDR_DQ0 D1 DDR3_D0
PS_DDR_DM0 B1 DDR3_DM0
PS_DDR_DM1 H3 DDR3_DM1
PS_DDR_DM2 P1 DDR3_DM2
PS_DDR_DM3 AA2 DDR3_DM3
PS_DDR_DQS_N0 D2 DDR3_DQS0_N
PS_DDR_DQS_P0 C2 DDR3_DQS0_P
PS_DDR_DQS_N1 J2 DDR3_DQS1_N
PS_DDR_DQS_P1 H2 DDR3_DQS1_P
PS_DDR_DQS_N2 P2 DDR3_DQS2_N
PS_DDR_DQS_P2 N2 DDR3_DQS2_P
PS_DDR_DQS_N3 W2 DDR3_DQS3_N
PS_DDR_DQS_P3 V2 DDR3_DQS3_P
IC17F XC7Z020-1CLG484C
R126 80.6 1%
R129 80.6 1%
R130 80.6 1%
C84 100nF
DDR3_ODT0 P5
DDRVREFZ H7
VCC3V3
Bank 500
PS_CLK F7 PS_CLK
PS_POR_B B5 PS_POR_B
PS_MIO0 G6
PS_MIO1 A1 SPI_CS
PS_MIO2 A2 SPI_DQ0/MODE3
PS_MIO3 F6 SPI_DQ1/MODE1
PS_MIO4 E4 SPI_DQ2/MODE2
PS_MIO5 A3 SPI_DQ3/MODE0
PS_MIO6 A4 R121 40.2 SPI_SCK/MODE4
PS_MIO7 D5 VCFG0
PS_MIO8 E5 SPI_SCLK_FB/VCFG1
PS_MIO9 C4 ETH_RST_B
PS_MIO10 G7 SYZYGY_A_DET
PS_MIO11 B4 SYZYGY_B_DET
PS_MIO12 C5 SYZYGY_SCL
PS_MIO13 A6 SYZYGY_SDA
PS_MIO14 B6 UART_TXD_IN
PS_MIO15 E6 UART_RXD_OUT
IC17G XC7Z020-1CLG484C
VCC1V8
Bank 501
PS_MIO_VREF F8 VREF0V9
PS_SRST_B C9 PS_RST
PS_MIO16 D6 ETH_TXCK
PS_MIO17 E9 ETH_TXD0
PS_MIO18 A7 ETH_TXD1
PS_MIO19 E10 ETH_TXD2
PS_MIO20 A8 ETH_TXD3
PS_MIO21 F11 ETH_TXCTL
PS_MIO22 A14 ETH_RXCK
PS_MIO23 E11 ETH_RXD0
PS_MIO24 B7 ETH_RXD1
PS_MIO25 F12 ETH_RXD2
PS_MIO26 A13 ETH_RXD3
PS_MIO27 D7 ETH_RXCTL
PS_MIO28 A12 USBOTG_DATA4
PS_MIO29 E8 USBOTG_DIR
PS_MIO30 A11 USBOTG_STP
PS_MIO31 F9 USBOTG_NXT
PS_MIO32 C7 USBOTG_DATA0
PS_MIO33 G13 USBOTG_DATA1
PS_MIO34 B12 USBOTG_DATA2
PS_MIO35 F14 USBOTG_DATA3
PS_MIO36 A9 USBOTG_CLK
PS_MIO37 B14 USBOTG_DATA5
PS_MIO38 F13 USBOTG_DATA6
PS_MIO39 C13 USBOTG_DATA7
PS_MIO40 E14 R124 40.2 1% SD_CCLK
PS_MIO41 C8 SD_CMD
PS_MIO42 D8 SD_D0
PS_MIO43 B11 SD_D1
PS_MIO44 E13 SD_D2
PS_MIO45 B9 SD_D3
PS_MIO46 D12 USBOTG_RESETN
PS_MIO47 B10 SD_CD
PS_MIO48 D11 ETH_INT_PU_B
PS_MIO49 C14 USBOTG_OC
PS_MIO50 D13
PS_MIO51 C10
PS_MIO52 D10 ETH_MDC
PS_MIO53 C12 ETH_MDIO
IC17H XC7Z020-1CLG484C
R122 20K SPI_SCLK_FB/VCFG1
R123 20K VCFG0
R125 20K SPI_DQ1/MODE1
JP3 No Load
R127 1K
R128 20K SPI_DQ0/MODE3
JP4 No Load
R131 1K
R132 20K SPI_SCK/MODE4
R133 10K PS_RST
BTNR KSS331GLFS
R134 1K
R135 20K SPI_DQ3/MODE0
R138 20K SPI_DQ2/MODE2
R139 1K
JTAG
QSPI
SD
1x4
JP5
R136 10K 1%
R140 10K 1%
C85 10nF
R137 10K 1%
R141 10K 1%
C86 10nF
UG933 says that if a resistor divider is used to generate DDRVREF then a separate divider and high frequency decoupling capacitor should be used for each IC.
IC18
VDD
OUT
EN
GND
DSC1121CE5-33.3333
C87 100nF
R142 24 PS_CLK
GND
Title
Eclypse Z7
Rev
B.2
Circuit
DDR and MIO Banks
Doc# 500-393
Engineer MTA
Author GMA
Date 10/28/2020
Sheet# 7 out of 15
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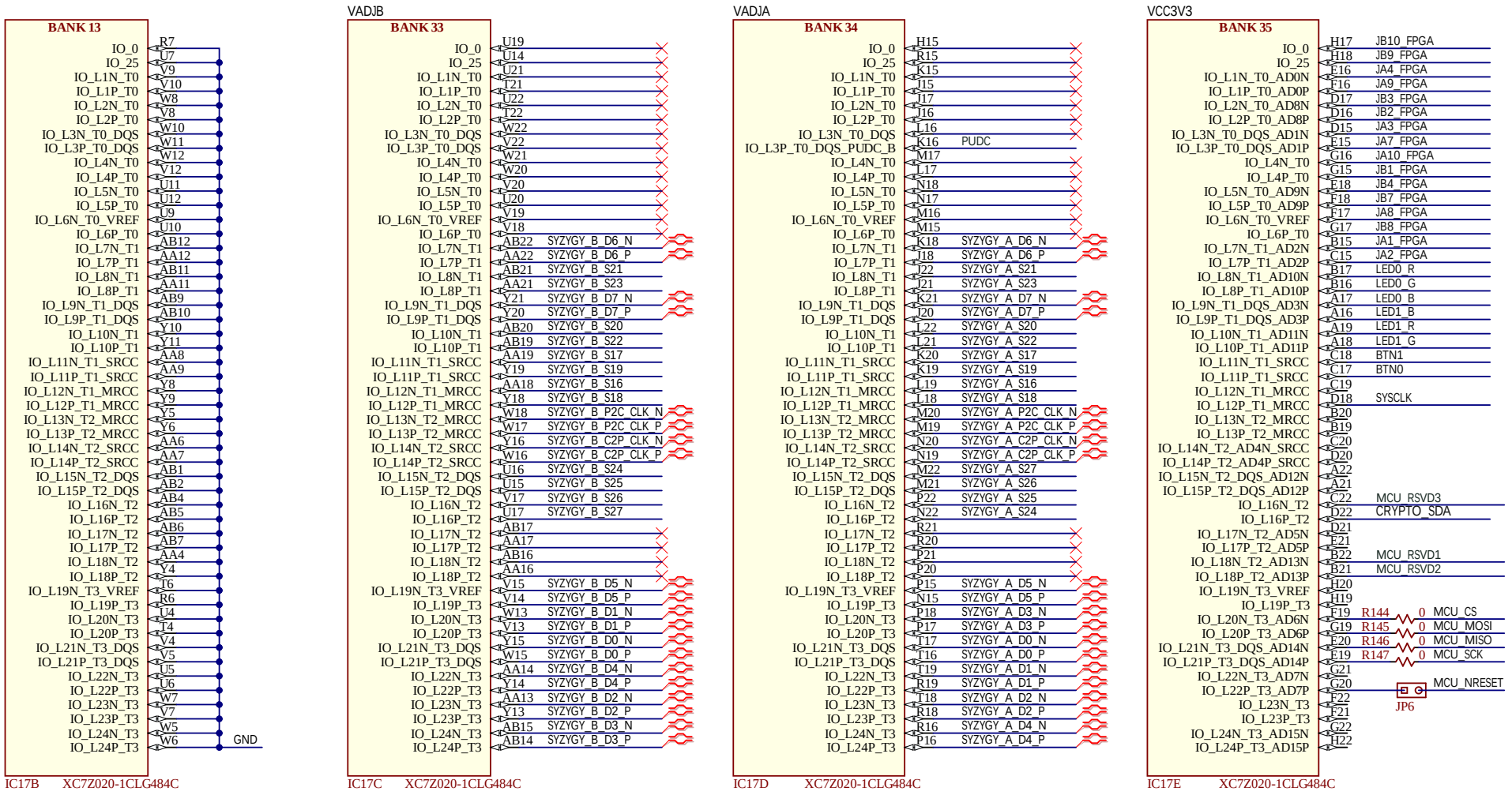

Title	Eclypse Z7
Rev	B.2
Circuit	FPGA Banks
Doc#	500-393
Engineer	MTA
Author	GMA
Date	10/28/2020
Sheet#	8 out of 15

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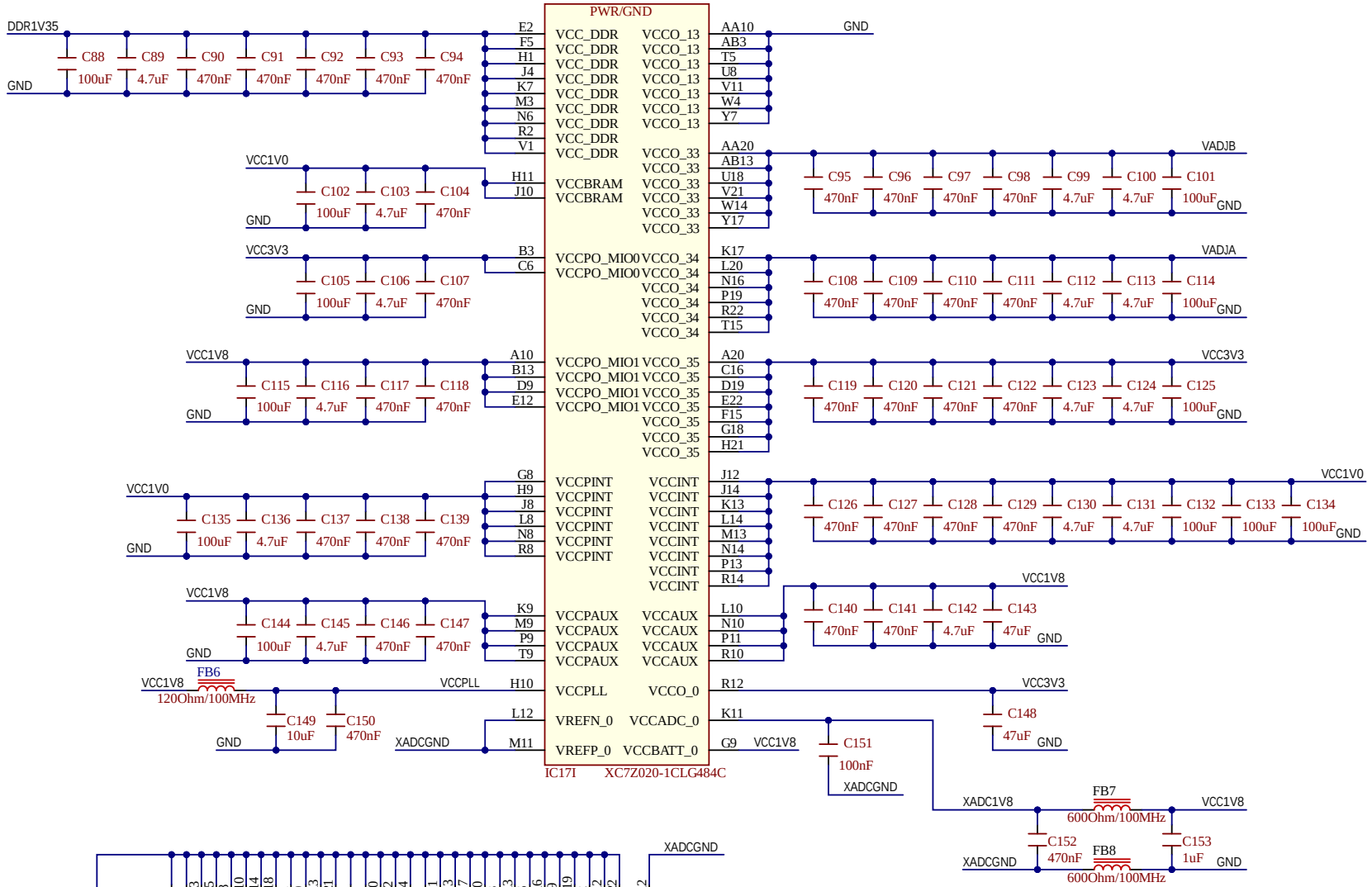
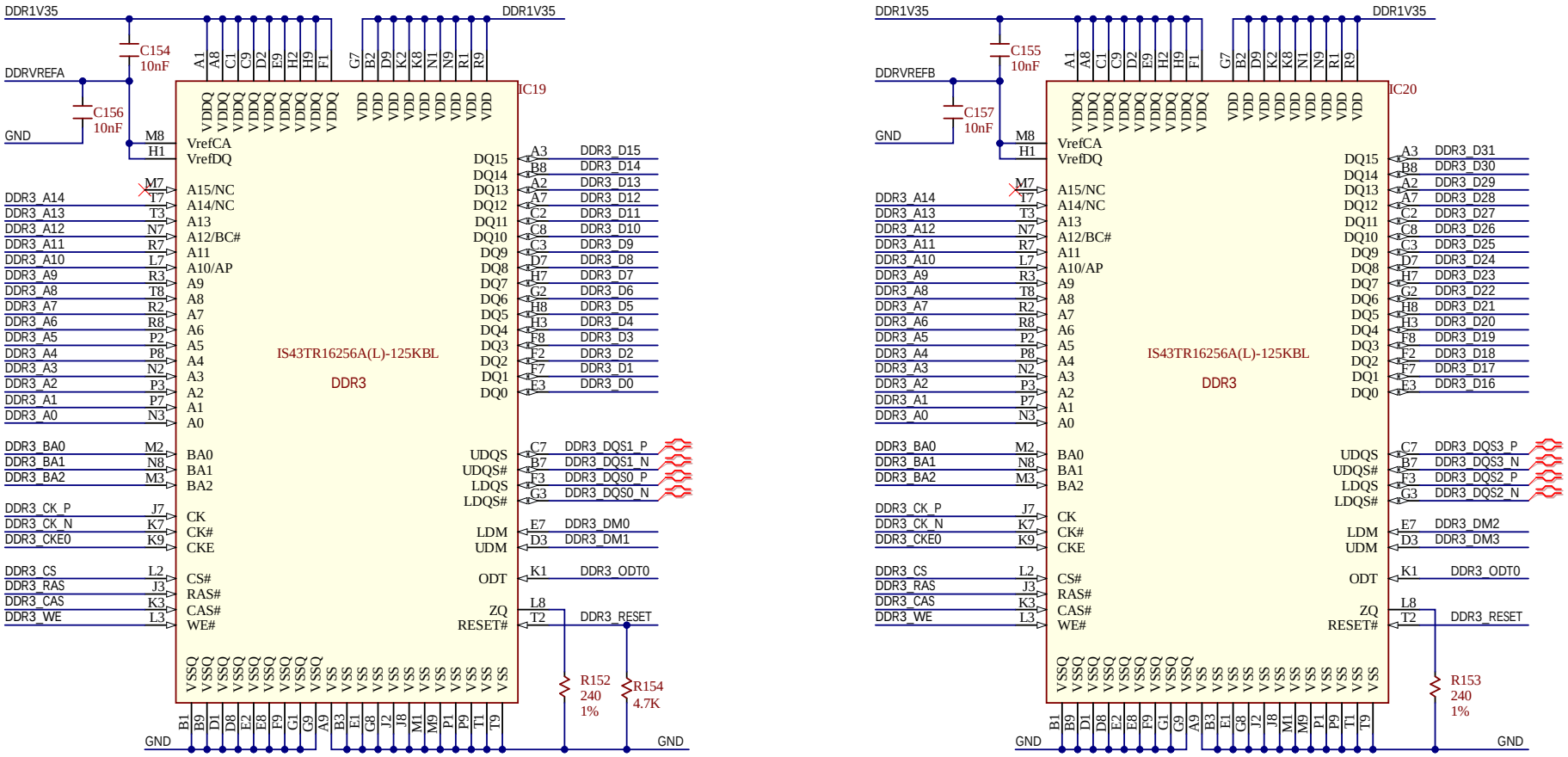
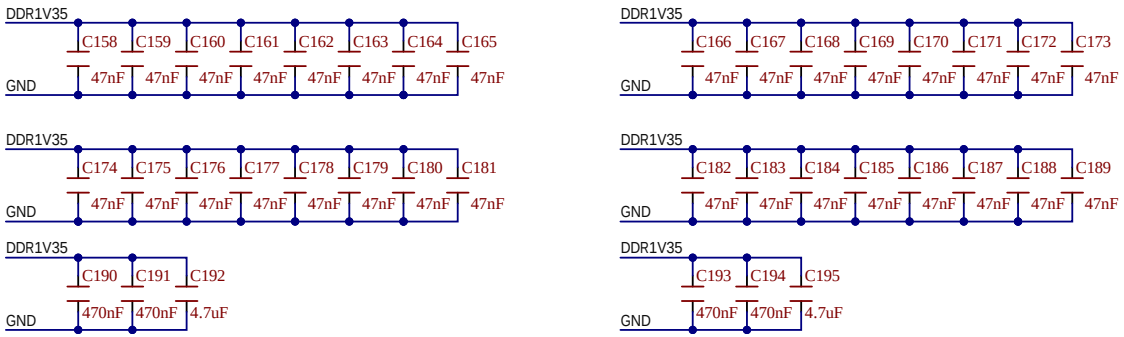


Title	Eclypse Z7
Rev	B.2
Circuit	FPGA Power
Doc#	500-393
Engineer	MTA
Author	GMA
Date	10/28/2020
Sheet#	9 out of 15



NOTE: Please select Micron MT41K256M16 RE-125 as the Memory Part in the Vivado DDR Configuration.



Title	Eclypse Z7
Rev	B.2
Circuit	DDR3L Memory
Doc#	500-393
Engineer	MTA
Author	GMA
Date	10/28/2020
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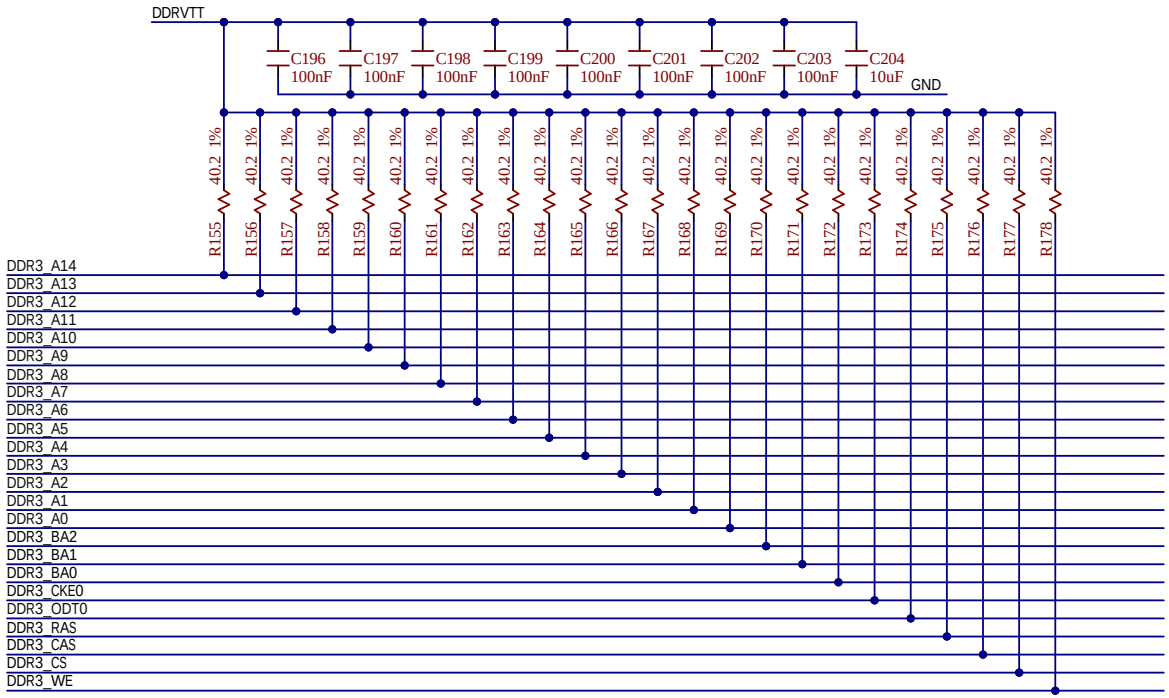
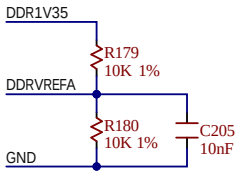
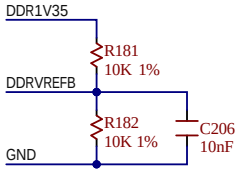
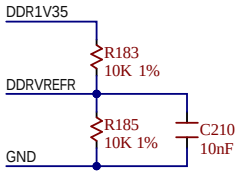
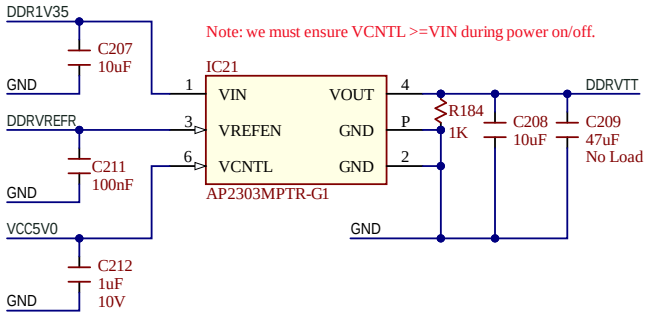


UG933 says that if a resistor divider is used to generate DDRVREF then a separate divider and high frequency decoupling capacitor should be used for each IC.









Title	Eclypse Z7
Rev	B.2
Circuit	DDR3L Termination
Doc#	500-393
Engineer	MTA
Author	GMA
Date	10/28/2020
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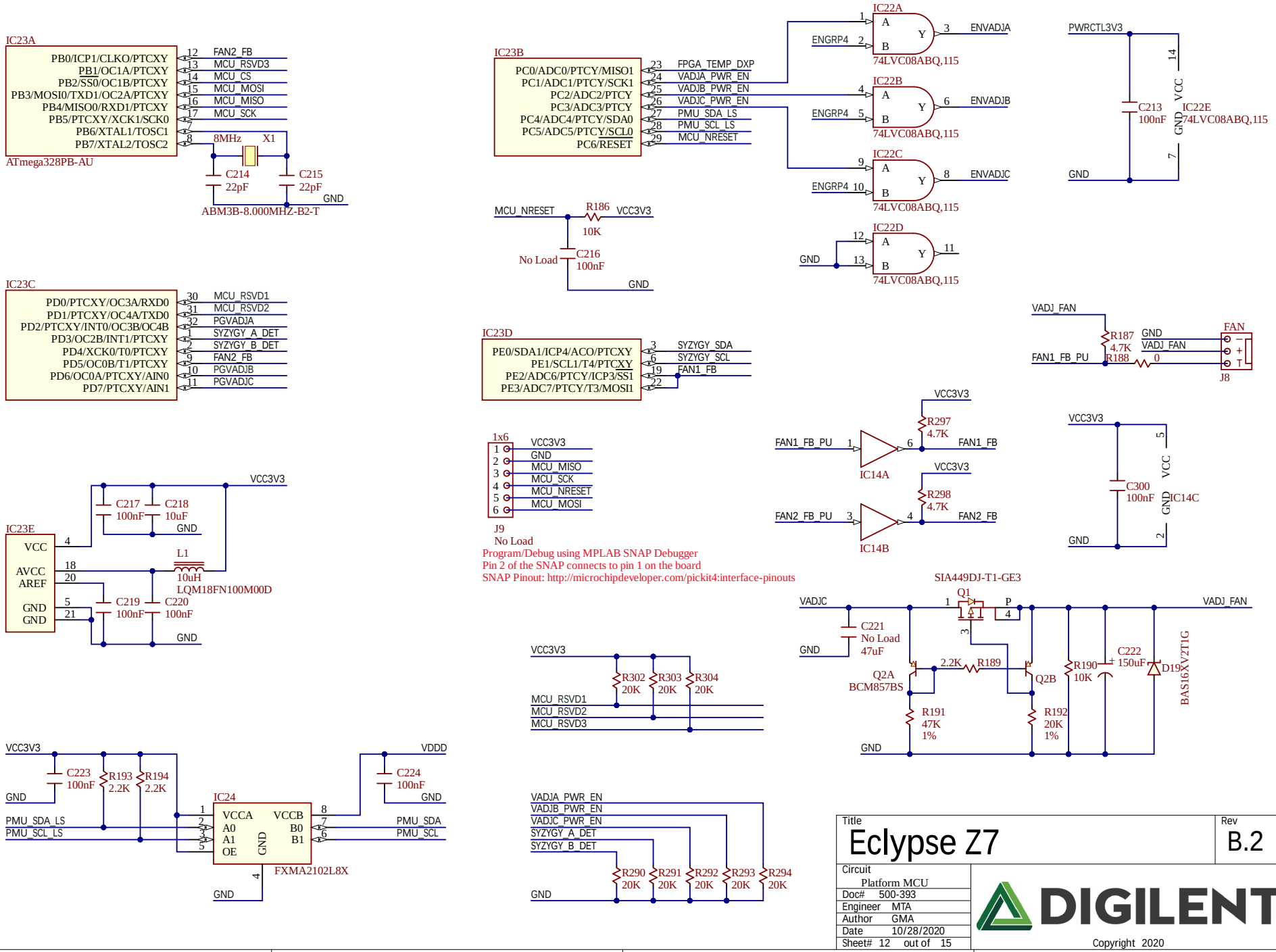
IC23A
PB0/ICP1/CLKO/PTCXY
PB1/OC1A/PTCXY
PB2/SS0/OC1B/PTCXY
PB3/MOSI0/TXD1/OC2A/PTCXY
PB4/MISO0/RXD1/PTCXY
PB5/PTCXY/XCK1/SCK0
PB6/XTAL1/TOSC1
PB7/XTAL2/TOSC2
ATmega328PB-AU
FAN2_FB
MCU_RSVD3
MCU_CS
MCU_MOSI
MCU_MISO
MCU_SCK
8MHz
X1
C214
22pF
C215
22pF
GND
ABM3B-8.000MHZ-B2-T
IC23B
PC0/ADC0/PTCY/MISO1
PC1/ADC1/PTCY/SCK1
PC2/ADC2/PTCY
PC3/ADC3/PTCY
PC4/ADC4/PTCY/SDA0
PC5/ADC5/PTCY/SCL0
PC6/RESET
FPGA_TEMP_DXP
VADJA_PWR_EN
VADJB_PWR_EN
VADJC_PWR_EN
PMU_SDA_LS
PMU_SCL_LS
MCU_NRESET
IC22A
ENGRP4
ENVADJA
74LVC08ABQ,115
IC22B
ENGRP4
ENVADJB
74LVC08ABQ,115
IC22C
ENGRP4
ENVADJC
74LVC08ABQ,115
IC22D
GND
74LVC08ABQ,115
PWRCTL3V3
C213
100nF
VCC
GND
IC22E
74LVC08ABQ,115
GND
MCU_NRESET
R186
10K
VCC3V3
No Load
C216
100nF
GND
IC23C
PD0/PTCXY/OC3A/RXD0
PD1/PTCXY/OC4A/TXD0
PD2/PTCXY/INT0/OC3B/OC4B
PD3/OC2B/INT1/PTCXY
PD4/XCK0/T0/PTCXY
PD5/OC0B/T1/PTCXY
PD6/OC0A/PTCXY/AIN0
PD7/PTCXY/AIN1
MCU_RSVD1
MCU_RSVD2
PGVADJA
SYZYGY_A_DET
SYZYGY_B_DET
FAN2_FB
PGVADJB
PGVADJC
IC23D
PE0/SDA1/ICP4/ACO/PTCXY
PE1/SCL1/T4/PTCXY
PE2/ADC6/PTCY/ICP3/SS1
PE3/ADC7/PTCY/T3/MOSI1
SYZYGY_SDA
SYZYGY_SCL
FAN1_FB
VADJ_FAN
R187
4.7K
R188
FAN1_FB_PU
GND
VADJ_FAN
0
FAN
J8
1x6
VCC3V3
GND
MCU_MISO
MCU_SCK
MCU_NRESET
MCU_MOSI
J9
No Load
Program/Debug using MPLAB SNAP Debugger
Pin 2 of the SNAP connects to pin 1 on the board
SNAP Pinout: http://microchipdeveloper.com/pickit4:interface-pinouts
VCC3V3
R297
4.7K
FAN1_FB_PU
FAN1_FB
IC14A
VCC3V3
R298
4.7K
FAN2_FB_PU
FAN2_FB
IC14B
VCC3V3
C300
100nF
VCC
GND
IC14C
GND
IC23E
VCC
AVCC
AREF
GND
GND
C217
100nF
C218
10uF
GND
L1
10uH
LQM18FN100M00D
C219
100nF
C220
100nF
GND
VCC3V3
SIA449DJ-T1-GE3
Q1
VADJC
C221
No Load
47uF
GND
2.2K
R189
Q2A
BCM857BS
Q2B
R190
10K
C222
150uF
D19
BAS16XV2T1G
VADJ_FAN
R191
47K
1%
R192
20K
1%
GND
VCC3V3
R302
20K
R303
20K
R304
20K
MCU_RSVD1
MCU_RSVD2
MCU_RSVD3
VCC3V3
C223
100nF
R193
2.2K
R194
2.2K
GND
PMU_SDA_LS
PMU_SCL_LS
IC24
VCCA
A0
A1
OE
GND
VCCB
B0
B1
FXMA2102L8X
VDDD
C224
100nF
GND
PMU_SDA
PMU_SCL
GND
VADJA_PWR_EN
VADJB_PWR_EN
VADJC_PWR_EN
SYZYGY_A_DET
SYZYGY_B_DET
R290
20K
R291
20K
R292
20K
R293
20K
R294
20K
GND
Title
Eclypse Z7
Rev
B.2
Circuit
Platform MCU
Doc# 500-393
Engineer MTA
Author GMA
Date 10/28/2020
Sheet# 12 out of 15
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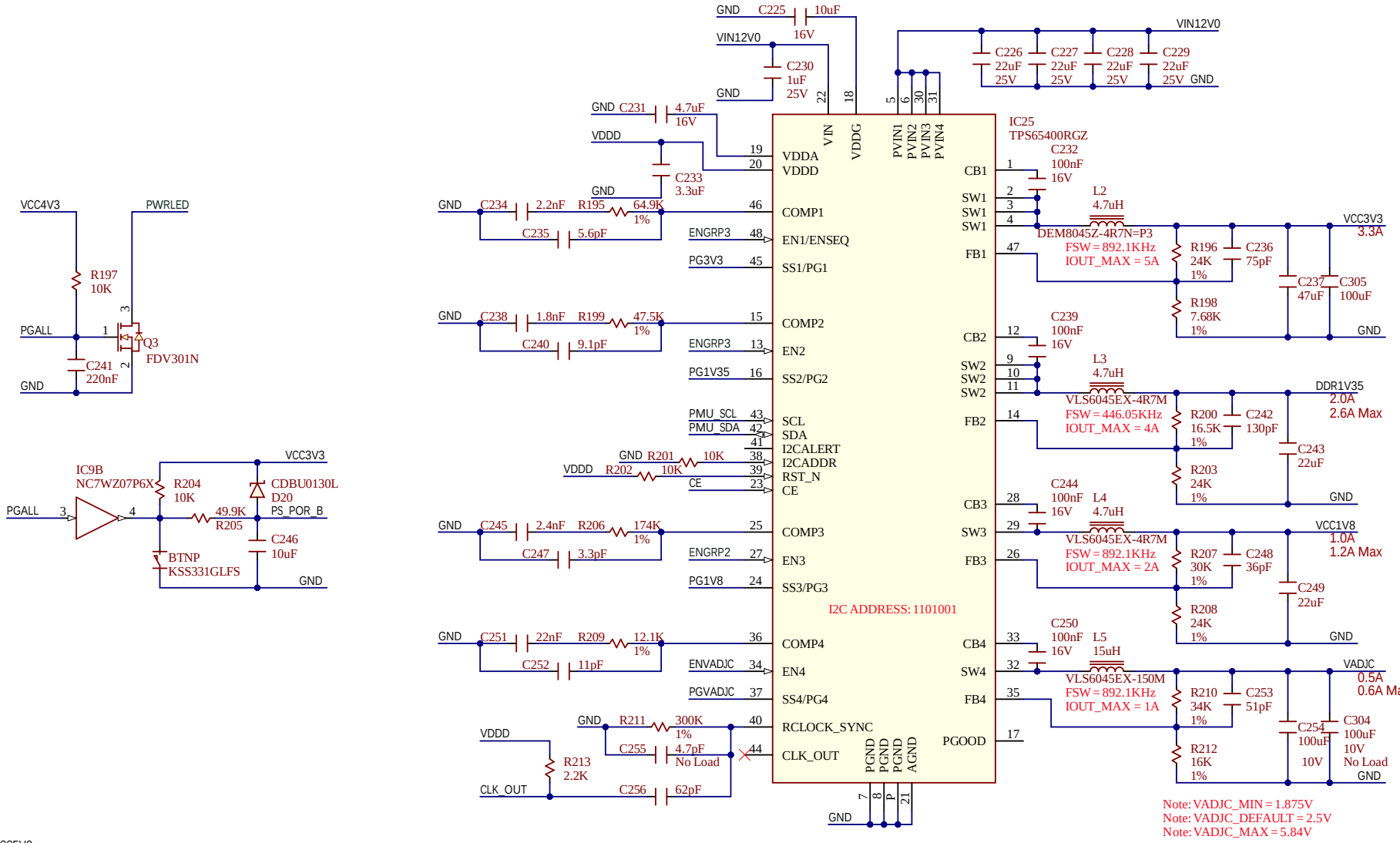

Title	Eclypse Z7
Rev	B.2
Circuit	Power Regulation
Doc#	500-393
Engineer	MTA
Author	GMA
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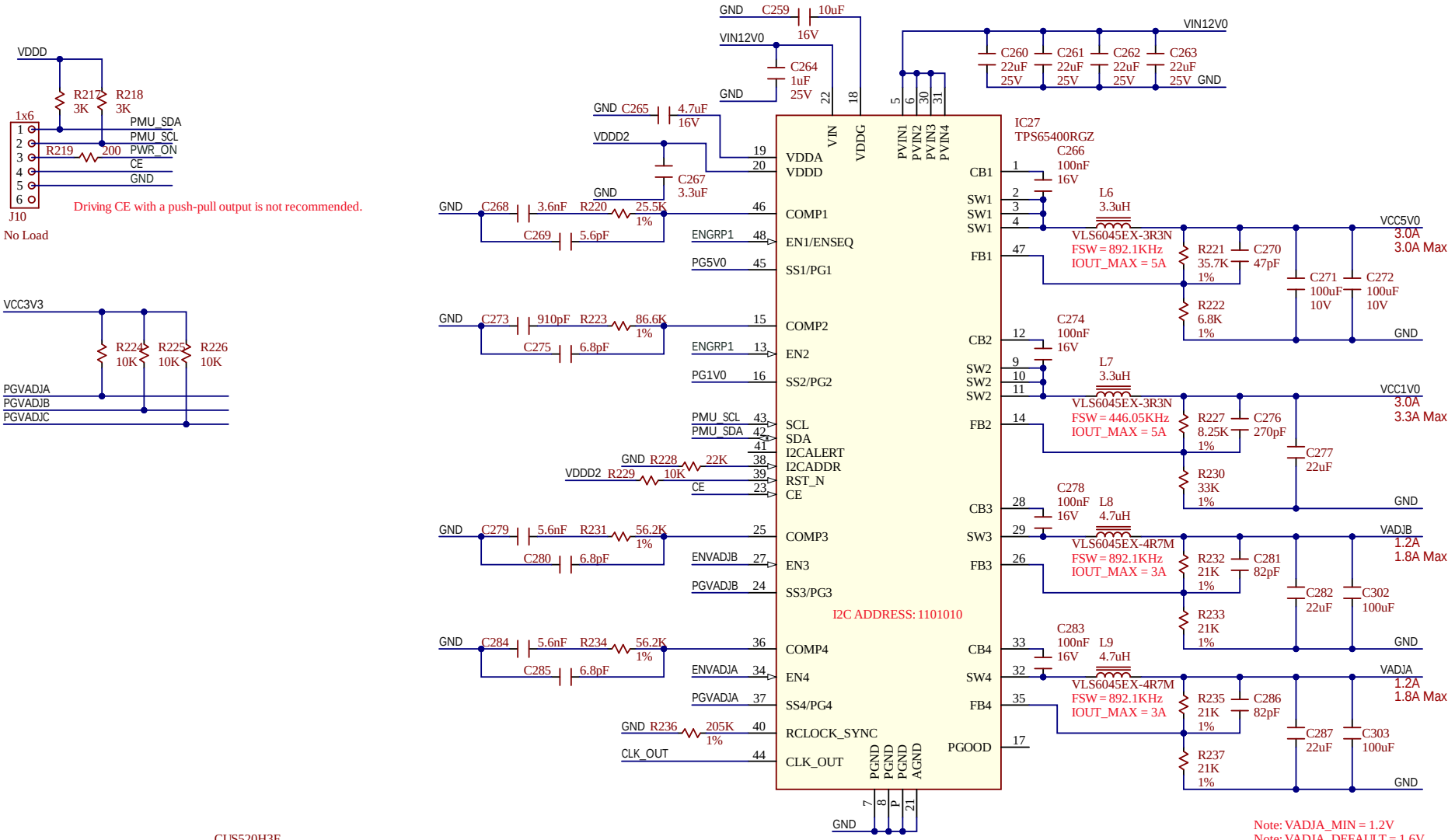

Title	Eclypse Z7
Rev	B.2
Circuit	Power Regulation
Doc#	500-393
Engineer	MTA
Author	GMA
Date	10/28/2020
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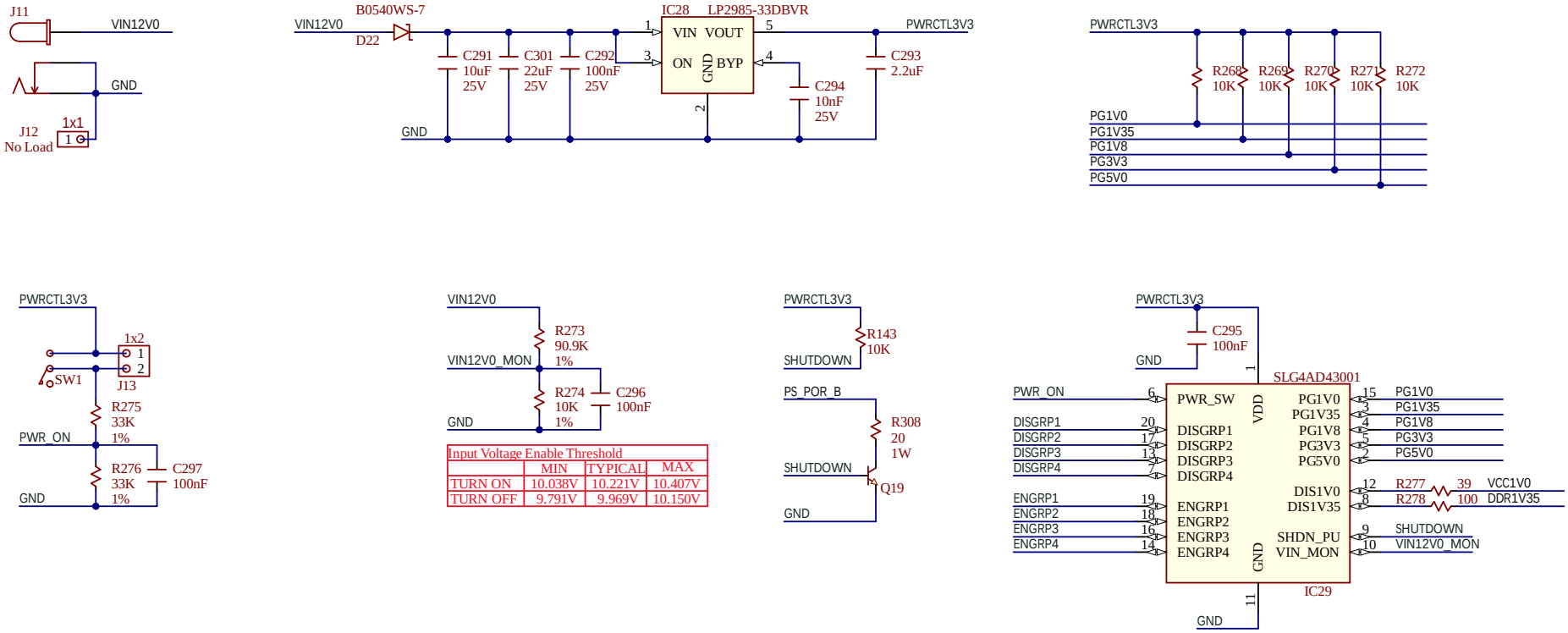
Note: Input Voltage 12V only!



Input Voltage Enable Threshold			
	MIN	TYPICAL	MAX
TURN ON	10.038V	10.221V	10.407V
TURN OFF	9.791V	9.969V	10.150V

Title	Eclypse Z7
Rev	B.2
Circuit	Regulation and Sequencer
Doc#	500-393
Engineer	MTA
Author	GMA
Date	10/28/2020
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