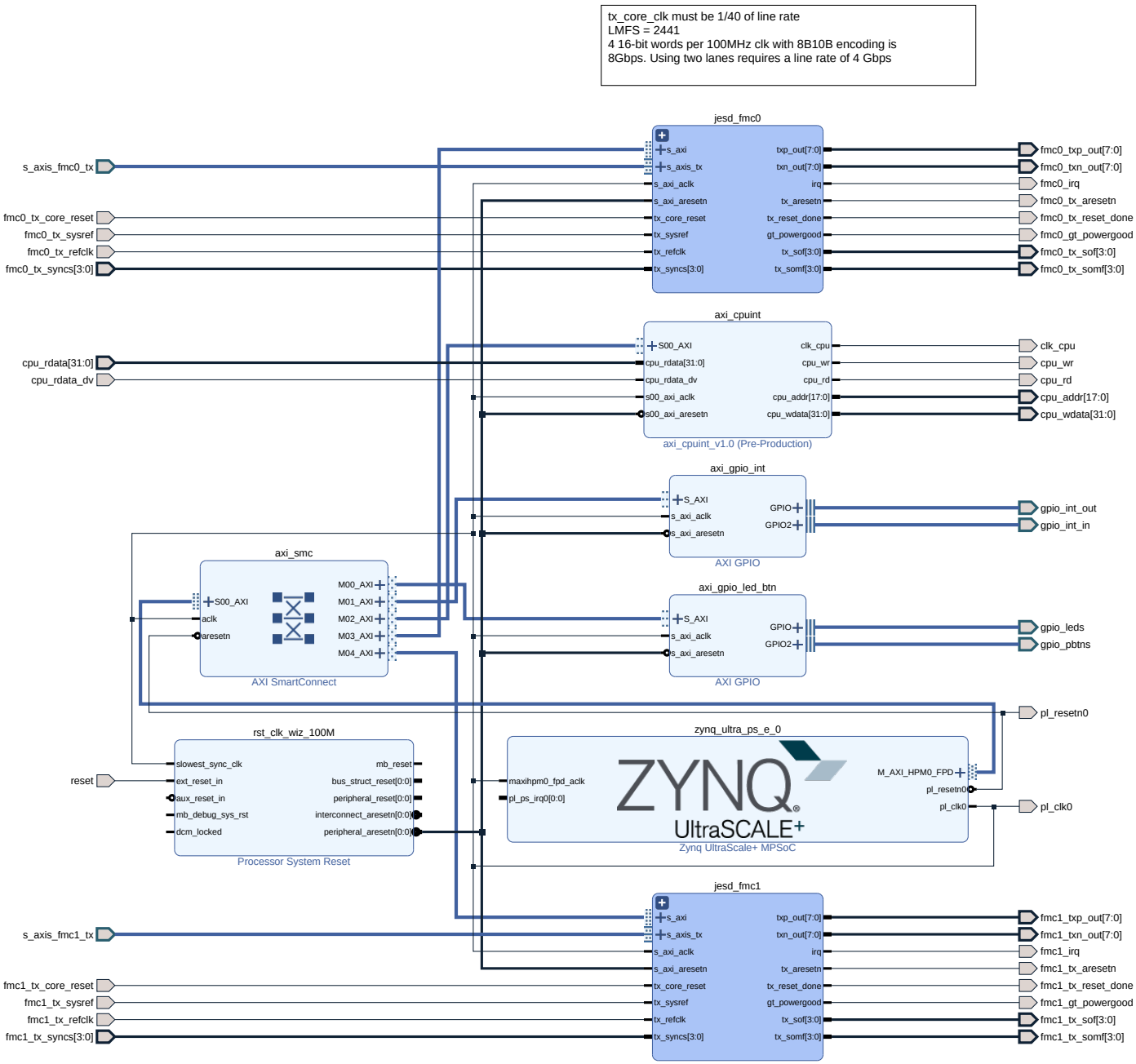
tx_core_clk must be 1/40 of line rate
LMFS = 2441
4 16-bit words per 100MHz clk with 8B10B encoding is
8Gbps. Using two lanes requires a line rate of 4 Gbps
jesd_fmc0
s_axi_fmc0_tx
fmc0_tx_core_reset
fmc0_tx_sysref
fmc0_tx_refclk
fmc0_tx_syncs[3:0]
s_axi
s_axis_tx
s_axi_aclk
s_axi_aresetn
tx_core_reset
tx_sysref
tx_refclk
tx_syncs[3:0]
txp_out[7:0]
txn_out[7:0]
irq
tx_aresetn
tx_reset_done
gt_powergood
tx_sof[3:0]
tx_somf[3:0]
fmc0_txp_out[7:0]
fmc0_txn_out[7:0]
fmc0_irq
fmc0_tx_aresetn
fmc0_tx_reset_done
fmc0_gt_powergood
fmc0_tx_sof[3:0]
fmc0_tx_somf[3:0]
axi_cpuint
cpu_rdata[31:0]
cpu_rdata_dv
S00_AXI
cpu_rdata[31:0]
cpu_rdata_dv
s00_axi_aclk
s00_axi_aresetn
clk_cpu
cpu_wr
cpu_rd
cpu_addr[17:0]
cpu_wdata[31:0]
clk_cpu
cpu_wr
cpu_rd
cpu_addr[17:0]
cpu_wdata[31:0]
axi_cpuint_v1.0 (Pre-Production)
axi_gpio_int
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
GPIO2
gpio_int_out
gpio_int_in
AXI GPIO
axi_smc
S00_AXI
aclk
aresetn
M00_AXI
M01_AXI
M02_AXI
M03_AXI
M04_AXI
AXI SmartConnect
axi_gpio_led_btn
S_AXI
s_axi_aclk
s_axi_aresetn
GPIO
GPIO2
gpio_leds
gpio_pbtns
AXI GPIO
pl_resetn0
rst_clk_wiz_100M
reset
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
zynq_ultra_ps_e_0
maxihpm0_fpd_aclk
pl_ps_irq0[0:0]
ZYNQ
UltraSCALE+
M_AXI_HPM0_FPD
pl_resetn0
pl_clk0
Zynq UltraScale+ MPSoC
pl_clk0
jesd_fmc1
s_axi_fmc1_tx
fmc1_tx_core_reset
fmc1_tx_sysref
fmc1_tx_refclk
fmc1_tx_syncs[3:0]
s_axi
s_axis_tx
s_axi_aclk
s_axi_aresetn
tx_core_reset
tx_sysref
tx_refclk
tx_syncs[3:0]
txp_out[7:0]
txn_out[7:0]
irq
tx_aresetn
tx_reset_done
gt_powergood
tx_sof[3:0]
tx_somf[3:0]
fmc1_txp_out[7:0]
fmc1_txn_out[7:0]
fmc1_irq
fmc1_tx_aresetn
fmc1_tx_reset_done
fmc1_gt_powergood
fmc1_tx_sof[3:0]
fmc1_tx_somf[3:0]