Understanding JESD204B Link Parameters

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The digital interface of high-speed data converters is beginning to make the transition from LVDS over to JESD204B. This interface was released in its original form, JESD204, in 2006, revised to JESD204A in 2008, and revised once more in August 2011 to the current JESD204B. The interface brings efficiency and offers several advantages over its CMOS and LVDS predecessors in terms of speed, size, and cost.

Designs employing JESD204B enjoy the benefits of a faster interface to keep pace with the faster sampling rates of converters. There is a reduction in pin count, which leads to smaller packages, less trace routes, and lowers overall system cost. The standard applies to both analog-to-digital converters (ADCs) as well as digital-to-analog converters (DACs) and is primarily intended as a common interface to field programmable gate arrays (FPGAs) — for example, the Xilinx Kintex or Vertex platforms — but may also be used with ASICs.

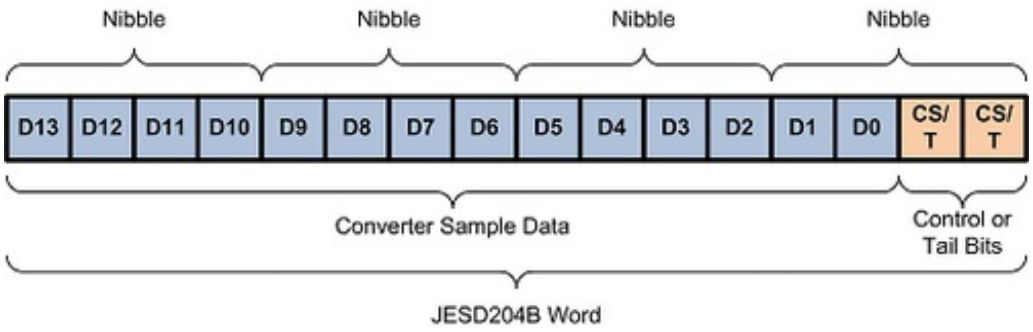
JESD204B differs from its predecessors in upfront complexity due to the new terms and parameters that it introduces. Specifically, there are link parameters that define the characteristics of the link. A closer examination of these parameters provides great insight into the structure of the link. Understanding the link parameters helps provide a better understanding of how a link is structured based on converter properties, lane count and speed, and receiver capabilities.

Converters, resolution, and what's the word?

The most logical place to begin is with the *M* and *N* parameters. M is the number of converters per converter device (or package or IC), and N is the resolution of the converters. For a quad-channel ADC with a resolution of 14 bits, M would be 4, and N would be 14. Next, the *N'* parameter is defined, which is the JESD204B word size. The converter sample resolution is broken down into four-bit nibbles. A 14-bit converter, as well as a 16-bit converter, has four nibbles, while a 12-bit converter has three nibbles.

The N' parameter is found by multiplying the number of nibbles by four. It can be advantageous to both the transmitter and receiver to set N' to 16 for converters with resolutions ranging from eight bits to 16 bits. This allows for the same transmitter and receiver to be used for multiple converters, easing overall system design. A non-complete nibble has room for either control bits (*CS*) or tail bits (*T*) as defined by the JESD204B standard. The equation N' = N + CS + T must be satisfied.

For example, a 14-bit converter with N' = 16 would have two bits left that could be used for control bits and/or tail bits. The figure below gives a visual representation of the how the converter data is mapped into a JESD204B word for a 14-bit converter with N' = 16. If there are no tail bits or control bits, the JESD204B word is the same as the sample data. This would occur in this case if the resolution of the converter were equal to 16 bits instead of 14 bits. It is important to note that the left most bit is the most significant bit of the converter sample. Samples are transmitted across the link MSB first and LSB last. Control bits, if any, are appended after the LSB to each conversion sample.



JESD204B word structure.

Samples, lanes, and frames, oh my

So now that we have the number of converters, the resolution of those converters, and we know the JESD204 word size, the next thing is to start looking at the structure of the link. The *S* parameter is the number of transmitted samples per converter per frame. Typically, the S parameter is set to one. This parameter must always be an integer to minimize cross talk between the JESD204B circuitry and the analog circuitry of the converter. The JESD204B specification allows for this parameter to be greater than one, but it is simpler to set S to one such that the frame clock (*FC*) and sample clock of the converter can be equal. For a 500MSPS converter and S = 1, the frame clock rate is 500MHz.

The next parameter to set is the number of lanes, *L* . In order to determine the number of lanes required, the maximum lane rate must be known. The maximum lane rate is determined by two main factors: the output driver capability of the transmitter and the input capability of the receiver. To calculate the lane line rate and determine the number of lanes, Equation 1 is used:

Lane Rate = (M x S x N' x 10/8 x FC)/L Eq. 1

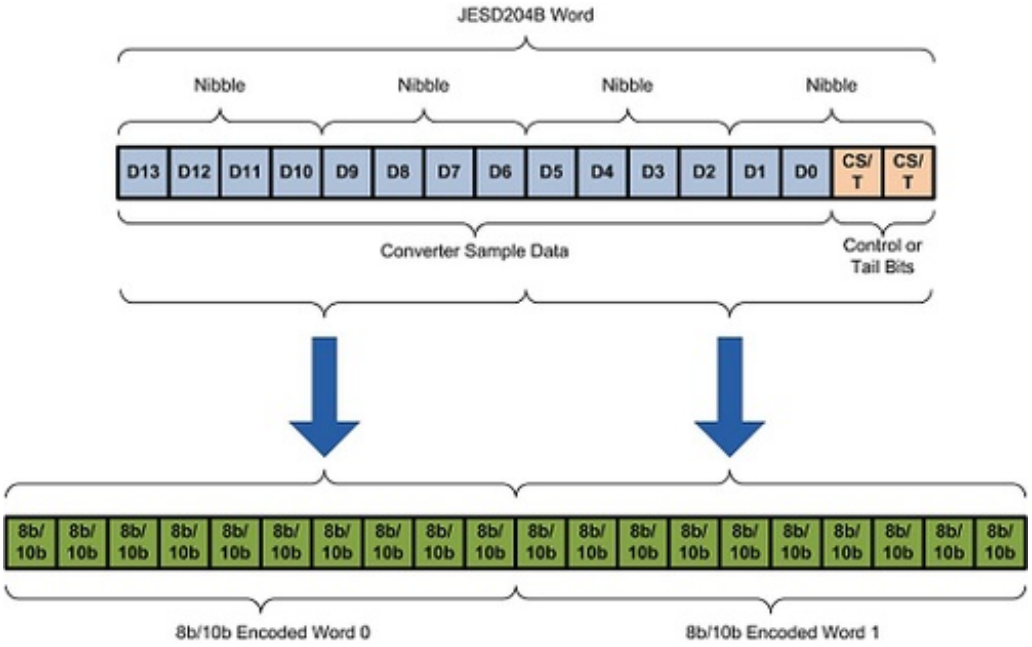
Using the example information above with a quad-channel, 500MSPS 14-bit converter with N' = 16 and S = 1, we can set the L parameter to different values and find the resultant lane rate to make sure it falls within system limitations. In this case, let's assume the maximum lane rate that can be supported by the transmitter and receiver is equal to the maximum lane rate defined for the JESD204B specification, which is 12.5Gbit/s. If L = 2, the resultant lane rate is (4 x 1 x 16 x 10/8 x 500MHz)/2 = 20Gbit/s. This exceeds the accepted maximum. Clearly, L must be set to 4 in order to reduce the lane rate below the accepted maximum. With L = 4, the lane rate is 10Gbit/s, which complies with the maximum rate of 12.5Gbit/s.

After using the number of converters, the number of samples per frame, the JESD204B word size, and the maximum lane rate to calculate the number of lanes, we can determine the number of octets transmitted per frame, F . In order to determine this parameter, Equation 2 can be used:

F = (M x S x N')/(8 x L) Eq. 2

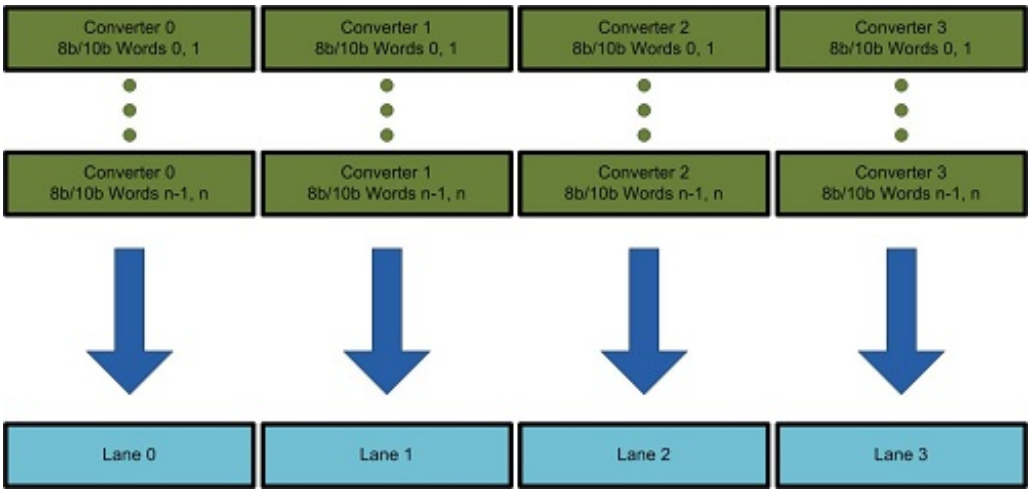
Continuing with the information from the previous examples, F can be calculated. Substituting the values, we have F = (4 x 1 x 16)/(8 x 4) = 2. So for a quad-channel, 500MSPS 14-bit converter with four JESD204B lanes, there are two octets needed to transmit one sample of data per frame, which results in a lane rate of 10Gbit/s.

The two octets are passed through an 8b/10b encoder before being output on the lane. The 10/8 factor in Eq. 1 is a result of this encoding scheme. It is important to understand the octet formation through the above process first and then recognize the additional overhead added by the 8b/10b encoder. Taking another look at the JESD204B word, this image shows a figurative breakdown of the octets in the JESD204B word and how it fits into the 8b/10b encoded word (or octet). For the example above with N = 14 and N' = 16, the converter sample is transmitted in two 8b/10b encoded words.



JESD204B 8b/10b encoded words.

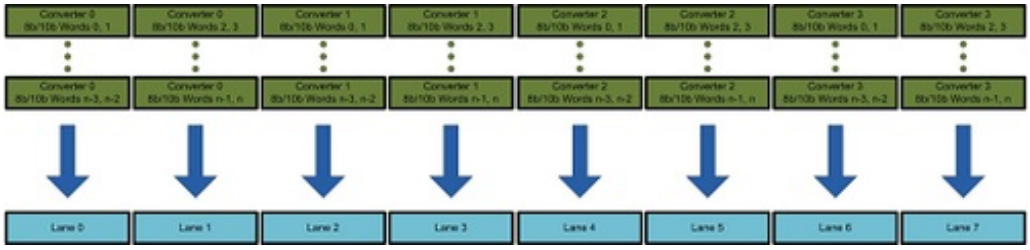
These 8b/10b words are transmitted over four lanes, so this means that each lane transmits sample from each of the four converters (M = 4, L = 4). Each of the samples gets mapped into an 8b/10b word and will simultaneously appear on the output lanes. This means that the four converters within the package will all be aligned in time. Not only will the sampling instant of the converters be aligned (since they are in the same package), but the transmission over the JESD204B link will be aligned as well. The image below shows how the samples from the four converters will be mapped on to the four JESD204B lanes. Each output lanes receives data from one of the four converters. Samples are output successively starting with sample 0, which has been mapped into 8b/10b Word 0 and Word 1, up to sample n, which has been mapped into 8b/10b Word n-1 and Word n.



JESD204B 8b/10b encoded converter words mapped on to lanes.

Let's take an example where a system limitation of 5Gbit/s lane rate exists. In this case, the data from each of the four converters must be mapped on to two lanes, so that lane rate can be dropped from 10Gbit/s down to 5Gbit/s. The figure below shows how the 8b/10b words from the four converters are mapped on to eight output lanes. In this case, 8b/10b Word 0 and Word 2 are output at the same time, as are 8b/10b Word 1 and Word 3, and so on.

One note here is that mapping the samples from a single converter on to multiple lanes was not a part of the original JESD204 specification but was introduced in the JESD204A specification and thus included in the JESD204B specification. This allows for cases such as the one described here where system limitations dictate how the link must be configured to meet lane rate speeds. This configurability along with the higher potential lanes rates allows many different configuration options for a designer using the JESD204B protocol. Where lane rates must be kept slower, more lanes can be used, and where lane rate speed is not an issue, the maximum rate can be used to keep the number of lanes to a minimum.



JESD204B 8b/10b encoded converter words mapped on to two lanes per converter.
(For a larger view, click here.)

Based upon the data bits in the converter sample, the appropriate 8b/10b word is encoded. This table gives a subset of the values for the data bits and their respective 8b/10b encoded words. The encoding scheme utilizes analysis of the running disparity of the serial data stream to monitor the DC imbalance. Due to the amount of available 8b/10b words, only a subset is shown here for simplicity. The entire table can be found in Appendix B of the Xilinx RocketIO User Guide UG024.

Data Byte Name	Converter Sample Data	Current Running Disparity --	Current Running Disparity +
D0.0	00000000	1001110100	0110001011
D1.0	00000001	0111010100	1000101011
D2.0	00000010	1011010100	0100101011
D3.0	00000011	1100011011	0011100100
D4.0	00000100	1101010100	0010101011
D5.0	00000101	1010011011	0101100100
D6.0	00000110	0110011011	1001100100

Sample of 8b/10b encoded words.

The converter data that is mapped into 8b/10b words is organized into frames and multiframes according to the JESD204B specification. In most cases, it is simpler to make S equal to 1 as discussed earlier. Setting S to 1 means that the frame rate and the converter

sample clock are equal. These frames are grouped into multiframes. The number of multiframes, K , can be between 1 and 32.

As converter sample rates push higher and higher, a faster interface is necessary to keep pace. JESD204B enables the converter interface to keep pace with the converter sample rates while offering a reduction in pin count, which leads to smaller packages, less trace routes, and lowers overall system cost. JESD204B does differ from its predecessors in that it requires a bit more upfront complexity, due to the new terms and parameters that it introduces. An examination of these parameters has hopefully provided some insight into the structure of the link. Understanding the link parameters should now equip you as a JESD204B user with a better understanding of how a link is structured based on converter properties, lane count and speed, and receiver capabilities.

References:

- JESD204B Survival Guide; Analog Devices
- JEDEC Standard JESD204B (July 2011); JEDEC Solid State Technology Association (registration required)
- Xilinx RocketIO Transceiver User Guide UG024 (Feb. 2007); Xilinx Inc.

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