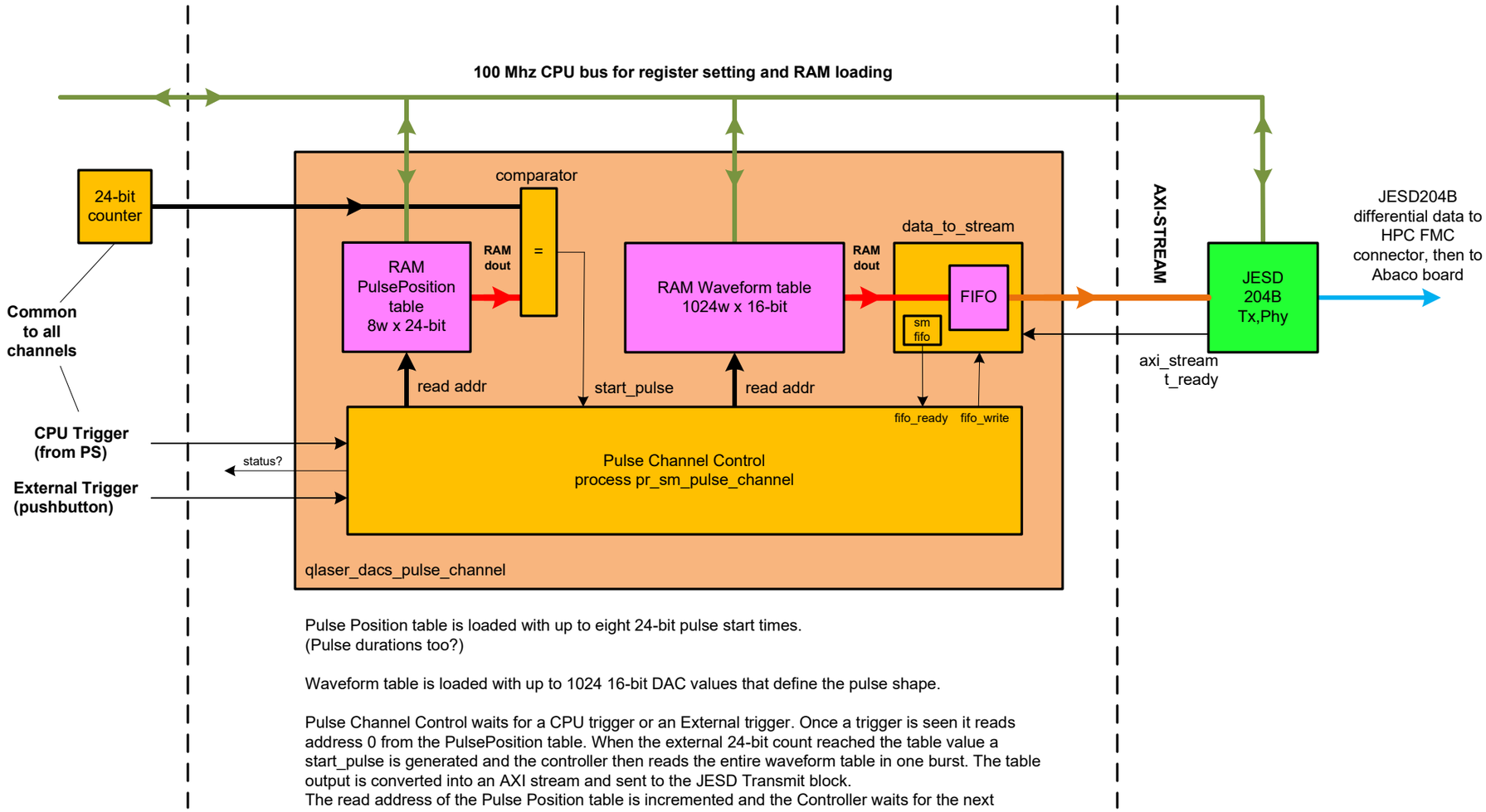
Laser Control FPGA
Block Diagram of one JESD DAC channel
(FPGA contains 32 channels)



Pulse Position table is loaded with up to eight 24-bit pulse start times.
(Pulse durations too?)

Waveform table is loaded with up to 1024 16-bit DAC values that define the pulse shape.

Pulse Channel Control waits for a CPU trigger or an External trigger. Once a trigger is seen it reads address 0 from the PulsePosition table. When the external 24-bit count reached the table value a start_pulse is generated and the controller then reads the entire waveform table in one burst. The table output is converted into an AXI stream and sent to the JESD Transmit block.
The read address of the Pulse Position table is incremented and the Controller waits for the next start_pulse the outpus the waveform table again.

The data_to_stream block uses a FIFO to buffer the waveform data and supplies AXI-stream data to the JESD block. The JESD block could apply ‘backpressure’ using the axi_s bus tready signal to pause the data.

Xilinx IP blocks (Standard)
Xilinx IP blocks (addnl license)
UW code blocks

JESD bus
AXI-Stream bus
CPU bus (cs,rd,wr,addr, din,dout