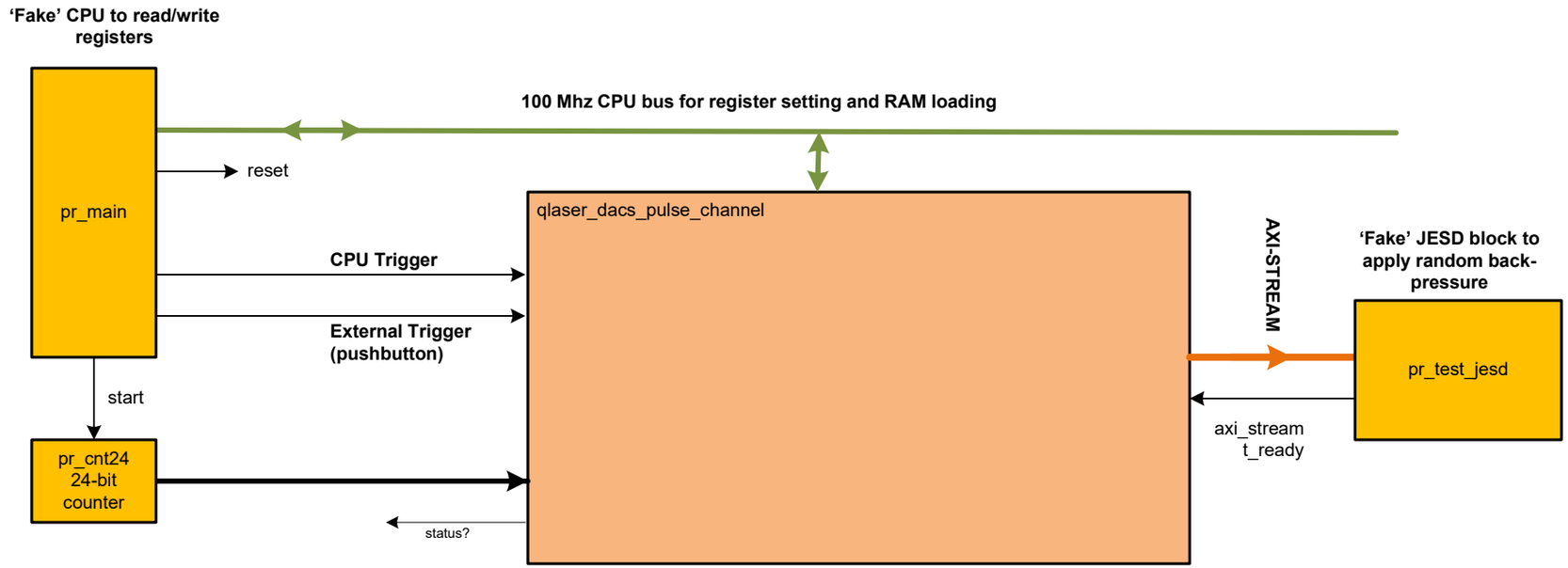
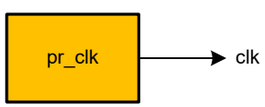
Laser Control FPGA
Test bench for one JESD DAC channel





Process to generate 100MHz clock for all testbench blocks

The pr_main proess:c

Generates the reset signal.
Tests the register and RAM read/write then programs the RAMs.
Generates the counter 'start' and the trigger to the pulse_channel block.

Observe waveform data on AXI-Stream output.

pr_test_jesd block could keep 'tready' high initially then after intial debugging could apply backpressure to test that feature.

Second step would be to use a model of the JESD block to replace pr_test_jesd

Third step would be to use a VHDL generate statement to instantiate 32 copies of the pulse channel block.