# Spec axi\_if\_cpubus.

This is a Vivado IP block that is used in a Vivado block diagram. The block is connected as an AXI-lite bus slave and allows the block diagram CPU to have a simplified bus interface to HDL blocks outside of the block diagram. It does not support burst transfers.

The simplified CPU bus interface has an output 18-bit (byte) address bus, 32-bit write data, with read and write strobes. There is a 32-bit input data bus with a data valid signal for data returned by read operations.

The external block must drive ‘cpu\_rdata\_dv’ high when the ‘cpu\_rd’ signal is high, and it is driving valid output data ‘cpu\_rdata’ bus. Once ‘cpu\_rd’ is set low then the ‘cpu\_rdata\_dv’ input must be driven low.

The block passes though the AXI clock ‘s00\_axi\_aclk’ to the ‘clk\_cpu’.

# Vivado Symbol

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# Block I/O

-- AXI-lite slave interface

s00\_axi\_aresetn Active low reset

s00\_axi\_aclk AXI-lite bus clock

s00\_axi AXI-lite bus

-- CPU Control interface connected to block diagram pins

cpu\_clk : out std\_logic;

cpu\_wr : out std\_logic;

cpu\_rd : out std\_logic;

cpu\_addr : out std\_logic\_vector(17 downto 0);

cpu\_wdata : out std\_logic\_vector(31 downto 0);

cpu\_rdata : in std\_logic\_vector(31 downto 0);

cpu\_rdata\_dv : in std\_logic;

# Register table.

The block has no internal registers but is assigned a base address and has a byte address range of 0x3FFFF. Writes and reads within this space are passed through to the CPU bus.

# Document Version

1.0 Initial version