2021_01_13_EE538_Lecture2_W2021

January 14, 2021

1 EE 538: Analog Integrated Circuit Design

1.1 Winter 2021

1.2 Instructor: Jason Silver

1.3 Python packages/modules

[2]:
```
import matplotlib as mpl
from matplotlib import pyplot as plt
import numpy as np
from scipy import signal
#%matplotlib notebook

mpl.rcParams['font.size'] = 12
mpl.rcParams['legend.fontsize'] = 'large'

def plot_xy(x, y, xlabel, ylabel):
    fig, ax = plt.subplots(figsize=(10.0, 7.5));
    ax.plot(x, y, 'b');
    ax.grid();
    ax.set_xlabel(xlabel);
    ax.set_ylabel(ylabel);

def plot_xy2(x1, y1, x1label, y1label, x2, y2, x2label, y2label):
    fig, ax = plt.subplots(2, figsize = (10.0, 7.5));
    ax[0].plot(x1, y1, 'b');
    ax[0].set_ylabel(y1label)
    ax[0].grid()

    ax[1].plot(x2, y2, 'b');
    ax[1].set_xlabel(x1label)
    ax[1].set_xlabel(x2label);
    ax[1].set_ylabel(y2label);
    ax[1].grid();

    fig.align_ylabels(ax[:])
```

```python
def plot_xlogy(x, y, xlabel, ylabel):
    fig, ax = plt.subplots(figsize=(10.0, 7.5));
    ax.semilogy(x, y, 'b');
    ax.grid();
    ax.set_xlabel(xlabel);
    ax.set_ylabel(ylabel);

def nmos_iv_sweep(V_gs, V_ds, W, L, lmda):
    u_n = 350                    # electron mobility (device parameter)
    e_ox = 3.9*8.854e-12/100; # relative permittivity
    t_ox = 9e-9*100;           # oxide thickness
    C_ox = e_ox/t_ox           # oxide capacitance
    V_thn = 0.7                 # threshold voltage (device parameter)
    V_ov = V_gs - V_thn
    Ldn = 0.08e-6
    Leff = L - 2*Ldn

    I_d = []

    for i in range(len(V_ds)):
        I_d.append(np.piecewise(V_ds[i], [V_ds[i] < V_ov, V_ds[i] >= V_ov],
                               [u_n*C_ox*(W/Leff)*(V_gs - V_thn - V_ds[i]/
 ↪2)*V_ds[i]*(1+lmda*V_ds[i]) ,
                                0.5*u_n*C_ox*(W/Leff)*(V_gs -␣
 ↪V_thn)**2*(1+lmda*V_ds[i])]))

    return np.array(I_d)

def pmos_iv_sweep(V_sg, V_sd, W, L, lmda):
    u_p = 100                    # electron mobility (device parameter)
    e_ox = 3.9*8.854e-12/100; # relative permittivity
    t_ox = 9e-9*100;           # oxide thickness
    C_ox = e_ox/t_ox           # oxide capacitance
    V_thp = -0.8                  # threshold voltage (device parameter)
    V_ov = V_sg - np.abs(V_thp)
    Ldp = 0.09e-6
    Leff = L - 2*Ldp

    I_d = []

    for i in range(len(V_sd)):
        I_d.append(np.piecewise(V_sd[i], [V_sd[i] < V_ov, V_sd[i] >= V_ov],
                               [u_p*C_ox*(W/Leff)*(V_sg - np.abs(V_thp) - V_sd[i]/
 ↪2)*V_sd[i]*(1+lmda*V_sd[i]) ,
                                0.5*u_p*C_ox*(W/Leff)*(V_sg - np.
 ↪abs(V_thp))**2*(1+lmda*V_sd[i])]))
```

```
    return np.array(I_d)

def nmos_iv_sat(V_gs, V_ds, W, L, lmda):
    u_n = 350                   # electron mobility (device parameter)
    e_ox = 3.9*8.854e-12/100; # relative permittivity
    t_ox = 9e-9*100;          # oxide thickness
    C_ox = e_ox/t_ox          # oxide capacitance
    V_thn = 0.7                # threshold voltage (device parameter)
    V_ov = V_gs - V_thn
    Ldn = 0.08e-6
    Leff = L - 2*Ldn

    I_d = 0.5*u_n*C_ox*(W/Leff)*(V_gs - V_thn)**2*(1+lmda*V_ds)

    return I_d
```

2 Lecture 2 - Single-Stage MOS Amplifiers

2.1 Announcements

- Assignment 1 posted, due Sunday January 17
  - PDF submission on Canvas
- Office hours
  - Thursdays at 7pm (Jason)
  - Fridays at 7pm (Thushara)

2.2 Week 2

- Chapter 2 of Razavi (basic MOS physics)
  - Review: DC small signal model (2.4.3)
- Chapter 3 of Razavi (single-stage amplifiers)
- Chapter 5 of Razavi (current mirrors)
  - Section 5.1 Basic Current Mirrors

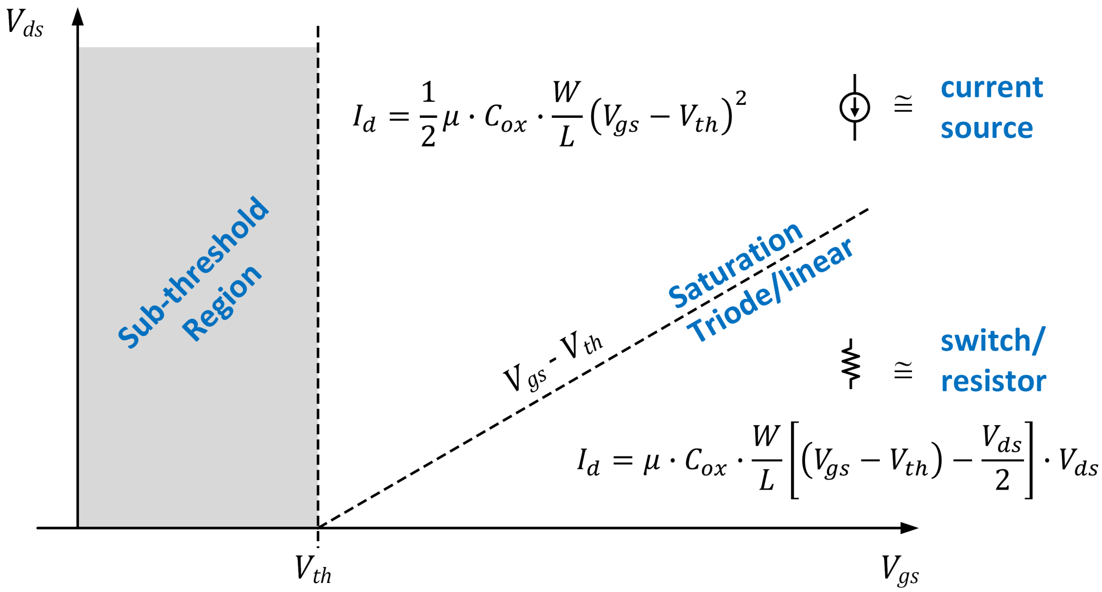
2.3 Overview

- Last time…
  - MOSFET drain current a product of vertical (V_{GS}) and lateral (V_{DS}) electric fields
  - MOS behaves as a resistor in triode ($V_{DS} << V_{GS}\breve{}V_{TH}$) and a current source in saturation ($V_{DS} > V_{GS}\breve{}V_{TH}$)
  - Small-signal model obtained by linearizing MOS behavior about a DC operating point (i.e. specific value of $V_{GS} = V_{GS0}$)
- Today…
  - Small signal model, cont.
  - PMOS transistors
  - Common source amplifier
    - Passive load

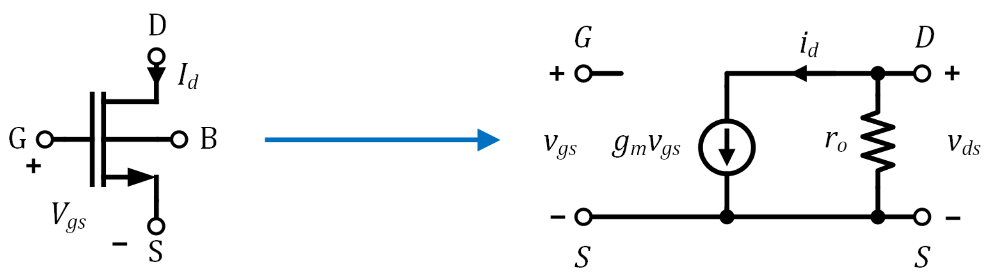
* Active load

- Basic current mirrors

2.4 First-order MOS model summary



2.5 DC small-signal model

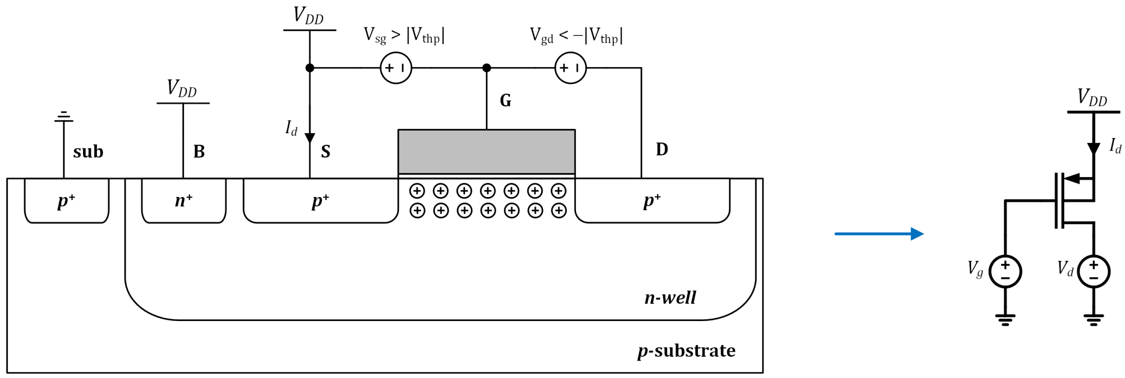


$$I_D = f(V_{GS}, V_{DS})$$

$$g_m = \frac{2I_{D0}}{V_{OV}} \qquad r_o = \frac{1}{g_{ds}} = \frac{1}{\lambda I_{D0}}$$

- Small-signal model replaces nonlinear $I_D(V_{GS}, V_{DS})$ with linear parameters g_m and r_o that enable the use of linear circuit analysis techniques
- *Important*: All DC voltages become AC ground in the small-signal model

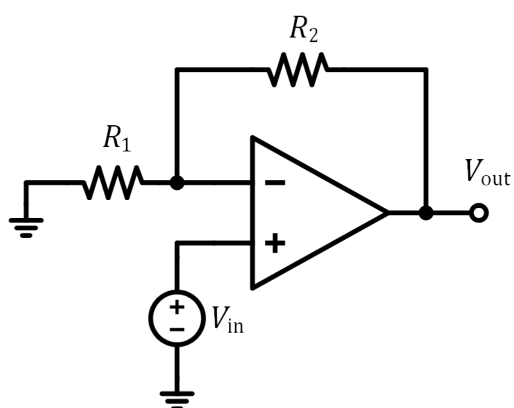
2.6 PMOS transistor



- In $CMOS$ processes, $PMOS$ transistors are produced in the same substrate as NMOS
- To operate in saturation, the following requirements must be satisfied:
  - $V_{sg} > |V_{thp}|$
  - $V_{sd} > V_{sg} - |V_{thp}|$
- The saturation current for a $PMOS$ transistor is thus given by

$$I_d = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{sg} - |V_{thp}|)^2(1 + \lambda V_{sd}) \tag{1}$$

2.7 High-gain amplifier design



$$G = \frac{V_{out}}{V_{in}} = \frac{A_v}{1 + \beta A_v} \tag{2}$$

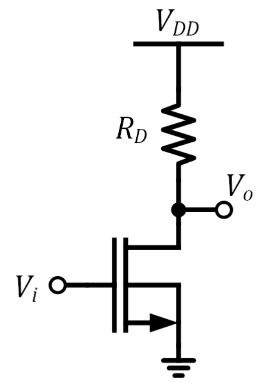
$$\beta = \frac{R_1}{R_1 + R_2} \tag{3}$$

- if $\beta A_v >> 1$,

$$G = \frac{A_v}{1 + \beta A_v} \rightarrow \frac{1}{\beta} \tag{4}$$

- High-gain amplifiers are used to desensitize transfer functions to temperature- and manufacturing-dependent physical parameters (e.g. g_m and r_o)
- Typical values of A_v for opamps are $100 - 140dB$ $(100,000 - 10,000,000V/V)$
- High *open-loop* gain (A_v) $\rightarrow$ precise *closed-loop* gain (G)
- For this reason, when designing CMOS amplifiers (i.e. opamps and OTAs) substantial emphasis is placed on achieving high open-loop gain

2.8 Common-source amplifier



$$I_d = \frac{1}{2}\mu \cdot C_{ox} \cdot \frac{W}{L}(V_i - V_{th})^2(1 + \lambda V_o) \tag{5}$$

$$V_o = V_{DD} - I_d \cdot R_D \tag{6}$$

- The common-source amplifier is an exemplary model of how we achieve gain in analog circuits:
  - Change in the output current ΔI_d is realized (primarily) by a change in the input voltage ΔV_i and the voltage-current relationship of the device
  - Output voltage changes as the result of ΔI_d flowing through the output resistance of the circuit (in this case, R_D)

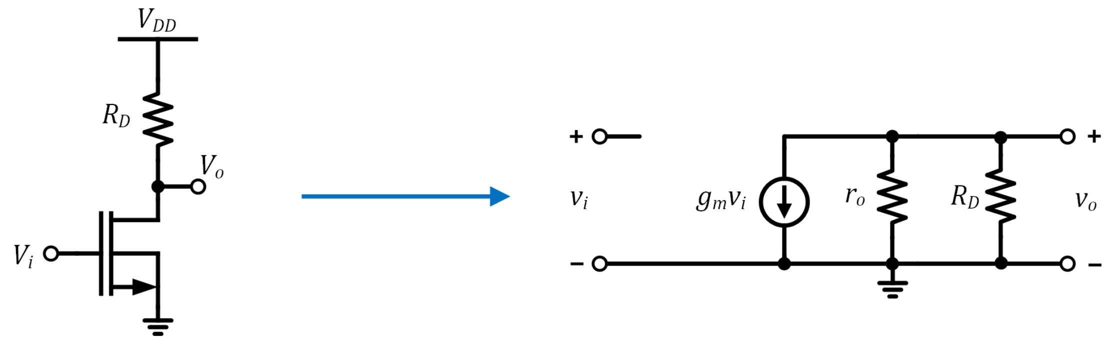
2.9 Ouput voltage minimum/maximum (swing)

- For the maximum voltage, when $V_o = V_{DD}$, current no longer flows through R_D and changes in the input cannot effect changes in the output
- For the minimum, to ensure the transistor remains in saturation V_o should be greater than the overdrive voltage, $V_i - V_{th}$
- The valid range of output voltages is thus

$$V_i - V_{th} < V_o < V_{DD} \tag{7}$$

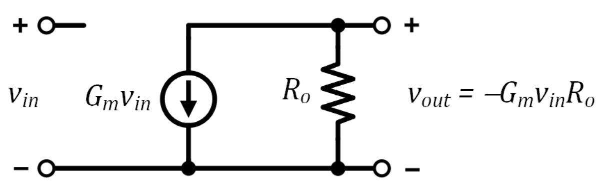
- Assuming signals swing symmetrically above and below the operating point, we can maximize use of the output swing by selecting R_D and I_D to an output operating point at the output of $V_O = V_{DD}/2$

2.10 Small-signal model



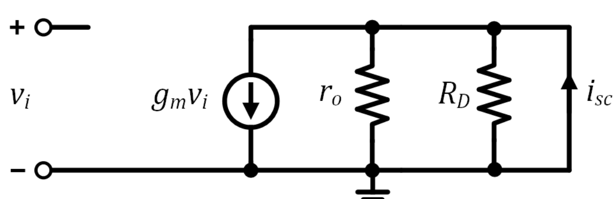
- V_{DD} is a *DC* (constant) voltage, making it an *AC* (small-signal) ground
- r_o and R_D appear in parallel in the small-signal model

2.11 MOS amplifier analysis



- Voltage gain in transistor-based circuits is *almost always* realized as the product of a transconductance G_m and a small-signal resistance R_o
- Analysis approach: Use Norton analysis to determine the parameters G_m and R_o using the small signal model
  - Find the short-circuit current i_{sc} to determine $G_m = i_{sc}/v_{in}$
  - The output resistance R_o is determiend by setting $v_{in} = 0$, applying a test voltage to the output, and finding the expression for the resulting current

2.12 Common-source Norton model (Gm)

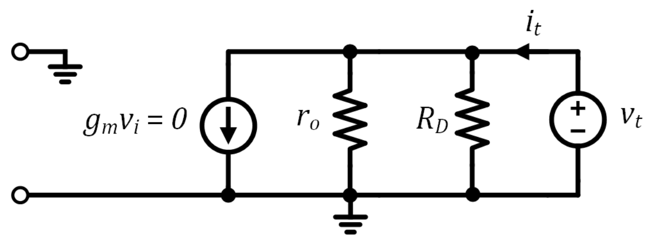


- To determine G_m in the Norton model, short the output terminals and measure i_{sc}
- Due to the short circuit, no current flows through r_o or R_D
- G_m is determined by taking the ratio of i_{sc} to v_i:

$$G_m = \frac{i_{sc}}{v_i} = \frac{g_m \cdot v_i}{v_i} = g_m \tag{8}$$

- Thus, in the case of the common-source amplifier, $G_m = g_m$

2.13 Common-source Norton model (Ro)



- To determine R_o, apply a test voltage v_t between the output terminals and measure i_t
- Here we can see that i_t is given by

$$i_t = v_t \cdot \left(\frac{1}{r_o} + \frac{1}{R_D} \right) \tag{9}$$

- Thus, R_o is just the parallel combination of r_o and R_D:

$$R_o = \frac{v_t}{i_t} = \left(\frac{1}{r_o} + \frac{1}{R_D} \right)^{-1} = \boxed{r_o || R_D} \tag{10}$$

- The voltage gain is thus

$$- G_m \cdot R_o = -g_m \cdot r_o || R_D \tag{11}$$

2.14 Relative magnitudes of RD and ro

- Output resistance r_o is given by the expression

$$r_o \approx \frac{1}{\lambda I_{D0}} \tag{12}$$

- Typical drain resistance R_D can be expressed as (assumes output DC operating point of $V_{DD}/2$, which allows for maximal output signal swing)

$$R_D \approx \frac{V_{DD}}{2 I_{D0}} \tag{13}$$

- For $V_{DD} = 3V$ and $\lambda = 0.1 V^{-1}$, $r_o \approx 7 \times R_D$
- Thus, for the common-source amplifier,

$$\boxed{A_v = -g_m (r_o || R_D) \approx -g_m \cdot R_D} \tag{14}$$

2.15 Maximum gain with RD

- What is the maximum gain that can be achieved with a passive (resistive) load?

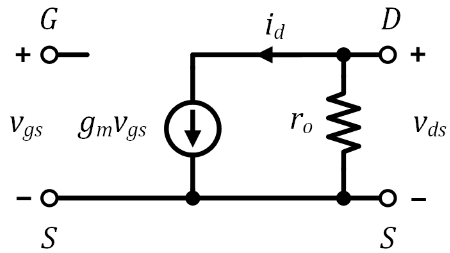
$$A_v \approx -g_m \cdot R_D = -\frac{2 I_{D0}}{V_{ov}} R_D \tag{15}$$

- Assuming an operating point for the output voltage of $V_{DD}/2$, the gain is given by

$$|A_v| \approx \frac{2 \cdot V_{DD}/2}{R_D \cdot V_{ov}} \cdot R_D = \frac{V_{DD}}{V_{ov}} \tag{16}$$

- Assuming $V_{DD} = 3V$ and $V_{ov} = 150mV$, this limits the gain to approximately $20V/V$
- This is generally too low to be useful in building an opamp
- How do we increase gain?

2.16 MOS DC model (intrinsic gain)



$$g_m = \frac{2I_{D0}}{V_{OV}} \tag{17}$$

$$r_o = \frac{1}{g_{ds}} = \frac{1}{\lambda I_{D0}} \tag{18}$$

$$\left|\frac{v_{ds}}{v_{gs}}\right| = \frac{g_m}{g_{ds}} = \frac{2}{\lambda V_{OV}} \tag{19}$$

- Recall that the intrisic gain of the transistor is given by the product of g_m and r_o
- g_m increases linearly with drain current, while r_o is inversely dependent, keeping their product constant
- What is a typical value for $g_m r_o$?

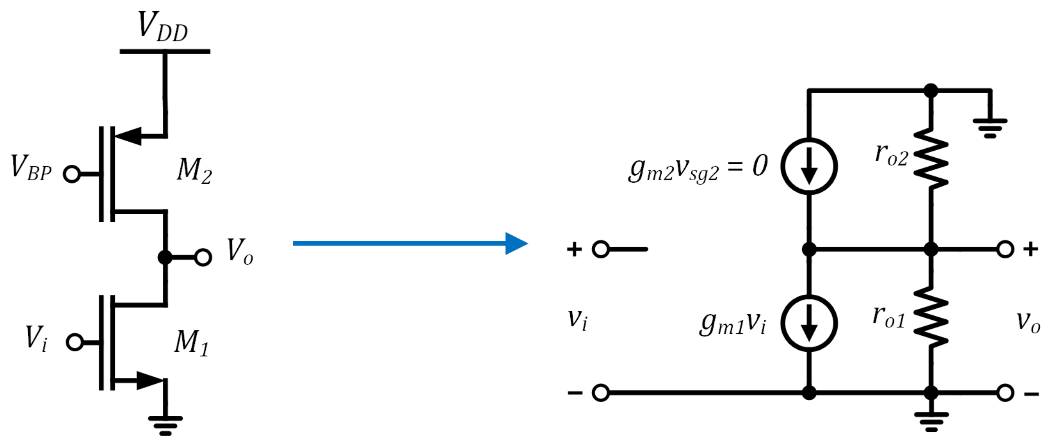
2.17 Intrinsic gain

- In our Level 1 "process" $\lambda_n = 0.1V^{-1}$
- In order to maximize signal swing, we want to use a relatively low overdrive voltage ($V_{ov} = V_{GS} - V_{th}$)
- Assuming a gate bias of $V_{GS0} = 0.9V$ (for example), the intrinsic gain is given as

$$g_m r_o \approx \frac{2}{\lambda V_{ov}} = \frac{2}{0.1V^{-1} \times 200mV} = 100V/V \tag{20}$$

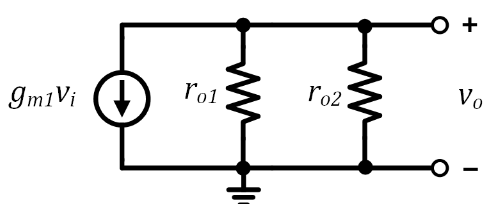
- This is $5\times$ the theoretical gain with a resistive load
- How can we can advantage of intrinsic gain to build amplifiers with gains approaching/exceeding $100dB$?

2.18 Common-source with active load



- We can increase the gain of the common-source statge by replacing the resistor $R_D$with a $PMOS$ transistor in saturation
- This is referred to as an *active* load, since it replaces a passive device (resistor) with an active one (transistor)
- The bias voltage V_{BP} sets the DC operating point ($g_{m1,2}$ and $r_{o1,2}$) of the amplifier stage by controlling the drain currents of M_1 and M_2
- Because both V_S and V_G of M_2 are DC voltages, its transconductance current is zero in the small-signal model

2.19 Small-signal gain



- In this circuit, M_1 functions as a transconductor and M_2 behaves as a resistance
- The small-signal gain expression is identical to that of the passive load, with R_D replaced by r_{o2}:

$$A_v = \frac{v_o}{v_i} = -g_{m1} \cdot (r_{o1}||r_{o2}) \tag{21}$$

- If we make the (somewhat dubious) assumption that $r_{op} = r_{on} = r_o$, we can relate the gain of the active load stage to the MOSFET's intrinsic gain:

$$A_v = \frac{v_o}{v_i} = -g_{m1} \cdot (r_{o1}||r_{o2}) \approx -\frac{g_m \cdot r_o}{2} \tag{22}$$

- In practice $r_{on} \neq r_{op}$, but are of the same order of magnitude

2.20 Magnitude of the gain

- Recall that the gain of the common-source stage with a passive load (R_D) is

$$A_v = -g_m(r_o||R_D) \approx -g_m \cdot R_D \tag{23}$$

- For a nominal *DC* output votage of $V_{DD}/2$ (i.e. the *DC* operating point), this is

$$|A_v| \approx \frac{2 \cdot V_{DD}/2}{R_D \cdot V_{ov}} \cdot R_D = \frac{V_{DD}}{V_{ov}} \leq 20V/V \tag{24}$$

- For the active-load stage, the gain is given by

$$A_v = \frac{v_o}{v_i} = -g_{m1} \cdot (r_{o1}||r_{o2}) \tag{25}$$

- Using our Level 1 process parameters ($\lambda_n = 0.1, \lambda_p = 0.2$), this becomes

$$A_v = -g_{m1} \cdot (r_{o1}||r_{o2}) = -g_{m1} \cdot r_{o1}\frac{r_{o2}}{r_{o1} + r_{o2}} \approx -33V/V \tag{26}$$

- This is an improvement, but still fairly low. We'll discuss how to increase this soon...

2.21 Ouput voltage range

- When V_o is at its maximum value, M_2 still needs to be in saturation to operate as a high-resistance load, requiring

$$V_o < V_{DD} - (V_{DD} - V_{BP} + |V_{thp}|) = V_{BP} - |V_{thp}| \tag{27}$$

- Similarly, M_1 needs to remain in saturation, setting the lower bound on V_o as

$$V_o > V_{GS1} - V_{thn} \tag{28}$$

- The valid range of output voltages is thus

$$V_{GS1} - V_{thn} < V_o < V_{BP} - |V_{thp}| \tag{29}$$

- One way to look at this is to say the output swing is $V_{DD} - 2V_{OV}$
- Again to maximize use of this range we would like to set the operating point of V_o to approximately $V_{DD}/2$
- How do we set the operating point?

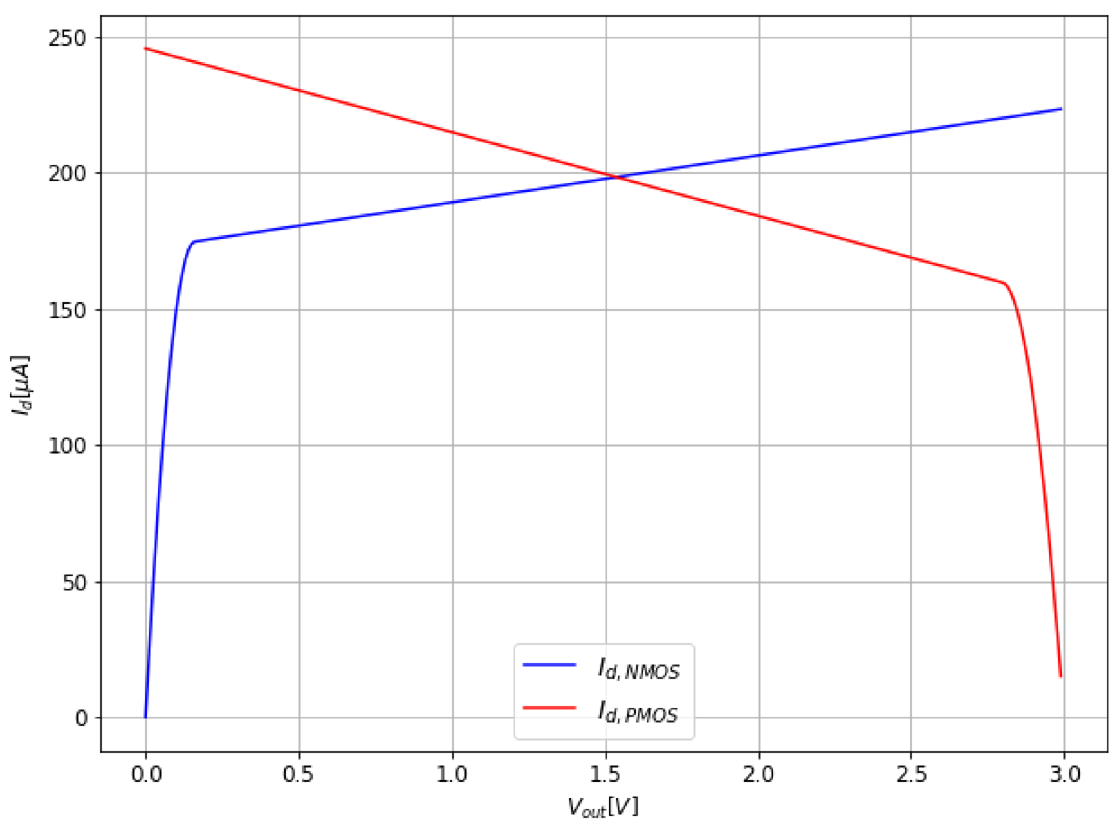
[3]:
```
def plot_cs_op_point(V_DD, V_BP, V_GS1, V_out):
    I_d1 = nmos_iv_sweep(V_GS1, V_out, 100, 1, 0.1)
    I_d2 = pmos_iv_sweep(V_DD-V_BP, V_DD-V_out, 200, 1, 0.2)

    fig, ax = plt.subplots(figsize=(10.0, 7.5))
    ax.plot(V_out, 1e6*I_d1, label=r'$I_{d,NMOS}$', color='blue')
    ax.plot(V_out, 1e6*I_d2, label=r'$I_{d,PMOS}$', color='red')
```

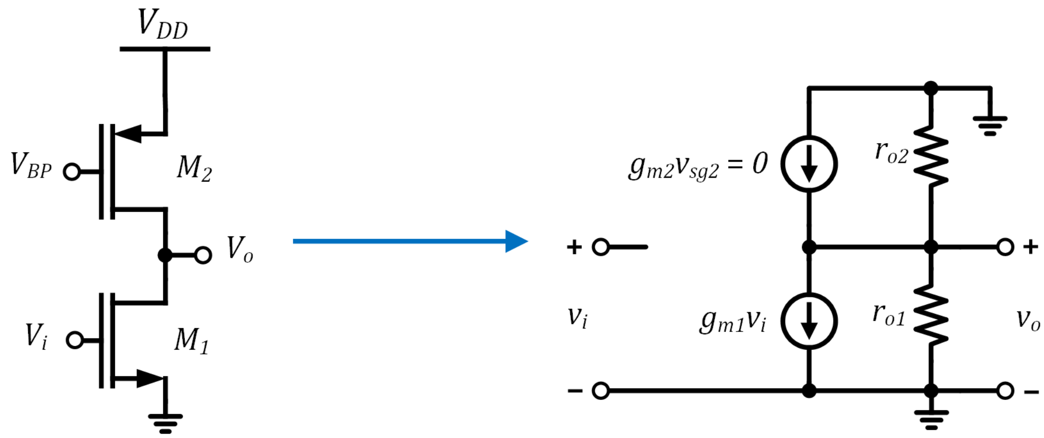
```
    ax.set_xlabel(r'$V_{out} [V]$')
    ax.set_ylabel(r'$I_{d} [\mu A]$')
    ax.legend()
    ax.grid()
```

- Because $I_{D1} = I_{D2}$, the point at which the drain current curves intersect constitutes the operating point of the circuit
- For a nominal (DC) input voltage of $0.86V$, both transistors are approximately in the middle of their saturation ranges and the output voltage is ~$V_{DD}/2$
- However, if V_{GS1} is changed slightly (or if device parameters differ due to manufacturing variability), the resulting operating point can place either M_1 or M_2 in triode, drastically decreasing the gain
- Feedback is required to stabilize the output DC voltage at a desired value (more on this later)

[6]:
```
V_DD = 3
V_BP = 2
V_GS1 = .86
V_out = np.arange(0,3,step=0.01)
plot_cs_op_point(V_DD, V_BP, V_GS1, V_out)
```



2.22 Common-source biasing

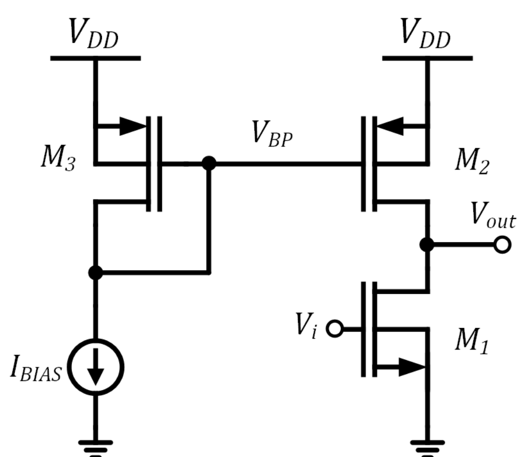


- If the output voltage is maintained such that both M_1 and M_2 remain in saturation, the gain is determined by

$$A_v = \frac{v_o}{v_i} = -g_{m1} \cdot r_{o1}||r_{o2} \tag{30}$$

- where $g_{m1} = 2I_{D1}/V_{OV1}$, $r_{o2} = 1/\lambda_n I_{D1}$, $r_{o1} = 1/\lambda_p I_{D2}$, and $I_{D1} = I_{D2}$
- I_{D2} (I_{D1}) constitutes the DC operating point of the circuit, and is often referred to as the "bias current"
- How do we control I_{D2}?

2.23 Basic current mirror



- Assuming $\lambda_p = 0$, if $(W/L)_2$ $ = (W/L)_3$,

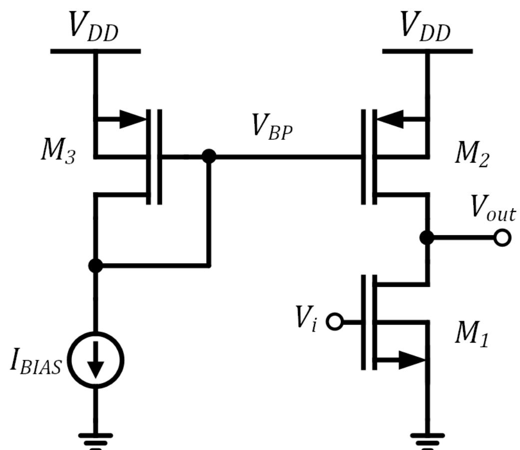
$$I_{D1} = I_{D2} = I_{D3} = I_{BIAS} \tag{31}$$

- Hence,

$$g_{m1} = \frac{2I_{BIAS}}{V_{OV}}, \quad r_{o1} = \frac{1}{\lambda_n I_{BIAS}}, \quad r_{o2} = \frac{1}{\lambda_p I_{BIAS}} \tag{32}$$

- A "diode-connected" transistor (M_3 in the figure) converts a current (I_{BIAS}) into a voltage (V_{BP}) based on the relation
- Current biasing in this manner allows us to control the small-signal performance of the circuit by designing I_{BIAS} to achieve specific goals (e.g. gain, bandwidth, noise)

2.24 Current mirror operation



- Again, assuming $\lambda_p = 0$

$$V_{SG3} = |V_{thp}| + \sqrt{\frac{2 \cdot I_{BIAS}}{\mu_p C_{ox} \left(\frac{W}{L}\right)_3}} \tag{33}$$

- The commmon-source bias current is thus

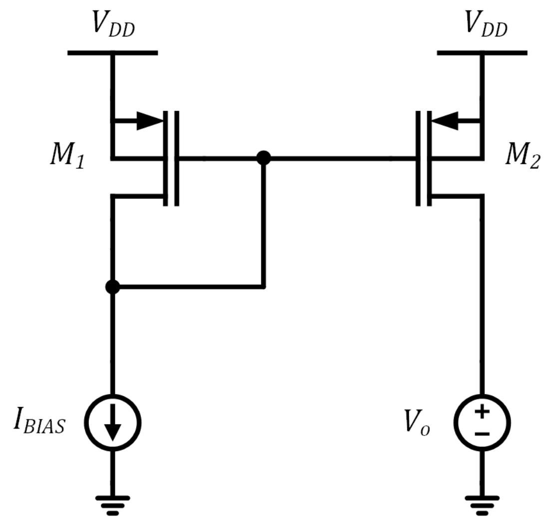
$$I_{D1} = I_{D2} = \frac{1}{2}\mu \cdot C_{ox} \cdot \frac{W}{L}(V_{DD} - V_{BP} - |V_{thp}|)^2 \tag{34}$$

- The "diode" connection (gate and drain shorted together) ensures M_3 is always in saturation, since

$$V_{SG} = V_{SD} > V_{SG} - |V_{thp}| \tag{35}$$

- Because M_2 and M_3 share gate and source connections, M_2 "mirrors" (i.e. copies) M_3's current
- However, we have ignored the fact that V_{SD2} is not necessarily equal to V_{SD3}
- How do I_{D1}, I_{D2} vary with V_{out}?

2.25 Finite output resistance



- Considering the effect of channel-length modulation on M_2's drain current gives

$$I_{D2} = \frac{1}{2}\mu \cdot C_{ox} \cdot \frac{W}{L}(V_{DD} - V_{BP} - |V_{thp}|)^2[1 + \lambda(V_{DD} - V_o)] \tag{36}$$

- To assess the dependence of I_{D2} on V_o, we can take the derivative

$$\frac{\partial I_{D2}}{\partial V_o} = \frac{1}{r_{o2}} \tag{37}$$

- The purpose of M_2 is to provide current for the common-source stage
- The output resistance of the current mirror captures the dependence of I_{D2}, which determines *how* effectively it operates as a current source
- It turns out then that the same factor limiting voltage gain in the common-source stage limits the precision of a current mirror: *output resistance*
- How can we increase output resistance and, as a result, gain?
- More on this next time…

2.26 Summary

- High gain in operational amplifiers (Opamps) and operational *transconductance* amplifiers (OTAs) is achieved using (one or more) structures similar in form to the common-source stage
  - Voltage gain is realized as the product of a transconductance (G_m) and a resistance (R_o)
- Active loads enable higher values of R_o, and thus higher gain, than passive loads
- Current biasing allows us to precisely define the critical small-signal parameters (g_m, r_o) that determine circuit performance
- Finite MOS output resistance limits both gain and the precision of current mirrors
- Next time, we will look at how to build both better current mirrors and voltage amplification stages