2021_01_20_EE538_Lecture3_W2021

January 23, 2021

1 EE 538: Analog Integrated Circuit Design

1.1 Winter 2021

1.2 Instructor: Jason Silver

1.3 Python packages/modules

[2]:
```
import matplotlib as mpl
from matplotlib import pyplot as plt
import numpy as np
from scipy import signal
#%matplotlib notebook

mpl.rcParams['font.size'] = 12
mpl.rcParams['legend.fontsize'] = 'large'

def plot_xy(x, y, xlabel, ylabel):
    fig, ax = plt.subplots(figsize=(10.0, 7.5));
    ax.plot(x, y, 'b');
    ax.grid();
    ax.set_xlabel(xlabel);
    ax.set_ylabel(ylabel);

def plot_xy2(x1, y1, x1label, y1label, x2, y2, x2label, y2label):
    fig, ax = plt.subplots(2, figsize = (10.0, 7.5));
    ax[0].plot(x1, y1, 'b');
    ax[0].set_ylabel(y1label)
    ax[0].grid()

    ax[1].plot(x2, y2, 'b');
    ax[1].set_xlabel(x1label)
    ax[1].set_xlabel(x2label);
    ax[1].set_ylabel(y2label);
    ax[1].grid();

    fig.align_ylabels(ax[:])
```

```
def plot_xlogy(x, y, xlabel, ylabel):
    fig, ax = plt.subplots(figsize=(10.0, 7.5));
    ax.semilogy(x, y, 'b');
    ax.grid();
    ax.set_xlabel(xlabel);
    ax.set_ylabel(ylabel);

def nmos_iv_sweep(V_gs, V_ds, W, L, lmda):
    u_n = 350                  # electron mobility (device parameter)
    e_ox = 3.9*8.854e-12/100; # relative permittivity
    t_ox = 9e-9*100;           # oxide thickness
    C_ox = e_ox/t_ox           # oxide capacitance
    V_thn = 0.7                 # threshold voltage (device parameter)
    V_ov = V_gs - V_thn
    Ldn = 0.08e-6
    Leff = L - 2*Ldn

    I_d = []

    for i in range(len(V_ds)):
        I_d.append(np.piecewise(V_ds[i], [V_ds[i] < V_ov, V_ds[i] >= V_ov],
                        [u_n*C_ox*(W/Leff)*(V_gs - V_thn - V_ds[i]/
 ↪2)*V_ds[i]*(1+lmda*V_ds[i]) ,
                         0.5*u_n*C_ox*(W/Leff)*(V_gs -␣
 ↪V_thn)**2*(1+lmda*V_ds[i])]))

    return np.array(I_d)

def pmos_iv_sweep(V_sg, V_sd, W, L, lmda):
    u_p = 100                  # electron mobility (device parameter)
    e_ox = 3.9*8.854e-12/100; # relative permittivity
    t_ox = 9e-9*100;           # oxide thickness
    C_ox = e_ox/t_ox           # oxide capacitance
    V_thp = -0.8                 # threshold voltage (device parameter)
    V_ov = V_sg - np.abs(V_thp)
    Ldp = 0.09e-6
    Leff = L - 2*Ldp

    I_d = []

    for i in range(len(V_sd)):
        I_d.append(np.piecewise(V_sd[i], [V_sd[i] < V_ov, V_sd[i] >= V_ov],
                        [u_p*C_ox*(W/Leff)*(V_sg - np.abs(V_thp) - V_sd[i]/
 ↪2)*V_sd[i]*(1+lmda*V_sd[i]) ,
                         0.5*u_p*C_ox*(W/Leff)*(V_sg - np.
 ↪abs(V_thp))**2*(1+lmda*V_sd[i])]))
```

```
    return np.array(I_d)

def nmos_iv_sat(V_gs, V_ds, W, L, lmda):
    u_n = 350                  # electron mobility (device parameter)
    e_ox = 3.9*8.854e-12/100; # relative permittivity
    t_ox = 9e-9*100;           # oxide thickness
    C_ox = e_ox/t_ox           # oxide capacitance
    V_thn = 0.7                 # threshold voltage (device parameter)
    V_ov = V_gs - V_thn
    Ldn = 0.08e-6
    Leff = L - 2*Ldn

    I_d = 0.5*u_n*C_ox*(W/Leff)*(V_gs - V_thn)**2*(1+lmda*V_ds)

    return I_d
```

2 Lecture 3 - High-gain MOS Amplifier Structures

2.1 Announcements

- Assignment 2 posted, due Sunday January 24
  - PDF submission on Canvas

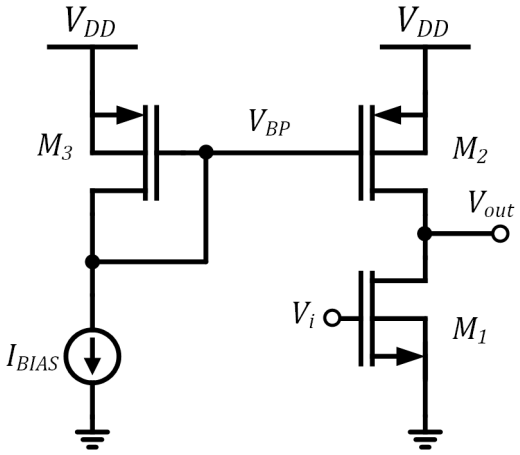
2.2 Week 3

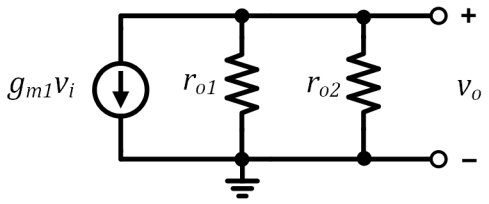
- Chapter 3 of Razavi (single-stage amplifiers)
- Chapter 5 of Razavi (current mirrors)
  - Section 5.1 Basic Current Mirrors
  - Section 5.2 Cascode Current Mirrors

2.3 Overview

- Last time...
  - Small signal model, cont.
  - PMOS transistors
  - Common source amplifier
    - Passive load
    - Active load
  - Basic current mirrors
- Today...
  - Source degeneration
  - Cascode current mirror
  - Cascode amplifier
  - Body effect
  - Cascode biasing

2.4 Common-source amplifier (review)





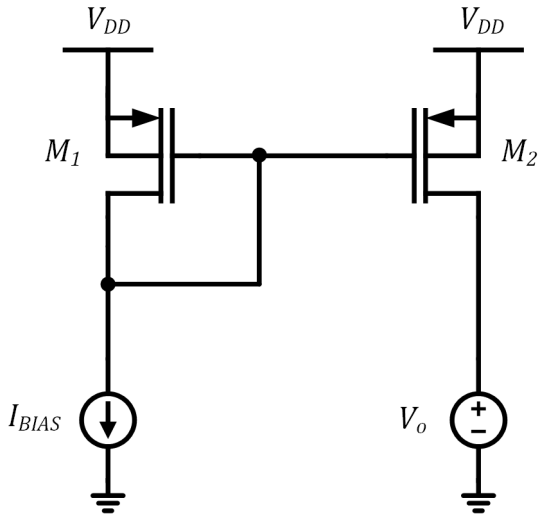
$$\frac{v_o}{v_i} = -G_m \cdot R_o = g_{m1} \cdot r_{o1} \frac{\frac{1}{\lambda_p I_{D2}}}{\frac{1}{\lambda_n I_{D2}} + \frac{1}{\lambda_p I_{D2}}} \tag{1}$$

$$\tag{2}$$

$$= \frac{1}{\lambda_n \cdot V_{OV1}} \frac{\lambda_n}{\lambda_p + \lambda_n} = \boxed{\frac{g_{m1} r_{o1}}{3}} \tag{3}$$

- Compared to the passively-loaded stage, higher gain is achieved by increasing output resistance using an active load r_{o2}
- Bias voltage V_{BP} is produced using the current mirror formed by M_2, M_3

2.5 Current mirror sizing



$$V_{SG2} = V_{SG1} \tag{4}$$

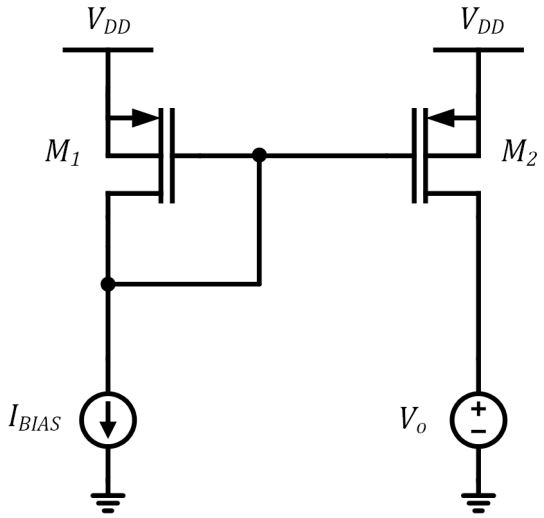
$$I_{BIAS} = I_{D1} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_1 (V_{SG1} - |V_{thp}|)^2 \tag{5}$$

$$I_{D2} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_2 (V_{SG2} - |V_{thp}|)^2 \tag{6}$$

$$\frac{(W/L)_2}{(W/L)_1} = K \rightarrow \boxed{I_{D2} = K \cdot I_{BIAS}} \tag{7}$$

- When sizing current mirrors, we assume infinite output impedance (i.e. $\lambda = 0$) since V_o isn't constant
- We then select an integer ratio of $(W/L)_2$ to $(W/L)_1$ to achieve a specific output current

2.6 Current source output resistance



$$\frac{1}{R_o} = \frac{\partial I_{D2}}{\partial V_o} \tag{8}$$

$$\tag{9}$$

$$= \frac{\partial}{\partial V_o}\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{SG2} - |V_{thp}|)^2)[1 + \lambda_p(V_{DD} - V_o)] \tag{10}$$

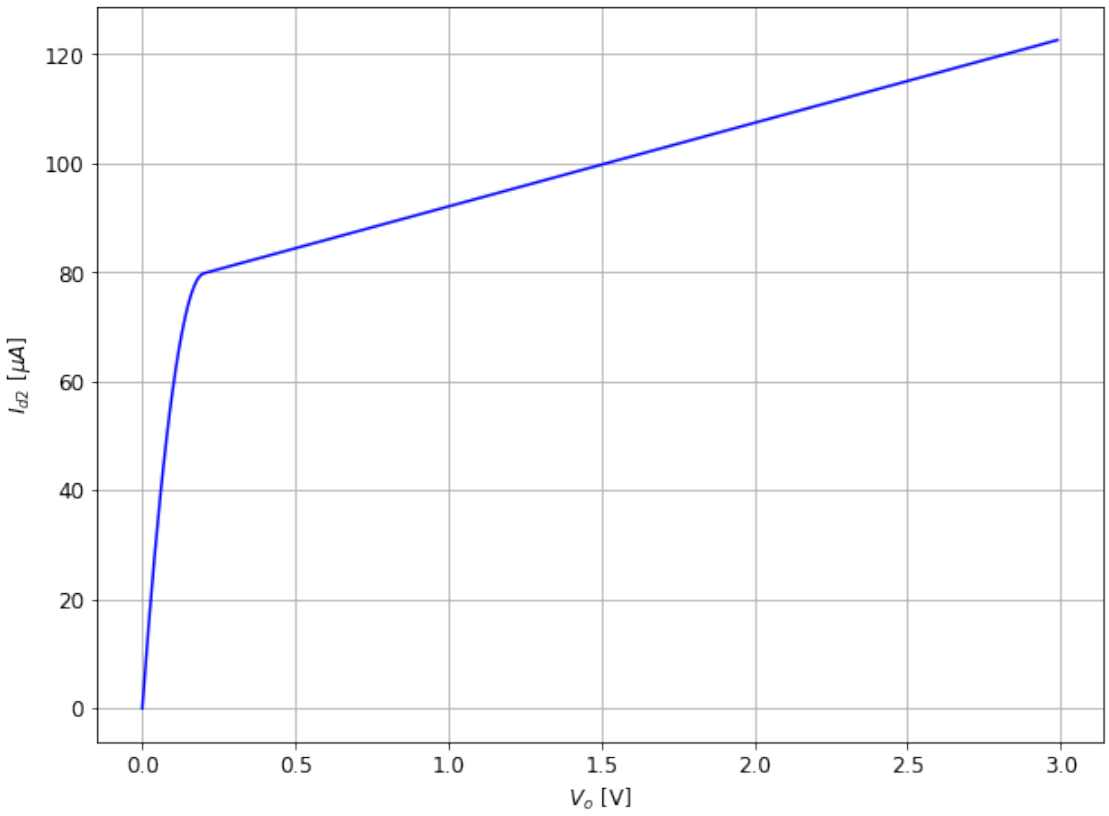
$$\tag{11}$$

$$\approx \lambda_p I_{D2} \tag{12}$$

$$\rightarrow \boxed{R_o \approx \frac{1}{\lambda_p I_{D2}} = r_{o2}} \tag{13}$$

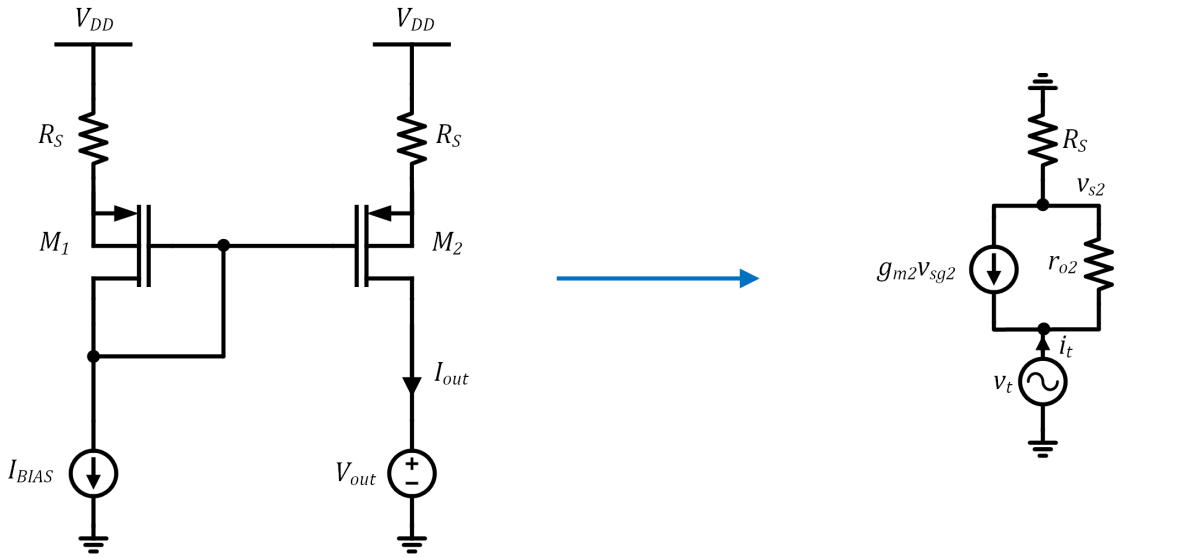
- The output resistance of a current source determines its sensitivity to output voltage
- In the case of a current source based on a single *MOSFET*, the output resistance is equal to the intrinsic output resistance of the transistor, r_o
- Assume that we design our circuit for a nominal operating point of $V_o = 1.5V$ and $I_{D2} = 100\mu A$

[16]:
```
lambda_p = 0.2
V_o = np.arange(0, 3, 0.01)
I_d2 = pmos_iv_sweep(1, V_o, 100, 1, lambda_p)
plot_xy(V_o, 1e6*I_d2, r'$V_{o}$ [V]', r'$I_{d2}$ [$\mu A$]')
```



- The finite output resistance of M_2 causes I_{out} to vary significantly with V_o ($\pm$20%!)
- This will affect various circuit parameters, such as g_m, bandwidth, stability, etc.
- How do we reduce the variability in I_{d2}?

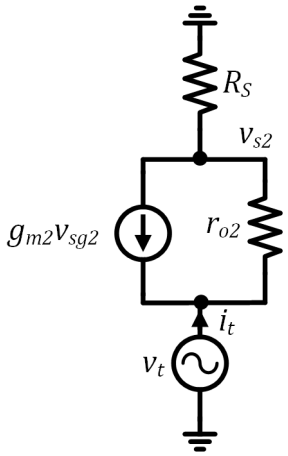
2.7 Source degeneration



$$R_o = \frac{v_t}{i_t} = ? \tag{14}$$

- Resistor between source of $PMOS$ and V_{DD} is referred to as "source degeneration"
- This is a form of negative feedback that increases the output resistance of the current source over that of a MOS transistor alone

2.8 Small-signal behavior



$$i_t = \frac{v_{s2}}{R_S} = -g_{m2}v_{sg2} + \frac{v_t - v_{s2}}{r_{o2}} \tag{15}$$

$$v_{s2} = i_t R_S \tag{16}$$

$$\boxed{R_o = \frac{v_t}{i_t} = r_{o2}(1 + g_{m2}R_S) + R_S} \tag{17}$$

- As v_t increases, so does the source voltage v_{s2}
- This results in an increase in the current $g_{m2}v_{s2}$, which is in the direction opposite to i_t
- The resulting negative feedback increases the output resistance of the degenerated current source

2.9 Increased output resistance

- If we assume a voltage drop across R_S of $200mV$, then

$$R_S = \frac{0.2V}{I_{D2}} \tag{18}$$

- The output resistance of the degenerated current source is

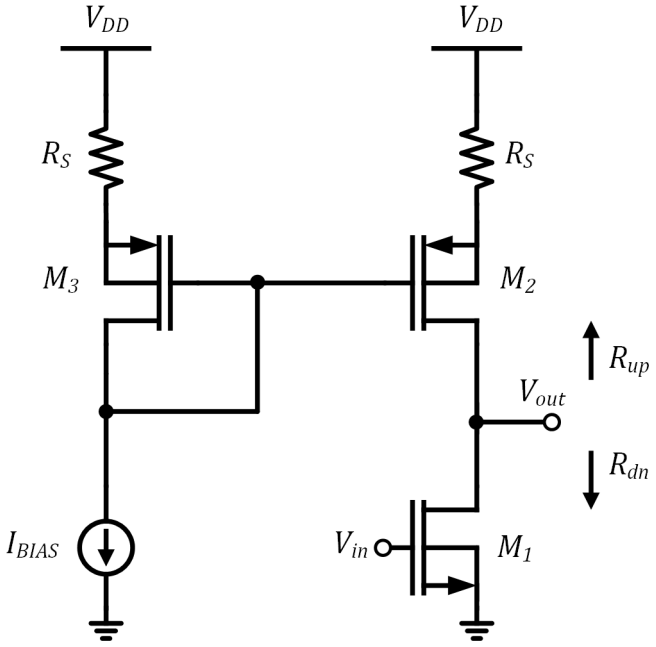
$$R_o = r_{o2}(1 + g_{m2}R_S) + R_S = r_{o2}\left(1 + \frac{2I_{D2}}{V_{OV2}}\frac{0.2V}{I_{D2}}\right) + R_S \tag{19}$$

- For $V_{OV2} = 0.2V$, we obtain

$$R_o = 3r_{o2} + R_S \approx 3r_{o2} \tag{20}$$

- The original output resistance, r_{o2}, is increased by the gain of the feedback loop, $g_{m2}R_S$, and added to the series resistance R_S

2.10 Common-source amplifier with degeneration



$$R_{up} = r_{o2}(1 + g_{m2}R_S) + R_S \tag{21}$$

$$R_{dn} = r_{o1} \tag{22}$$

$$R_o = R_{up}||R_{dn} \tag{23}$$
$$\tag{24}$$
$$= [r_{o2}(1 + g_{m2}R_S) + R_S]\,||r_{o1} \tag{25}$$
$$\tag{26}$$

$$\boxed{A_v = -g_{m1}R_o} \tag{27}$$

- The amplifier output resistance is the parallel combination of the current source resistance and r_{o1}
- Let's take a look at a typical value for this...
- Recall that for $R_S = 0.2V/I_{D2}$ and $V_{OV2} = 0.2V$, the output resistance of the degenerated current source is

$$R_{up} = 3r_{o2} + R_S \approx 3r_{o2} \tag{28}$$

- This small-signal resistance appears in parallel with $R_{dn} = r_{o1}$, resulting in

$$R_o \approx 3r_{o2}||r_{o1} \tag{29}$$

- Using our process model parameters $\lambda_p = 0.2V^{-1}$ and $\lambda_n = 0.1V^{-1}$, we find

$$R_o \approx 3r_{o2}||r_{o1} = \frac{(\frac{3}{\lambda_p I_{D2}})(\frac{1}{\lambda_n I_{D2}})}{\frac{3}{\lambda_p I_{D2}} + \frac{1}{\lambda_n I_{D2}}} = \frac{(\frac{3}{\lambda_p I_{D2}})(\frac{1}{\lambda_n I_{D2}})}{\frac{3\lambda_n + \lambda_p}{\lambda_n \lambda_p I_{D2}}} = \frac{3}{(3\lambda_n + 2\lambda_n)I_{D2}} = \frac{3}{5}r_{on} \tag{30}$$

- We have increased the output resistance (and hence the gain) of the common-source amplifier by about 20%
- Can we do better?
- What if $R_S = r_{op}$?
- In this case, the output resistance of the current source becomes

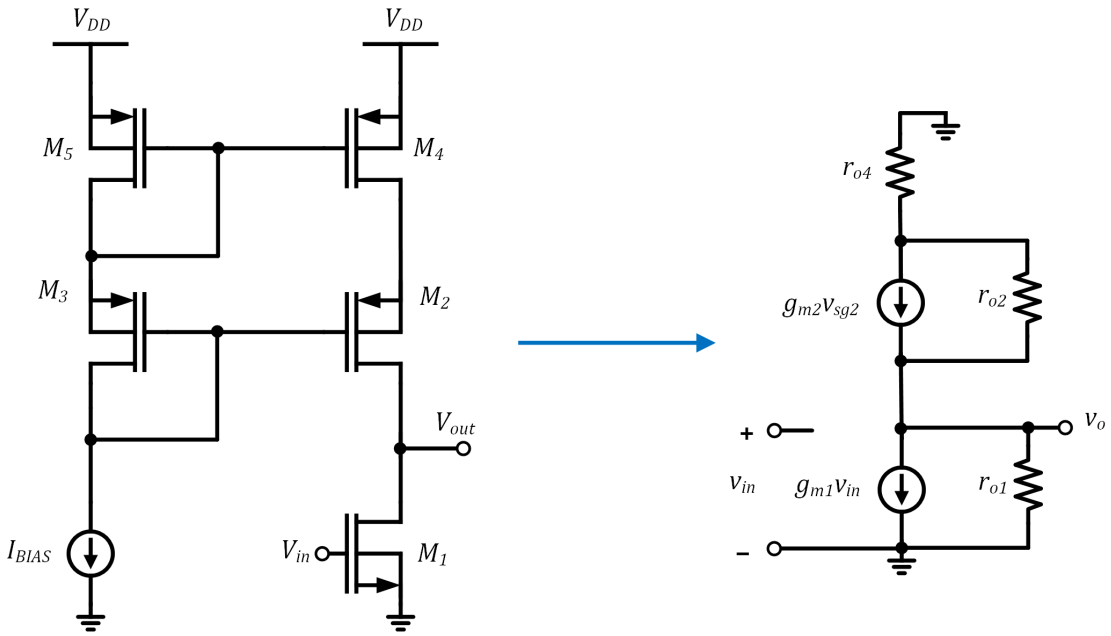
$$R_{up} = r_{op}(1 + g_{m2}r_{op}) + r_{op} \tag{31}$$

- $g_{m2}r_{op}$ is equal to the intrinsic gain of a $PMOS$ transistor. If we take this to be at least $10V/V$, the current source output impedance becomes

$$R_{up} = r_{op}(1 + g_{m2}r_{op}) + r_{op} \geq 12r_{op} \tag{32}$$

- This is more than an order of magnitude higher than the output impedance of a single transistor. How do we achieve this?

2.11 Common-source amplifier with cascode load



- "Cascoding" is source degeneration using r_o in place of R_S
- The *DC* gain of this configuration is

$$A_v = -G_m \cdot R_o = -g_{m1} \cdot r_{o1} || \left[r_{o2}(1 + g_{m2} r_{o4}) + r_{o4} \right] \approx -g_{m1} r_{o1} \tag{33}$$

- By setting the output impedance of the current source to be much greater than that of M_1, our gain is nearly equal to the intrinsic gain of M_1

2.12 Summary (so far)

- Common-source amplifier with resistive load provides only modest gain

$$|A_v| \approx g_{m1} R_D = \frac{2I_{D1}}{V_{OV1}} \frac{V_{DD}/2}{I_{D1}} = \frac{V_{DD}}{V_{OV1}} \tag{34}$$

- An active load increases this slightly

$$|A_v| = g_{m1} \cdot r_{o1} || r_{o2} \approx g_{m1} \frac{r_{o1}}{3} \tag{35}$$

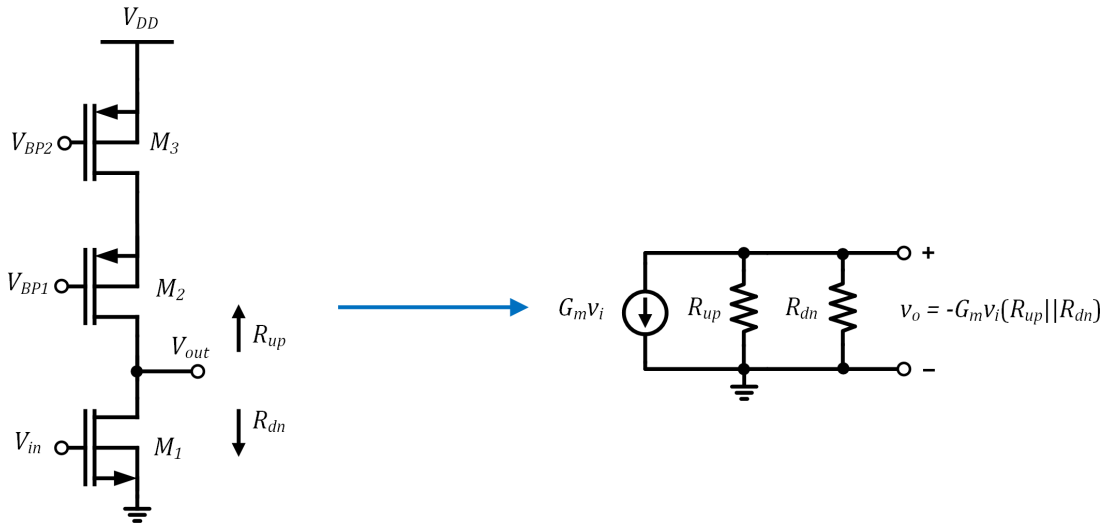
- Source degeneration increases output resistance of current source and (slightly) increases gain

$$|A_v| = g_{m1} \cdot r_{o1} || \left[r_{o2}(1 + g_{m2} R_S) + R_S \right] \approx \frac{3}{5} g_{m1} r_{o1} \tag{36}$$

- The cascode current source significantly increases output resistance of the current source/active load

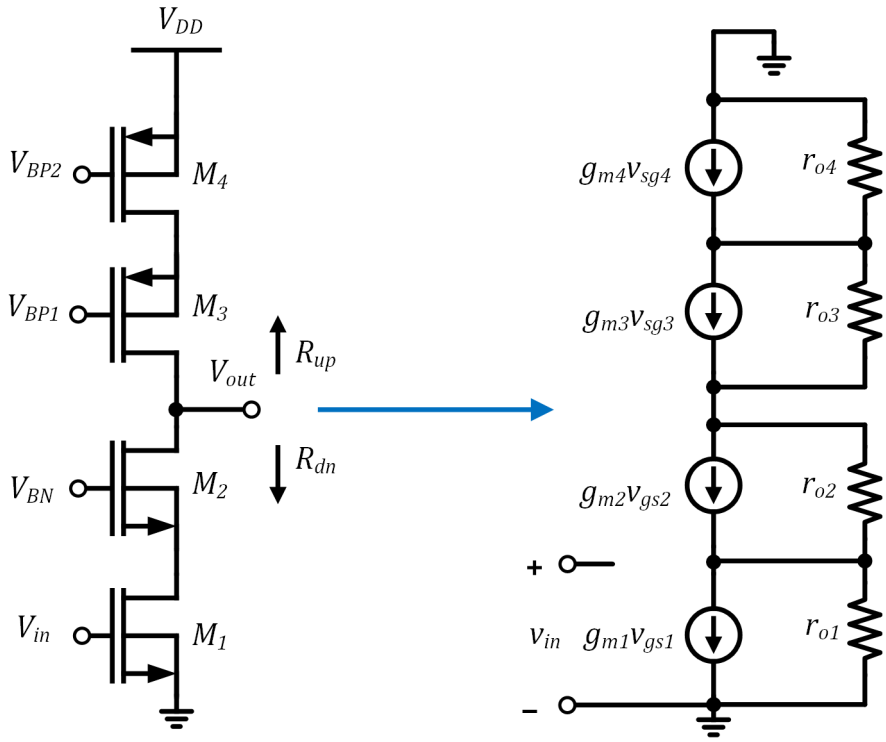
$$|A_v| = g_{m1} \cdot r_{o1} || \left[r_{o2}(1 + g_{m2} r_{o4}) + r_{o4} \right] \approx g_{m1} r_{o1} \tag{37}$$

2.13 Common-source with cascode load



- $R_{up} \approx g_{m2} r_{o2} r_{o3}$, while $R_{dn} = r_{o1}$
- Cascode current-source load impedance (R_{up}) is ~$g_m r_o$ times higher than r_{o1} (R_{dn})
- If we can increase R_{dn} by the same factor, we can significantly increase our gain
- How do we accomplish this?

2.14 Cascode amplifier

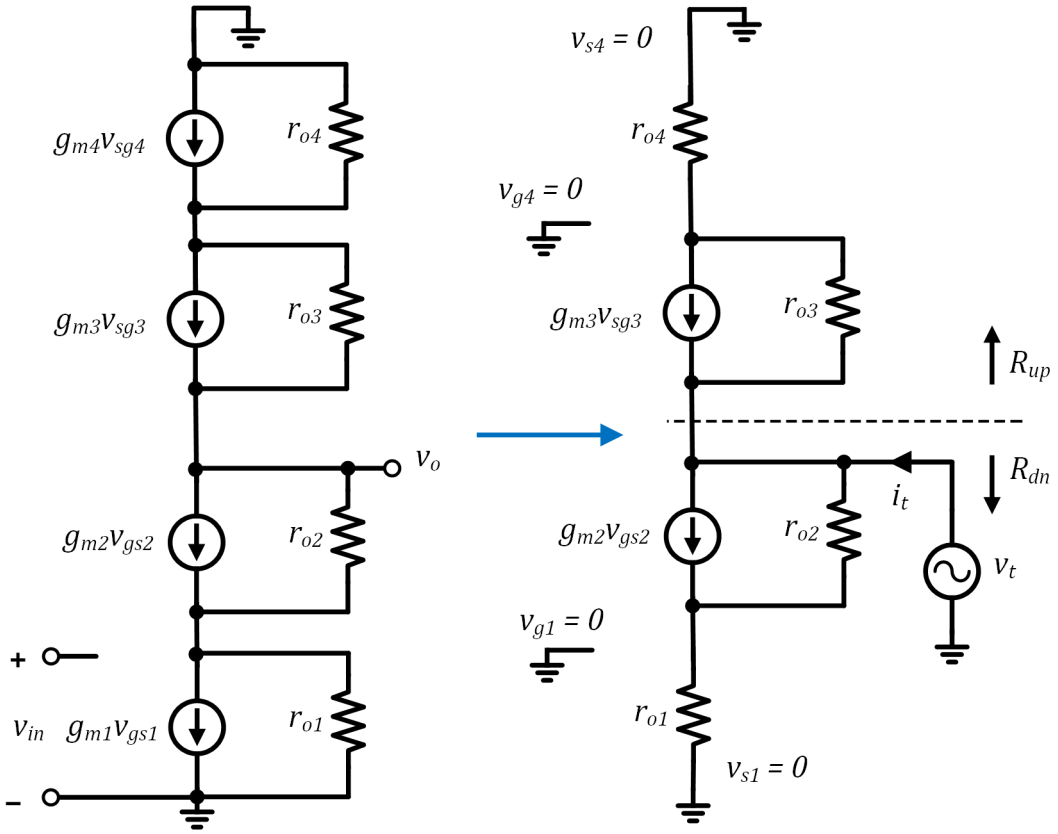


- A "fully cascoded" amplifier consists of symmetric stacks of $NMOS$ and $PMOS$ devices
- Recall that R_{up} is given by

$$R_{up} = r_{o3}(1 + g_{m3}r_{o4}) + r_{o4} \approx g_{m3}r_{o3}r_{o4} \tag{38}$$

- What about R_{dn}?

2.15 Cascode amplifier output impedance (Ro)



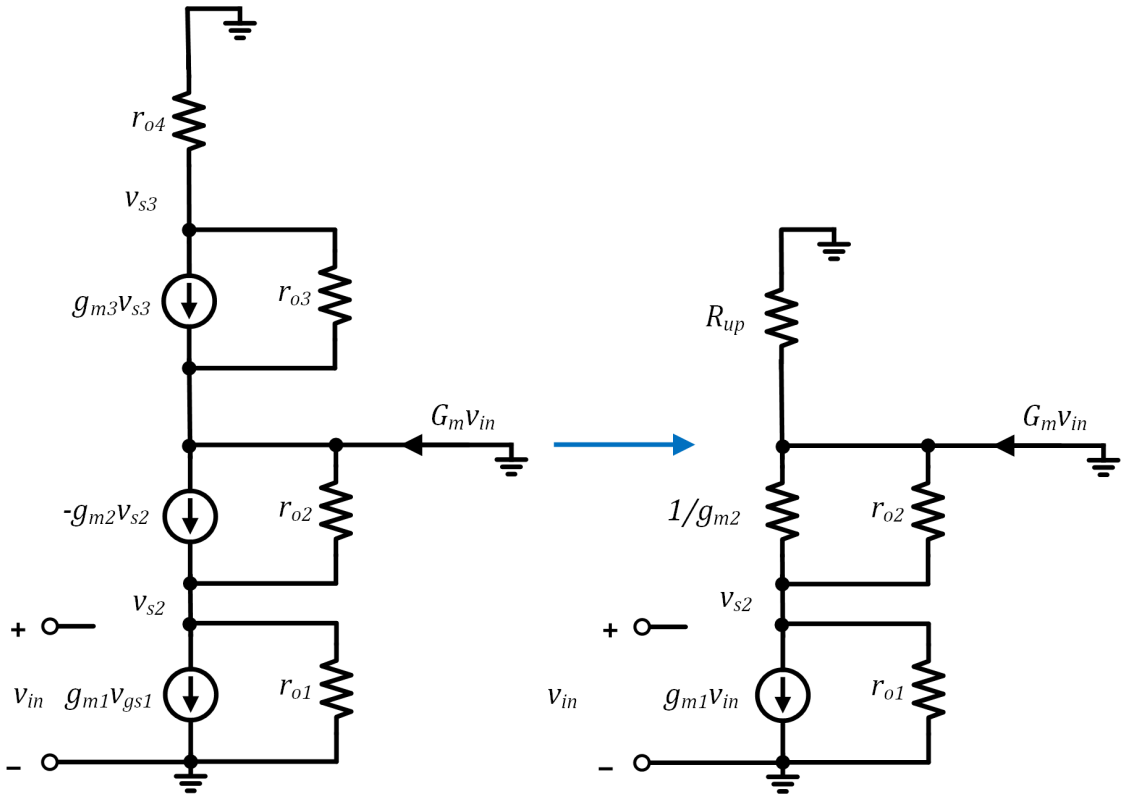
- Input voltage (v_{g1}) is set to zero when determining R_o (Thevenin approach)
- Based on the symmetry of R_{up}, R_{dn}, we can directly write

$$R_{dn} = r_{o2}(1 + g_{m2}r_{o1}) + r_{o1} \approx g_{m2}r_{o2}r_{o1} \tag{39}$$

- The output impedance is the parallel combination of the two:

$$R_o \approx g_{m2}r_{o2}r_{o1} || g_{m3}r_{o3}r_{o4} \approx \frac{g_m r_o^2}{2} \tag{40}$$

2.16 Cascode amplifier output impedance (Gm)

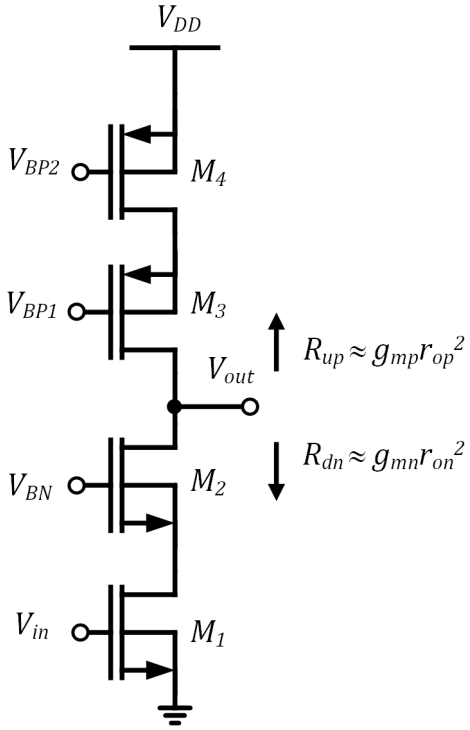


- Current through r_{o1} shunted by parallel combination of $1/g_{m2}$ and r_{o2}:

$$G_m v_{in} = g_{m1} v_{in} \cdot \frac{r_{o1}}{\frac{1}{g_{m2}} || r_{o2} + r_{o1}} \approx g_{m1} v_{in} \tag{41}$$

- As long as $r_{o1}, r_{o2} >> 1/g_{m1}$, G_m is approximately equal to g_{m1}

2.17 Cascode amplifier voltage gain



$$A_v = \frac{v_{out}}{v_{in}} \tag{42}$$

$$\tag{43}$$

$$= -G_m \cdot R_o \tag{44}$$

$$\tag{45}$$

$$\approx \boxed{-g_{m1}[g_{m3} r_{op}^2 || g_{m2} r_{on}^2]} \tag{46}$$

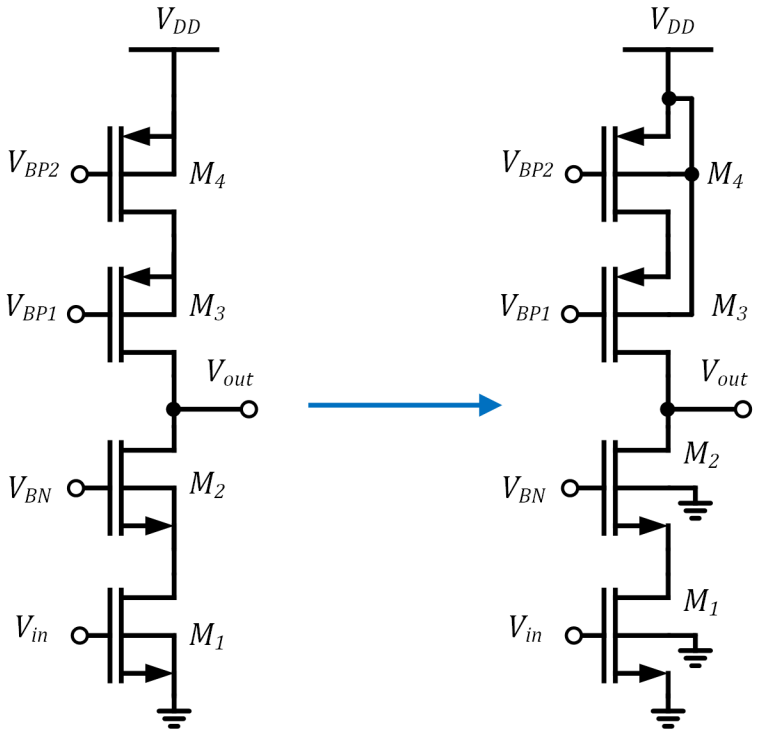
- R_{up} and R_{dn} both based on r_o and scaled by $g_m r_o$ (degeneration)
- Gain is approximately $g_m r_o$ times higher than that of a common source with active load
- Let's put some numbers to this...

- In our Level 1 model, $\lambda_n = 0.1V^{-1}$
- To achieve high gain, we want to use a relatively low overdrive voltage, say $200mV$
- For simplicity, let's assume $g_{mn} r_{on} = g_{mp} r_{op} = g_m r_o$. The cascode amplifier gain is thus

$$|A_v| \approx \frac{g_m^2 r_o^2}{2} = \left(\frac{I_D}{V_{OV}} \frac{1}{\lambda I_D} \right)^2 = 2,500 V/V \tag{47}$$

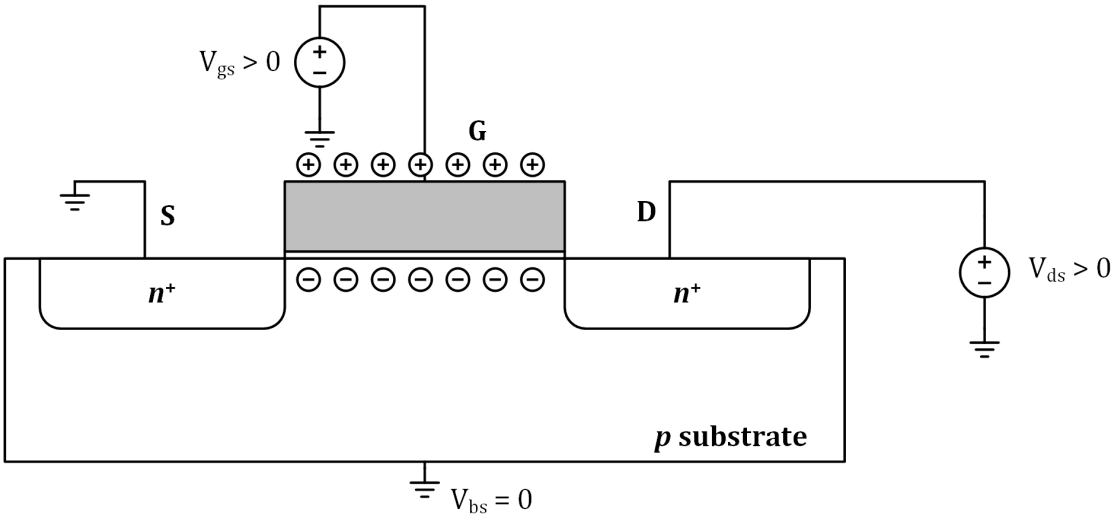
- By "cascoding," we increase our gain from $30dB$ with a resistive load to nearly $70dB$!
- Our actual gain will typically be a bit lower than this, since g_m and r_o won't be the same for all devices

2.18 Cascode bulk connections



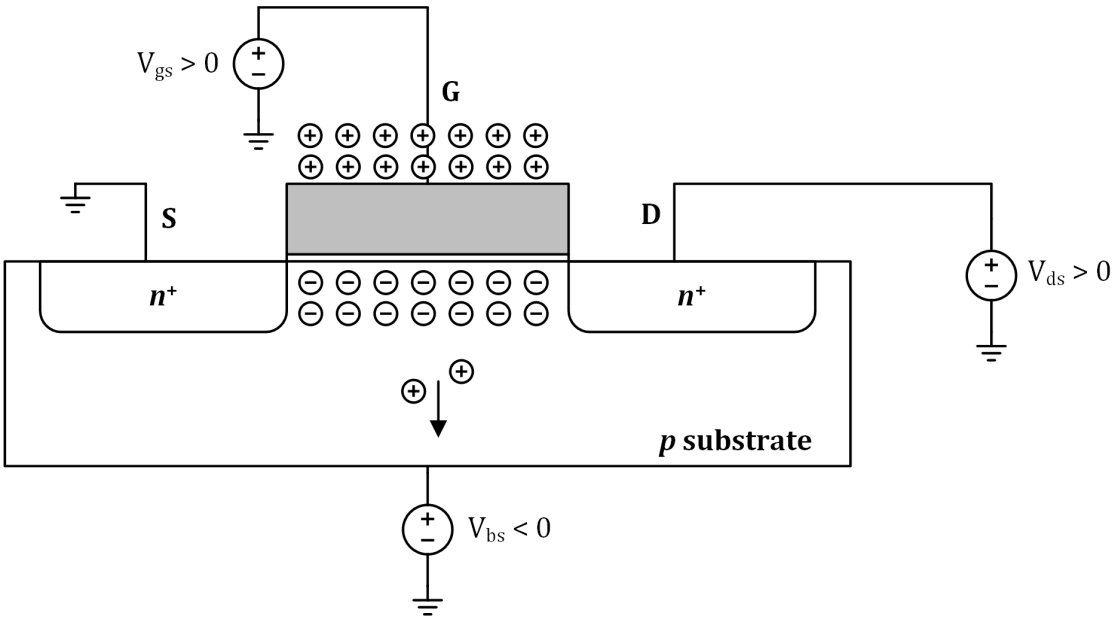
- In the cascode and source-dengerated structures, $PMOS/NMOS$ source terminals may not be connected to V_{DD}/GND
- Whereas $PMOS$ devices are fabricated in *n-wells* and can have independent source potentials, $NMOS$ bulks comprise the chip substrate and must be biased at the same potential ($0V$, in most cases)
- Both the large- and small-signal behavior of the $MOSFET$ are affected by nonzero values of V_{bs} via modulation of the threshold voltage

2.19 Definition of threshold voltage



- As V_{gs} increases from 0, holes are repelled from the substrate region under the gate, leaving behind a negatively-charged depletion region
- Charge balance requries that positive gate charge mirror the immobile depletion charge
- As V_{gs} continues to increase, electrons are attracted from source and drain to form an inversion layer

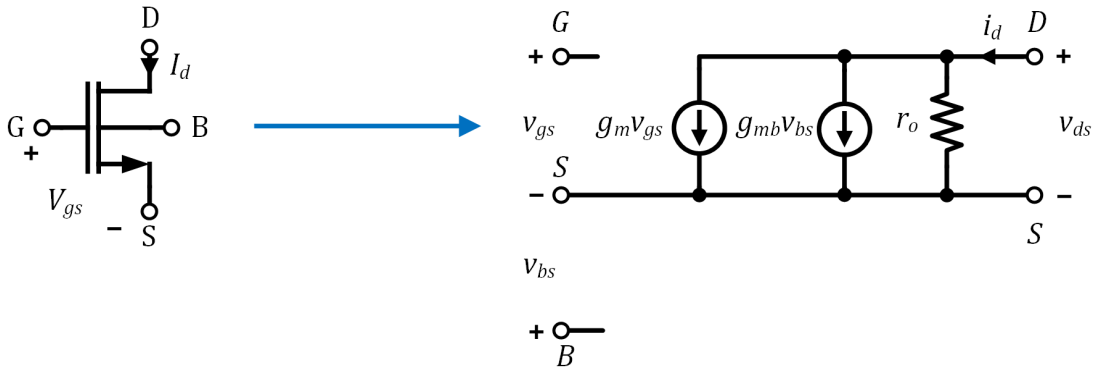
2.20 Body effect (Vbs < 0)



- For $V_{bs} < 0$, some holes are pulled from the interface toward the bulk terminal, resulting in more negative charge in the depletion region
- More positive gate charge is thus required to form an inversion layer, increasing V_{th}
- The threshold voltage thus increases with increasing V_{sb}, and is defined as

$$V_{th} = V_{th0} + \gamma(\sqrt{2\phi_F + V_{sb}} - \sqrt{2\phi_F}) \tag{48}$$

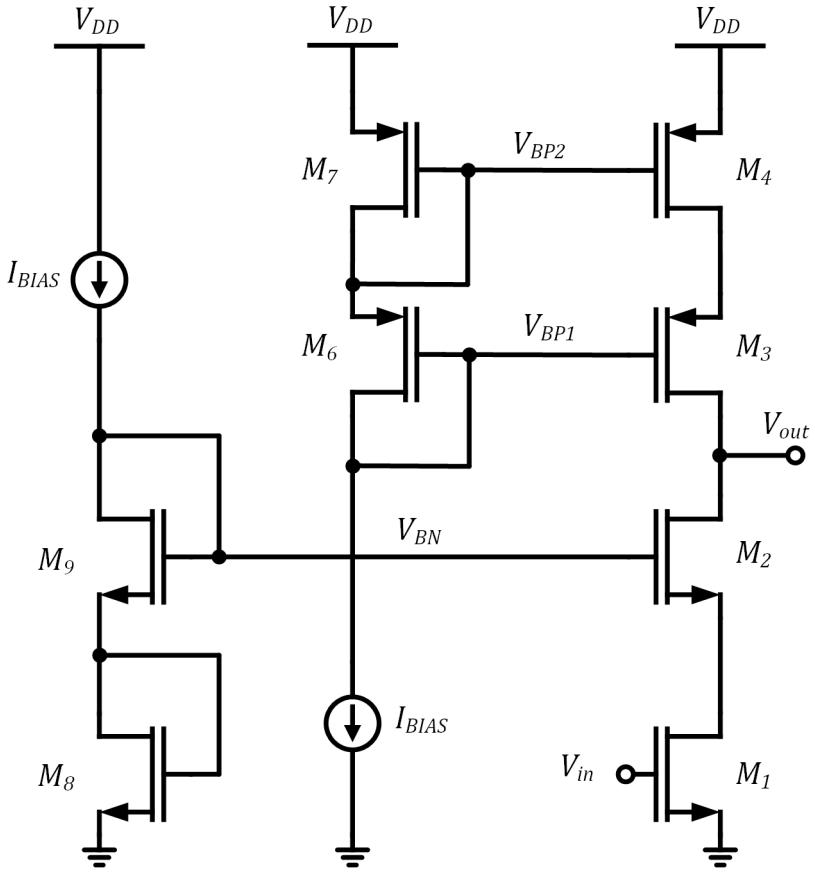
2.21 Body effect (small signal)



$$g_{mb} = \frac{\partial I_D}{\partial V_{BS}} = g_m \frac{\gamma}{2\sqrt{2\phi_F + V_{SB}}} = \eta g_m \tag{49}$$

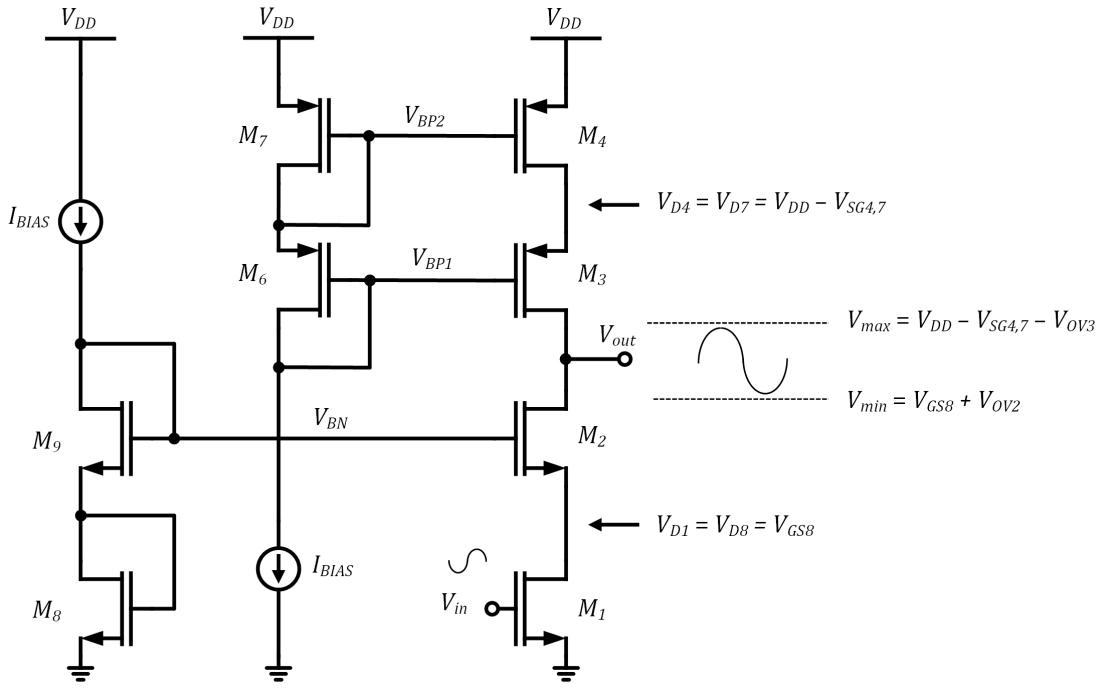
- When $v_{bs} \neq 0$, the bulk terminal acts as a second "gate" (body effect is often referred to as the "back-gate" effect)
- A typical range for γ is between 0.1 and 0.5, depending on the process technology
- Affects source-degenerated, cascode, source follower, and common-gate configurations
- Only needs to be considered when $v_{bs} \neq 0$

2.22 Cascode biasing



- Here is one possible bias configuration (of several) for a cascode amplifier
- A cascode current mirror ($M_{3,4}$, $M_{6,7}$) is used to set the bias voltages V_{BP1} and V_{BP2}
- V_{BN} establishes a gate voltage for M_2, while a diode-connected M_8 ensures that M_2's source is at a high enough potential to keep M_1 in saturation

2.23 Cascode voltage swing



2.24 Summary

- Degeneration and cascoding use negative feedback to signficantly increase the output resistance of the simple current source
- Higher output resistance means greater precision in current mirrors, and higher gain in amplifiers
- Adding a cascode transistor also increases the output resistance of the input path
- The gain of the cascode amplifier is approximately $g_m r_o$ times higher than that of a common-source amplifier with active load
- Device stacking also results in the body effect, which should be considered during design
- The increased output resistance comes at the cost of lower output swing, due to stacking of more transistors