2021_02_10_EE538_Lecture6_W2021

February 10, 2021

1 EE 538: Analog Integrated Circuit Design

1.1 Winter 2021

1.2 Instructor: Jason Silver

1.3 Python packages/modules

[73]:

```
import matplotlib as mpl
from matplotlib import pyplot as plt
import numpy as np
from scipy import signal
#%matplotlib notebook

mpl.rcParams['font.size'] = 12
mpl.rcParams['legend.fontsize'] = 'large'

def plot_xy(x, y, xlabel, ylabel):
    fig, ax = plt.subplots(figsize=(10.0, 7.5));
    ax.plot(x, y, 'b');
    ax.grid();
    ax.set_xlabel(xlabel);
    ax.set_ylabel(ylabel);

def plot_xy2(x1, y1, x1label, y1label, x2, y2, x2label, y2label):
    fig, ax = plt.subplots(2, figsize = (10.0, 7.5));
    ax[0].plot(x1, y1, 'b');
    ax[0].set_ylabel(y1label)
    ax[0].grid()

    ax[1].plot(x2, y2, 'b');
    ax[1].set_xlabel(x1label)
    ax[1].set_xlabel(x2label);
    ax[1].set_ylabel(y2label);
    ax[1].grid();

    fig.align_ylabels(ax[:])
```

```
def plot_x2y(x, y1, y2, xlabel, ylabel, y1label, y2label):

    fig, ax = plt.subplots(figsize=(10.0, 7.5));
    ax.plot(x, y1, 'b')
    ax.plot(x, y2, 'r')
    ax.legend( [y1label,y2label] ,loc='upper center', ncol=5, fancybox=True,
           shadow=True, bbox_to_anchor=(0.5,1.1))
    ax.grid()
    ax.set_xlabel(xlabel)
    ax.set_ylabel(ylabel)

def plot_xy3(x, y1, y2, y3, xlabel, y1label, y2label, y3label):
    fig, ax = plt.subplots(3, figsize=(10.0,7.5))

    ax[0].plot(x, y1)
    ax[0].set_ylabel(y1label)
    ax[0].grid()

    ax[1].plot(x, y2)
    ax[1].set_ylabel(y2label)
    ax[1].grid()

    ax[2].plot(x, y3)
    ax[2].set_ylabel(y3label)
    ax[2].set_xlabel(xlabel)
    ax[2].grid()

def plot_xlogy(x, y, xlabel, ylabel):
    fig, ax = plt.subplots(figsize=(10.0, 7.5));
    ax.semilogy(x, y, 'b');
    ax.grid();
    ax.set_xlabel(xlabel);
    ax.set_ylabel(ylabel);

def nmos_iv_sweep(V_gs, V_ds, W, L, lmda):
    u_n = 350                 # electron mobility (device parameter)
    e_ox = 3.9*8.854e-12/100; # relative permittivity
    t_ox = 9e-9*100;          # oxide thickness
    C_ox = e_ox/t_ox          # oxide capacitance
    V_thn = 0.7                # threshold voltage (device parameter)
    V_ov = V_gs - V_thn
    Ldn = 0.08e-6
    Leff = L - 2*Ldn

    I_d = []

    for i in range(len(V_ds)):
        I_d.append(np.piecewise(V_ds[i], [V_ds[i] < V_ov, V_ds[i] >= V_ov],
                       [u_n*C_ox*(W/Leff)*(V_gs - V_thn - V_ds[i]/
 ↪2)*V_ds[i]*(1+lmda*V_ds[i]) ,
                        0.5*u_n*C_ox*(W/Leff)*(V_gs -␣
 ↪V_thn)**2*(1+lmda*V_ds[i])]))

    return np.array(I_d)

def pmos_iv_sweep(V_sg, V_sd, W, L, lmda):
    u_p = 100                  # electron mobility (device parameter)
    e_ox = 3.9*8.854e-12/100; # relative permittivity
    t_ox = 9e-9*100;           # oxide thickness
    C_ox = e_ox/t_ox           # oxide capacitance
    V_thp = -0.8                 # threshold voltage (device parameter)
    V_ov = V_sg - np.abs(V_thp)
    Ldp = 0.09e-6
    Leff = L - 2*Ldp

    I_d = []

    for i in range(len(V_sd)):
        I_d.append(np.piecewise(V_sd[i], [V_sd[i] < V_ov, V_sd[i] >= V_ov],
                       [u_p*C_ox*(W/Leff)*(V_sg - np.abs(V_thp) - V_sd[i]/
 ↪2)*V_sd[i]*(1+lmda*V_sd[i]) ,
                        0.5*u_p*C_ox*(W/Leff)*(V_sg - np.
 ↪abs(V_thp))**2*(1+lmda*V_sd[i])]))

    return np.array(I_d)

def nmos_iv_sat(V_gs, V_ds, W, L, lmda):
    u_n = 350                  # electron mobility (device parameter)
    e_ox = 3.9*8.854e-12/100; # relative permittivity
    t_ox = 9e-9*100;           # oxide thickness
    C_ox = e_ox/t_ox           # oxide capacitance
    V_thn = 0.7                 # threshold voltage (device parameter)
    V_ov = V_gs - V_thn
    Ldn = 0.08e-6
    Leff = L - 2*Ldn

    I_d = 0.5*u_n*C_ox*(W/Leff)*(V_gs - V_thn)**2*(1+lmda*V_ds)

    return I_d

def nmos_diff_pair(V_id, I_ss, R_D, W, L, V_dd):
    u_n = 350                  # electron mobility (device parameter)
    e_ox = 3.9*8.854e-12/100; # relative permittivity
    t_ox = 9e-9*100;           # oxide thickness
    C_ox = e_ox/t_ox           # oxide capacitance
    V_thn = 0.7                 # threshold voltage (device parameter)
    Ldn = 0.08e-6
    Leff = L - 2*Ldn

    I_dp = I_ss/2 + 0.25*u_n*C_ox*(W/L)*V_id*np.sqrt(4*I_ss/(u_n*C_ox*(W/L)) - V_id**2)
    I_dm = I_ss/2 - 0.25*u_n*C_ox*(W/L)*V_id*np.sqrt(4*I_ss/(u_n*C_ox*(W/L)) - V_id**2)

    return I_dp, I_dm
```

2 Lecture 6 - Frequency Response of MOS Amplifiers

2.1 Announcements

- Assignment 5 posted, due Sunday February 14
  - PDF submission on Canvas
- Midterm exam will be available February 15-21 (due the 21st)
  - 180-minute time limit, administered as a Canvas quiz
  - Will cover material through Lecture 5
    - MOS physics/operation
    - Small-signal model
    - Single-stage amplifiers
    - Current mirrors and biasing
    - Differential amplifiers

2.2 Week 6

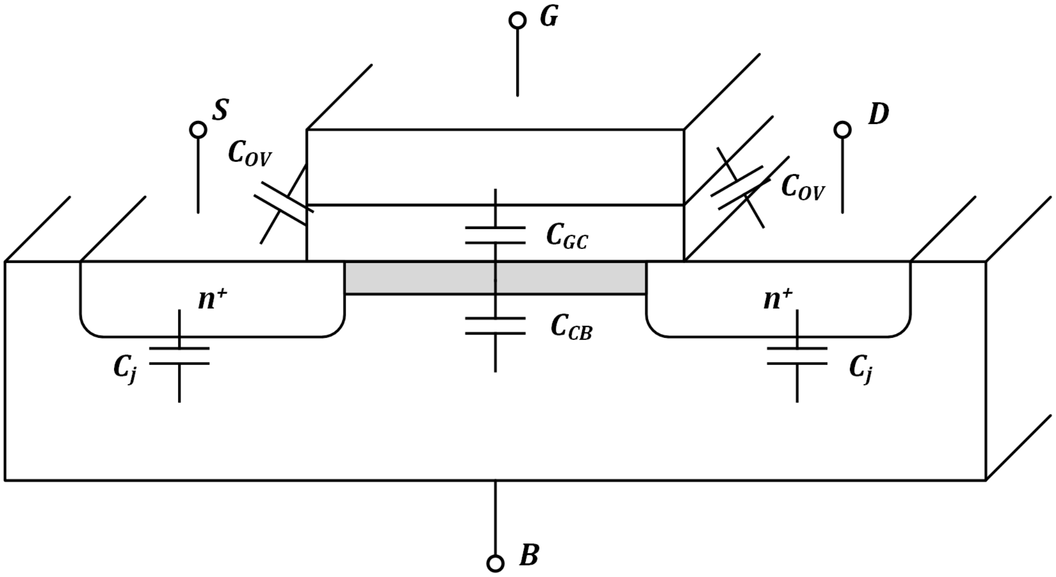
- Chapter 2 of Razavi (MOS physics)
  - Section 2.4.2 MOS Device Capacitances
- Chapter 6 of Razavi (frequency response)
  - Section 6.2 Common Source Stage
  - Section 6.3 Source Followers
  - Section 6.5 Cascode Stage
  - Section 6.6 Differential Pair
  - Section 6.7 Gain-Bandwidth Tradeoffs

2.3 Overview

- Last time…
  - Single-ended vs differential signaling
  - Differential amplifiers
  - 5-transistor MOS OTA
  - Telescopic and Folded Cascode OTAs
- Today…
  - MOS capacitance

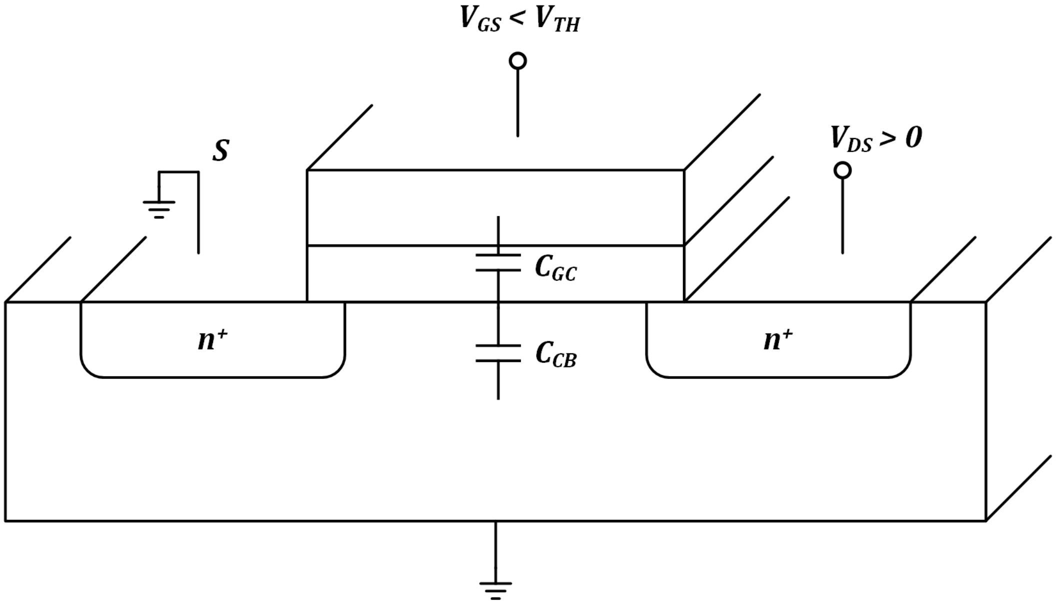
- – Common source amplifier
- – Miller Effect
- – Zero Value Time Constant (ZVTC) analysis
- – Gain-bandwidth product

2.4 MOS device capacitance



- MOS model comprises both intrinsic and extrinsic capacitances
- Intrinsic capacitances (C_{GC}, C_{GB}) are fundamental to device operation
- Extrinsic capacitances (C_j, C_{OV}) are incidental to its structure

2.5 Intrinsic capacitance: subthreshold



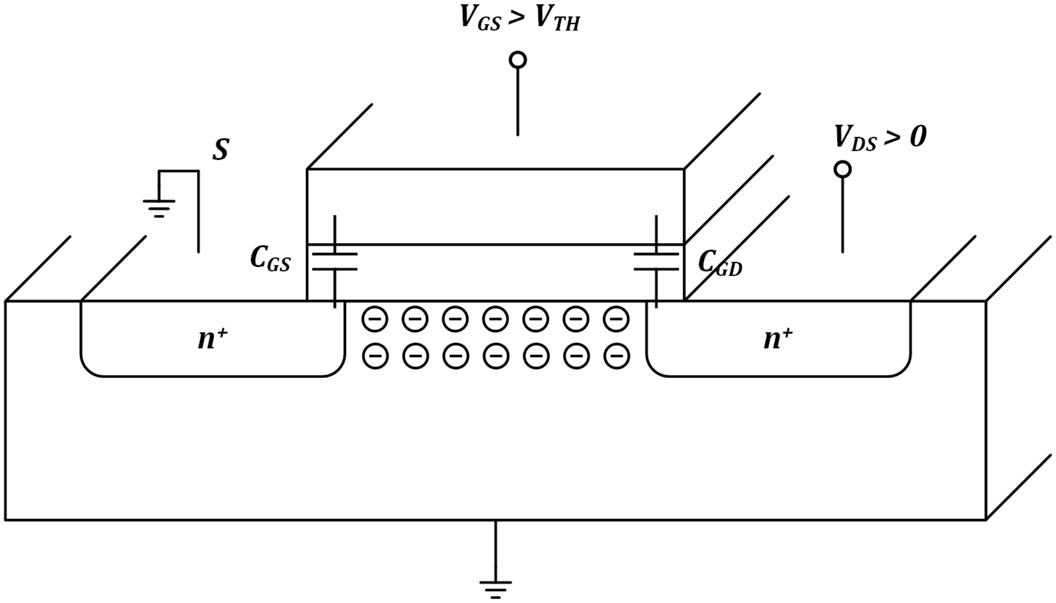
$$C_{CB} = WL\sqrt{\frac{q\epsilon_{Si}N_{sub}}{4\phi_F}} \tag{1}$$

$$C_{GC} = WLC_{ox} \tag{2}$$

$$\boxed{C_G = \frac{C_{CB}C_{GC}}{C_{CB} + C_{GC}}} \tag{3}$$

- For $V_{GS} < V_{th}$ no conductive channel exists between source and drain
- C_{GC} and C_{CB} form a series capacitance
- The ratio of C_{GC} to C_{CB} sets the factor n in the subthreshold drain current expression

2.6 Intrinsic capacitance: triode

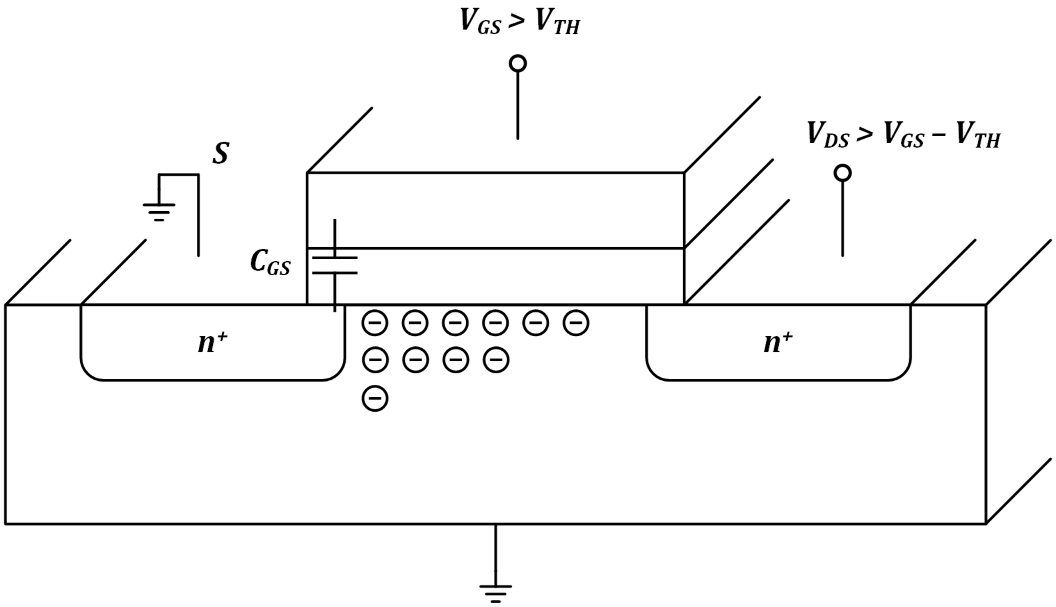


$$C_{GS} - C_{GD} = \frac{1}{2}WLC_{ox} \tag{4}$$

$$\boxed{C_G = C_{GS} + C_{GD} = WLC_{ox}} \tag{5}$$

- In triode, the gate and channel form a parallel plate capacitance $CGC = WL\epsilon_{ox}/t_{ox} = WLC_{ox}$
- Approximation using lumped capacitance C_{GS} and C_{GD} between gate-source and gate-drain terminals, each equal to $C_{GC}/2$
- Depletion (junction) capacitance is typically negligible in comparison

2.7 Intrinsic capacitance: saturation

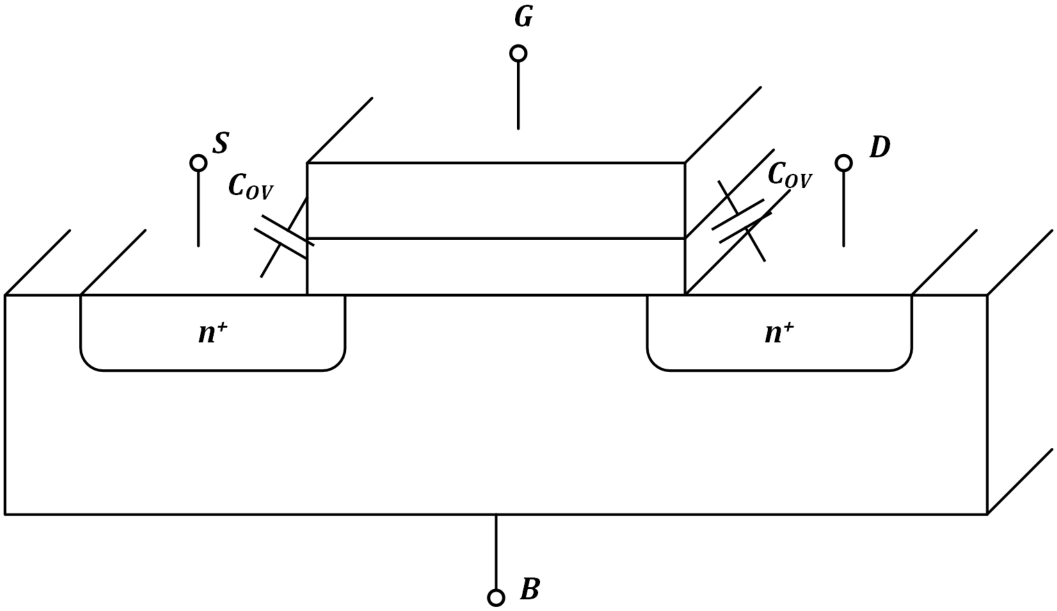


$$C_{GD} \approx 0 \tag{6}$$

$$\boxed{C_G = C_{GS} = \frac{2}{3} WLC_{ox}} \tag{7}$$

- In saturation, the "bottom plate" associated with C_{GC} isn't uniform along the channel
- Detailed analysis gives $C_G = C_{GS} = (2/3)WLC_{ox}$
- Drain voltage no longer affects channel charge, so $C_{GD} = 0$

2.8 Extrinsic capacitance (COV)

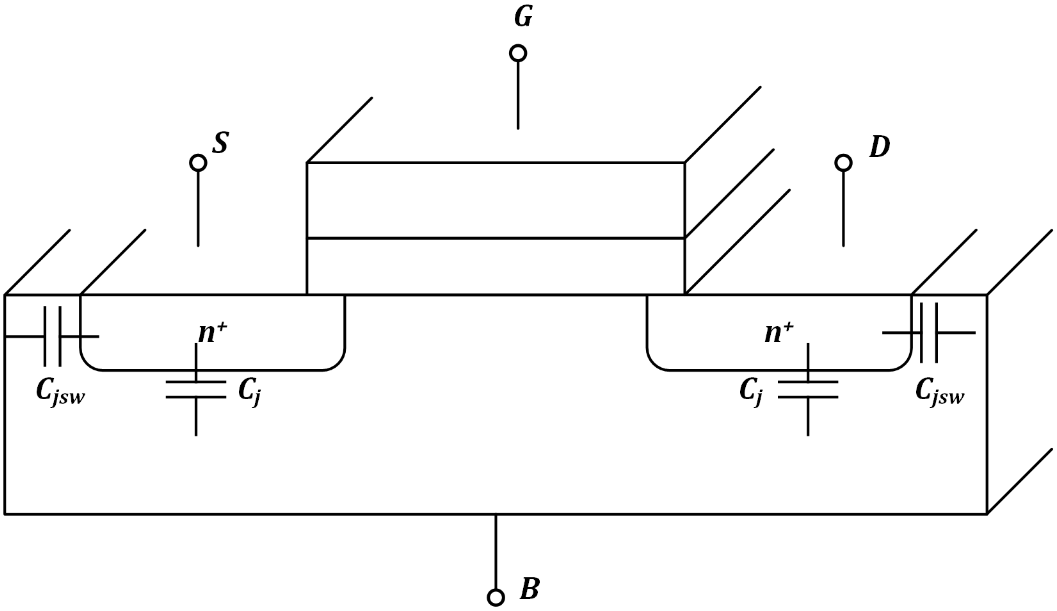


$$\boxed{C_{OV} = WC_{GD0}} \tag{8}$$

$$[C_{GD0}] = F/m \tag{9}$$

- Due to diffusion during device fabrication, both source and drain regions extend under the gate by ΔL
- The overlap between gate polysilicon and S/D regions results in a capacitance-per-unit-width C_{OV}
- “Fringe” electric fields also contribute to the capacitance

2.9 Extrinsic capacitance (Cj)



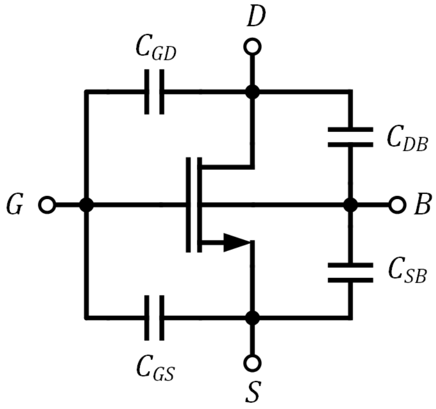
$$\boxed{C_{j,tot} = A_{SD}C_j + P_{SD}C_{jsw}} \tag{10}$$

$$[C_j] = F/m^2 \tag{11}$$

$$[C_{jsw}] = F/m \tag{12}$$

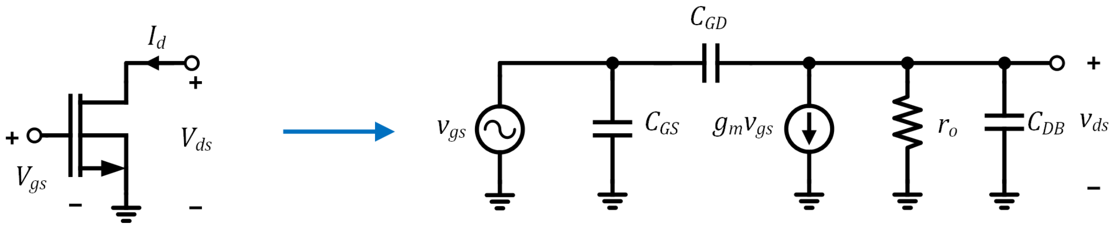
- Source and drain regions form *pn*-junction capacitances with the bulk semiconductor (C_{SB}, C_{DB})
- These junctions are nominally reverse-biased (for an NMOS transistor, the bulk is biased at the most negative potential in the system, typically ground)
- Similarly for PMOS devices, the *n*-type bulk is biased at V_{DD}, reverse-biasing the junction
- Junction capacitances scale with transistor width

2.10 MOS saturation model



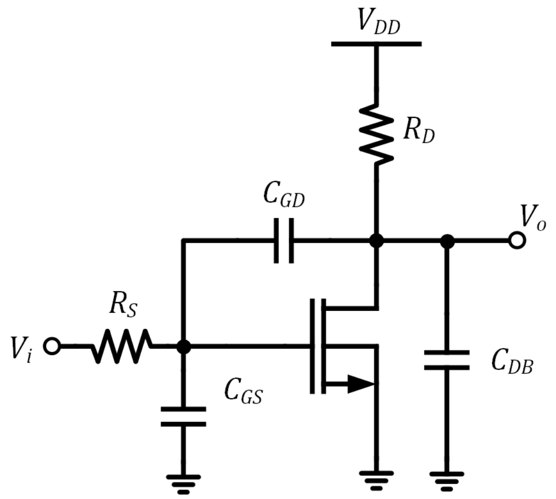
- MOS capacitance in saturation is largely dominated by C_{GS}, so in many cases other capacitances are neglected in hand calculations
- All intrinsic/extrinsic capacitances increase with gate dimensions, such that larger transistors exhibit higher capacitance
- The ultimate limit of usability of the MOS transistor as a gain element is determined by intrinsic device capacitance, and is described by the transit frequency (f_t) of a device

2.11 Small-signal MOS model (AC)



- In analog design, we typically use MOS devices in a common-source or current-source configuration
- Small-signal models quickly become unwieldy due to the large number of devices/parameters
- Again, we should use the simplest model that is accurate enough for our purposes!

2.12 Common-source amplifier

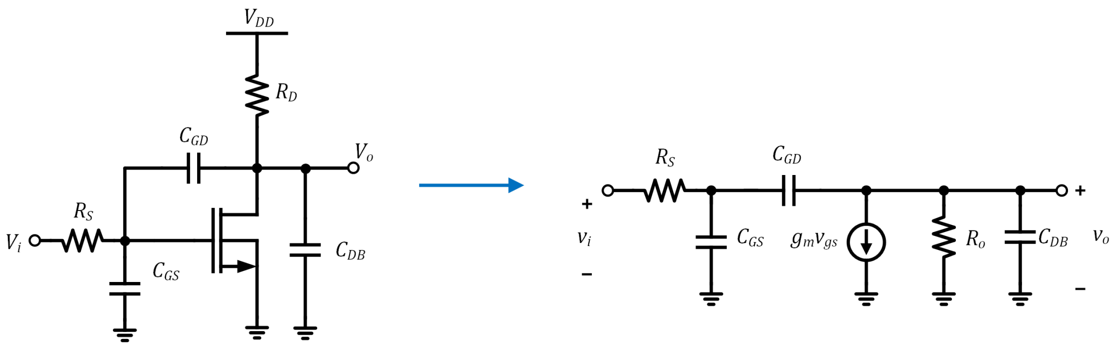


- We are interested in finding v_o/v_i (small-signal gain) as a function of frequency:

$$A_v(s) = \frac{v_o}{v_i}(s) = ? \tag{13}$$

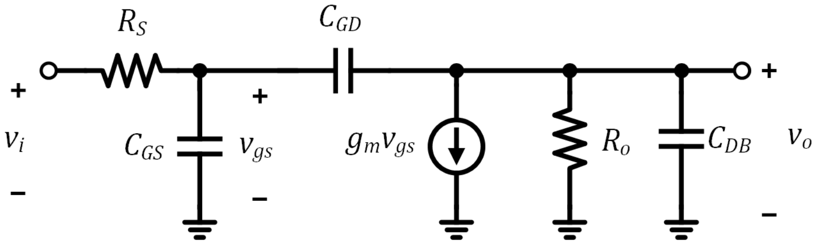
- Device capacitance plays a role, as do other capacitances (e.g. load capacitors or subsequent stage parasitics) - For now, we'll perform our analysis with only the MOS capacitances

2.13 Common-source small-signal model



- Complete small-signal model includes g_m, r_o, and MOS capacitances
- Small-signal analysis is a bit more involved that at DC, but hand analysis is still manageable for one or two devices
- The output resistance is given by $R_o = r_o || R_D$
- R_S represents the output (Thevenin) resistance of the previous stage

2.14 Complete small-signal analysis



$$\frac{v_i - v_{gs}}{R_S} = sC_{GS}v_{gs} + sC_{GD}(v_{gs} - v_o) \tag{14}$$

$$sC_{GD}(v_{gs} - v_o) = g_m v_{gs} + v_o\left(sC_{GB} + \frac{1}{R_o}\right) \tag{15}$$

- This system of equations is deceptively simple!
- Let's solve for v_o/v_i...

- The small-signal AC model is used to obtain two KCL equations, one for the gate node and one for the drain

$$\frac{v_i - v_{gs}}{R_S} = sC_{GS}v_{gs} + sC_{GD}(v_{gs} - v_o) \tag{16}$$

$$sC_{GD}(v_{gs} - v_o) = g_m v_{gs} + v_o\left(sC_{GB} + \frac{1}{R_o}\right) \tag{17}$$

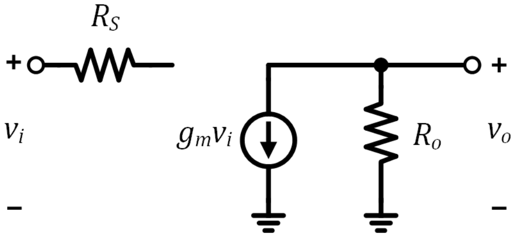
- From this pair of equations we obtain

$$A_v(s) = \frac{v_o}{v_i} = \frac{(sC_{GD} - g_m)R_o}{R_S R_o \xi s^2 + [R_S(1 + g_m R_o)C_{GD} + R_S C_{GS} + R_D(C_{GD} + C_{DB})]s + 1} \tag{18}$$

- where the term ξ is given by

$$\xi = C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB} \tag{19}$$

2.15 Low-frequency response



- To understand the performance of the amplifier at low frequencies, we can "open-circuit" capacitances in the small-signal model

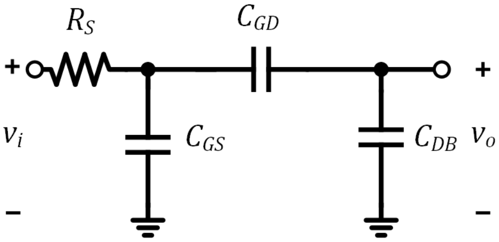
- The transfer function of the common-source amplifier is given by

$$A_v(s) = \frac{(sC_{GD} - g_m)R_o}{R_S R_o \xi s^2 + [R_S(1+g_m R_o)C_{GD} + R_S C_{GS} + R_o(C_{GD}+C_{DB})]s + 1} \tag{20}$$

- If we let $s \to 0$, we obtain the low-frequency (DC) response

$$\lim_{s\to 0} A_v(s) = -g_m R_o = -g_m r_o || R_D \approx \boxed{-g_m R_D} \tag{21}$$

2.16 High-frequency response



- To assess the behavior of the circuit at high frequencies, we note that capacitances will shunt (i.e. short-circuit) other circuit elements due to the fact that their impedances are decreasing with frequency
- As $s \to \infty$ in the transfer function, we obtain

$$\lim_{s\to\infty} A_v(s) = \frac{C_{GD}}{sR_S(C_{GS}C_{GD} + C_{GS}C_{DB} + C_{GD}C_{DB})} \tag{22}$$

2.17 Common-source dominant pole

- The common-source transfer function can be expressed as

$$A_v(s) = \frac{(sC_{GD} - g_m)R_o}{R_S R_o \xi s^2 + [R_S(1+g_m R_o)C_{GD} + R_S C_{GS} + R_o(C_{GD}+C_{DB})]s + 1} \tag{23}$$

$$\tag{24}$$

$$= \frac{(sC_{GD} - g_m)R_o}{\dfrac{s^2}{\omega_{p1}\omega_{p2}} + \left(\dfrac{1}{\omega_{p1}} + \dfrac{1}{\omega_{p2}}\right)s + 1} \tag{25}$$

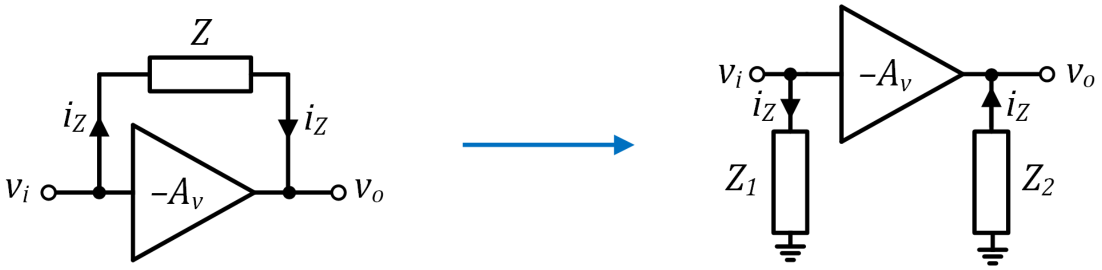
- If we assume that $\omega_{p1} << \omega_{p2}$ (the so-called "dominant-pole approximation"), ω_{p1} can be approximated as

$$\omega_{p1} \approx \frac{1}{R_S(1+g_m R_o)C_{GD} + R_S C_{GS} + R_D(C_{GD}+C_{DB})} \tag{26}$$

2.18 Common-source frequency response

- By making some assumptions (i.e. the dominant pole approximation) we were able to arrive at some results that provide some design insight
- However, this was only possible after somewhat lengthy (small-signal) analysis, and this even for a circuit with only a single transistor
- Let's look at a couple of useful methods for simplifying the frequency response analysis of MOS circuits: Miller's Theorem and Zero-Value Time Constant Analysis

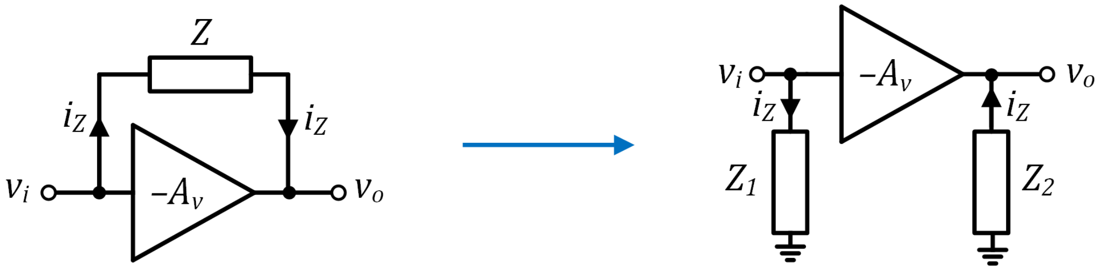
2.19 Miller's Theorem



(a) (b)

- Theorem: If Circuit (a) can be represented as Circuit (b), then Z_1 and Z_2 can be given by

$$Z_1 = \frac{Z}{1 + A_v} \qquad Z_2 = Z \cdot (1 + A_v) \tag{27}$$



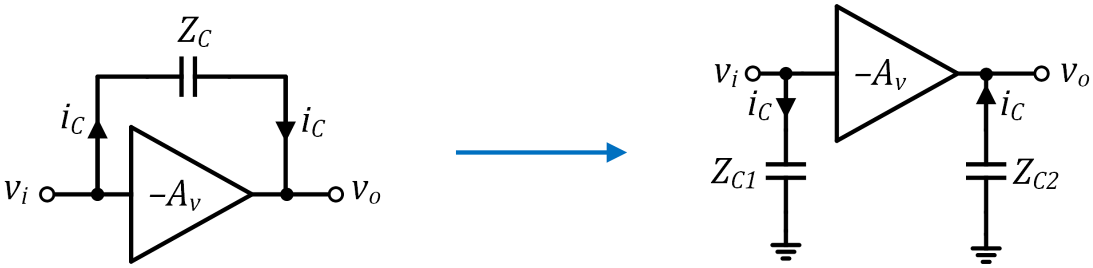
(a) (b)

- The current through Z, i_Z, is given by

$$i_Z = \frac{v_i - v_o}{Z} = \frac{v_i(1 + A_v)}{Z} = \frac{-v_o\left(\frac{1}{A_v} + 1\right)}{Z} \tag{28}$$

- We can then relate Z_1 and Z_2 to i_Z and the node voltages v_i and v_o

$$Z_1 = \frac{v_i}{i_Z} = \frac{Z}{1 + A_v} \qquad Z_2 = -\frac{v_o}{i_Z} = \frac{Z}{\frac{1}{A_v} + 1} = \frac{A_v Z}{A_v + 1} \tag{29}$$



$$Z_{C1} = \frac{Z_C}{1 + A_v} = \frac{1}{sC(1 + A_v)} = \frac{1}{sC_1} \tag{30}$$

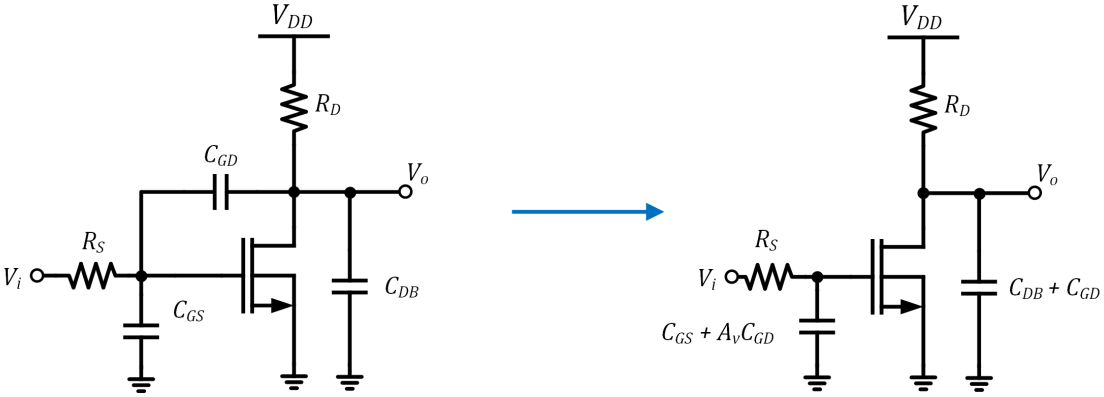
$$\boxed{C_1 = (1 + A_v) \cdot C \approx A_v \cdot C} \tag{31}$$

$$Z_{C2} = \frac{A_v Z_C}{1 + A_v} = \frac{A_v}{sC(1 + A_v)} = \frac{1}{sC_2} \tag{32}$$

$$\boxed{C_2 = \frac{(1 + A_v) \cdot C}{A_v} \approx C} \tag{33}$$

- Due to the amplification of v_i by A_v, the voltage across capacitor C is increased by a factor A_v
- This increases the current through C by the same factor (A_v), increasing the *effective* capacitance "seen" by v_i (C_1) by A_v
- From the perspective of v_o, v_i appears as a small-signal ground, so the effective capacitance for v_o (C_2) is just C

2.20 Common-source Miller approximation



- By applying Miller's Theorem to the common-source amplifier, we greatly simplify the analysis of its frequency response
- Note that in using Miller's approximation, we neglect a zero in the transfer function, as well as interaction between the input and output nodes of the amplifier

2.21 Input and output poles

- The input pole is given by

$$\omega_{p1} \approx \frac{1}{R_S(C_{GS} + A_v C_{GD})} \tag{34}$$

- And the output pole is predicted to be

$$\omega_{p2} \approx \frac{1}{R_o(C_{DB} + C_{GD})} \tag{35}$$

- This is an intuitive approach, and it provides a fair estimate of the input pole frequency
- However, due to its neglect of the interaction between v_i and v_o, Miller's approach provides a poor estimate of the output pole

2.22 Zero-value time constant (ZVTC) analysis

$$A_v(s) = \frac{v_o}{v_i}(s) = \frac{A_0}{(\tau_1 s + 1)(\tau_2 s + 1) \cdots (\tau_n s + 1)} = \frac{A_0}{D(s)} \tag{36}$$

$$D(s) = b_n s^n + b_{n-1} s^{n-1} + \cdots b_1 s + 1 \tag{37}$$

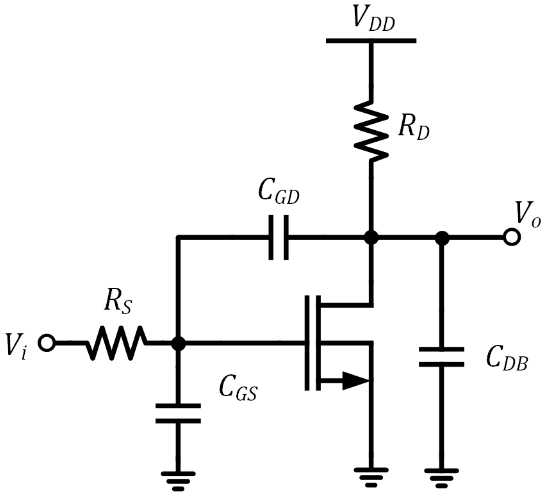
$$A(s) \approx \frac{A_0}{b_1 s + 1} = \frac{A_0}{(\sum_{i-1}^{n} \tau_i)s + 1} \qquad \omega_{3dB} \approx \frac{1}{b_1} \tag{38}$$

- Transfer function an nth order polynomial with coefficients comprised of n time constants
- With the dominant pole assumption, the $3dB$ frequency can be calculated using the linear term coefficient, b_1

2.23 Applying the ZVTC method

- To determine $\tau_1 \cdots \tau_n$ we short the input voltage and find the resistance seen by each capacitor in the circuit
- To find the resistance seen by the i^{th} capacitor C_i, open-circuit (remove) the other capacitances and replace the i^{th} capacitor with a test voltage
- Compute the resistance R_i by taking the ratio of the applied voltage v_t to the resulting current i_t
- The i^{th} time constant is computed as the product of C_i and R_i

2.24 Common-source using ZVTC



$$\tau_1 = R_o C_{DB} \tag{39}$$

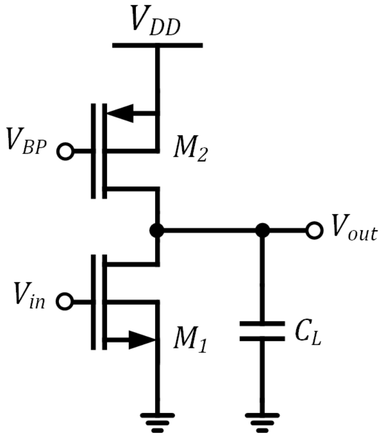
$$\tau_2 = R_S C_{GS} \tag{40}$$

$$\tau_3 = (R_o + g_m R_S R_o + R_S) C_{GD} \tag{41}$$

$$\omega_{3dB} \approx \frac{1}{R_S(1+g_m R_o)C_{GD} + R_S C_{GS} + R_o(C_{DB}+C_{GD})} \tag{42}$$

- We arrive at an accurate expression for ω_{p1} by an intuitive approach
- The ZVTC method still has limitations (e.g. when poles are close together)
- We should combine the ZVTC method with SPICE/Cadence for design

2.25 Dominant-pole behavior



- DC gain:

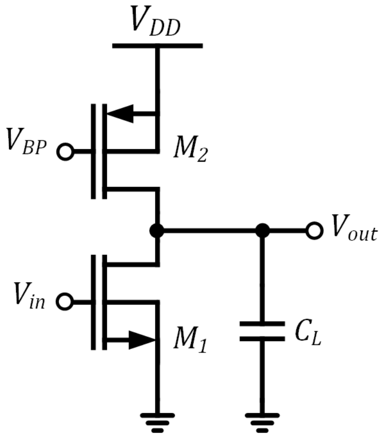
$$A_{v,DC} = -g_m R_o \tag{43}$$

- Output pole:

$$\omega_{3dB} \approx \frac{1}{R_o C_L} \tag{44}$$

- For many applications we need to assume (or guarantee) that our amplifiers exhibit behavior similar to that of single-pole circuits (this is for stability reasons, which we'll discuss later)
- We do this by ensuring one pole is "dominant," i.e. much lower in frequency than other poles
- Here we are assuming that C_L is large enough for us to ignore other "parasitic" capacitances

2.26 Gain-bandwidth product



- DC gain:

$$A_{v,DC} = -g_m R_o \tag{45}$$

- Output pole:

$$\omega_{3dB} \approx \frac{1}{R_o C_L} \tag{46}$$

- If we assume dominant-pole behavior for the common-source amplifier, we can evaluate its gain-bandwidth product as

$$GBW \approx |A_{v,DC}| \cdot f_{3dB} = g_m R_o \cdot \frac{1}{2\pi R_o C_L} = \frac{g_m}{2\pi C_L} \tag{47}$$

- In many practical cases the gain-bandwidth product turns out to be a constant that is *independent of output resistance*

- This can be explained by the observation that as R_o increases, gain increases while bandwidth decreases, keeping their product constant

2.27 Summary

- The high-frequency behavior of MOS amplifiers is limited by intrinsic and extrinsic transistor capacitances
- The frequency dependence of an amplifier's gain, input, and output impedances can be quantified in terms of poles and zeros contributed by those capacitances
- The dominant pole of a common-source amplifier can be estimated via rigorous small-signal analysis, Miller's Theorem, or ZVTC analysis, though only the full small-signal transfer function can provide accurate assessments of non-dominant poles
- When designing MOS analog circuits, we will use the dominant-pole approximation to provide an estimate of the gain-bandwidth product, and only include the effects of other "non-dominant" poles when analyzing stability