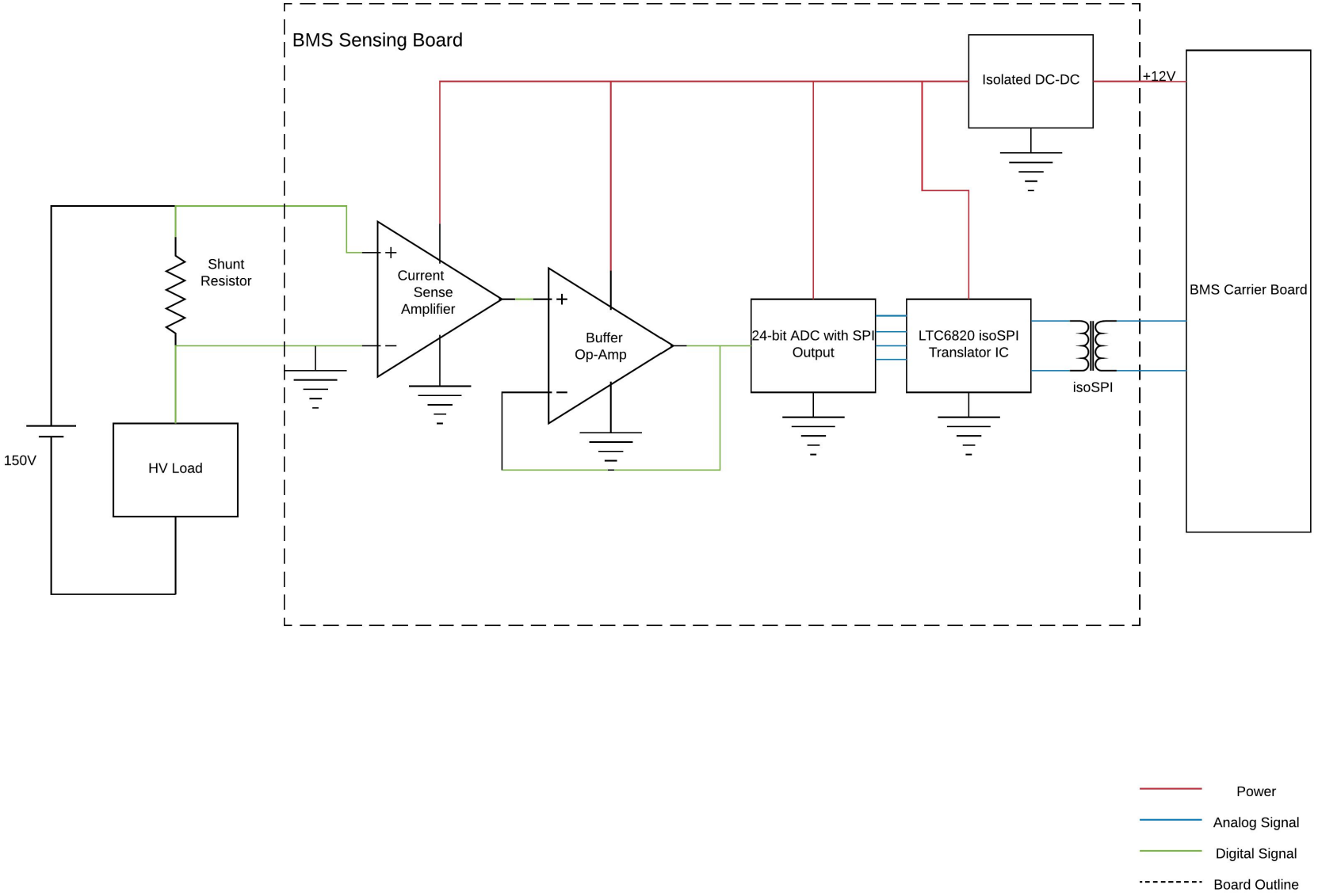
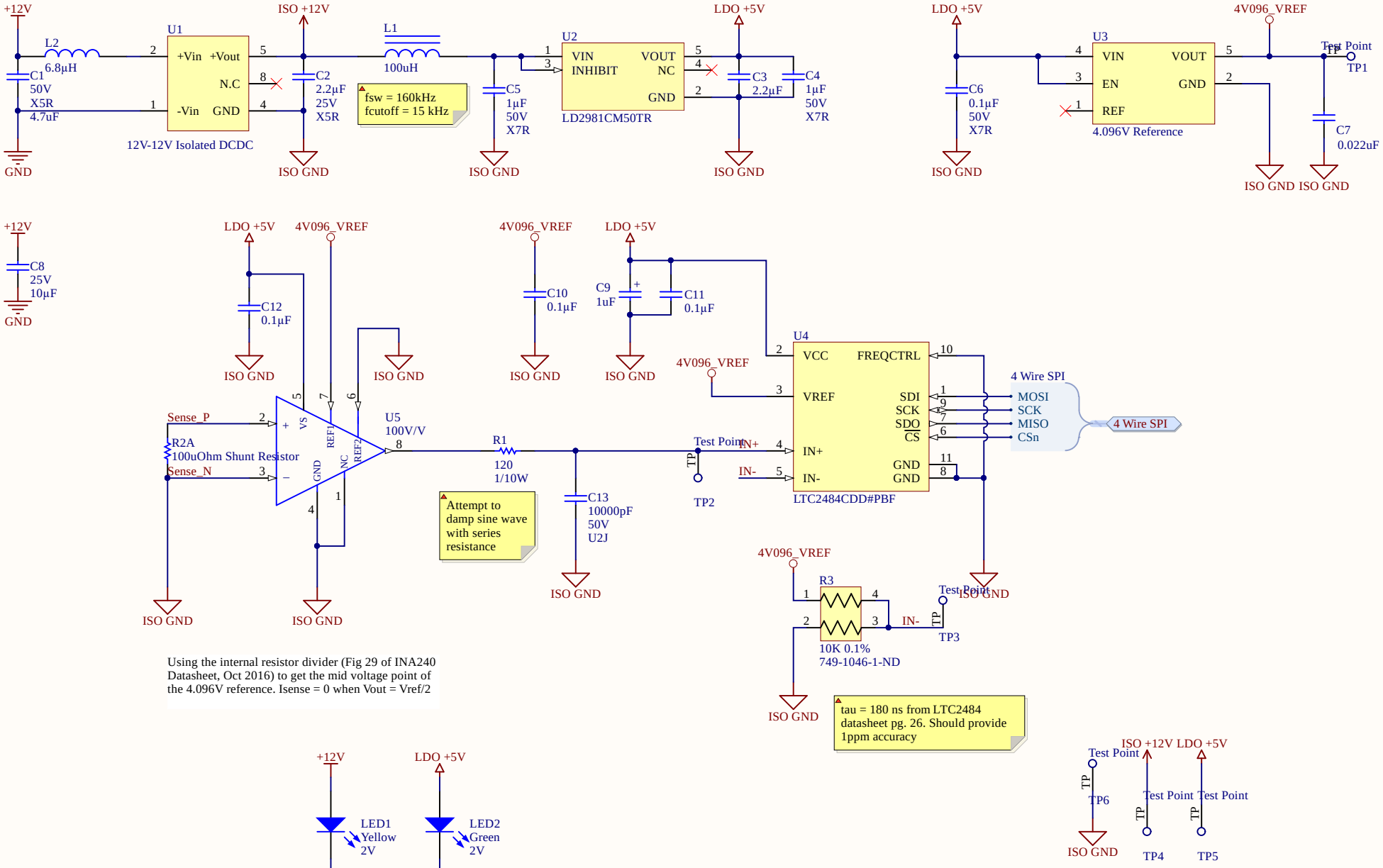


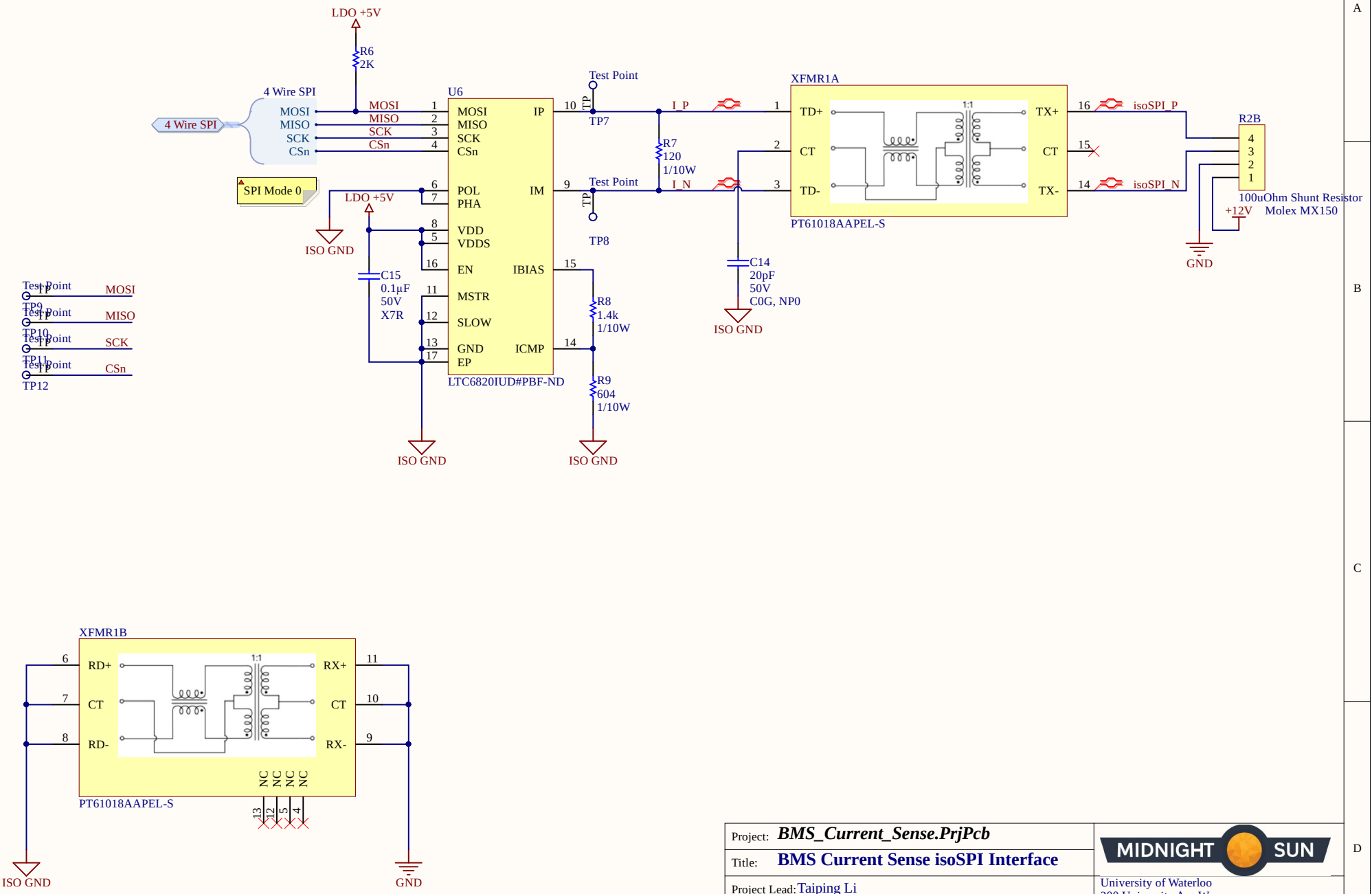
Last Updated: Oct 29, 2017

Project: ***BMS_Current_Sense.PrjPcb***		MIDNIGHT SUN
Title: **BMS Current Sense Block Diagram**		
Project Lead: Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 2.2	
Date: 2018-02-23	Sheet 1 of 3	Website: www.uwmidsun.com



Project: *BMS_Current_Sense.PrjPcb*	
Title: **BMS Current Sense Board**	
Project Lead: Taiping Li	
Size: Letter	Revision: 2.2
Date: 2018-02-23	Sheet 2 of 3

MIDNIGHT SUN
University of Waterloo
200 University Ave W
Waterloo, ON, Canada
N2L 3E9
Website: www.uwmidsun.com

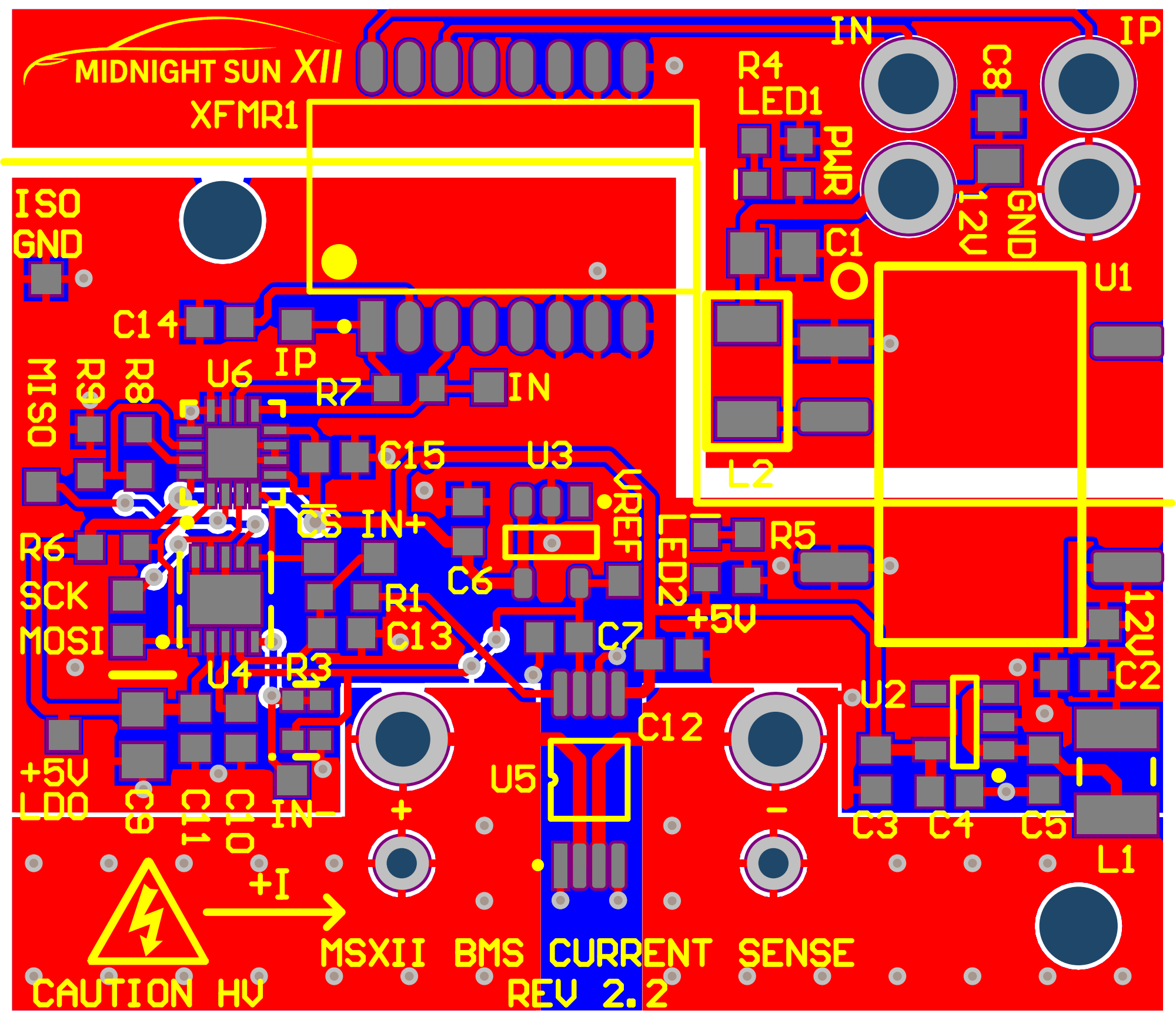


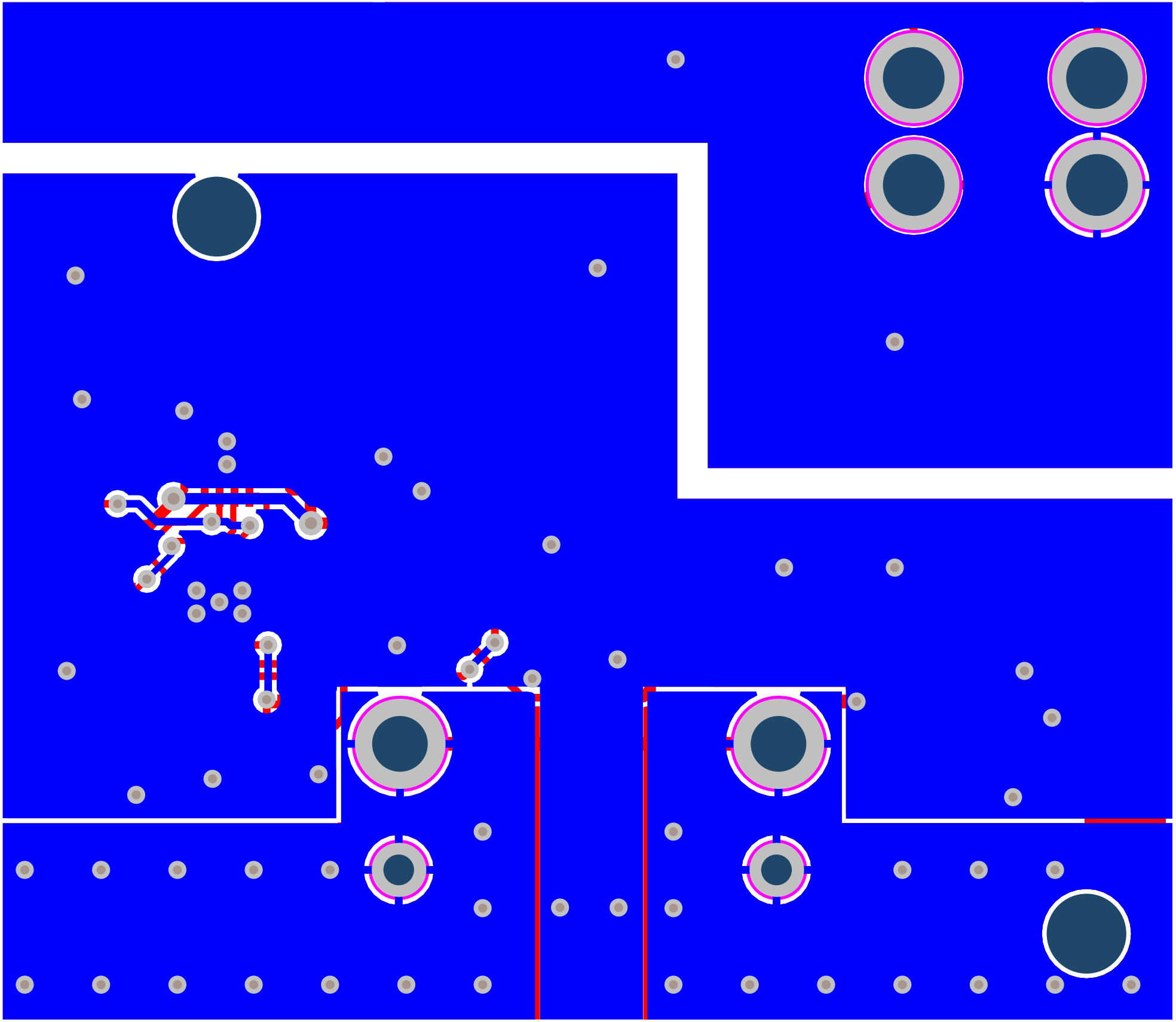
Project: *BMS_Current_Sense.PrjPcb*		MIDNIGHT SUN
Title: **BMS Current Sense isoSPI Interface**		
Project Lead: Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 2.2	
Date: 2018-02-23	Sheet 3 of 3	Website: www.uwmidsun.com

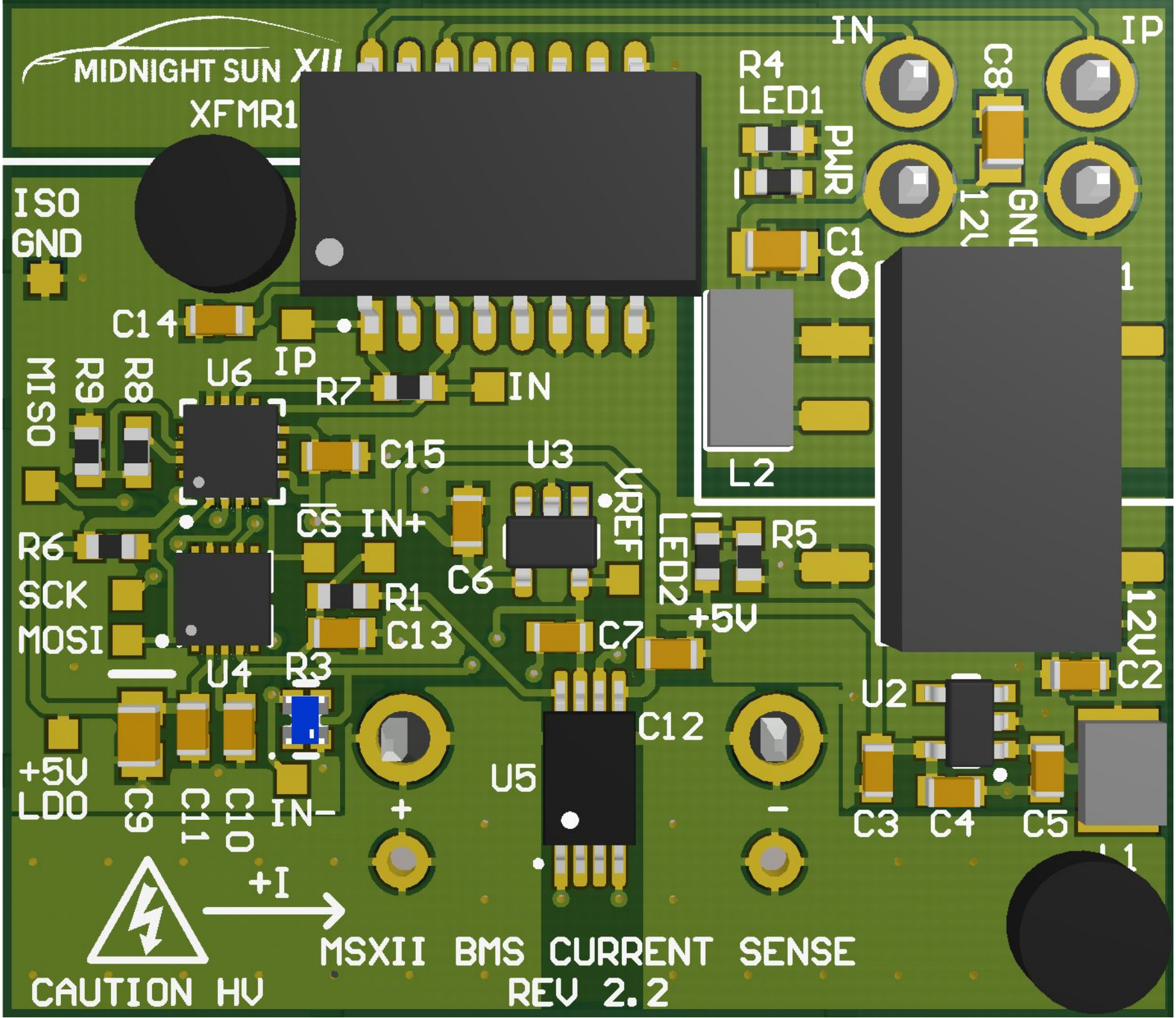
Bill of Materials

Project:	BMS_Current_Sense.PrjPcb
Revision:	2.2
Project Lead:	Taiping Li
Generated On:	2018-02-23 9:40:54 PM
Production Quantity:	1
Currency	CAD
Total Parts Count:	35

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Supplier Order Qty 1	Supplier Subtotal 1
CAP CER 4.7UF 50V 10% X5R 0805	C1	Murata Electronics North America	GRT21BR61H475ME13L	Digi-Key	490-12395-1-ND	0.56	1	$ 0.56
CAP CER 2.2UF 25V 10% X5R 0603	C2, C3	Murata Electronics North America	GRM188R61E225KA12D	Digi-Key	490-10731-1-ND	0.21	2	$ 0.42
CAP CER 1UF 50V 10% X7R 0603	C4, C5	Taiyo Yuden	UMK107AB7105KA-T	Digi-Key	587-3247-1-ND	0.36	2	$ 0.72
CAP CER 0.1UF 50V 10% X7R 0603	C6, C10, C11, C12, C15	AVX Corporation	06035C104KAT2A	Digi-Key	478-5052-1-ND	0.13	5	$ 0.65
CAP CER 0.022UF 50V 10% X7R 0603	C7	Murata Electronics North America	GRM188R71H223KA01D	Digi-Key	490-1517-1-ND	0.16	1	$ 0.16
CAP CER 10uF 25V 10% X5R 0805	C8	Murata Electronics North America	GRM21BR61E106KA73L	Digi-Key	490-5523-1-ND	0.29	1	$ 0.29
CAP TANT 1UF 25V 10% 0805	C9	AVX Corporation	TAJR105K025RNJ	Digi-Key	478-8928-1-ND	0.95	1	$ 0.95
CAP CER 10nF 50V 5% X7R 0603	C13	KEMET	C0603C103J5JAC7867	Digi-Key	399-13384-1-ND	0.35	1	$ 0.35
CAP CER 20PF 50V ±5% C0G/NP0 0603	C14	Murata Electronics North America	GRM1885C1H200JA01D	Digi-Key	490-1410-1-ND	0.15	1	$ 0.15
IND 100uH 60mA 5% 1210	L1	EPCOS (TDK)	B82422T1104J000	Digi-Key	495-5646-1-ND	0.65	1	$ 0.65
IND 6.8uH 260mA 20% 1210	L2	TDK Corporation	NLFV32T-6R8M-EF	Digi-Key	445-15776-1-ND	0.59	1	$ 0.59
LED YELLOW CLEAR 2.1V 0603	LED1	Wurth Electronics Inc.	150060YS75000	Digi-Key	732-4981-1-ND	0.19	1	$ 0.19
LED GREEN CLEAR 2V 0603	LED2	Wurth Electronics Inc.	150060VS75000	Digi-Key	732-4980-1-ND	0.19	1	$ 0.19
RES 120 OHM 1% 1/10W 0603	R1, R7	Yageo	RC0603FR-07120RL	Digi-Key	311-120HRCT-ND	0.14	2	$ 0.28
RES SHUNT 100UOHM 5% 36W 60MM	R2	Vishay Dale	WSBM8518L1000JK	Digi-Key	541-1906-ND	19.08	1	$ 19.08
RES ARRAY 10K OHM 0.1% 2RES 0606	R3	Vishay Beyschlag	ACASN1002S1002P1AT	Digi-Key	749-1046-1-ND	0.84	1	$ 0.84
RES 4.7K OHM 1% 1/10W 0603	R4	Yageo	RC0603FR-074K7L	Digi-Key	311-4.70KHRCT-ND	0.14	1	$ 0.14
RES 2K OHM 1% 1/10W 0603	R5, R6	Yageo	RC0603FR-072KL	Digi-Key	311-2.00KHRCT-ND	0.14	2	$ 0.28
RES 1.4k OHM 1% 1/10W 0603	R8	Yageo	RC0603FR-071K4L	Digi-Key	311-1.40KHRCT-ND	0.14	1	$ 0.14
RES 604 OHM 1% 1/10W 0603	R9	Yageo	RC0603FR-07604RL	Digi-Key	311-604HRCT-ND	0.14	1	$ 0.14
IC DCDC ISOLATED 12V 1W 8-SMD 5-LEAD	U1	XP Power	ISE1212A	Digi-Key	1470-2950-1-ND	6.68	1	$ 6.68
IC REG LDO 5V 0.1A SOT23-5	U2	STMicroelectronics	LD2981CM50TR	Digi-Key	497-7787-1-ND	0.84	1	$ 0.84
IC VREF SERIES 4.096V 5MA SOT23-5	U3	Texas Instruments	LM4120AIM5-4.1/NOPB	Digi-Key	LM4120AIM5-4.1/NOPBCT-ND	3.11	1	$ 3.11
IC ADC 24BIT 10-DFN	U4	Linear Technology	LTC2484CDD#PBF	Digi-Key	LTC2484CDD#PBF-ND	7.13	1	$ 7.13
IC CURRENT AMPLIFIER INA240 8-TSSOP	U5	Texas Instruments	INA240A3PWR	Digi-Key	296-45090-1-ND	3.76	1	$ 3.76
IC ISOSPI COMM INTERFACE LTC6820IUD	U6	Linear Technology/Analog Devices	LTC6820IUD#PBF	Digi-Key	LTC6820IUD#PBF-ND	7.1	1	$ 7.10
IC PULSE XFMR 1CT:1CT 350UH SMD	XFMR1	Bourns Inc.	PT61018AAPEL-S	Digi-Key	PT61018AAPEL-SCT-ND	2.47	1	$ 2.47
							Total:	$ 57.86


MIDNIGHT SUN XII
XFMR1
IN
IP
R4
LED1
PWR
C8
12V
GND
ISO
GND
C1
U1
C14
IP
U6
R7
IN
MISO
R8
R9
C15
U3
L2
VREF
IN+
C6
R5
R6
SCK
MOSI
R1
C13
C7
LED2
+5V
12V
U4
R3
C12
U2
C2
+5V
LDO
C9
C11
C10
IN-
U5
+
-
C3
C4
C5
L1
+I
MSXII BMS CURRENT SENSE
REV 2.2
CAUTION HV




MIDNIGHT SUN XII
XFMR1
ISO GND
IN
IP
R4
LED1
PWR
C8
12V
GND
C1
L2
L1
C14
IP
R7
IN
MISO
R9
R8
U6
C15
U3
VREF
CS
IN+
R6
SCK
MOSI
C6
R1
C13
LED2
+5V
R5
C7
U4
R3
C2
U2
C12
U5
+5V LDO
C9
C11
C10
IN−
+
−
C3
C4
C5
+I
CAUTION HV
MSXII BMS CURRENT SENSE
REV 2.2

Electrical Rules Check Report

Class	Document	Message
Warning	BMS_Current_Sense.SchDoc	Net IN+_2 has no driving source (Pin C13-1,Pin R1-2,Pin TP2-TP,Pin U4-4)
Warning	BMS_Current_Sense.SchDoc	Net IN-_2 has no driving source (Pin R3-3,Pin R3-4,Pin TP3-TP,Pin U4-5)
Warning	BMS_Current_Sense.SchDoc	Net Sense_2_P has no driving source (Pin R2-5,Pin U5-2)
Warning	BMS_Current_Sense.SchDoc	Nets Wire Sense_N has multiple names (Net Label Sense_N,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND,Power Object ISO GND)
Warning	Block Diagram.SchDoc	Nets Wire Sense_N has multiple names (Net Label Sense_N,Power Object ISO GND)

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_BMS_Current_Sens
e\BMS_Current_Sense.PcbDoc

Warnings 0
Rule Violations 142

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=10mil) (InComponent('R1')),(All)	0
Clearance Constraint (Gap=6mil) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=6mil) (Max=50mil) (Preferred=10mil) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air Gap=10mil) (Entries=4)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	2
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=10mil) (All),(All)	57
Silk To Solder Mask (Clearance=10mil) (IsPad),(All)	71
Silk to Silk (Clearance=10mil) (All),(All)	12
Net Antennae (Tolerance=0mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Total	142

Hole Size Constraint (Min=1mil) (Max=100mil) (All)
Hole Size Constraint: (104.331mil > 100mil) Pad R2-0(3401.457mil,3103.662mil) on Multi-Layer Actual Hole Size = 104.331mil
Hole Size Constraint: (104.331mil > 100mil) Pad R2-0(4541.221mil,2166.654mil) on Multi-Layer Actual Hole Size = 104.331mil

Minimum Solder Mask Sliver (Gap=10mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad R3-1(3495mil,2413mil) on Top Layer And Pad R3-2(3532.008mil,2413mil) on Top
Minimum Solder Mask Sliver Constraint: (1.449mil < 10mil) Between Pad R3-4(3495mil,2466.15mil) on Top Layer And Pad R3-3(3532.008mil,2466.15mil)
Minimum Solder Mask Sliver Constraint: (5.583mil < 10mil) Between Pad C13-2(3586.575mil,2555mil) on Top Layer And Pad R1-1(3592.449mil,2604mil)
Minimum Solder Mask Sliver Constraint: (6.583mil < 10mil) Between Pad IN+-TP(3610mil,2655mil) on Top Layer And Pad R1-1(3592.449mil,2604mil) on
Minimum Solder Mask Sliver Constraint: (5.583mil < 10mil) Between Pad C13-1(3533.425mil,2555mil) on Top Layer And Pad R1-2(3531.425mil,2604mil)
Minimum Solder Mask Sliver Constraint: (6.583mil < 10mil) Between Pad CS-TP(3530mil,2655mil) on Top Layer And Pad R1-2(3531.425mil,2604mil) on
Minimum Solder Mask Sliver Constraint: (8.567mil < 10mil) Between Pad U5-5(3928.032mil,2475mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U2-2(4435mil,2437.402mil) on Top Layer And Pad U2-3(4435mil,2474.803mil) on
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U2-1(4435mil,2400mil) on Top Layer And Pad U2-2(4435mil,2437.402mil) on Top
Minimum Solder Mask Sliver Constraint: (5.78mil < 10mil) Between Pad U3-2(3839mil,2730.134mil) on Top Layer And Pad U3-1(3876.402mil,2730.134mil)
Minimum Solder Mask Sliver Constraint: (5.779mil < 10mil) Between Pad U3-3(3801.599mil,2730.134mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U6-2(3405.157mil,2738.898mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-1(3385.472mil,2738.898mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U6-3(3424.843mil,2738.898mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-2(3405.157mil,2738.898mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U6-4(3444.528mil,2738.898mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-3(3424.843mil,2738.898mil)
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-4(3444.528mil,2738.898mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U6-6(3471.102mil,2785.157mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-5(3471.102mil,2765.472mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U6-7(3471.102mil,2804.843mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-6(3471.102mil,2785.157mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U6-8(3471.102mil,2824.528mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-7(3471.102mil,2804.843mil)
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-8(3471.102mil,2824.528mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U6-10(3424.843mil,2851.102mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-9(3444.528mil,2851.102mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U6-11(3405.157mil,2851.102mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-10(3424.843mil,2851.102mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U6-12(3385.472mil,2851.102mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-11(3405.157mil,2851.102mil)
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-12(3385.472mil,2851.102mil)
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-13(3358.898mil,2824.528mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U6-14(3358.898mil,2804.843mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U6-15(3358.898mil,2785.157mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-14(3358.898mil,2804.843mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U6-16(3358.898mil,2765.472mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-15(3358.898mil,2785.157mil)
Minimum Solder Mask Sliver Constraint: (0.858mil < 10mil) Between Pad U6-17(3415mil,2795mil) on Top Layer And Pad U6-16(3358.898mil,2765.472mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-2(3385.315mil,2543.898mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-11(3405mil,2600mil) on Top Layer And Pad U4-1(3365.63mil,2543.898mil) on
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-3(3405mil,2543.898mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-11(3405mil,2600mil) on Top Layer And Pad U4-2(3385.315mil,2543.898mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-4(3424.685mil,2543.898mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-11(3405mil,2600mil) on Top Layer And Pad U4-3(3405mil,2543.898mil) on
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-11(3405mil,2600mil) on Top Layer And Pad U4-4(3424.685mil,2543.898mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-5(3444.37mil,2543.898mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-11(3405mil,2600mil) on Top Layer And Pad U4-5(3444.37mil,2543.898mil) on
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-7(3424.685mil,2656.102mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-11(3405mil,2600mil) on Top Layer And Pad U4-6(3444.37mil,2656.102mil) on
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-8(3405mil,2656.102mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-11(3405mil,2600mil) on Top Layer And Pad U4-7(3424.685mil,2656.102mil)

Minimum Solder Mask Sliver (Gap=10mil) (All),(All)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-9(3385.315mil,2656.102mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-11(3405mil,2600mil) on Top Layer And Pad U4-8(3405mil,2656.102mil) on
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-11(3405mil,2600mil) on Top Layer And Pad U4-9(3385.315mil,2656.102mil)
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-10(3365.63mil,2656.102mil) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (1.843mil < 10mil) Between Pad U4-11(3405mil,2600mil) on Top Layer And Pad U4-10(3365.63mil,2656.102mil)

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (8.143mil < 10mil) Between Arc (3467.441mil,2391.347mil) on Top Overlay And Pad IN--TP(3494mil,2360mil) on
Silk To Solder Mask Clearance Constraint: (5.191mil < 10mil) Between Text "C4" (4346mil,2285.685mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (9.725mil < 10mil) Between Track (4405.472mil,2378.347mil)(4405.472mil,2496.457mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (9.725mil < 10mil) Between Track (4373.976mil,2378.347mil)(4405.472mil,2378.347mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (5.191mil < 10mil) Between Text "C4" (4346mil,2285.685mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (8.756mil < 10mil) Between Text "U4" (3385mil,2485mil) on Top Overlay And Pad C10-1(3426mil,2455.575mil)
Silk To Solder Mask Clearance Constraint: (4.055mil < 10mil) Between Track (3498.937mil,2391.347mil)(3526.496mil,2391.347mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (4.055mil < 10mil) Between Track (3498.937mil,2391.347mil)(3526.496mil,2391.347mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (4.055mil < 10mil) Between Track (3498.937mil,2487.803mil)(3526.496mil,2487.803mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (4.055mil < 10mil) Between Track (3498.937mil,2487.803mil)(3526.496mil,2487.803mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (9.913mil < 10mil) Between Text "R1" (3622.047mil,2586.614mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (9.585mil < 10mil) Between Text "C5" (4469mil,2285.685mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (9.585mil < 10mil) Between Text "C3" (4244.095mil,2285.685mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (7.756mil < 10mil) Between Text "C7" (3905mil,2536mil) on Top Overlay And Pad C7-1(3876.575mil,2550mil) on
Silk To Solder Mask Clearance Constraint: (3.616mil < 10mil) Between Text "C7" (3905mil,2536mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (5.876mil < 10mil) Between Text "R3" (3490mil,2495mil) on Top Overlay And Pad C13-1(3533.425mil,2555mil)
Silk To Solder Mask Clearance Constraint: (9.961mil < 10mil) Between Text "12V" (4385mil,3140mil) on Top Overlay And Pad C8-1(4435mil,3175.551mil)
Silk To Solder Mask Clearance Constraint: (9.961mil < 10mil) Between Text "GND" (4450mil,3140mil) on Top Overlay And Pad C8-1(4435mil,3175.551mil)
Silk To Solder Mask Clearance Constraint: (8.961mil < 10mil) Between Track (4045.669mil,2801.811mil)(4045.669mil,3004.567mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.567mil < 10mil) Between Track (4045.669mil,2801.811mil)(4154.331mil,2801.811mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.961mil < 10mil) Between Track (4154.331mil,2801.811mil)(4154.331mil,3004.567mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.961mil < 10mil) Between Track (4045.669mil,2801.811mil)(4045.669mil,3004.567mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.961mil < 10mil) Between Track (4045.669mil,3004.567mil)(4154.331mil,3004.567mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.961mil < 10mil) Between Track (4154.331mil,2801.811mil)(4154.331mil,3004.567mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (6.496mil < 10mil) Between Track (4084.803mil,3133.496mil)(4084.803mil,3169.339mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (9.845mil < 10mil) Between Text "LED2" (3985mil,2710mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (6.496mil < 10mil) Between Track (4026.528mil,2711.197mil)(4062.37mil,2711.197mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (9.845mil < 10mil) Between Text "LED2" (3985mil,2710mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (9.546mil < 10mil) Between Track (4545.669mil,2542.913mil)(4545.669mil,3042.913mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (9.546mil < 10mil) Between Track (4545.669mil,2542.913mil)(4545.669mil,3042.913mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (7.976mil < 10mil) Between Track (4275.197mil,2542.913mil)(4275.197mil,3042.913mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (7.972mil < 10mil) Between Track (4275.197mil,2542.913mil)(4275.197mil,3042.913mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (7.972mil < 10mil) Between Track (4275.197mil,2542.913mil)(4275.197mil,3042.913mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (4.444mil < 10mil) Between Text "R5" (4135mil,2670mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (4.921mil < 10mil) Between Track (4373.976mil,2378.347mil)(4373.976mil,2496.457mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (9.305mil < 10mil) Between Track (4373.976mil,2378.347mil)(4405.472mil,2378.347mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (4.921mil < 10mil) Between Track (4373.976mil,2378.347mil)(4373.976mil,2496.457mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (9.305mil < 10mil) Between Track (4373.976mil,2496.457mil)(4405.472mil,2496.457mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (4.921mil < 10mil) Between Track (4405.472mil,2378.347mil)(4405.472mil,2496.457mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (9.305mil < 10mil) Between Track (4373.976mil,2496.457mil)(4405.472mil,2496.457mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (4.921mil < 10mil) Between Track (4405.472mil,2378.347mil)(4405.472mil,2496.457mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (4.921mil < 10mil) Between Track (4405.472mil,2378.347mil)(4405.472mil,2496.457mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (9.305mil < 10mil) Between Track (4373.976mil,2378.347mil)(4405.472mil,2378.347mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.852mil < 10mil) Between Track (3517.126mil,3260.984mil)(4032.874mil,3260.984mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.852mil < 10mil) Between Track (3517.126mil,3260.984mil)(4032.874mil,3260.984mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.852mil < 10mil) Between Track (3517.126mil,3260.984mil)(4032.874mil,3260.984mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.852mil < 10mil) Between Track (3517.126mil,3260.984mil)(4032.874mil,3260.984mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.852mil < 10mil) Between Track (3517.126mil,3260.984mil)(4032.874mil,3260.984mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.852mil < 10mil) Between Track (3517.126mil,3260.984mil)(4032.874mil,3260.984mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.852mil < 10mil) Between Track (3517.126mil,3260.984mil)(4032.874mil,3260.984mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.852mil < 10mil) Between Track (3517.126mil,3260.984mil)(4032.874mil,3260.984mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.851mil < 10mil) Between Track (3517.126mil,3009.016mil)(4032.874mil,3009.016mil) on Top Overlay And

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (8.851mil < 10mil) Between Track (3517.126mil,3009.016mil)(4032.874mil,3009.016mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.851mil < 10mil) Between Track (3517.126mil,3009.016mil)(4032.874mil,3009.016mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.851mil < 10mil) Between Track (3517.126mil,3009.016mil)(4032.874mil,3009.016mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.851mil < 10mil) Between Track (3517.126mil,3009.016mil)(4032.874mil,3009.016mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.851mil < 10mil) Between Track (3517.126mil,3009.016mil)(4032.874mil,3009.016mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.851mil < 10mil) Between Track (3517.126mil,3009.016mil)(4032.874mil,3009.016mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.858mil < 10mil) Between Track (3517.126mil,3009.016mil)(4032.874mil,3009.016mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (6.662mil < 10mil) Between Track (3498.937mil,2391.347mil)(3526.496mil,2391.347mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (5.876mil < 10mil) Between Text "IN-" (3470mil,2300mil) on Top Overlay And Pad IN--TP(3494mil,2360mil) on
Silk To Solder Mask Clearance Constraint: (7.077mil < 10mil) Between Text "VREF" (3925mil,2770mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (7.362mil < 10mil) Between Text "IN+" (3590mil,2685mil) on Top Overlay And Pad IN+-TP(3610mil,2655mil) on
Silk To Solder Mask Clearance Constraint: (3.449mil < 10mil) Between Track (4545.669mil,2542.913mil)(4545.669mil,3042.913mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.858mil < 10mil) Between Text "12V" (4600mil,2620mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (4.394mil < 10mil) Between Track (4275.197mil,2542.913mil)(4545.669mil,2542.913mil) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (8.071mil < 10mil) Between Text "ISO

GND" (3120mil,3050mil) on Top Overlay And Pad ISO GND-TP(3166.339mil,3025.591mil) on Top Layer [Top Overlay] to [

Silk To Solder Mask (Clearance=10mil) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (7.362mil < 10mil) Between Text "IN" (3785.905mil,2866.89mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (7.402mil < 10mil) Between Text "CS" (3503.937mil,2685.039mil) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (8.314mil < 10mil) Between Text "12V" (4385mil,3140mil) on Top Overlay And Pad R2-1(4314.842mil,3145mil)
Silk To Solder Mask Clearance Constraint: (9.234mil < 10mil) Between Text "IP" (4600mil,3340mil) on Top Overlay And Pad R2-4(4555mil,3284.764mil) on

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (8.055mil < 10mil) Between Text "C1" (4208.661mil,3059.055mil) on Top Overlay And Arc (4235.827mil,3023.228mil) on
Silk To Silk Clearance Constraint: (4.504mil < 10mil) Between Text "VREF" (3925mil,2770mil) on Top Overlay And Arc (3909.866mil,2730.134mil) on Top
Silk To Silk Clearance Constraint: (2.431mil < 10mil) Between Text "CS" (3503.937mil,2685.039mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (Collision < 10mil) Between Text "R3" (3490mil,2495mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.404mil < 10mil) Between Text "L2" (4078.74mil,2751.968mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (4.207mil < 10mil) Between Text "LED2" (3985mil,2710mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.419mil < 10mil) Between Text "12V" (4385mil,3140mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (4.171mil < 10mil) Between Text "GND" (4450mil,3140mil) on Top Overlay And Track
Silk To Silk Clearance Constraint: (9.91mil < 10mil) Between Text "MSXII BMS CURRENT SENSE

REV 2.2" (3110.236mil,2055.118mil) on Top Overlay And Track (3540mil,2165mil)(3560mil,2185mil) on Top Overlay Silk T

Silk to Silk (Clearance=10mil) (All),(All)
Silk To Silk Clearance Constraint: (7.308mil < 10mil) Between Text "C2" (4594.488mil,2484.252mil) on Top Overlay And Text "12V" (4600mil,2620mil) on
Silk To Silk Clearance Constraint: (9.609mil < 10mil) Between Text "R4" (4092mil,3294mil) on Top Overlay And Text "LED1" (4092mil,3247mil) on Top
Silk To Silk Clearance Constraint: (7.609mil < 10mil) Between Text "+5V" (3135mil,2355mil) on Top Overlay And Text "LDO" (3135mil,2310mil) on Top