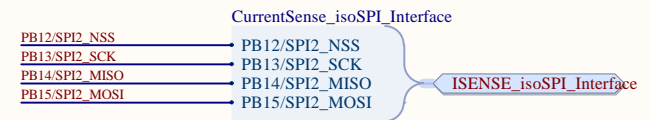
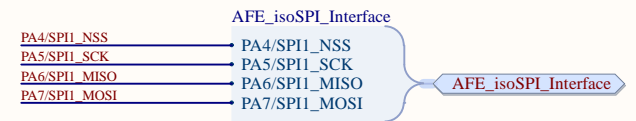
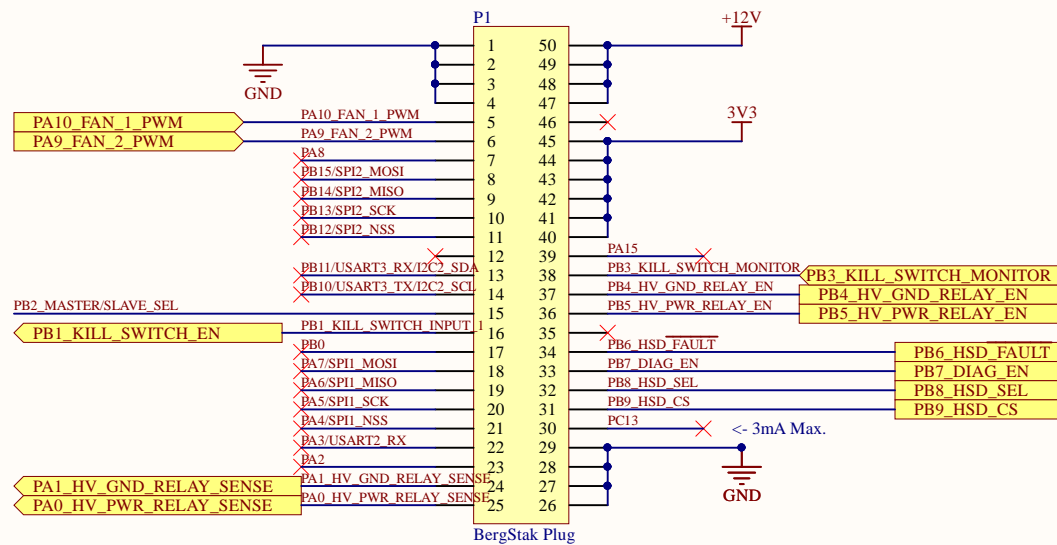


### Controller Board




Project: <b>BMS_Carrier_Board.PrfPcb</b>		<div>MIDNIGHTSUN</div>
Title: <b>Controller Board Interface</b>		
Project Lead: Aashmika Mali & Liam Hawkins		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 5.0	
Date: 2019-06-12	Sheet 1 of 4	
		Website: <a href="http://www.uwmidsun.com">www.uwmidsun.com</a>

Table 4. SPI Modes

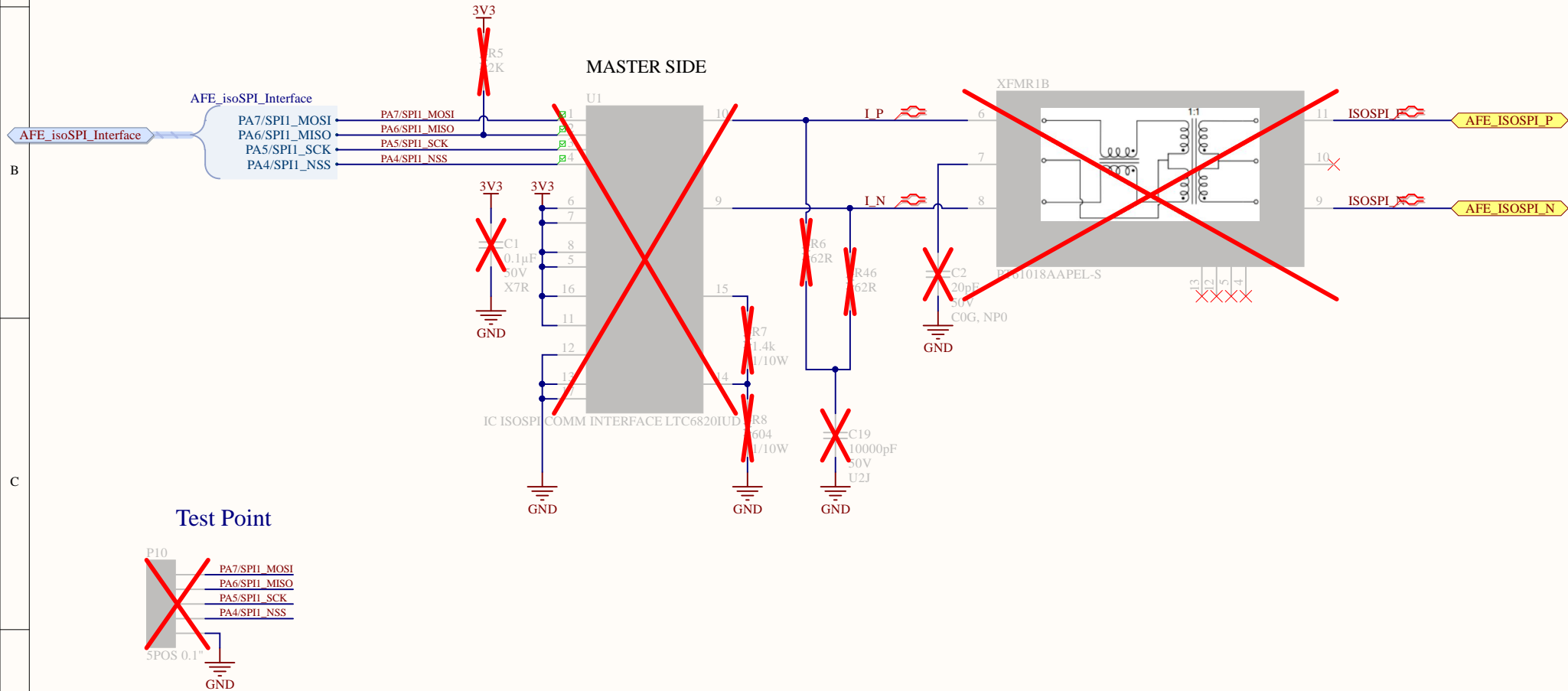
MODE	POL	PHA	DESCRIPTION
0	0	0	SCK Idles Low, Latches on Rising (1st) Edge
1	0	1	SCK Idles Low, Latches on Falling (2nd) Edge
2	1	0	SCK Idles High, Latches on Falling (1st) Edge
3	1	1	SCK Idles High, Latches on Rising (2nd) Edge

SCK idles high, latches on 2nd rising edge

Pulse Drive Current  $I_{IP} = 20 \times I_{BIAS} = 20\text{mA}$

Transmitted Differential Signal Amplitude  $V_A = I_{IP} \times 120 / 2 = 1.2\text{V}$

Bias Current  $I_{BIAS}$  can be adjusted from 0.1mA to 1mA  
Currently set to 1mA



Project: **BMS\_Carrier\_Board.PrjPcb**

Title: **BMS Interface**

Project Lead: Aashmika Mali & Liam Hawkins

Size: Letter

Date: 2019-06-12

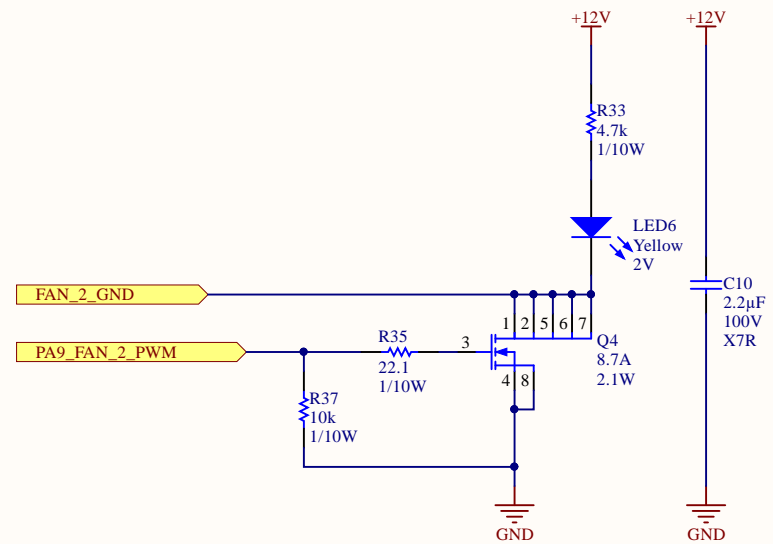
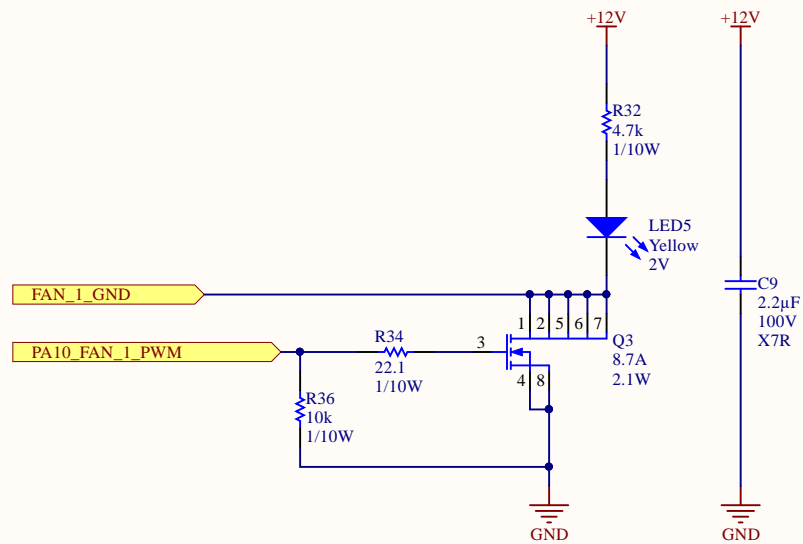
Revision: 5.0


Sheet3 of 4



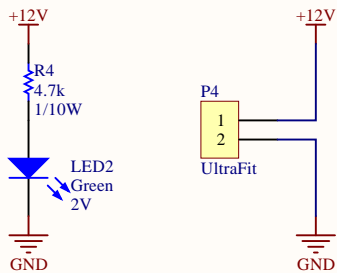
University of Waterloo  
200 University Ave W  
Waterloo, ON, Canada  
N2L 3E9

Website: [www.uwmidsun.com](http://www.uwmidsun.com)

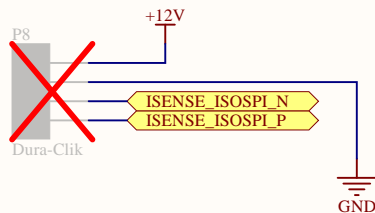


Project: <b>BMS_Carrier_Board.PrjPcb</b>		
Title: <b>BMS Fan and Relay Control</b>		
Project Lead: Aashmika Mali & Liam Hawkins		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 5.0	
Date: 2019-06-12	Sheet4 of 4	
		Website: <a href="http://www.uwmidSun.com">www.uwmidSun.com</a>

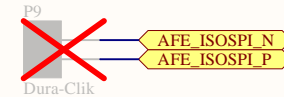
## 12V Power



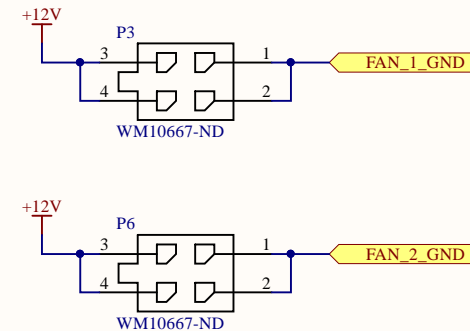
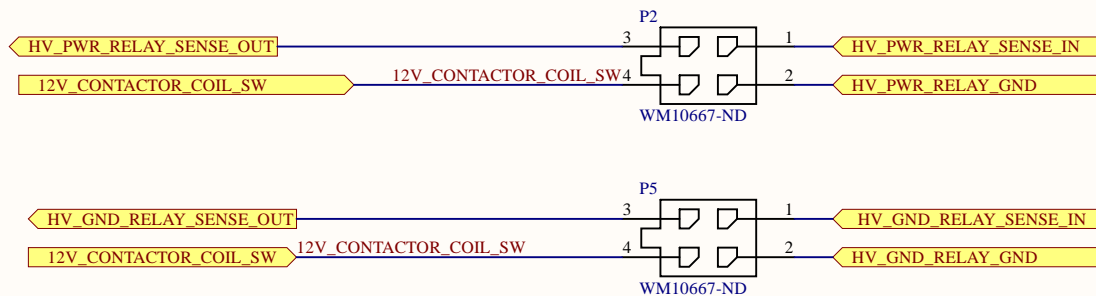
## BMS Current Sense



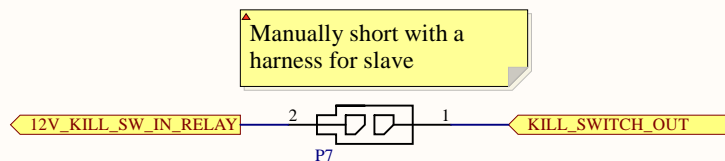
## AFE isoSPI




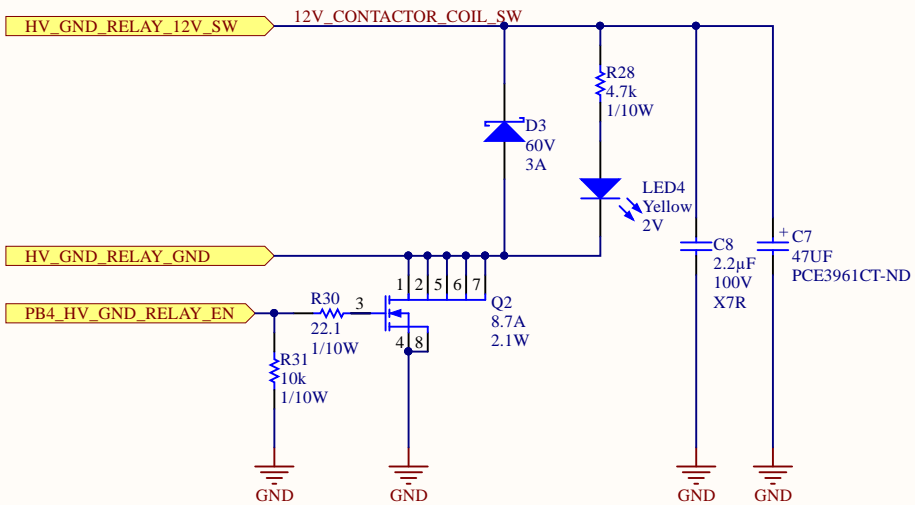
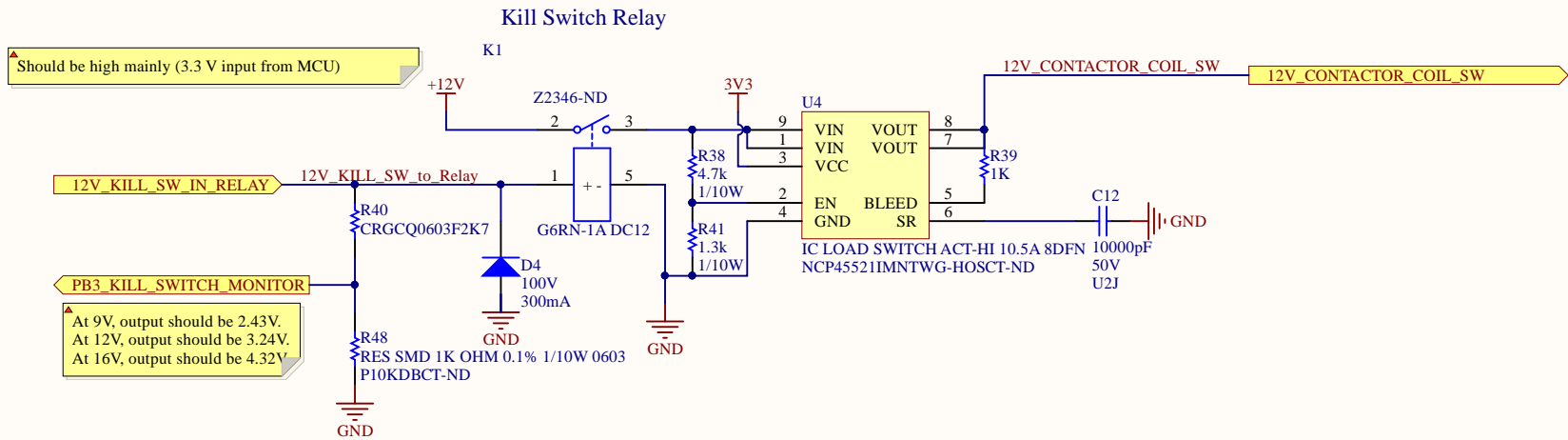
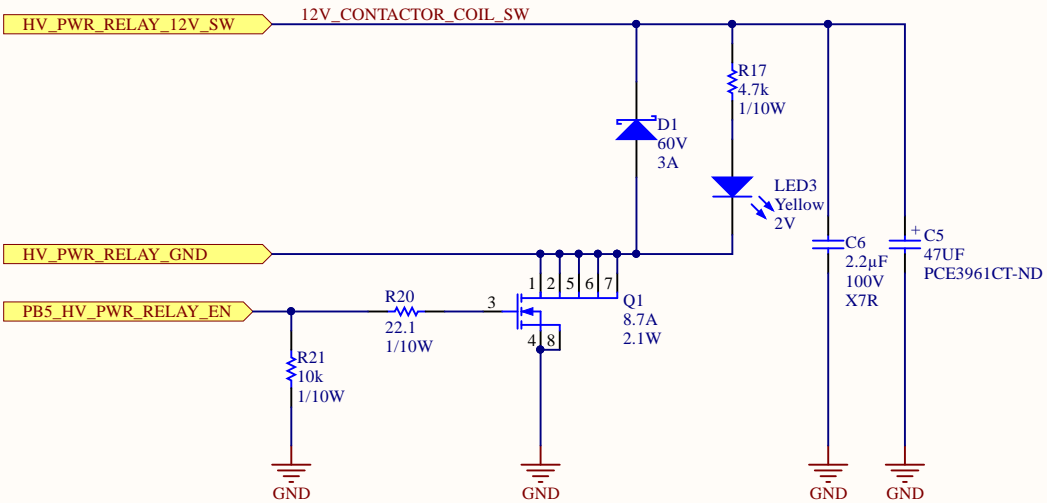
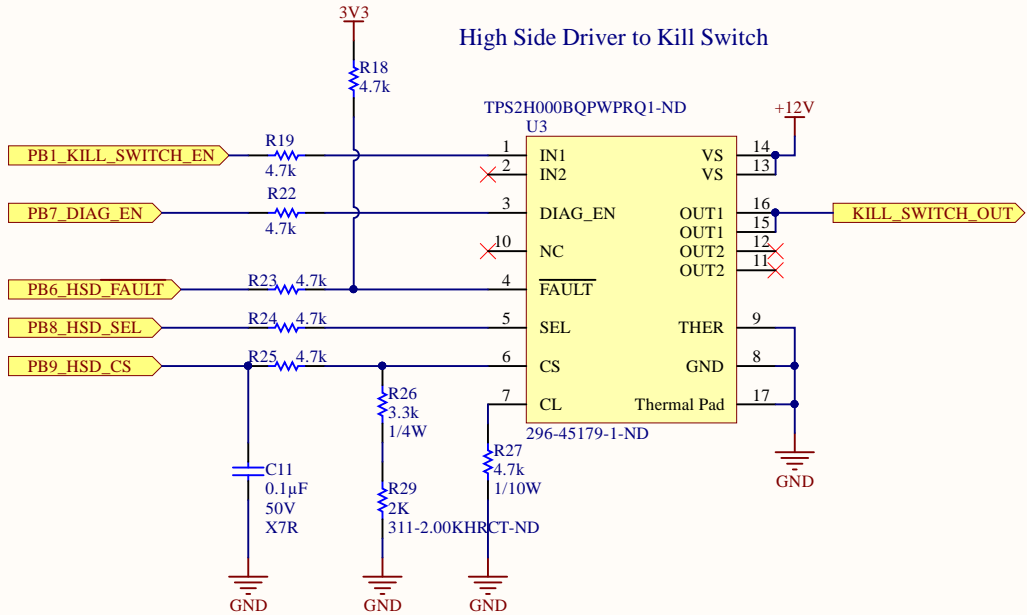
## Fan & Relays




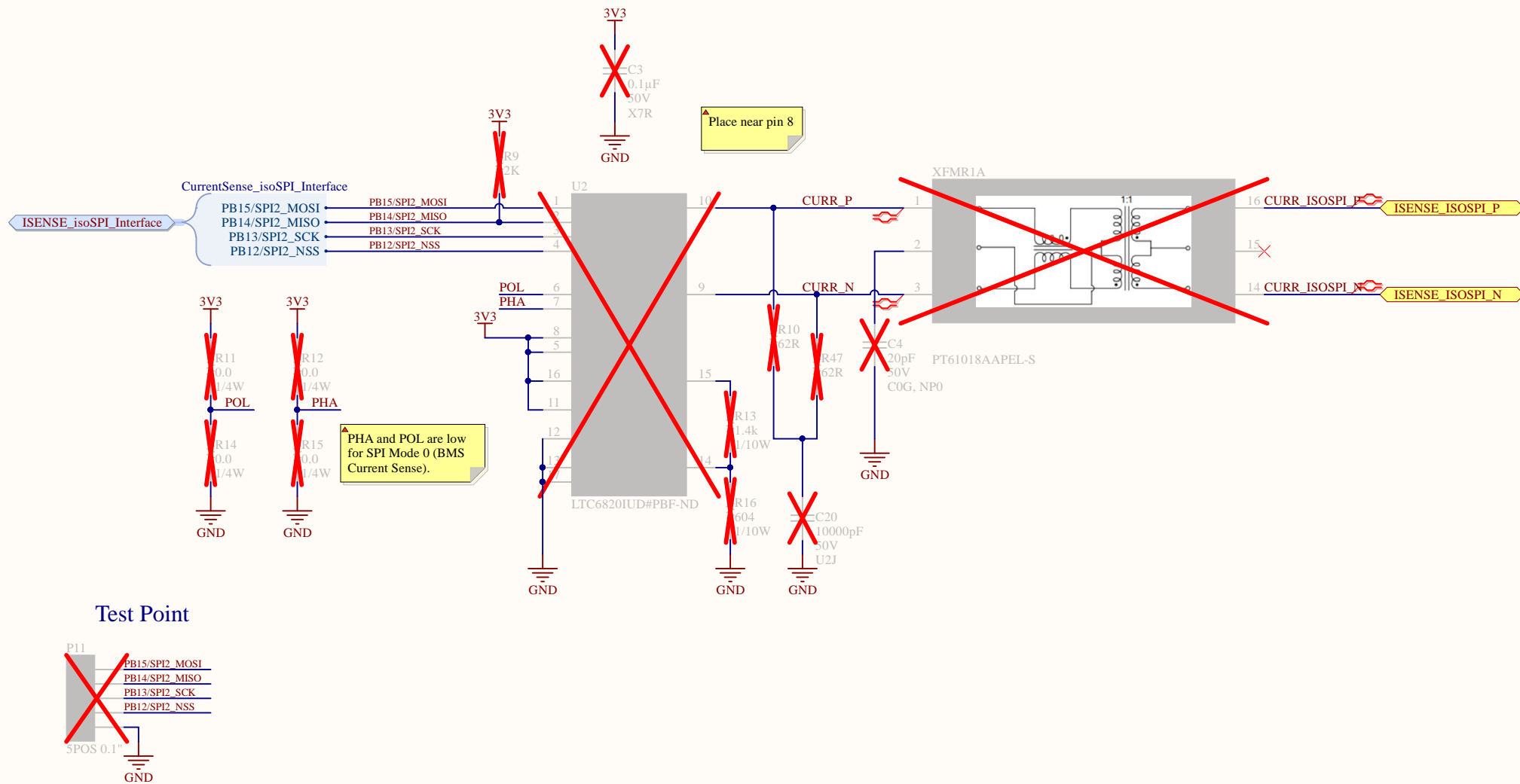
## Kill Switch



Project: <b>BMS_Carrier_Board.PrfPcb</b>		<div><div>MIDNIGHT</div><div></div><div>SUN</div></div>
Title: <b>BMS Fan and Relay Control</b>		
Project Lead: Aashmika Mali & Liam Hawkins		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 5.0	
Date: 2019-06-12	Sheet4 of 4	Website: <a href="http://www.uwmidsun.com">www.uwmidsun.com</a>



PROJECT		BMS_Carrier_Board.PrjPcb		<div><div>MIDNIGHT</div><div></div><div>S</div></div> <div>Engineering 5 - 1002 University of Waterloo (519) 888-4567 x32978 hardware@uwmidsun.com</div>
DOCUMENT		BMS Fan and Relay Control		
PART NUMBER	MS-ELE0003	VARIANT	BMS Carrier - Slave Battery Box	
DRAWN BY	Aashmika Mali & Liam Hawkins	REVISION	5.0	
LAST MODIFIED	2019-06-12	SHEET	4 OF 4	

Project: **BMS\_Carrier\_Board.PrjPcb**Title: **Current Sense isoSPI Interface**

Project Lead: Aashmika Mali &amp; Liam Hawkins

Size: **Letter**Revision: **5.0**Date: **2019-06-12**

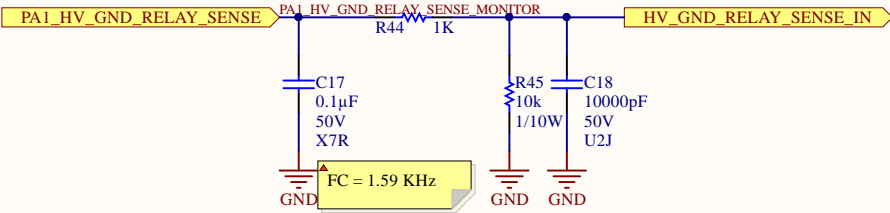
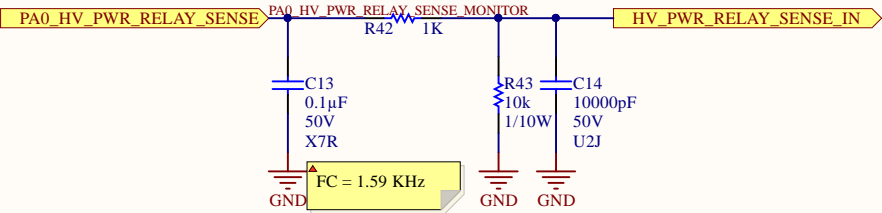
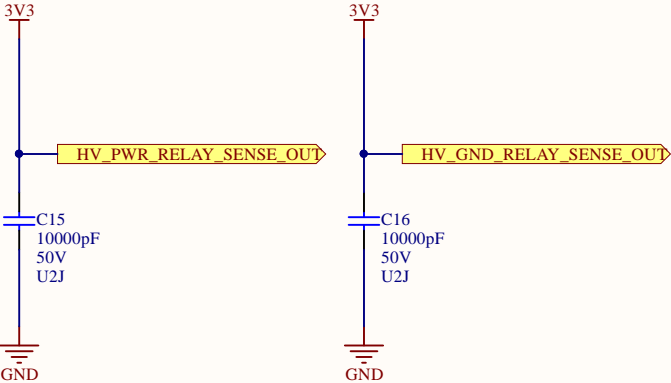
Sheet\* of \*



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200 University Ave W  
Waterloo, ON, Canada  
N2L 3E9

Website: [www.uwmidsun.com](http://www.uwmidsun.com)

Firmware Detection State of Contactor

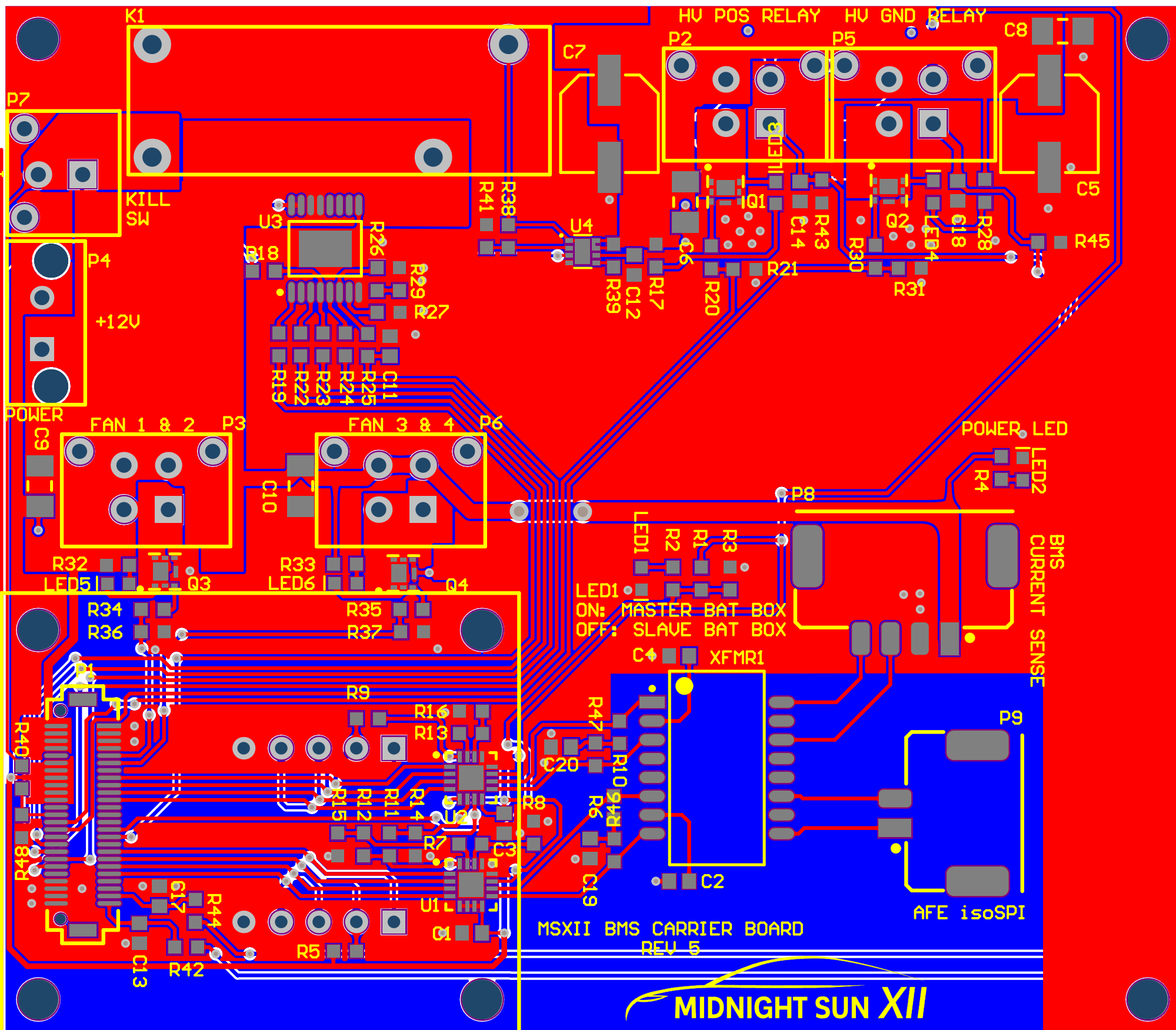


Project: <b>BMS_Carrier_Board.PrjPcb</b>		<div><div>MIDNIGHT</div><div>SUN</div></div>
Title: <b>Firmware Detection State of Contactor</b>		
Project Author <b>Aashmika Mali &amp; Liam Hawkins</b>		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: <b>Letter</b>	Revision: <b>5.0</b>	
Date: <b>2019-06-12</b>	Sheet* of *	Website:

Bill of Materials	
Project:	BMS_Carrier_Board.PrjPcb
Revision:	5.0
Project Lead:	Aashmika Mali & Liam Haw kins
Generated On:	2019-06-12 11:38 PM
Production Quantity:	1
Currency	CAD
Total Parts Count:	70

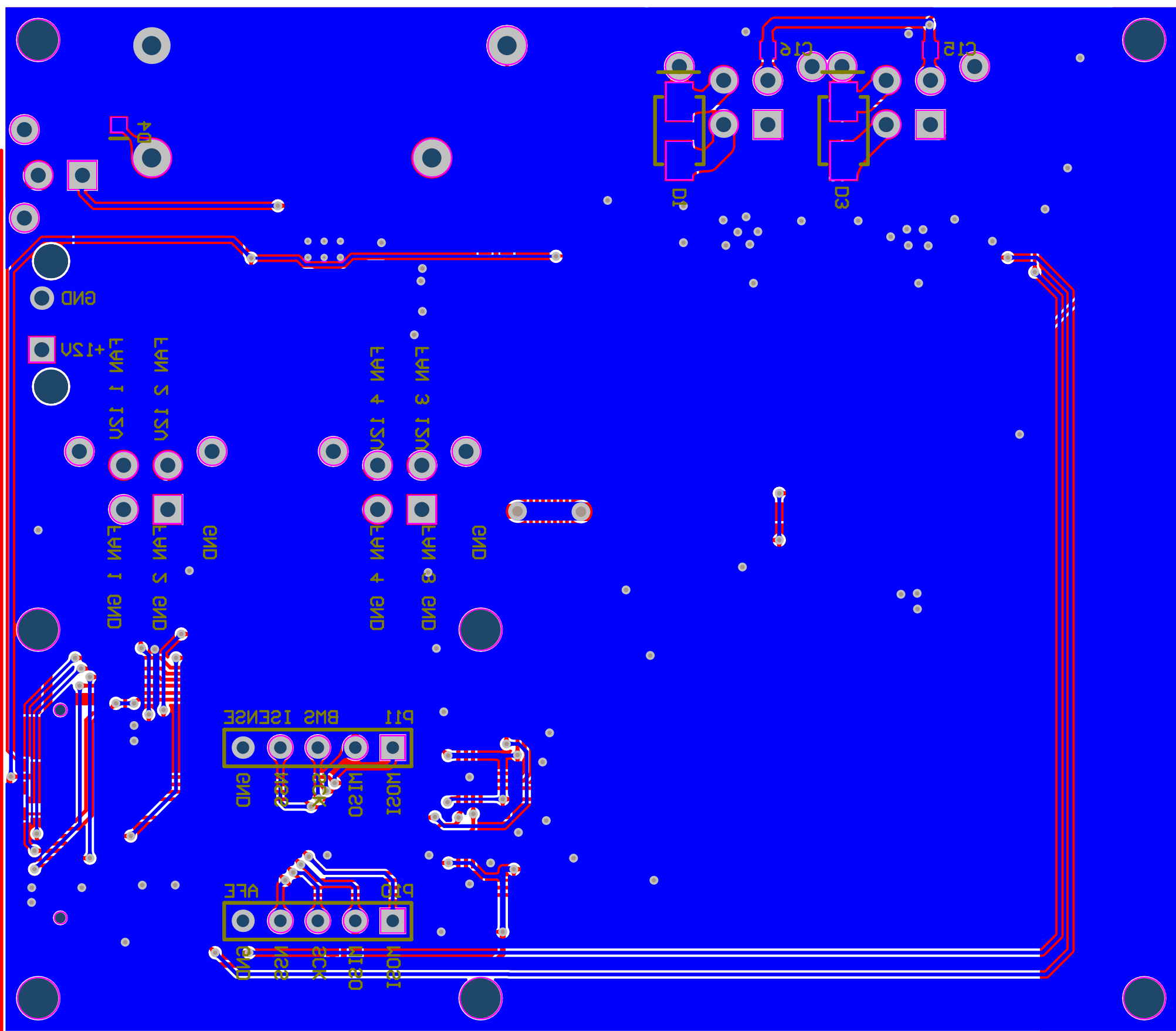
[illegible]

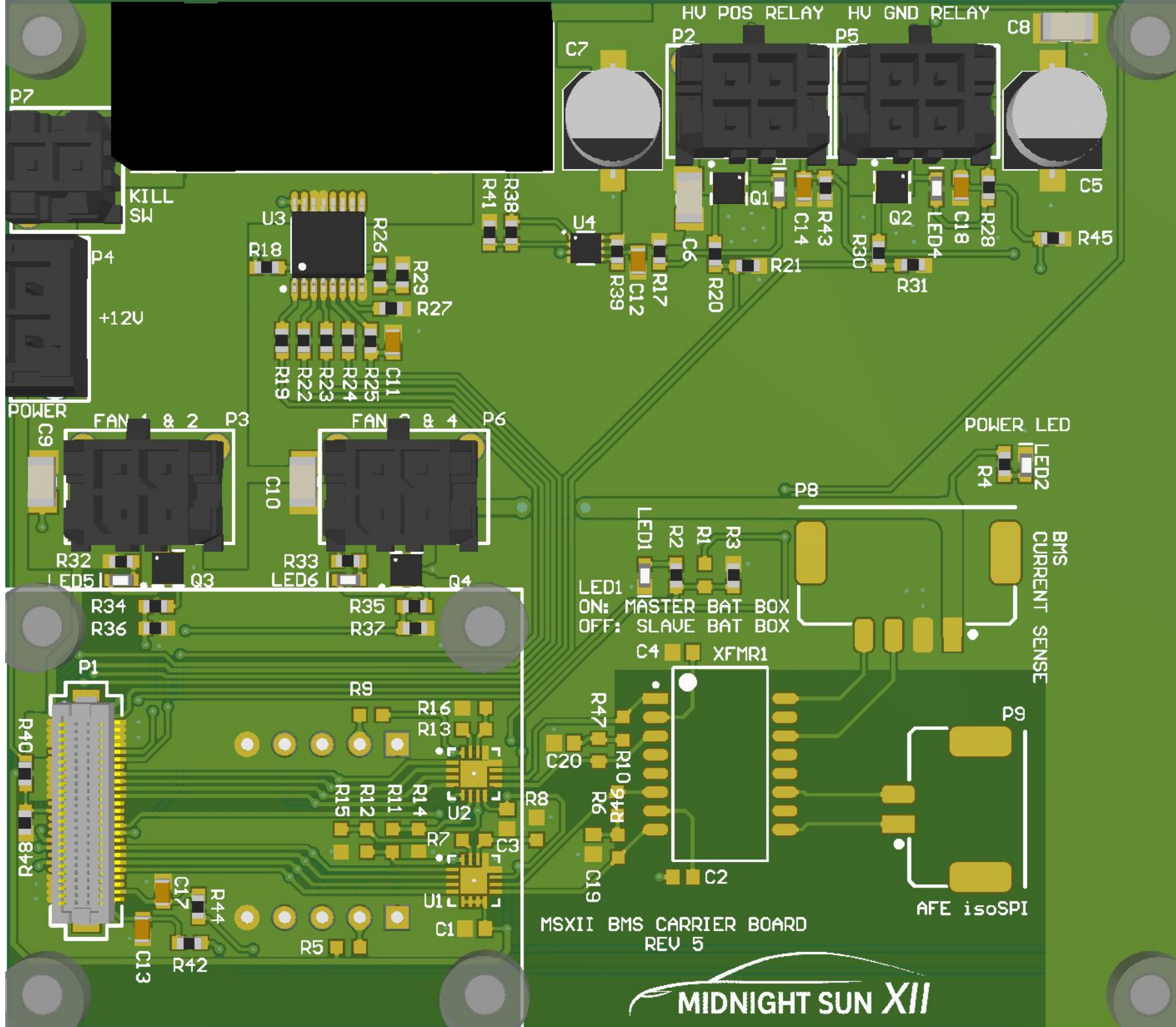




MSXII BMS CARRIER BOARD  
REV 5

MIDNIGHT SUN XII





## Electrical Rules Check Report

Class	Document	Message
Warning	Controller_Board_Interface.SchDoc	Net 3V3 has no driving source (Pin C1-1,Pin C3-1,Pin C15-1,Pin C16-1,Pin P1-40,Pin P1-41,Pin P1-42,Pin P1-43,Pin P1-44,Pin P1-45,Pin P2-3,Pin P5-3,Pin R1-1,Pin R5-1,Pin R9-1,Pin R11-1,Pin R12-1,Pin R18-2,Pin U1-5,Pin U1-6,Pin U1-7,Pin U1-8,Pin U1-11,Pin U1-16,Pin U2-5,Pin U2-8,Pin U2-11,Pin U2-16,Pin U4-3)
Error	BMS Carrier - Connectors.SchDoc	Net 12V_CONTACTOR_COIL_SW contains multiple Input Ports (Port 12V_CONTACTOR_COIL_SW,Port 12V_CONTACTOR_COIL_SW)
Error	BMS Carrier - Battery Relay Controls.SchDoc	Net 12V_CONTACTOR_COIL_SW contains multiple Input Ports (Port 12V_CONTACTOR_COIL_SW,Port 12V_CONTACTOR_COIL_SW,Port HV_GND_RELAY_12V_SW,Port HV_PWR_RELAY_12V_SW)
Error	BMS Carrier - Battery Relay Controls.SchDoc	Net 12V_CONTACTOR_COIL_SW contains multiple Input Ports (Port HV_GND_RELAY_12V_SW,Port HV_PWR_RELAY_12V_SW)
Error	BMS Carrier - Battery Relay Controls.SchDoc	Net NetD1_1 contains multiple Input Ports (Port HV_PWR_RELAY_GND,Port HV_PWR_RELAY_GND)
Error	BMS Carrier - Battery Relay Controls.SchDoc	Net NetD3_1 contains multiple Input Ports (Port HV_GND_RELAY_GND,Port HV_GND_RELAY_GND)
Error	BMS Carrier - Fan Controls.SchDoc	Net NetLED5_2 contains multiple Input Ports (Port FAN_1_GND,Port FAN_1_GND)
Error	BMS Carrier - Fan Controls.SchDoc	Net NetLED6_2 contains multiple Input Ports (Port FAN_2_GND,Port FAN_2_GND)
Error	BMS Carrier - Fan Controls.SchDoc	Net PA9_FAN_2_PWM contains multiple Input Ports (Port PA9_FAN_2_PWM,Port PA9_FAN_2_PWM)
Error	BMS Carrier - Fan Controls.SchDoc	Net PA10_FAN_1_PWM contains multiple Input Ports (Port PA10_FAN_1_PWM,Port PA10_FAN_1_PWM)
Warning	BMS Carrier - AFE Interface.SchDoc	Nets Wire PA0_HV_PWR_RELAY_SENSE has multiple names (Net Label PA0_HV_PWR_RELAY_SENSE,Net Label PA0_HV_PWR_RELAY_SENSE_MONITOR)
Warning	BMS Carrier - AFE Interface.SchDoc	Nets Wire PA1_HV_GND_RELAY_SENSE has multiple names (Net Label PA1_HV_GND_RELAY_SENSE,Net Label PA1_HV_GND_RELAY_SENSE_MONITOR)

## Design Rules Verification Report

Filename : C:\Users\Liam\Documents\UWaterloo\Midnight Sun\Hardware Repository\hardw

Warnings 0  
Rule Violations 102

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( (All) )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.203mm) (Max=2.54mm) (Preferred=0.203mm) (All)	0
Power Plane Connect Rule(Direct Connect )(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=5.08mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	102
Silk To Solder Mask (Clearance=0.254mm) (Disabled)(IsPad),(All)	0
Silk to Silk (Clearance=0.254mm) (Disabled)(All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	102

<b>Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)</b>
Minimum Solder Mask Sliver Constraint: (0.244mm < 0.254mm) Between Pad C13-1(9.324mm,7.675mm) on Top Layer And Pad C17-1(10.7mm,8.825mm)
Minimum Solder Mask Sliver Constraint: (0.027mm < 0.254mm) Between Pad D1-2(45.975mm,63.32mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.027mm < 0.254mm) Between Pad D3-2(57.11mm,63.32mm) on Bottom Layer And Pad P5-0(57mm,65.7mm) on
Minimum Solder Mask Sliver Constraint: (0.226mm < 0.254mm) Between Pad LED5-1(8.649mm,30.645mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.226mm < 0.254mm) Between Pad LED5-2(7.149mm,30.645mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(4mm,22.05mm) on Multi-Layer And Pad P1-(5.5mm,22.8mm) on Top
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.254mm) Between Pad P1-(4mm,7.95mm) on Multi-Layer And Pad P1-(5.5mm,7.2mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad P2-0(54.975mm,65.7mm) on Multi-Layer And Pad P5-0(57mm,65.7mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q1-1(48.025mm,57.8mm) on Top Layer And Pad Q1-2(48.025mm,57.15mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q1-2(48.025mm,57.15mm) on Top Layer And Pad Q1-3(48.025mm,56.5mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q1-3(48.025mm,56.5mm) on Top Layer And Pad Q1-7(48.95mm,57.45mm)
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.254mm) Between Pad Q1-3(48.025mm,56.5mm) on Top Layer And Pad Q1-8(48.95mm,56.41mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q1-4(49.875mm,56.5mm) on Top Layer And Pad Q1-5(49.875mm,57.15mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q1-4(49.875mm,56.5mm) on Top Layer And Pad Q1-7(48.95mm,57.45mm)
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.254mm) Between Pad Q1-4(49.875mm,56.5mm) on Top Layer And Pad Q1-8(48.95mm,56.41mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q1-5(49.875mm,57.15mm) on Top Layer And Pad Q1-6(49.875mm,57.8mm)
Minimum Solder Mask Sliver Constraint: (0.187mm < 0.254mm) Between Pad Q1-7(48.95mm,57.45mm) on Top Layer And Pad Q1-8(48.95mm,56.41mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q2-1(59.075mm,57.884mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q2-2(59.075mm,57.234mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q2-3(59.075mm,56.584mm) on Top Layer And Pad Q2-7(60mm,57.534mm)
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.254mm) Between Pad Q2-3(59.075mm,56.584mm) on Top Layer And Pad Q2-8(60mm,56.494mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q2-4(60.925mm,56.584mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q2-4(60.925mm,56.584mm) on Top Layer And Pad Q2-7(60mm,57.534mm)
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.254mm) Between Pad Q2-4(60.925mm,56.584mm) on Top Layer And Pad Q2-8(60mm,56.494mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q2-5(60.925mm,57.234mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.187mm < 0.254mm) Between Pad Q2-7(60mm,57.534mm) on Top Layer And Pad Q2-8(60mm,56.494mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q3-1(10.4mm,30.525mm) on Top Layer And Pad Q3-2(11.05mm,30.525mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q3-2(11.05mm,30.525mm) on Top Layer And Pad Q3-3(11.7mm,30.525mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q3-3(11.7mm,30.525mm) on Top Layer And Pad Q3-7(10.75mm,31.45mm)
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.254mm) Between Pad Q3-3(11.7mm,30.525mm) on Top Layer And Pad Q3-8(11.79mm,31.45mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q3-4(11.7mm,32.375mm) on Top Layer And Pad Q3-5(11.05mm,32.375mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q3-4(11.7mm,32.375mm) on Top Layer And Pad Q3-7(10.75mm,31.45mm)
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.254mm) Between Pad Q3-4(11.7mm,32.375mm) on Top Layer And Pad Q3-8(11.79mm,31.45mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q3-5(11.05mm,32.375mm) on Top Layer And Pad Q3-6(10.4mm,32.375mm)
Minimum Solder Mask Sliver Constraint: (0.187mm < 0.254mm) Between Pad Q3-7(10.75mm,31.45mm) on Top Layer And Pad Q3-8(11.79mm,31.45mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q4-1(26.528mm,30.402mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q4-2(27.178mm,30.402mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q4-3(27.828mm,30.402mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.254mm) Between Pad Q4-3(27.828mm,30.402mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q4-4(27.828mm,32.252mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q4-4(27.828mm,32.252mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.202mm < 0.254mm) Between Pad Q4-4(27.828mm,32.252mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad Q4-5(27.178mm,32.252mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.187mm < 0.254mm) Between Pad Q4-7(26.878mm,31.327mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U1-1(30.325mm,11mm) on Top Layer And Pad U1-17(31.75mm,10.25mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-1(30.325mm,11mm) on Top Layer And Pad U1-2(30.325mm,10.5mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-10(33.175mm,10mm) on Top Layer And Pad U1-11(33.175mm,10.5mm)
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U1-10(33.175mm,10mm) on Top Layer And Pad U1-17(31.75mm,10.25mm)
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-10(33.175mm,10mm) on Top Layer And Pad U1-9(33.175mm,9.5mm) on
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-11(33.175mm,10.5mm) on Top Layer And Pad U1-12(33.175mm,11mm)
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U1-11(33.175mm,10.5mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.022mm < 0.254mm) Between Pad U1-12(33.175mm,11mm) on Top Layer And Pad U1-17(31.75mm,10.25mm)

