







# **Electrical Rules Check Report**

Class	Document	Message
Warning	Center Console.SchDoc	Off grid Net Label CONSOLE_IO_INTERRUPT at 8013.711mil,4100mil
Warning	Center Console.SchDoc	Off grid Net Label GP0/POWER_BTN at 2283.468mil,6700mil
Warning	Center Console.SchDoc	Off grid Net Label GP0/POWER_BTN at 8383.469mil,4900mil
Warning	Center Console.SchDoc	Off grid Net Label GP0/POWER_LED at 2290.883mil,6600mil
Warning	Center Console.SchDoc	Off grid Net Label GP0/POWER_LED at 8390.883mil,2900mil
Warning	Center Console.SchDoc	Off grid Net Label GP1/DRIVE_BTN at 2323.636mil,6500mil
Warning	Center Console.SchDoc	Off grid Net Label GP1/DRIVE_BTN at 8423.636mil,4800mil
Warning	Center Console.SchDoc	Off grid Net Label GP1/DRIVE_LED at 2331.05mil,6400mil
Warning	Center Console.SchDoc	Off grid Net Label GP1/DRIVE_LED at 8431.05mil,2800mil
Warning	Center Console.SchDoc	Off grid Net Label GP2/NEUTRAL_BTN at 2178.177mil,6300mil
Warning	Center Console.SchDoc	Off grid Net Label GP2/NEUTRAL_BTN at 8278.177mil,4700mil
Warning	Center Console.SchDoc	Off grid Net Label GP2/NEUTRAL_LED at 2185.592mil,6200mil
Warning	Center Console.SchDoc	Off grid Net Label GP2/NEUTRAL_LED at 8285.592mil,2700mil
Warning	Center Console.SchDoc	Off grid Net Label GP3/REVERSE_BTN at 2198.151mil,5600mil
Warning	Center Console.SchDoc	Off grid Net Label GP3/REVERSE_BTN at 8298.151mil,4600mil
Warning	Center Console.SchDoc	Off grid Net Label GP3/REVERSE_LED at 2205.565mil,5500mil
Warning	Center Console.SchDoc	Off grid Net Label GP3/REVERSE_LED at 8305.565mil,2600mil
Warning	Center Console.SchDoc	Off grid Net Label GP4/HAZARDS_BTN at 2173.063mil,5400mil
Warning	Center Console.SchDoc	Off grid Net Label GP4/HAZARDS_BTN at 8273.063mil,4500mil
Warning	Center Console.SchDoc	Off grid Net Label GP4/HAZARDS_LED at 2180.477mil,5300mil
Warning	Center Console.SchDoc	Off grid Net Label GP4/HAZARDS_LED at 8280.477mil,2500mil
Warning	Center Console.SchDoc	Off grid Net Label GP5/LOWBEAMS_BTN at 2082.807mil,5200mil
Warning	Center Console.SchDoc	Off grid Net Label GP5/LOWBEAMS_BTN at 8182.807mil,4400mil
Warning	Center Console.SchDoc	Off grid Net Label GP5/LOWBEAMS_LED at 2090.221mil,5100mil
Warning	Center Console.SchDoc	Off grid Net Label GP5/LOWBEAMS_LED at 8190.221mil,2400mil
Warning	Center Console.SchDoc	Off grid Net Label GP6/DRL_BTN at 2418.918mil,4400mil
Warning	Center Console.SchDoc	Off grid Net Label GP6/DRL_BTN at 8518.918mil,4300mil
Warning	Center Console.SchDoc	Off grid Net Label GP6/DRL_LED at 2426.332mil,4300mil
Warning	Center Console.SchDoc	Off grid Net Label GP6/DRL_LED at 8526.332mil,2300mil
Warning	Center Console.SchDoc	Off grid Net Label GP7/BPS_FAULT_LED at 2110.151mil,4100mi
Warning	Center Console.SchDoc	Off grid Net Label GP7/BPS_FAULT_LED at 8210.151mil,2200mil
Warning	Center Console.SchDoc	Off grid Net Label GP7/SPARE_IN at 2403.795mil,4200mil
Warning	Center Console.SchDoc	Off grid Net Label GP7/SPARE_IN at 8503.795mil,4200mil

## **Design Rules Verification Report**

Filename: \\vmware-host\Shared Folders\projects\hardware\MSXII\_Center\_Console\_Switch

Warnings 0

Rule Violations 16

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( (All) )	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.635mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	4
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	9
Silk to Silk (Clearance=0.254mm) (All),(All)	3
Net Antennae (Tolerance=0mm) (AII)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	16

#### Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)

Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm

Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(2.5mm,57.5mm) on Multi-Layer Actual Hole Size = 2.7mm

Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(57.5mm,2.5mm) on Multi-Layer Actual Hole Size = 2.7mm

Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(57.5mm,57.5mm) on Multi-Layer Actual Hole Size = 2.7mm

### Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (0.209mm < 0.254mm) Between Pad LED1-2(22.376mm,52.832mm) on Top Layer Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P1-(27.8mm,6mm) on Top Layer And Tracl Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P1-(49mm,6mm) on Top Layer And Tracl Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P2-(7.495mm,32.45mm) on Top Layer And Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P2-(7.495mm,53.65mm) on Top Layer And Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P3-(54mm,18.8mm) on Top Layer And Tracl Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P3-(54mm,40mm) on Top Layer And Tracl Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P4-(7.495mm,28.925mm) on Top Layer And Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P4-(7.495mm,28.925mm) on Top Layer And Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P4-(7.495mm,7.725mm) on Top Layer And Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P4-(7.495mm,7.725mm) on Top Layer And Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P4-(7.495mm,7.725mm) on Top Layer And Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P4-(7.495mm,7.725mm) on Top Layer And Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P4-(7.495mm,7.725mm) on Top Layer And Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P4-(7.495mm,7.725mm) on Top Layer And Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P4-(7.495mm,7.725mm) on Top Layer And Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P4-(7.495mm,7.725mm) on Top Layer And Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P4-(7.495mm,7.725mm) on Top Layer And Silk To Solder Mask Clear

#### Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Arc (46.02mm,21mm) on Top Overlay And Text "NEUTRAL Silk To Silk Clearance Constraint: (0.19mm < 0.254mm) Between Text "U1" (31.242mm,23.769mm) on Top Overlay And Trac Silk To Silk Clearance Constraint: (0.194mm < 0.254mm) Between Text "U1" (31.242mm,23.769mm) on Top Overlay And Trac Silk To Silk Clearance Constraint: (0.194mm < 0.254mm) Between Text "U1" (31.242mm,23.769mm) on Top Overlay And Trac Silk To Silk Clearance Constraint: (0.194mm < 0.254mm) Between Text "U1" (31.242mm,23.769mm) on Top Overlay And Trac Silk To Silk Clearance Constraint: (0.194mm < 0.254mm) Between Text "U1" (31.242mm,23.769mm) on Top Overlay And Trac Silk To Silk Clearance Constraint: (0.194mm < 0.254mm) Between Text "U1" (31.242mm,23.769mm) on Top Overlay And Trac Silk To Silk Clearance Constraint: (0.194mm < 0.254mm) Between Text "U1" (31.242mm,23.769mm) on Top Overlay And Trac Silk To Silk Clearance Constraint: (0.194mm < 0.254mm) Between Text "U1" (31.242mm,23.769mm) on Top Overlay And Trac Silk To Silk Clearance Constraint: (0.194mm < 0.254mm) Between Text "U1" (31.242mm,23.769mm) on Top Overlay And Text "U1" (31.242mm,23.769mm) on Top Overlay And