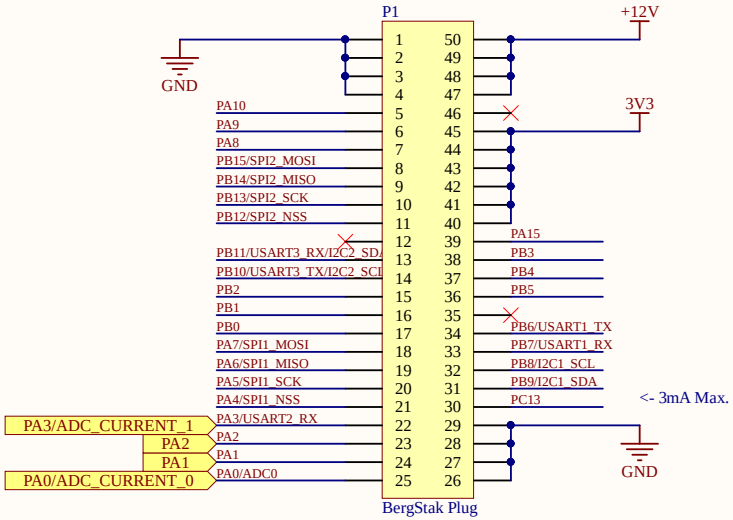
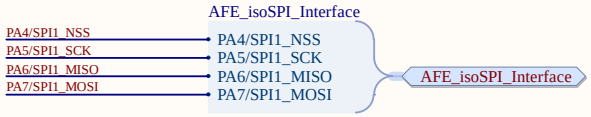
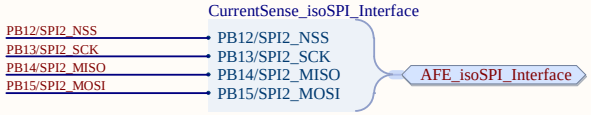






Project: ***BMS_Carrier_Board.PrjPcb***		MIDNIGHT SUN
Title: **Controller Board Interface**		
Project Lead: Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 2.1	
Date: 2017-10-30	Sheet 1 of 4	Website: www.uwmidsun.com

Table 4. SPI Modes

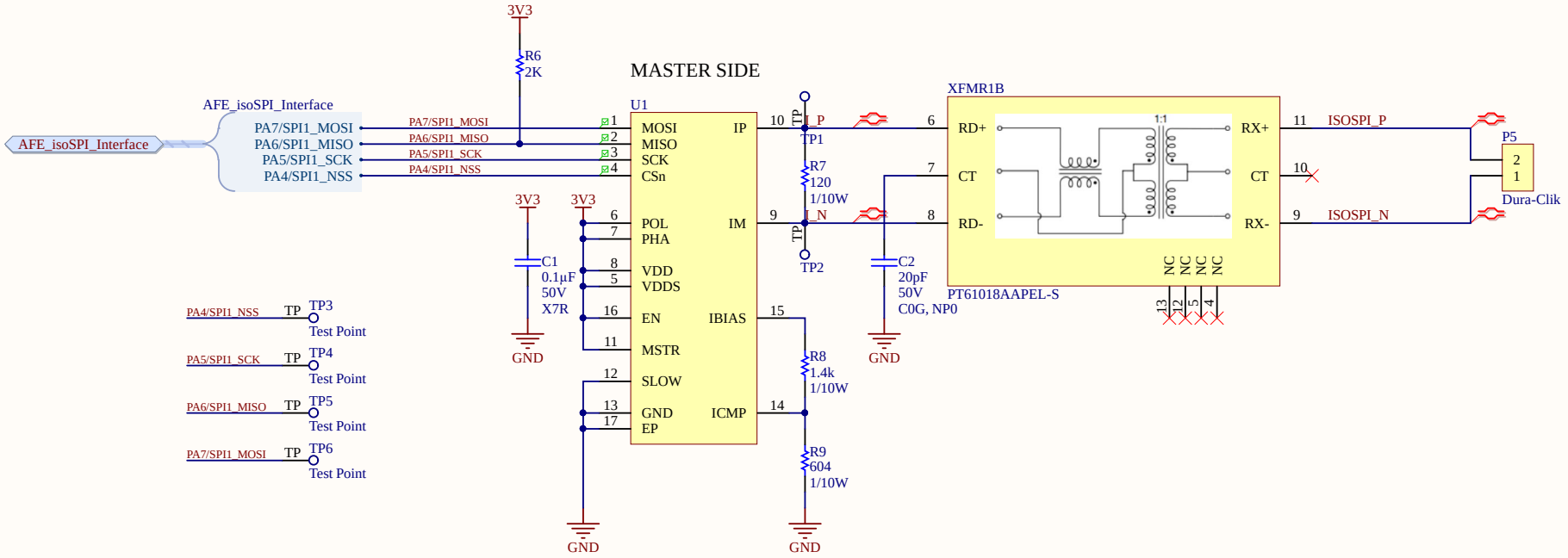
MODE	POL	PHA	DESCRIPTION
0	0	0	SCK Idles Low, Latches on Rising (1st) Edge
1	0	1	SCK Idles Low, Latches on Falling (2nd) Edge
2	1	0	SCK Idles High, Latches on Falling (1st) Edge
3	1	1	SCK Idles High, Latches on Rising (2nd) Edge

SCK idles high, latches on 2nd rising edge

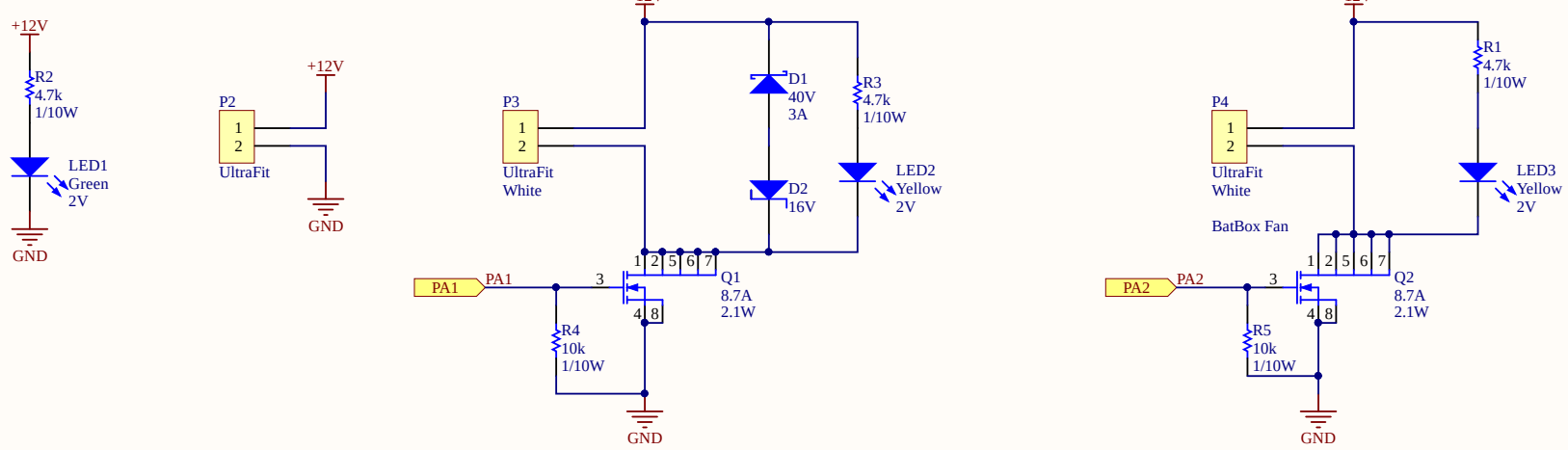
Pulse Drive Current I_IP = 20*I_BIAS = 20mA

Transmitted Differential Signal Amplitude V_A = I_IP*120/2 = 1.2V

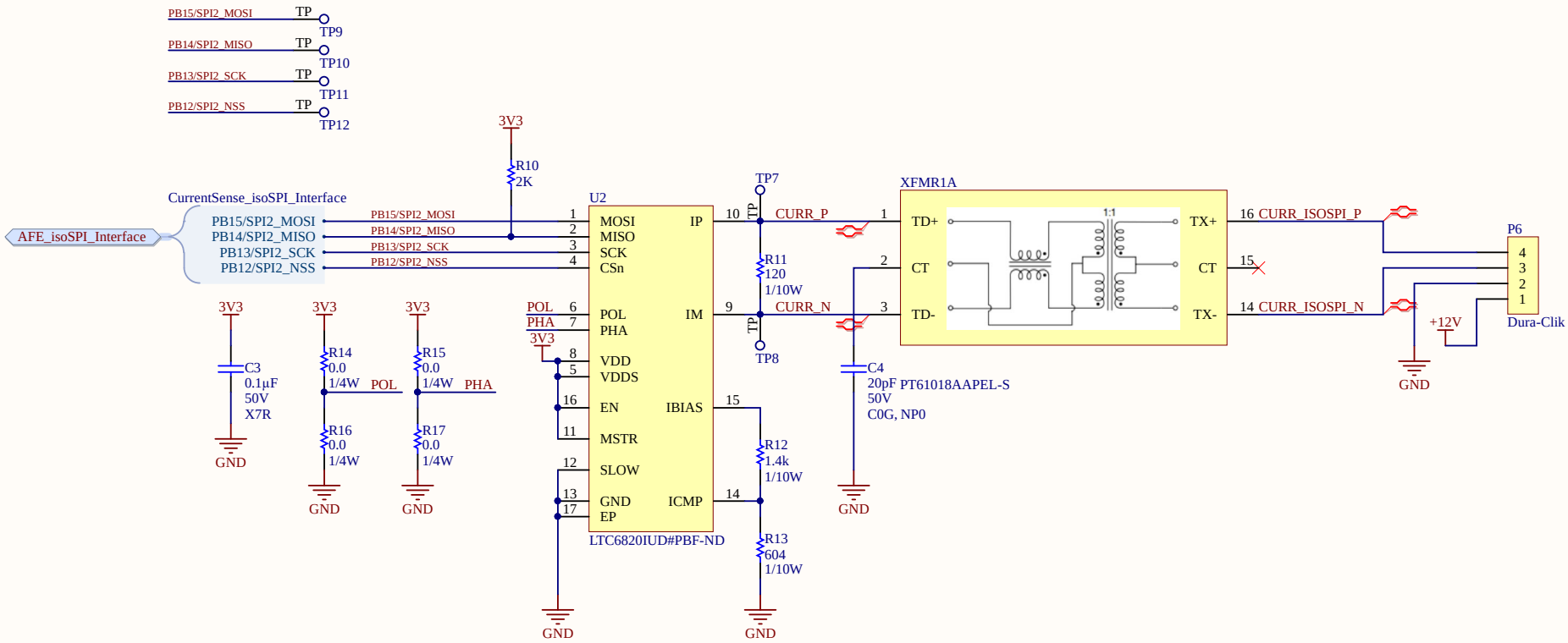
Bias Current I_BIAS can be adjusted from 0.1mA to 1mA
Currently set to 1mA



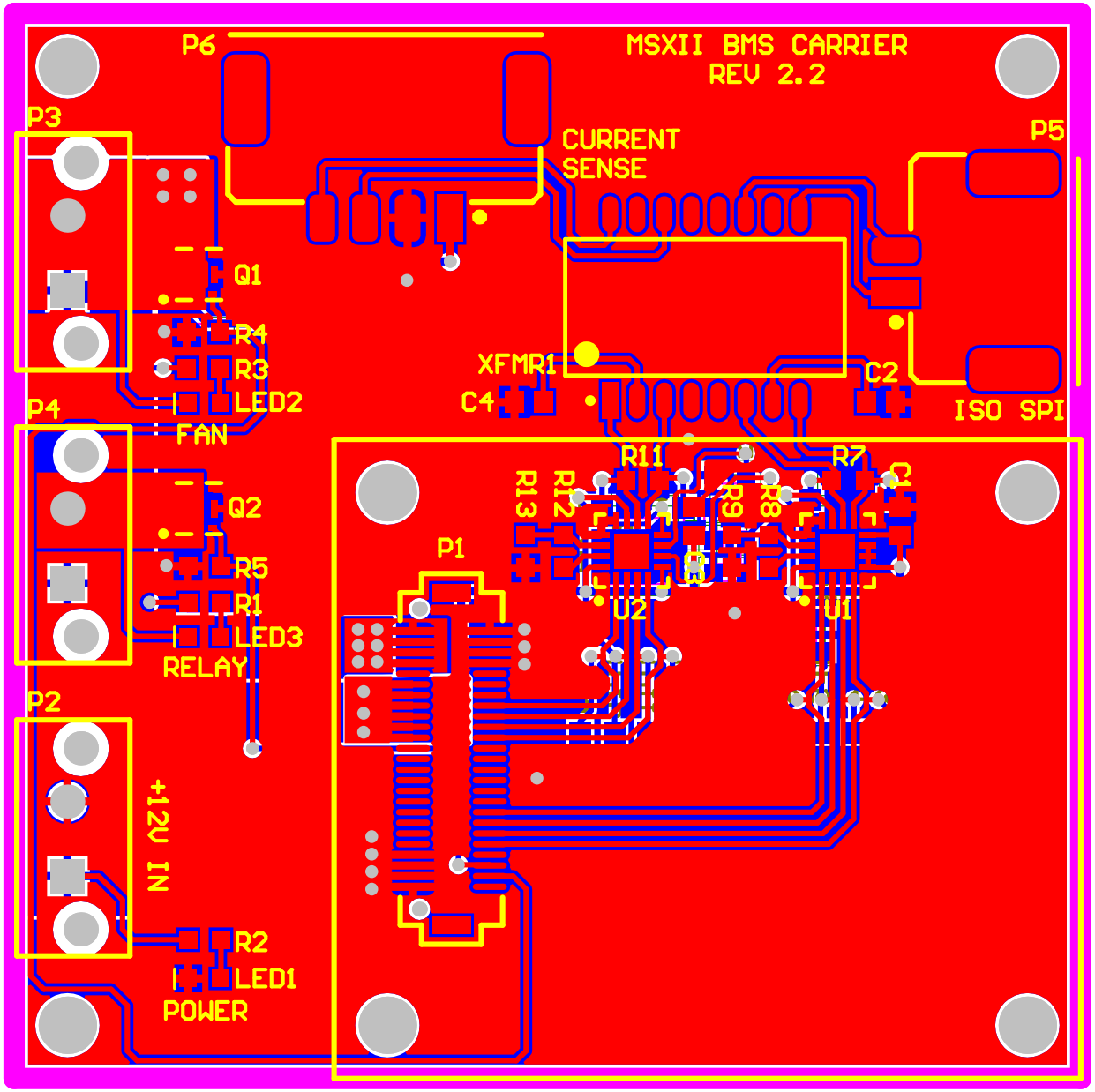
Project: *BMS_Carrier_Board.PrjPcb*		MIDNIGHT SUN
Title: **BMS Interface**		
Project Lead: Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 2.1	
Date: 2017-10-30	Sheet 3 of 4	Website: www.uwmidsun.com

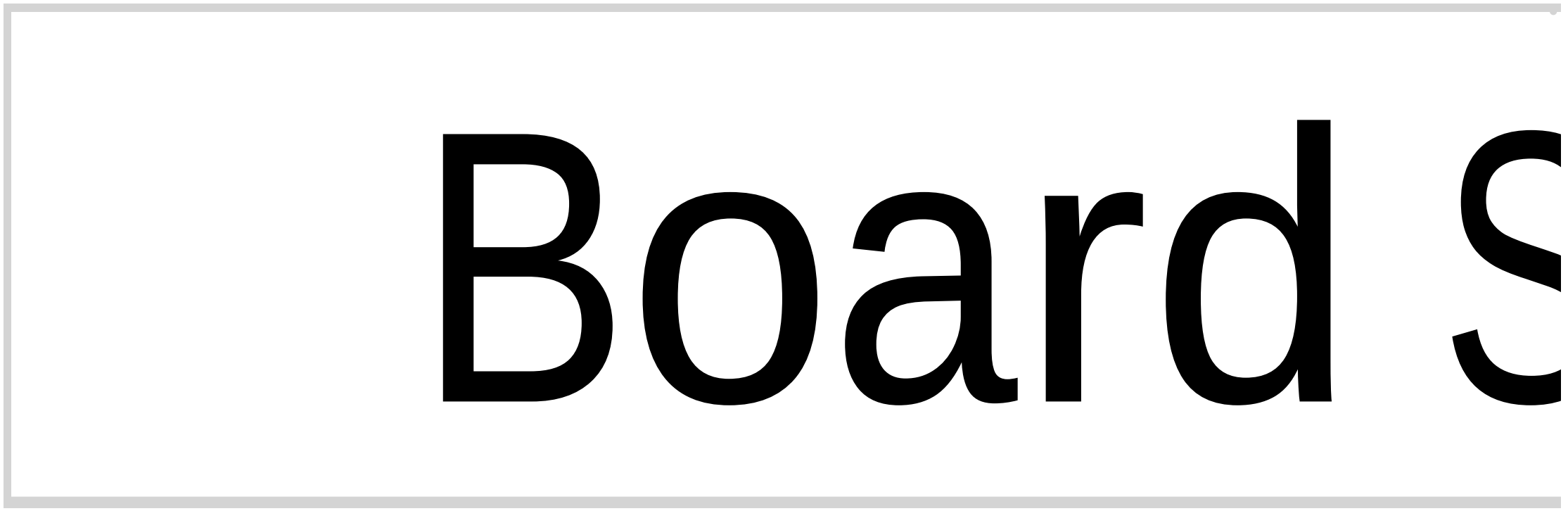


Project: ***BMS_Carrier_Board.PrjPcb***		MIDNIGHT SUN
Title: **BMS Fan and Relay Control**		
Project Lead: Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 2.1	
Date: 2017-10-30	Sheet 4 of 4	Website: www.uwmidsun.com



Project: ***BMS_Carrier_Board.PrjPcb***		MIDNIGHT SUN
Title: **Current Sense isoSPI Interface**		
Project Lead: Taiping Li		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 2.1	
Date: 2017-10-30	Sheet* of *	Website: www.uwmidsun.com


MSXII BMS CARRIER
REV 2.2
P6
P3
P4
P2
P5
P1
CURRENT
SENSE
Q1
R4
R3
LED2
FAN
Q2
R5
R1
LED3
RELAY
R2
LED1
POWER
+12V IN
XFMR1
C4
C2
ISO SPI
R11
R7
C1
R12
R13
R9
R8
U2
U1


Board S