
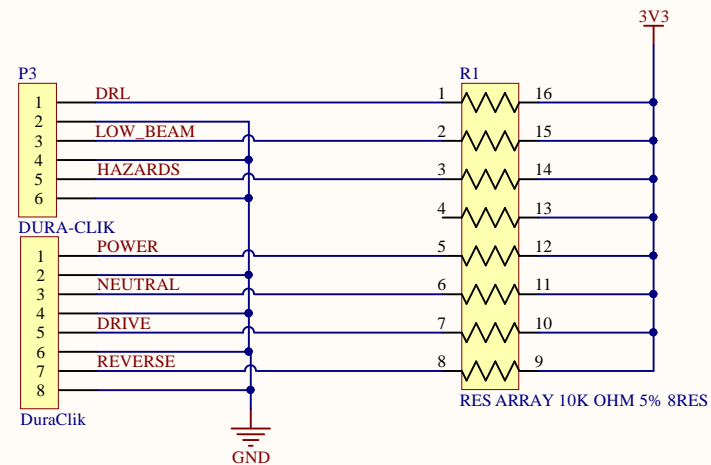


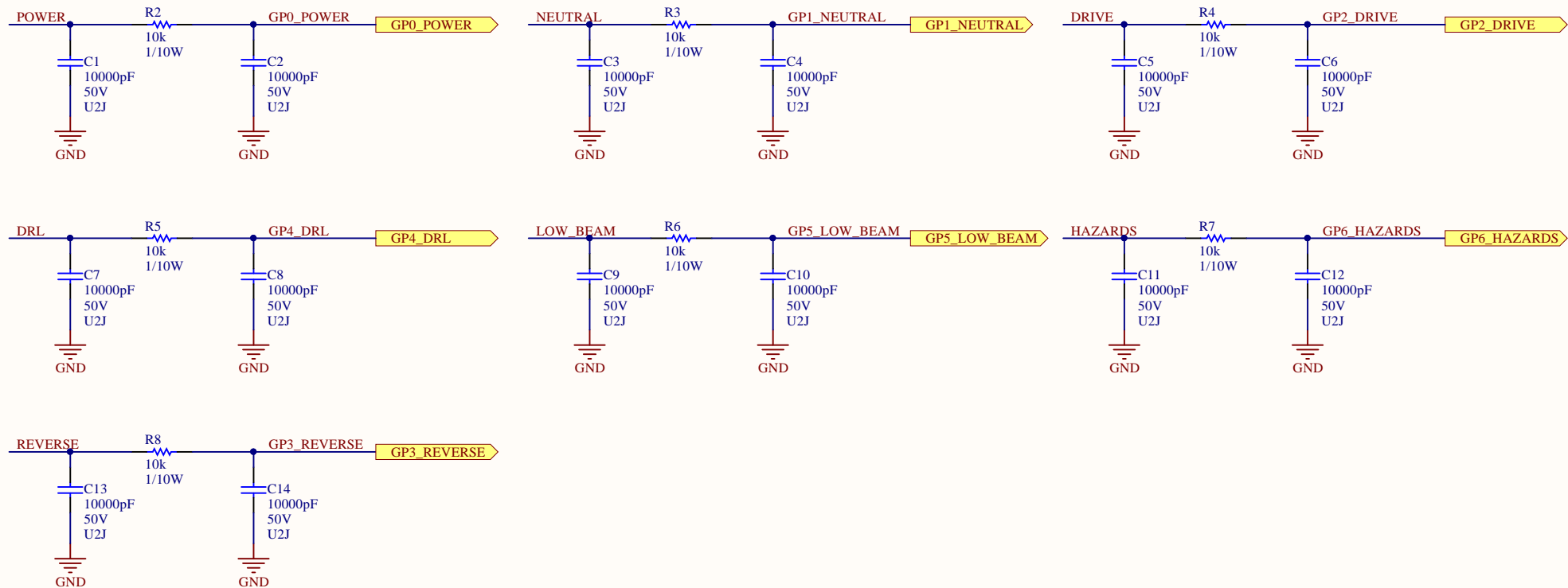
Project: <i>MSXII_Center_Console_Switches.PrjPcb</i>		
Title: Center Console IO Expander		
Project Author: Media Labib		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9 Website: www.uwmidsun.com
Size: Letter	Revision: 1.2	
Date: 2018-05-21	Sheet 1 of 2	

A



A

B




B

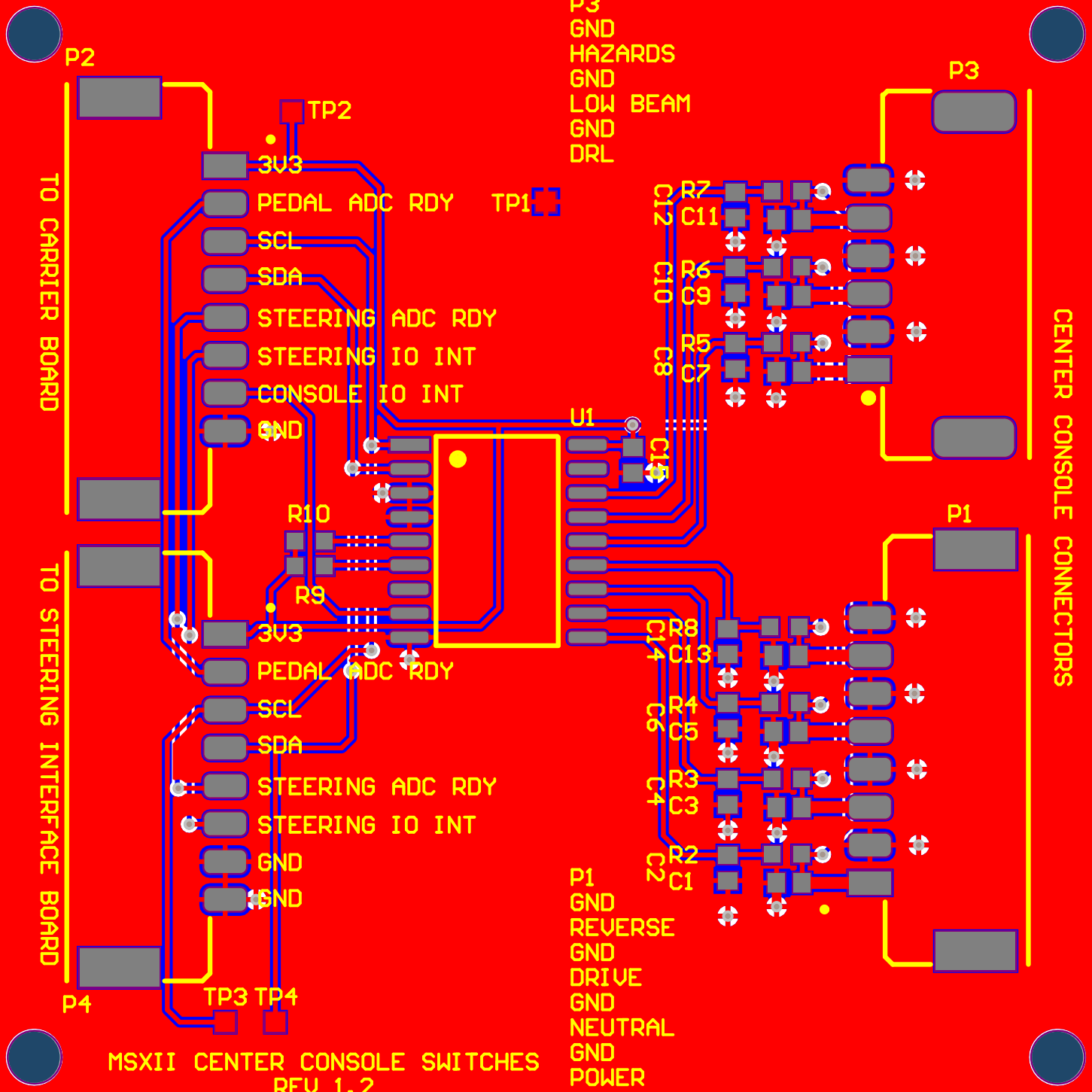
C

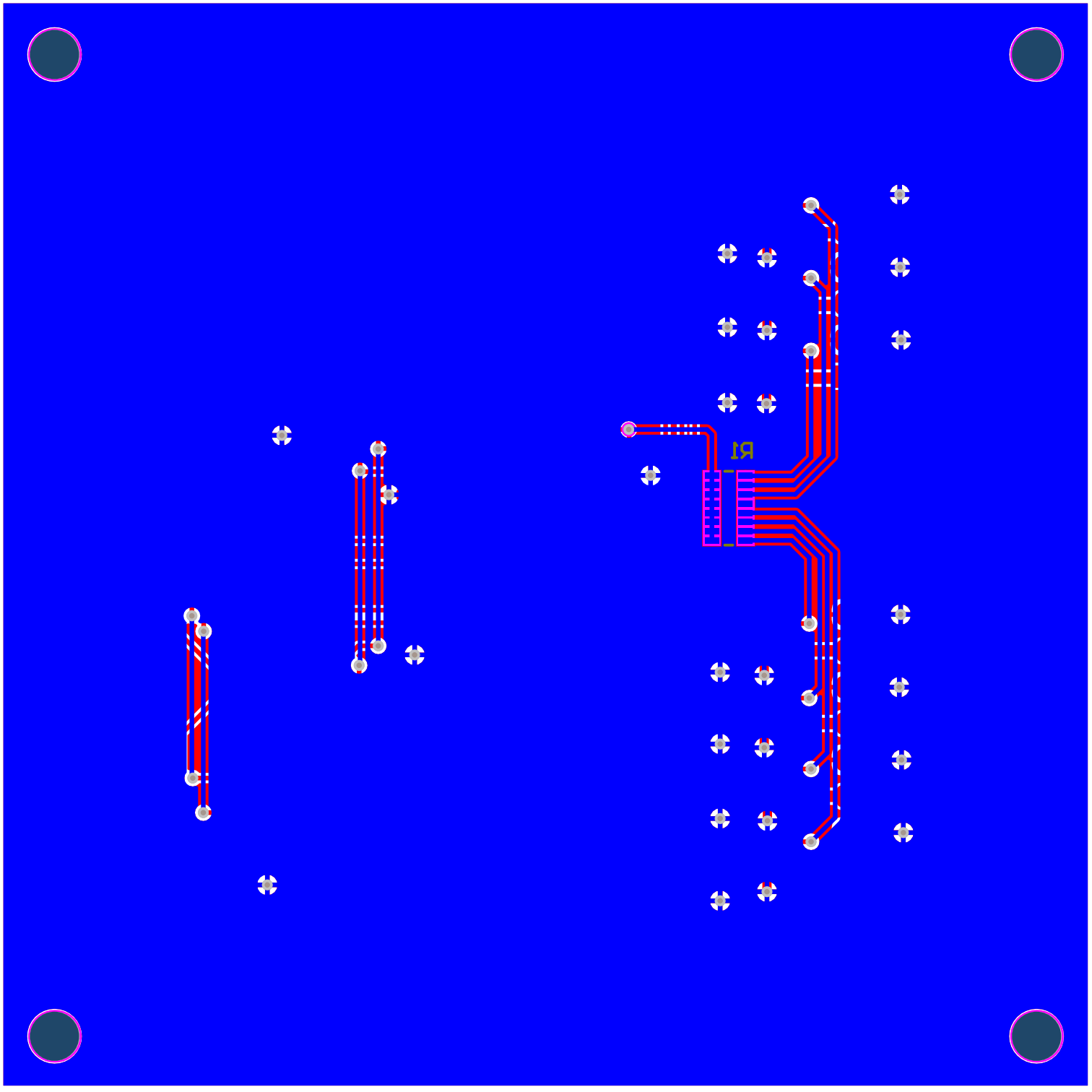
C

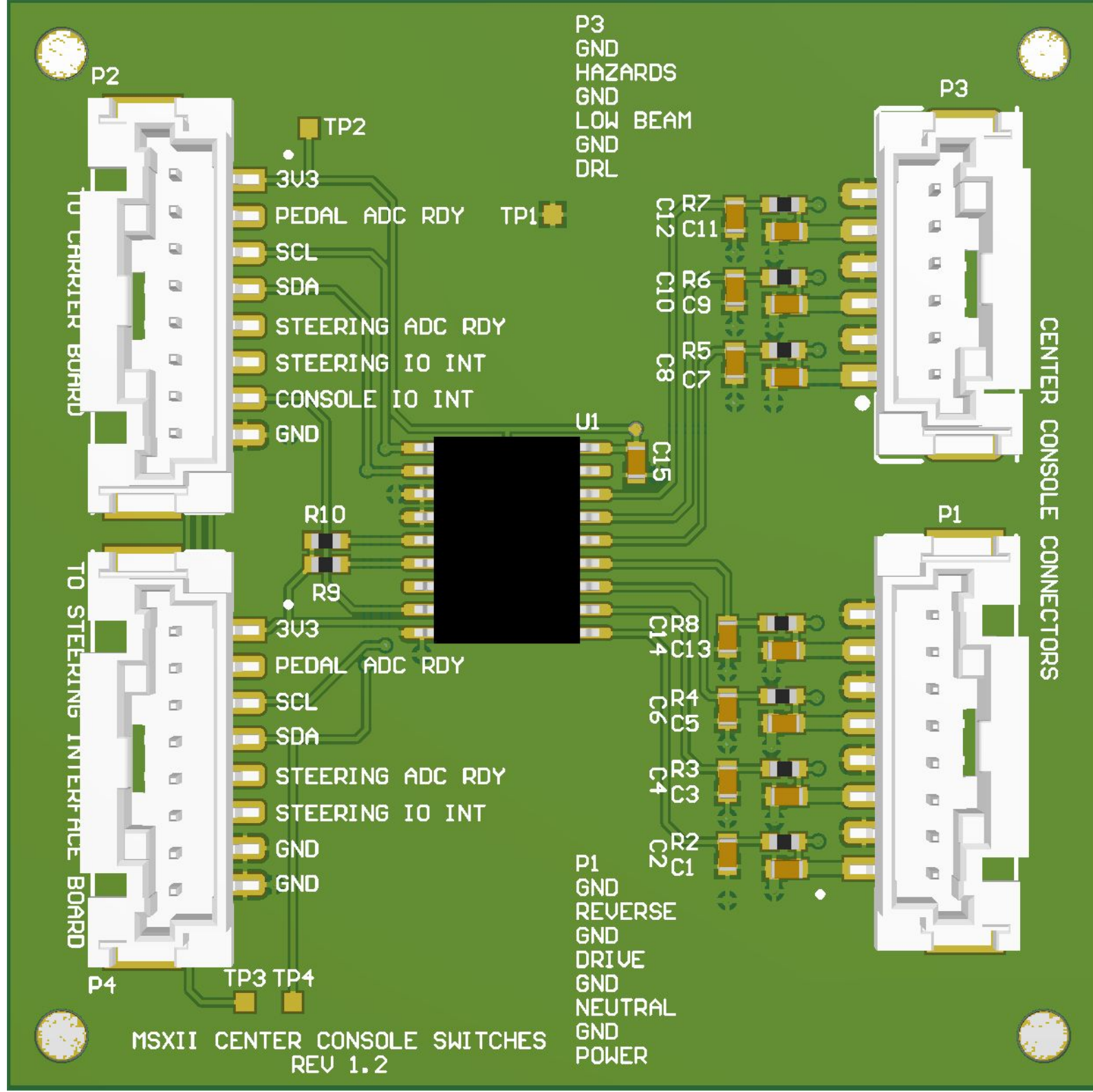
D

D

Project: <i>MSXII_Center_Console_Switches.PrjPcb</i>		
Title: Center Console Inputs		
Project Author: Mena Labib		University of Waterloo 200 University Ave W Waterloo, ON, Canada N2L 3E9
Size: Letter	Revision: 1.2	
Date: 2018-05-21	Sheet2 of 2	
		Website: www.uwmidsun.com







Electrical Rules Check Report

Class	Document	Message
Warning	Center Console - IO Expander.SchDoc	GP0_POWER contains IO Pin and Input Port objects (Port GP0_POWER)
Warning	Center Console - IO Expander.SchDoc	GP1_NEUTRAL contains IO Pin and Input Port objects (Port GP1_NEUTRAL)
Warning	Center Console - IO Expander.SchDoc	GP2_DRIVE contains IO Pin and Input Port objects (Port GP2_DRIVE)
Warning	Center Console - IO Expander.SchDoc	GP3_REVERSE contains IO Pin and Input Port objects (Port GP3_REVERSE)
Warning	Center Console - IO Expander.SchDoc	GP4_DRL contains IO Pin and Input Port objects (Port GP4_DRL)
Warning	Center Console - IO Expander.SchDoc	GP5_LOW_BEAM contains IO Pin and Input Port objects (Port GP5_LOW_BEAM)
Warning	Center Console - IO Expander.SchDoc	GP6_HAZARDS contains IO Pin and Input Port objects (Port GP6_HAZARDS)
Warning	Center Console - IO Expander.SchDoc	NetR9_2 has no driving source (Pin R9-2,Pin U1-6)
Warning	Center Console - IO Expander.SchDoc	NetR10_2 has no driving source (Pin R10-2,Pin U1-5)

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\MidnightSun\hardware\MSXII_Center_Console_Swit

Warnings 0

Rule Violations 23

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.635mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	4
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	3
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	6
Silk to Silk (Clearance=0.254mm) (All),(All)	10
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	23

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(3mm,3mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(3mm,57mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(57mm,3mm) on Multi-Layer Actual Hole Size = 2.7mm	
Hole Size Constraint: (2.7mm > 2.54mm) Pad Free-(57mm,57mm) on Multi-Layer Actual Hole Size = 2.7mm	

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad C15-1(34.6mm,35.2mm) on Top Layer And Via (34.575mm,36.375mm) from	
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-1(16.775mm,30.225mm) on Top Layer And Pad	
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R10-2(18.325mm,30.225mm) on Top Layer And Pad	

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	
Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P1-(52.68mm,29.8mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P1-(52.68mm,8.6mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P2-(7.495mm,32.45mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P2-(7.495mm,53.65mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P4-(7.495mm,28.925mm) on Top Layer And Track	
Silk To Solder Mask Clearance Constraint: (0.153mm < 0.254mm) Between Pad P4-(7.495mm,7.725mm) on Top Layer And Track	

Silk to Silk (Clearance=0.254mm) (All),(All)	
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "C1" (36.6mm,11.9mm) on Top Overlay And Text "C2" (35.4mm,13.7mm) on Top	
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "C13" (36.6mm,23.9mm) on Top Overlay And Text "C14" (35.4mm,26mm) on Top	
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "C14" (35.4mm,26mm) on Top Overlay And Text "R8" (36.6mm,25.275mm) on Top	
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "C2" (35.4mm,13.7mm) on Top Overlay And Text "R2" (36.6mm,13.3mm) on Top	
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "C3" (36.6mm,15.9mm) on Top Overlay And Text "C4" (35.4mm,17.7mm) on Top	
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "C4" (35.4mm,17.7mm) on Top Overlay And Text "R3" (36.6mm,17.3mm) on Top	
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "C5" (36.6mm,19.8mm) on Top Overlay And Text "C6" (35.4mm,21.6mm) on Top	
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "C6" (35.4mm,21.6mm) on Top Overlay And Text "R4" (36.6mm,21.2mm) on Top	
Silk To Silk Clearance Constraint: (0.241mm < 0.254mm) Between Text "TP3" (12mm,5.8mm) on Top Overlay And Track	
Silk To Silk Clearance Constraint: (0.241mm < 0.254mm) Between Text "TP3" (12mm,5.8mm) on Top Overlay And Track	