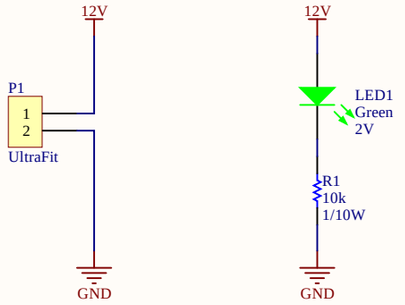
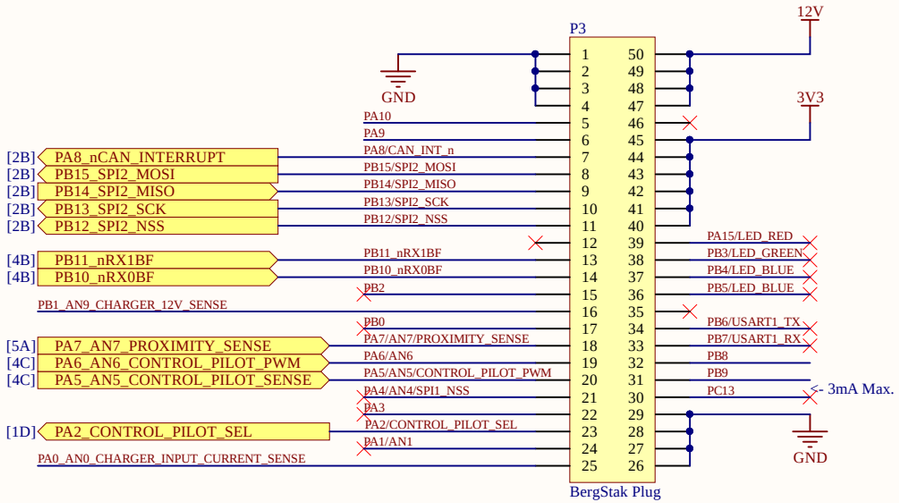
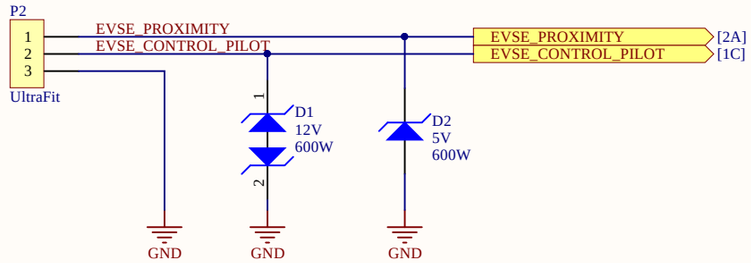
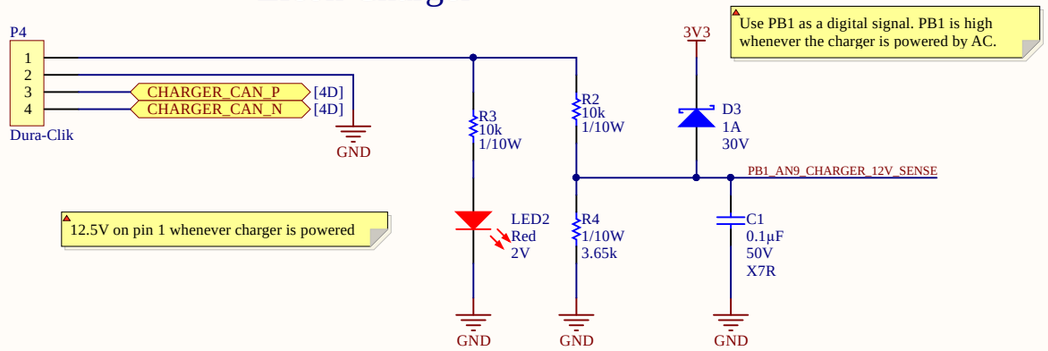


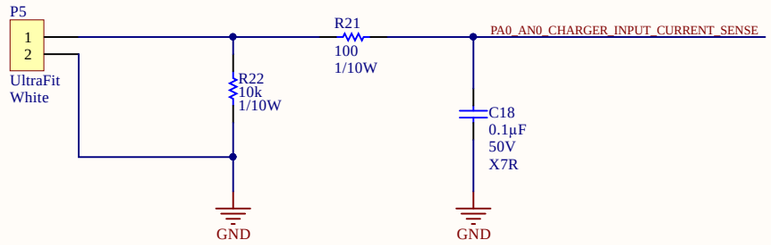


Vehicle Inlet



Elcon Charger





PROJECT	MSXII_ChargerInterface.PrjPcb		MIDNIGHT SUN
DOCUMENT	Charger Interface - Connectors		
PART NUMBER	MS40013-03	VARIANT	[No Variations]
DRAWN BY	Taiping Li, Peiliang Guo	REVISION	3.0
LAST MODIFIED	2019-03-17	SHEET	1 OF 3

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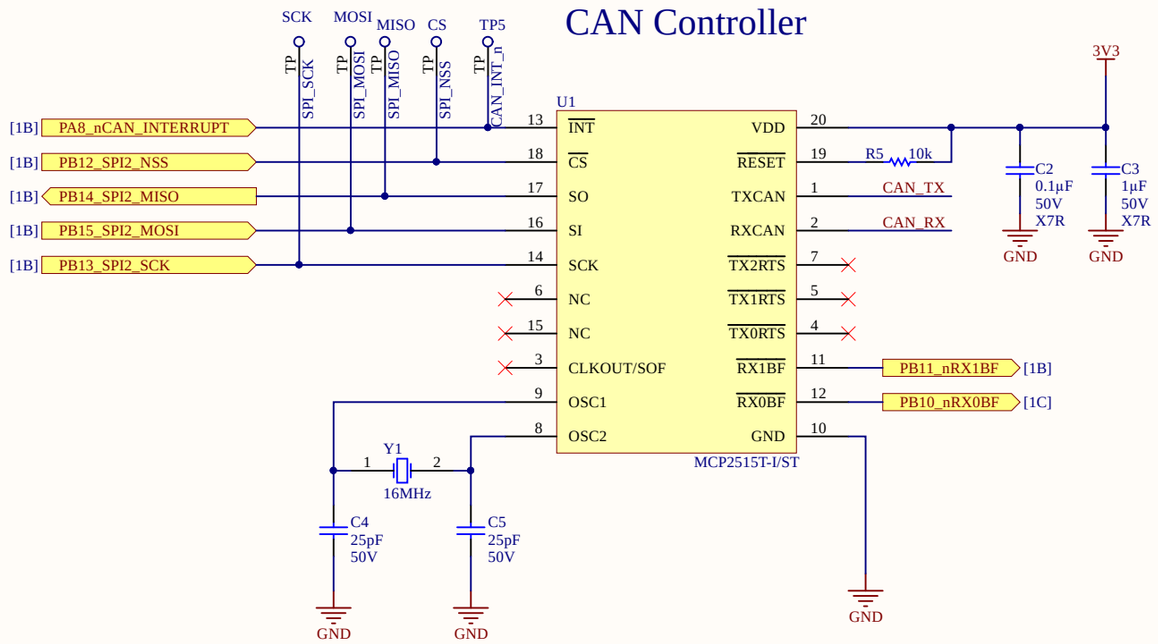
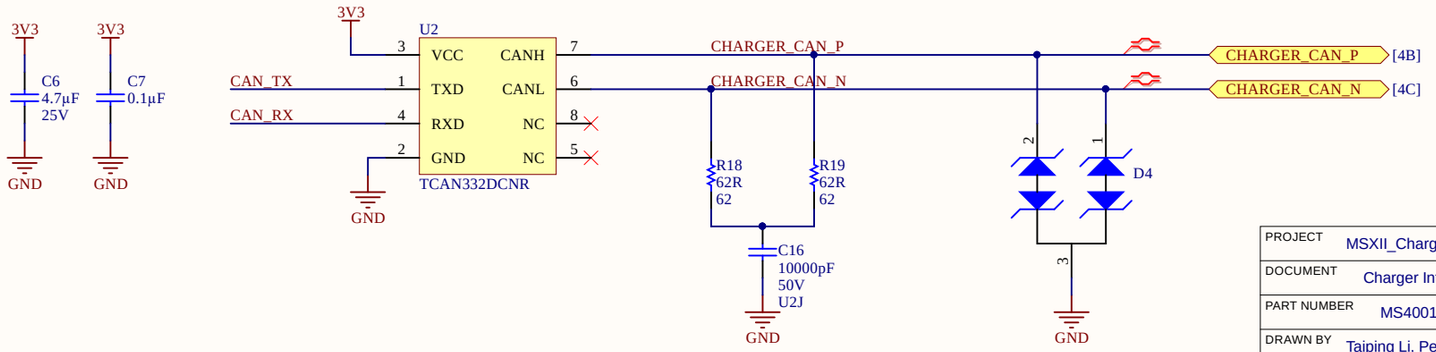
University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com

CAN Controller



CAN Transceiver



PROJECT	MSXII_ChargerInterface.PrjPcb		
DOCUMENT	Charger Interface - CAN		
PART NUMBER	MS40013-03	VARIANT	[No Variations]
DRAWN BY	Taiping Li, Peiliang Guo	REVISION	3.0
LAST MODIFIED	2019-03-17	SHEET	2 OF 3

MIDNIGHT SUN

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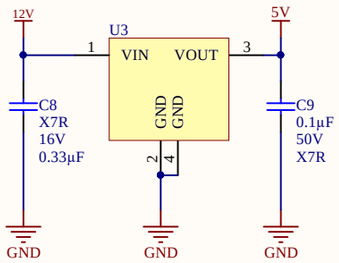
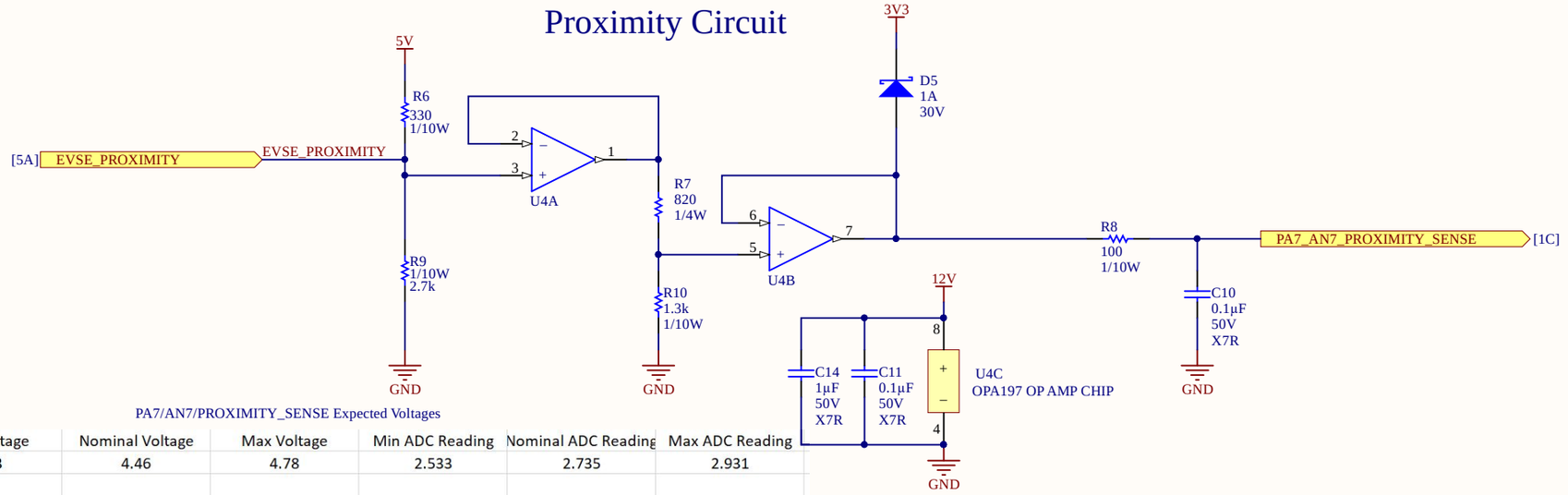
University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com

5V Power Supply



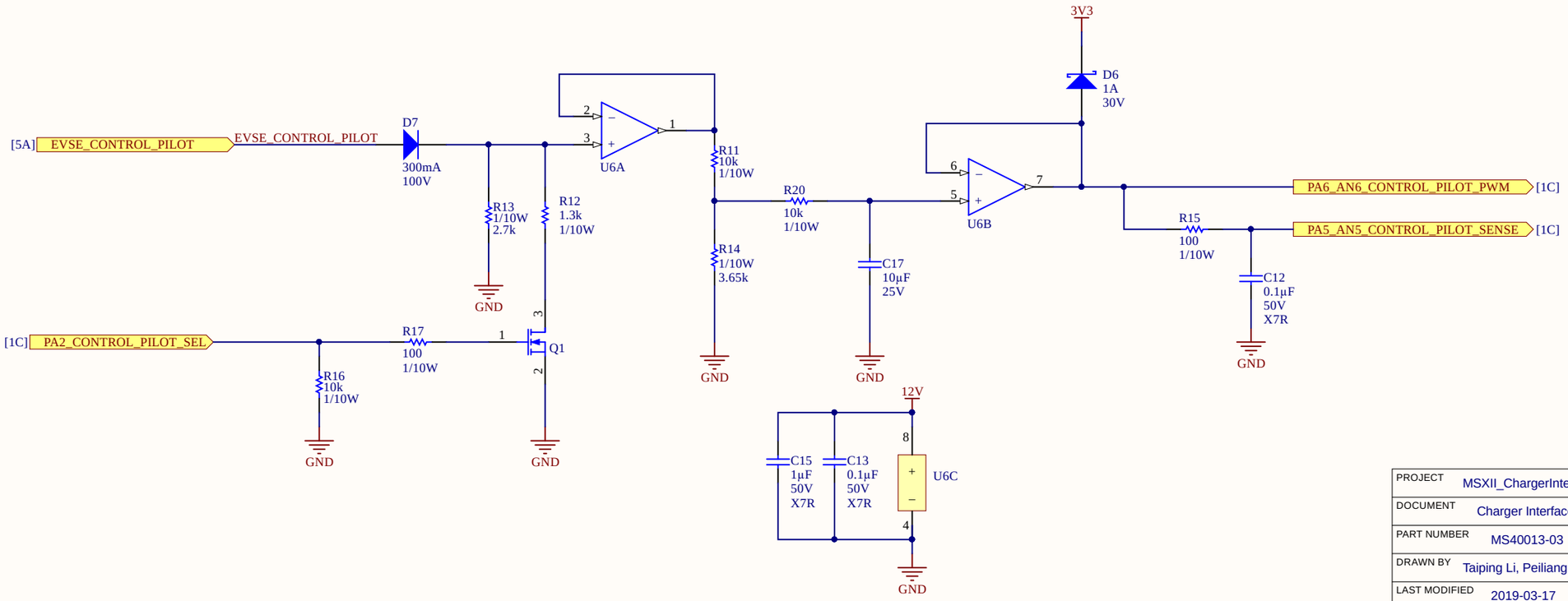
Proximity Circuit



PA7/AN7/PROXIMITY_SENSE Expected Voltages

Description	Min Voltage	Nominal Voltage	Max Voltage	Min ADC Reading	Nominal ADC Reading	Max ADC Reading
EVSE Not Connected	4.13	4.46	4.78	2.533	2.735	2.931
EVSE Connector plugged in, button is peleased	1.23	1.53	1.82	0.754	0.938	1.116
EVSE Connector is plugged In, button is pressed	2.38	2.77	3.16	1.459	1.699	1.938

Control Pilot Circuit



PROJECT	MSXII_ChargerInterface.PrjPcb		
DOCUMENT	Charger Interface - J1772 Interface		
PART NUMBER	MS40013-03	VARIANT	[No Variations]
DRAWN BY	Taiping Li, Peiliang Guo	REVISION	3.0
LAST MODIFIED	2019-03-17	SHEET	3 OF 3

MIDNIGHT SUN

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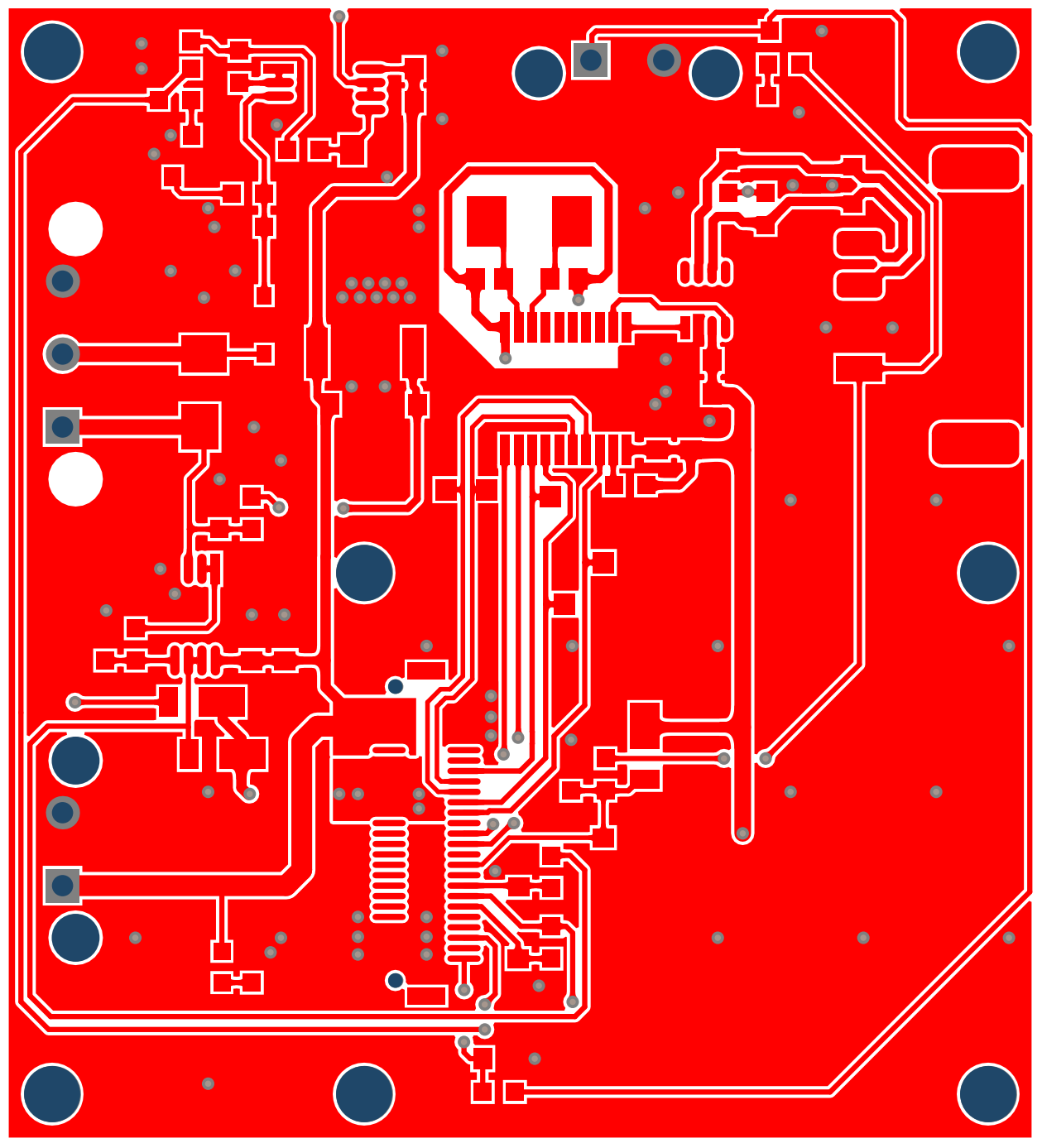
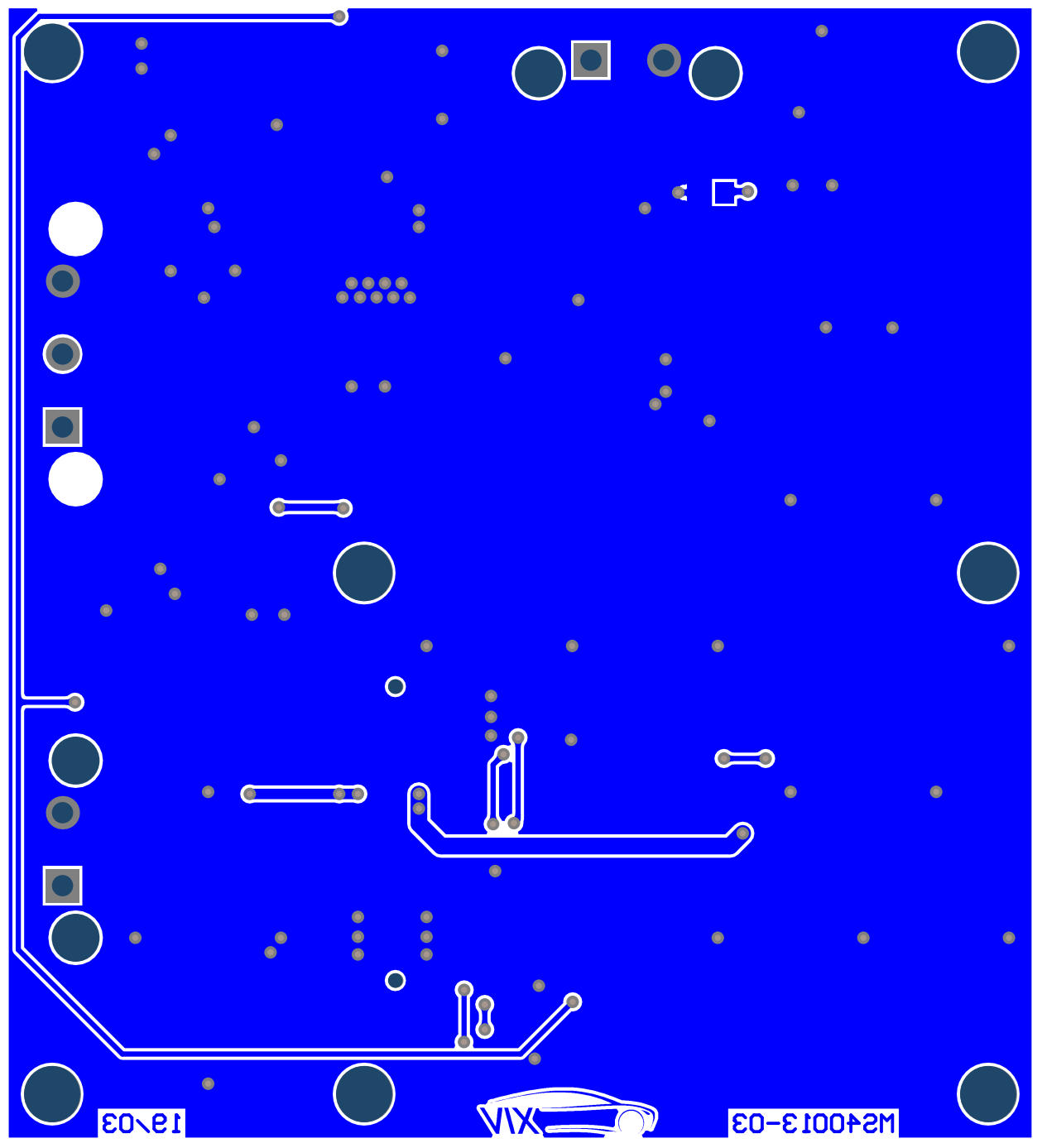
University of Waterloo
(519) 888-4567 x32978
hardware@uwmidsun.com

Bill of Materials

Project:	MSXII_ChargerInterface.PrjPcb
Revision:	3
Project Lead:	Taiping Li, Peiliang Guo
Generated On:	2019-03-17 17:35
Production Quantity:	1
Currency	CAD
Total Parts Count:	61

LibRef	Designator	Manufacturer 1	Manufacturer Part Number 1	Supplier 1	Supplier Part Number 1	Supplier Unit Price 1	Quantity	Supplier Subtotal 1
CAP CER 0.1UF 50V 10% X7R 0603	C1, C2, C7, C9, C10, C11, C12, C13, C18	Kyocera AVX	06035C-104KAT2A	Digi-Key	478-5052-1-ND	0.21338	9	$ 1.92
CAP CER 1UF 50V 10% X7R 0603	C3, C14, C15	Taiyo Yuden	UMK107AB7105KA-T	Digi-Key	587-3247-1-ND	0.37342	3	$ 1.12
CAP CER 25PF 50V ±5% C0G/NP0 0603	C4, C5	Samsung	CL10C250JB8NNNC	Digi-Key	1276-2244-1-ND	0.13336	2	$ 0.27
CAP CER 4.7UF 25V 10% X5R 0603	C6	Murata	GRM188R61E475KE11D	Digi-Key	490-7203-1-ND	0.49345	1	$ 0.49
CAP CER 0.33UF 16V 10% X7R 0603	C8	KEMET	C0603C334K4RACTU	Digi-Key	399-4916-1-ND	0.48011	1	$ 0.48
CAP CER 10nF 50V 5% X7R 0603	C16	KEMET	C0603C103J5JACTU	Digi-Key	399-13384-1-ND	0.48011	1	$ 0.48
CAP CER 10uF 25V 10% X5R 0805	C17	Murata	GRM21BR61E106KA73L	Digi-Key	490-5523-1-ND	0.57347	1	$ 0.57
DIODE TVS 12VWM 19.6VC DO-214AA (SMB)	D1	Vishay Semiconductors	SMBJ12CD-M3/H	Digi-Key	SMBJ12CD-M3/HGICT-ND	0.66682	1	$ 0.67
DIODE TVS 5VWM 9.1VC DO-214AA (SMB)	D2	Vishay Semiconductors	SMBJ5.0D-M3/H	Digi-Key	SMBJ5.0D-M3/HGICT-ND	0.49345	1	$ 0.49
DIODE SCHOTTKY 30V 1A POWERDI123	D3, D5, D6	Diodes	DFLS130L-7	Digi-Key	DFLS130LDICT-ND	0.66682	3	$ 2.00
DIODE TVS 24VWM 70VC SOT23	D4	Nexperia	PESD1CAN,215	Digi-Key	1727-3817-1-ND	0.65349	1	$ 0.65
DIODE GEN PURP 100V 300MA SOD123	D7	Diodes Zetex	1N4148WQ-7-F	Digi-Key	1N4148WQ-7-FDICT-ND	0.2934	1	$ 0.29
LED GREEN CLEAR 2V 0603	LED1	Wurth Electronics	150060VS75000	Digi-Key	732-4980-1-ND	0.18671	1	$ 0.19
LED RED CLEAR 2V 0603	LED2	Wurth Electronics	150060RS75000	Digi-Key	732-4978-1-ND	0.18671	1	$ 0.19
CONN 2POS ULTRA-FIT 0.138"	P1	Molex	1722861302	Digi-Key	WM11673-ND	1.95	1	$ 1.95
CONN 3POS ULTRA-FIT 0.138"	P2	Molex	1722871103	Digi-Key	WM11702-ND	1.09	1	$ 1.09
CONN 50POS Bergstak Plug 0.02"	P3	Amphenol FCI	10132797-055100LF	Digi-Key	609-5226-1-ND	1.87	1	$ 1.87
CONN 4POS DURA-CLIK 0.079"	P4	Molex	560020-0420	Digi-Key	WM10864CT-ND	2.21	1	$ 2.21
CONN 2POS ULTRA-FIT NATURAL COLOR 0.138	P5	Molex	1722872102	Digi-Key	WM11722-ND	1.15	1	$ 1.15
MOSFET N-CH 30V 6.2A 0.9W SOT-23	Q1	Diodes	DMN3023L-7	Digi-Key	DMN3023L-7DICT-ND	0.60014	1	$ 0.60
RES 10K OHM 1% 1/10W 0603	R1, R2, R3, R5, R11, R16, R20, R22	Yageo Phycomp	RC0603FR-0710KL	Digi-Key	311-10.0KHRCT-ND	0.13336	8	$ 1.07
RES 3.65K OHM 0.1% 1/10W 0603	R4, R14	Panasonic	ERA3AEB3651V	Digi-Key	P3.65KDBCT-ND	0.46678	2	$ 0.93
RES 330 OHM 1% 1/10W 0603	R6	TE Connectivity	CRGCQ0603F330R	Digi-Key	A129682TR-ND		1	
RES 820 OHM 5% 1/4W 0603	R7	Rohm	ESR03EZPJ821	Digi-Key	RHM820DCT-ND	0.13336	1	$ 0.13
RES 100 OHM 1% 1/10W 0603	R8, R15, R17, R21	Yageo	RC0603FR-07100RL	Digi-Key	311-100HRCT-ND	0.13336	4	$ 0.53
RES 2.7K OHM 1% 1/10W 0603	R9, R13	TE Connectivity	3-2176339-0	Digi-Key	A129693TR-ND		2	
RES 1.3K OHM 1% 1/10W 0603	R10, R12	Yageo	RC0603FR-071K3L	Digi-Key	311-1.30KHRCT-ND	0.13336	2	$ 0.27
RES 62 OHM 0.1% 1/10W 0603	R18, R19	Panasonic	ERA3AEB620V	Digi-Key	P62DBCT-ND	0.46678	2	$ 0.93
CAN SPI CONTROLLER MCP2515T-I/ST 20-TSS	U1	Microchip	MCP2515T-I/ST	Digi-Key	MCP2515T-I/STCT-ND	2.73	1	$ 2.73
IC CAN Tranceiver TCAN332DR	U2	Texas Instruments	TCAN332DCNR	Digi-Key	296-47355-1-ND	3.03	1	$ 3.03
IC REG LDO 5V 0.5A SOT223	U3	Texas Instruments	UA78M05IDCYR	Digi-Key	296-17616-1-ND	0.85354	1	$ 0.85
IC OP AMP DUAL GP RR 10MHZ 8-VSSOP	U4, U6	Texas Instruments	OPA2197IDGKR	Digi-Key	296-47349-1-ND	3.21	2	$ 6.43
CRYSTAL 16 MHz 18PF 2-SMD	Y1	Abracon	ABM3-16.000MHZ-D2Y-T	Digi-Key	535-10638-1-ND	0.92022	1	$ 0.92
							Total:	$ 36.52




19/03
MS4001 3-03

Design Rules Verification Report

Filename : C:\Users\Taiping\Documents\Midnight Sun\hardware\MSXII_ChargerInterface\Charger Interface.PcbDoc

Warnings 0
Rule Violations 109

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=2.54mm) (Preferred=0.25mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm) (Air Gap=0.254mm)	0
Minimum Annular Ring (Minimum=0.15mm) (All)	0
Hole Size Constraint (Min=0.3mm) (Max=6.3mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)	36
Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)	24
Silk to Silk (Clearance=0.254mm) (OnLayer('Bottom Overlay')),(OnLayer('Bottom Overlay'))	0
Silk to Silk (Clearance=0.254mm) (OnLayer('Top Overlay')),(OnLayer('Top Overlay'))	29
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	20
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	109

Minimum Solder Mask Sliver (Gap=0.3mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C10-1(24.925mm,12.425mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C1-1(29mm,14.8mm) on Top Layer And Pad C1-2(29mm,13.45mm) on Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C11-1(12.1mm,23.3mm) on Top Layer And Pad C11-2(12.1mm,24.65mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C12-1(24.9mm,9mm) on Top Layer And Pad C12-2(24.9mm,7.65mm) on Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C13-1(19.9mm,51.7mm) on Top Layer And Pad C13-2(21.25mm,51.7mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C14-1(13.7mm,23.3mm) on Top Layer And Pad C14-2(13.7mm,24.65mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C15-1(19.9mm,50.1mm) on Top Layer And Pad C15-2(21.25mm,50.1mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C16-1(34.825mm,45.75mm) on Bottom Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C18-1(23.2mm,4.2mm) on Top Layer And Pad C18-2(24.55mm,4.2mm) on Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C2-1(31.6mm,33.4mm) on Top Layer And Pad C2-2(31.6mm,34.75mm) on Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C3-1(33.2mm,33.4mm) on Top Layer And Pad C3-2(33.2mm,34.75mm) on Top
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.3mm) Between Pad C3-2(33.2mm,34.75mm) on Top Layer And Pad C6-1(32.888mm,36.1mm) on
Minimum Solder Mask Sliver Constraint: (0.248mm < 0.3mm) Between Pad C3-2(33.2mm,34.75mm) on Top Layer And Pad C6-2(34.238mm,36.1mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C4-1(24.2mm,41.6mm) on Top Layer And Pad C4-2(22.85mm,41.6mm) on Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C5-1(26.45mm,41.6mm) on Top Layer And Pad C5-2(27.8mm,41.6mm) on Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C6-1(32.888mm,36.1mm) on Top Layer And Pad C6-2(34.238mm,36.1mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C7-1(32.888mm,37.7mm) on Top Layer And Pad C7-2(34.238mm,37.7mm) on
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C8-1(15.85mm,35.6mm) on Top Layer And Pad C8-2(17.2mm,35.6mm) on Top
Minimum Solder Mask Sliver Constraint: (0.298mm < 0.3mm) Between Pad C9-1(20.05mm,35.562mm) on Top Layer And Pad C9-2(18.7mm,35.562mm) on
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P3-(19mm,22.05mm) on Multi-Layer And Pad P3-(20.5mm,22.8mm) on Top
Minimum Solder Mask Sliver Constraint: (0.105mm < 0.3mm) Between Pad P3-(19mm,7.95mm) on Multi-Layer And Pad P3-(20.5mm,7.2mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.3mm) Between Pad R14-1(9.175mm,53mm) on Top Layer And Pad R16-1(9.175mm,51.7mm) on
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.3mm) Between Pad R14-2(7.625mm,53mm) on Top Layer And Pad R16-2(7.625mm,51.7mm) on
Minimum Solder Mask Sliver Constraint: (0.049mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region (0 hole(s)) Bottom Solder [Bottom
Minimum Solder Mask Sliver Constraint: (0.106mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region (0 hole(s)) Bottom Solder [Bottom
Minimum Solder Mask Sliver Constraint: (0.228mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region (0 hole(s)) Bottom Solder [Bottom
Minimum Solder Mask Sliver Constraint: (0.231mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region (0 hole(s)) Bottom Solder [Bottom
Minimum Solder Mask Sliver Constraint: (0.237mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region (0 hole(s)) Bottom Solder [Bottom
Minimum Solder Mask Sliver Constraint: (0.285mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region (0 hole(s)) Bottom Solder [Bottom
Minimum Solder Mask Sliver Constraint: (0.287mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region (0 hole(s)) Bottom Solder [Bottom
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Minimum Solder Mask Sliver Constraint: (0.299mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region (0 hole(s)) Bottom Solder [Bottom
Minimum Solder Mask Sliver Constraint: (0.299mm < 0.3mm) Between Region (0 hole(s)) Bottom Solder And Region (0 hole(s)) Bottom Solder [Bottom
Minimum Solder Mask Sliver Constraint: (0.007mm < 0.3mm) Between Via (16.452mm,40.725mm) from Top Layer to Bottom Layer And Via
Minimum Solder Mask Sliver Constraint: (0.044mm < 0.3mm) Between Via (16.452mm,40.725mm) from Top Layer to Bottom Layer And Via

Silk To Solder Mask (Clearance=0.178mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.09mm < 0.178mm) Between Arc (41mm,44.25mm) on Top Overlay And Pad P4-4(41.309mm,43.31mm) on
Silk To Solder Mask Clearance Constraint: (0.092mm < 0.178mm) Between Pad C11-2(12.1mm,24.65mm) on Top Layer And Text "C11" (11.75mm,27mm)
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad C1-2(29mm,13.45mm) on Top Layer And Text "C10" (27.45mm,14mm) on
Silk To Solder Mask Clearance Constraint: (0.125mm < 0.178mm) Between Pad C12-2(24.9mm,7.65mm) on Top Layer And Text "C12" (24.5mm,7mm) on
Silk To Solder Mask Clearance Constraint: (0.076mm < 0.178mm) Between Pad C14-2(13.7mm,24.65mm) on Top Layer And Text "C14"
Silk To Solder Mask Clearance Constraint: (0.165mm < 0.178mm) Between Pad C5-2(27.8mm,41.6mm) on Top Layer And Text "C5" (28.49mm,41.1mm)
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad P3-1(22.3mm,21mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.178mm) Between Pad P3-25(22.3mm,9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad P3-26(18.7mm,9mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.166mm < 0.178mm) Between Pad P3-50(18.7mm,21mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.119mm < 0.178mm) Between Pad P4-7(46.889mm,33.71mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.16mm < 0.178mm) Between Pad P4-7(46.889mm,46.91mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q1-1(9.2mm,48.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.058mm < 0.178mm) Between Pad Q1-2(7.4mm,48.5mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.05mm < 0.178mm) Between Pad R18-1(36.8mm,44.2mm) on Top Layer And Text "CANL"
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-1(32.925mm,39.275mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U2-2(33.575mm,39.275mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U2-3(34.225mm,39.275mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.177mm < 0.178mm) Between Pad U2-4(34.875mm,39.275mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-5(34.875mm,41.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-6(34.225mm,41.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-7(33.575mm,41.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.178mm) Between Pad U2-8(32.925mm,41.925mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.162mm < 0.178mm) Between Pad U3-4(17.55mm,43.868mm) on Top Layer And Text "R13"

Silk to Silk (Clearance=0.254mm) (OnLayer('Top Overlay')),(OnLayer('Top Overlay'))
Silk To Silk Clearance Constraint: (0.234mm < 0.254mm) Between Arc (30.9mm,39.3mm) on Top Overlay And Text "U1" (31mm,37.95mm) on Top Overlay
Silk To Silk Clearance Constraint: (0.243mm < 0.254mm) Between Arc (32.15mm,39.275mm) on Top Overlay And Text "U1" (31mm,37.95mm) on Top
Silk To Silk Clearance Constraint: (0.119mm < 0.254mm) Between Text "C10" (27.45mm,14mm) on Top Overlay And Text "R8" (28.5mm,12.5mm) on Top
Silk To Silk Clearance Constraint: (0.204mm < 0.254mm) Between Text "C13" (22.25mm,51.265mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.204mm < 0.254mm) Between Text "C15" (22.25mm,49.75mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "C2" (34.4mm,35.25mm) on Top Overlay And Text "C3" (35.6mm,35.25mm) on Top
Silk To Silk Clearance Constraint: (0.168mm < 0.254mm) Between Text "CP" (6.3mm,38.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.148mm < 0.254mm) Between Text "CS" (30mm,27.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.25mm < 0.254mm) Between Text "CURRENT SENSE" (25.1mm,48mm) on Top Overlay And Text "R19"
Silk To Silk Clearance Constraint: (0.168mm < 0.254mm) Between Text "CURRENT SENSE" (25.1mm,48mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.125mm < 0.254mm) Between Text "D1" (9.4mm,43.6mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.215mm < 0.254mm) Between Text "D3" (30.5mm,23.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.229mm < 0.254mm) Between Text "J1772

INLET" (1.4mm,28mm) on Top Overlay And Track (0.38mm,30.7mm)(5.93mm,30.7mm) on Top Overlay Silk Text to Silk Clea

Silk to Silk (Clearance=0.254mm) (OnLayer('Top Overlay')),(OnLayer('Top Overlay'))
Silk To Silk Clearance Constraint: (0.175mm < 0.254mm) Between Text "MOSI" (22.75mm,35.25mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.22mm < 0.254mm) Between Text "MOSI" (22.75mm,35.25mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.169mm < 0.254mm) Between Text "P1" (0.6mm,20.2mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.168mm < 0.254mm) Between Text "P1" (0.6mm,20.2mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.108mm < 0.254mm) Between Text "P2" (0.3mm,45.6mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "P2" (0.3mm,45.6mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.21mm < 0.254mm) Between Text "P3" (19.8mm,24.2mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.254mm < 0.254mm) Between Text "POWER" (1.5mm,7.5mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.168mm < 0.254mm) Between Text "PROX" (6.3mm,36mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "Q1" (5.63mm,46.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.098mm < 0.254mm) Between Text "Q1" (5.63mm,46.7mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.15mm < 0.254mm) Between Text "R10" (2.3mm,25.2mm) on Top Overlay And Text "R7" (3.4mm,25.2mm) on Top
Silk To Silk Clearance Constraint: (0.225mm < 0.254mm) Between Text "TP5" (26mm,29.5mm) on Top Overlay And Track (15mm,30mm)(50mm,30mm) on
Silk To Silk Clearance Constraint: (0.086mm < 0.254mm) Between Text "U2" (30.9mm,41.3mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.086mm < 0.254mm) Between Text "U2" (30.9mm,41.3mm) on Top Overlay And Track
Silk To Silk Clearance Constraint: (0.175mm < 0.254mm) Between Text "U6" (15mm,52.6mm) on Top Overlay And Track

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (0.145mm < 0.406mm) Between Board Edge And Text "ELCON CHARGER" (39.575mm,31.6mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.15mm < 0.406mm) Between Board Edge And Text "P2" (0.3mm,45.6mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.25mm < 0.406mm) Between Board Edge And Text "P5" (22.8mm,53.8mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.253mm < 0.406mm) Between Board Edge And Track (0.38mm,30.7mm)(0.38mm,34.4mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.253mm < 0.406mm) Between Board Edge And Track (0.38mm,30.7mm)(5.93mm,30.7mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.253mm < 0.406mm) Between Board Edge And Track (0.38mm,34.4mm)(0.38mm,41.625mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.253mm < 0.406mm) Between Board Edge And Track (0.38mm,41.625mm)(0.38mm,45.3mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.253mm < 0.406mm) Between Board Edge And Track (0.38mm,45.3mm)(5.93mm,45.3mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (15mm,0mm)(15mm,14.4mm) on Top Overlay
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (15mm,30mm)(50mm,30mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.403mm < 0.406mm) Between Board Edge And Track (24.655mm,49.17mm)(24.655mm,54.47mm) on Top
Board Outline Clearance(Outline Edge): (0.403mm < 0.406mm) Between Board Edge And Track (24.655mm,54.47mm)(32.9mm,54.47mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.403mm < 0.406mm) Between Board Edge And Track (31.9mm,54.47mm)(35.73mm,54.47mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.403mm < 0.406mm) Between Board Edge And Track (35.73mm,49.17mm)(35.73mm,54.47mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Track (39.9mm,2.6mm)(49.5mm,12.2mm) on Top Layer
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (43.5mm,0mm)(50mm,0mm) on Top Overlay
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Track (49.5mm,12.2mm)(49.5mm,48.5mm) on Top Layer
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (49.919mm,33.035mm)(49.919mm,47.635mm) on Top
Board Outline Clearance(Outline Edge): (0.375mm < 0.406mm) Between Board Edge And Track (49mm,49mm)(49.5mm,48.5mm) on Top Layer
Board Outline Clearance(Outline Edge): (Collision < 0.406mm) Between Board Edge And Track (50mm,0mm)(50mm,30mm) on Top Overlay

Electrical Rules Check Report

Class	Document	Message
Warning	Charger Interface - J1772 Interface.SchDoc	Net NetC17_1 has no driving source (Pin C17-1,Pin R20-2,Pin U6-5)
Warning	Charger Interface - J1772 Interface.SchDoc	Net NetD7_2 has no driving source (Pin D7-2,Pin R12-1,Pin R13-1,Pin U6-3)
Warning	Charger Interface - J1772 Interface.SchDoc	Net NetR7_2 has no driving source (Pin R7-2,Pin R10-1,Pin U4-5)
Error	Charger Interface - CAN.SchDoc	Net PA9 has only one pin (Pin P3-6)
Error	Charger Interface - CAN.SchDoc	Net PA10 has only one pin (Pin P3-5)
Error	Charger Interface - CAN.SchDoc	Net PB8 has only one pin (Pin P3-32)
Error	Charger Interface - CAN.SchDoc	Net PB9 has only one pin (Pin P3-31)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PA2/CONTROL_PILOT_SEL has multiple names (Net Label PA2/CONTROL_PILOT_SEL,Port PA2_CONTROL_PILOT_SEL)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PA2/CONTROL_PILOT_SEL has multiple names (Net Label PA2/CONTROL_PILOT_SEL,Port PA2_CONTROL_PILOT_SEL,Port PA2_CONTROL_PILOT_SEL)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PA5/AN5/CONTROL_PILOT_PWM has multiple names (Net Label PA5/AN5/CONTROL_PILOT_PWM,Port PA5_AN5_CONTROL_PILOT_SENSE)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PA5/AN5/CONTROL_PILOT_PWM has multiple names (Net Label PA5/AN5/CONTROL_PILOT_PWM,Port PA5_AN5_CONTROL_PILOT_SENSE,Port PA5_AN5_CONTROL_PILOT_SENSE)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PA6/AN6 has multiple names (Net Label PA6/AN6,Port PA6_AN6_CONTROL_PILOT_PWM)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PA6/AN6 has multiple names (Net Label PA6/AN6,Port PA6_AN6_CONTROL_PILOT_PWM,Port PA6_AN6_CONTROL_PILOT_PWM)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PA7/AN7/PROXIMITY_SENSE has multiple names (Net Label PA7/AN7/PROXIMITY_SENSE,Port PA7_AN7_PROXIMITY_SENSE)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PA7/AN7/PROXIMITY_SENSE has multiple names (Net Label PA7/AN7/PROXIMITY_SENSE,Port PA7_AN7_PROXIMITY_SENSE,Port PA7_AN7_PROXIMITY_SENSE)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PA8/CAN_INT_n has multiple names (Net Label PA8/CAN_INT_n,Port PA8_nCAN_INTERRUPT)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PA8/CAN_INT_n has multiple names (Net Label PA8/CAN_INT_n,Port PA8_nCAN_INTERRUPT,Port PA8_nCAN_INTERRUPT)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PB12/SPI2_NSS has multiple names (Net Label PB12/SPI2_NSS,Port PB12_SPI2_NSS)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PB12/SPI2_NSS has multiple names (Net Label PB12/SPI2_NSS,Port PB12_SPI2_NSS,Port PB12_SPI2_NSS)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PB13/SPI2_SCK has multiple names (Net Label PB13/SPI2_SCK,Port PB13_SPI2_SCK)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PB13/SPI2_SCK has multiple names (Net Label PB13/SPI2_SCK,Port PB13_SPI2_SCK,Port PB13_SPI2_SCK)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PB14/SPI2_MISO has multiple names (Net Label PB14/SPI2_MISO,Port PB14_SPI2_MISO)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PB14/SPI2_MISO has multiple names (Net Label PB14/SPI2_MISO,Port PB14_SPI2_MISO,Port PB14_SPI2_MISO)
Warning	Charger Interface - Connectors.SchDoc	Nets Wire PB15/SPI2_MOSI has multiple names (Net Label PB15/SPI2_MOSI,Port PB15_SPI2_MOSI)
Warning	Charger Interface - CAN.SchDoc	Nets Wire PB15/SPI2_MOSI has multiple names (Net Label PB15/SPI2_MOSI,Port PB15_SPI2_MOSI,Port PB15_SPI2_MOSI)
Warning	Charger Interface - Connectors.SchDoc	Off grid Net Label PA2/CONTROL_PILOT_SEL at 3006.571mil,3800mil