

A

A

B

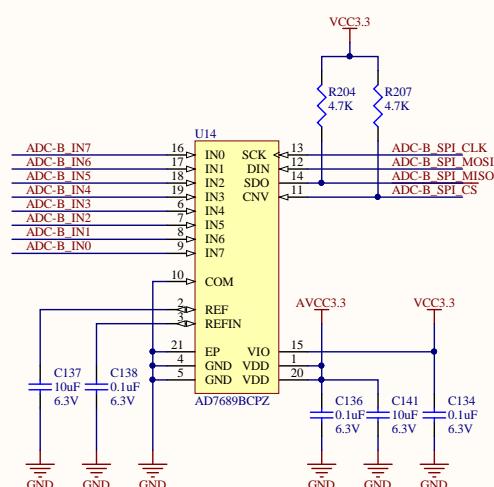
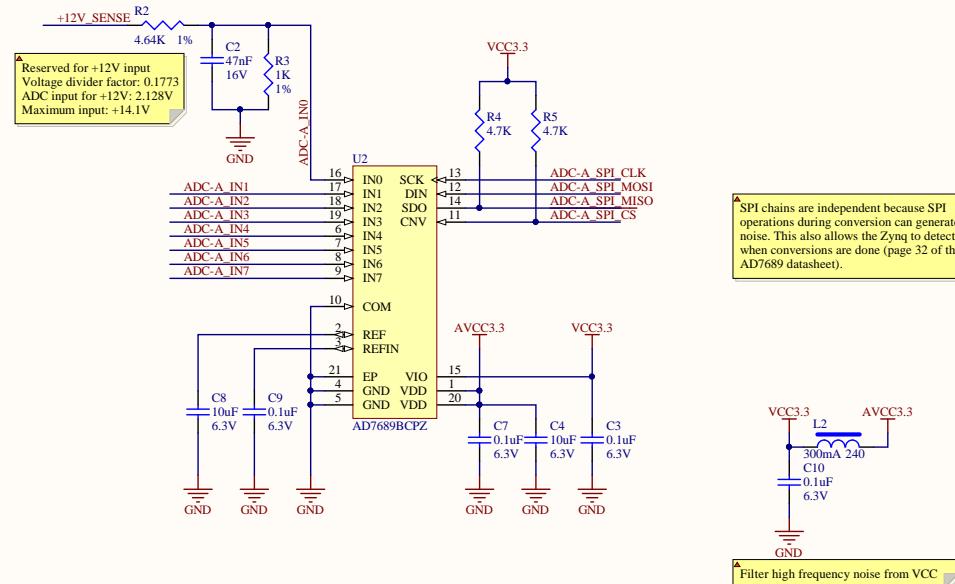
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C

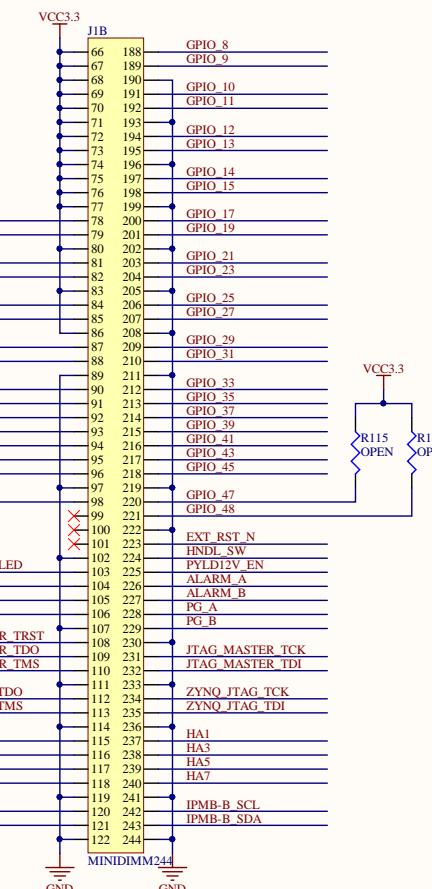
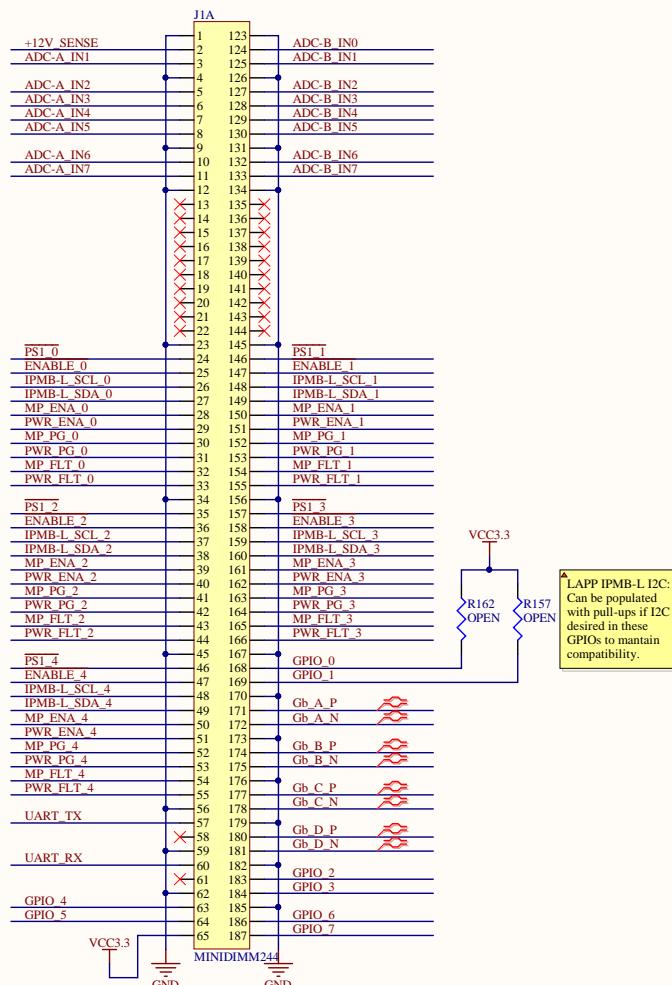
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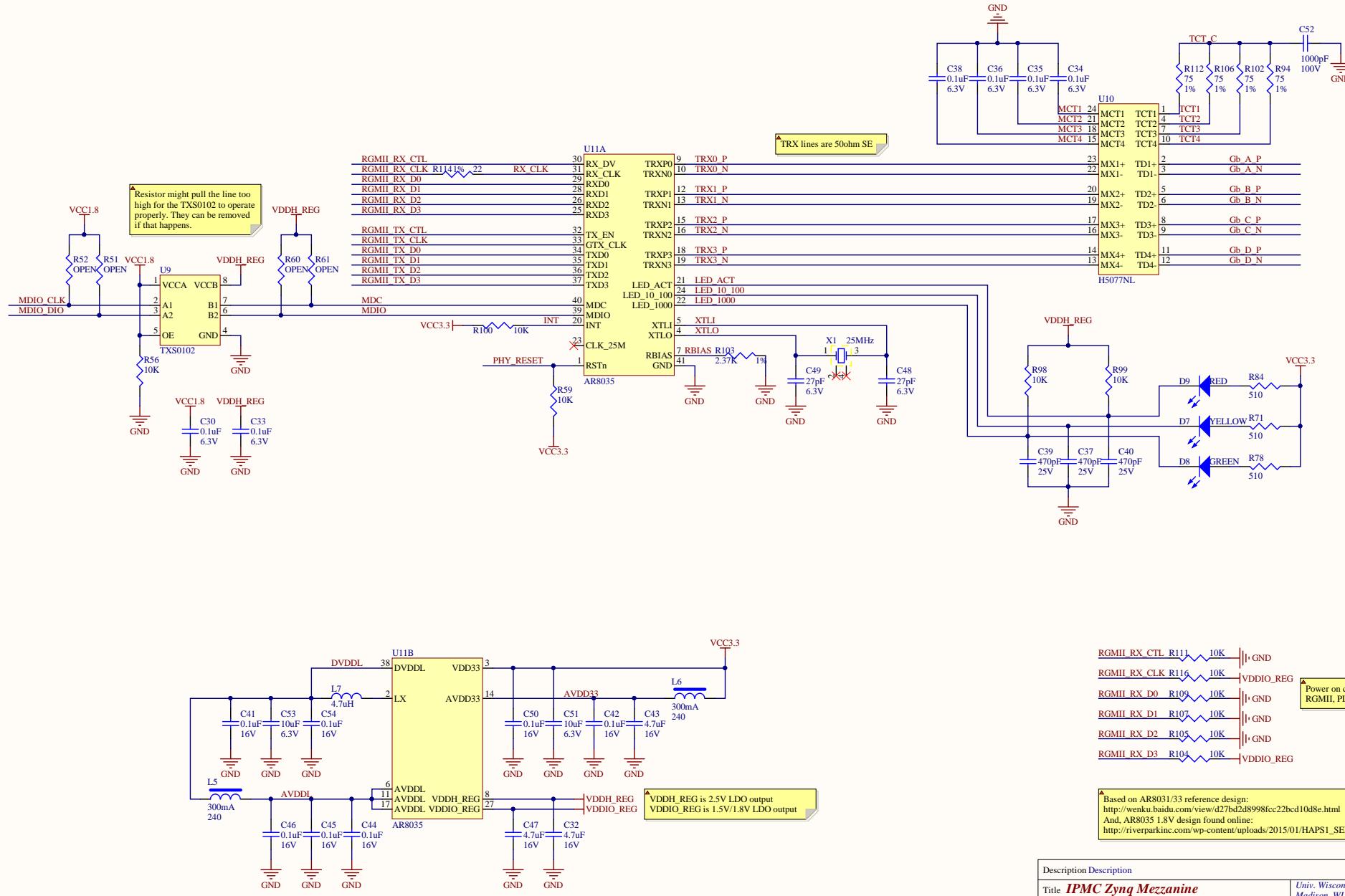
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Description	Description	Univ. Wisconsin-Madison Madison, WI 53706	Cannot open file \cernchdfs\Users\m mpv\Desktop\Uw-ma
Title	IPMC Zynq Mezzanine		
Size:	A3	Number:*	Revision revA
Date:	24/02/2017	Time: 17:20:59	Sheet * of *
File:	AnalogSense.SchDoc		Author: Vicente, M., Gorski, T., Tikalsky, J.



Description	Description	Univ. Wisconsin-Madison Madison, WI 53706	Cannot open file \cernchdfs\Users\mmpv\Desktop\Uw-ma
Title	IPMC_Zynq Mezzanine		
Size:	A3	Number:*	Revision:revA
Date:	24/02/2017	Time: 17:21:00	Sheet: * of *
File:	BoardConnector.SchDoc		Author: Vicente, M., Gorski, T., Tikalsky, J.



Description	Description
Title	IPMC Zynq Mezzanine
Size:	A3
Number:	*
Revision:	RevA
Date:	24/02/2017
Time:	17:21:00
Sheet #:	*
File:	Ethernet.SchDoc
	Author: Vicente, M., Gorski, T., Tikalsky, J.
	Univ. Wisconsin-Madison Madison, WI 53706
	Cannot open file \cern\hdf5\Users\unmpv\Desktop\UW-ma

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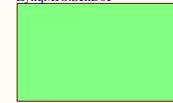
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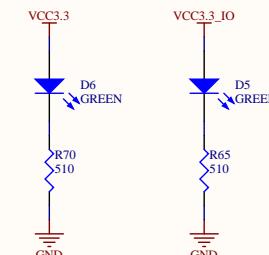
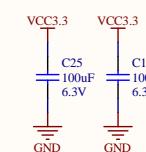
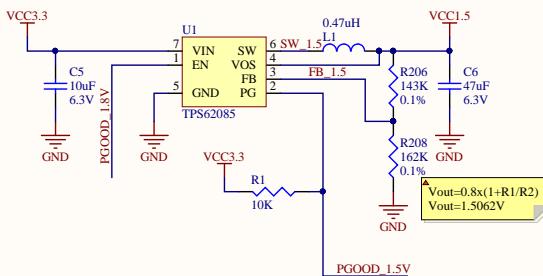
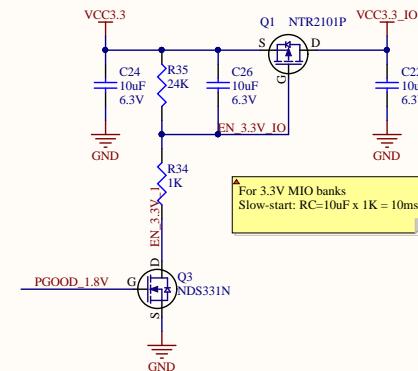
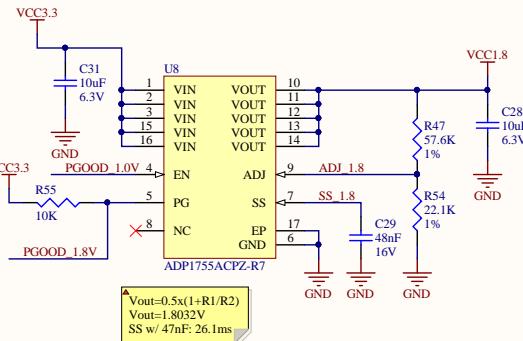
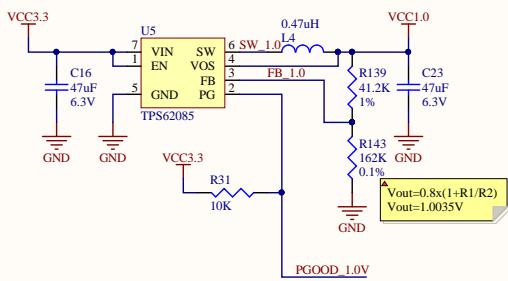
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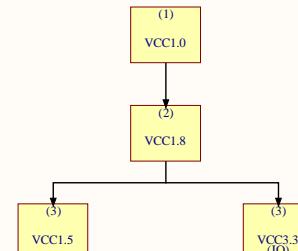
ZYNQ MIO
ZynqMIO.SchDoc



Description	Description		
Title	IPMC Zynq Mezzanine	Univ. Wisconsin-Madison Madison, WI 53706	Cannot open file \cernch\dfs\Users\mmpv\Desktop\Uw-ma
Size:	A3	Number:*	Revision revA
Date:	24/02/2017	Time: 17:21:00	Sheet* of *
File:	IPMC.SchDoc		Author: Vicente, M., Gorski, T., Tikalsky, J.



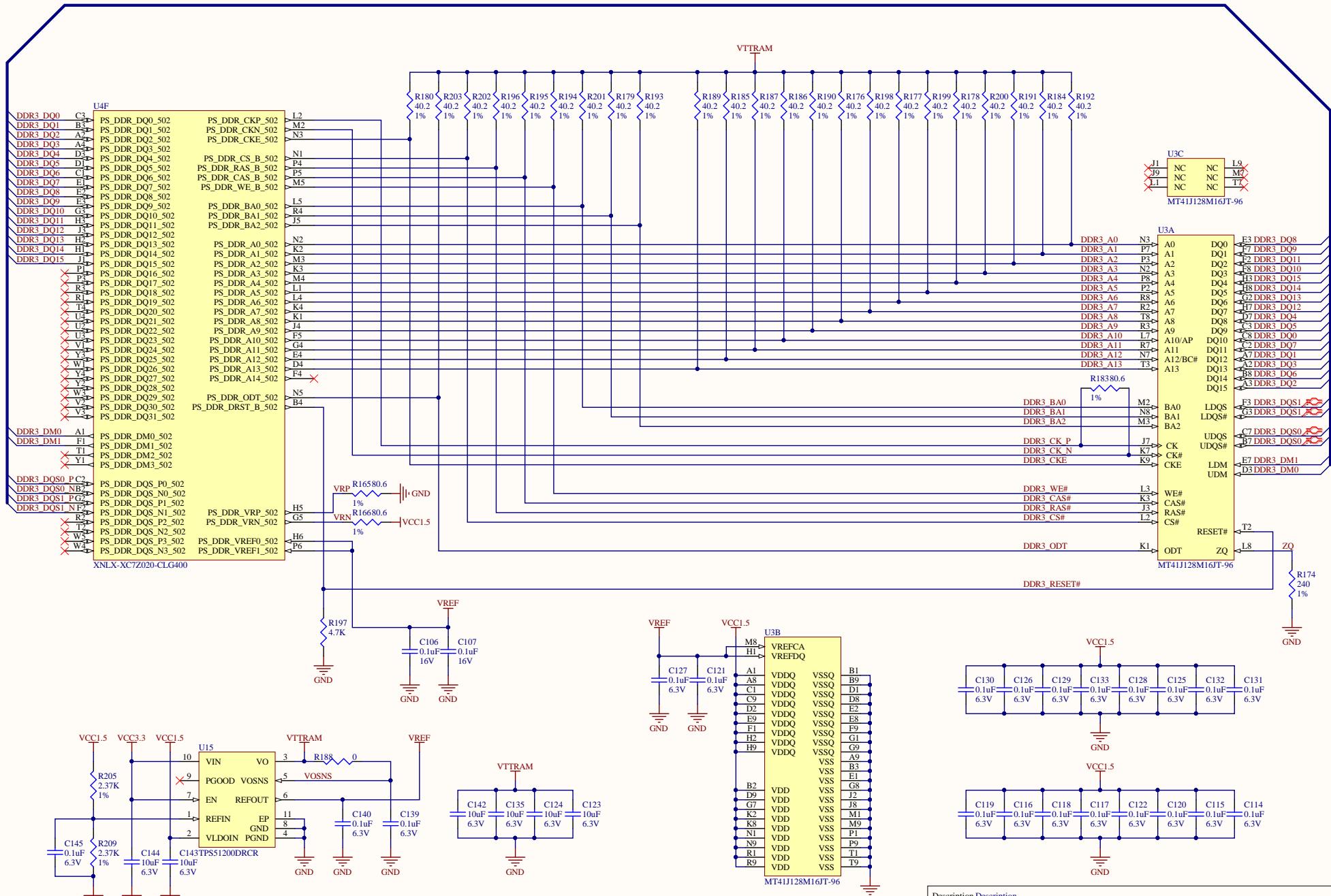
Power sequence for Zynq



► LDO converters are interchangeable with the following components:
ADP1753 (0.8A) and ADP1741 (2.0A)

Potentially, a cheaper and small option is also available: LD39050 (0.5A, no soft-start) or LD39100 (1.0A, no soft-start)

Description	Description
Title	IPMC Zyng Mezzanine
Size:	A3
Number:	* RevA
Date:	24/02/2017
Time:	17:21:00
Sheet:	* of *
File:	PowerSequence SchDoc
Author:	Vicente M. Gorski T. Tikalsky J.
	Cannot open file \\cern.ch\\dfs\\Users\\mmpv\\Desktop\\Uw-ma



Description Description

Title **IPMC Zynq Mezzanine**

Univ. Wisconsin-Madison
Madison, WI 53706

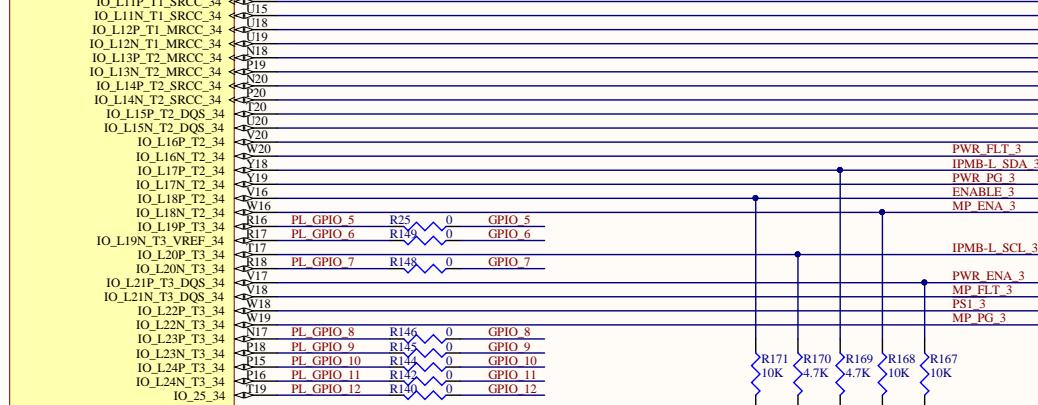
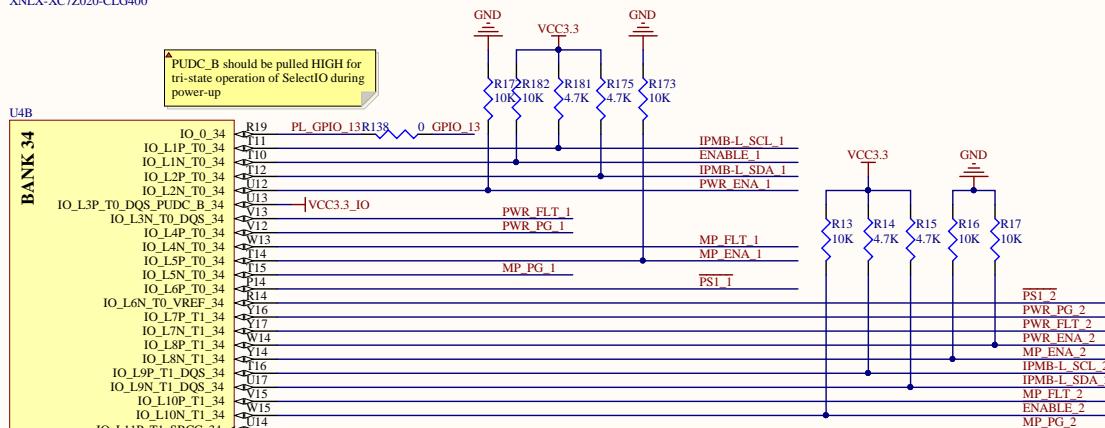
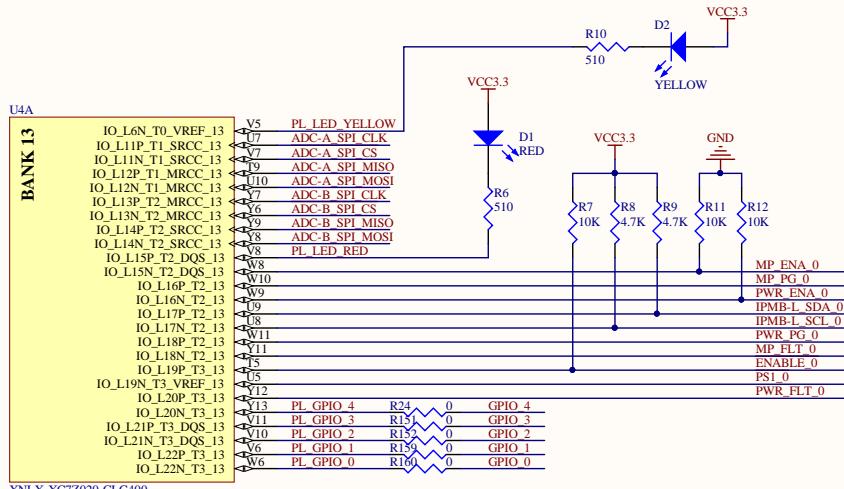
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Size: A3 Number: * Revision: revA

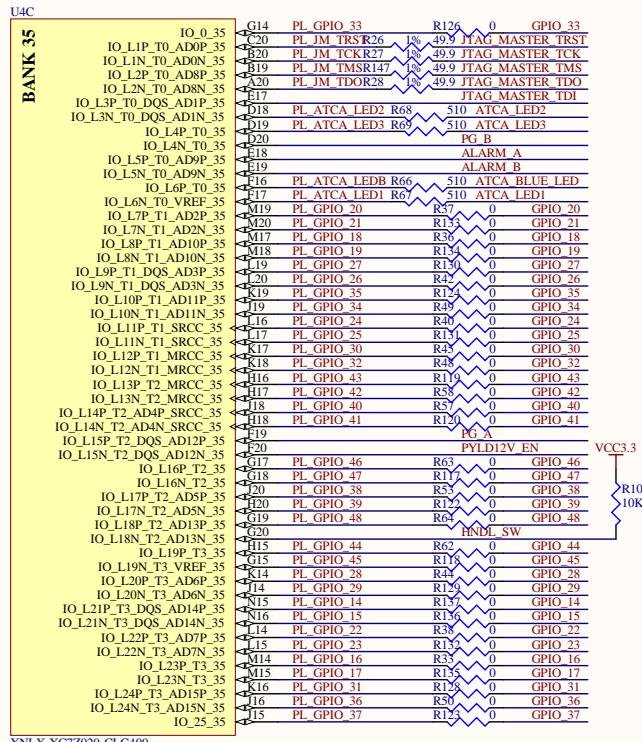
Date: 24/02/2017 Time: 17:21:01 Sheet: * of *

File: ZynqDDR.SchDoc

Author: Vicente, M., Gorski, T., Tikhalsky, J.

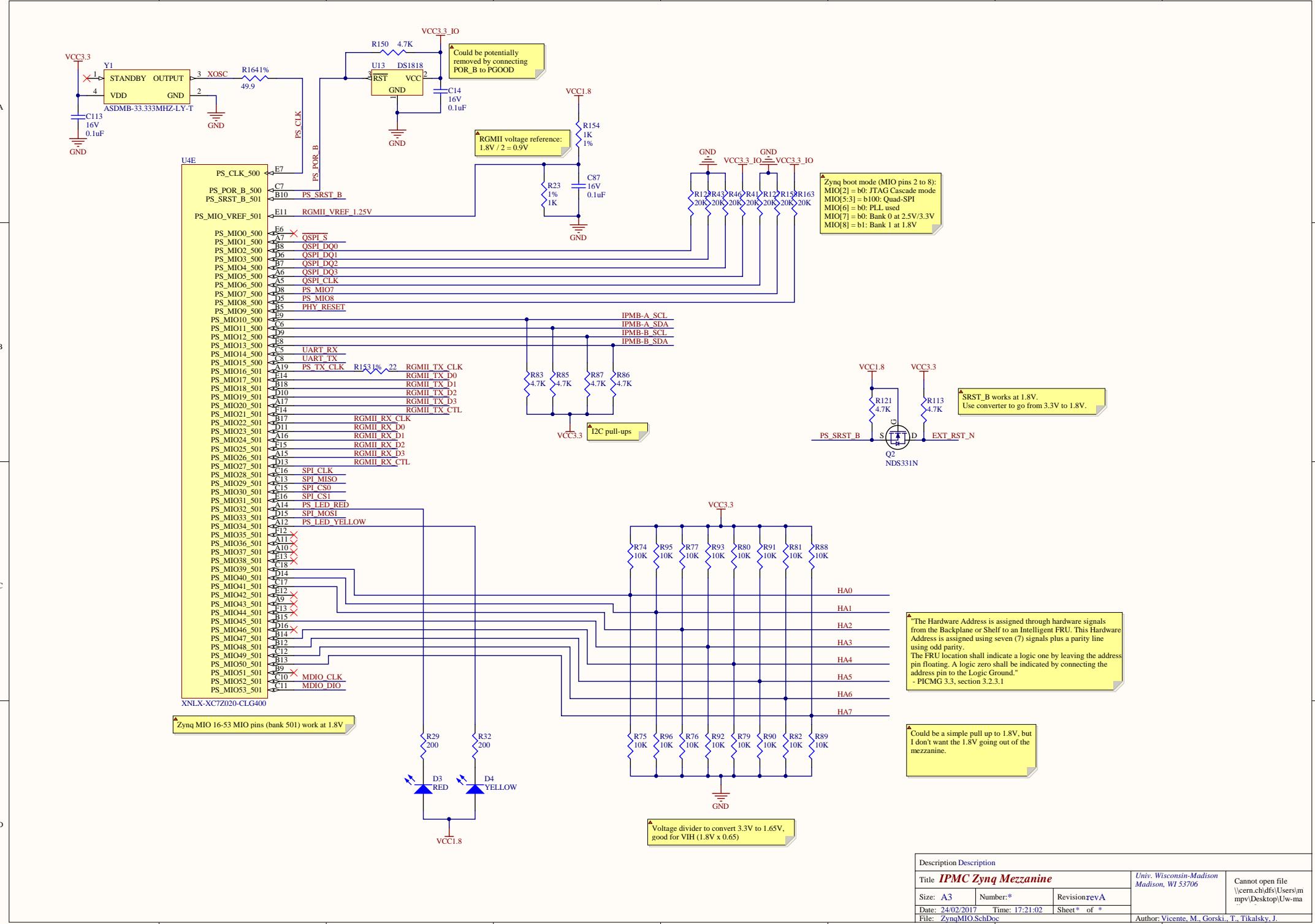


Title: IPMC Zynq Mezzanine	Univ. Wisconsin-Madison Madison, WI 53706	Cannot open file \cernch\dfs\Users\mmpv\Desktop\Uw-ma
Size: A3	Number: *	Revision revA
Date: 24/02/2017	Time: 17:21:01	Sheet * of *
File: ZynqEMIO.schDoc		Author: Vicente, M., Gorski, T., Tikalsky, J.



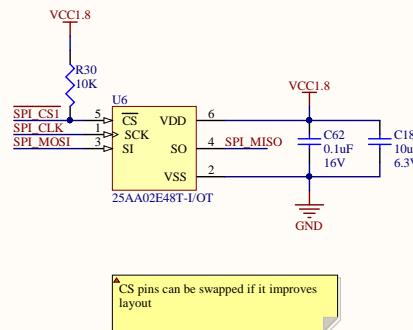
For the handle switch (HNDL_SW):
 "Provide a right-angle 3-pin header, such as a Molex 53780-0390 or equivalent, to connect to a Face Plate-mounted microswitch within 25 mm of the lower recommended Component Side 2 keepout zone shown in Figure D-2, "PICMG 3.0 R1.0 overall Handle design." Pin 1 is the COMMON connection, Pin 2 is the NC (Normally Closed) contact, and Pin 3 is the NO (Normally Open) contact. Note: Front Board vendors need to ensure that they maintain the necessary Creepage and Clearance distances to any metal connected to Shelf Ground." - PICMG 3.0 R3.0, D.1.1

Description		Description
Title IPMC Zynq Mezzanine		
Size: A3	Number: *	Revision revA
Date: 24/02/2017	Time: 17:21:01	Sheet * of *
File: ZynqEMIO_2.SchDoc		Author: Vicente, M., Gorski, T., Tikalsky, J.
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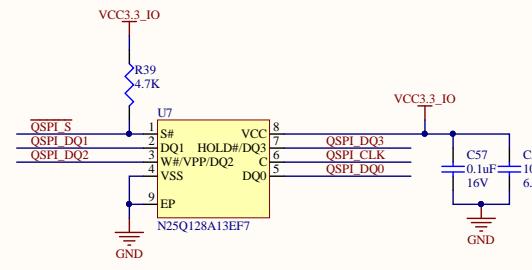
A

A



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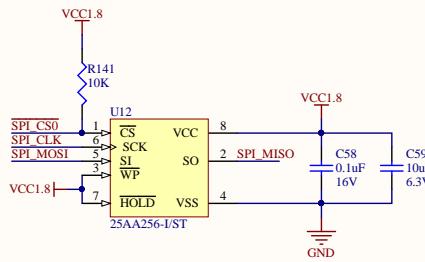
B



QSPI has 16MBytes
Needs 50ohm lines
C should be pulled LOW, but there is already the Zynq strap-pins.
40 MHz is the max speed allowed due to the hold times imposed by Zynq.
Check ZC702 schematic for more details.

C

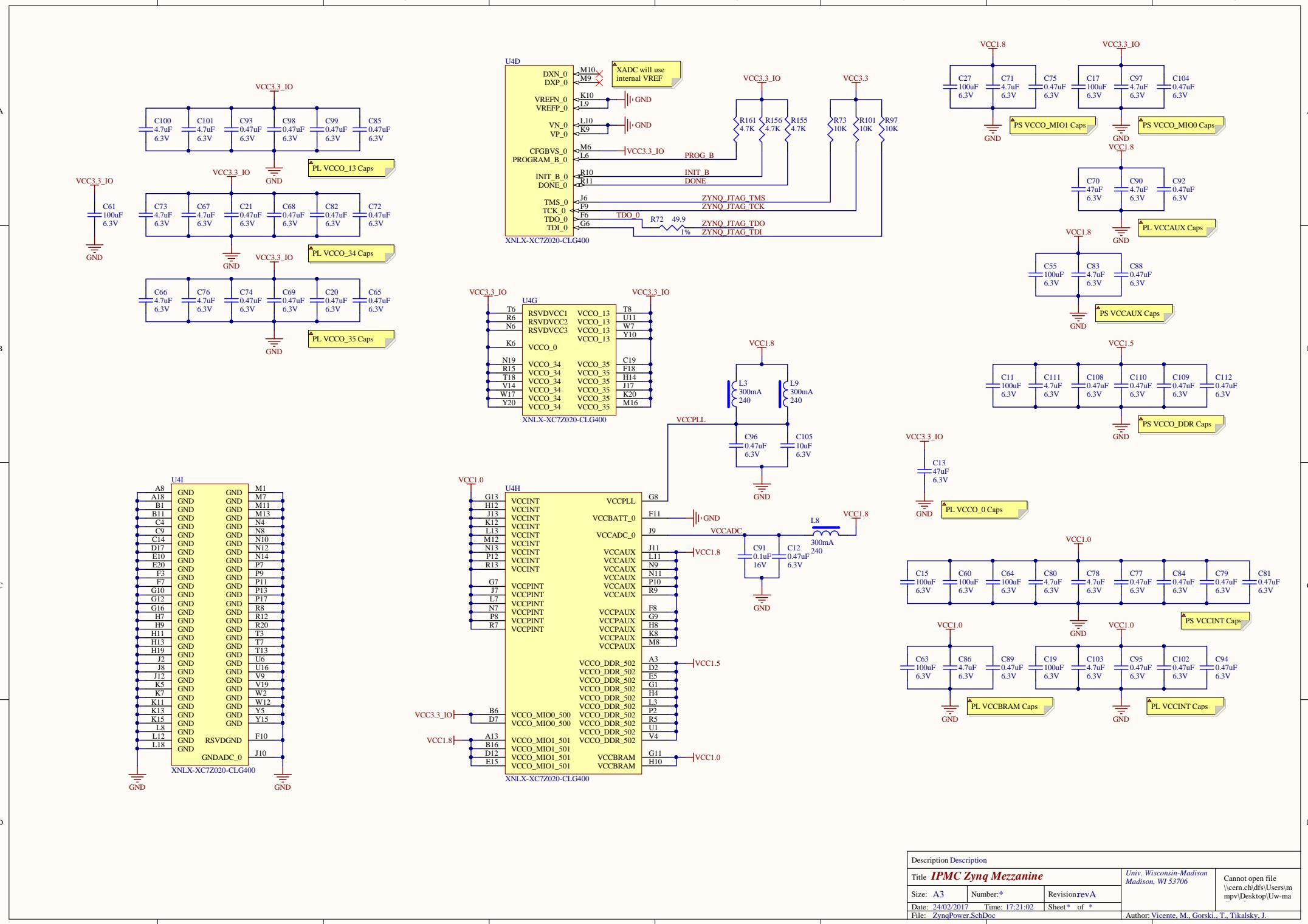
C



D

D

Description	Description	Univ. Wisconsin-Madison Madison, WI 53706	Cannot open file \\cernchdfs\Users\mmpv\Desktop\Uw-ma
Title	IPMC Zynq Mezzanine		
Size:	A3	Number:*	Revision revA
Date:	24/02/2017	Time: 17:21:02	Sheet * of *
File:	ZynqPeripherals.SchDoc		Author: Vicente, M., Gorski, T., Tikalsky, J.

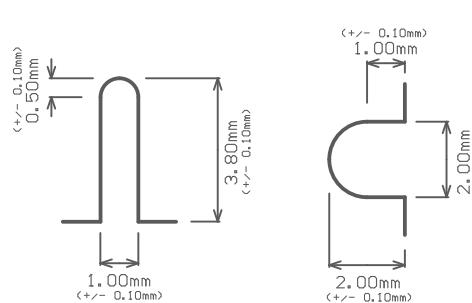


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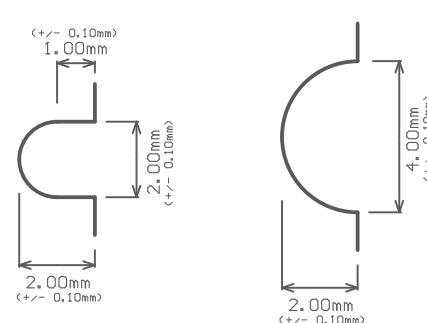
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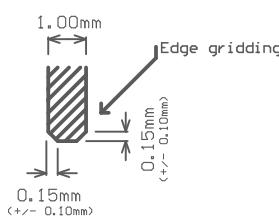


Detail 1



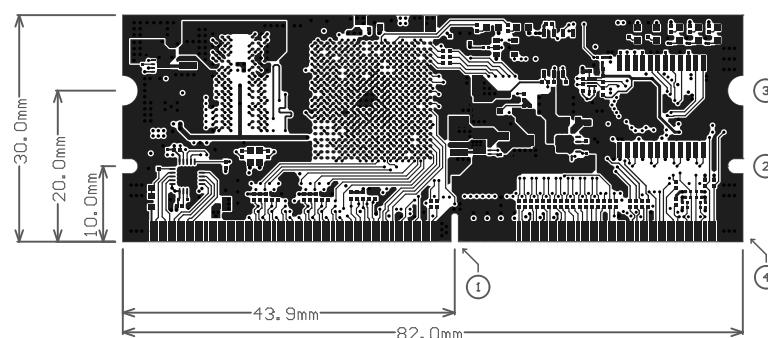
Detail 2

Detail 3

Detail 4
(PCB side view)

UW IPMC ZYNQ MEZZANINE

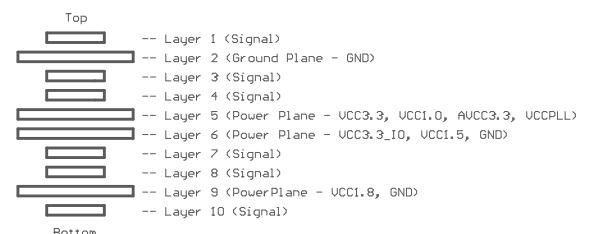
Layer 1 - Signal (Copper)



Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm +/- 0.10mm
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
 Internal layers (3, 4, 7, 8):
 40 Ohm: 6 mil tracks in artwork
 50 Ohm: 4.0 mil tracks in artwork
 External Layers (1 and 10):
 40 Ohm: 9.5 mil tracks in artwork
 50 Ohm: 6.5 mil tracks in artwork
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
 a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
 d. Drill locations are partitioned into 3 separate drill files
 * Plated-through holes
 * Non-Plated-through holes
 * Plated slots
6. Finish:
 a. Board contains a hard gold finish area on the south edge of the top and bottom surface.
 Area to receive hard gold finish is identified in two separate photoplot layers.
 Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 b. Overall board finish is immersion gold.
7. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
8. Red colored solder mask shall be applied to both top and bottom surfaces.
 Mask shall be photoimangible, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (Class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
 a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
 DC resistance shall be 10 ohms or less
 c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing.
 Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
 a. Tolerance of 0.03mm between pads.
 b. Board edge to pads maximum of 0.25mm.
 c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	REV: revA
PCB DESIGNER: Vicente, M.		
DATE: 24FEB2017	PART NO:	
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO:	SCALE: 1:1

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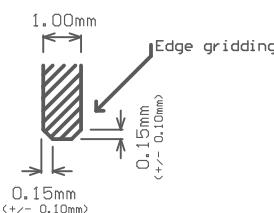
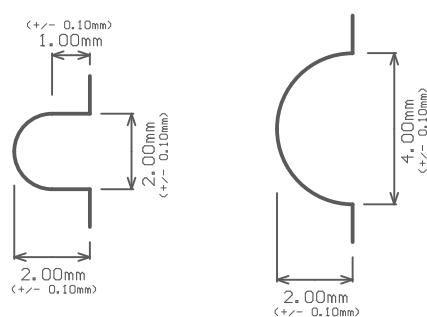
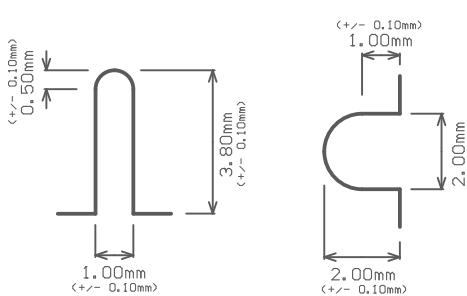
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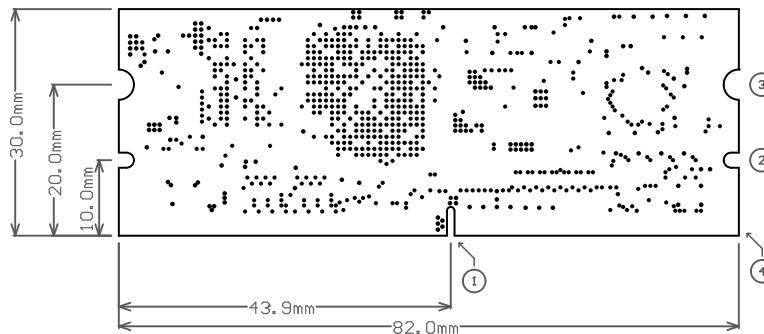
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Detail 4
(PCB side view)

UW IPMC ZYNQ MEZZANINE

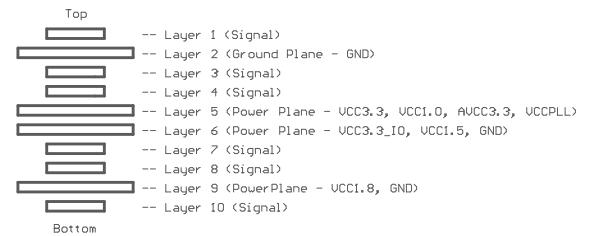
Layer 2 - Ground Plane (Copper, Mask)



Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
 - Internal layers (3, 4, 7, 8):
 - 40 Ohm: 6 mil tracks in artwork
 - 50 Ohm: 4.0 mil tracks in artwork
 - External Layers (1 and 10):
 - 40 Ohm: 9.5 mil tracks in artwork
 - 50 Ohm: 6.5 mil tracks in artwork
4. Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
5. Holes:
 - a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
 - d. Drill locations are partitioned into 3 separate drill files
 - * Plated-through holes
 - * Non-Plated-through holes
 - * Plated slots
6. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
7. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
8. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagineable, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (Class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
 - c. DC resistance shall be 10 ohms or less
 - d. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - e. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
 - a. Tolerance of 0.03mm between pads.
 - b. Board edge to pads maximum of 0.25mm.
 - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

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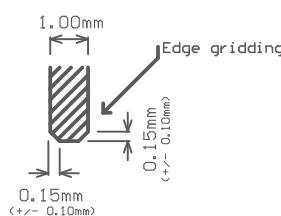
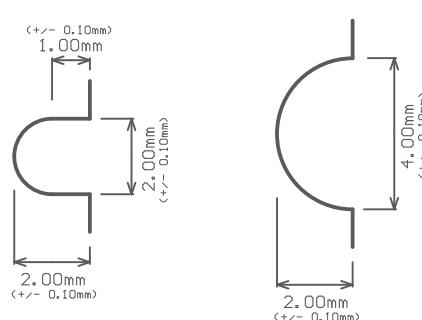
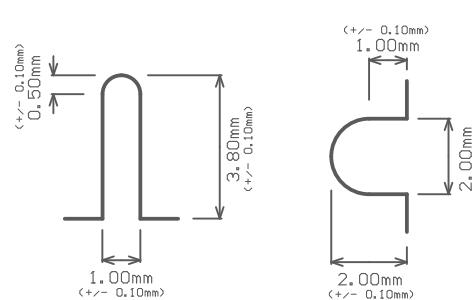
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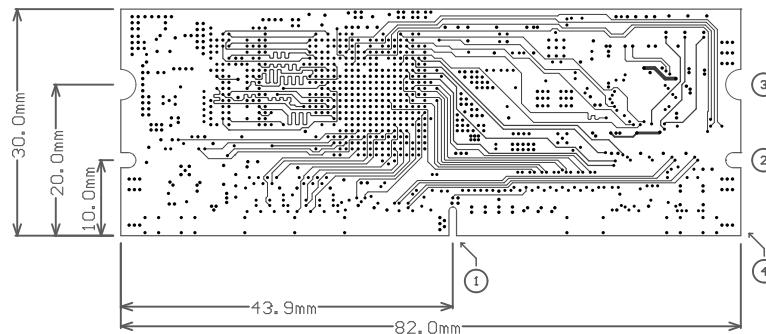
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Detail 4
(PCB side view)

UW IPMC ZYNQ MEZZANINE

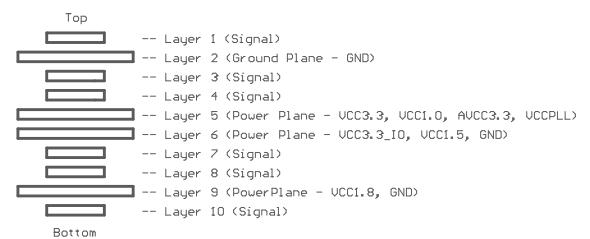
Layer 3 - Signal (Copper)



Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
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50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
 - a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
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6. Finish:
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7. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
8. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimangible, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (Class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
 - a. Tolerance of 0.03mm between pads.
 - b. Board edge to pads maximum of 0.25mm.
 - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

1

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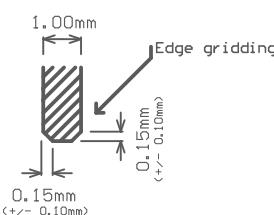
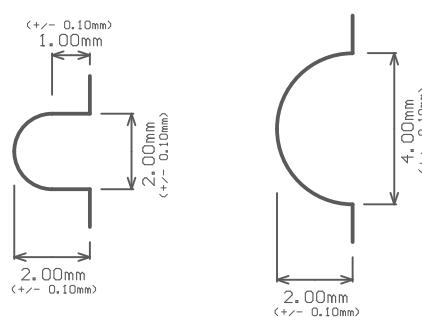
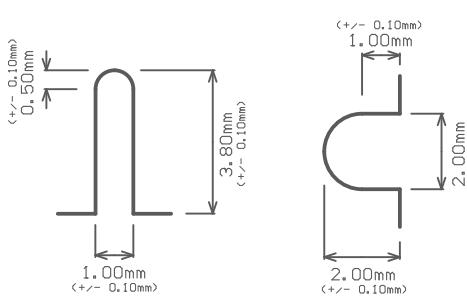
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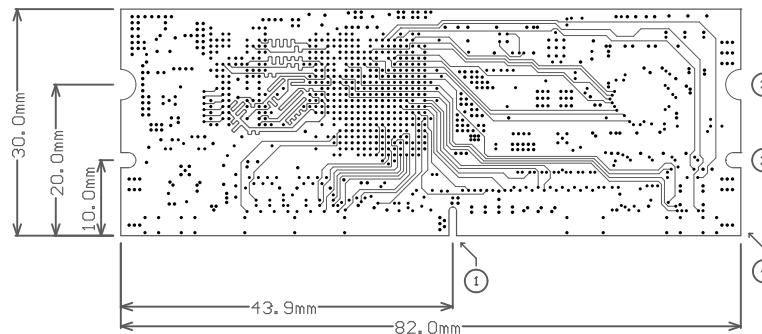
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Detail 4
(PCB side view)

UW IPMC ZYNQ MEZZANINE

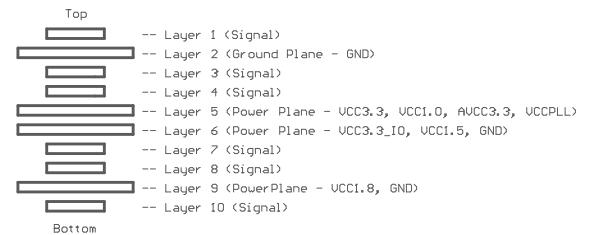
Layer 4 - Signal (Copper)



Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
d. Drill locations are partitioned into 3 separate drill files
* Plated-through holes
* Non-Plated-through holes
* Plated slots
6. Finish:
a. Board contains a hard gold finish area on the south edge of the top and bottom surface.
Area to receive hard gold finish is identified in two separate photoplot layers.
Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
b. Overall board finish is immersion gold.
7. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
8. Red colored solder mask shall be applied to both top and bottom surfaces.
Mask shall be photoimagineable, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (Class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
a. All layers to undergo optical inspection (machine-based) of all layers before lamination
b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
DC resistance shall be 10 ohms or less
c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing.
Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
a. Tolerance of 0.03mm between pads.
b. Board edge to pads maximum of 0.25mm.
c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 24FEB2017	PART NO.:	REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.:	SCALE: 1:1

1

2

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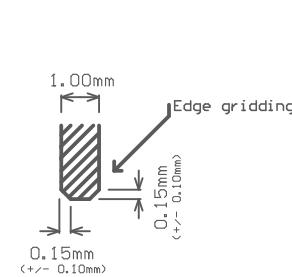
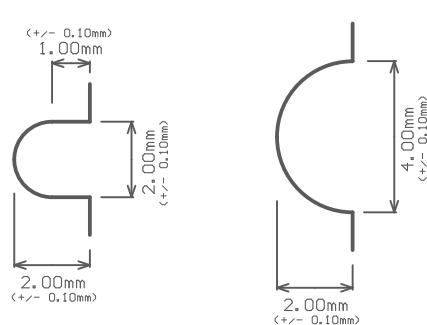
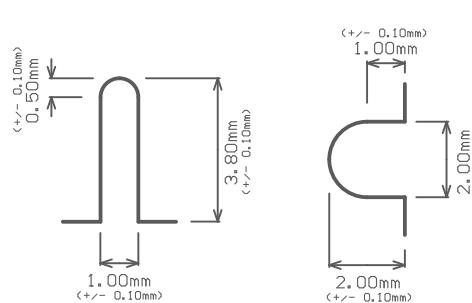
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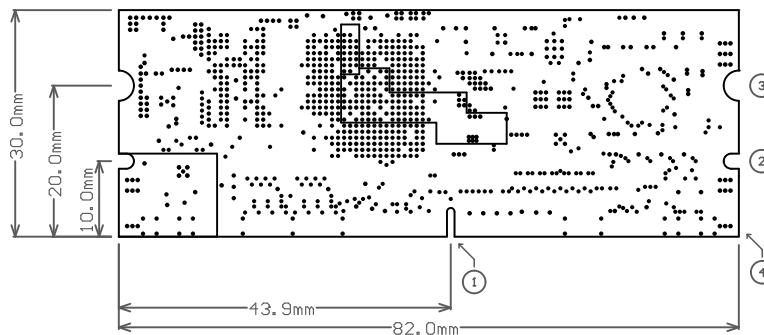
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Detail 4
(PCB side view)

UW IPMC ZYNQ MEZZANINE

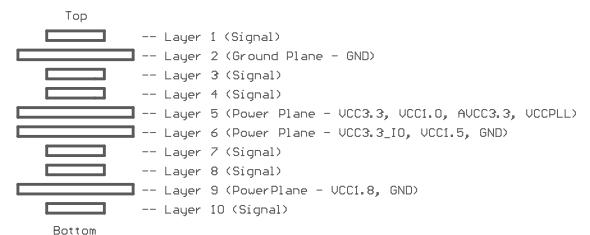
Layer 5 - Power Plane (Copper, Mask)



Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
 - Internal layers (3, 4, 7, 8):
 - 40 Ohm: 6 mil tracks in artwork
 - 50 Ohm: 4.0 mil tracks in artwork
 - External Layers (1 and 10):
 - 40 Ohm: 9.5 mil tracks in artwork
 - 50 Ohm: 6.5 mil tracks in artwork
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
4. Holes:
 - a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
 - d. Drill locations are partitioned into 3 separate drill files
 - * Plated-through holes
 - * Non-Plated-through holes
 - * Plated slots
5. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
6. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
7. Red colored solder mask shall be applied to both top and bottom surfaces.
8. Mask shall be photoimagable, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (Class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
 - c. DC resistance shall be 10 ohms or less
 - d. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - e. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
 - a. Tolerance of 0.03mm between pads.
 - b. Board edge to pads maximum of 0.25mm.
 - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

1

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A

B

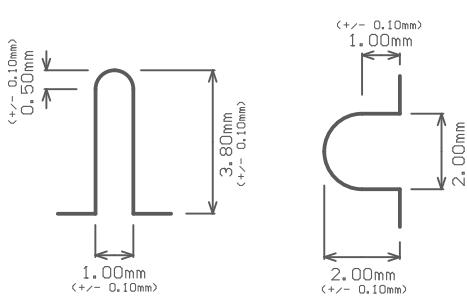
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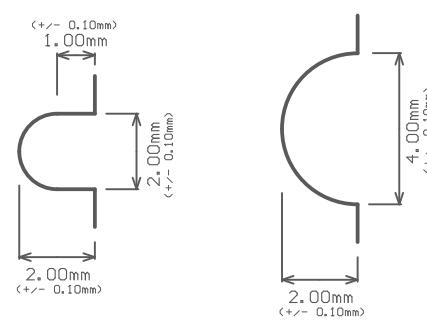
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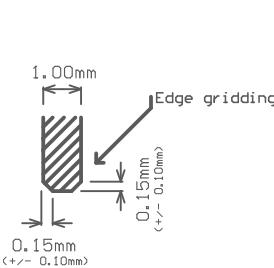
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Detail 1



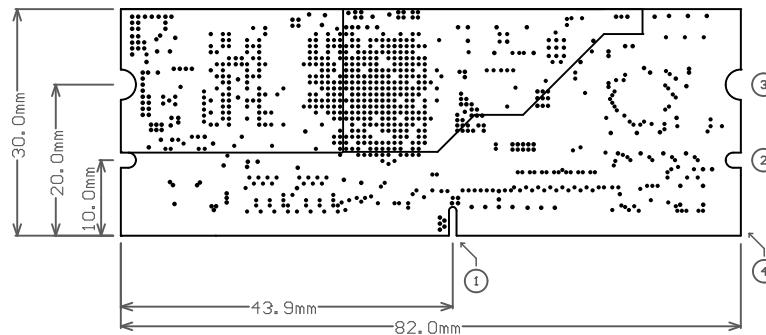
Detail 2



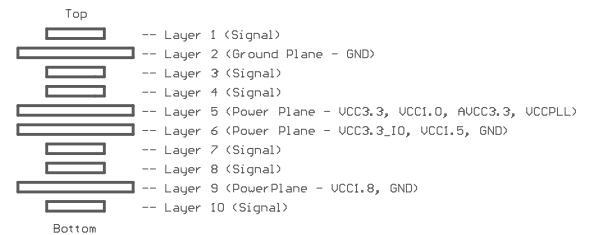
Detail 3

Detail 4
(PCB side view)**UW IPMC ZYNQ MEZZANINE**

Layer 6 - Power Plane (Copper, Mask)

**Specifications:**

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm +/- 0.10mm
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
 - Internal layers (3, 4, 7, 8):
 - 40 Ohm: 6 mil tracks in artwork
 - 50 Ohm: 4.0 mil tracks in artwork
 - External Layers (1 and 10):
 - 40 Ohm: 9.5 mil tracks in artwork
 - 50 Ohm: 6.5 mil tracks in artwork
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
4. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
 - d. Drill locations are partitioned into 3 separate drill files
 - * Plated-through holes
 - * Non-Plated-through holes
 - * Plated slots
5. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
6. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
7. Red colored solder mask shall be applied to both top and bottom surfaces.
8. Mask shall be photoimagable, with maximum thickness of 3 mils.
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED.
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (Class 2).
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction.
13. Design origin is at the bottom-left corner of the PCB.
14. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
 - c. DC resistance shall be 10 ohms or less
 - d. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - e. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units.
16. South edge-to-edge connector details:
 - a. Tolerance of 0.03mm between pads.
 - b. Board edge to pads maximum of 0.25mm.
 - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer StackupUniv. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

1

2

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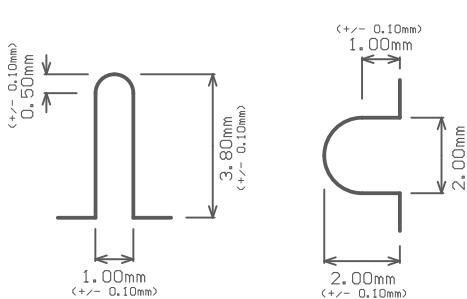
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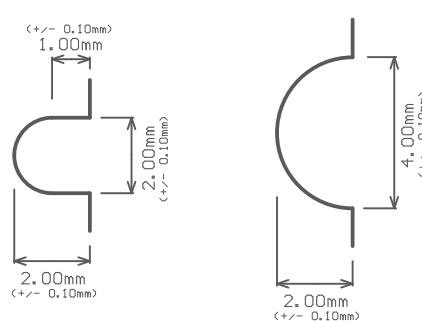
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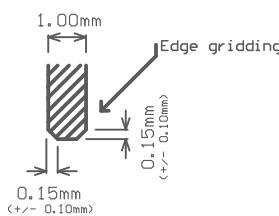


Detail 1



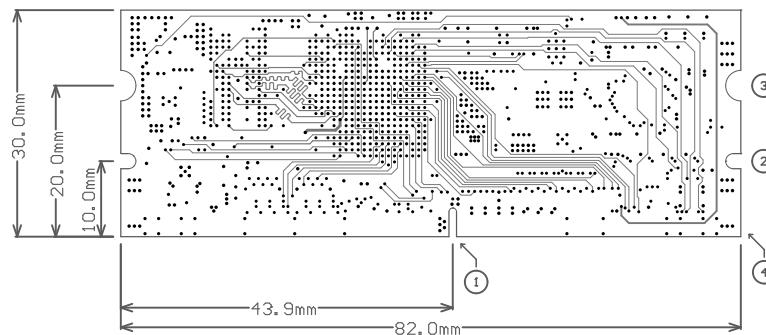
Detail 2

Detail 3

Detail 4
(PCB side view)

UW IPMC ZYNQ MEZZANINE

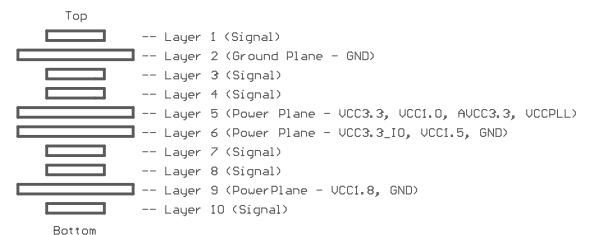
Layer 7 - Signal (Copper)



Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm +/- 0.10mm
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
 - d. Drill locations are partitioned into 3 separate drill files
 - * Plated-through holes
 - * Non-Plated-through holes
 - * Plated slots
6. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
7. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
8. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagineable, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
 - a. Tolerance of 0.03mm between pads.
 - b. Board edge to pads maximum of 0.25mm.
 - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 24FEB2017	PART NO.:	REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.:	SCALE: 1:1

1

2

3

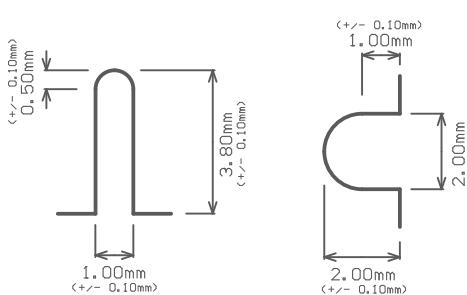
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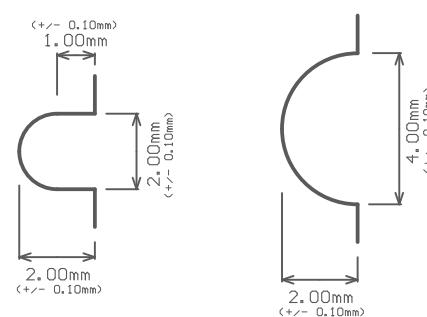
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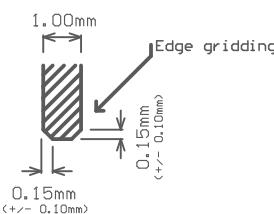
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Detail 1



Detail 2



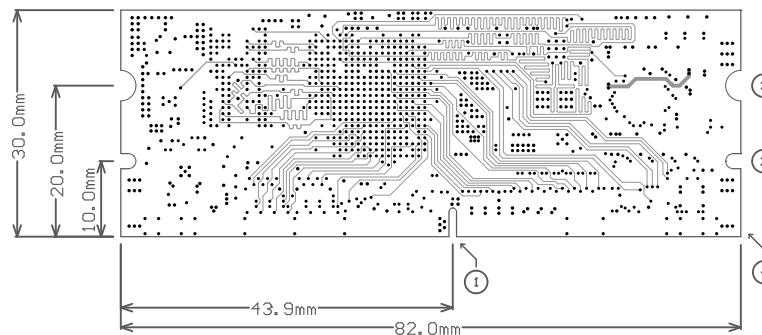
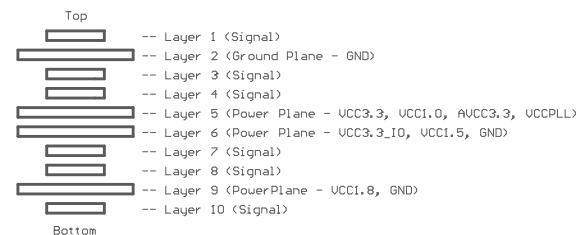
Detail 3

Detail 4
(PCB side view)**Specifications:**

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^\circ\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
 Internal layers (3, 4, 7, 8):
 40 Ohm: 6 mil tracks in artwork
 50 Ohm: 4.0 mil tracks in artwork
 External Layers (1 and 10):
 40 Ohm: 9.5 mil tracks in artwork
 50 Ohm: 6.5 mil tracks in artwork
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
4. Holes:
 a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing.
 b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed.
 c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
 d. Drill locations are partitioned into 3 separate drill files
 * Plated-through holes
 * Non-Plated-through holes
 * Plated slots
5. Finish:
 a. Board contains a hard gold finish area on the south edge of the top and bottom surface.
 Area to receive hard gold finish is identified in two separate photoplot layers.
 Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 b. Overall board finish is immersion gold.
6. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
7. Red colored solder mask shall be applied to both top and bottom surfaces.
 Mask shall be photoimposable, with maximum thickness of 3 mils
8. Mask shall be photoimposable, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (Class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
 a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
 DC resistance shall be 10 ohms or less
 c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing.
 Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
 a. Tolerance of 0.03mm between pads.
 b. Board edge to pads maximum of 0.25mm.
 c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

UW IPMC ZYNQ MEZZANINE

Layer 8 - Signal (Copper)

**Layer Stackup**Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	REV: revA
PCB DESIGNER: Vicente, M.	DATE: 24FEB2017	
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	PART NO:	DWG NO:
		SCALE: 1:1

1

2

3

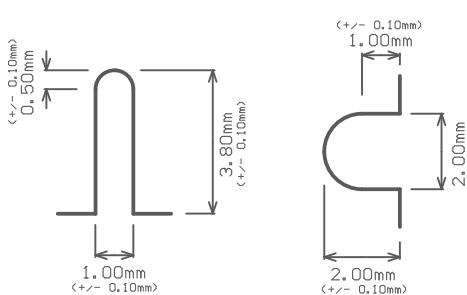
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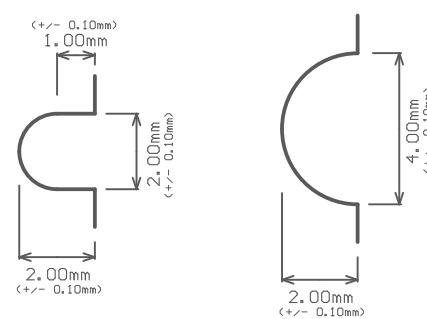
2

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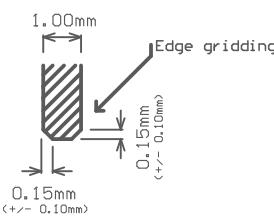


Detail 1



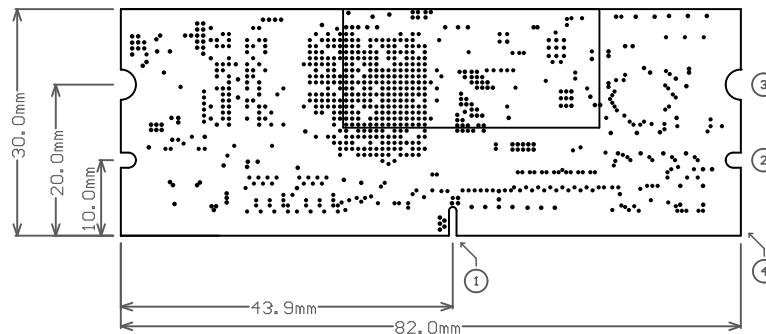
Detail 2

Detail 3

Detail 4
(PCB side view)

UW IPMC ZYNQ MEZZANINE

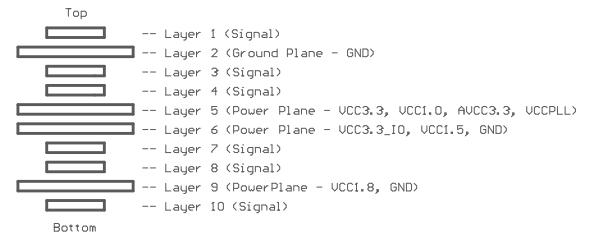
Layer 9 - Power Plane (Copper, Mask)



Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm +/- 0.10mm
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
 - Internal layers (3, 4, 7, 8):
 - 40 Ohm: 6 mil tracks in artwork
 - 50 Ohm: 4.0 mil tracks in artwork
 - External Layers (1 and 10):
 - 40 Ohm: 9.5 mil tracks in artwork
 - 50 Ohm: 6.5 mil tracks in artwork
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
4. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
 - d. Drill locations are partitioned into 3 separate drill files
 - * Plated-through holes
 - * Non-Plated-through holes
 - * Plated slots
5. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
6. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
7. Red colored solder mask shall be applied to both top and bottom surfaces.
8. Mask shall be photoimagable, with maximum thickness of 3 mils.
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED.
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2).
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction.
13. Design origin is at the bottom-left corner of the PCB.
14. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
 - c. DC resistance shall be 10 ohms or less
 - d. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - e. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units.
16. South edge-to-edge connector details:
 - a. Tolerance of 0.03mm between pads.
 - b. Board edge to pads maximum of 0.25mm.
 - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup

Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module
PCB DESIGNER: Vicente, M.	PART NO.: revA
DATE: 24FEB2017	REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: 1:1

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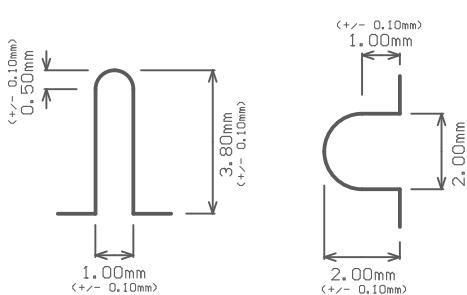
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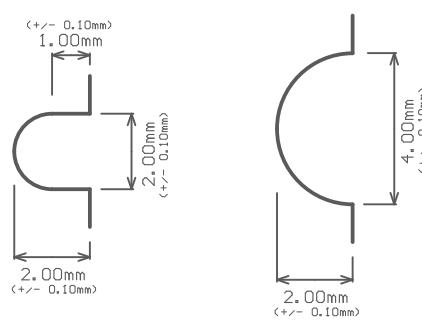
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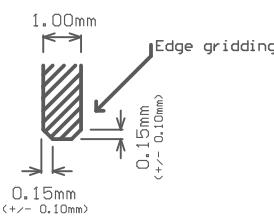


Detail 1



Detail 2

Detail 3

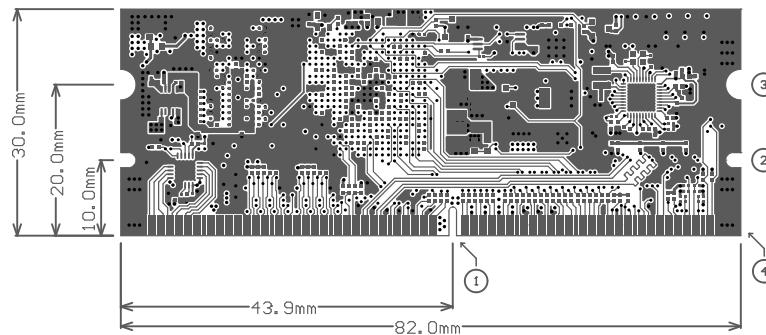
Detail 4
(PCB side view)

Specifications:

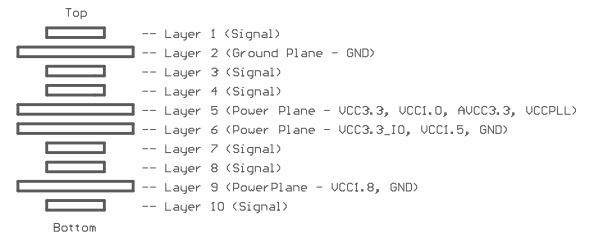
1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm +/- 0.10mm
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
 - d. Drill locations are partitioned into 3 separate drill files
 - * Plated-through holes
 - * Non-Plated-through holes
 - * Plated slots
6. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
7. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
8. Red colored solder mask shall be applied to both top and bottom surfaces.
9. Mask shall be photoimagineable, with maximum thickness of 3 mils
10. Layers 2, 5, 6 and 9 are power planes and are INVERTED
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
 - c. DC resistance shall be 10 ohms or less
 - d. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - e. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
 - a. Tolerance of 0.03mm between pads.
 - b. Board edge to pads maximum of 0.25mm.
 - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

UW IPMC ZYNQ MEZZANINE

Layer 10 - Signal (Copper)



Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER:
Vicente, M., Gorski, T., Tikalsky, J.
PCB DESIGNER:
Vicente, M.
DATE:
24FEB2017
FILE NAME:
UW_IPMC_ZYNQ.PCBDOC

TITLE:
UW IPMC Zynq Module

PART NO:

REV:
revA

DWG NO:

SCALE:
1:1

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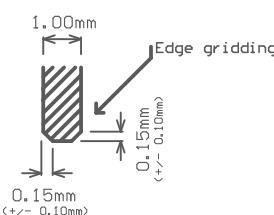
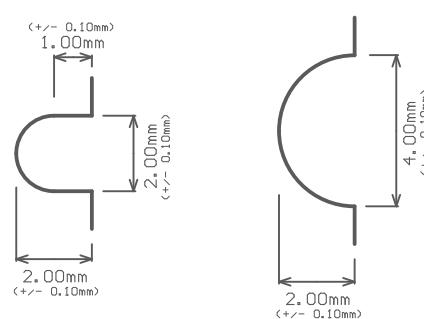
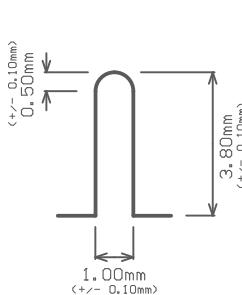
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Detail 4
(PCB side view)

Detail 1

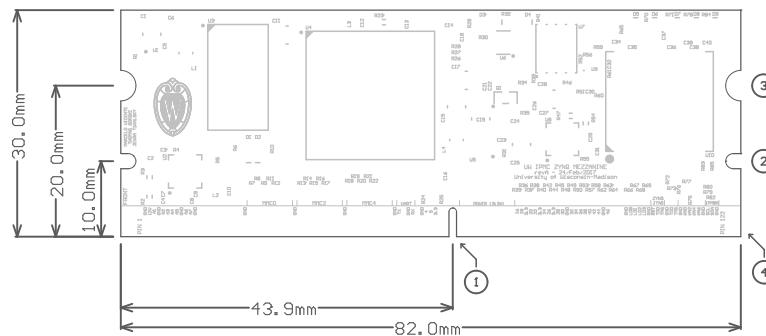
Detail 2

Detail 3

Detail 4

UW IPMC ZYNQ MEZZANINE

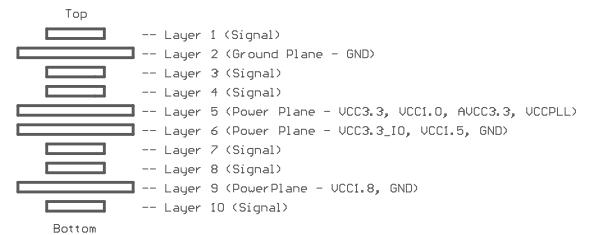
Top Overlay (Ink)



Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
4. Holes:
a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
d. Drill locations are partitioned into 3 separate drill files
* Plated-through holes
* Non-Plated-through holes
* Plated slots
5. Finish:
a. Board contains a hard gold finish area on the south edge of the top and bottom surface.
Area to receive hard gold finish is identified in two separate photoplot layers.
Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
b. Overall board finish is immersion gold.
6. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
7. Red colored solder mask shall be applied to both top and bottom surfaces.
Mask shall be photoimposable, with maximum thickness of 3 mils
8. Layers 2, 5, 6 and 9 are power planes and are INVERTED
9. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
10. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
11. Combination of bow and twist shall not exceed 10 mils/inch along any direction
12. Design origin is at the bottom-left corner of the PCB
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
a. All layers to undergo optical inspection (machine-based) of all layers before lamination
b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
DC resistance shall be 10 ohms or less
c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing.
Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
a. Tolerance of 0.03mm between pads.
b. Board edge to pads maximum of 0.25mm.
c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER:
Vicente, M., Gorski, T., Tikalsky, J.

PCB DESIGNER:
Vicente, M.

DATE:
24FEB2017

FILE NAME:
UW_IPMC_ZYNQ.PCBDOC

TITLE:
UW IPMC Zynq Module

PART NO:

REV:
revA

DWG NO:

SCALE:
1:1

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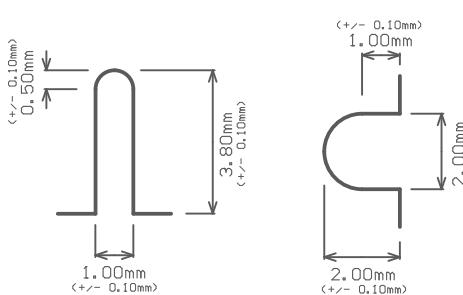
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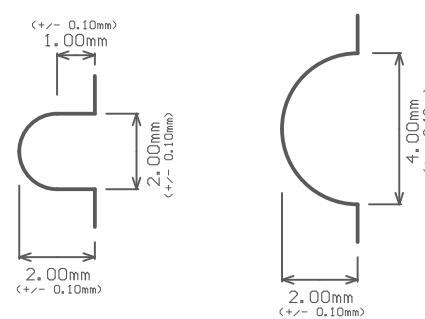
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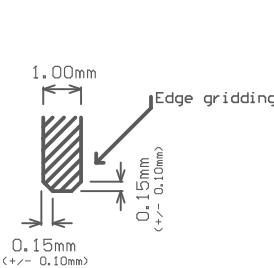
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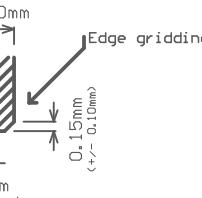
Detail 1



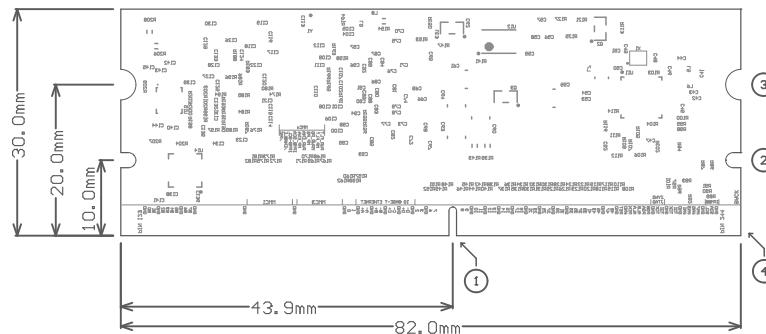
Detail 2



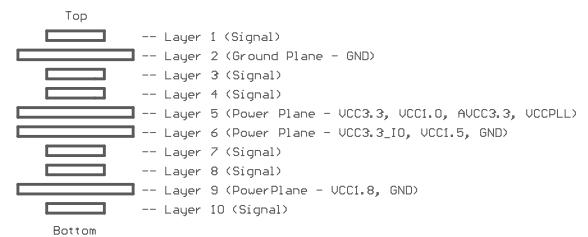
Detail 3

Detail 4
(PCB side view)**UW IPMC ZYNQ MEZZANINE**

Bottom Overlay (Ink)

**Specifications:**

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm +/- 0.10mm
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
 - Internal layers (3, 4, 7, 8):
 - 40 Ohm: 6 mil tracks in artwork
 - 50 Ohm: 4.0 mil tracks in artwork
 - External Layers (1 and 10):
 - 40 Ohm: 9.5 mil tracks in artwork
 - 50 Ohm: 6.5 mil tracks in artwork
4. Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
5. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
 - d. Drill locations are partitioned into 3 separate drill files
 - * Plated-through holes
 - * Non-Plated-through holes
 - * Plated slots
6. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
7. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
8. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimposable, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
 - a. Tolerance of 0.03mm between pads.
 - b. Board edge to pads maximum of 0.25mm.
 - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer StackupUniv. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module
PCB DESIGNER: Vicente, M.	PART NO:
DATE: 24FEB2017	REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO:
	SCALE: 1:1

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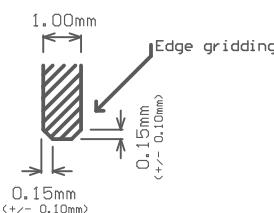
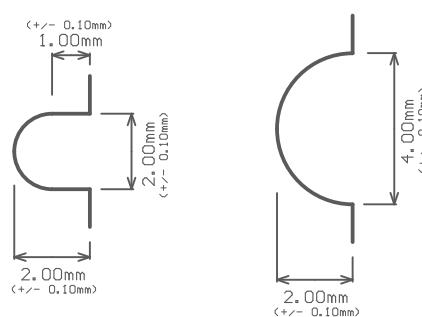
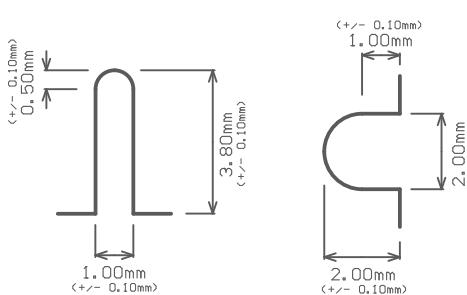
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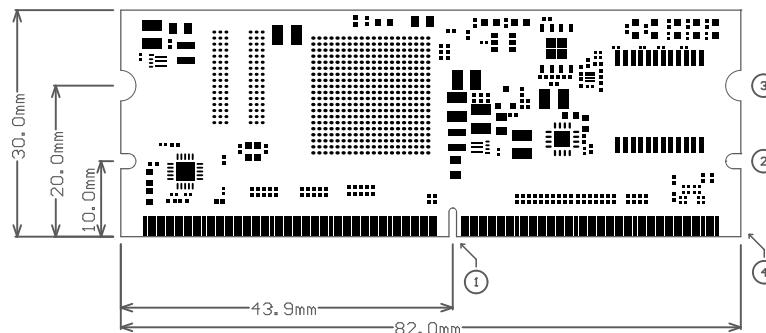
Detail 4
(PCB side view)

Specifications:

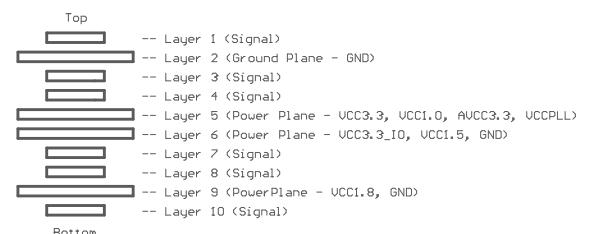
1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
 - a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
 - d. Drill locations are partitioned into 3 separate drill files
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 - * Non-Plated-through holes
 - * Plated slots
6. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
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9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
 - a. Tolerance of 0.03mm between pads.
 - b. Board edge to pads maximum of 0.25mm.
 - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

UW IPMC ZYNQ MEZZANINE

Top Paste (Paste)



Layer Stackup



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Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

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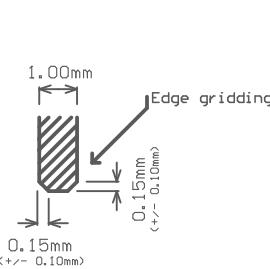
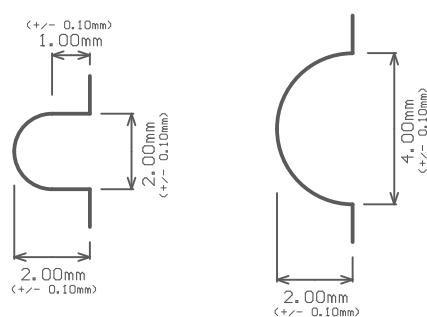
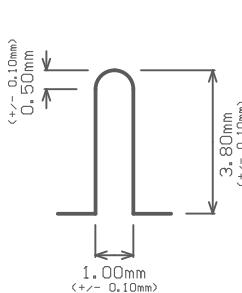
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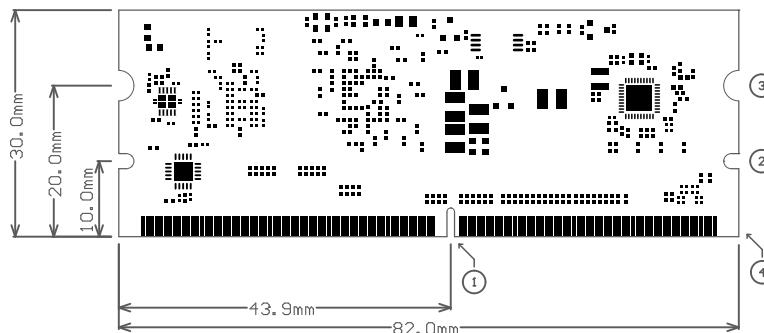
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Detail 4
(PCB side view)

UW IPMC ZYNQ MEZZANINE

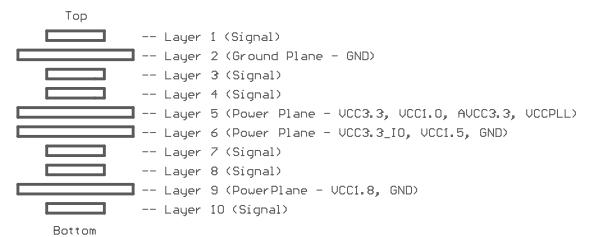
Bottom Paste (Paste)



Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
4. Holes:
a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing.
b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed.
c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
d. Drill locations are partitioned into 3 separate drill files
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* Plated slots
5. Finish:
a. Board contains a hard gold finish area on the south edge of the top and bottom surface.
Area to receive hard gold finish is identified in two separate photoplot layers.
Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
b. Overall board finish is immersion gold.
6. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
7. Red colored solder mask shall be applied to both top and bottom surfaces.
8. Mask shall be photoimposable, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
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12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
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14. Testing:
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c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing.
Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
a. Tolerance of 0.03mm between pads.
b. Board edge to pads maximum of 0.25mm.
c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



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A

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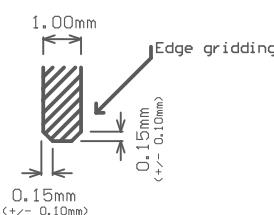
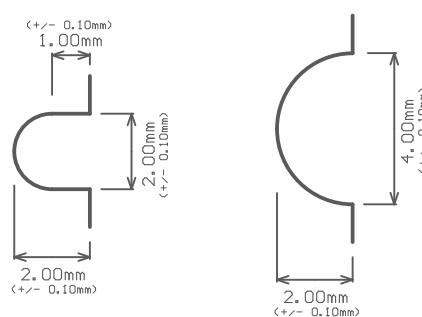
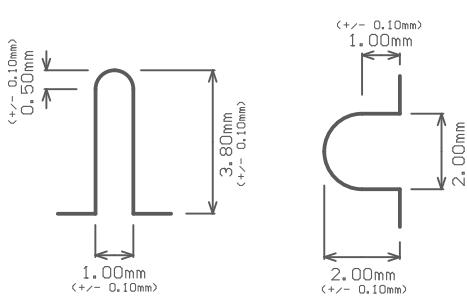
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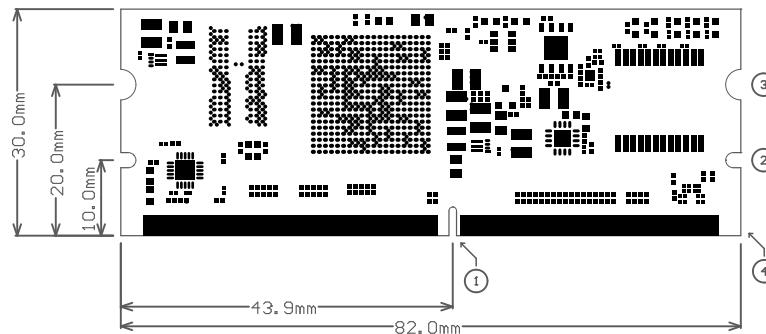
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Detail 4
(PCB side view)

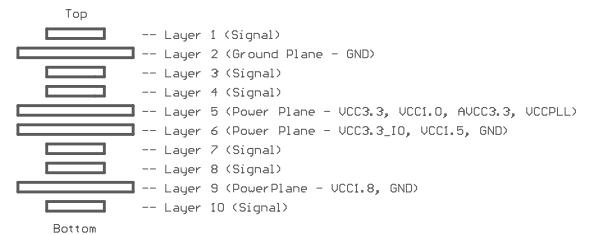
UW IPMC ZYNQ MEZZANINE



Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
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* Non-Plated-through holes
* Plated slots
5. Finish:
a. Board contains a hard gold finish area on the south edge of the top and bottom surface.
Area to receive hard gold finish is identified in two separate photoplot layers.
Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
b. Overall board finish is immersion gold.
6. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
7. Red colored solder mask shall be applied to both top and bottom surfaces.
8. Mask shall be photoimagable, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (Class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
a. All layers to undergo optical inspection (machine-based) of all layers before lamination
b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
DC resistance shall be 10 ohms or less
c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing.
Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
a. Tolerance of 0.03mm between pads.
b. Board edge to pads maximum of 0.25mm.
c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

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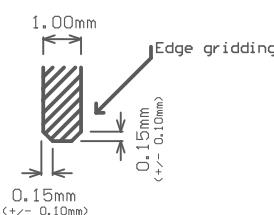
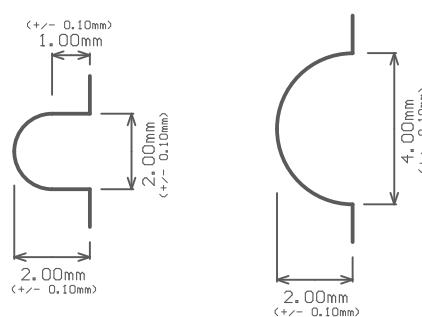
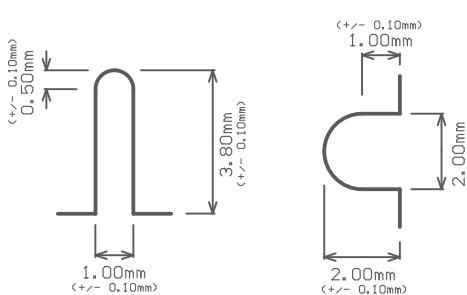
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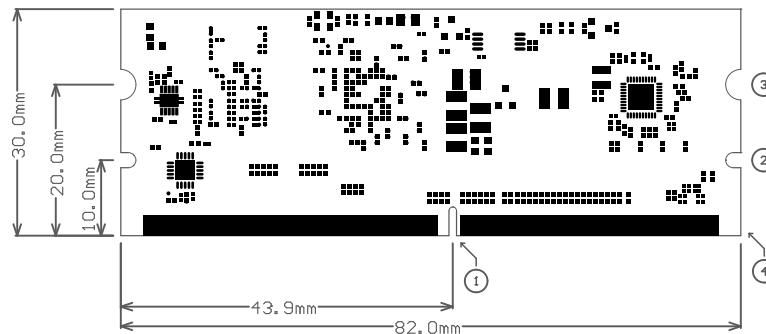
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Detail 4
(PCB side view)

UW IPMC ZYNQ MEZZANINE

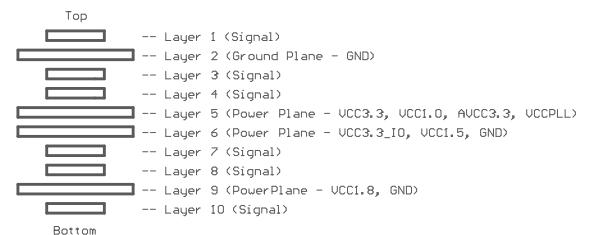
Bottom Solder (Mask)



Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
4. Holes:
a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing.
b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed.
c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
d. Drill locations are partitioned into 3 separate drill files
* Plated-through holes
* Non-Plated-through holes
* Plated slots
5. Finish:
a. Board contains a hard gold finish area on the south edge of the top and bottom surface.
Area to receive hard gold finish is identified in two separate photoplot layers.
Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
b. Overall board finish is immersion gold.
6. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
7. Red colored solder mask shall be applied to both top and bottom surfaces.
8. Mask shall be photoimposable, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (Class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
a. All layers to undergo optical inspection (machine-based) of all layers before lamination
b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
DC resistance shall be 10 ohms or less
c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing.
Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
a. Tolerance of 0.03mm between pads.
b. Board edge to pads maximum of 0.25mm.
c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER:
Vicente, M., Gorski, T., Tikalsky, J.

PCB DESIGNER:
Vicente, M.

DATE:
24FEB2017

FILE NAME:
UW_IPMC_ZYNQ.PCBDOC

TITLE:
UW IPMC Zynq Module

PART NO:

REV:
revA

DWG NO:

SCALE:
1:1

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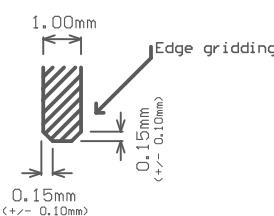
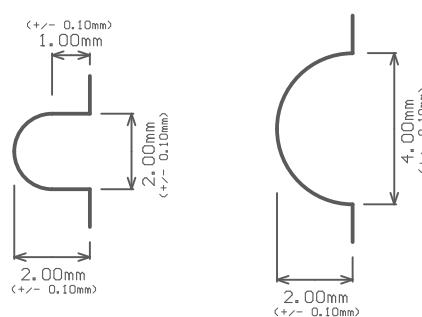
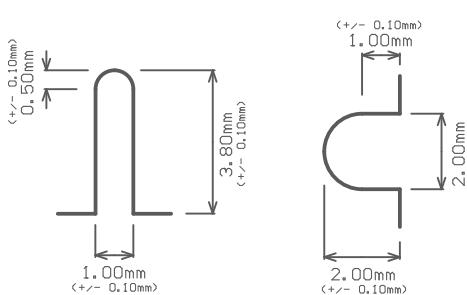
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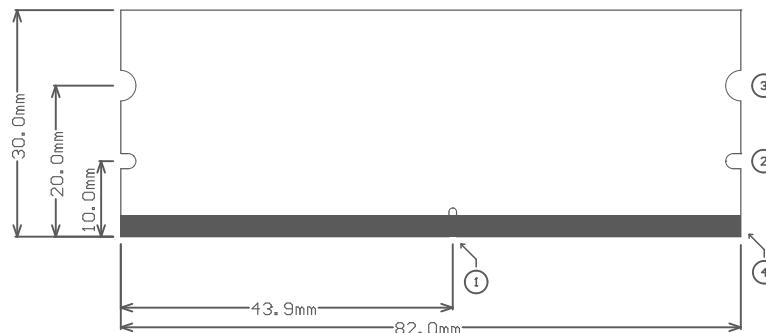


Detail 4
(PCB side view)

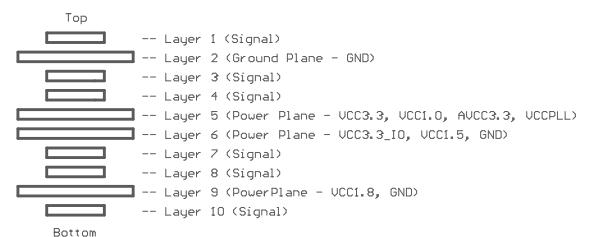
Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
4. Holes:
 - a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
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 - * Plated slots
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8. Mask shall be photoimagineable, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
 - a. Tolerance of 0.03mm between pads.
 - b. Board edge to pads maximum of 0.25mm.
 - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

UW IPMC ZYNQ MEZZANINE



Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 24FEB2017	PART NO.:	REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.:	SCALE: 1:1

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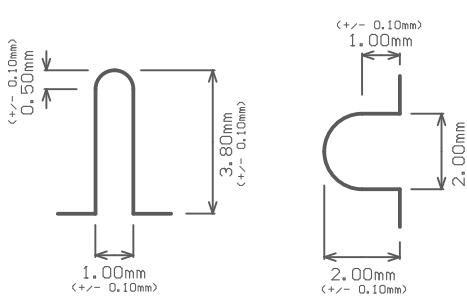
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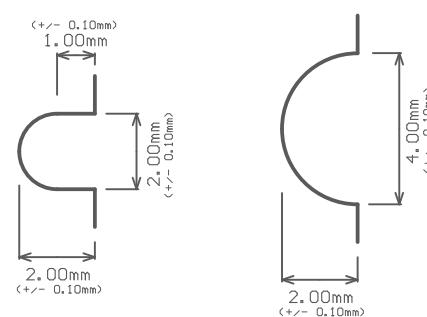
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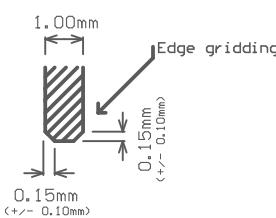


Detail 1



Detail 2

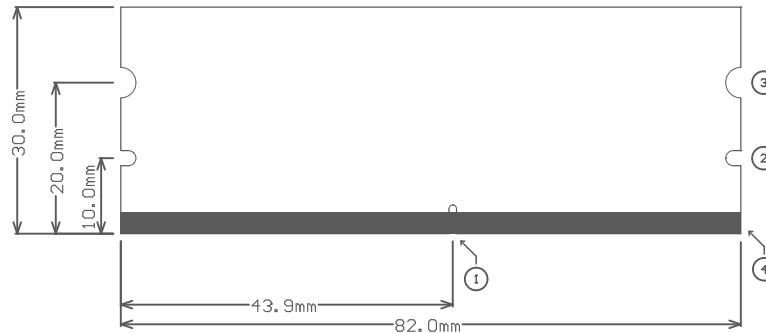
Detail 3

Detail 4
(PCB side view)

Specifications:

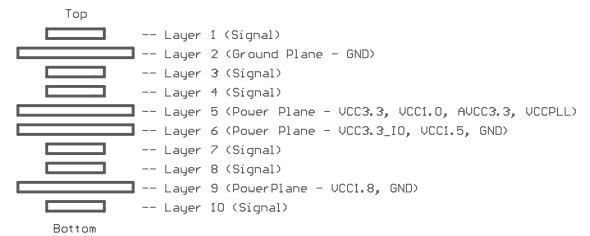
1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm +/- 0.10mm
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
 - Internal layers (3, 4, 7, 8):
 - 40 Ohm: 6 mil tracks in artwork
 - 50 Ohm: 4.0 mil tracks in artwork
 - External Layers (1 and 10):
 - 40 Ohm: 9.5 mil tracks in artwork
 - 50 Ohm: 6.5 mil tracks in artwork
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
4. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
 - d. Drill locations are partitioned into 3 separate drill files
 - * Plated-through holes
 - * Non-Plated-through holes
 - * Plated slots
5. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
6. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
7. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimangible, with maximum thickness of 3 mils
8. Mask shall be photoimangible, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
 - a. Tolerance of 0.03mm between pads.
 - b. Board edge to pads maximum of 0.25mm.
 - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

UW IPMC ZYNQ MEZZANINE



Bottom Hard Gold (Mask)

Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 24FEB2017	PART NO.:	REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.:	SCALE: 1:1

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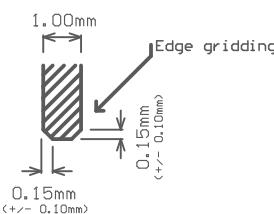
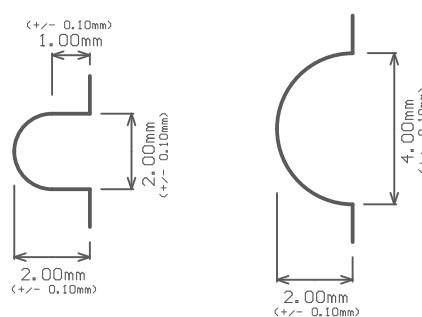
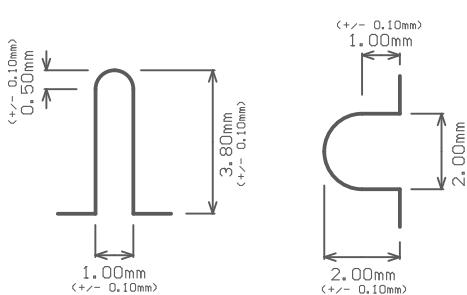
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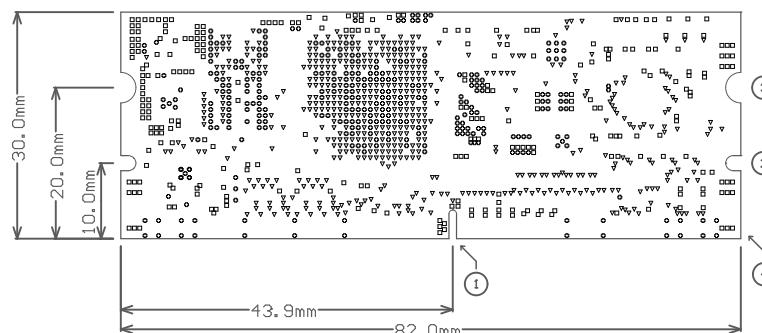


Detail 4
(PCB side view)

Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
 - a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
 - d. Drill locations are partitioned into 3 separate drill files
 - * Plated-through holes
 - * Non-Plated-through holes
 - * Plated slots
6. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
7. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
8. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimposable, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
 - a. Tolerance of 0.03mm between pads.
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 - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

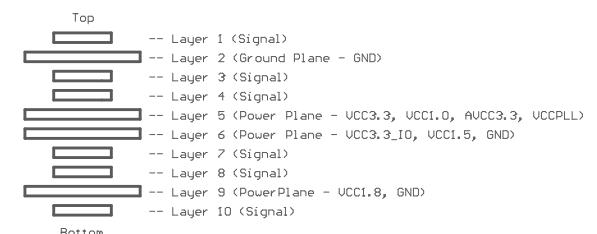
UW IPMC ZYNQ MEZZANINE



Drill Guide

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length	Rout Path Length
□	278	8.00mil (0.203mm)	PTH	Round	-	-
◊	304	7.00mil (0.178mm)	PTH	Round	-	-
▽	530	6.00mil (0.152mm)	PTH	Round	-	-
1112 Total						

Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER:
Vicente, M., Gorski, T., Tikalsky, J.

PCB DESIGNER:
Vicente, M.

DATE:
24FEB2017

FILE NAME:
UW_IPMC_ZYNQ.PCBDOC

TITLE:
UW IPMC Zynq Module

PART NO:

REV:
revA

DWG NO:

SCALE:
1:1

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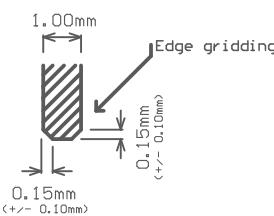
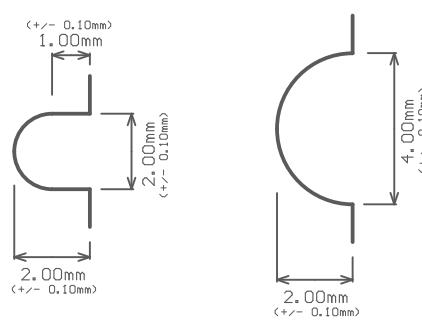
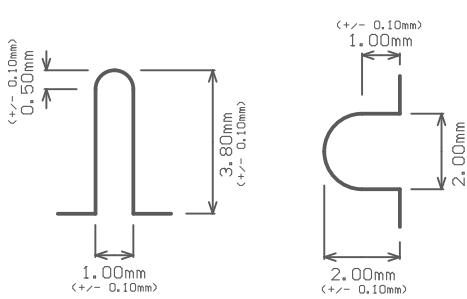
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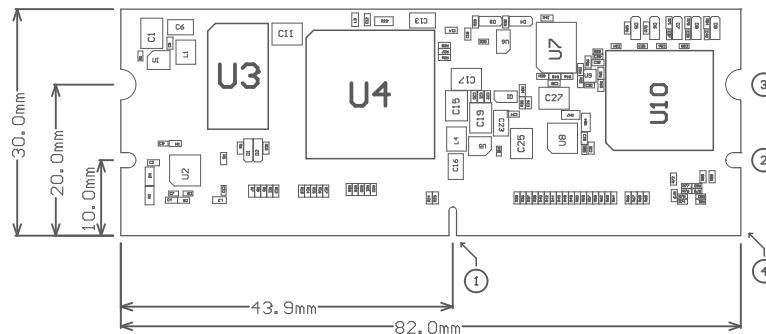


Detail 4
(PCB side view)

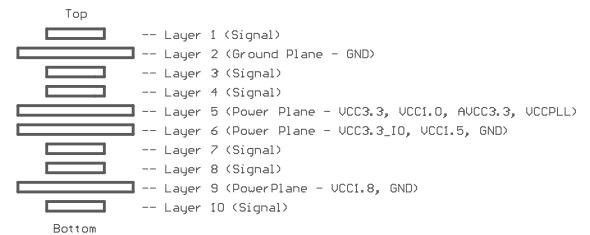
Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
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UW IPMC ZYNQ MEZZANINE



Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

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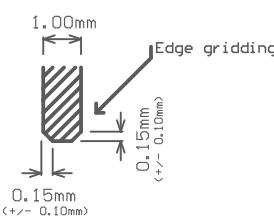
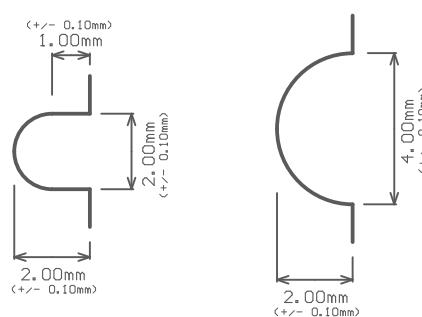
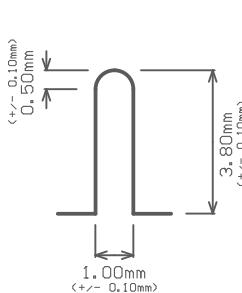
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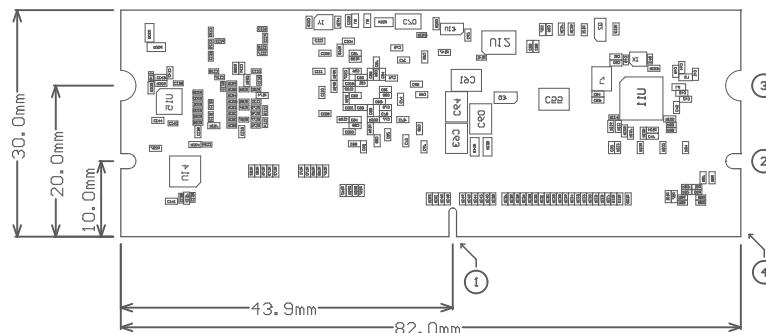
3

4



Detail 4
(PCB side view)

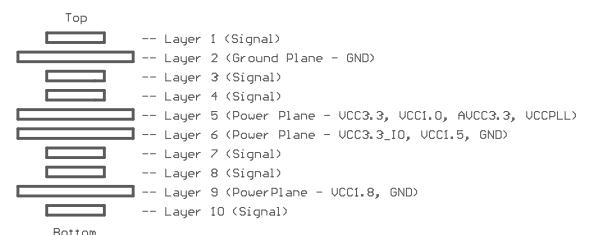
UW IPMC ZYNQ MEZZANINE



Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Controlled impedance 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
 - a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. 6mil and 7mil holes might be exposed as defined in the solder masks and drill files.
 - d. Drill locations are partitioned into 3 separate drill files
 - * Plated-through holes
 - * Non-Plated-through holes
 - * Plated slots
6. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
7. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
8. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimangible, with maximum thickness of 3 mils
9. Layers 2, 5, 6 and 9 are power planes and are INVERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (Class 2)
12. Combination of bow and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
15. Locations in IPC-D-356A file are given in 2.4 English units
16. South edge-to-edge connector details:
 - a. Tolerance of 0.03mm between pads.
 - b. Board edge to pads maximum of 0.25mm.
 - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



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ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

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