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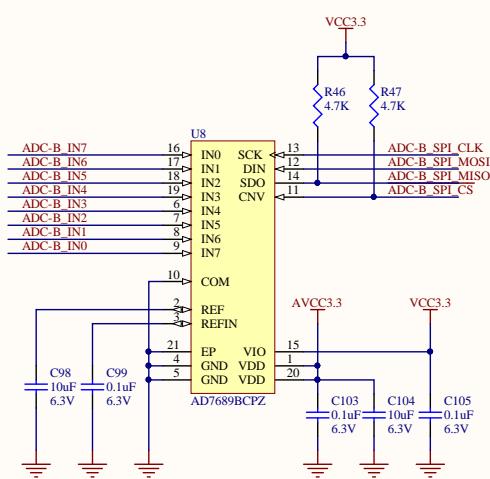
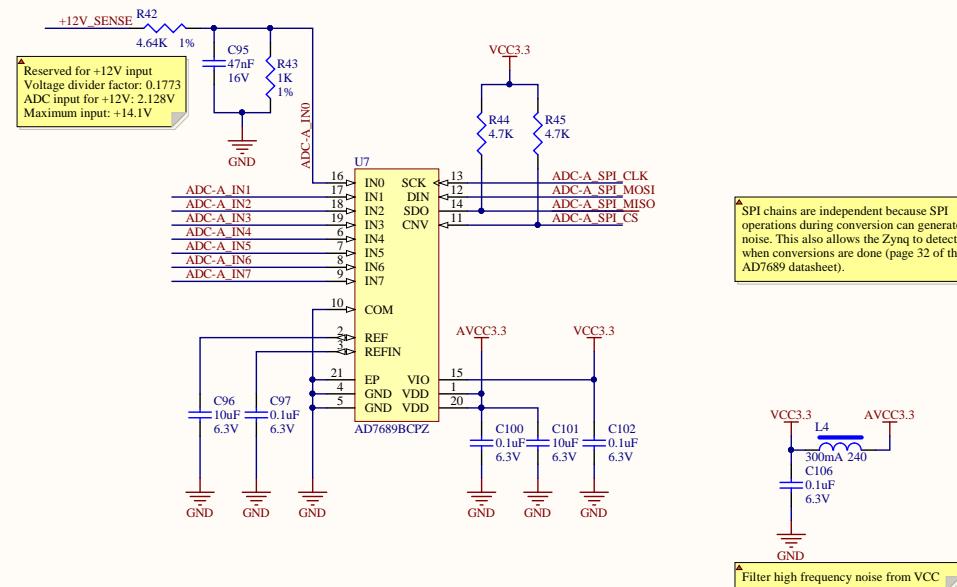
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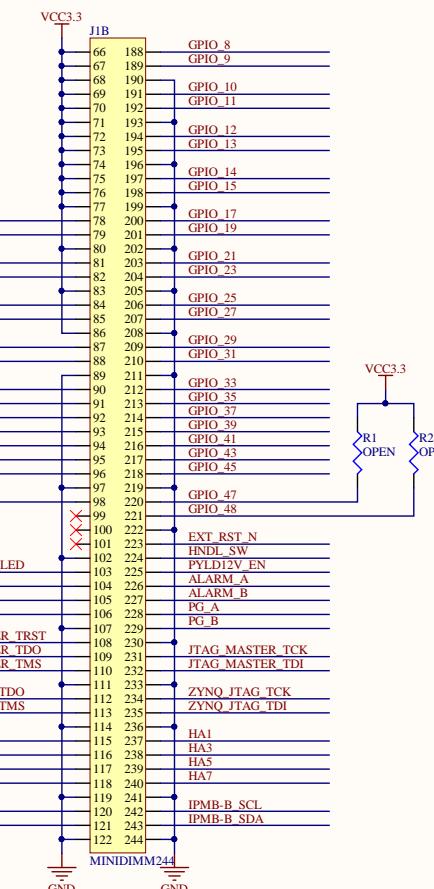
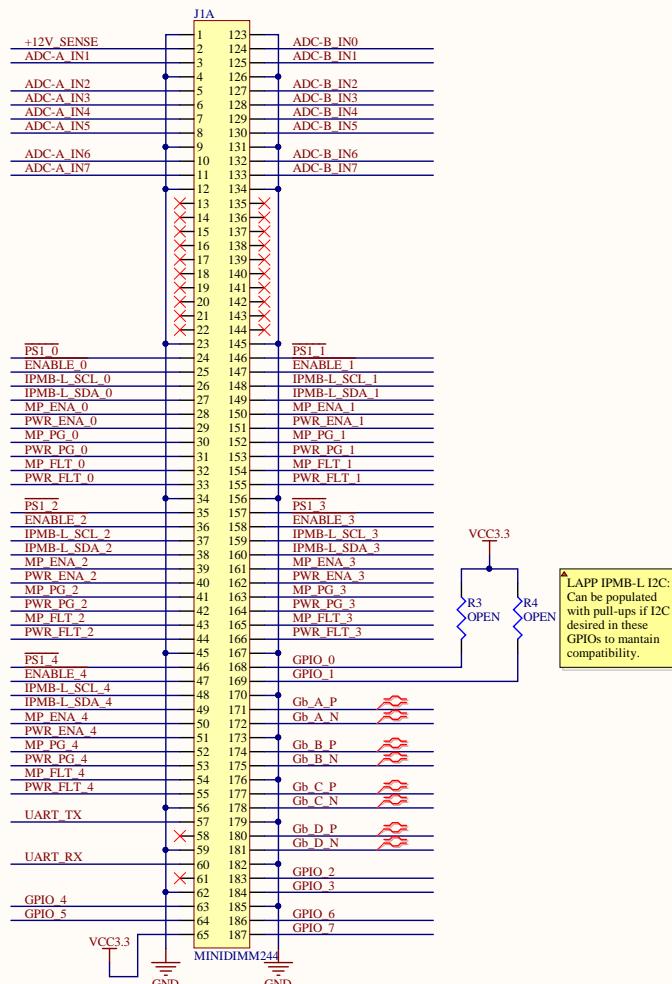
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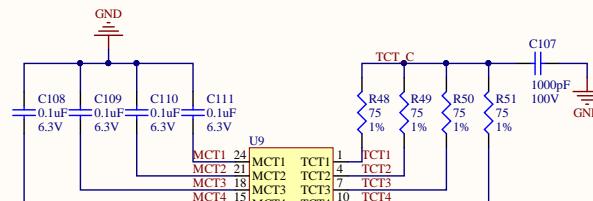


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Date:	21/02/2017 Time: 16:30:42
File:	AnalogSense.SchDoc
	Author: Vicente, M., Gorski, T., Tikhalsky, J.
	Univ. Wisconsin-Madison Madison, WI 53706
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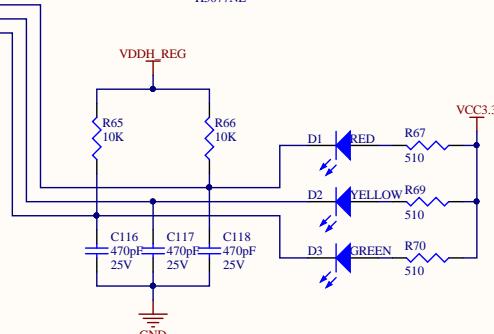
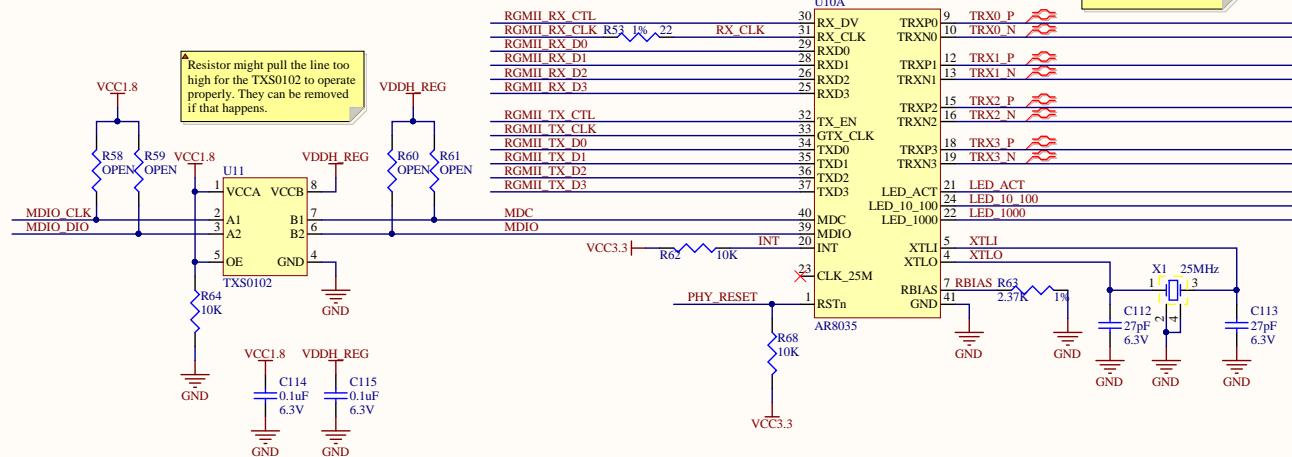
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Title	<b>IPMC_Zynq Mezzanine</b>		
Size:	A3	Number:*	Revision:revA
Date:	21/02/2017	Time: 16:30:42	Sheet: * of *
File:	BoardConnector.SchDoc		Author: Vicente, M., Gorski, T., Tikalsky, J.

A

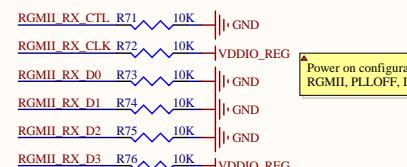
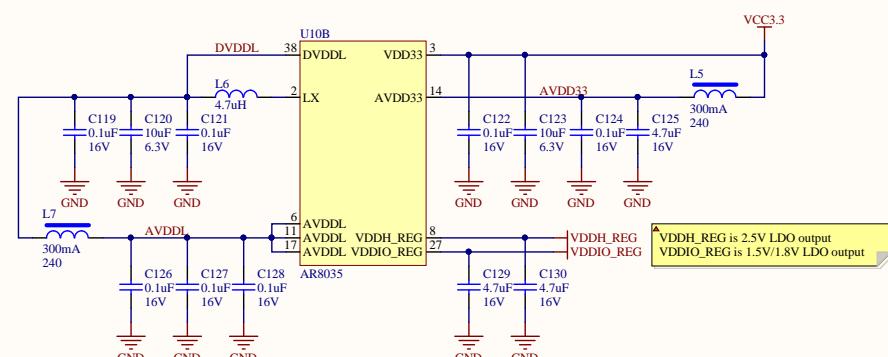


TRX lines are 100Ω

B

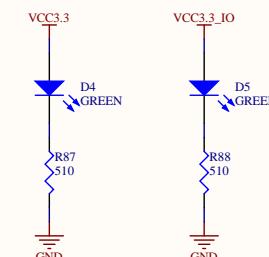
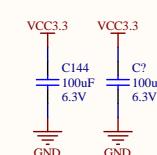
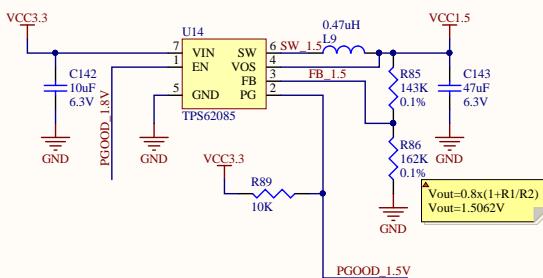
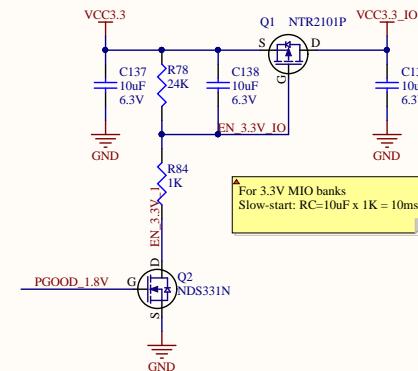
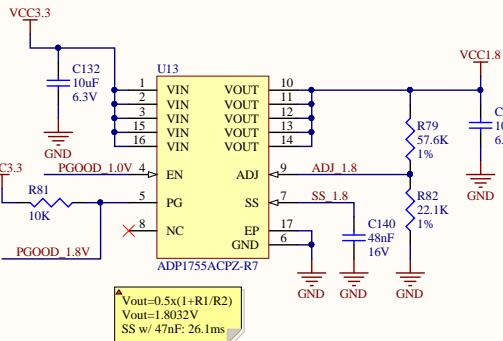
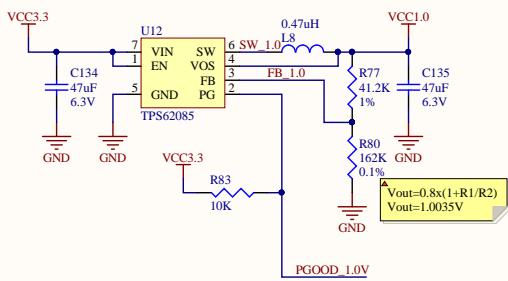


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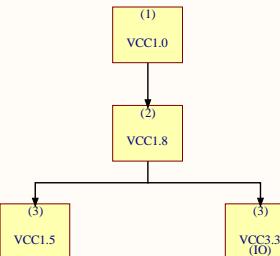


Based on AR8031/33 reference design:  
<http://wenku.baidu.com/view/d27bd2d8998fcc22bcd10d8e.html>  
And, AR8035 1.8V design found online:  
[http://riverparkinc.com/wp-content/uploads/2015/01/HAPS1\\_SERVICE\\_MANUAL.pdf](http://riverparkinc.com/wp-content/uploads/2015/01/HAPS1_SERVICE_MANUAL.pdf)

Description		Description	Univ. Wisconsin-Madison Madison, WI 53706	Cannot open file \cernchdfs\Users\m mpv\Desktop\Uw-ma
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Size: A3		Number: *	Revision revA	
Date: 21/02/2017		Time: 16:30:42	Sheet * of *	
File: Ethernet.SchDoc				Author: Vicente, M., Gorski, T., Tikalsky, J.

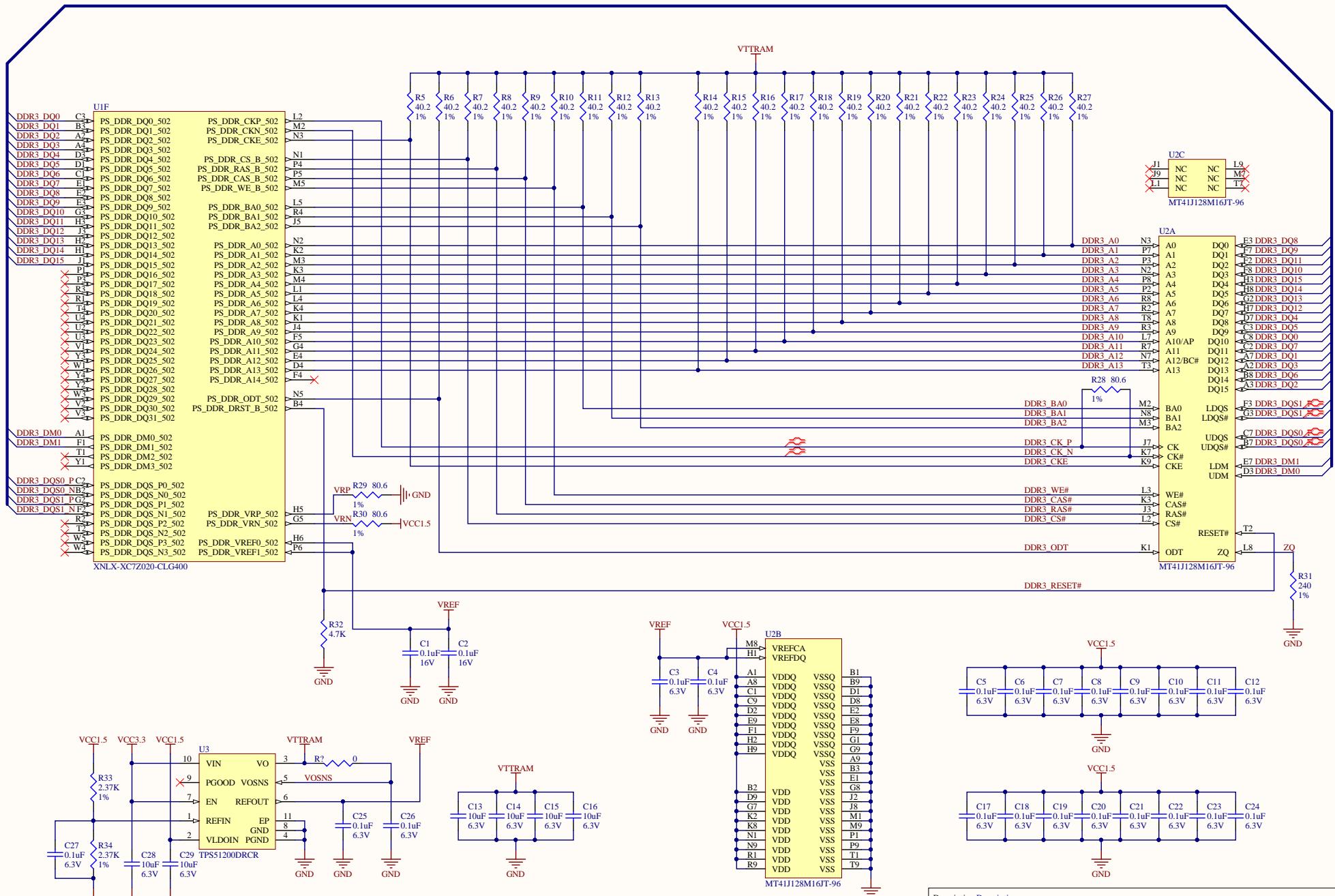


## Power sequence for Zynq

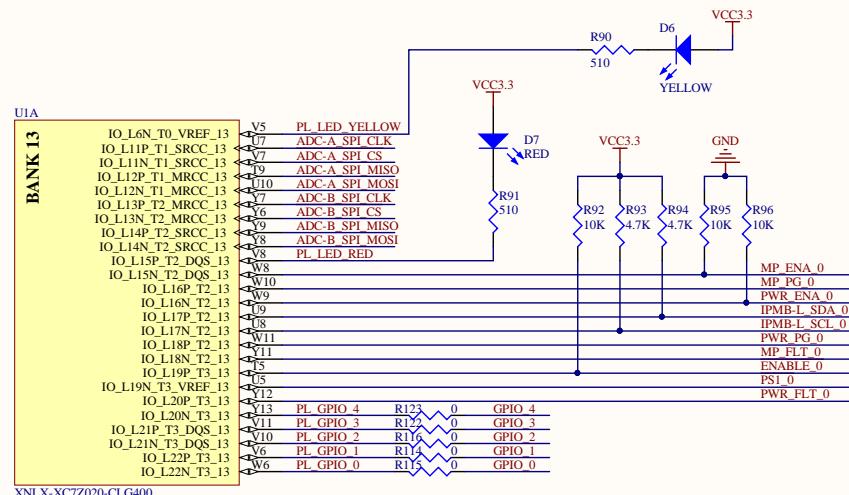


LDO converters are interchangeable with the following components:  
ADP1753 (0.8A) and ADP1741 (2.0A)

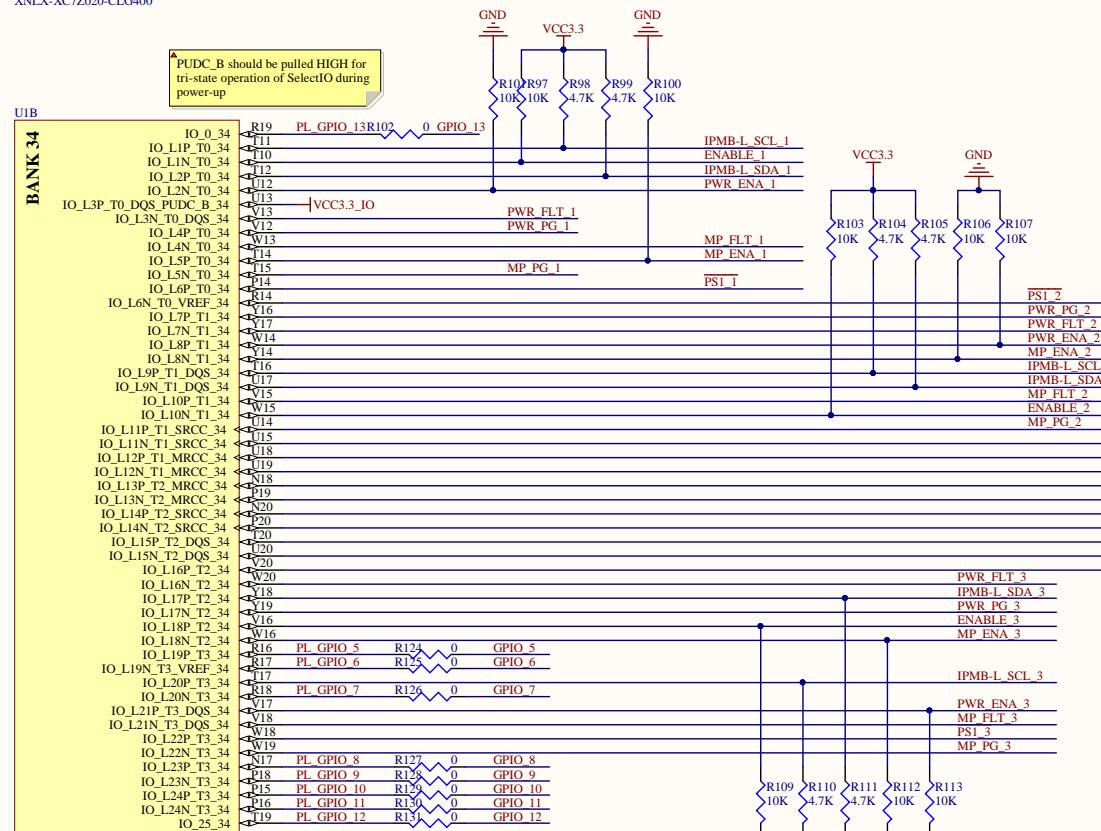
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Date:	21/02/2017
File:	PowerSequence_SchDoc
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Time:	16:30:42
Sheet:	* of *
Revision:	revA
Author:	Vicente, M., Gorski, T., Tikalsky, J.
	Univ. Wisconsin-Madison Madison, WI 53706
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Description	Description
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Date:	21/02/2017
Time:	16:30:42
File:	ZynqDDR.SchDoc
Author:	Vicente, M., Gorski, T., Tikalsky, J.
Rev:	revA
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Univ. Wisconsin-Madison Madison, WI 53706	Cannot open file \cern.ch\dfs\Users\nmpv\Desktop\Uw-ma

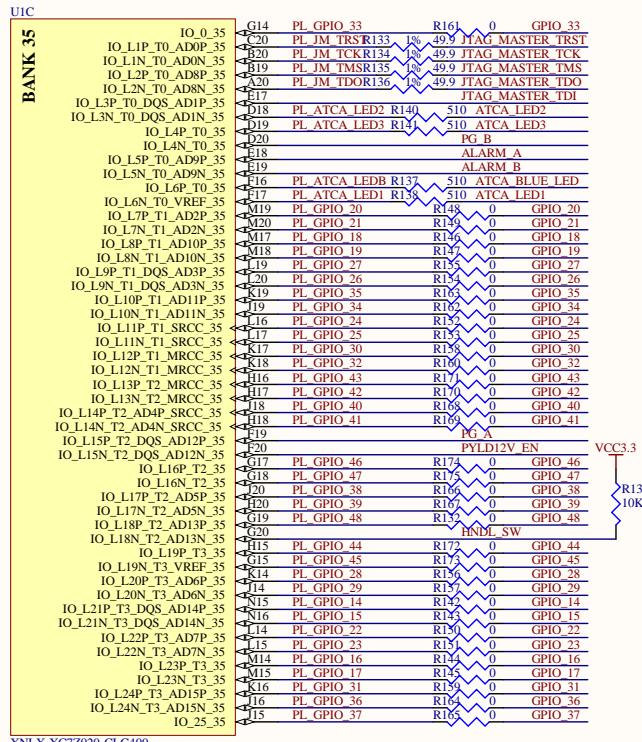


XNLX-XC7Z020-CLG40



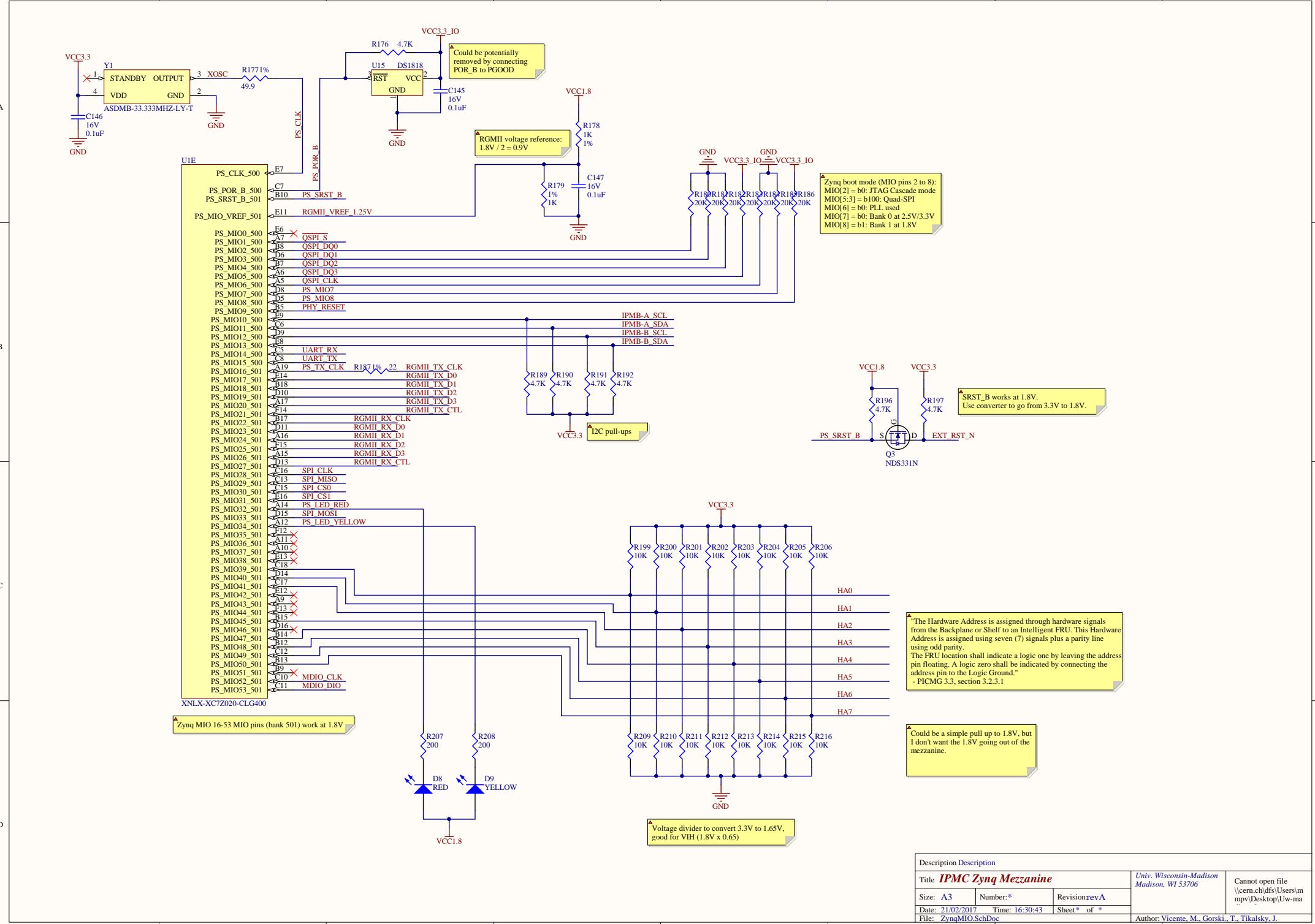
XNLX-XC7Z020-CLG40

Description	Description
Title: <b>IPMC Zynq Mezzanine</b>	Univ. Wisconsin-Madison Madison, WI 53706
Size: A3	Number: * Revision revA
Date: 21/02/2017	Time: 16:30:43 Sheet * of *
File: ZyneMeMIO.SchDoc	Author: Vicente, M., Gorski, T., Tikalsky, J.
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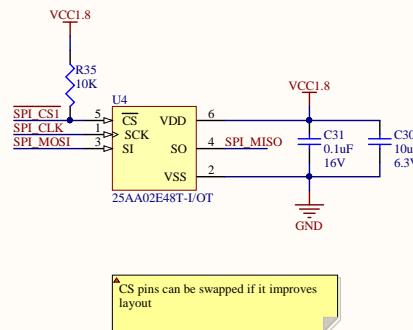
▲ For the handle switch (HNDL\_SW):  
 "Provide a right-angle 3-pin header, such as a Molex 53780-0390 or equivalent, to connect to a Face Plate-mounted microswitch within 25 mm of the lower recommended Component Side 2 keepout zone shown in Figure D-2, "PICMG 3.0 R1.0 overall Handle design." Pin 1 is the COMMON connection, Pin 2 is the NC (Normally Closed) contact, and Pin 3 is the NO (Normally Open) contact. Note: Front Board vendors need to ensure that they maintain the necessary Creepage and Clearance distances to any metal connected to Shelf Ground." - PICMG 3.0 R3.0, D.1.1

Description		Description	
<b>Title</b> <i>IPMC Zynq Mezzanine</i>		<i>Univ. Wisconsin-Madison Madison, WI 53706</i>	
Size: A3	Number: *	Revision: revA	Cannot open file \\cernchdfs\\Users\\mmpv\\Desktop\\Uw-ma
Date: 21/02/2017	Time: 16:30:43	Sheet: * of *	
File: ZynqEMIO_2.SchDoc			Author: Vicente, M., Gorski, T., Tikalsky, J.



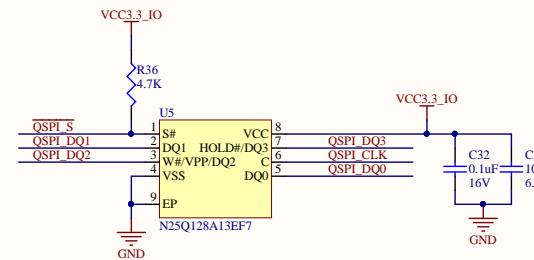
A

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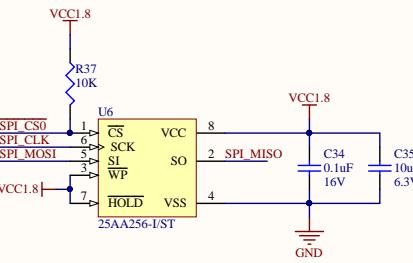
B



QSPI has 16MBytes  
Needs 50ohm lines  
C should be pulled LOW, but there is already the Zynq strap-pins.  
40 MHz is the max speed allowed due to the hold times imposed by Zynq.  
Check ZC702 schematic for more details.

C

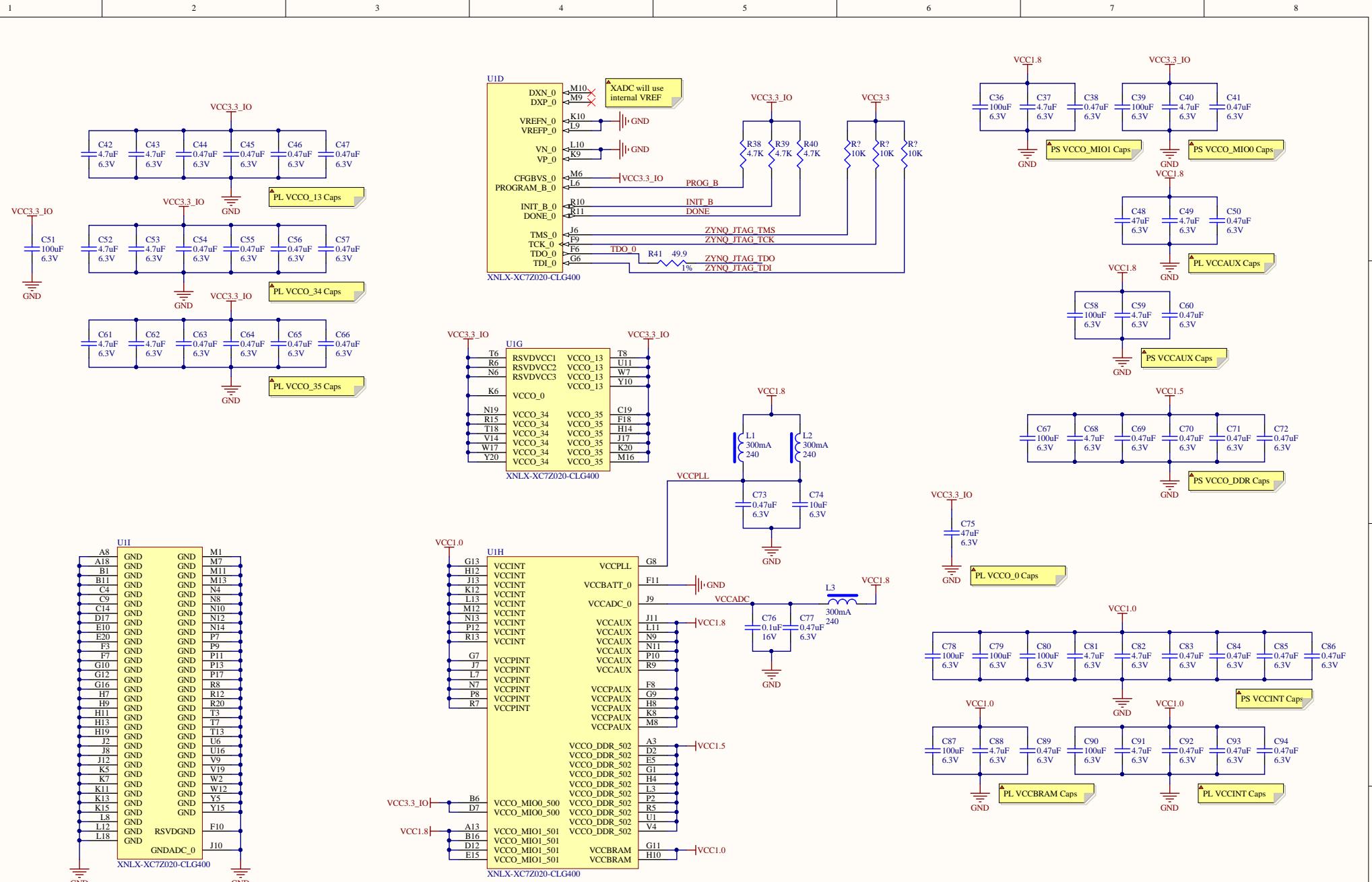
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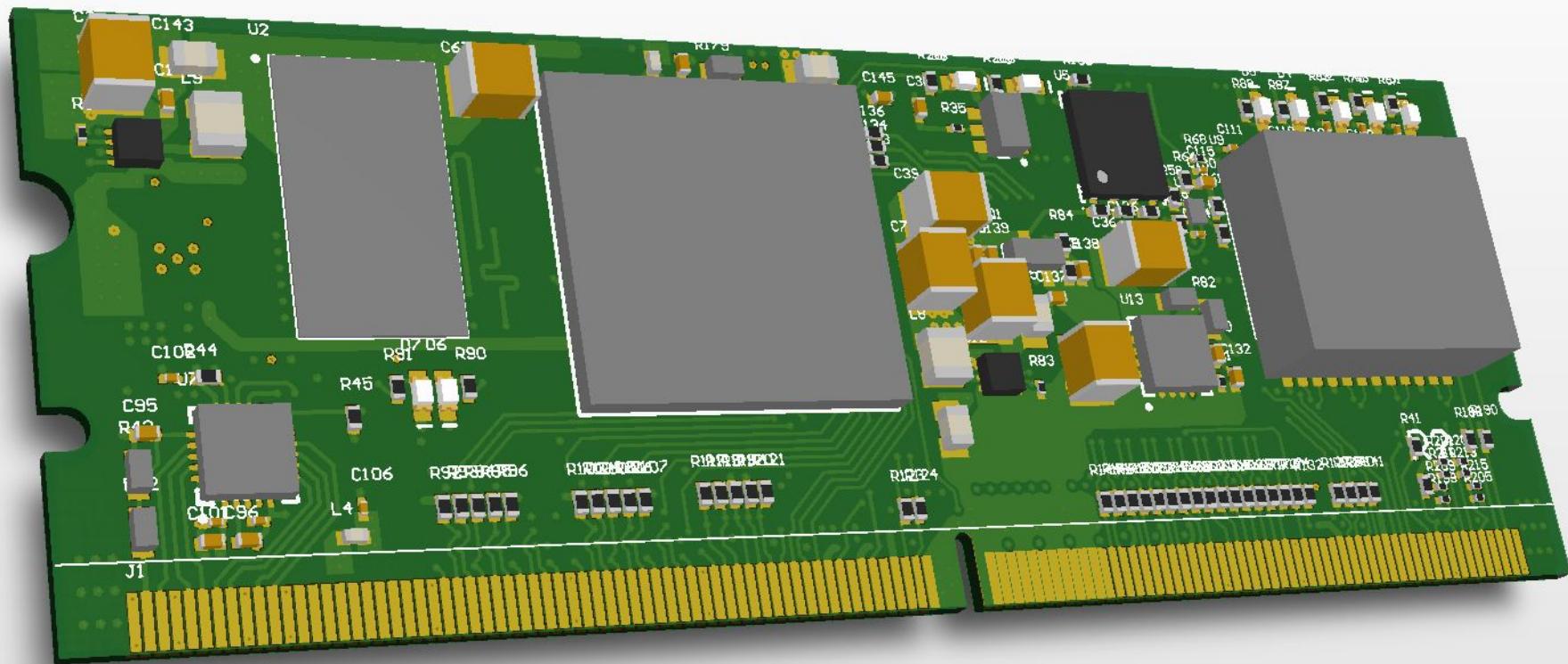
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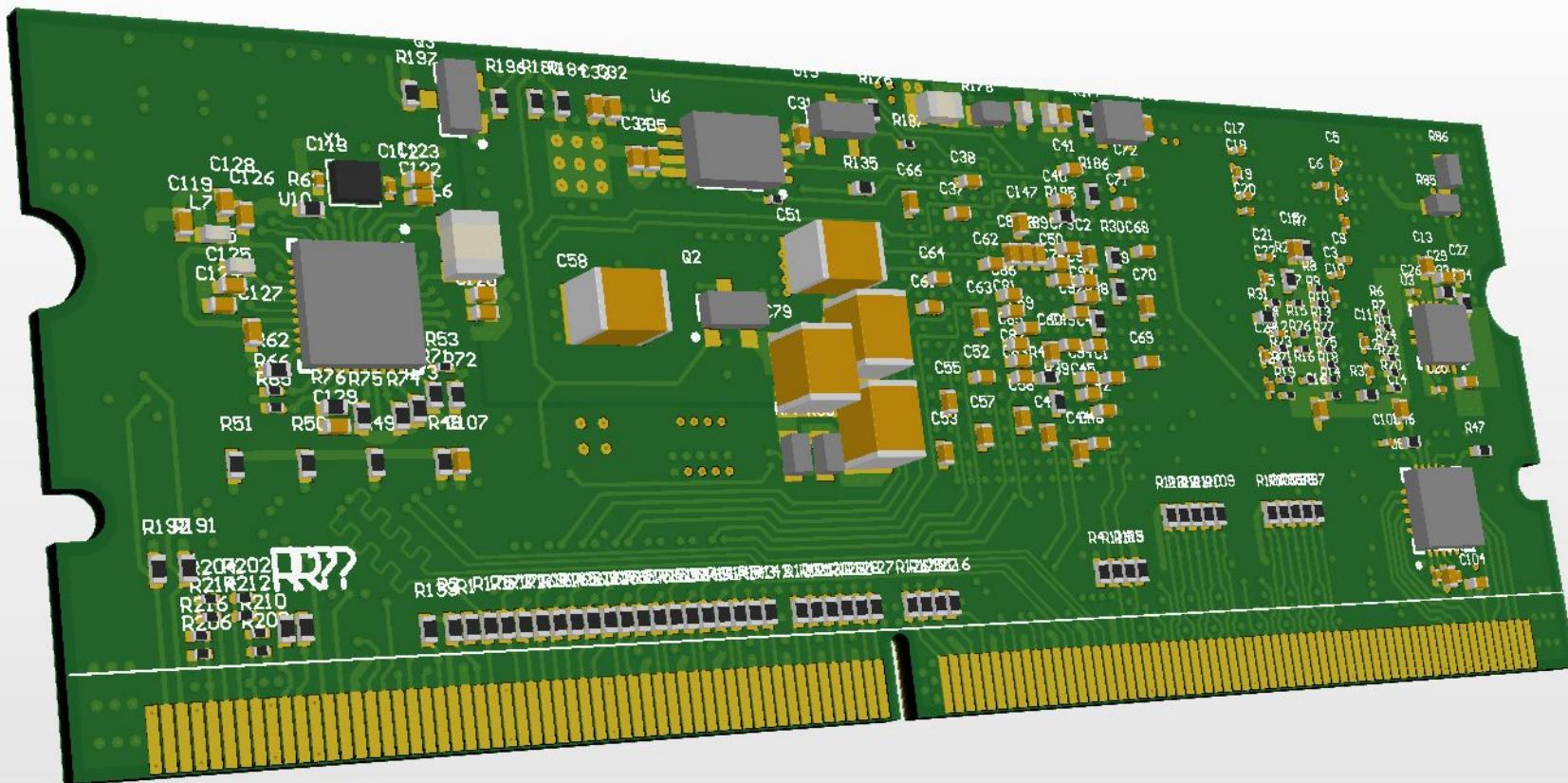
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Description	Description	Univ. Wisconsin-Madison Madison, WI 53706	Cannot open file \\cernchdfs\Users\mmpv\Desktop\Uw-ma
Title	<b>IPMC Zynq Mezzanine</b>		
Size:	A3	Number:*	Revision revA
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File:	ZynqPeripherals.SchDoc		Author: Vicente, M., Gorski, T., Tikalsky, J.

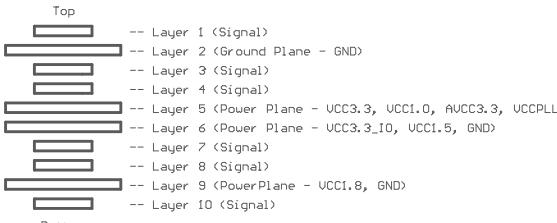


Description	Description		
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Size:	A3	Number: * Revision: revA	
Date:	21/02/2017	Time: 16:30:43	Sheet * of *
File:	ZynqPower.SchDoc	Author:	Vicente, M., Gorski, T., Tikhaisky, J.



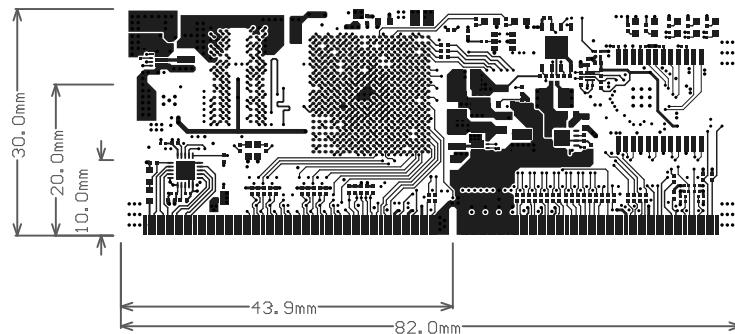


## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.6mm  $\pm$  0.16mm
3. Controlled impedance: Impedance Control Not Required
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
  - a. Hole diameters are given as after plating  $\pm$  3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All holes are exposed
  - d. Drill locations are partitioned into 3 separate drill files:
    - \* Plated-thru holes
    - \* Non-Plated-through holes
    - \* Plated slots
6. Finish: immersion gold
7. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
8. Solder Mask (SMBC) to be applied to both top and bottom sides.
9. Solder mask thickness to be no less than 3 mils
10. Layers 3 and 4 are power planes and are INERTED
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
13. Combination of board and twist shall not exceed 10 mils/inch along any direction
14. Design origin is at the bottom-left corner of the PCB
15. Optical inspection:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
  - c. DC resistance shall be 10 ohms or less
16. Locations in IPC-D-356A file are given in 2.4 English units
17. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
- x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:
  - Internal layers (3, 4, 7, 8):
    - 40 Ohms 6 mil tracks in artwork
    - 50 Ohms 4.5 mil tracks in artwork
    - 100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
  - External Layers (1 and 10):
    - 40 Ohms 9.5 mil tracks in artwork
    - 50 Ohms 7.5 mil tracks in artwork
    - 100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm$  10%. All other track widths in the artwork are given as before-etching.

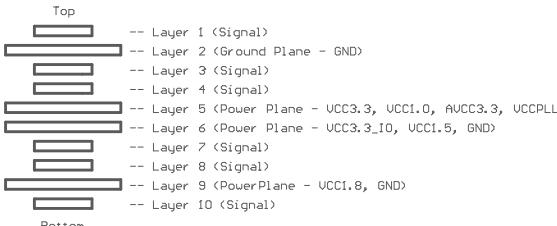


**UW IPMC ZYNQ MEZZANINE**  
Layer 1 - Signal (Copper)

Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 10AUG2016	PART NO.:	REV: revA
FILE NAME: UW_SAM4N_MMCI_DevBoard	DWG NO.:	SCALE: 1:1

## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.6mm  $\pm$  0.16mm
3. Controlled impedance: Impedance Control Not Required
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
  - a. Hole diameters are given as after plating  $\pm$  3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All holes are exposed
  - d. Drill locations are partitioned into 3 separate drill files:
    - \* Plated-thru holes
    - \* Non-Plated-through holes
    - \* Plated slots
6. Finish: immersion gold
7. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
8. Solder Mask (SMBC) to be applied to both top and bottom sides.
9. Layers 3 and 4 are power planes and are INERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
12. Combination of board and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
  - c. Resistance between planes, and non-connected plated through holes and vias shall be 10 Megohms or larger
15. Locations in IPC-D-356A file are given in 2.4 English units
16. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
17. Mechanical layer 2 corresponds to the board outline and layer 16 to the fab drawings.
- x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:
  - Internal layers (3, 4, 7, 8):
    - 40 Ohms 6 mil tracks in artwork
    - 50 Ohms 4.5 mil tracks in artwork
    - 100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
  - External Layers (1 and 10):
    - 40 Ohms 9.5 mil tracks in artwork
    - 50 Ohms 7.5 mil tracks in artwork
    - 100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm$  10%. All other track widths in the artwork are given as before-etching.



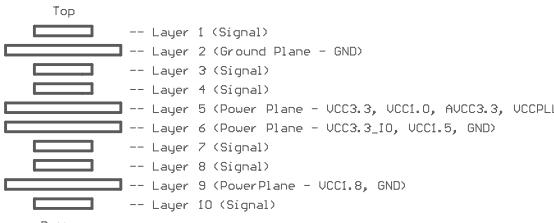
**UW IPMC ZYNQ MEZZANINE**

**Layer 2 - Ground Plane (Copper, Mask)**

Univ. of Wisconsin-Madison  
Madison, WI 53706

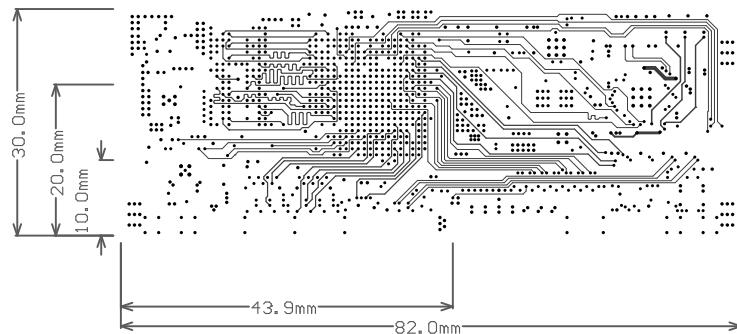
ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 10AUG2016	PART NO.:	REV: revA
FILE NAME: UW_SAM4N_MMCI_DevBoard	DWG NO.:	SCALE: 1:1

## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.6mm  $\pm$  0.16mm
3. Controlled impedance: Impedance Control Not Required
4. All layers use 1/2 oz. copper (before plating)
5. Holes:  
  - a. Hole diameters are given as after plating  $\pm$  3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All holes are exposed
  - d. Drill locations are partitioned into 3 separate drill files:
    - \* Plated-thru-holes
    - \* Non-Plated-through holes
    - \* Plated slots
6. Finish: immersion gold
7. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
8. Solder Mask (SMBC) to be applied to both top and bottom sides.
9. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
10. Layers 3 and 4 are power planes and are INERTED
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
12. Combination of board and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:  
  - a. All layers will undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
  - c. DC resistance shall be 10 ohms or less
15. Locations in IPC-D-356A file are given in 2.4 English units
16. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
17. Mechanical layer 2 corresponds to the board outline and layer 16 to the fab drawings.
- x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:  
  - Internal layers (3, 4, 7, 8):  
 40 Ohms 6 mil tracks in artwork  
 50 Ohms 4.5 mil tracks in artwork  
 100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
  - External Layers (1 and 10):  
 40 Ohms 9.5 mil tracks in artwork  
 50 Ohms 7.5 mil tracks in artwork  
 100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm$  10%. All other track widths in the artwork are given as before-etching.



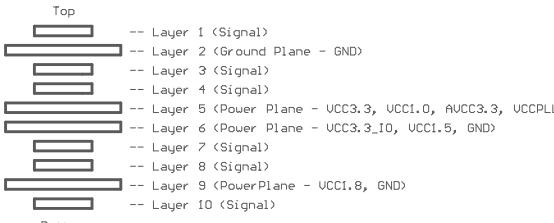
## UW IPMC ZYNQ MEZZANINE

### Layer 3 - Signal (Copper)

Univ. of Wisconsin-Madison  
Madison, WI 53706

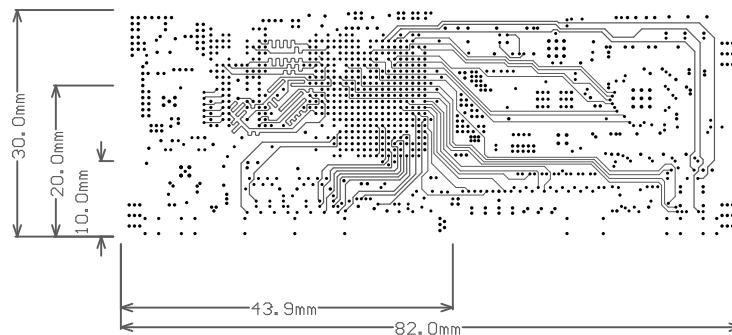
ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 10AUG2016	PART NO.:	REV: revA
FILE NAME: UW_SAM4N_MMCI_DevBoard	DWG NO.:	SCALE: 1:1

## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.6mm  $\pm$  0.16mm
3. Controlled impedance: Impedance Control Not Required
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
  - a. Hole diameters are given as after plating  $\pm$  3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All holes are exposed
  - d. Drill locations are partitioned into 3 separate drill files:
    - \* Plated-thru holes
    - \* Non-Plated-through holes
    - \* Plated slots
6. Finish: immersion gold
7. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
8. Solder Mask (SMBC) to be applied to both top and bottom sides.
9. Layers 3 and 4 are power planes and are INERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
12. Combination of board and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
15. Locations in IPC-D-356A file are given in 2.4 English units
16. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
17. Mechanical layer 2 corresponds to the board outline and layer 16 to the fab drawings.
- x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:
  - Internal layers (3, 4, 7, 8):
    - 40 Ohms 6 mil tracks in artwork
    - 50 Ohms 4.5 mil tracks in artwork
    - 100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
  - External Layers (1 and 10):
    - 40 Ohms 9.5 mil tracks in artwork
    - 50 Ohms 7.5 mil tracks in artwork
    - 100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm$  10%. All other track widths in the artwork are given as before-etching.



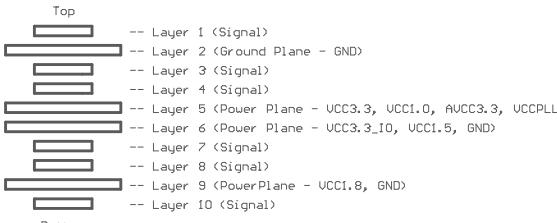
**UW IPMC ZYNQ MEZZANINE**

**Layer 4 - Signal (Copper)**

Univ. of Wisconsin-Madison  
Madison, WI 53706

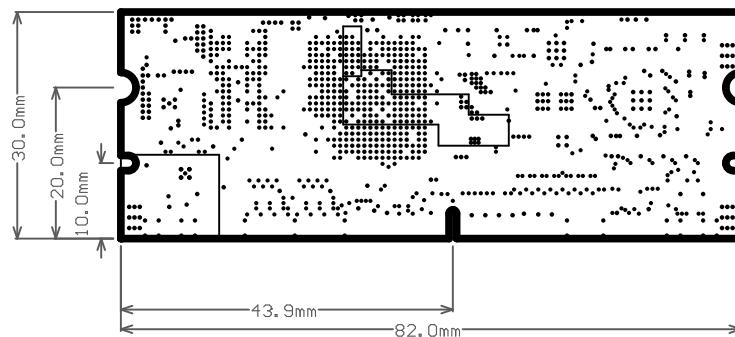
ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 10AUG2016	PART NO.:	REV: revA
FILE NAME: UW_SAM4N_MMCI_DevBoard	DWG NO.:	SCALE: 1:1

## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.6mm  $\pm$  0.16mm
3. Controlled impedance: Impedance Control Not Required
4. All layers use 1/2 oz. copper (before plating)
  - a. Hole diameters are given as after plating  $\pm$  3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All holes are exposed
  - d. Drill locations are partitioned into 3 separate drill files:
    - \* Plated-thru-holes
    - \* Non-Plated-through holes
    - \* Plated slots
5. Finish: immersion gold
6. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
7. Solder Mask (SMBC) to be applied to both top and bottom sides.
8. SMA pads to be placed on top and bottom layers with a pitch of 3 mils
9. Layers 3 and 4 are power planes and are INSERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
12. Combination of board and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
15. Locations in IPC-D-356A file are given in 2.4 English units
16. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
17. Mechanical layer 2 corresponds to the board outline and layer 16 to the fab drawings.
- x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:
  - Internal layers (3, 4, 7, 8):
    - 40 Ohms 6 mil tracks in artwork
    - 50 Ohms 4.5 mil tracks in artwork
    - 100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
  - External Layers (1 and 10):
    - 40 Ohms 9.5 mil tracks in artwork
    - 50 Ohms 7.5 mil tracks in artwork
    - 100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm$  10%. All other track widths in the artwork are given as before-etching.



UW IPMC ZYNQ MEZZANINE

Layer 5 - Power Plane (Copper, Mask)

Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER:  
Vicente, M., Gorski, T., Tikalsky, J.

PCB DESIGNER:  
Vicente, M.

DATE:  
10AUG2016

FILE NAME:  
UW\_SAM4N\_MMCI\_DevBoard

TITLE:  
UW IPMC Zynq Module

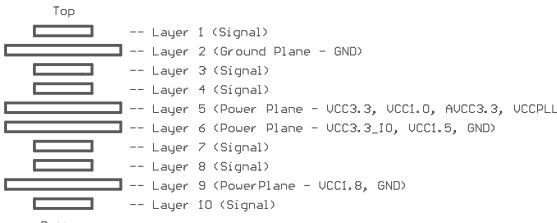
PART NO:

REV:  
revA

DWG NO:

SCALE:  
1:1

## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
  2. Overall thickness is 1.6mm  $\pm$  0.16mm
  3. Controlled impedance: Impedance Control Not Required
  4. All layers use 1/2 oz. copper (before plating)
  5. Holes:
    - a. Hole diameters are given as after plating  $\pm$  3mils, except as noted on drill drawing
    - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
    - c. All holes are exposed
    - d. Drill locations are partitioned into 3 separate drill files:
      - \* Plated-thru-holes
      - \* Non-Plated-through holes
      - \* Plated slots
  6. Finish: immersion gold
  7. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
  8. Solder Mask (SMBC) to be applied to both top and bottom sides.
  9. Solder mask thickness shall be 1 mil with a tolerance of 3 mils
  10. Layers 3 and 4 are power planes and are INSERTED
  11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
  12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
  13. Combination of board and twist shall not exceed 10 mils/inch along any direction
  14. Design origin is at the bottom-left corner of the PCB
  15. Optical inspection:
    - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
    - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
    - c. DC resistance shall be 10 ohms or less
  16. Locations in IPC-D-356A file are given in 2.4 English units
  17. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
  18. Mechanical layer 2 corresponds to the board outline and layer 16 to the fab drawings.
  - x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):
40 Ohms 6 mil tracks in artwork
50 Ohms 4.5 mil tracks in artwork
100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
External Layers (1 and 10):
40 Ohms 9.5 mil tracks in artwork
50 Ohms 7.5 mil tracks in artwork
100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm$  10%. All other track widths in the artwork are given as before-etching.



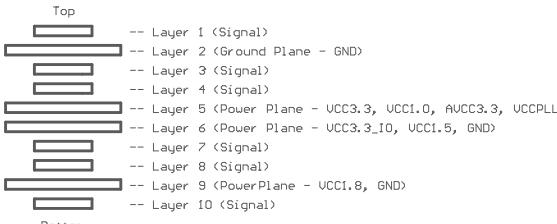
UW IPMC ZYNQ MEZZANINE

Layer 6 - Power Plane (Copper, Mask)

Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 10AUG2016	PART NO.:	REV: revA
FILE NAME: UW_SAM4N_MMCI_DevBoard	DWG NO.:	SCALE: 1:1

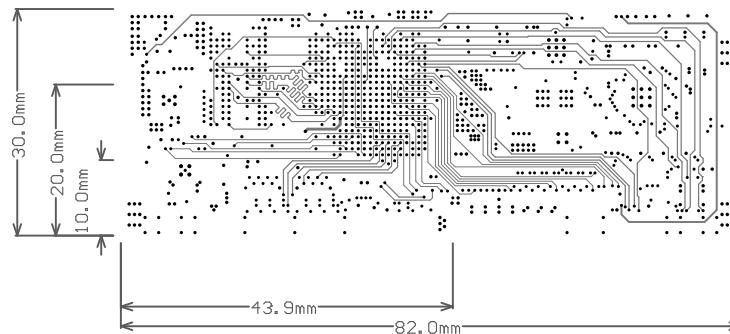
## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
  2. Overall thickness is 1.6mm  $\pm$  0.16mm
  3. Controlled impedance: Impedance Control Not Required
  4. All layers use 1/2 oz. copper (before plating)
  5. Holes:
    - a. Hole diameters are given as after plating  $\pm$  3mils, except as noted on drill drawing
    - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
    - c. All holes are exposed
    - d. Drill locations are partitioned into 3 separate drill files:
      - \* Plated-thru-holes
      - \* Non-Plated-through holes
      - \* Plated slots
  6. Finish: immersion gold
  7. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
  8. Solder Mask (SMBC) to be applied to both top and bottom sides.
  9. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
  10. Layers 3 and 4 are power planes and are INSERTED
  11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
  12. Combination of board and twist shall not exceed 10 mils/inch along any direction
  13. Design origin is at the bottom-left corner of the PCB
  14. DRILLING:
    - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
    - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
    - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
  15. Locations in IPC-D-356A file are given in 2.4 English units
  16. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
  17. Mechanical layer 2 corresponds to the board outline and layer 16 to the fab drawings.
  - x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):
40 Ohms 6 mil tracks in artwork
50 Ohms 4.5 mil tracks in artwork
100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
External Layers (1 and 10):
40 Ohms 9.5 mil tracks in artwork
50 Ohms 7.5 mil tracks in artwork
100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm$  10%. All other track widths in the artwork are given as before-etching.



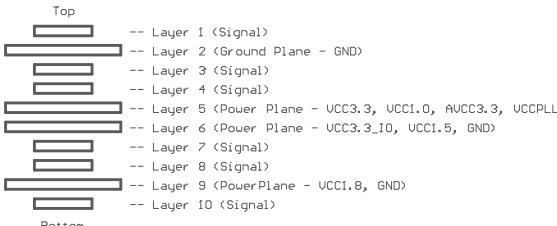
UW IPMC ZYNQ MEZZANINE

Layer 7 - Signal (Copper)

Univ. of Wisconsin-Madison  
Madison, WI 53706

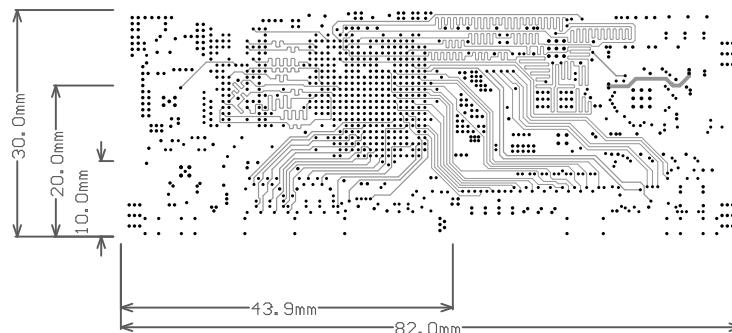
ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 10AUG2016	PART NO.:	REV: revA
FILE NAME: UW_SAM4N_MMCI_DevBoard	DWG NO.:	SCALE: 1:1

## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
  2. Overall thickness is 1.6mm  $\pm$  0.16mm
  3. Controlled impedance: Impedance Control Not Required
  4. All layers use 1/2 oz. copper (before plating)
    - a. Hole diameters are given as after plating  $\pm$  3mils, except as noted on drill drawing
    - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
    - c. All holes are exposed
    - d. Drill locations are partitioned into 3 separate drill files:
      - \* Plated-thru-holes
      - \* Non-Plated-through holes
      - \* Plated slots
  5. Finish: immersion gold
  6. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
  7. Solder Mask (SMBC) to be applied to both top and bottom sides.
  8. Board shall be built with a board thickness of 3 mils
  9. Layers 3 and 4 are power planes and are INERTED
  10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
  11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
  12. Combination of board and twist shall not exceed 10 mils/inch along any direction
  13. Design origin is at the bottom-left corner of the PCB
  14. Testing:
    - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
    - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
    - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
  15. Locations in IPC-D-356A file are given in 2.4 English units
  16. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
  17. Mechanical layer 2 corresponds to the board outline and layer 16 to the fab drawings.
  - x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:
    - Internal layers (3, 4, 7, 8):
      - 40 Ohms 6 mil tracks in artwork
      - 50 Ohms 4.5 mil tracks in artwork
      - 100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
    - External Layers (1 and 10):
      - 40 Ohms 9.5 mil tracks in artwork
      - 50 Ohms 7.5 mil tracks in artwork
      - 100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm$  10%. All other track widths in the artwork are given as before-etching.



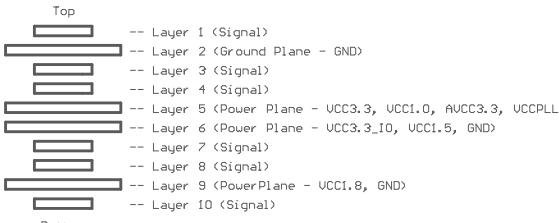
UW IPMC ZYNQ MEZZANINE

Layer 8 - Signal (Copper)

Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 10AUG2016	PART NO.:	REV: revA
FILE NAME: UW_SAM4N_MMCI_DevBoard	DWG NO.:	SCALE: 1:1

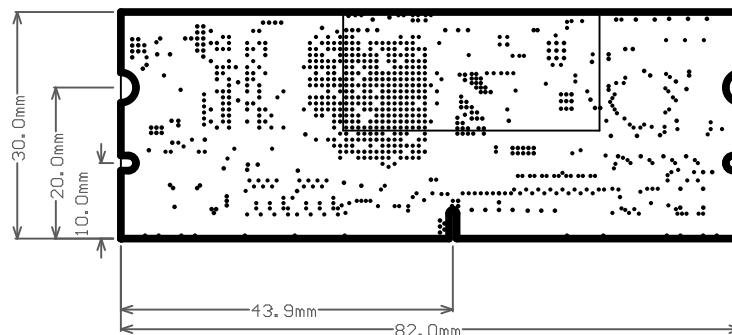
## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
  2. Overall thickness is 1.6mm  $\pm$  0.16mm
  3. Controlled impedance: Impedance Control Not Required
  4. All layers use 1/2 oz. copper (before plating)
  5. Holes:
    - a. Hole diameters are given as after plating  $\pm$  3mils, except as noted on drill drawing
    - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
    - c. All holes are exposed
    - d. Drill locations are partitioned into 3 separate drill files:
      - \* Plated-thru-holes
      - \* Non-Plated-through holes
      - \* Plated slots
  6. Finish: Immersion gold
  7. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
  8. Solder Mask (SMBC) to be applied to both top and bottom sides.
  9. Layers 3 and 4 are power planes and are INSERTED
  10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
  11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
  12. Combination of board and twist shall not exceed 10 mils/inch along any direction
  13. Design origin is at the bottom-left corner of the PCB
  14. Testing:
    - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
    - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
    - c. DC resistance shall be 10 ohms or less
  15. Locations in IPC-D-356A file are given in 2.4 English units
  16. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
  17. Mechanical layer 2 corresponds to the board outline and layer 16 to the fab drawings.
  - x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):
40 Ohms: 6 mil tracks in artwork
50 Ohms: 4.5 mil tracks in artwork
100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
External Layers (1 and 10):
40 Ohms: 9.5 mil tracks in artwork
50 Ohms: 7.5 mil tracks in artwork
100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm$  10%. All other track widths in the artwork are given as before-etching.



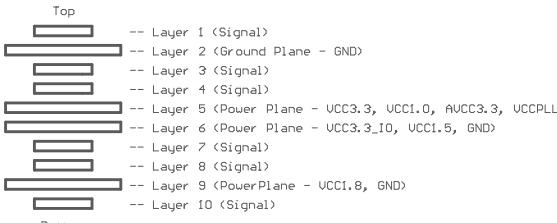
UW IPMC ZYNQ MEZZANINE

Layer 9 - Power Plane (Copper, Mask)

Univ. of Wisconsin-Madison  
Madison, WI 53706

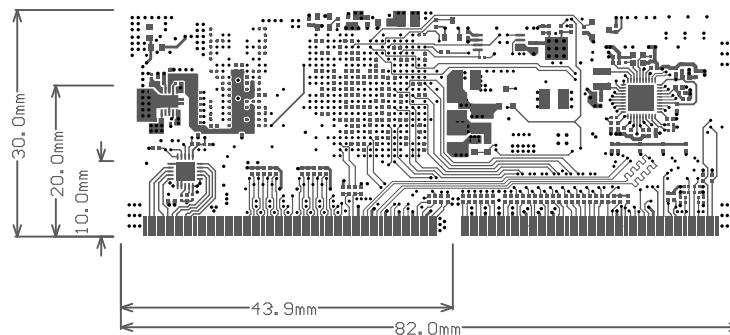
ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 10AUG2016	PART NO.:	REV: revA
FILE NAME: UW_SAM4N_MMCI_DevBoard	DWG NO.:	SCALE: 1:1

## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.6mm +/- 0.16mm
3. Controlled impedance: Impedance Control Not Required
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
  - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All holes are exposed
  - d. Drill locations are partitioned into 3 separate drill files:
    - \* Plated-thru holes
    - \* Non-Plated-through holes
    - \* Plated slots
6. Finish: immersion gold
7. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
8. Solder Mask (SMBC) to be applied to both top and bottom sides.
9. Board shall be manufactured with a thickness tolerance of 3 mils
10. Layers 3 and 4 are power planes and are INERTED
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
13. Combination of board and twist shall not exceed 10 mils/inch along any direction
14. Design origin is at the bottom-left corner of the PCB
15. Designing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
16. Locations in IPC-D-356A file are given in 2.4 English units
17. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
18. Mechanical layer 2 corresponds to the board outline and layer 16 to the fab drawings.
- x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:
  - Internal layers (3, 4, 7, 8):
    - 40 Ohms 6 mil tracks in artwork
    - 50 Ohms 4.5 mil tracks in artwork
    - 100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
  - External Layers (1 and 10):
    - 40 Ohms 9.5 mil tracks in artwork
    - 50 Ohms 7.5 mil tracks in artwork
    - 100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.



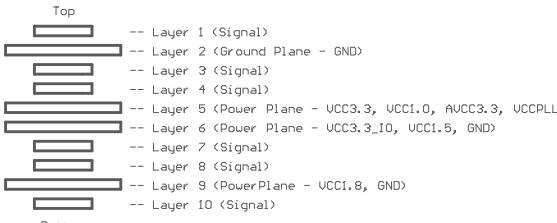
UW IPMC ZYNQ MEZZANINE

Layer 10 - Signal (Copper)

Univ. of Wisconsin-Madison  
Madison, WI 53706

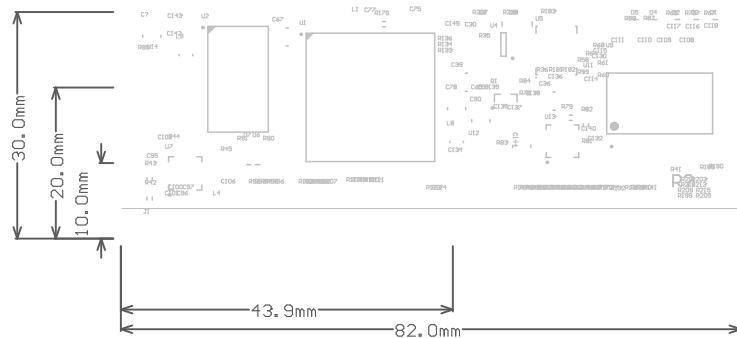
ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 10AUG2016	PART NO.:	REV: revA
FILE NAME: UW_SAM4N_MMCI_DevBoard	DWG NO.:	SCALE: 1:1

## Layer Stackup

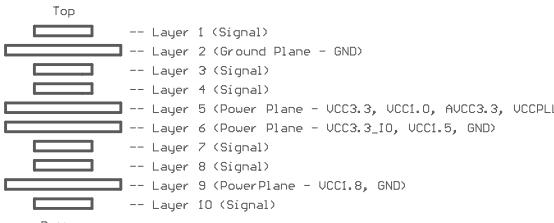


## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.6mm  $\pm$  0.16mm
3. Controlled impedance: Impedance Control Not Required
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
  - a. Hole diameters are given as after plating  $\pm$  3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All holes are exposed
  - d. Drill locations are partitioned into 3 separate drill files:
    - \* Plated-thru holes
    - \* Non-Plated-through holes
    - \* Plated slots
6. Finish: Immersion gold
7. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
8. Solder Mask (SMBC) to be applied to both top and bottom sides.
9. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
10. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (Class 2)
11. Combination of board and twist shall not exceed 10 mils/inch along any direction
12. Design origin is at the bottom-left corner of the PCB
13. Designing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
14. Locations in IPC-D-356A file are given in 2.4 English units
15. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
16. Mechanical layer 2 corresponds to the board outline and layer 16 to the fab drawings.
- x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:
  - Internal layers (3, 4, 7, 8):
    - 40 Ohms 6 mil tracks in artwork
    - 50 Ohms 4.5 mil tracks in artwork
    - 100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
  - External Layers (1 and 10):
    - 40 Ohms 9.5 mil tracks in artwork
    - 50 Ohms 7.5 mil tracks in artwork
    - 100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm$  10%. All other track widths in the artwork are given as before-etching.

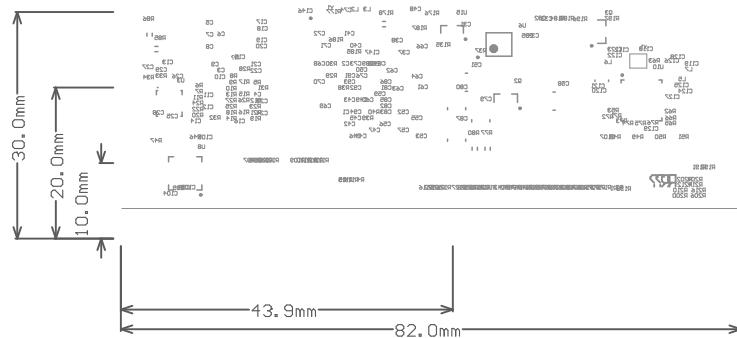


## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.6mm  $\pm$  0.16mm
3. Controlled impedance: Impedance Control Not Required
4. All layers use 1/2 oz. copper (before plating)
  - a. Hole diameters are given as after plating  $\pm$  3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All holes are exposed
  - d. Drill locations are partitioned into 3 separate drill files:
    - \* Plated-thru holes
    - \* Non-Plated-through holes
    - \* Plated slots
5. Finish: immersion gold
6. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
7. Solder Mask (SMBC) to be applied to both top and bottom sides.
8. Solder mask to be applied to all internal layers with a thickness of 3 mils
9. Layers 3 and 4 are power planes and are INSERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
12. Combination of board and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Optical inspection
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
15. Locations in IPC-D-356A file are given in 2.4 English units
16. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
17. Mechanical layer 2 corresponds to the board outline and layer 16 to the fab drawings.
- x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:
  - Internal layers (3, 4, 7, 8):
    - 40 Ohms 6 mil tracks in artwork
    - 50 Ohms 4.5 mil tracks in artwork
    - 100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
  - External Layers (1 and 10):
    - 40 Ohms 9.5 mil tracks in artwork
    - 50 Ohms 7.5 mil tracks in artwork
    - 100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm$  10%. All other track widths in the artwork are given as before-etching.



UW IPMC ZYNQ MEZZANINE

Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER:  
Vicente, M., Gorski, T., Tikalsky, J.

PCB DESIGNER:  
Vicente, M.

DATE:  
10AUG2016

FILE NAME:  
UW\_SAM4N\_MMC\_DevBoard

TITLE:  
UW IPMC Zynq Module

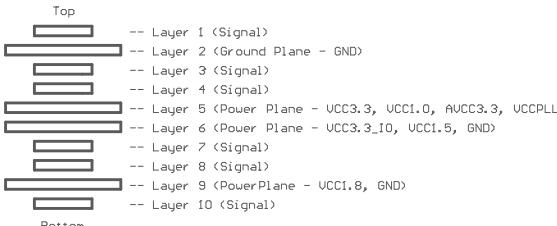
PART NO.:

REV:  
revA

DWG NO.:

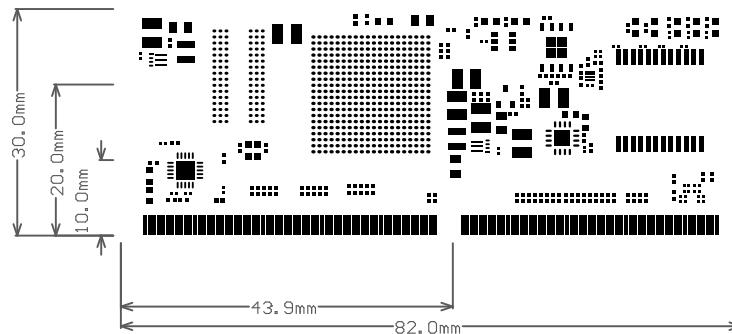
SCALE:  
1:1

## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.6mm  $\pm$  0.16mm
3. Controlled impedance: Impedance Control Not Required
4. All layers use 1/2 oz. copper (before plating)
5. Holes:  
  - a. Hole diameters are given as after plating  $\pm$  3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All holes are exposed
  - d. Drill locations are partitioned into 3 separate drill files:  
    - \* Plated-thru holes
    - \* Non-Plated-through holes
    - \* Plated slots
6. Finish: immersion gold
7. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
8. Solder Mask (SMBC) to be applied to both top and bottom sides.
9. Solder mask thickness to be 1 mil with a tolerance of 3 mils
10. Layers 3 and 4 are power planes and are INERTED
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
13. Combination of board and twist shall not exceed 10 mils/inch along any direction
14. Design origin is at the bottom-left corner of the PCB
15. Optical inspection:  
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
  - c. DC resistance shall be 10 ohms or less
16. Locations in IPC-D-356A file are given in 2.4 English units
17. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
- x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:  
  - Internal layers (3, 4, 7, 8):  
    - 40 Ohms 6 mil tracks in artwork
    - 50 Ohms 4.5 mil tracks in artwork
    - 100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
  - External Layers (1 and 10):  
    - 40 Ohms 9.5 mil tracks in artwork
    - 50 Ohms 7.5 mil tracks in artwork
    - 100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm$  10%. All other track widths in the artwork are given as before-etching.

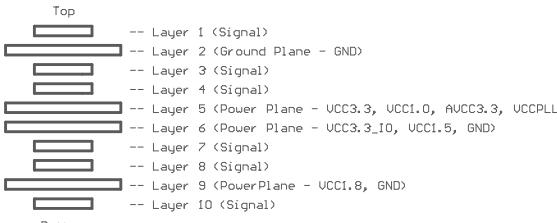


UW IPMC ZYNQ MEZZANINE

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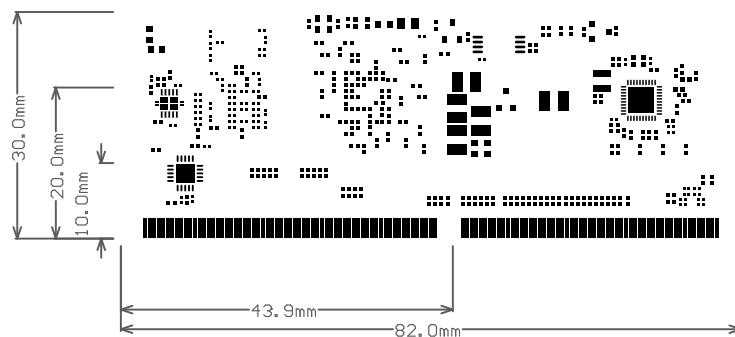
ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 10AUG2016	PART NO.:	REV: revA
FILE NAME: UW_SAM4N_MMCI_DevBoard	DWG NO.:	SCALE: 1:1

## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.6mm  $\pm$  0.16mm
3. Controlled impedance: Impedance Control Not Required
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
  - a. Hole diameters are given as after plating  $\pm$  3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All holes are exposed
  - d. Drill locations are partitioned into 3 separate drill files:
    - \* Plated-thru holes
    - \* Non-Plated-through holes
    - \* Plated slots
6. Finish: immersion gold
7. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
8. Solder Mask (SMBC) to be applied to both top and bottom sides.
9. Layers 3 and 4 are power planes and are INERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
12. Combination of board and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
15. Locations in IPC-D-356A file are given in 2.4 English units
16. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
17. Mechanical layer 2 corresponds to the board outline and layer 16 to the fab drawings.
- x. Impedance 40 and 50 ohm single-ended and 100 ohm differential traces on internal/external layers as follows:
  - Internal layers (3, 4, 7, 8):
    - 40 Ohms 6 mil tracks in artwork
    - 50 Ohms 4.5 mil tracks in artwork
    - 100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
  - External Layers (1 and 10):
    - 40 Ohms 9.5 mil tracks in artwork
    - 50 Ohms 7.5 mil tracks in artwork
    - 100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm$  10%. All other track widths in the artwork are given as before-etching.

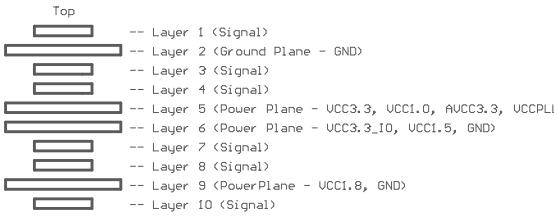


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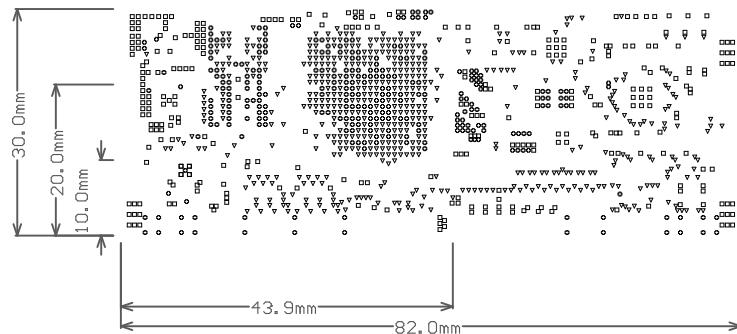
ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW IPMC Zynq Module	
PCB DESIGNER: Vicente, M.		
DATE: 10AUG2016	PART NO.:	REV: revA
FILE NAME: UW_SAM4N_MMCI_DevBoard	DWG NO.:	SCALE: 1:1

## Layer Stackup



## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.6mm +/- 0.16mm
3. Controlled impedance: Impedance Control Not Required
4. All layers use 1/2 oz. copper (before plating)
5. Holes:
  - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All holes are exposed
  - d. Drill locations are partitioned into 3 separate drill files:
    - \* Plated-thru holes
    - \* Non-Plated-through holes
    - \* Plated slots
6. Finish: immersion gold
7. Minimum observed signal layer clearances is 6 mils on layers 1, 2, 5 and 6
8. Solder Mask (SMBC) to be applied to both top and bottom sides.
9. Layers 3 and 4 are power planes and are INSERTED
10. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
11. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (Class 2)
12. Combination of board and twist shall not exceed 10 mils/inch along any direction
13. Design origin is at the bottom-left corner of the PCB
14. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data.
  - c. DC resistance shall be 10 ohms or less
15. Locations in IPC-D-356A file are given in 2.4 English units
16. Mechanical layers 29 and 30 correspond to top and bottom assembly part reference respectively.
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    - 100 Ohm, differential: 4.4 mil tracks with edge-to-edge separation in range of 5.45 to 6.05 mils.
  - External Layers (1 and 10):
    - 40 Ohms 9.5 mil tracks in artwork
    - 50 Ohms 7.5 mil tracks in artwork
    - 100 Ohm, differential: 5 mil tracks with 6mil edge-to-edge separation
- Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.



UW IPMC ZYNQ MEZZANINE

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length	Rout Path Length
◇	274	7.00mil (0.178mm)	PTH	Round	-	-
□	314	8.00mil (0.203mm)	PTH	Round	-	-
▽	529	6.00mil (0.152mm)	PTH	Round	-	-
1117 Total						

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ENGINEER:  
Vicente, M., Gorski, T., Tikalsky, J.

TITLE:  
UW IPMC Zynq Module

PCB DESIGNER:  
Vicente, M.

PART NO:

D

DATE:  
10AUG2016

REV:  
revA

FILE NAME:  
UW\_SAM4N\_MMCI\_DevBoard

DWG NO:

D