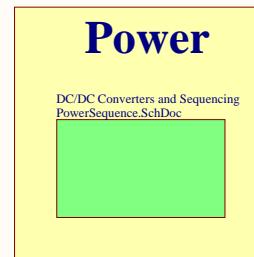
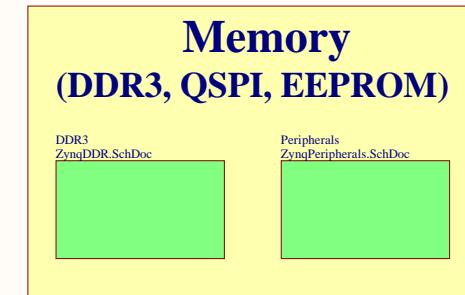
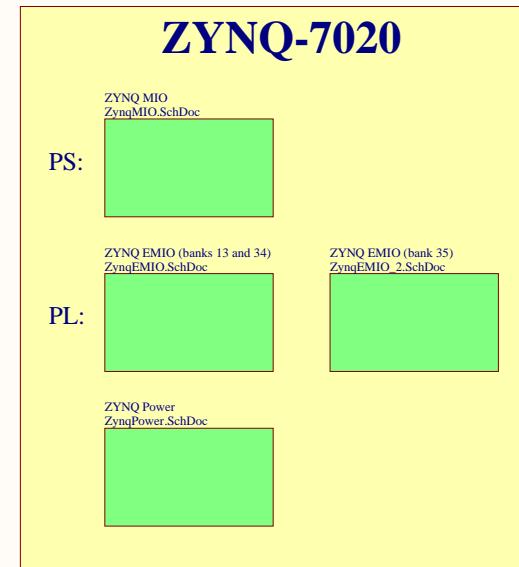
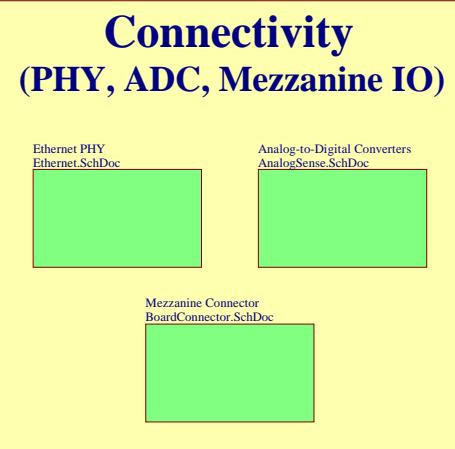


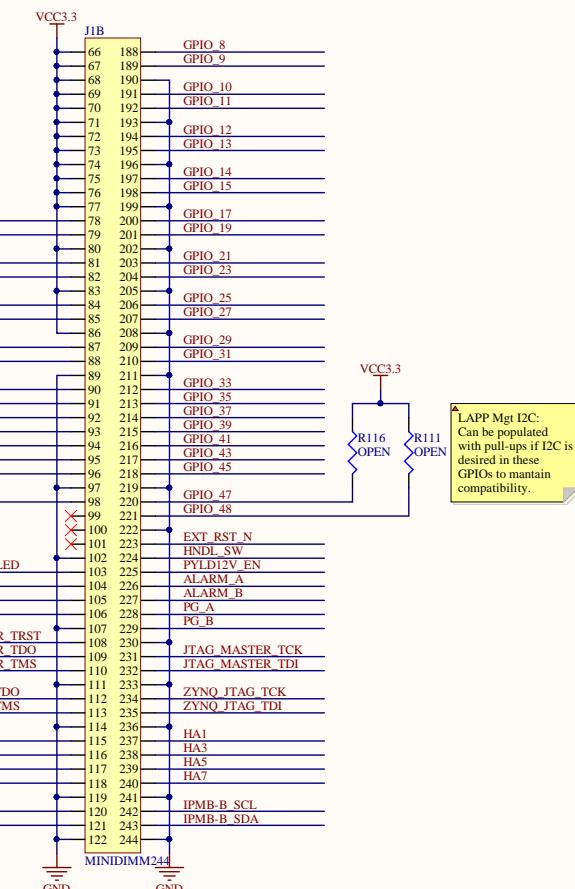
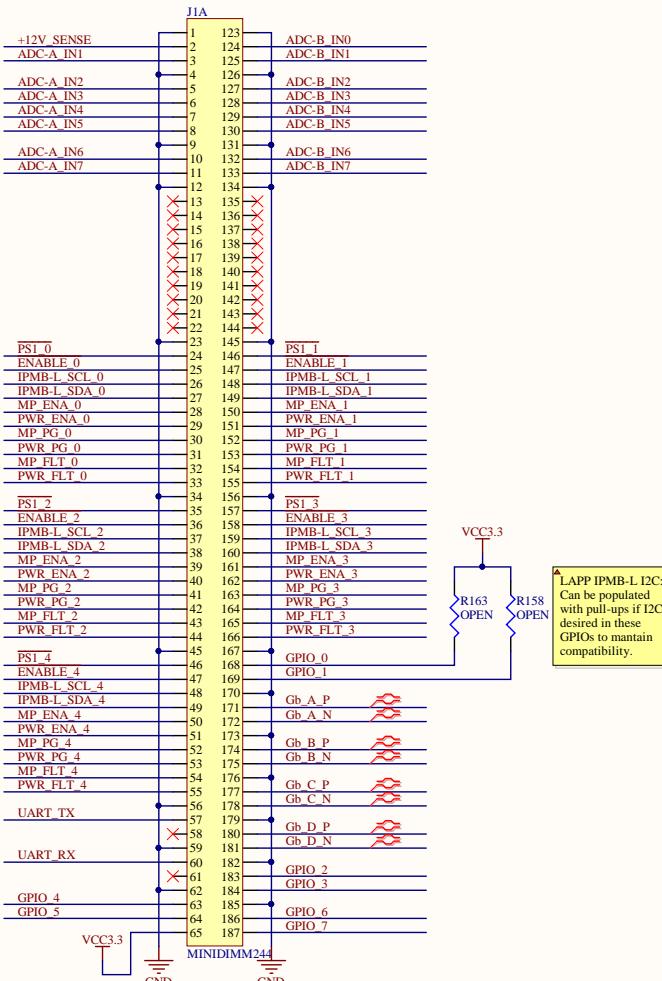
# UW-IPMC MEZZANINE (revA)



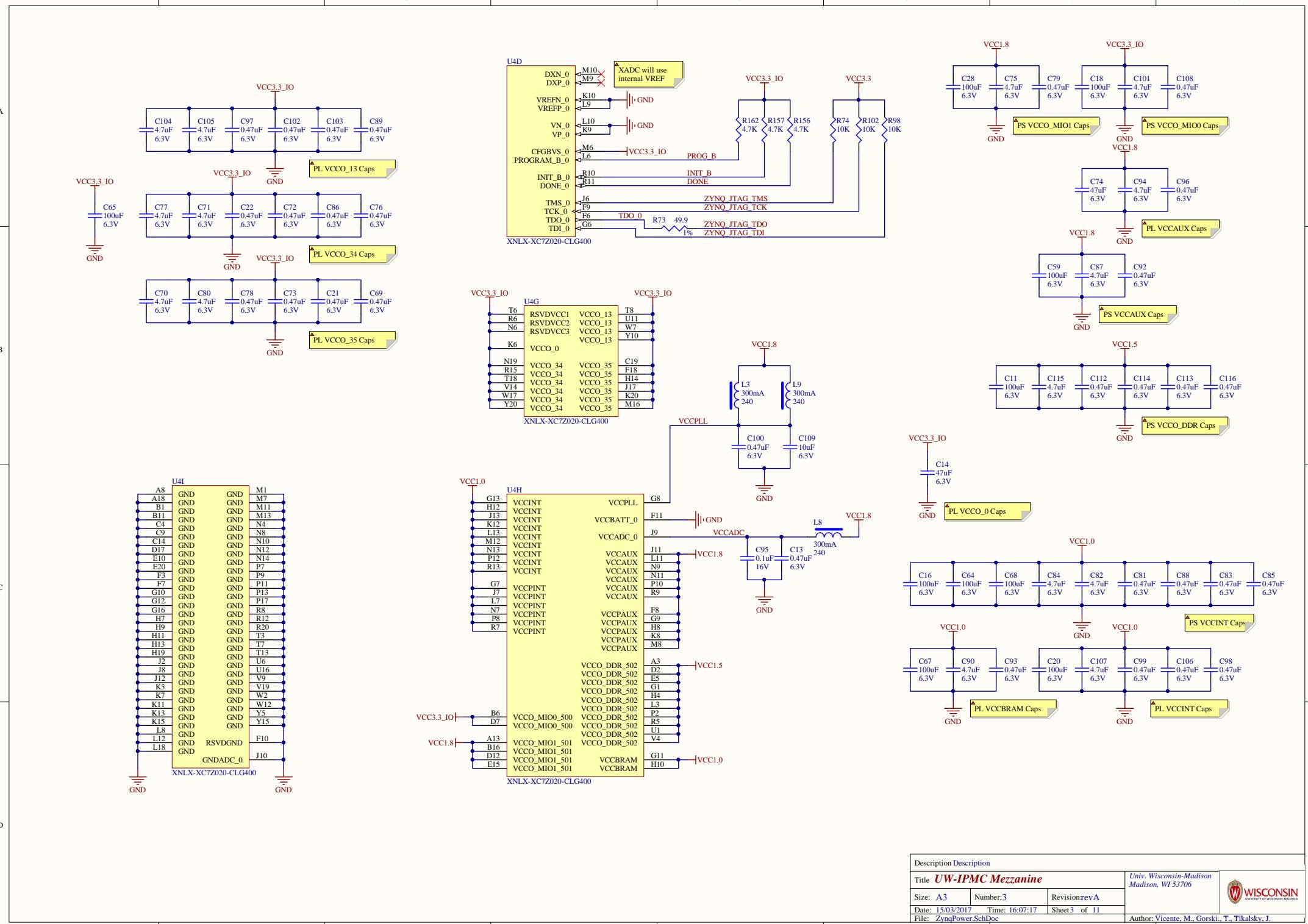
Description	Description			
Title	<b>UW-IPMC Mezzanine</b>	Univ. Wisconsin-Madison	Madison, WI 53706	
Size:	A3	Number:	1	Revision: revA
Date:	15/03/2017	Time:	16:07:17	Sheet 1 of 11
File:	IPMC.SchDoc	Author:	Vicente, M., Gorski, T., Tikalsky, J.	

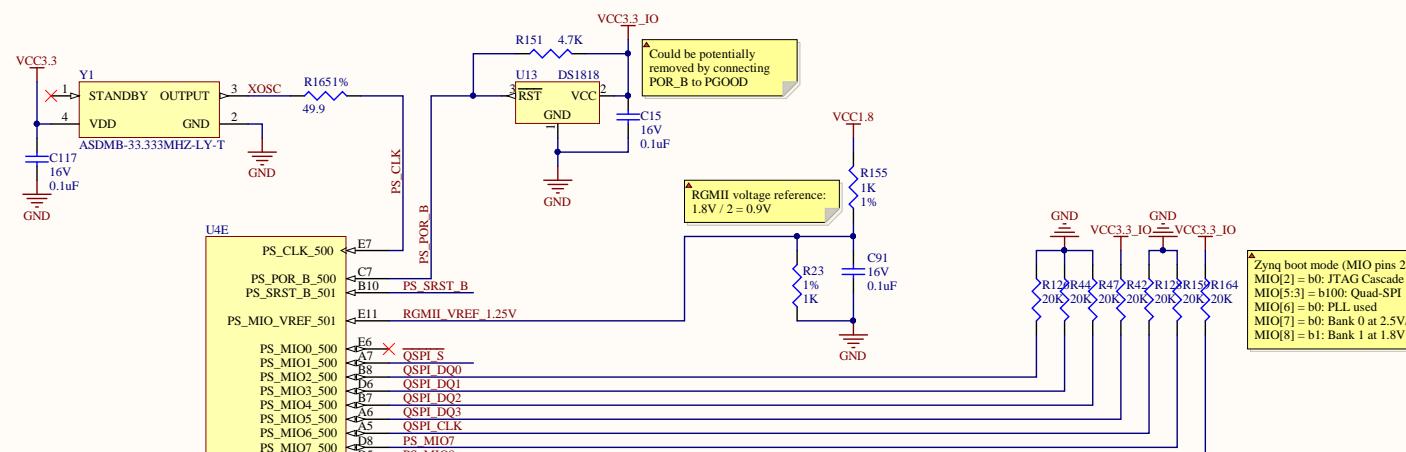
A

A

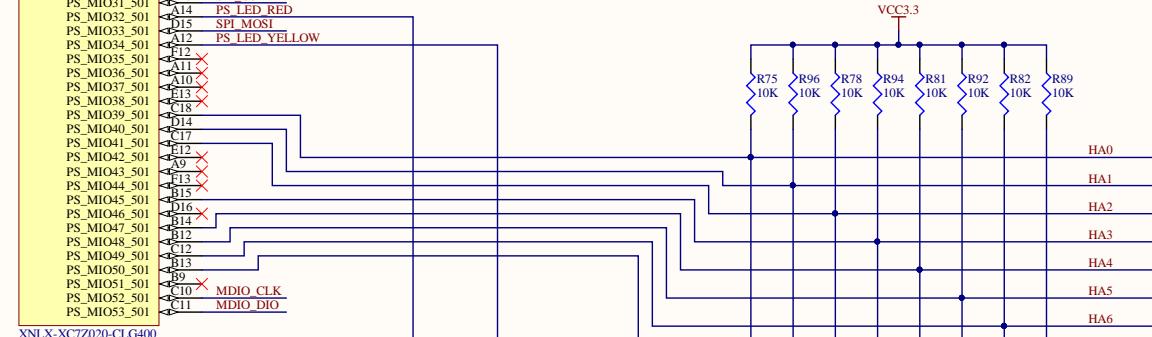
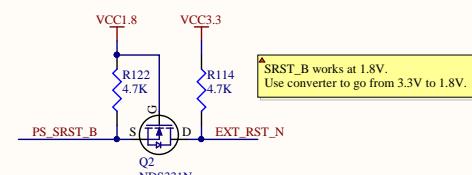
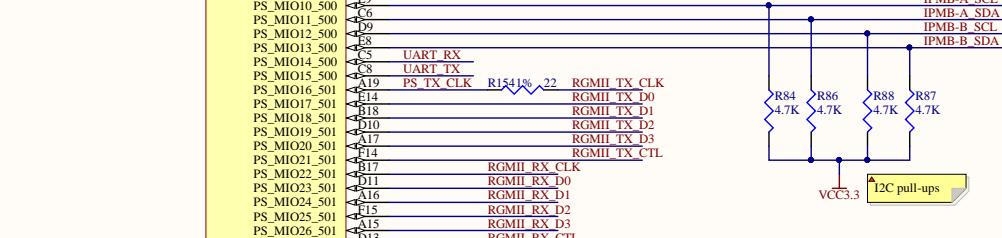


Description	Description
Title	<b>UW-IPMC Mezzanine</b>
Size	A3
Date	15/03/2017
File	BoardConnector.SchDoc
Number	2
Time	16:07:17
Revision	revA
Sheet	2 of 11
Author	Vicente, M., Gorski, T., Tikalsky, J.

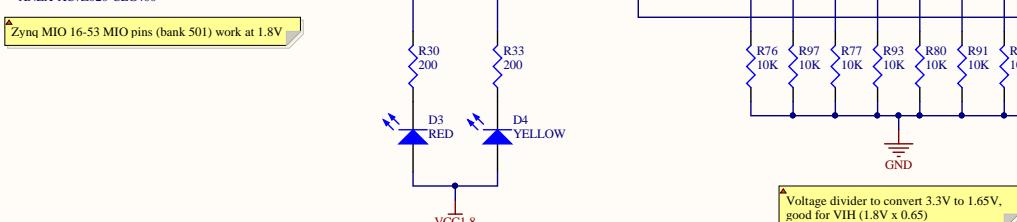




Zynq boot mode (MIO pins 2 to 8):  
MIO[2] = b0: JTAG Cascade mode  
MIO[5:3] = b100: Quad-SPI  
MIO[6] = b0: PLL used  
MIO[7] = b0: Bank 0 at 2.5V/3.3V  
MIO[8] = b1: Bank 1 at 1.8V

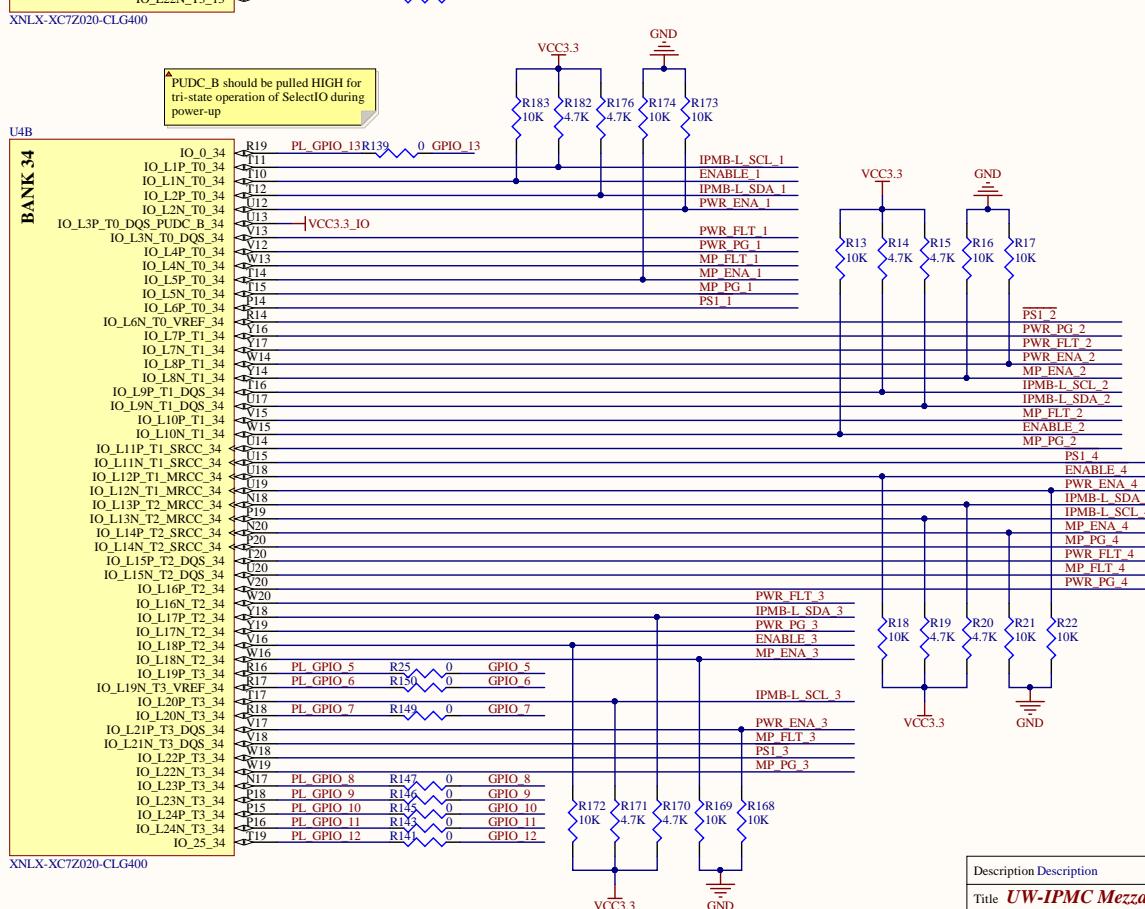
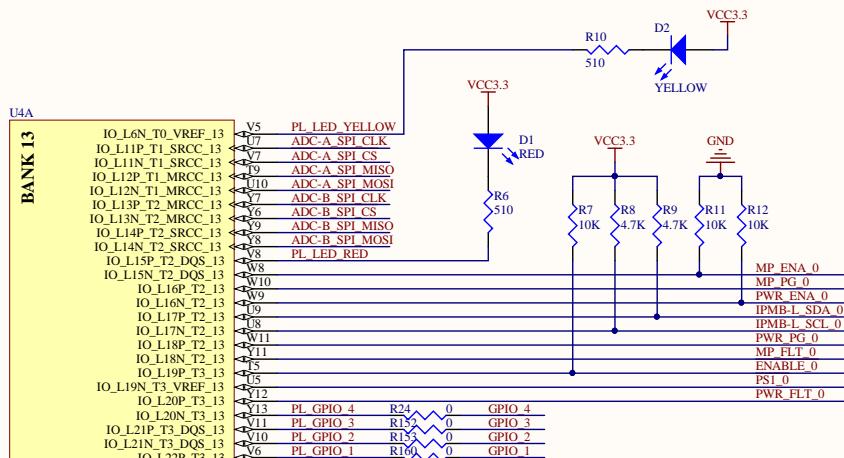


The Hardware Address is assigned through hardware signals from the Backplane or Shelf to an Intelligent FRU. This Hardware Address is assigned using seven (7) signals plus a parity line using odd parity.  
The FRU location shall indicate a logic one by leaving the address pin floating. A logic zero shall be indicated by connecting the address pin to the Logic Ground. - PICMG 3.3, section 3.2.3.1



Could be a simple pull up to 1.8V, but I don't want the 1.8V going out of the mezzanine.

Description Description					
Title	UW-IPMC Mezzanine	Univ. Wisconsin-Madison Madison, WI 53706			
Size:	A3	Number:	4	Revision:	revA
Date:	15/03/2017	Time:	16:07:17	Sheet:	4 of 11
File:	ZynqMIO.SchDoc	Author:	Vicente, M., Gorski, T., Tikalsky, J.		



Description		
<b>Title</b> UW-IPMC Mezzanine		
Size: A3	Number: 5	Revision: revA
Date: 15/03/2017	Time: 16:07:17	Sheet 5 of 11
File: ZyngEMIO.schDoc		Author: Vicente, M., Gorski, T., Tikalsky, J.
Univ. Wisconsin-Madison Madison, WI 53706		

A

A

B

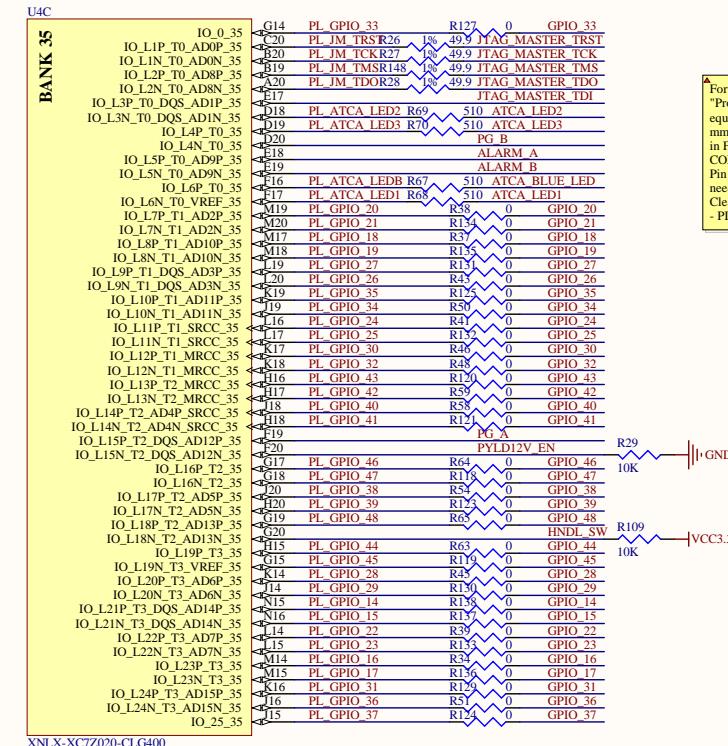
B

C

C

D

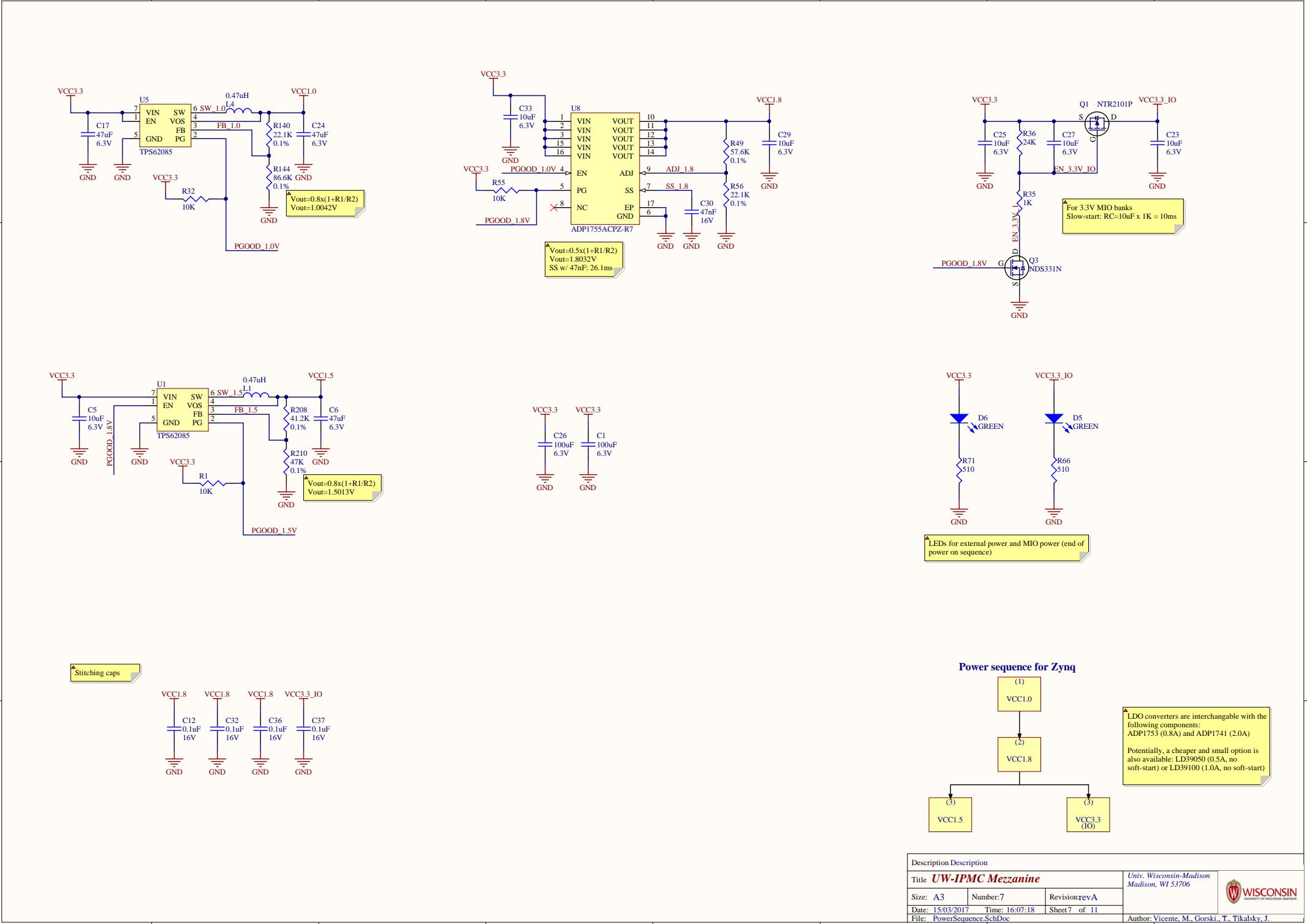
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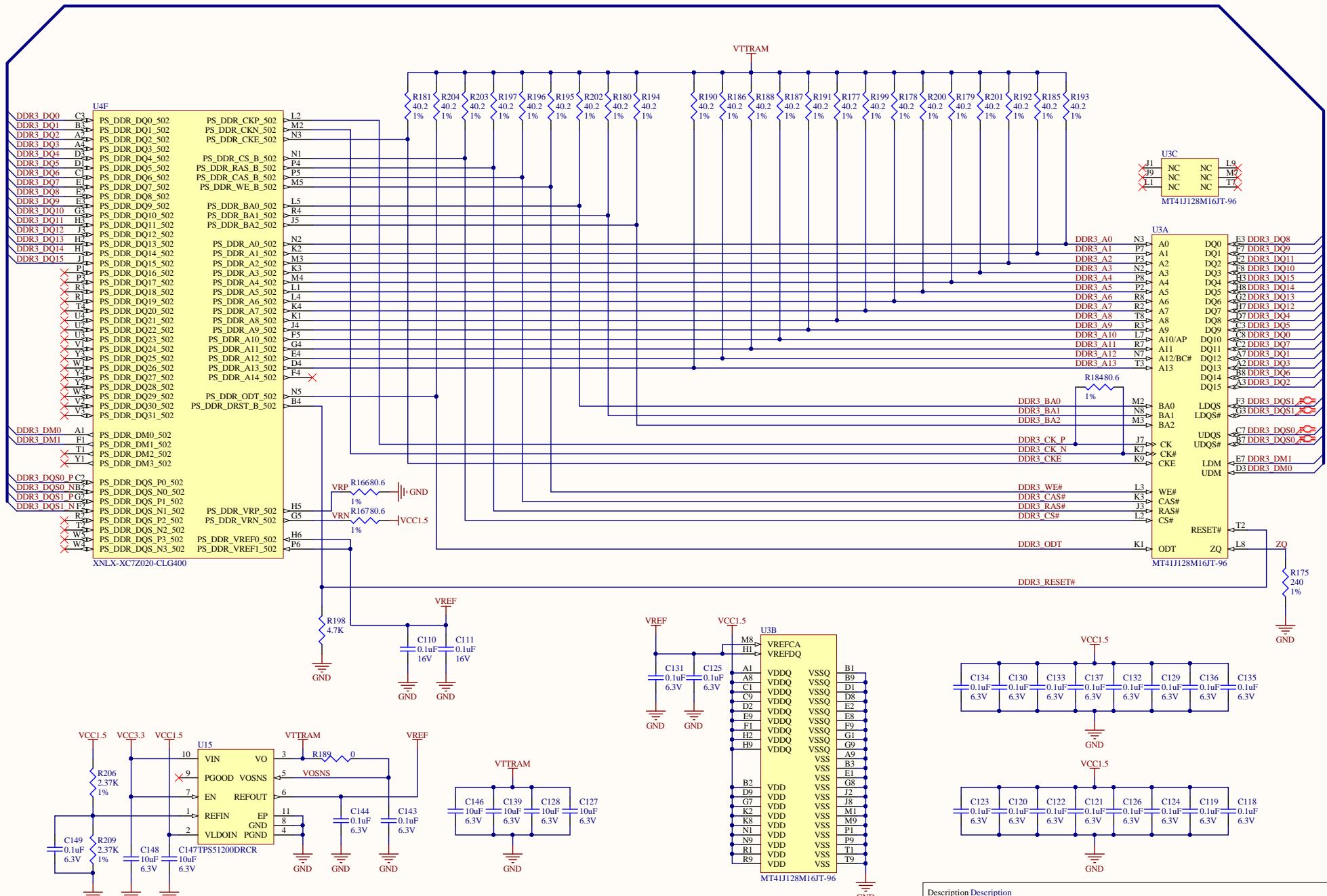


For the handle switch (HNDL\_SW):  
 Provide a right-angle 3-pin header, such as a Molex 53780-0390 or equivalent, to connect to a Face Plate-mounted microswitch within 25 mm of the lower recommended Component Side 2 keepout zone shown in Figure D-2. "PICMG 3.0 R1.0 overall Handle design." Pin 1 is the COMMON connection, Pin 2 is the NC (Normally Closed) contact, and Pin 3 is the NO (Normally Open) contact. Note: Front Board vendors need to ensure that they maintain the necessary Creepage and Clearance distances to any metal connected to Shelf Ground."

- PICMG 3.0 R3.0, D.1.1

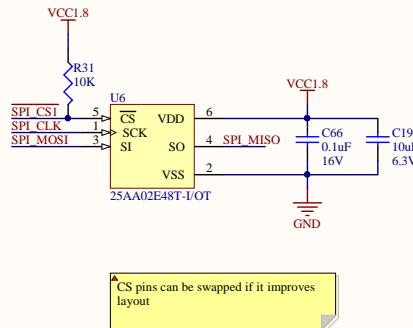
Description		
<b>Title</b> UW-IPMC Mezzanine		
Size: A3	Number: 6	Revision: revA
Date: 15/03/2017	Time: 16:07:18	Sheet 6 of 11
File: ZynqEMIO_2SchDoc		Author: Vicente, M., Gorski, T., Tikalsky, J.
<i>Univ. Wisconsin-Madison Madison, WI 53706</i>		





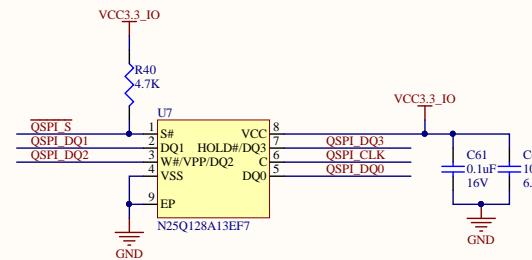
A

A



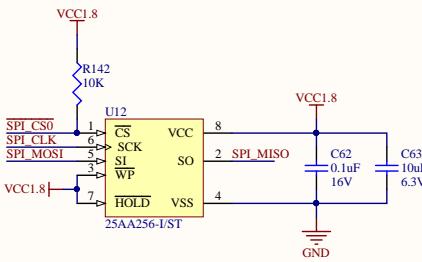
B

B



C

C



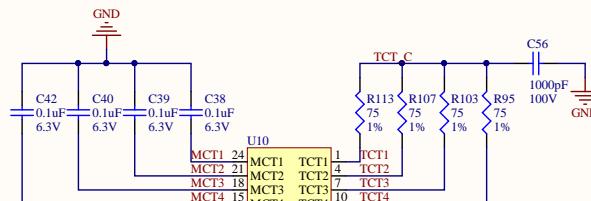
D

D

**QSPI has 16MBytes  
Needs 50ohm lines  
C should be pulled LOW, but there is already the Zynq strap-pins.  
40 MHz is the max speed allowed due to the hold times imposed by Zynq.  
Check ZC702 schematic for more details.**

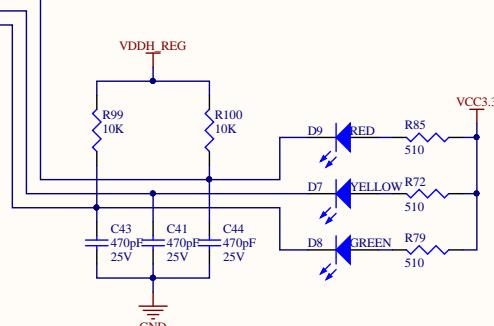
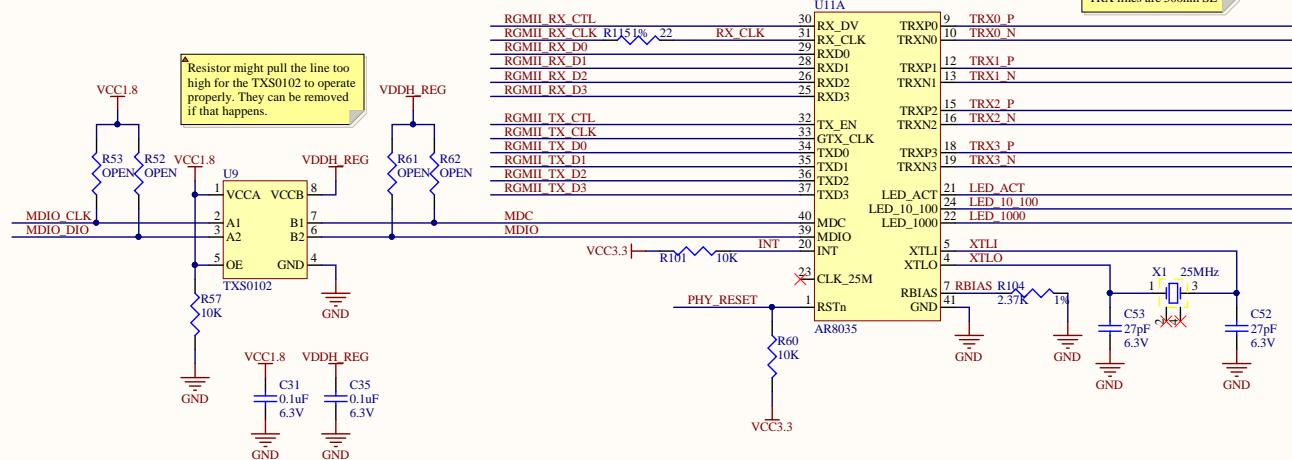
Description		
<b>Title</b> UW-IPMC Mezzanine		
Size: A3	Number: 9	Revision revA
Date: 15/03/2017	Time: 16:07:18	Sheet 9 of 11
File: ZynqPeripherals.SchDoc		Author: Vicente, M., Gorski, T., Tikalsky, J.
<i>Univ. Wisconsin-Madison Madison, WI 53706</i>		

A

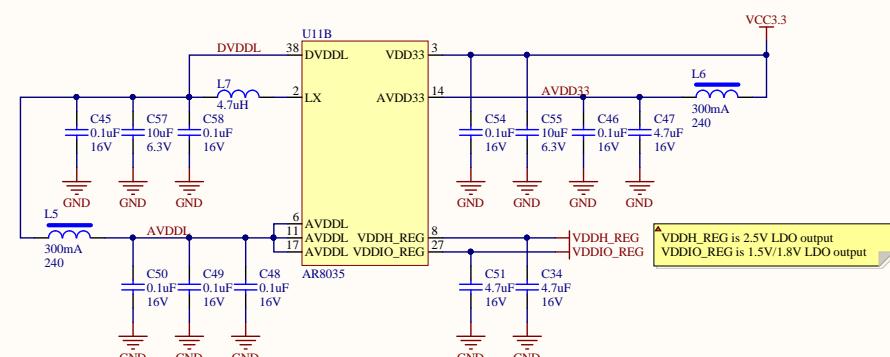


TRX lines are 50ohm SE

B



C



RGMII\_RX\_CTL R112 10K || GND  
 RGMII\_RX\_CLK R117 10K || VDDIO\_REG  
 RGMII\_RX\_D0 R110 10K || GND  
 RGMII\_RX\_D1 R103 10K || GND  
 RGMII\_RX\_D2 R106 10K || GND  
 RGMII\_RX\_D3 R105 10K || VDDIO\_REG

Power on configuration:  
 RGMII, PLLOFF, INT

Based on AR8031/33 reference design:  
<http://wenku.baidu.com/view/d27bd2d8998fc22bcd10d8e.html>  
 And, AR8035 1.8V design found online:  
[http://riverparkinc.com/wp-content/uploads/2015/01/HAPS1\\_SERVICE\\_MANUAL.pdf](http://riverparkinc.com/wp-content/uploads/2015/01/HAPS1_SERVICE_MANUAL.pdf)

Description		
Title	Description	Univ. Wisconsin-Madison Madison, WI 53706
Size: A3	Number: 10	Revision: revA
Date: 15/03/2017	Time: 16:07:18	Sheet 10 of 11
File: EthernetSchDoc		Author: Vicente, M., Gorski, T., Tikalsky, J.



A

1

F

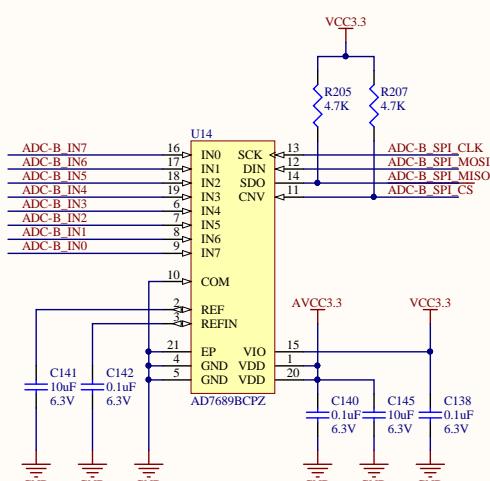
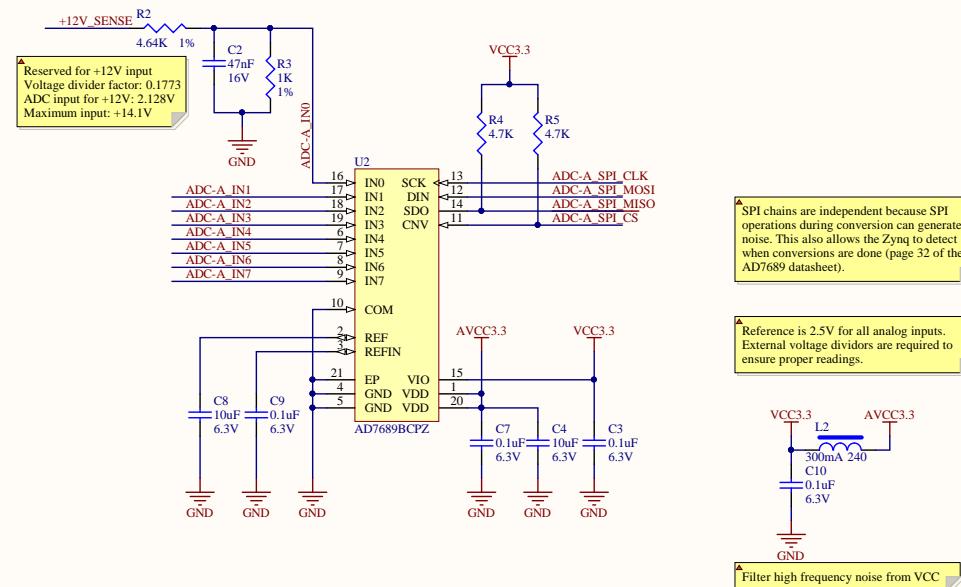
1

6

1

1

1

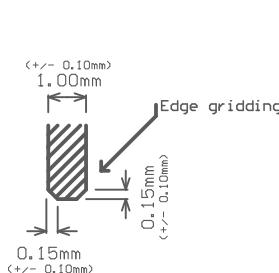
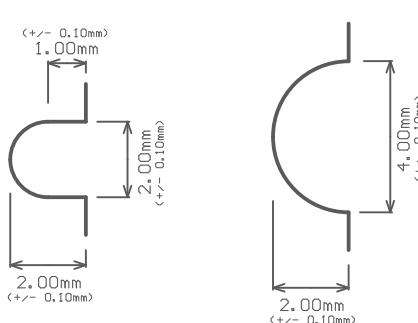
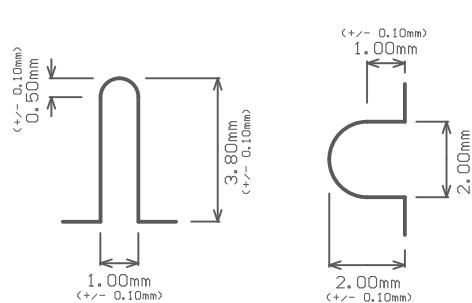


1

2

3

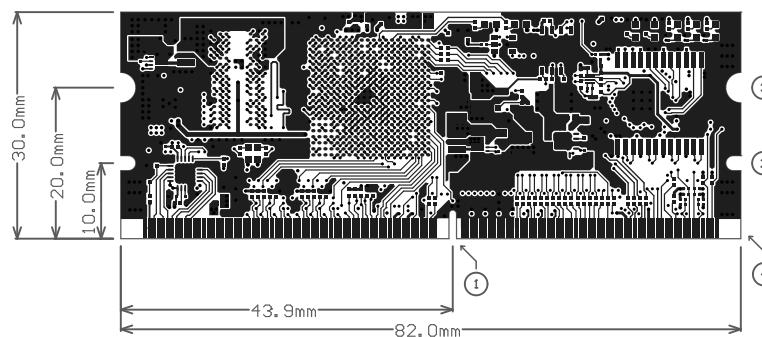
4



Detail 4  
(PCB side view)

### UW-IPMC MEZZANINE (revA)

Layer 1 - Signal (Copper)



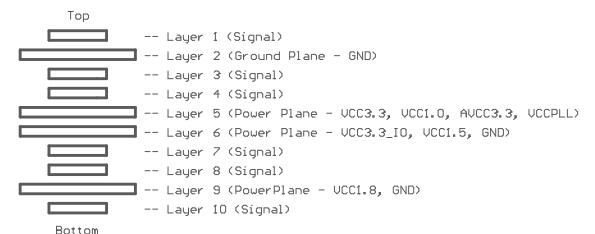
### Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm  $\pm 0.10$ mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm 10\%$ . All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating  $\pm 3$  mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagineable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2).
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction.
14. Design origin is at the bottom-left corner of the PCB.
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination.
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be  $\leq 10$  ohms or less.
  - c. Resistance between planes and non-connected plated through holes and vias shall be  $\leq 10$  Megohms or larger.
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm)  $\pm 10\%$ . Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units.
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

### Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

1

2

3

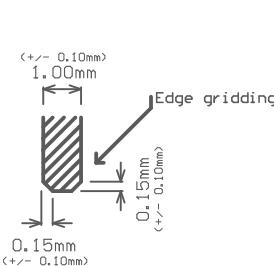
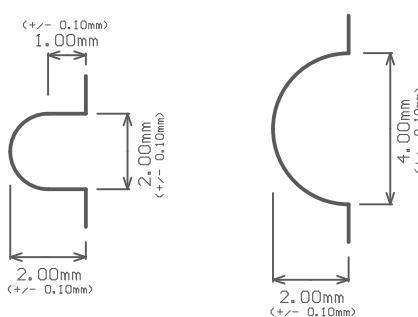
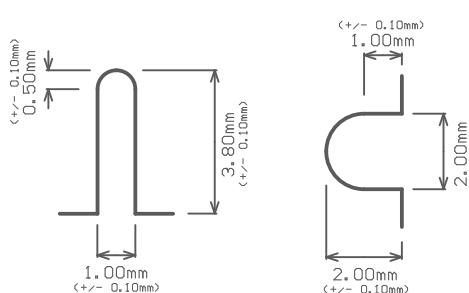
4

1

2

3

4



Detail 4  
(PCB side view)

## Specifications:

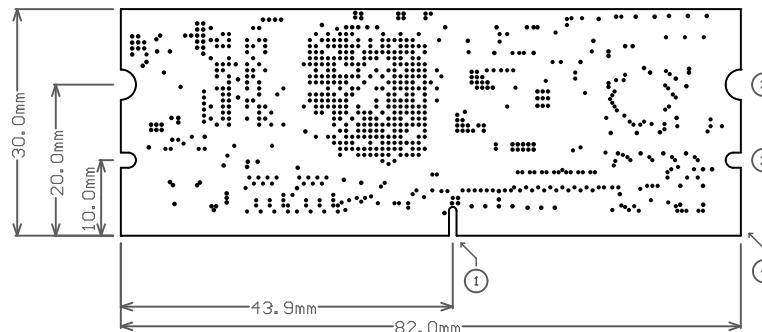
1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm  $\pm 0.10$ mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

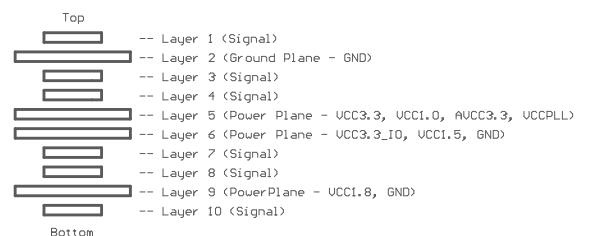
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm 10\%$ . All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating  $\pm 3$  mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimmagable, with maximum thickness of 3 mils
10. Layers 2, 5, 6 and 9 are power planes and are INERTED
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction
14. Design origin is at the bottom-left corner of the PCB
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm)  $\pm 10\%$ . Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

## UW-IPMC MEZZANINE (revA)

Layer 2 - Ground Plane (Copper, Mask)



## Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER:  
Vicente, M., Gorski, T., Tikalsky, J.  
  
PCB DESIGNER:  
Vicente, M.  
  
DATE:  
24FEB2017  
  
FILE NAME:  
UW\_IPMC\_ZYNQ.PCBDOC

TITLE:  
UW-IPMC Mezzanine

PART NO:

REV:  
revA

DWG NO:

SCALE:  
1:1

1

2

3

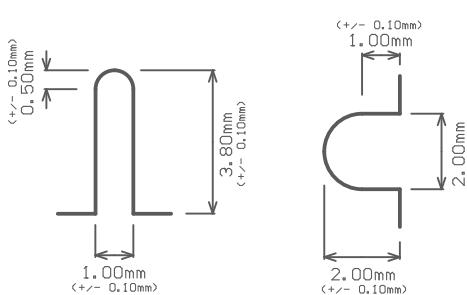
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1

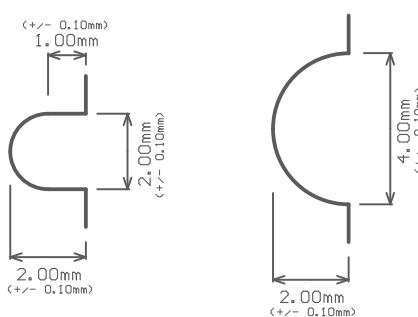
2

3

4

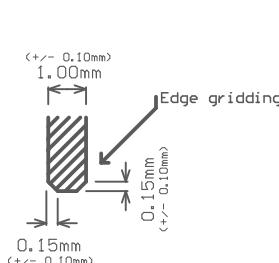


Detail 1



Detail 2

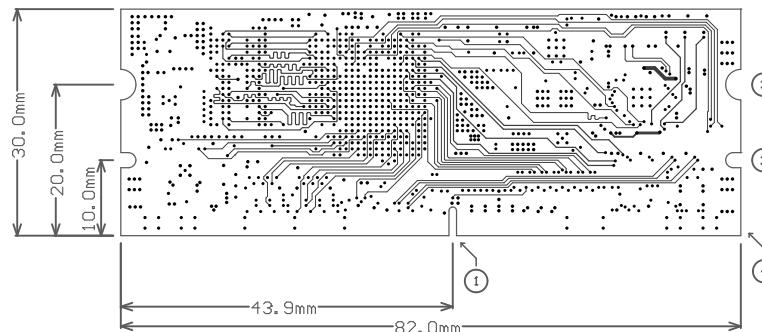
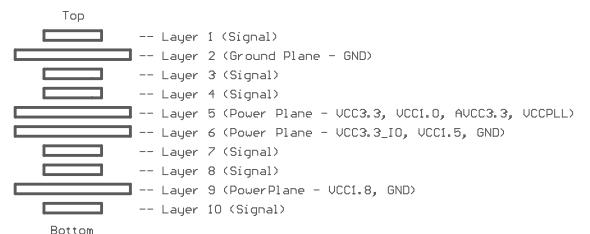
Detail 3

Detail 4  
(PCB side view)**Specifications:**

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
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9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction
14. Design origin is at the bottom-left corner of the PCB
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

**UW-IPMC MEZZANINE (revA)****Layer 3 - Signal (Copper)****Layer Stackup**Univ. of Wisconsin-Madison  
Madison, WI 53706ENGINEER:  
Vicente, M., Gorski, T., Tikalsky, J.PCB DESIGNER:  
Vicente, M.DATE:  
24FEB2017FILE NAME:  
UW\_IPMC\_ZYNQ.PCBDOCTITLE:  
UW-IPMC Mezzanine

PART NO:

REV:  
revA

DWG NO:

SCALE:  
1:1

1

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A

B

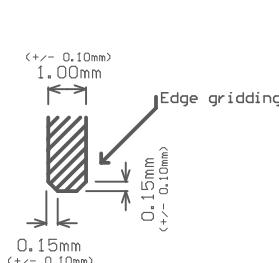
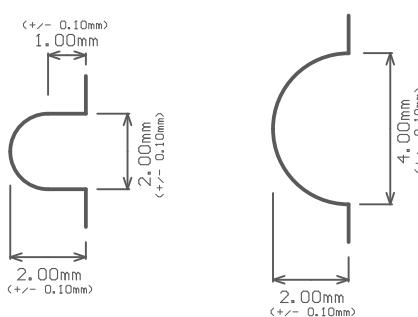
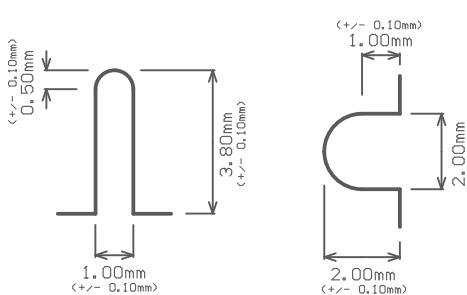
D

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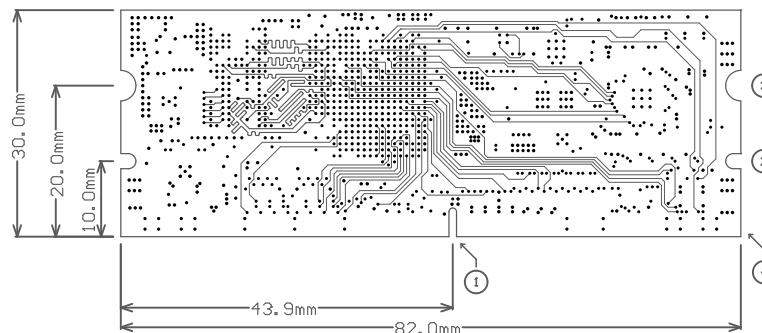
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Detail 4  
(PCB side view)

### UW-IPMC MEZZANINE (revA)

Layer 4 - Signal (Copper)



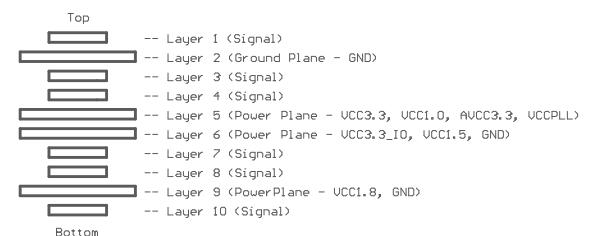
### Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction
14. Design origin is at the bottom-left corner of the PCB
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 0 ohms or less
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

### Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine	
PCB DESIGNER: Vicente, M.		
DATE: 24FEB2017	PART NO.:	REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.:	SCALE: 1:1

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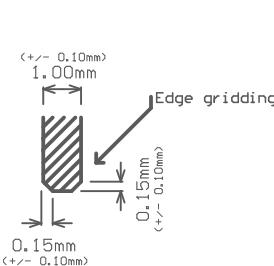
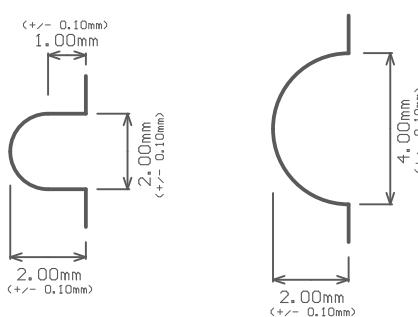
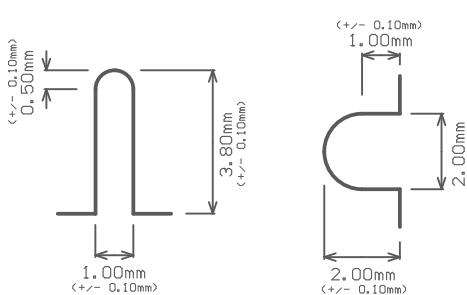
4

1

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Detail 4  
(PCB side view)

## Specifications:

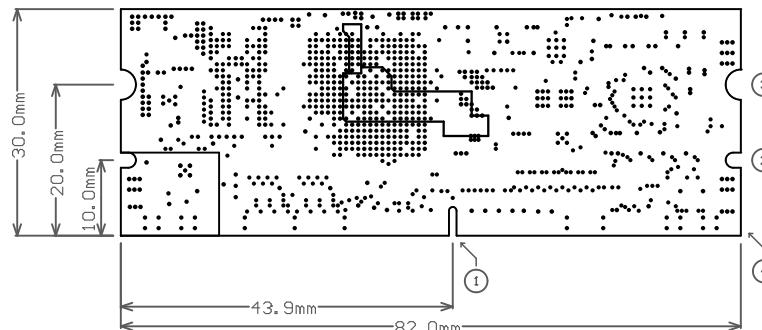
1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm  $\pm 0.10$ mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

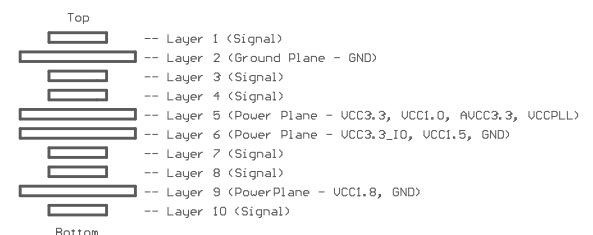
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm 10\%$ . All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating  $\pm 3$ mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2).
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction.
14. Design origin is at the bottom-left corner of the PCB.
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination.
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less.
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger.
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm)  $\pm 10\%$ . Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units.
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

## UW-IPMC MEZZANINE (revA)

Layer 5 - Power Plane (Copper, Mask)



## Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine		
PCB DESIGNER: Vicente, M.			
DATE: 24FEB2017	PART NO.:		REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.:		SCALE: 1:1

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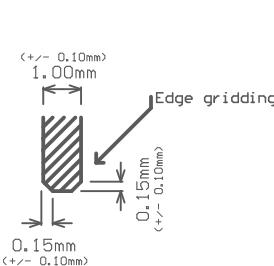
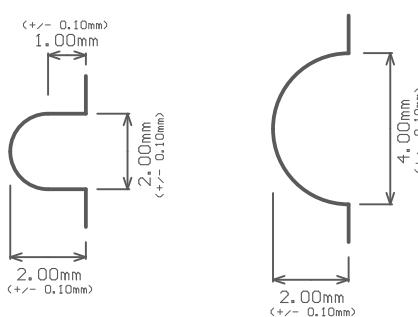
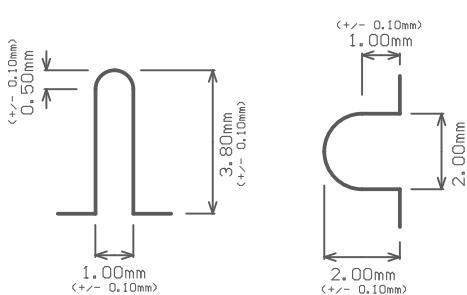
4

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Detail 4  
(PCB side view)

## Specifications:

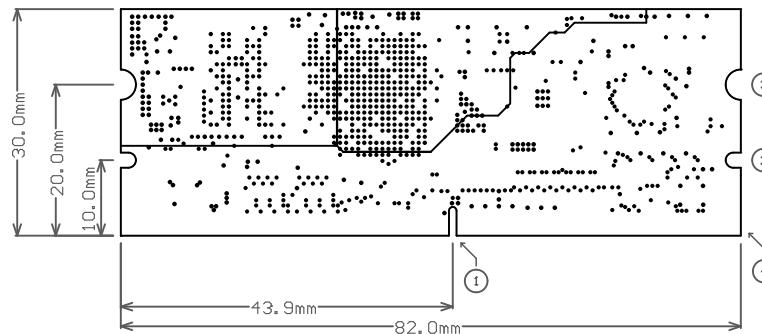
1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm  $\pm 0.10$ mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

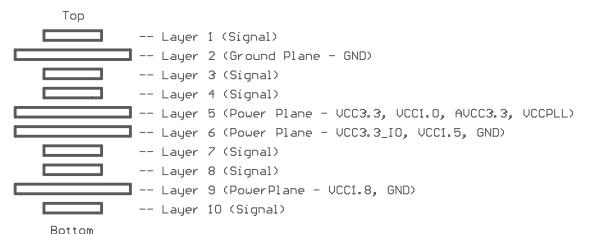
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm 10\%$ . All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating  $\pm 3$  mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagineable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2).
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction.
14. Design origin is at the bottom-left corner of the PCB.
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination.
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be  $< 10$  ohms or less.
  - c. Resistance between planes and non-connected plated through holes and vias shall be  $< 10$  Megohms or larger.
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm)  $\pm 10\%$ . Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units.
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

## UW-IPMC MEZZANINE (revA)

Layer 6 - Power Plane (Copper, Mask)



## Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

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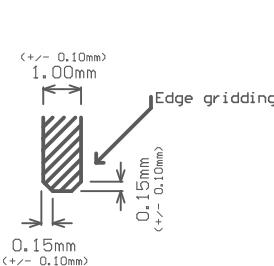
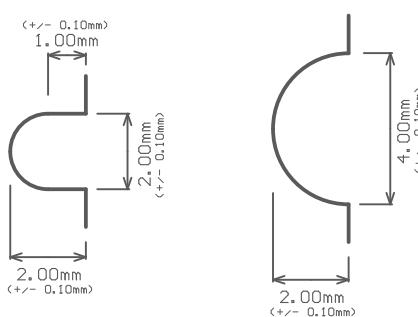
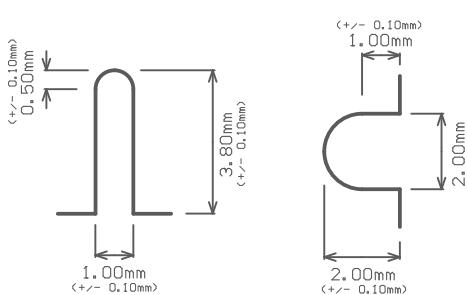
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Detail 4  
(PCB side view)

## Specifications:

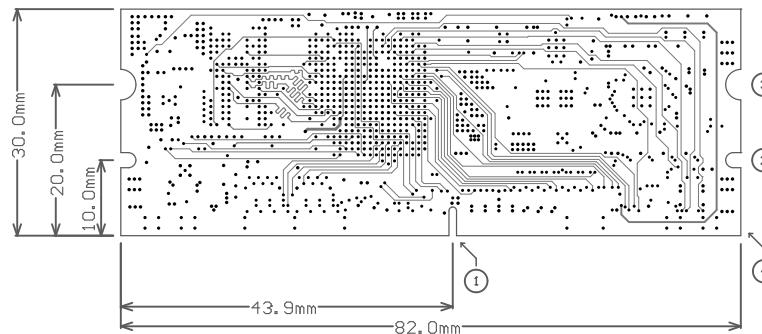
1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

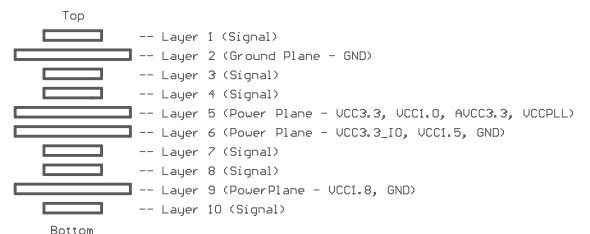
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagineable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction
14. Design origin is at the bottom-left corner of the PCB
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

## UW-IPMC MEZZANINE (revA)

Layer 7 - Signal (Copper)



## Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

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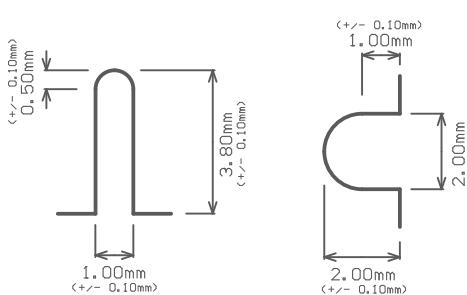
4

1

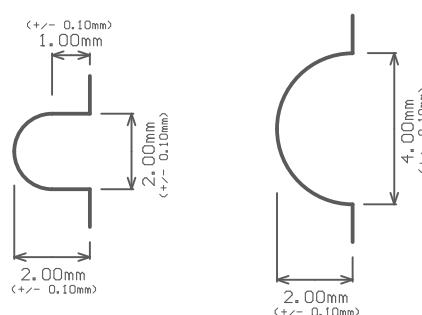
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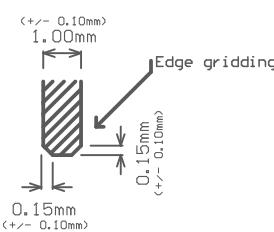
Detail 1



Detail 2

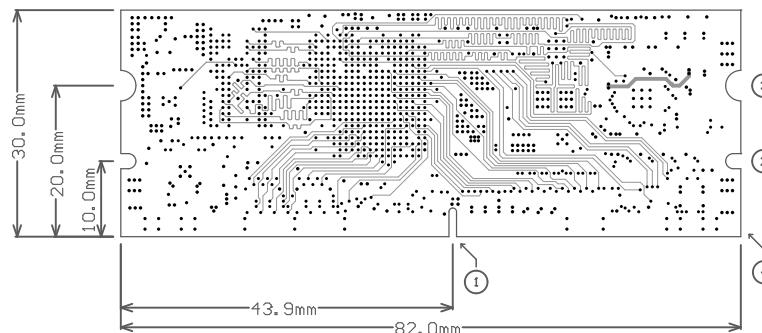


Detail 3

Detail 4  
(PCB side view)

## UW-IPMC MEZZANINE (revA)

Layer 8 - Signal (Copper)



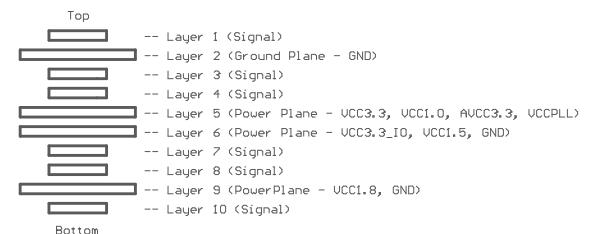
## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2).
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction.
14. Design origin is at the bottom-left corner of the PCB.
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination.
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 0 ohms or less.
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger.
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units.
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

## Layer Stackup

Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine
PCB DESIGNER: Vicente, M.	PART NO.: REV: revA
DATE: 24FEB2017	
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

1

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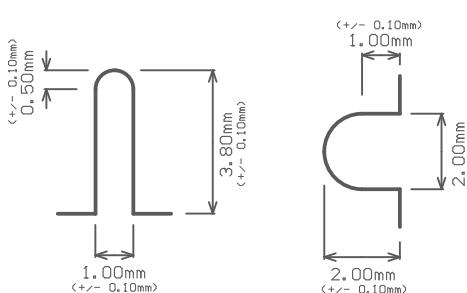
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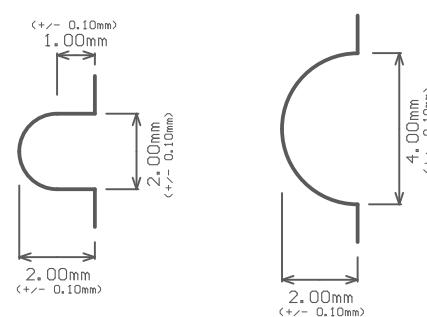
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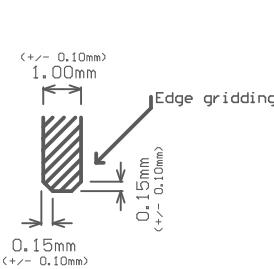


Detail 1



Detail 2

Detail 3

Detail 4  
(PCB side view)

## Specifications:

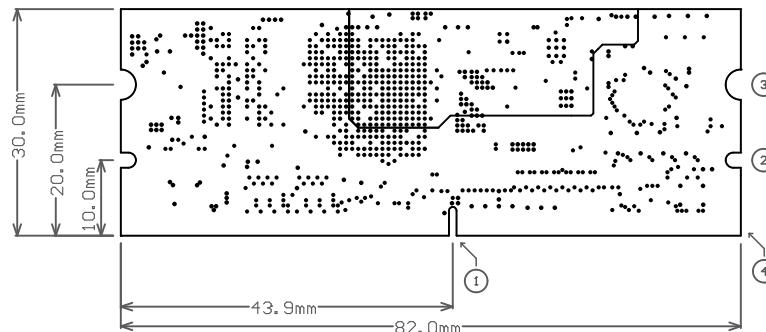
1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

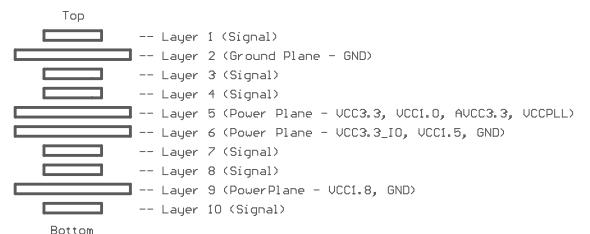
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
10. Layers 2, 5, 6 and 9 are power planes and are INERTED
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction
14. Design origin is at the bottom-left corner of the PCB
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

## UW-IPMC MEZZANINE (revA)

Layer 9 - Power Plane (Copper, Mask)



## Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine
PCB DESIGNER: Vicente, M.	PART NO.: REV: revA
DATE: 24FEB2017	
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

1

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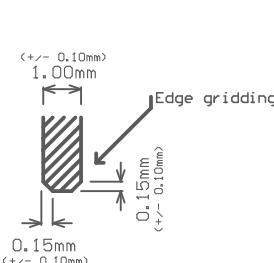
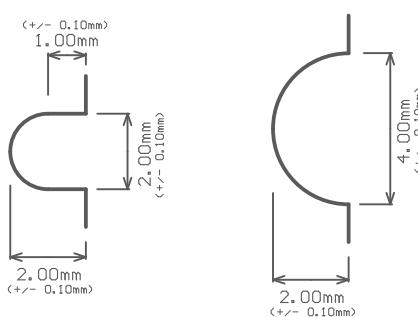
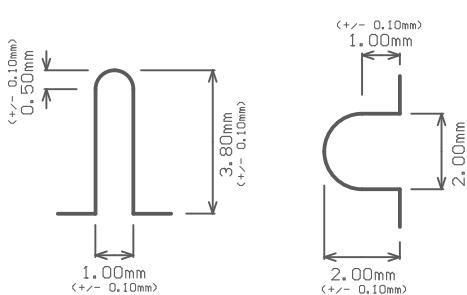
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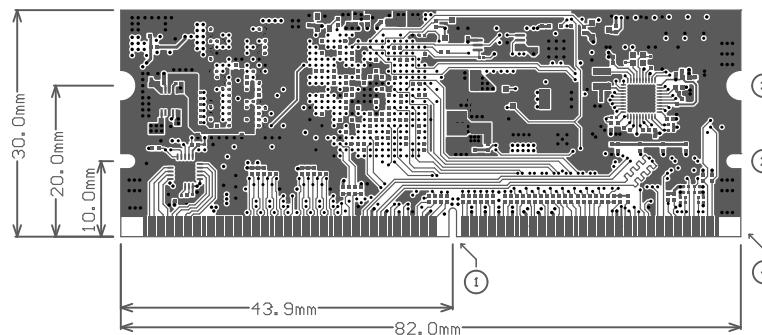
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Detail 4  
(PCB side view)

### UW-IPMC MEZZANINE (revA)

Layer 10 - Signal (Copper)



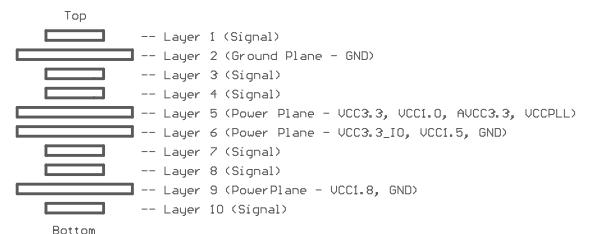
### Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm  $\pm 0.10$ mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm 10\%$ . All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating  $\pm 3$ mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimangible, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2).
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction.
14. Design origin is at the bottom-left corner of the PCB.
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination.
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be  $\leq 10$  ohms or less.
  - c. Resistance between planes and non-connected plated through holes and vias shall be  $\leq 10$  Megohms or larger.
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm)  $\pm 10\%$ . Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units.
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

### Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

1

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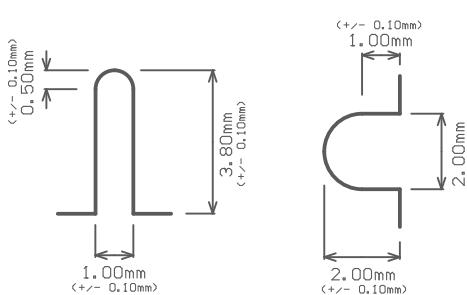
4

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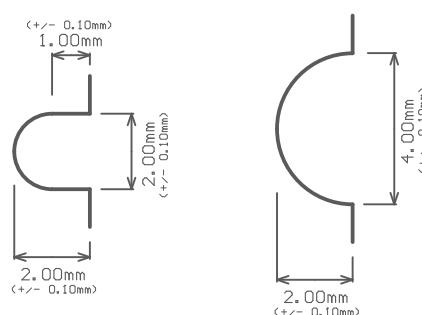
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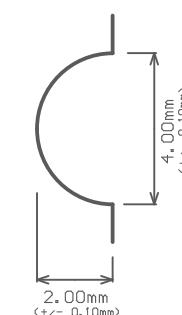
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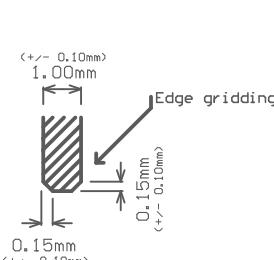
Detail 1



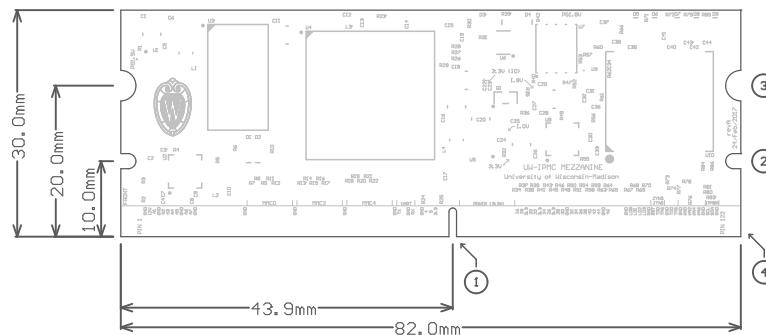
Detail 2



Detail 3

Detail 4  
(PCB side view)**UW-IPMC MEZZANINE (revA)**

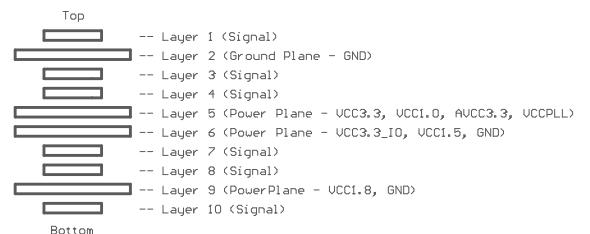
Top Overlay (Ink)

**Specifications:**

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface.
  - b. Area to receive hard gold finish is identified in two separate photoplot layers.
  - c. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - d. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
9. Red colored solder mask shall be applied to both top and bottom surfaces.
10. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Locations in IPC-D-356A file are given in 2.4 English units
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

**Layer Stackup**Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine	
PCB DESIGNER: Vicente, M.		
DATE: 24FEB2017	PART NO.:	REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.:	SCALE: 1:1

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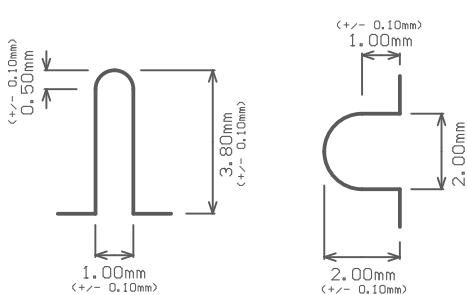
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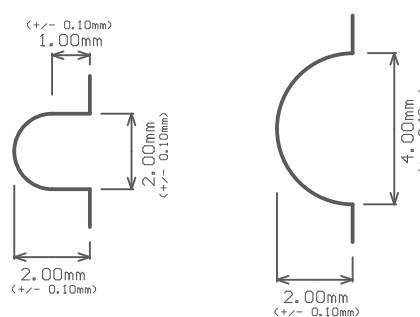
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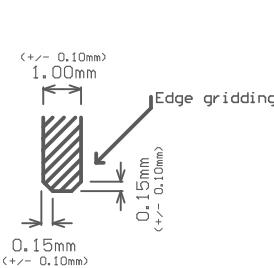


Detail 1



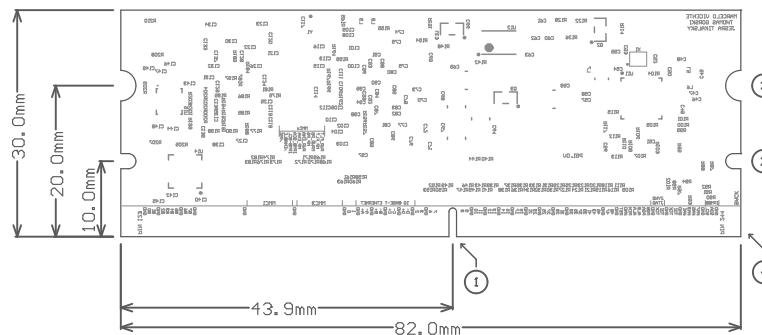
Detail 2

Detail 3

Detail 4  
(PCB side view)

## UW-IPMC MEZZANINE (revA)

Bottom Overlay (Ink)



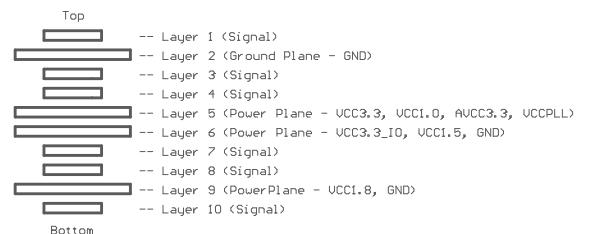
## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
10. Layers 2, 5, 6 and 9 are power planes and are INERTED
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction
14. Design origin is at the bottom-left corner of the PCB
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 0 ohms or less
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

## Layer Stackup

Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

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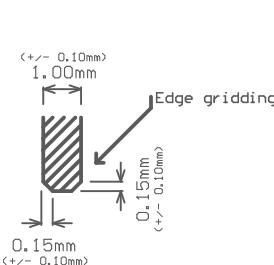
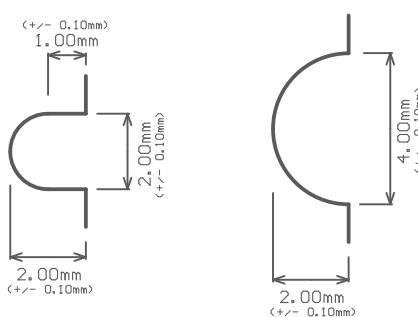
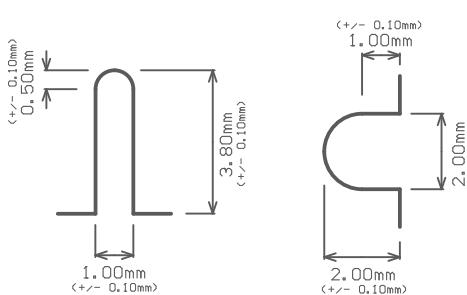
4

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Detail 4  
(PCB side view)

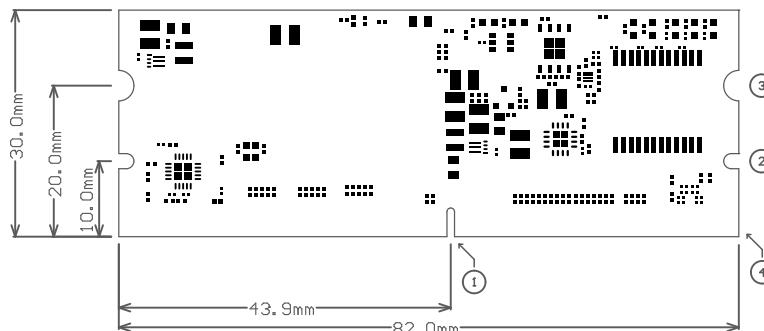
### Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm  $\pm 0.10$ mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

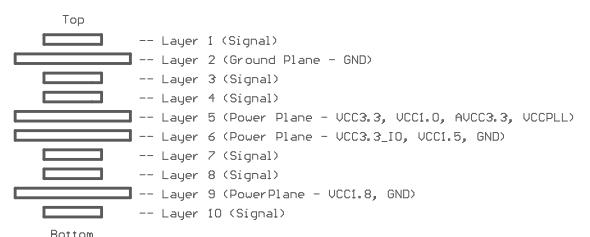
Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm 10\%$ . All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating  $\pm 3$ mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2).
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction.
14. Design origin is at the bottom-left corner of the PCB.
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination.
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be  $\leq 10$  ohms or less.
  - c. Resistance between planes and non-connected plated through holes and vias shall be  $\leq 10$  Megohms or larger.
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm)  $\pm 10\%$ . Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units.
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

### UW-IPMC MEZZANINE (revA)



### Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

1

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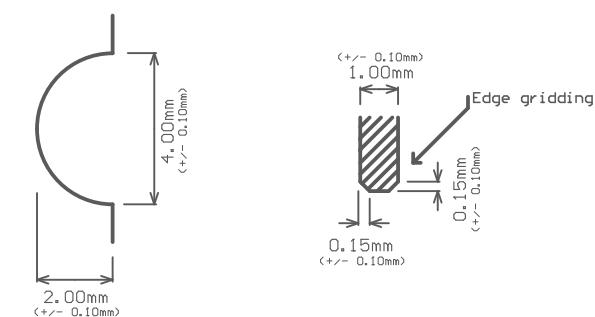
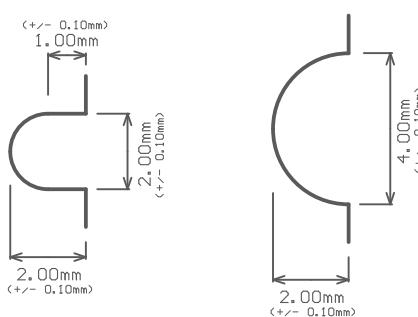
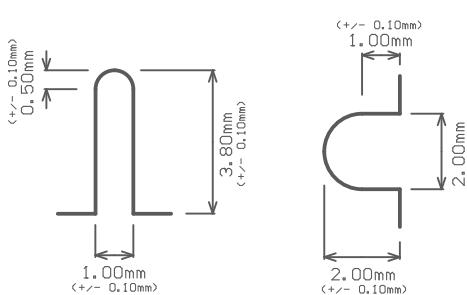
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1

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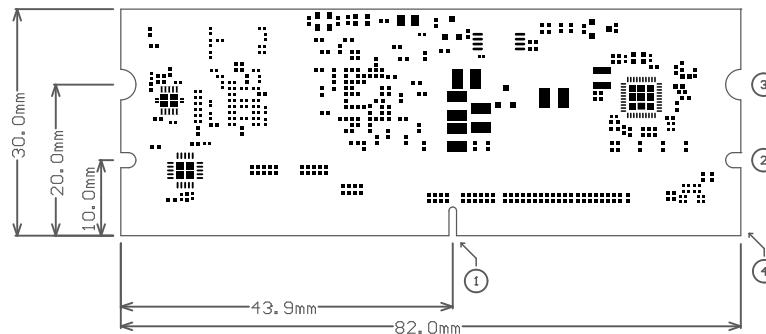
3

4



Detail 4  
(PCB side view)

### UW-IPMC MEZZANINE (revA)



Bottom Paste (Paste)

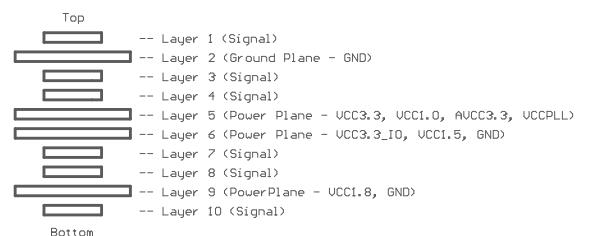
### Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm  $\pm 0.10$ mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm 10\%$ . All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating  $\pm 3$  mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2).
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction.
14. Design origin is at the bottom-left corner of the PCB.
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination.
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be  $\leq 10$  ohms or less.
  - c. Resistance between planes and non-connected plated through holes and vias shall be  $\leq 10$  Megohms or larger.
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm)  $\pm 10\%$ . Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units.
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

### Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

1

2

3

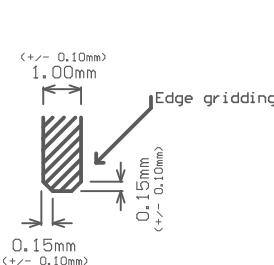
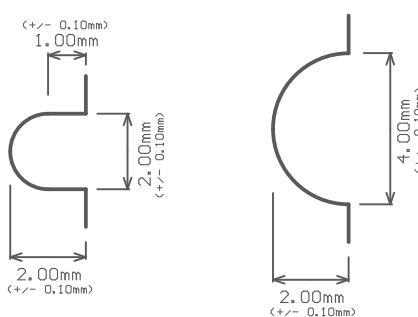
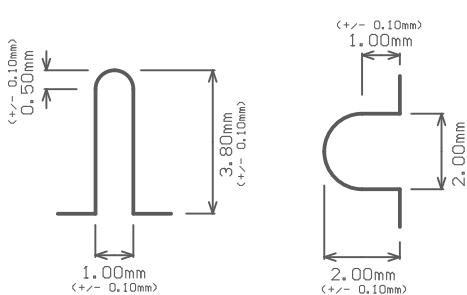
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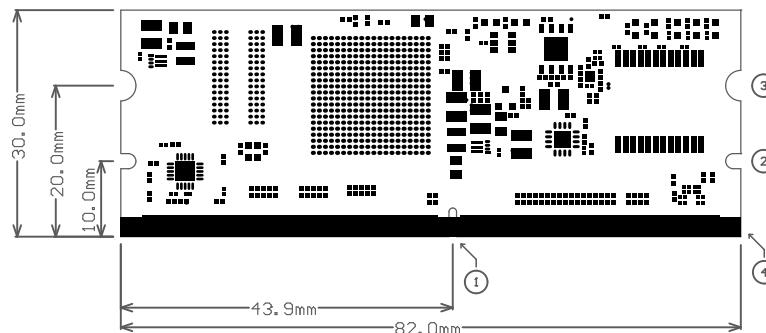
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4



Detail 4  
(PCB side view)

### UW-IPMC MEZZANINE (revA)



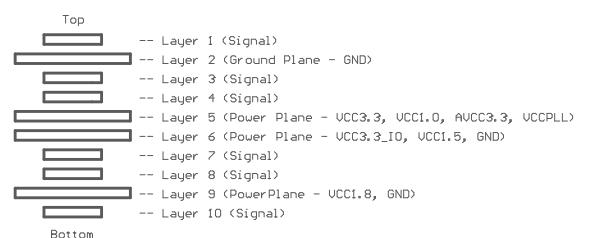
### Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm  $\pm 0.10$ mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm 10\%$ . All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating  $\pm 3$ mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction
14. Design origin is at the bottom-left corner of the PCB
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm)  $\pm 10\%$ . Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

### Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER:  
Vicente, M., Gorski, T., Tikalsky, J.

PCB DESIGNER:  
Vicente, M.

DATE:  
24FEB2017

FILE NAME:  
UW\_IPMC\_ZYNQ.PCBDOC

TITLE:  
UW-IPMC Mezzanine

PART NO:

REV:  
revA

DWG NO:

SCALE:  
1:1

1

2

3

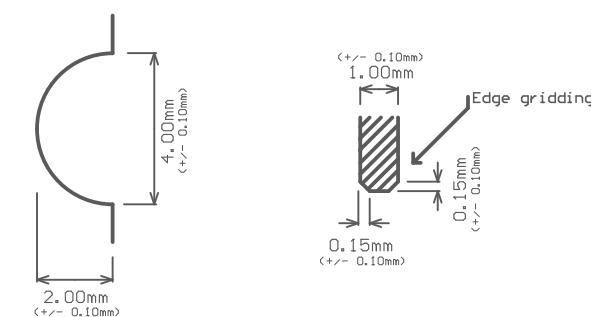
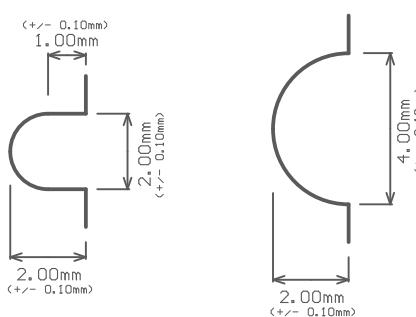
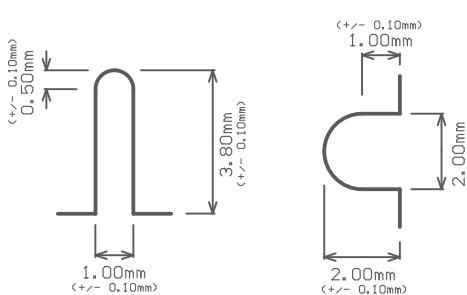
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**Detail 4**  
(PCB side view)

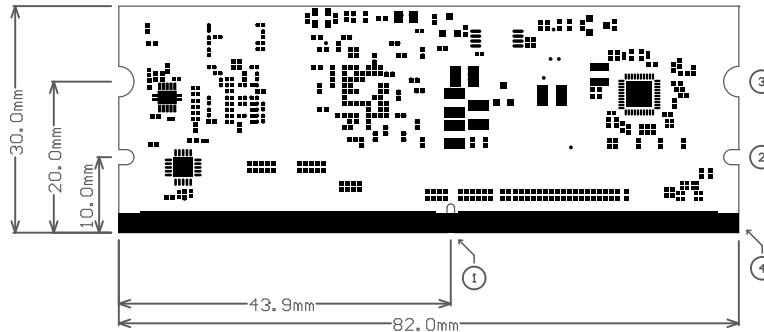
## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

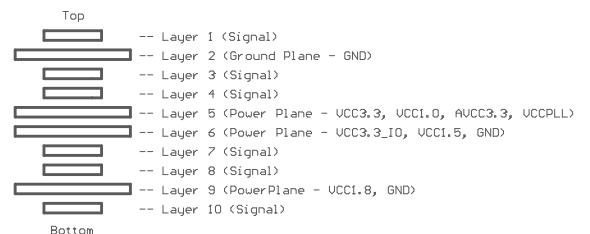
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction
14. Design origin is at the bottom-left corner of the PCB
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

**UW-IPMC MEZZANINE (revA)**



**Bottom Solder (Mask)**

## Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER:  
Vicente, M., Gorski, T., Tikalsky, J.

PCB DESIGNER:  
Vicente, M.

DATE:  
24FEB2017

FILE NAME:  
UW\_IPMC\_ZYNQ.PCBDOC

TITLE:  
UW-IPMC Mezzanine

PART NO:

REV:  
revA

DWG NO:

SCALE:  
1:1

1

2

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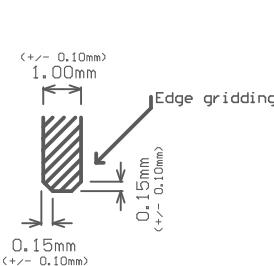
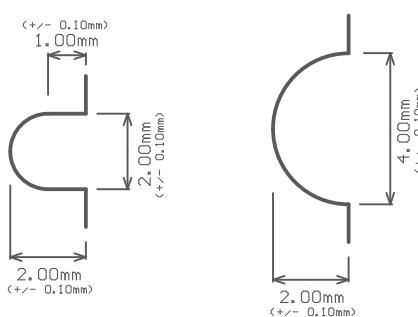
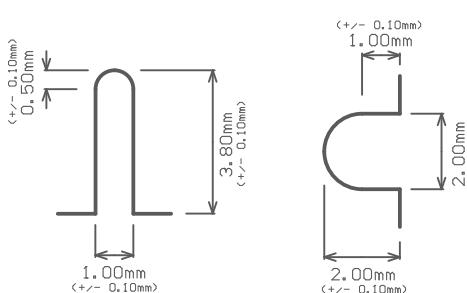
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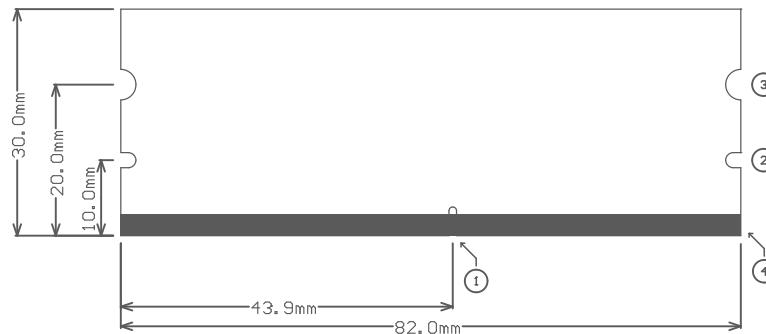
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Detail 4  
(PCB side view)

### UW-IPMC MEZZANINE (revA)



Top Hard Gold (Mask)

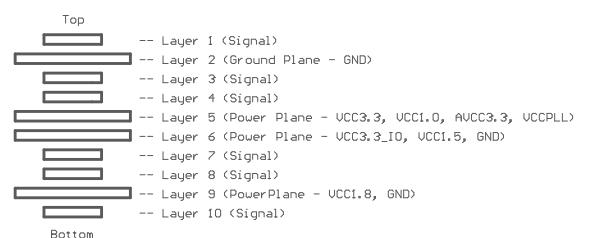
### Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm  $\pm 0.10$ mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm 10\%$ . All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating  $\pm 3$  mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2).
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction.
14. Design origin is at the bottom-left corner of the PCB.
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm)  $\pm 10\%$ . Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

### Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

1

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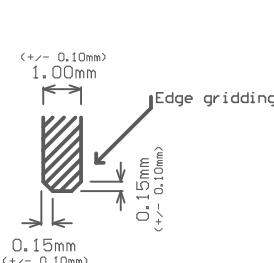
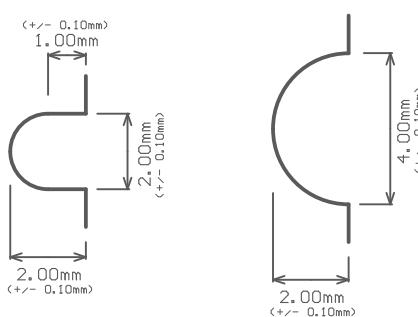
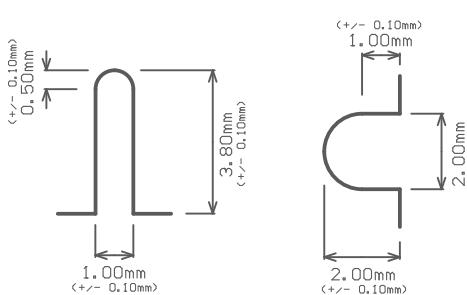
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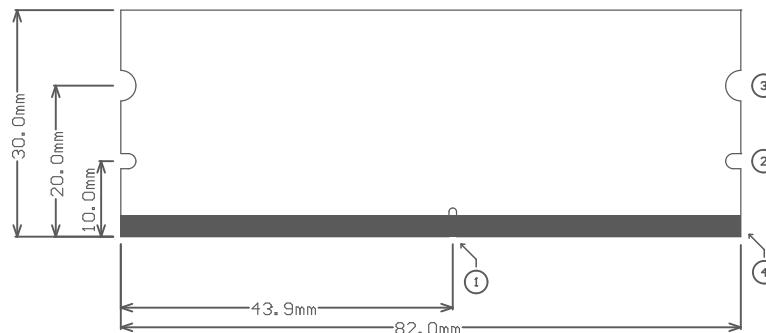
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Detail 4  
(PCB side view)

### UW-IPMC MEZZANINE (revA)



### Bottom Hard Gold (Mask)

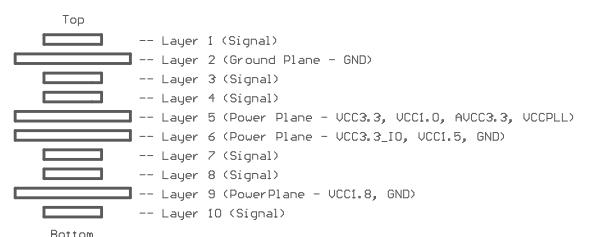
### Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm  $\pm 0.10$ mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within  $\pm 10\%$ . All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating  $\pm 3$ mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimmagable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2).
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction.
14. Design origin is at the bottom-left corner of the PCB.
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm)  $\pm 10\%$ . Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

### Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

1

2

3

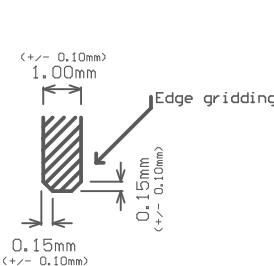
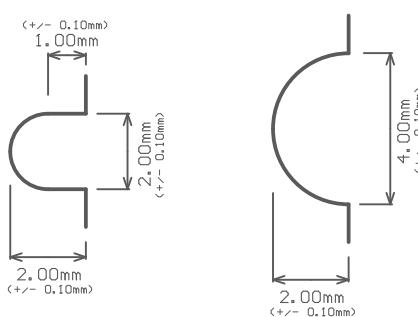
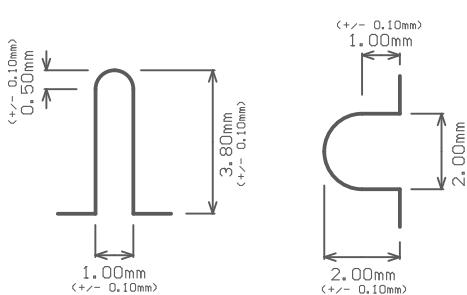
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1

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4



Detail 4  
(PCB side view)

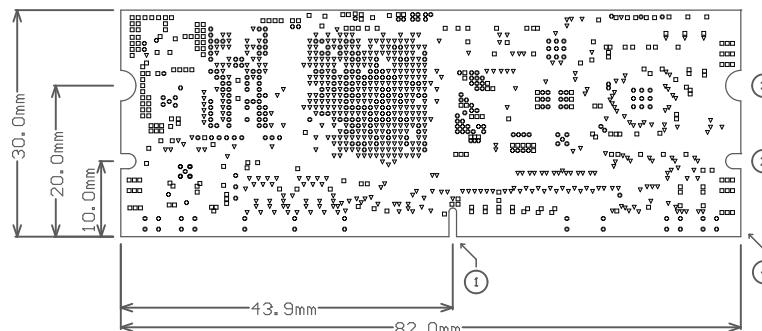
## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
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	50 Ohm: 6.5 mil tracks in artwork

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6. Holes:
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7. Finish:
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  - b. Overall board finish is immersion gold.
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9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagineable, with maximum thickness of 3 mils.
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12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2).
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction.
14. Design origin is at the bottom-left corner of the PCB.
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination.
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less.
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger.
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units.
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

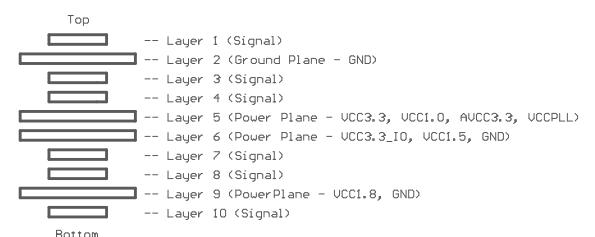
## UW-IPMC MEZZANINE (revA)



## Drill Guide

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length	Rout Path Length
□	275	8.00mil (0.203mm)	PTH	Round	-	-
◊	326	7.00mil (0.178mm)	PTH	Round	-	-
▽	530	6.00mil (0.152mm)	PTH	Round	-	-
<b>Total</b>						

## Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER:  
Vicente, M., Gorski, T., Tikalsky, J.

PCB DESIGNER:  
Vicente, M.

DATE:  
24FEB2017

FILE NAME:  
UW\_IPMC\_ZYNQ.PCBDOC

TITLE:  
UW-IPMC Mezzanine

PART NO:

REV:  
revA

DWG NO:

SCALE:  
1:1

1

2

3

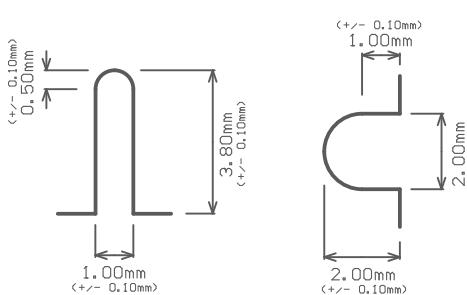
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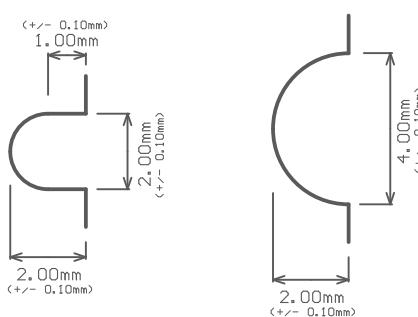
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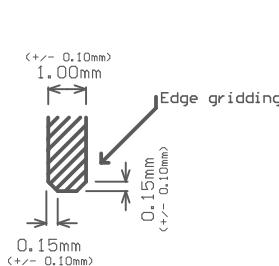


Detail 1

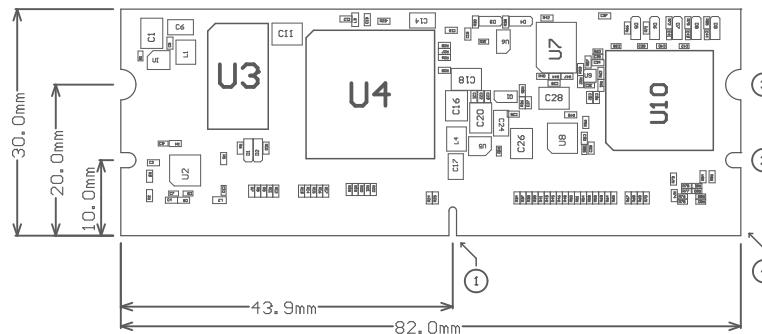


Detail 2

Detail 3

Detail 4  
(PCB side view)

## UW-IPMC MEZZANINE (revA)



## Top Assembly

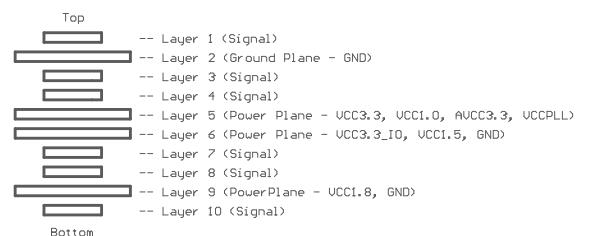
## Specifications:

1. Dielectric material is Tetrafunctional FR-4 with  $T_g > 170$  C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Panelization
  - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
  - b. Panels should contain fiducial marks for X,Y alignment
4. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
5. All layers use 1/2 oz. copper (before plating)
6. Holes:
  - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
  - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
  - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
  - d. Drills are plated-through holes and their locations are given in a separate drill file.
7. Finish:
  - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
  - b. Overall board finish is immersion gold.
8. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10).
9. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils.
10. Layers 2, 5, 6 and 9 are power planes and are INVERTED.
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink.
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2).
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction.
14. Design origin is at the bottom-left corner of the PCB.
15. Testing:
  - a. All layers to undergo optical inspection (machine-based) of all layers before lamination.
  - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less.
  - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger.
  - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
16. Locations in IPC-D-356A file are given in 2.4 English units.
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

## Layer Stackup

Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER: Vicente, M., Gorski, T., Tikalsky, J.	TITLE: UW-IPMC Mezzanine
PCB DESIGNER: Vicente, M.	
DATE: 24FEB2017	PART NO.: REV: revA
FILE NAME: UW_IPMC_ZYNQ.PCBDOC	DWG NO.: SCALE: 1:1

1

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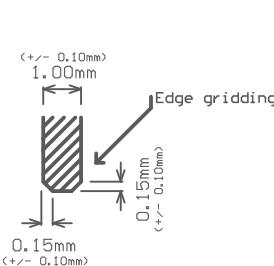
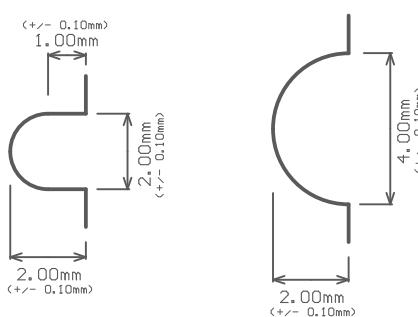
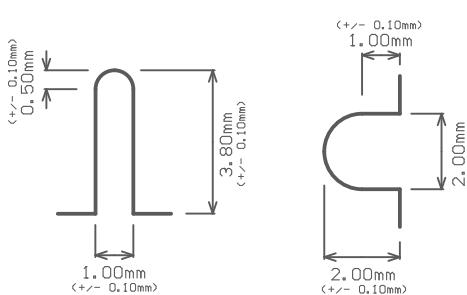
4

1

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3

4



**Detail 4**  
(PCB side view)

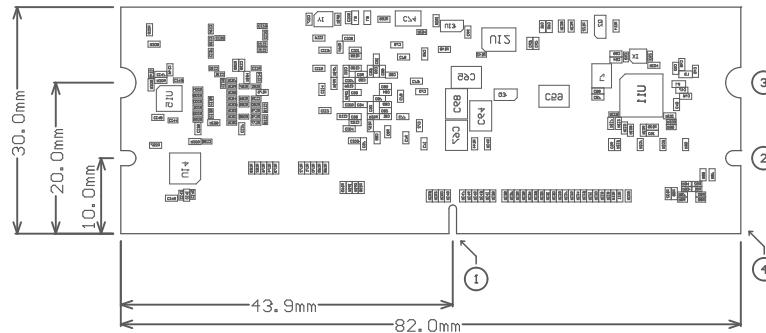
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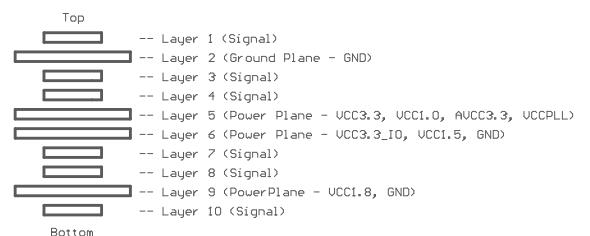
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10. Layers 2, 5, 6 and 9 are power planes and are INERTED
11. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
12. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
13. Combination of bow and twist shall not exceed 10 mils/inch along any direction
14. Design origin is at the bottom-left corner of the PCB
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16. Locations in IPC-D-356A file are given in 2.4 English units
17. South edge-to-edge connector details:
  - a. Tolerance of 0.03mm between pads.
  - b. Board edge to pads maximum of 0.25mm.
  - c. Details present in page 2 of the Molex 87783-0301 datasheet (included).

## UW-IPMC MEZZANINE (revA)



## Bottom Assembly

## Layer Stackup



Univ. of Wisconsin-Madison  
Madison, WI 53706

ENGINEER:  
Vicente, M., Gorski, T., Tikalsky, J.

PCB DESIGNER:  
Vicente, M.

DATE:  
24FEB2017

FILE NAME:  
UW\_IPMC\_ZYNQ.PCBDOC

TITLE:  
UW-IPMC Mezzanine

PART NO:

REV:  
revA

DWG NO:

SCALE:  
1:1

1

2

3

4

# Board Stack Report

Stack Up		Layer Stack				
Layer	Board Layer Stack	Board Layer Stack	Name	Material	Thickness	Constant
1			Top Paste			
2			Top Overlay			
3			Top Solder	Solder Resist	1.00mil	4.15
4			Component Side	Copper	2.83mil	
5			Dielectric 1		3.59mil	3.5
6			Ground Plane 1 (GND)	Copper	0.70mil	
7			Dielectric 2	FR-4	3.00mil	3.5
8			Inner Layer 1	Copper	0.70mil	
9			Dielectric 3		2.88mil	3.5
10			Inner Layer 2	Copper	0.70mil	
11			Dielectric 4		3.00mil	3.5
12			Power Plane 1	Copper	0.70mil	
13			Dielectric 5		3.58mil	3.5
14			Power Plane 2	Copper	0.70mil	
15			Dielectric 6		3.00mil	3.5
16			Inner Layer 3	Copper	0.70mil	
17			Dielectric 7		2.88mil	3.5
18			Inner Layer 4	Copper	0.70mil	
19			Dielectric 8		3.00mil	3.5
20			Power Plane 3	Copper	0.70mil	
21			Dielectric 9		3.59mil	3.5
22			Solder Side	Copper	2.83mil	
23			Bottom Solder	Solder Resist	1.00mil	4.15
24			Bottom Overlay			
25			Bottom Paste			
	Height : 41.78mil		Height : 41.78mil			

## Design Rules Verification Report

Filename : C:\CERN\APD\IPMC\Schematic\svn\trunk\uw\_ipmc\_zynq.PcbDoc

Warnings 0  
Rule Violations 0

Warnings	
Total	0
Rule Violations	
Clearance Constraint (Gap=4mil) (InNetClass('POWER_NETS')),(All)	0
Clearance Constraint (Gap=4mil) (InNetClass('NO_IMPEDANCE')),,(All)	0
Clearance Constraint (Gap=4mil) (OnMid),(All)	0
Clearance Constraint (Gap=4mil) (InNet('DDR3_') AND OnOutside),(All)	0
Clearance Constraint (Gap=4mil) (OnOutside),(All)	0
Clearance Constraint (Gap=7mil) (InPolygon),(All)	0
Clearance Constraint (Gap=4mil) (InNet('DDR3_') AND OnMid),(All)	0
Clearance Constraint (Gap=6mil) (InPolygon AND InNet('VTRAM')),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ( All) )	0
Width Constraint (Min=4mil) (Max=6.5mil) (Preferred=4mil) (All)	0
Width Constraint (Min=4.5mil) (Max=6mil) (Preferred=4.5mil) (InNetClass('NO_IMPEDANCE'))	0
Width Constraint (Min=6.4mil) (Max=50mil) (Preferred=20mil) (InNetClass('POWER_NETS'))	0
Width Constraint (Min=6mil) (Max=9.5mil) (Preferred=6mil) (InNet('DDR3_'))	0
Power Plane Connect Rule(Direct Connect)(Expansion=8mil) (Conductor Width=15mil) (Air Gap=6mil) (Entries=4) (All)	0
Acute Angle Constraint (Minimum=60.000) (All)	0
Hole Size Constraint (Min=6mil) (Max=100mil) (All)	0
Matched Lengths(Tolerance=50mil) (All)	0
Total	0

Comment	Quantity	Designator	Mfr	Ref Part No.	Footprint	Value	Rating	Tolerance	Rated Current	UW Inventory	Note
?	12	C1, C11, C16, C18, C20, C26, C28, C59, C64, C65, C67, C68	Murata	GRM158R4001 07M240L	C1210_IPC_H	100uF	A.3V		0		
?	2	C3, C39	Murata	GRM158R71C4 73KA01D	C0402_IPC_H	47nF	16V		?		
?	1	C3, C7, C9, C10, C31, C38, C38, C39, C40, C42, C118, C119, C120, C121, C122, C123, C124, C125, C126, C129, C130, C131, C132, C133, C134, C135, C136, C137, C138, C140, C142, C143, C144, C149	Murata (Panasonic ECG)	GRM158R4001 04K190 (EC) ZE0104K	C0201_IPC_H	0.1uF	A.3V		43	9	
?	2	C4, C5, C8, C19, C23, C25, C27, C29, C33, C55, C57, C40, C63, C109, C127, C128, C139, C141, C145, C146, C147, C148	Murata	GRM158R600J1 04K190	C0402_IPC_H	10uF	A.3V		?		
?	5	C4, C14, C17, C24, C26	TDK	C0124504047 04M25AC	C0805_M	47uF	A.3V		90	9	
?	20	C12, C13, C32, C36, C37, C45, C46, C48, C49, C50, C54, C58, C61, C62, C66, C91, C92, C100, C111, C117	Murata	GRM158R71C1 04KAB8D	C0402_IPC_H	0.1uF	16V		66	5	
?	1	C13, C21, C22, C65, C72, C73, C76, C78, C79, C81, C83, C85, C86, C89, C92, C93, C96, C97, C98, C99, C100, C102, C103, C104, C106, C108, C112, C113, C114, C116	Murata	GRM158R600J4 74K190	C0402_IPC_H	0.47uF	A.3V		?		
?	3	C34, C47, C51	AVX	C02704707MA 72A	C0402_IPC_H	4.7uF	16V		?		
?	1	C41, C43, C44	Panasonic ECG	C01-ZEH147H 04M25AC	C0201_IPC_H	470uF	25V		44	4	
?	2	C52, C53	Murata	GRM158R72A1 08010D	C0402_IPC_H	27pF	A.3V		?		
?	1	C56	Murata	GRM158R72A1 02K401D	C0402_IPC_H	1000pF	100V		?		
?	1	C70, C71, C75, C77, C80, C82, C84, C87, C90, C94, C101, C104, C105, C107, C115	TDK	C1005X50047 04M25AC	C0402_IPC_H	4.7uF	6.3V		90	3	
?	1	D1, D3, D9	Lite-On	L1ST-C1906KKT	LED0603_M	RED			58	7	
?	1	D2, D4, D7	Lite-On	L1ST-C1906SKT	LED0603_M	YELLOW			78	4	
?	1	D5, D6, D8	Lite-On	C1906GKT	LED0603_M	GREEN			70	1	
MINIDIMM	244	U13	NA	NA	minIDMM244				NA	Not a part	
DF1200015 -04104-P2	2	L1, L4	Murata	DFE250212F- 04M7M-P2	U2520_H	0.47uH	20%	?	?		
DK1000V4M	241-T	L2, L3, L5, L6, L8, L9	Taiyo Yuden	TK1000V4M24T1	L0402_H	240		300mA	0	47	
Wurth	744383230	L3	Wurth	74438323047	U2520_H	4.7uH	20%	?			
NTR2101P	1	O1	Device	NTR2101P	SOT23-H				?		
NDS311N	2	O2, O3	Device	NDS311N	SOT23-H				?		
?	1	R1, R31, R32, R55, R60, R75, R76, R77, R78, R80, R81, R82, R83, R89, R90, R91, R92, R93, R94, R96, R97, R99, R100, R142	Panasonic	ERJ-10NF100ZC R0201_IPC_H	10K	1%	?				
?	1	R2	Panasonic	ERJ-10NF100X R0402_IPC_H	4.64K	1%	?				
?	4	R3, R23, R35, R155	Panasonic ECG	2RKF1001X	R0402_IPC_H	1K	1%	?	1		
?	4	R4, R5, R8, R9, R14, R15, R19, R20, R40, R84, R86, R87, R88, R114, R122, R151, R154, R157, R162, R170, R171, R176,	Panasonic	ERJ-10NF100X R0402_IPC_H	4.7K	1%	?				
?	11	R6, R10, R66, R67, R68, R69, R70, R71, R79, R85	Panasonic ECG	2RKF5100X	R0402_IPC_H	510	1%	?	71	8	
?	6	R7, R11, R12, R13, R16, R17, R18, R21, R22, R29, R57, R74, R98, R101, R102, R105, R106, R108, R109, R110, R112, R117, R146, R147, R149, R150, R152, R153, R160, R161, R169	Panasonic ECG	ERJ-20EU200X	R0402_IPC_H	10K	5%	?	70	6	
?	6	R26, R27, R28, R73, R148, R165	Panasonic	ERJ-20EU200X	R0402_IPC_H	24K	1%	?	?		
?	7	R42, R44, R47, R126, R128, R159, R164	Panasonic ECG	2RKF2002X	R0402_IPC_H	20K	1%	?	3		
?	1	R49	Panasonic	ERJ-2A1B5762X	R0402_IPC_H	57.6K	0.1%	?			
?	1	R52, R53, R61, R62, R111, R116, R158, R163	Panasonic	ERJ-2A1B5762X	R0402_IPC_H	OPEN	1%	?	Do not assemble		
?	1	R56, R140	Panasonic	ERJ-2A1B212X	R0402_IPC_H	22.1K	0.1%	?			
?	4	R95, R101, R107, R113	Panasonic	ERJ-2A1B7580X	R0402_IPC_H	75	1%	?			
?	3	R104, R204, R209	Vishay	TKED	R0402_IPC_H	2.37K	1%	?			
?	2	R115, R154	Panasonic	ERJ-1GNF22R0C	R0201_IPC_H	22	1%	?			
?	1	R144	Panasonic ECG	2RKF664ZX	R0402_IPC_H	86.6K	0.1%	?	93		
?	1	R166, R167, R184	Panasonic ECG	2RKF908X	R0402_IPC_H	80.6	1%	?	92	2	
?	1	R175	Panasonic ECG	2RKF2400X	R0402_IPC_H	240	1%	?	71	0	
?	20	R200, R201, R202, S203, S204	Panasonic ECG	1GF40R02C	R0201_IPC_H	40.2	1%	?	96	2	
?	1	R208	Panasonic	ERJ-2A1B4122X	R0402_IPC_H	41.2K	0.1%	?			
?	1	R210	Panasonic	ERJ-2A1B4743X	R0402_IPC_H	47K	0.1%	?			
?	1	Texas Instruments	TPS62085	VS1ON-8_L					?		
?	1	U1, U5	Instruments	TPS62085	VS1ON-8_L				?		
AD7498C7	2	U2, U14	Analog	AD7498C7	CP-20-4N				?		
M14128 M16fj-96	3	U3	Micron	M1412812B16 JT-125	MIC1-JT-96				Any speed grade will work		
KXK	4	U4	Xilinx	KC7200 TCLG400C	CLG400						
AD73200- CLG400	1	U6	Microchip	25AA204-8f I/O/T	SOT-23-0T6_L				?		
25AA0264B T-I/O/T	1	U7	Microchip	ADP1755ACP2- R/T	CP-16-4L				?		
ADP1755ACP2- PZ_R7	1	U8	Analog	ADP1755ACP2- R/T	CP-16-4L				?		
TXS0102	1	U9	Texas Instruments	TXS0102DQER	X2SON-8_H				?		
U5071NL	1	U10	Pulse Electronics	U5071NL	U5071NL				?		
A69835	1	U11	Atheros	A69835	QFN40_H				?		
7544256- VST	1	U12	Microchip	25AA256-1/VST	TSSOP-328_L				?		
DS1819	1	U13	Maxim	DS1819R-10	SOT23_H				?	6	
TPS51200D -00B	1	U15	Instruments	TPS51200DRCR	DRK0010_V				Catalog	95	
XRCGB25M 00F3M008	1	U16	Murata	XRCGB25M008	XRCGB_L				?	11	
0	1	U17	F3M0080	XRCGB25M008	25MHz				?	03	
ASDM8-33.3	1	U18	Abracron	ASDM8-33.33	ABRA-ASDM8-4_V				?		

