ZYNQ-IPMC

**Hardware Specification and General Information**

# Description

ZYNQ-IPMC is a high versatile open-source self-contained Intelligent Platform Management Controller (IPMC) in a miniDIMM-244 mezzanine form factor with extended monitoring features targeted for Advance Telecommunications Computing Architecture (ATCA) applications in accordance with the PICMG 3.x standard.

# Features

* Self-contained IPMI compliant platform for ATCA applications:
  + Field-replaceable unit (FRU) information
  + Fault detection and reporting
  + MMC support via IPMB
* Extended monitoring and features:
  + Sub-millisecond fault response
  + Parallel sensor reading
  + Standard protocol support on GPIOs
  + Hardware accelerated feedback
* Single 3.3V supply and interfaces
* Open-source and NDA-free HW/FW/SW

# Hardware

* Powered by Xilinx Zynq-7020 or Z014S System-on-Chip (SoC)
  + Single-core or Dual-core ARM Cortex-A9 (667 MHz)
  + 256Mbytes of DDR3-1066 memory
  + 64Mbytes of QSPI flash storage
* 256Kbit EEPROM storage w/ unique MAC
* 1Gb ethernet w/ on-board transformers
* 109 fully configurable GPIOs
* 16 ADC inputs w/ 16-bit @ 10kSPS channel
* Master JTAG and UART interfaces

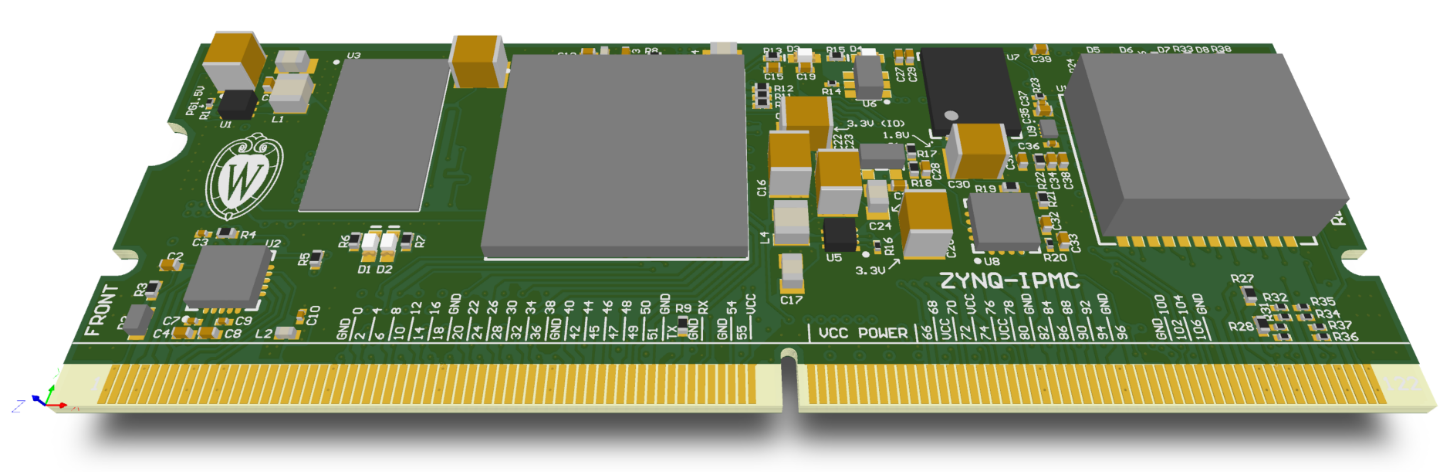


Figure 3.1 ZYNQ-IPMC (revB) rendering

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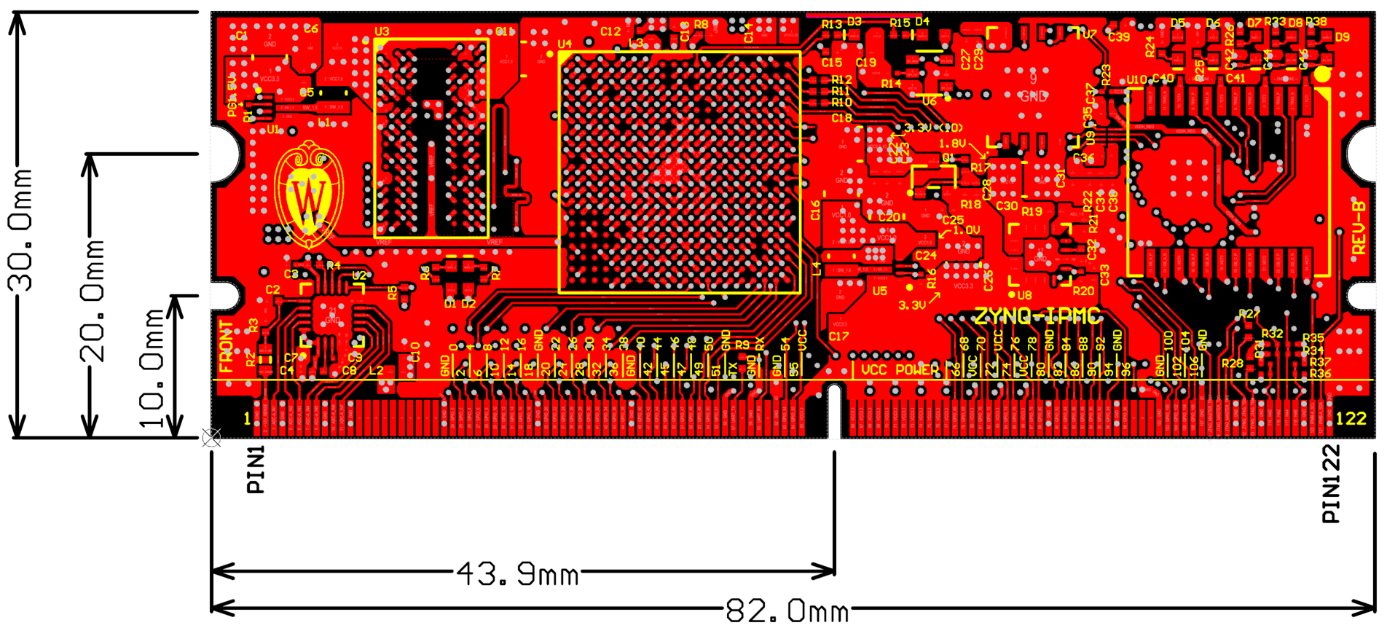
# Revision History

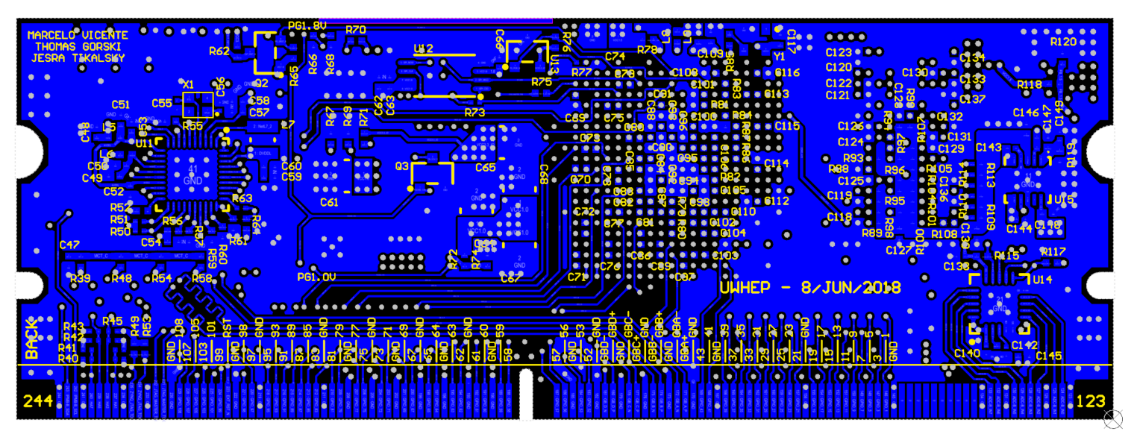
**Revision B (May 2019):**

* Adds measurements for power consumption for both Z7020 and Z7014S variants.
* Removes ‘DRAFT’ watermark, document no longer preliminary.

# Pin Configuration and Function

The following illustration is a representation of the ZYNQ-IPMC, as seen from the top (red) and bottom (blue) view.





## Pins by Function

Table 6.1 Pin type symbol definitions

|  |  |  |
| --- | --- | --- |
| **SYMBOL** | **PIN TYPE** | **DESCRIPTION** |
| A | Analog input | Analog input for sensing variable voltage levels |
| DIFF | Differential | Differential signal pair |
| I | Input | Input signal |
| I-PU | Input w/ pull-up | Input signal with on-board pull-up |
| I-PD | Input w/ pull-down | Input signal with on-board pull-down |
| O | Output | Output signal |
| I/O | Bidirectional | Bidirectional input or output signal |

Table 6.2 Pins by Function

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **GROUP** | **NAME** | **PIN NUMBER(S)** | **TYPE** | **LEVEL** | **DESCRIPTION** |
| Power | VCC | 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 80, 83, 86 | - | 3.3V | Main 3.3V supply |
| GND | 1, 4, 9, 12, 23, 34, 45, 55, 59, 62, 89, 97, 102, 107, 111, 114, 119, 122, 123, 126, 131, 134, 145, 156, 167, 170, 173, 176, 179, 182, 185, 190, 193, 196, 199, 202, 205, 208, 211, 219, 222, 230, 233, 236, 241, 244 | - | - | Logic ground |
| Analog | 12V\_SENSE | 2 | A | 12.0V | +12V sensing |
| ADC-A\_IN[1-7] | 3, 5, 6, 7, 8, 10, 11 | A | 2.5V | Bank A analog sensing |
| ADC-B\_IN[0-7] | 124, 125, 127, 128, 129, 130, 132, 133 | A | 2.5V | Bank B analog sensing |
| GPIO | GPIO\_[0-108] | 24, 146, 25, 147, 26, 148, 27, 149, 28, 150, 29, 151, 30, 152, 31, 153, 32, 154, 33, 155, 35, 157, 36, 158, 37, 159, 38, 160, 39, 161, 40, 162, 41, 163, 42, 164, 43, 165, 44, 166, 46, 168, 47, 169, 48, 49, 50, 51, 52, 53, 54, 55,183, 184, 54, 55, 186, 187, 188, 189, 191, 192, 194, 195, 197, 198, 78 , 200, 79, 201, 81, 203, 82, 204, 84, 206, 85, 207, 87, 209, 88, 210, 90, 212, 91, 213, 92, 214, 93, 215, 94, 216, 95, 217, 96, 218, 98, 220, 221, 224, 103, 225, 104, 226, 105, 227, 106, 228, 229 | I/O | 3.3V | General purpose input-outputs that can be configured to any standard or custom protocol |
| Ethernet | GB\_A\_[P,N] | 171, 172 | DIFF | 2.5V | 4-pair 1000BASE-T 1Gb ethernet after magnetics |
| GB\_B\_[P,N] | 174, 175 | DIFF |
| GB\_C\_[P,N] | 177, 178 | DIFF |
| GB\_D\_[P,N] | 180, 181 | DIFF |
| UART | UART\_TX | 57 | O | 3.3V | Serial console |
| UART\_RX | 60 | I |
| Reset | EXT\_RST\_N | 223 | I-PU | 3.3V | External reset, asserted low |
| Master JTAG | M-JTAG\_TRST | 108 | O | 3.3V | Master JTAG interface, drives a JTAG chain |
| M-JTAG\_TDO | 109 | I |
| M-JTAG\_TMS | 110 | O |
| M-JTAG\_TCK | 231 | O |
| M-JTAG\_TDI | 232 | O |
| ZYNQ JTAG | Z-JTAG\_TDO | 112 | O | 3.3V | Slave JTAG interface for Zynq firmware debugging and GDB access |
| Z-JTAG\_TMS | 113 | I-PU |
| Z-JTAG\_TCK | 234 | I-PU |
| Z-JTAG\_TDI | 235 | I-PU |
| Address | HA[0-7] ([[1]](#footnote-1)) | 115, 237, 116, 238, 117, 239, 118, 240 | I-PU | 1.8V | ATCA hardware address interface |
| IPMI Bus | IPMB-A\_SCL | 120 | I/O | 3.3V | IPMI bus interface, channel A |
| IPMB-A\_SDA | 121 | I/O |
| IPMB-B\_SCL | 242 | I/O | IPMI bus interface, channel B |
| IPMB-B\_SDA | 243 | I/O |
| - | NC | 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 58, 61, 99, 100, 101, 135, 136, 137, 138, 139, 140, 141, 142, 143, 144 | - | - | No connection |

# Specifications

## Absolute Maximum Ratings

over operating free-air temperature range

Table 7.1 Absolute Maximum Ratings

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | | | **MIN** | **MAX** | **UNIT** |
| VCC | Supply voltage range |  | -0.5 | 3.6 | V |
| VIN | Logic pin input voltage range (GPIO, UART, IPMI, etc.) |  | -0.4 | VCC+0.55 | V |
| VADC | Analog sense input range |  | -0.1 | 2.6 | V |

## Recommended Operating Conditions

over operating free-air temperature range

Table 7.2 Recommended Operating Conditions

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | | | | **MIN** | **TYP** | **MAX** | **UNIT** |
| VCC | Supply voltage | |  | -0.2 | 3.3 | 3.45 | V |
| VIN | Logic pin input voltage as LVCMOS33 | Logic LOW | | -0.3 | - | 0.8 | V |
| Logic HIGH | | 2.0 | - | 3.45 | V |
| VOUT | Logic pin output voltage as LVCMOS33 | Logic LOW | | - | - | 0.4 | V |
| Logic HIGH | | VCC-0.4 | - | VCC | V |
| IOUT | Maximum logic pin output current | |  | - | - | 16.0 | mA |
| IIN | Maximum current in a logic pin when forward biasing the clamp diode | |  | - | - | 10.0 | mA |
| VADC | Standard analog sensing pins voltage range | |  | 0.0 | - | 2.5 | V |
| VADC-12V | +12V sensing pin voltage range | |  | 0.0 |  | 14.1 | V |
| FADC | Analog sensing sampling frequency | |  |  |  | 10 | kHz |
| PIN | Total power consumption[[2]](#footnote-2) | Z7020 | | - | 2.15 | - | W |
| Z7014S | | - | 1.95 | - | W |

## Timing Characteristics

based on PCB routing

Table 7.3 Timing Characteristics

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | | | **TYP** | **UNIT** |
| tΔETH-DIFF | Propagation delay between ethernet differential P and N signals | Pair A | 1.8 | ps |
| Pair B | 0.6 | ps |
| Pair C | -5.8 | ps |
| Pair D | -5.5 | ps |
| tΔETH-PAIRS | Maximum propagation delay between ethernet pairs | B to D | 40.1 | ps |
| fADC | Maximum analog sensing sampling frequency |  | 10.0 | kHz |

# Architecture

**ZYNQ 7014S**

256MB DDR3

PHY

Magnetics

ADC

ADC-A\_IN

ADC

ADC-B\_IN

1000BASE-T

IPMB A/B

JTAG

GPIO

UART

64MB Flash

256Kbit EEPROM

MAC EEPROM

PS/PL LEDs

Status LEDs

x109

SPI

SPI

QSPI

SPI

SPI

RGMII

x8

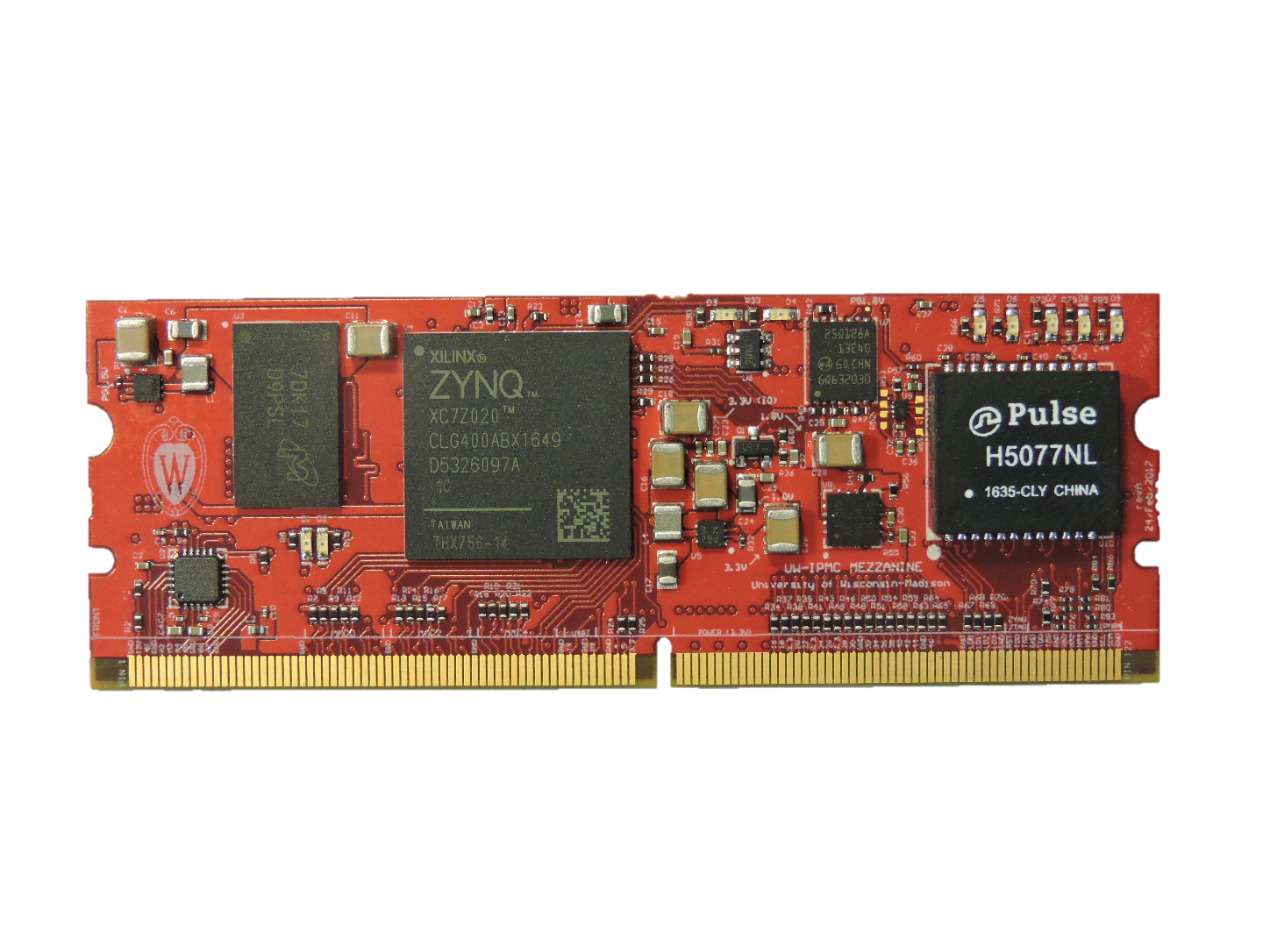
x8

## Programable and Status LEDs

A total of 9 LEDs are present on-board as seen in Figure 8.1. Table 8.1 as a brief description.

Table 8.1 On-board LED description

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **LED #** | **NAME** | **COLOR** | **DRIVER** | **DESCRIPTION** |
| 1 | PS\_LED\_RED | Red | Zynq PS | Programmable from the Zynq Processing System (PS) |
| 2 | PS\_LED\_YELLOW | Yellow | Zynq PS |
| 3 | POWER\_ON | Green | Power Supply | Indicates the card has power |
| 4 | POWER\_GOOD | Green | Power Supply | Indicates a good power sequencing |
| 5 | ETH\_10\_100 | Yellow | Ethernet Phy | 100M link when active, 10M otherwise |
| 6 | ETH\_1000 | Green | Ethernet Phy | 1000M when active, ETH\_10\_100 off |
| 7 | ETH\_ACT | Red | Ethernet Phy | Active link when on, activity when blinking |
| 8 | PL\_LED\_RED | Red | Zynq PL | Usable from the Zynq Programable Logic (PL) |
| 9 | PL\_LED\_YELLOW | Yellow | Zynq PL |



**1**

**2**

**3 4 5 6 7**

**8 9**

Figure 8.1 On-board LED locations

# ATCA Requirements

## Microswitch

A handle switch can be used to turn on and off the blade payload as shown in section D.1.1 of PICMG 3.0. Any available GPIO can be used to interface with microswitch being used. An external pull-up of 1kΩ or less is recommended to assert the signal when the switch is open as seen in Figure 9.1.

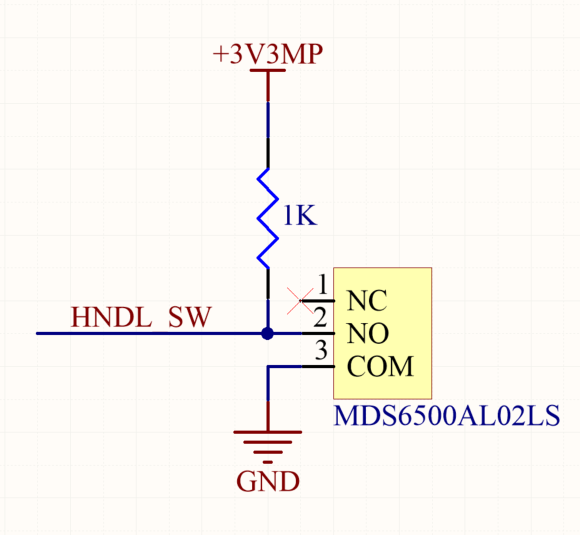


Figure 9.1 Microswitch Interface

## Hardware Address

The hardware address is set in accordance with PICMG 3.0 REQ 3.37: “Each IPM Controller in the Shelf shall be assigned a seven (7) bit Hardware Address and a corresponding odd parity bit that are “hardwired” at each FRU location on the Backplane or elsewhere in the Shelf. The FRU location shall indicate a logic one by leaving the address pin floating. A logic zero shall be indicated by connecting the address pin to the Logic Ground.”

Hardware Address pins are to be connected directly to the ATCA blade Zone-1 hardware address pins.

## IPMB A/B

IPMB A and B channels are available in accordance with PICMG 3.0 REQ 3.543: “IPM Controllers shall implement connections to IPMB-A and IPMB-B”.

IPMB interfaces are to be connected directly to the ATCA blade Zone-1 IPMB A/B pins.

## LEDs

Face Plate indications are described in section 3.2.5 of PICMG 3.0. These correspond to LED interfaces and should be connected to any available GPIO since assignment and configuration takes places in firmware.

These LEDs are recommended to be powered by the 3.3V management power (MP) source while being biased by 332Ω resistors as seen in Figure 9.2.

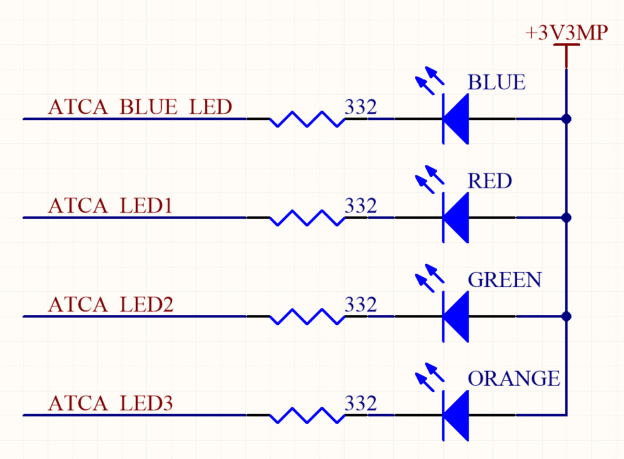


Figure 9.2 ATCA LED Interface

# Design considerations

## Analog Inputs

Analog sensing connections need to be dimensioned by having two factors in consideration: the maximum allowed voltage of 2.5V on analog sensing pins and the Nyquist frequency of 5kHz based on the sampling rate of 10kHz. In most cases a voltage divider is required between the analog pin and the and the signal, as shown in Figure 10.1.

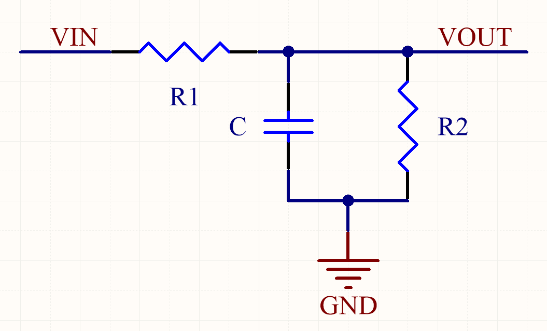


Figure 10.1 Voltage divider

Table 10.1 Example divider circuit values

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **INPUT VOLTAGE (V)** | **R1 (Ω)** | **R2 (Ω)** | **C (uF)** | **DIVIDER FACTOR** | **NOM. OUTPUT VOLTAGE (V)** | **MAX. INPUT VOLTAGE (V)** | **CUTOFF FREQ (Hz)** |
| 5.00 | 4640 | 3320 | 0.1 | 0.417 | 2.09 | 5.99 | 343 |
| 3.30 | 2740 | 4640 | 0.22 | 0.629 | 2.08 | 3.98 | 264 |
| 2.50 | 1000 | 4640 | 1.0 | 0.823 | 2.06 | 3.04 | 159 |
| 1.20 | 100 | - | 10.0 | 1.000 | 1.20 | 2.50 | 159 |

## Ethernet

Four differential pairs provide a 1000BASE-T ethernet connectivity. On-board magnetics are present on the IPMC and therefore these are not required externally. Each pair should be length matched and routed with 100Ω differential traces.

## General Purpose I/O (GPIO)

All 109 available GPIOs are connected to Zynq’s Programming Logic (PL) which allows for easy implementation of most standard protocols (SPI, I2C, UART, etc) as well as other custom interfaces. Individual GPIOs can be internally configured to be pulled-up, pulled-down and be internally terminated while supporting TTL and LVCMOS logic levels.

GPIOs are divided into 3 majors banks, highlighted in green, orange and blue in Figure 13.1, Table 13.1 and Table 13.2.

Table 10.2 GPIOs Banking

|  |  |  |  |
| --- | --- | --- | --- |
| **BANK COLOR** | **BANK NUMBER** | **GPIO COUNT** | **GPIO NUMBER** |
| Green | 13 | 15 | 0, 2, 4, 6, 8, 10, 12, 14, 16, 18, 41, 43, 52-54 |
| Orange | 34 | 49 | 1, 3, 5, 7, 9, 11, 13, 15, 17, 19-40, 42, 44-51, 55-63 |
| Blue | 35 | 45 | 64-108 |

**It is recommended that for moderate speed protocols the same bank is used to define the interface since this will facilitate internal FPGA routing, simplify clocking and improve signal quality. For protocols that require clock reception it is recommended to use a clock capable GPIO as indicated in** Table 13.2**.**

## Master JTAG

Dedicated pins provide a JTAG Master interface that can drive other JTAG capable devices. The IPMC will support Xilinx Virtual Cable (XVC) through TCP/IP.

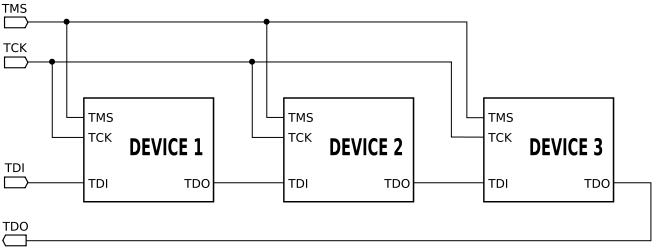


Figure 10.2 Example JTAG chain implementation (from Wikipedia)

## Debugging JTAG

A standard Xilinx JTAG header is recommended to be present and connected to these pins, or any other alternative approach. JTAG access greatly facilitates debugging and development of custom IPMC builds.

No pull-ups are required externally on input lines.

## IPMC Reset

An external reset of the IPMC can be issued by pulling down EXT\_RST\_N to ground. It is recommended to leave this pin floating or connect it to a push bottom that sets the logic state to logic ground when pressed.

# Mechanical and Mating

A miniDIMM DDR3 surface mount socket with 22.5 degrees insertion angle is recommended due to height restrictions imposed by PICMG 3.0 REQ 2.19: “Including tolerance accumulations, the maximum height of components (other than Component Side 1 covers or components under those Component Side 1 covers) in a single-Slot Front Board shall be 21.33 mm.”. This will assure that the IPMC won’t exceed the ATCA height envelope. Two Molex connectors are recommended:

* Molex 87783-0301 (IPMC front facing up)
* Molex 78035-0301 (IPMC front facing down)

Components are allowed under the IPMC but their height should be taken into consideration.

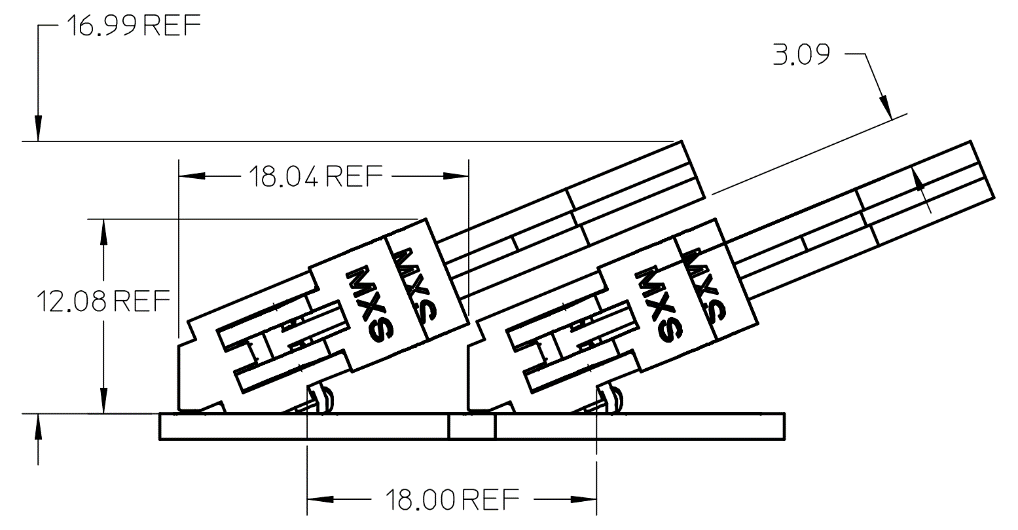


Figure 11.1 Molex 87783-0301 side view



Figure 11.2 IPMC height measurement

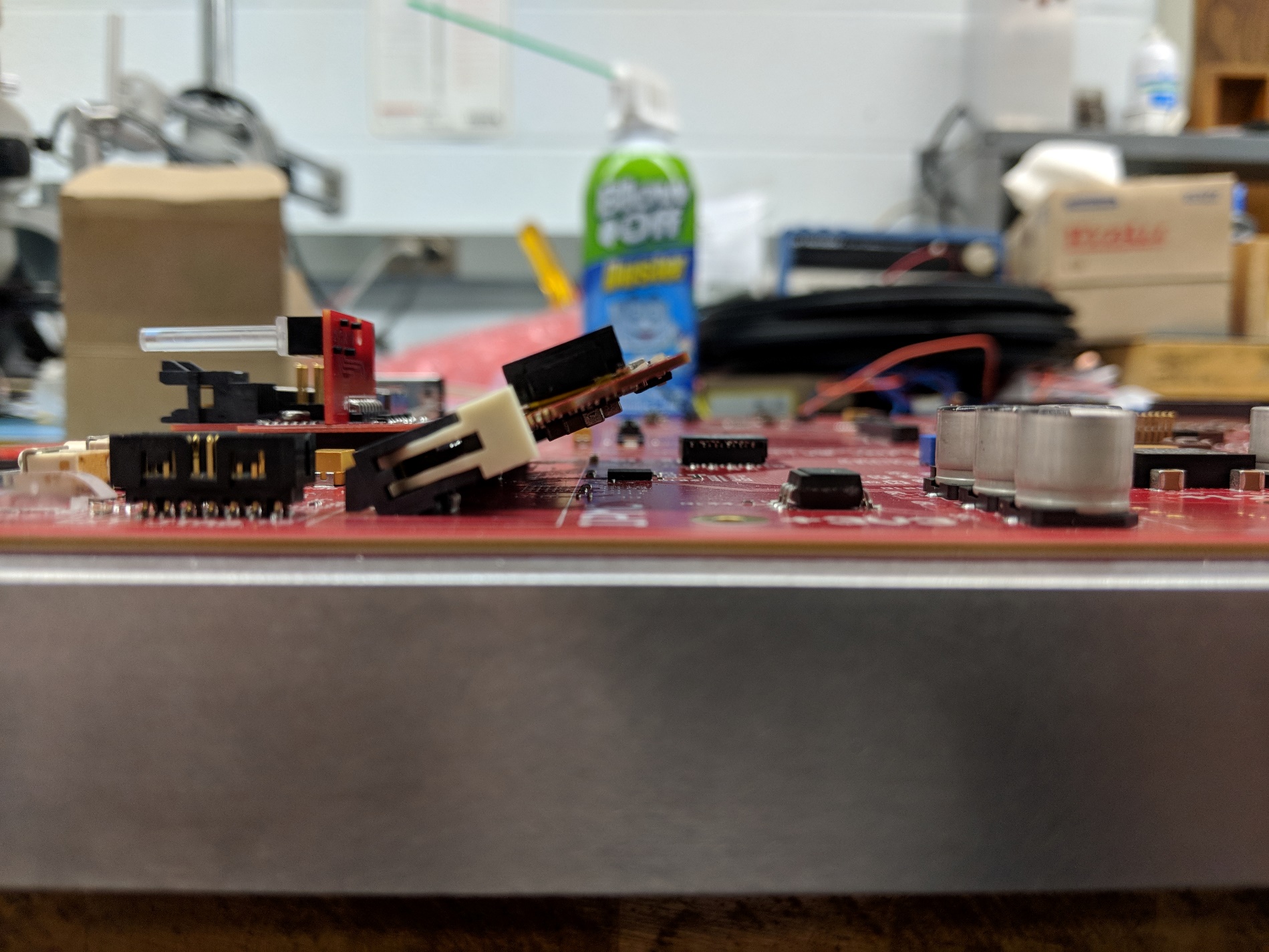


Figure 11.3 Observable clearance from IPMC to main board

# 

# Future Topics

Items planned to be added in a later revision of this document:

* Detailed architecture description (Ethernet PHY, ADCs, power sequencing, etc.)
* Operation Conditions -> Power consumption
* ATCA Interfaces -> MMC

# Appendix

## Schematic Symbol

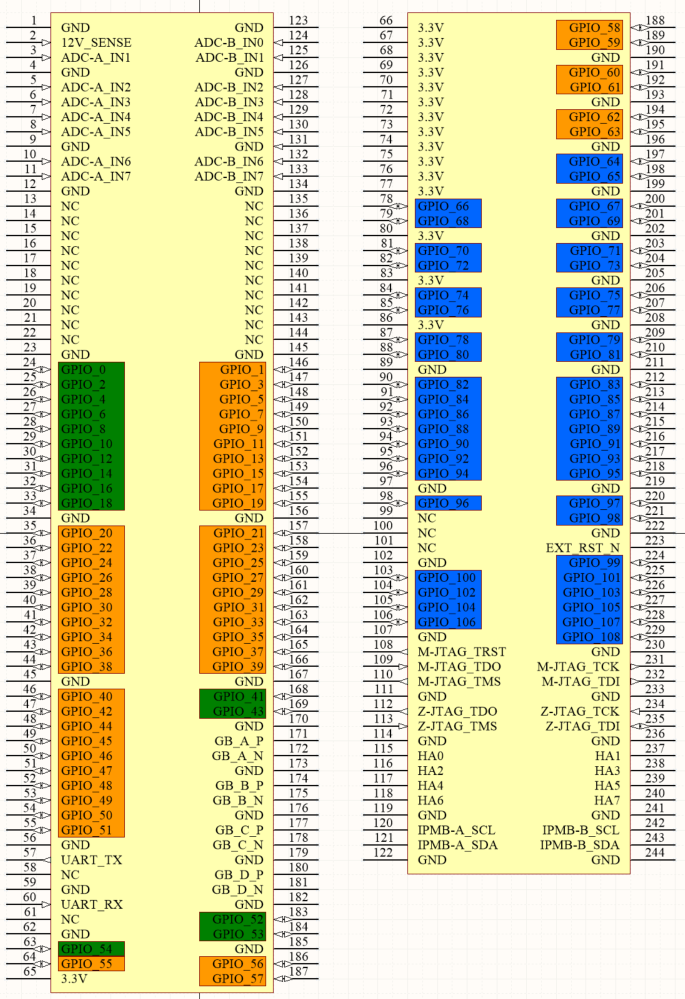


Figure 13.1 Altium Schematic Symbol

## Pin Assignment by Location

Table 13.1 Pin assignment by Location

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **NAME** | **PIN** | **PIN** | **NAME** |  | **NAME** | **PIN** | **PIN** | **NAME** |
| GND | **1** | **123** | GND |  | VCC3.3 | **66** | **188** | GPIO\_58 |
| +12V\_SENSE | **2** | **124** | ADC-B\_IN0 |  | VCC3.3 | **67** | **189** | GPIO\_59 |
| ADC-A\_IN1 | **3** | **125** | ADC-B\_IN1 |  | VCC3.3 | **68** | **190** | GND |
| GND | **4** | **126** | GND |  | VCC3.3 | **69** | **191** | GPIO\_60 |
| ADC-A\_IN2 | **5** | **127** | ADC-B\_IN2 |  | VCC3.3 | **70** | **192** | GPIO\_61 |
| ADC-A\_IN3 | **6** | **128** | ADC-B\_IN3 |  | VCC3.3 | **71** | **193** | GND |
| ADC-A\_IN4 | **7** | **129** | ADC-B\_IN4 |  | VCC3.3 | **72** | **194** | GPIO\_62 |
| ADC-A\_IN5 | **8** | **130** | ADC-B\_IN5 |  | VCC3.3 | **73** | **195** | GPIO\_63 |
| GND | **9** | **131** | GND |  | VCC3.3 | **74** | **196** | GND |
| ADC-A\_IN6 | **10** | **132** | ADC-B\_IN6 |  | VCC3.3 | **75** | **197** | GPIO\_64 |
| ADC-A\_IN7 | **11** | **133** | ADC-B\_IN7 |  | VCC3.3 | **76** | **198** | GPIO\_65 |
| GND | **12** | **134** | GND |  | VCC3.3 | **77** | **199** | GND |
| NC | **13** | **135** | NC |  | GPIO\_66 | **78** | **200** | GPIO\_67 |
| NC | **14** | **136** | NC |  | GPIO\_68 | **79** | **201** | GPIO\_69 |
| NC | **15** | **137** | NC |  | VCC3.3 | **80** | **202** | GND |
| NC | **16** | **138** | NC |  | GPIO\_70 | **81** | **203** | GPIO\_71 |
| NC | **17** | **139** | NC |  | GPIO\_72 | **82** | **204** | GPIO\_73 |
| NC | **18** | **140** | NC |  | VCC3.3 | **83** | **205** | GND |
| NC | **19** | **141** | NC |  | GPIO\_74 | **84** | **206** | GPIO\_75 |
| NC | **20** | **142** | NC |  | GPIO\_76 | **85** | **207** | GPIO\_77 |
| NC | **21** | **143** | NC |  | VCC3.3 | **86** | **208** | GND |
| NC | **22** | **144** | NC |  | GPIO\_78 | **87** | **209** | GPIO\_79 |
| GND | **23** | **145** | GND |  | GPIO\_80 | **88** | **210** | GPIO\_81 |
| GPIO\_0 | **24** | **146** | GPIO\_1 |  | GND | **89** | **211** | GND |
| GPIO\_2 | **25** | **147** | GPIO\_3 |  | GPIO\_82 | **90** | **212** | GPIO\_83 |
| GPIO\_4 | **26** | **148** | GPIO\_5 |  | GPIO\_84 | **91** | **213** | GPIO\_85 |
| GPIO\_6 | **27** | **149** | GPIO\_7 |  | GPIO\_86 | **92** | **214** | GPIO\_87 |
| GPIO\_8 | **28** | **150** | GPIO\_9 |  | GPIO\_88 | **93** | **215** | GPIO\_89 |
| GPIO\_10 | **29** | **151** | GPIO\_11 |  | GPIO\_90 | **94** | **216** | GPIO\_91 |
| GPIO\_12 | **30** | **152** | GPIO\_13 |  | GPIO\_92 | **95** | **217** | GPIO\_93 |
| GPIO\_14 | **31** | **153** | GPIO\_15 |  | GPIO\_94 | **96** | **218** | GPIO\_95 |
| GPIO\_16 | **32** | **154** | GPIO\_17 |  | GND | **97** | **219** | GND |
| GPIO\_18 | **33** | **155** | GPIO\_19 |  | GPIO\_96 | **98** | **220** | GPIO\_97 |
| GND | **34** | **156** | GND |  | NC | **99** | **221** | GPIO\_98 |
| GPIO\_20 | **35** | **157** | GPIO\_21 |  | NC | **100** | **222** | GND |
| GPIO\_22 | **36** | **158** | GPIO\_23 |  | NC | **101** | **223** | EXT\_RST\_N |
| GPIO\_24 | **37** | **159** | GPIO\_25 |  | GND | **102** | **224** | GPIO\_99 |
| GPIO\_26 | **38** | **160** | GPIO\_27 |  | GPIO\_100 | **103** | **225** | GPIO\_101 |
| GPIO\_28 | **39** | **161** | GPIO\_29 |  | GPIO\_102 | **104** | **226** | GPIO\_103 |
| GPIO\_30 | **40** | **162** | GPIO\_31 |  | GPIO\_104 | **105** | **227** | GPIO\_105 |
| GPIO\_32 | **41** | **163** | GPIO\_33 |  | GPIO\_106 | **106** | **228** | GPIO\_107 |
| GPIO\_34 | **42** | **164** | GPIO\_35 |  | GND | **107** | **229** | GPIO\_108 |
| GPIO\_36 | **43** | **165** | GPIO\_37 |  | M-JTAG\_TRST | **108** | **230** | GND |
| GPIO\_38 | **44** | **166** | GPIO\_39 |  | M-JTAG\_TDO | **109** | **231** | M-JTAG\_TCK |
| GND | **45** | **167** | GND |  | M-JTAG\_TMS | **110** | **232** | M-JTAG\_TDI |
| GPIO\_40 | **46** | **168** | GPIO\_41 |  | GND | **111** | **233** | GND |
| GPIO\_42 | **47** | **169** | GPIO\_43 |  | Z-JTAG\_TDO | **112** | **234** | Z-JTAG\_TCK |
| GPIO\_44 | **48** | **170** | GND |  | Z-JTAG\_TMS | **113** | **235** | Z-JTAG\_TDI |
| GPIO\_45 | **49** | **171** | GB\_A\_P |  | GND | **114** | **236** | GND |
| GPIO\_46 | **50** | **172** | GB\_A\_N |  | HA0 | **115** | **237** | HA1 |
| GPIO\_47 | **51** | **173** | GND |  | HA2 | **116** | **238** | HA3 |
| GPIO\_48 | **52** | **174** | GB\_B\_P |  | HA4 | **117** | **239** | HA5 |
| GPIO\_49 | **53** | **175** | GB\_B\_N |  | HA6 | **118** | **240** | HA7 |
| GPIO\_50 | **54** | **176** | GND |  | GND | **119** | **241** | GND |
| GPIO\_51 | **55** | **177** | GB\_C\_P |  | IPMB-A\_SCL | **120** | **242** | IPMB-B\_SCL |
| GND | **56** | **178** | GB\_C\_N |  | IPMB-A\_SDA | **121** | **243** | IPMB-B\_SDA |
| UART\_TX | **57** | **179** | GND |  | GND | **122** | **244** | GND |
| NC | **58** | **180** | GB\_D\_P |  |  |  |  |  |
| GND | **59** | **181** | GB\_D\_N |  |  |  |  |  |
| UART\_RX | **60** | **182** | GND |  |  |  |  |  |
| NC | **61** | **183** | GPIO\_52 |  |  |  |  |  |
| GND | **62** | **184** | GPIO\_53 |  |  |  |  |  |
| GPIO\_54 | **63** | **185** | GND |  |  |  |  |  |
| GPIO\_55 | **64** | **186** | GPIO\_56 |  |  |  |  |  |
| VCC3.3 | **65** | **187** | GPIO\_57 |  |  |  |  |  |

## GPIO Banking and Assignment

Table 13.2 GPIO-Zynq assignment

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **GPIO** | **IPMI PIN** | **BANK** | **ZYNQ PIN** | **CLOCK INPUT?** |  | **GPIO** | **IPMI PIN** | **BANK** | **ZYNQ PIN** | **CLOCK INPUT?** |
| 0 | 24 | 13 | U5 | - |  | 55 | 64 | 34 | R16 | - |
| 1 | 146 | 34 | P14 | - |  | 56 | 186 | 34 | R17 | - |
| 2 | 25 | 13 | T5 | - |  | 57 | 187 | 34 | R18 | - |
| 3 | 147 | 34 | T10 | - |  | 58 | 188 | 34 | N17 | - |
| 4 | 26 | 13 | U8 | - |  | 59 | 189 | 34 | P18 | - |
| 5 | 148 | 34 | T11 | - |  | 60 | 191 | 34 | P15 | - |
| 6 | 27 | 13 | U9 | - |  | 61 | 192 | 34 | P16 | - |
| 7 | 149 | 34 | T12 | - |  | 62 | 194 | 34 | T19 | - |
| 8 | 28 | 13 | W8 | - |  | 63 | 195 | 34 | R19 | - |
| 9 | 150 | 34 | T14 | - |  | 64 | 197 | 35 | N15 | - |
| 10 | 29 | 13 | W9 | - |  | 65 | 198 | 35 | N16 | - |
| 11 | 151 | 34 | U12 | - |  | 66 | 78 | 35 | M14 | - |
| 12 | 30 | 13 | W10 | - |  | 67 | 200 | 35 | M15 | - |
| 13 | 152 | 34 | T15 | - |  | 68 | 79 | 35 | M17 | - |
| 14 | 31 | 13 | W11 | - |  | 69 | 201 | 35 | M18 | - |
| 15 | 153 | 34 | V12 | - |  | 70 | 81 | 35 | M19 | - |
| 16 | 32 | 13 | Y11 | - |  | 71 | 203 | 35 | M20 | - |
| 17 | 154 | 34 | W13 | - |  | 72 | 82 | 35 | L14 | - |
| 18 | 33 | 13 | Y12 | - |  | 73 | 204 | 35 | L15 | - |
| 19 | 155 | 34 | V13 | - |  | 74 | 84 | 35 | L16 | Limited |
| 20 | 35 | 34 | R14 | - |  | 75 | 206 | 35 | L17 | Limited |
| 21 | 157 | 34 | W18 | - |  | 76 | 85 | 35 | L20 | - |
| 22 | 36 | 34 | W15 | - |  | 77 | 207 | 35 | L19 | - |
| 23 | 158 | 34 | V16 | - |  | 78 | 87 | 35 | K14 | - |
| 24 | 37 | 34 | T16 | - |  | 79 | 209 | 35 | J14 | - |
| 25 | 159 | 34 | T17 | - |  | 80 | 88 | 35 | K17 | Yes |
| 26 | 38 | 34 | U17 | - |  | 81 | 210 | 35 | K16 | - |
| 27 | 160 | 34 | Y18 | - |  | 82 | 90 | 35 | K18 | Yes |
| 28 | 39 | 34 | Y14 | - |  | 83 | 212 | 35 | G14 | - |
| 29 | 161 | 34 | W16 | - |  | 84 | 91 | 35 | J19 | - |
| 30 | 40 | 34 | W14 | - |  | 85 | 213 | 35 | K19 | - |
| 31 | 162 | 34 | V17 | - |  | 86 | 92 | 35 | J16 | - |
| 32 | 41 | 34 | U14 | Limited |  | 87 | 214 | 35 | J15 | - |
| 33 | 163 | 34 | W19 | - |  | 88 | 93 | 35 | J20 | - |
| 34 | 42 | 34 | Y16 | - |  | 89 | 215 | 35 | H20 | - |
| 35 | 164 | 34 | Y19 | - |  | 90 | 94 | 35 | J18 | - |
| 36 | 43 | 34 | V15 | - |  | 91 | 216 | 35 | H18 | - |
| 37 | 165 | 34 | V18 | - |  | 92 | 95 | 35 | H17 | Yes |
| 38 | 44 | 34 | Y17 | - |  | 93 | 217 | 35 | H16 | Yes |
| 39 | 166 | 34 | W20 | - |  | 94 | 96 | 35 | H15 | - |
| 40 | 46 | 34 | U15 | Limited |  | 95 | 218 | 35 | G15 | - |
| 41 | 168 | 13 | W6 | - |  | 96 | 98 | 35 | G17 | - |
| 42 | 47 | 34 | U18 | Yes |  | 97 | 220 | 35 | G18 | - |
| 43 | 169 | 13 | V6 | - |  | 98 | 221 | 35 | G19 | - |
| 44 | 48 | 34 | P19 | Yes |  | 99 | 224 | 35 | G20 | - |
| 45 | 49 | 34 | N18 | Yes |  | 100 | 103 | 35 | F16 | - |
| 46 | 50 | 34 | N20 | Limited |  | 101 | 225 | 35 | F20 | - |
| 47 | 51 | 34 | U19 | Yes |  | 102 | 104 | 35 | F17 | - |
| 48 | 52 | 34 | P20 | Limited |  | 103 | 226 | 35 | E18 | - |
| 49 | 53 | 34 | V20 | - |  | 104 | 105 | 35 | D18 | - |
| 50 | 54 | 34 | U20 | - |  | 105 | 227 | 35 | E19 | - |
| 51 | 55 | 34 | T20 | - |  | 106 | 106 | 35 | D19 | - |
| 52 | 183 | 13 | V10 | - |  | 107 | 228 | 35 | F19 | - |
| 53 | 184 | 13 | V11 | - |  | 108 | 229 | 35 | D20 | - |
| 54 | 63 | 13 | Y13 | - |  |  |  |  |  |  |

1. Hardware Address pins should not be driven, instead they should be left floating or connected to GND. [↑](#footnote-ref-1)
2. Obtained from real measurements using an IPMC testboard. [↑](#footnote-ref-2)