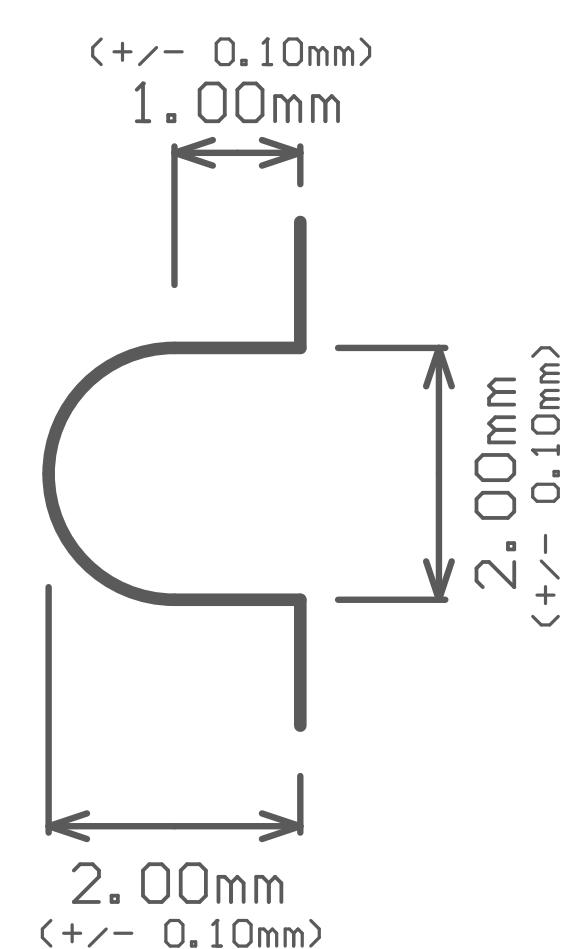
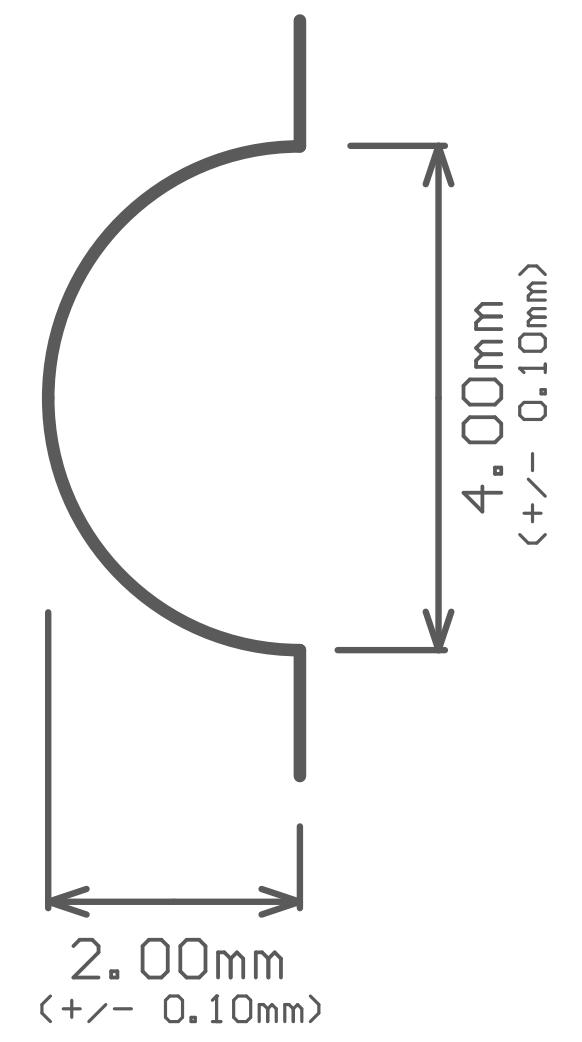


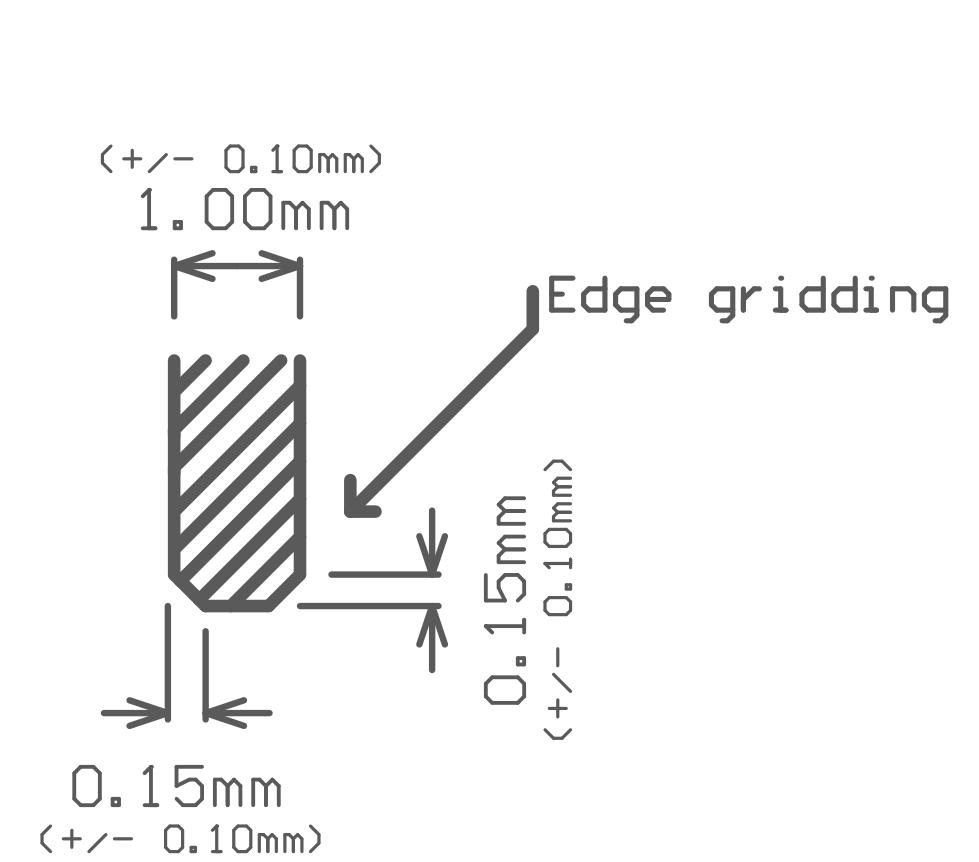
Detail 1



Detail 2

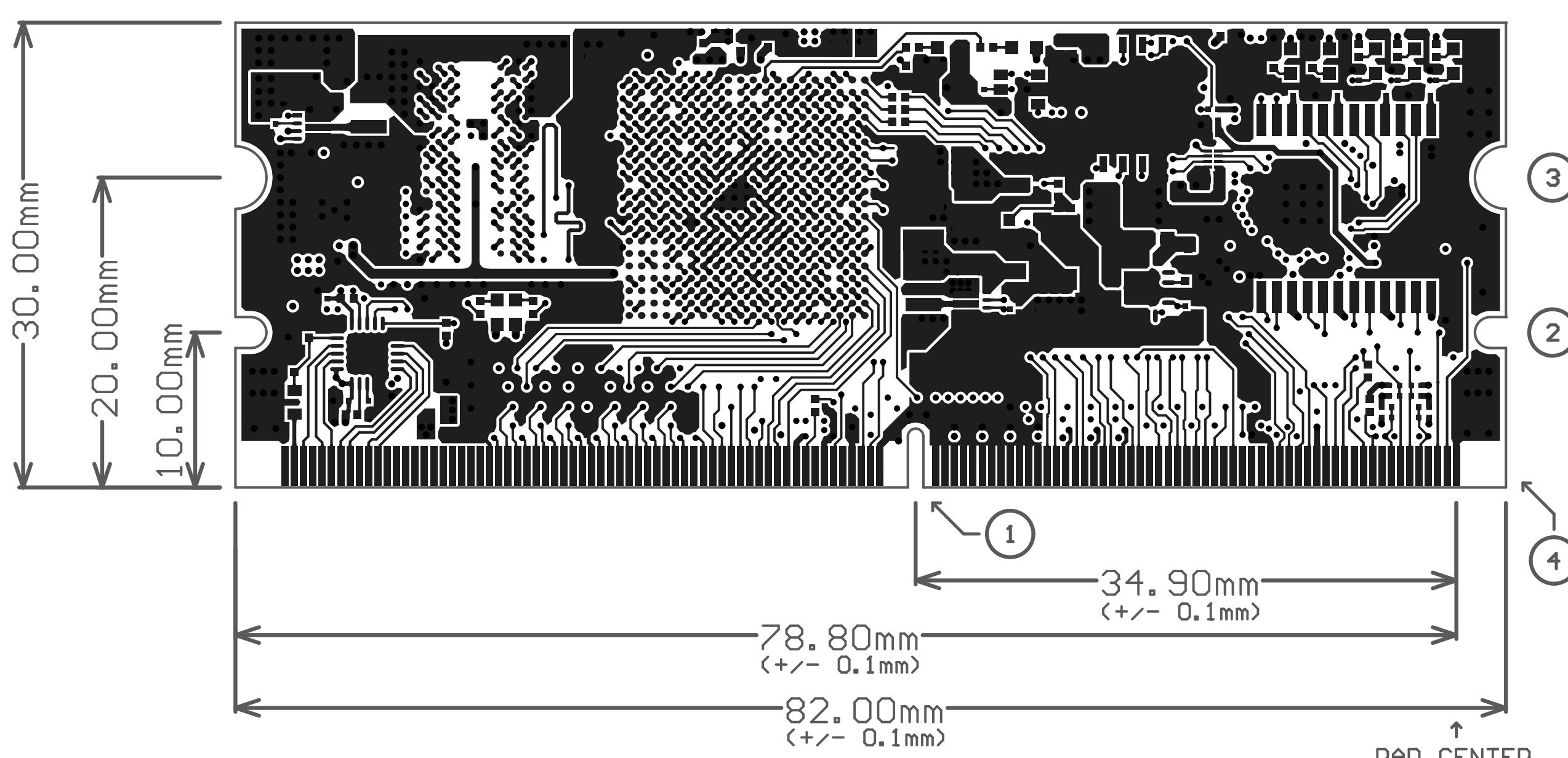


Detail 3

Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)

Layer 1 - Signal (Copper)



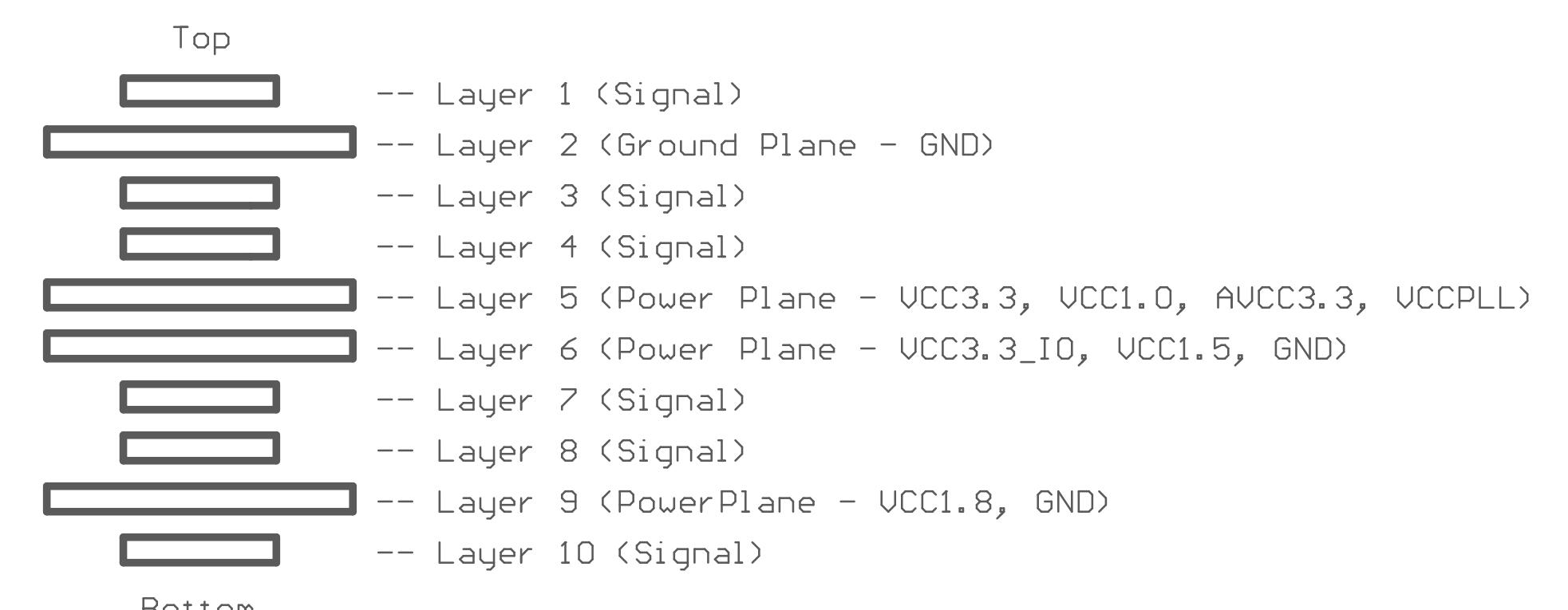
Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (Class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin—Madison
Madison, WI 53706

ENGINEER:
Vicente, M.

TITLE:
ZYNQ-IPMC

PCB DESIGNER:
Vicente, M.

DATE:
06JUN2019

PART NO.:

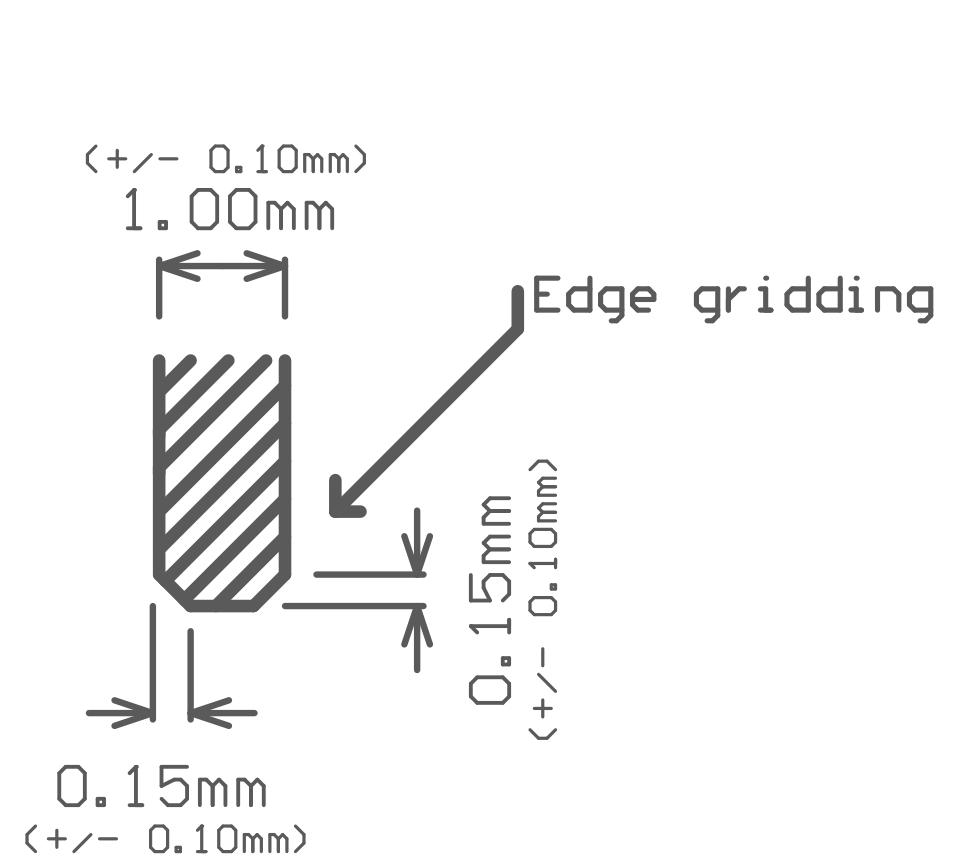
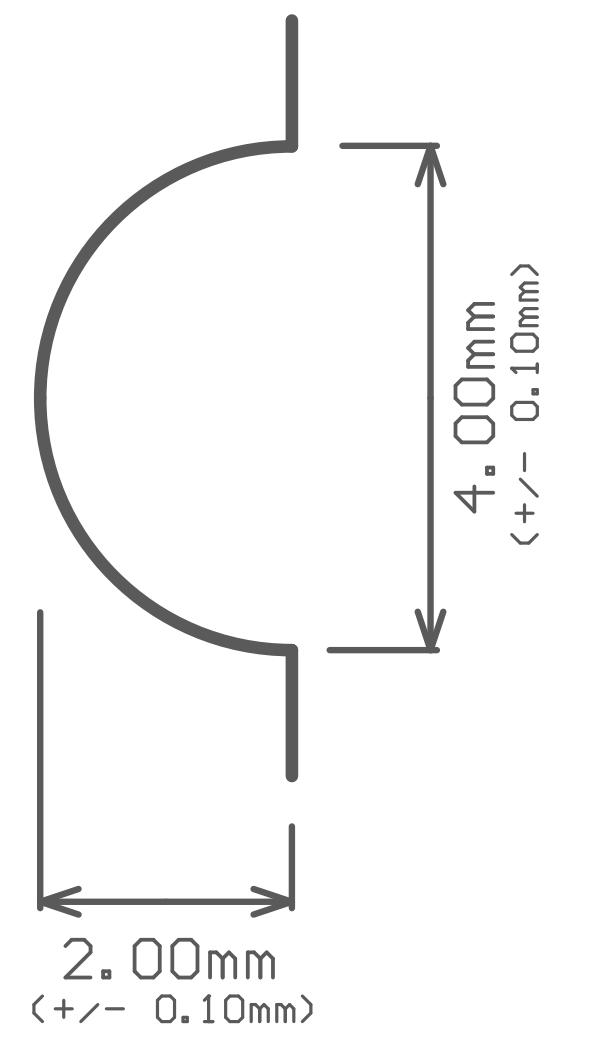
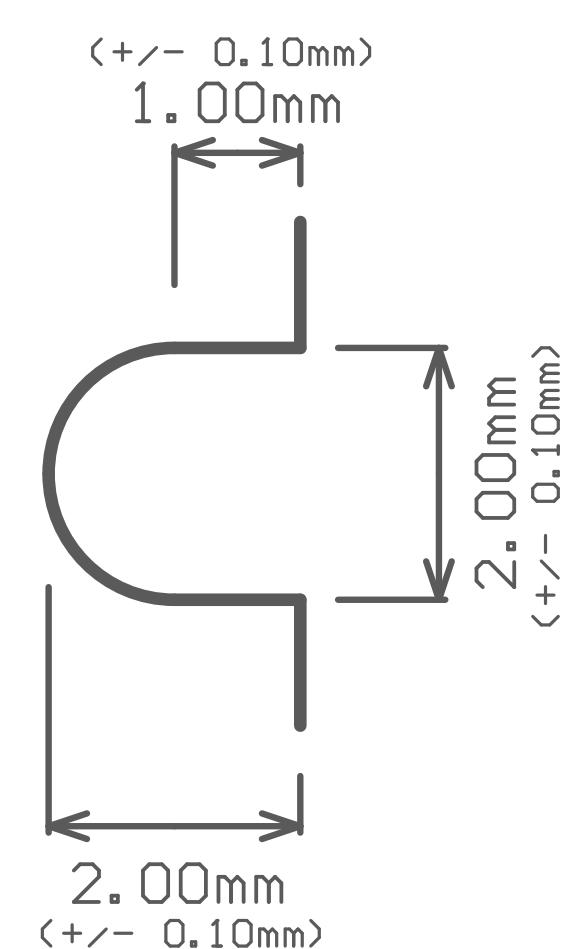
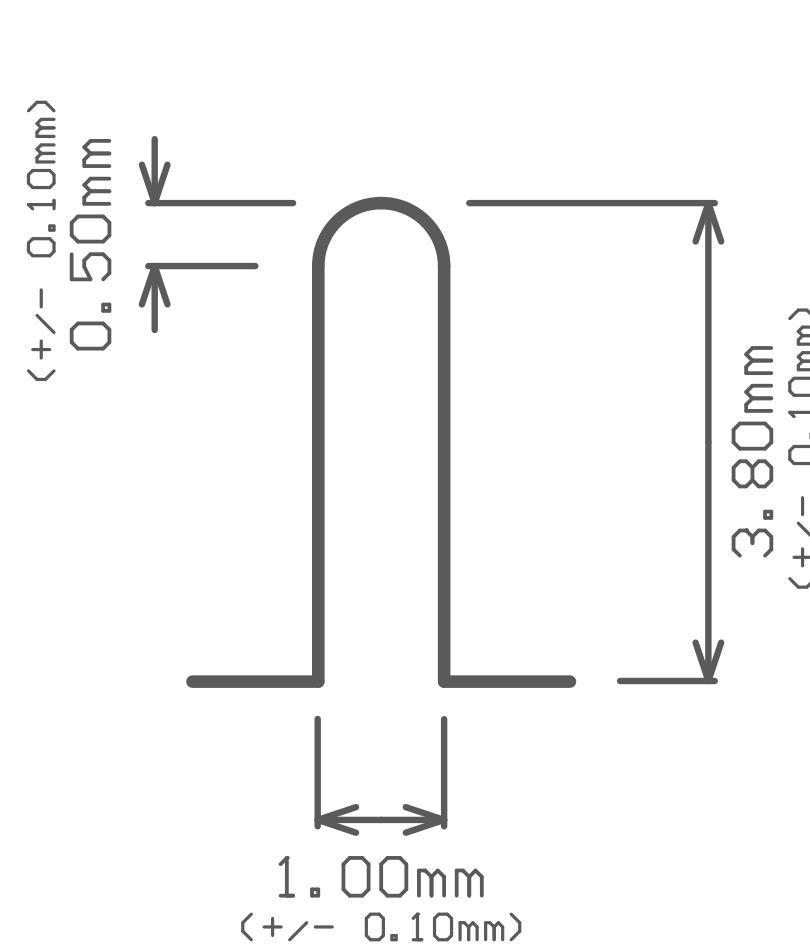
REV:

FILE NAME:
ZYNQ_IPMC.PCBDOC

DWG NO.:

SCALE:

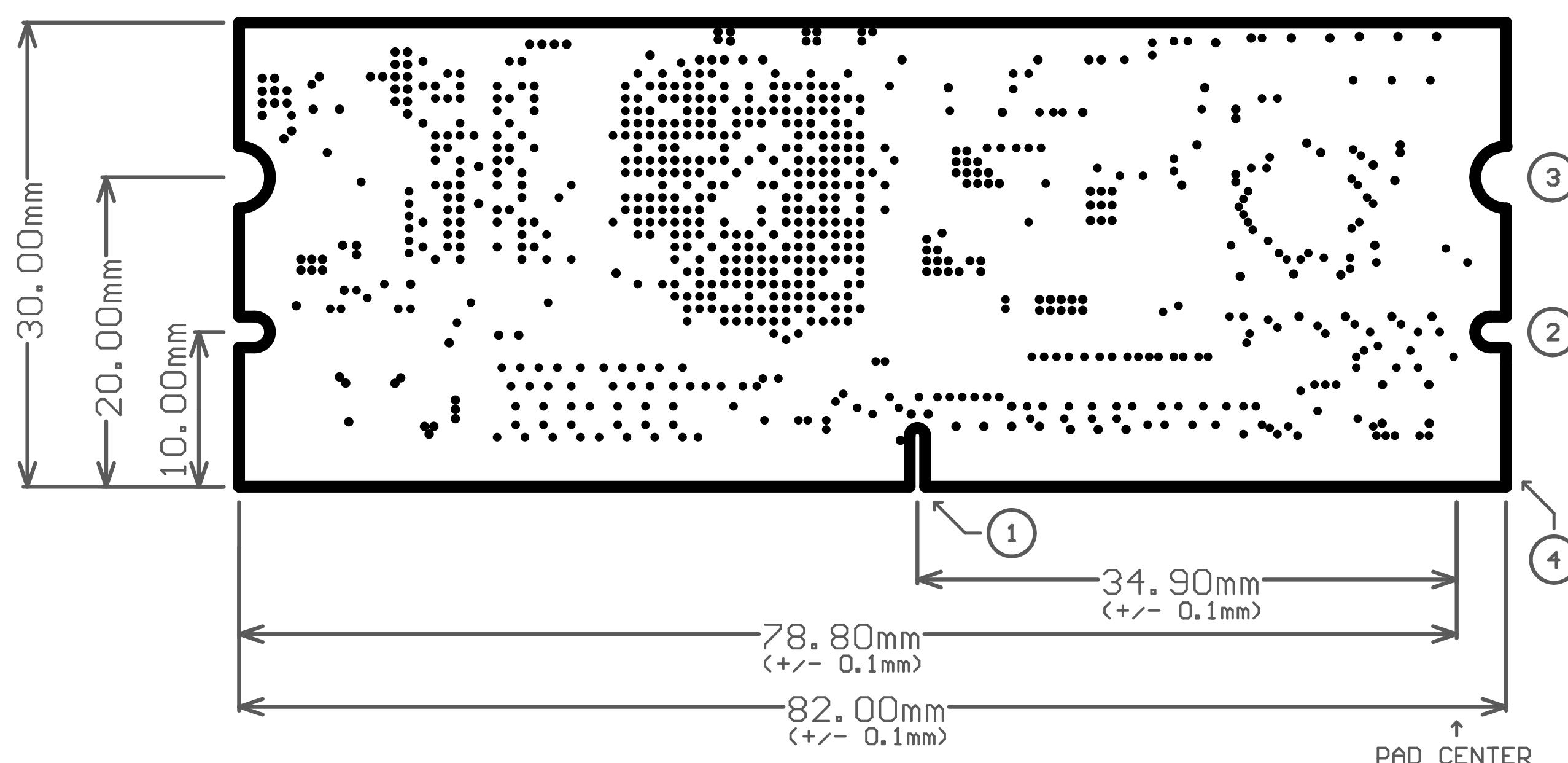
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Detail 1

Detail 2

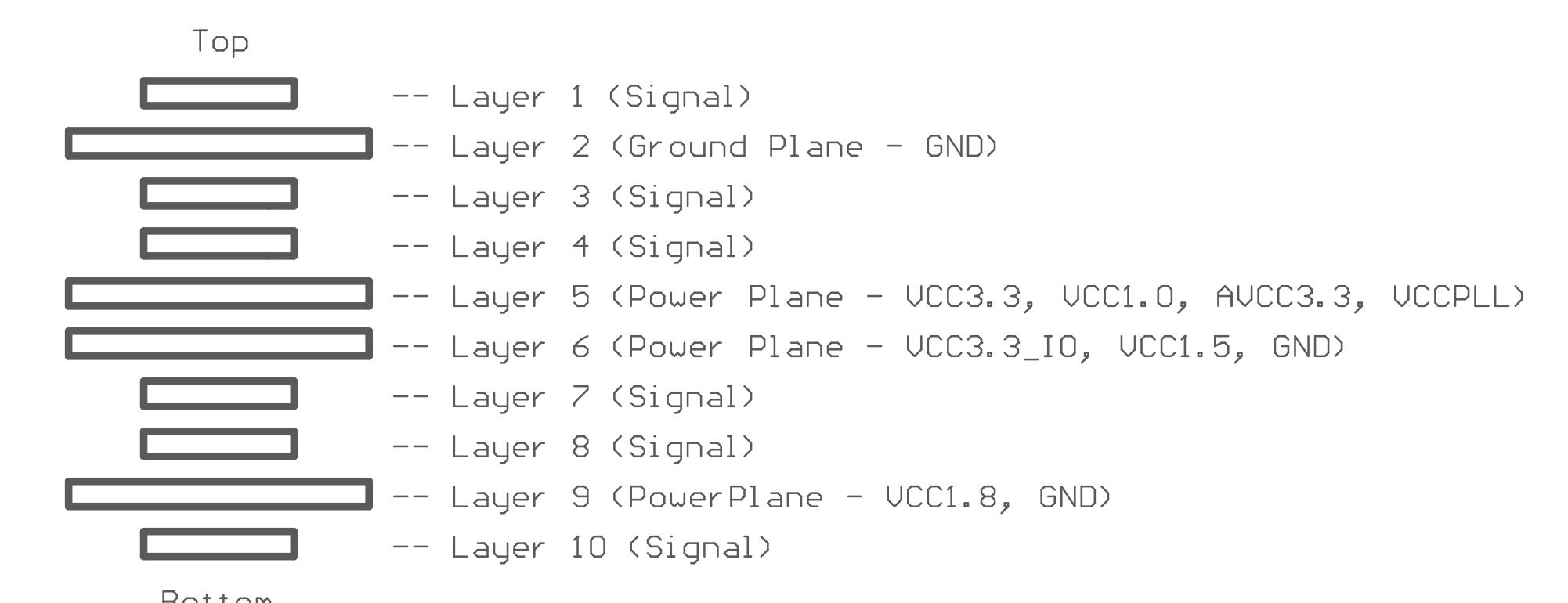
Detail 3

Detail 4
(PCB side view)**UW-IPMC MEZZANINE (revB)****Layer 2 - Ground Plane (Copper, Mask)****Specifications:**

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm +/- 0.10mm
3. Board dimensions are 82 by 30mm with tolerances of +/- 0.15mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

Internal layers (3, 4, 7, 8):	External Layers (1 and 10):
40 Ohm: 6 mil tracks in artwork	40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup

Univ. of Wisconsin—Madison
Madison, WI 53706

ENGINEER:
Vicente, M.

PCB DESIGNER:
Vicente, M.

DATE:
06JUN2019

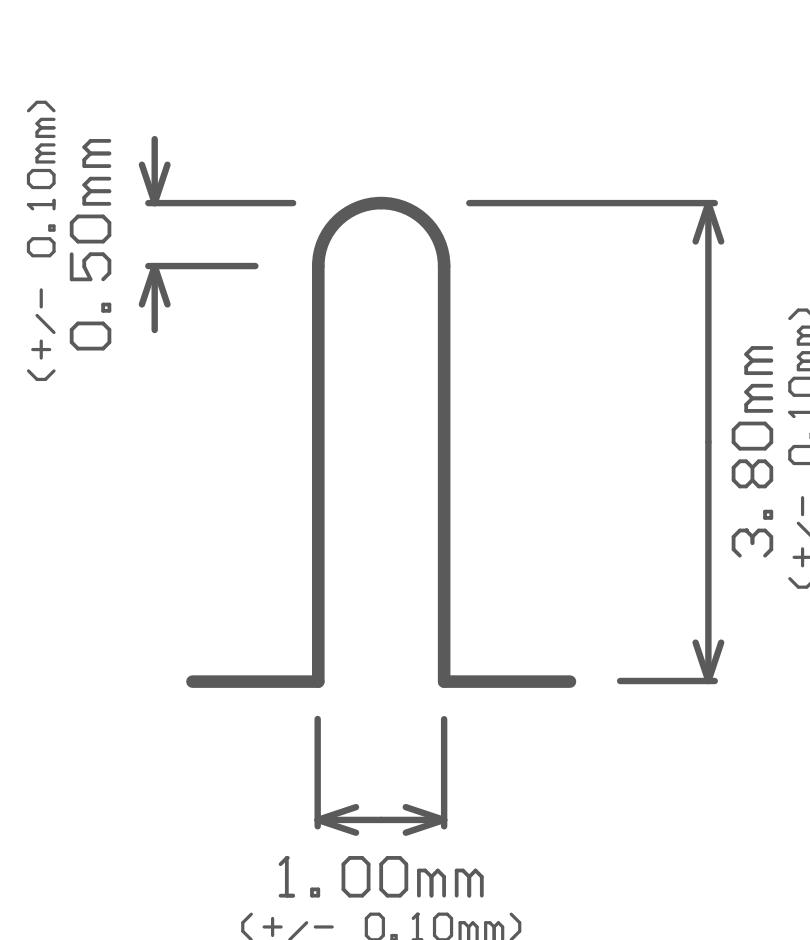
FILE NAME:
ZYNQ_IPMC.PCBDOC

TITLE:
ZYNQ-IPMC

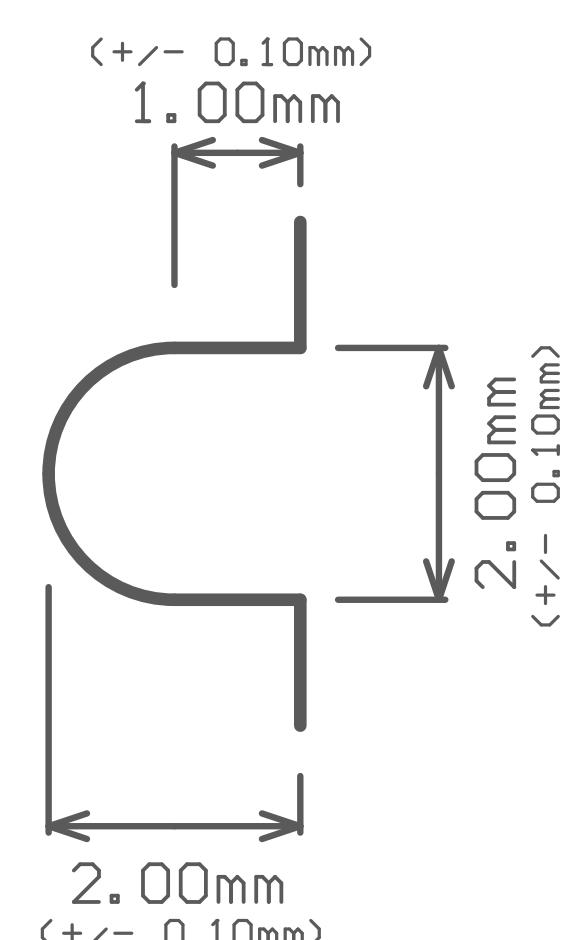
PART NO.:

REV:
revB1

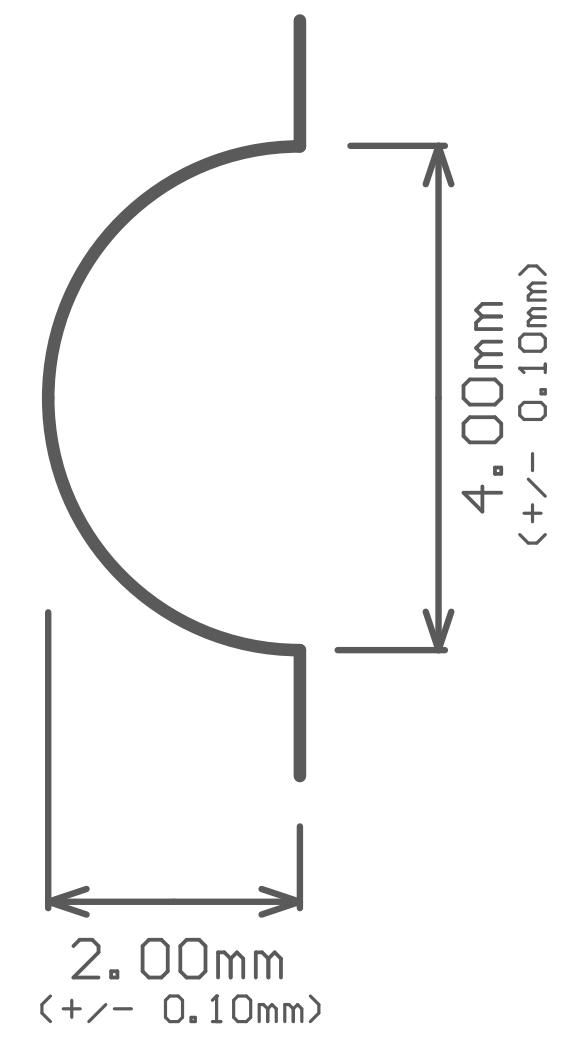
SCALE:
1:1



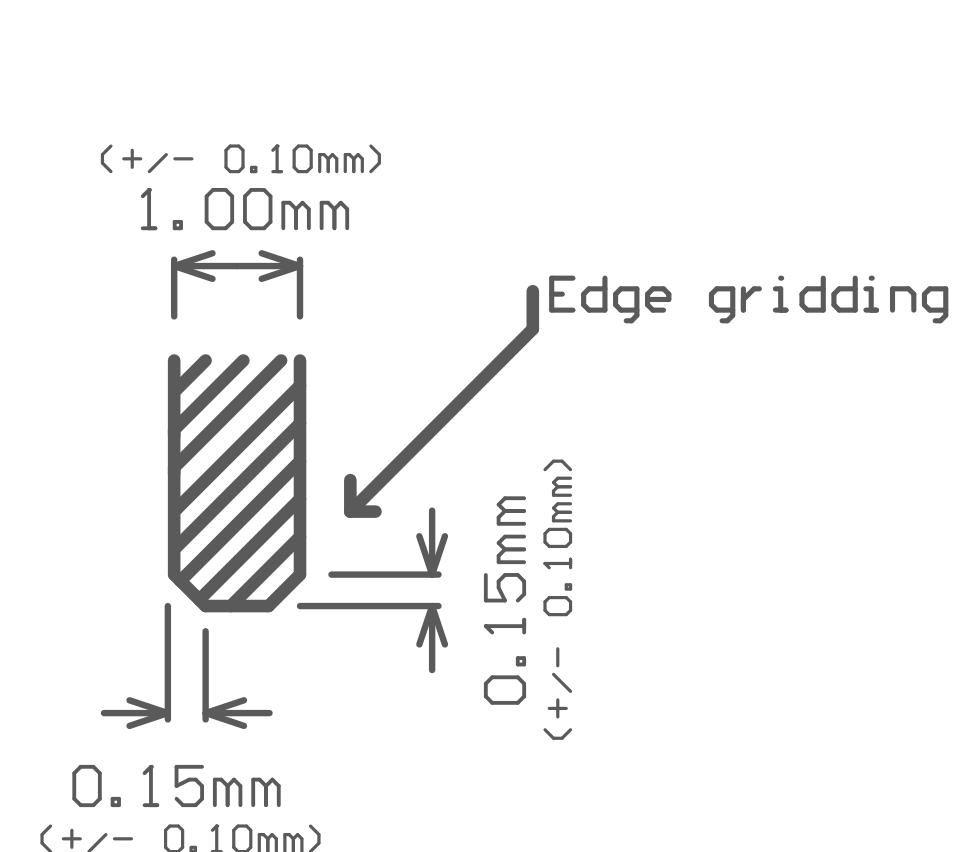
Detail 1



Detail 2



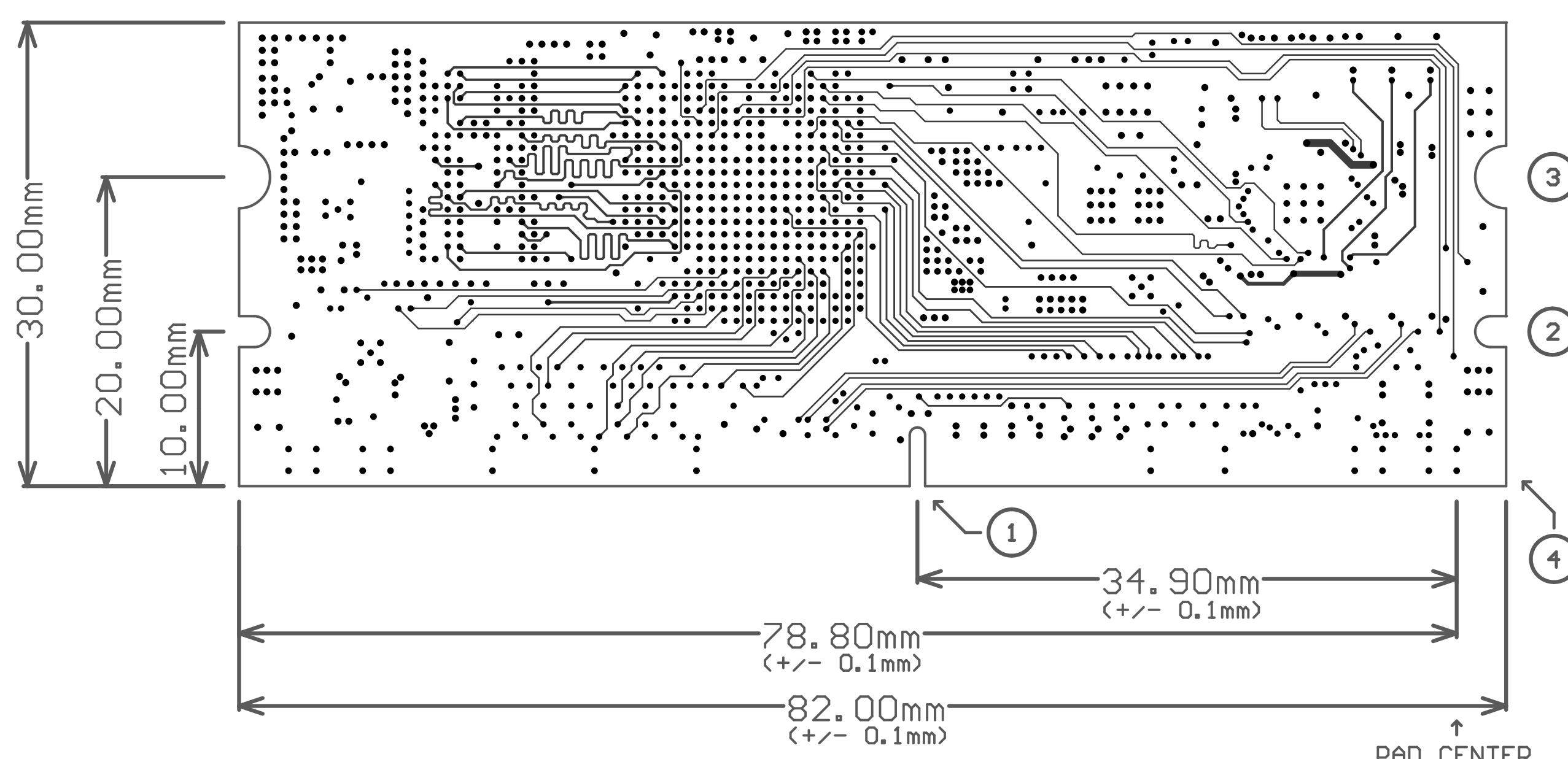
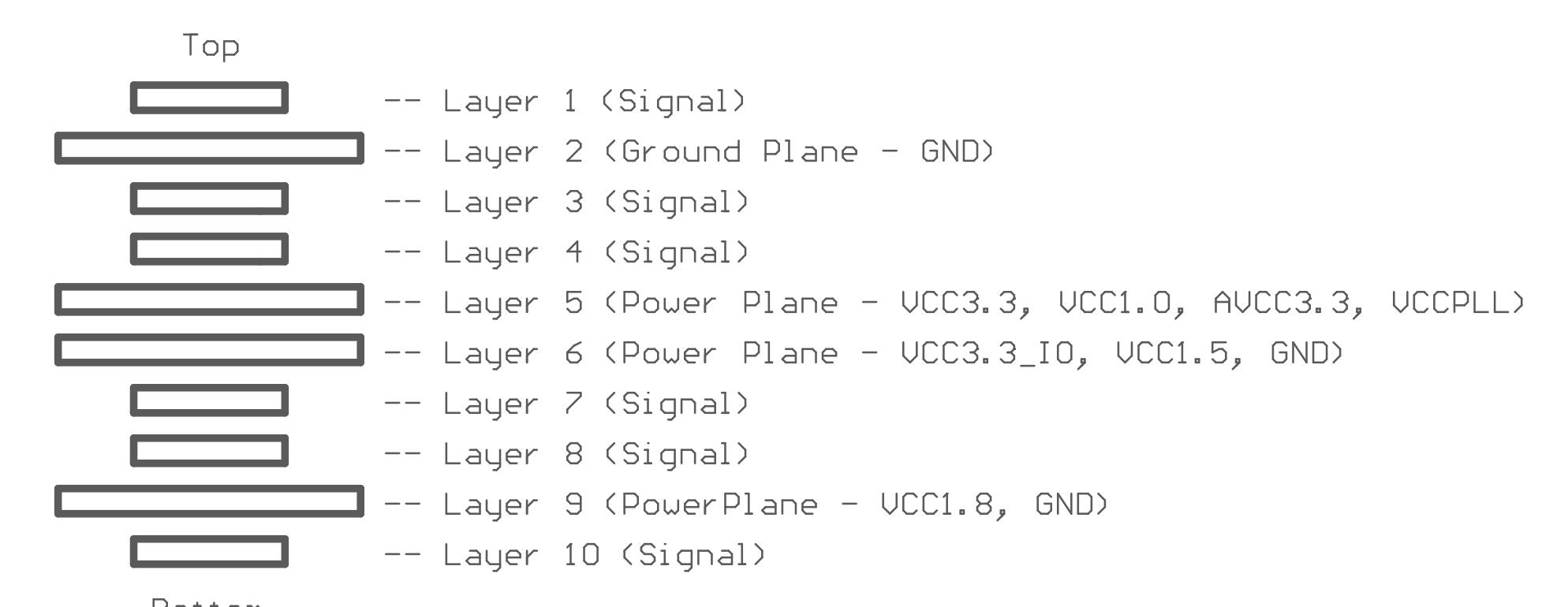
Detail 3

Detail 4
(PCB side view)**Specifications:**

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170$ C
2. Overall thickness is 1.0mm ± 0.10 mm
3. Board dimensions are 82 by 30mm with tolerances of ± 0.15 mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

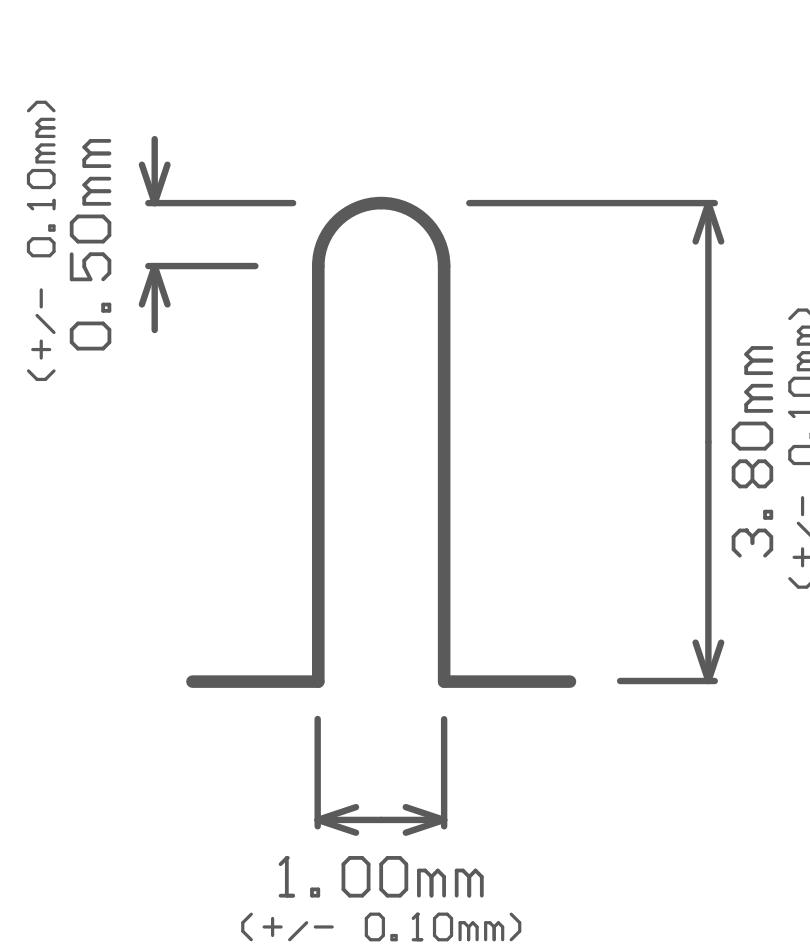
Internal layers (3, 4, 7, 8):	External Layers (1 and 10):
40 Ohm: 6 mil tracks in artwork	40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating ± 3 mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

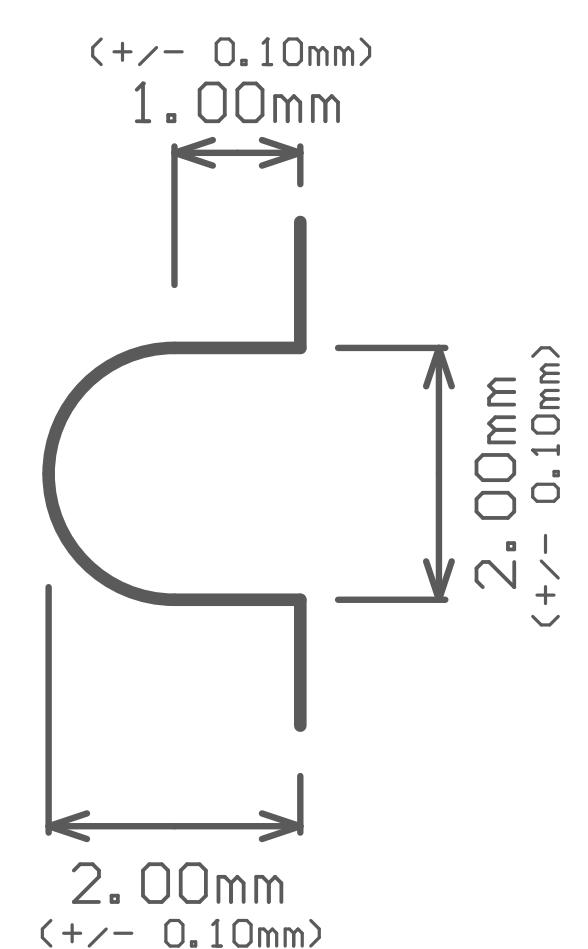
UW-IPMC MEZZANINE (revB)**Layer 3 - Signal (Copper)****Layer Stackup**Univ. of Wisconsin—Madison
Madison, WI 53706ENGINEER:
Vicente, M.PCB DESIGNER:
Vicente, M.DATE:
06JUN2019FILE NAME:
ZYNQ_IPMC.PCBDOCTITLE:
ZYNQ-IPMC

PART NO.:

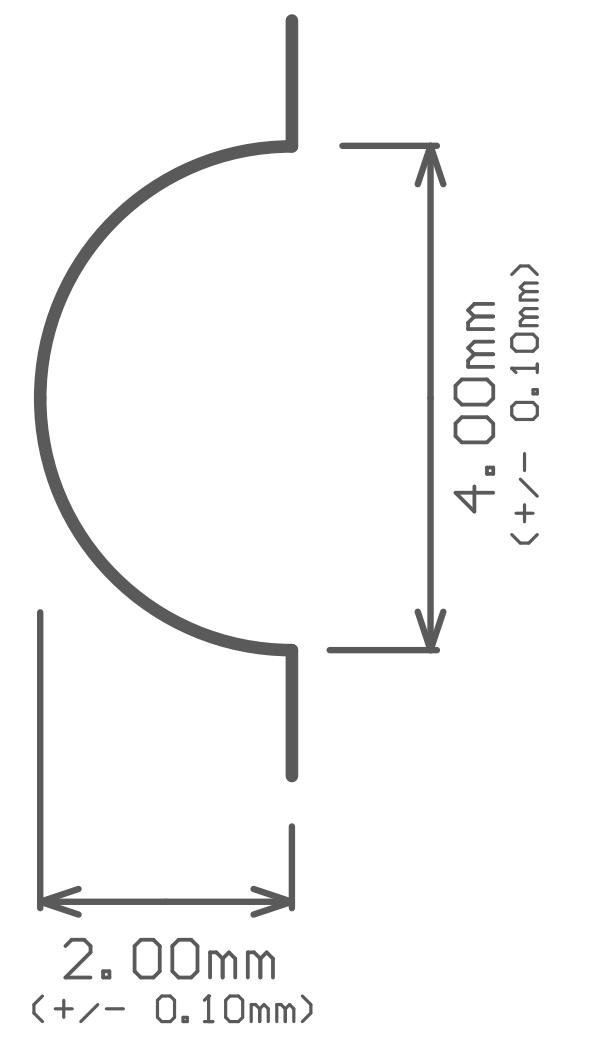
REV:
revB1SCALE:
1:1



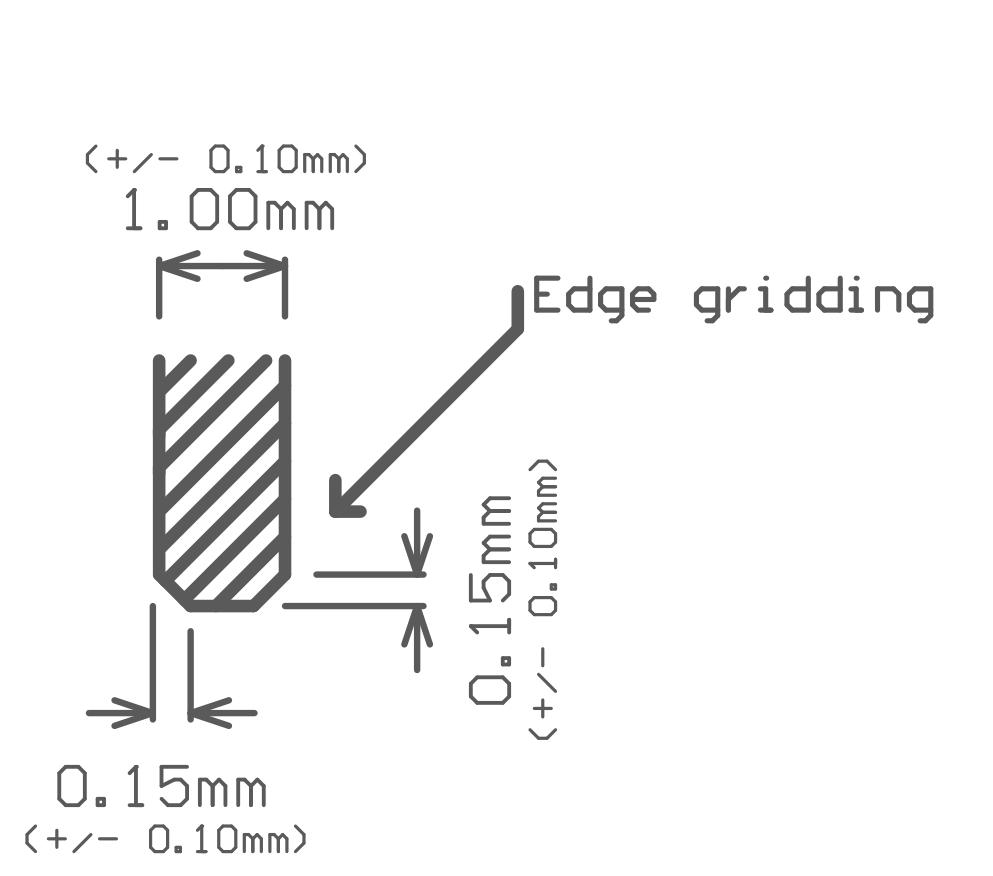
Detail 1



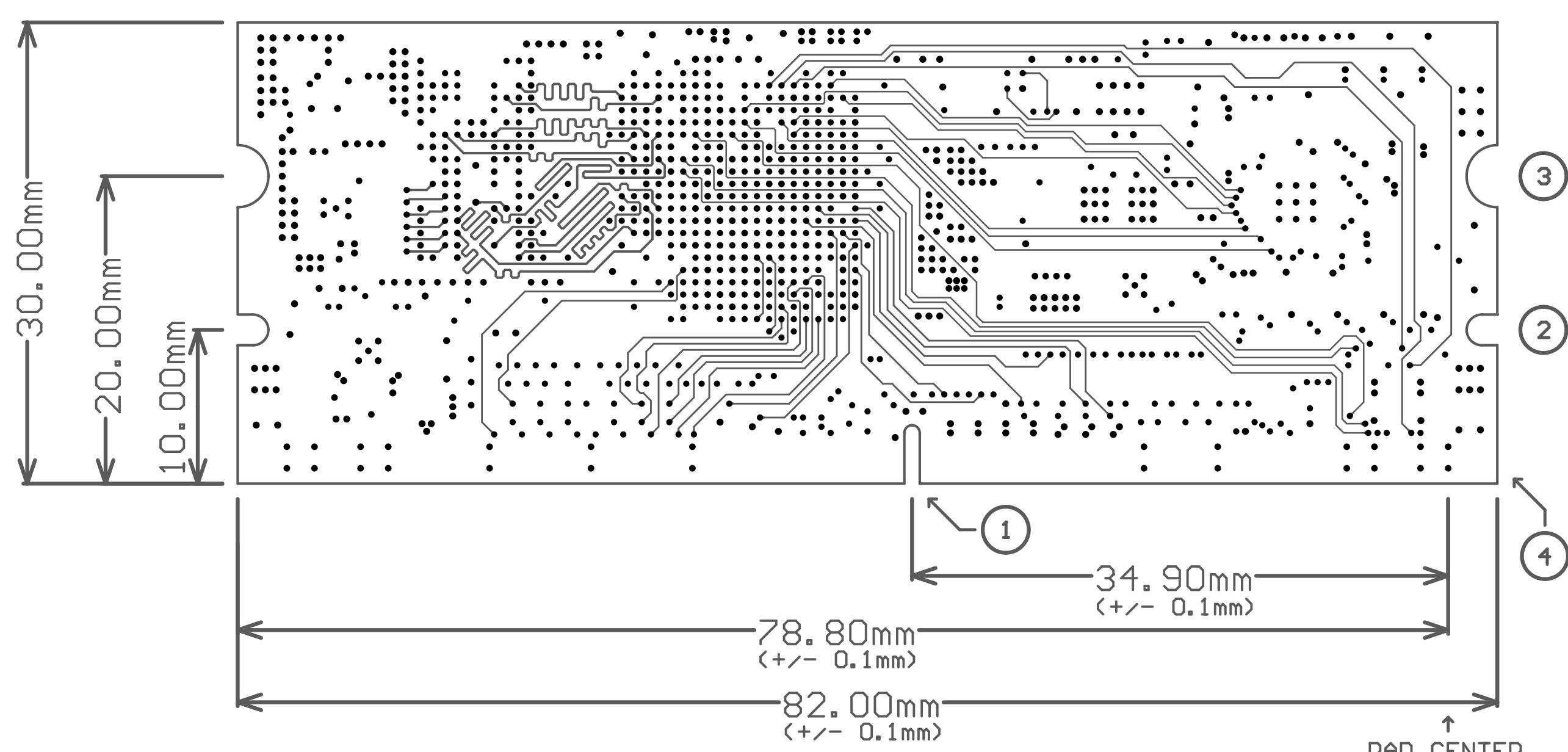
Detail 2



Detail 3

Detail 4
(PCB side view)**UW-IPMC MEZZANINE (revB)**

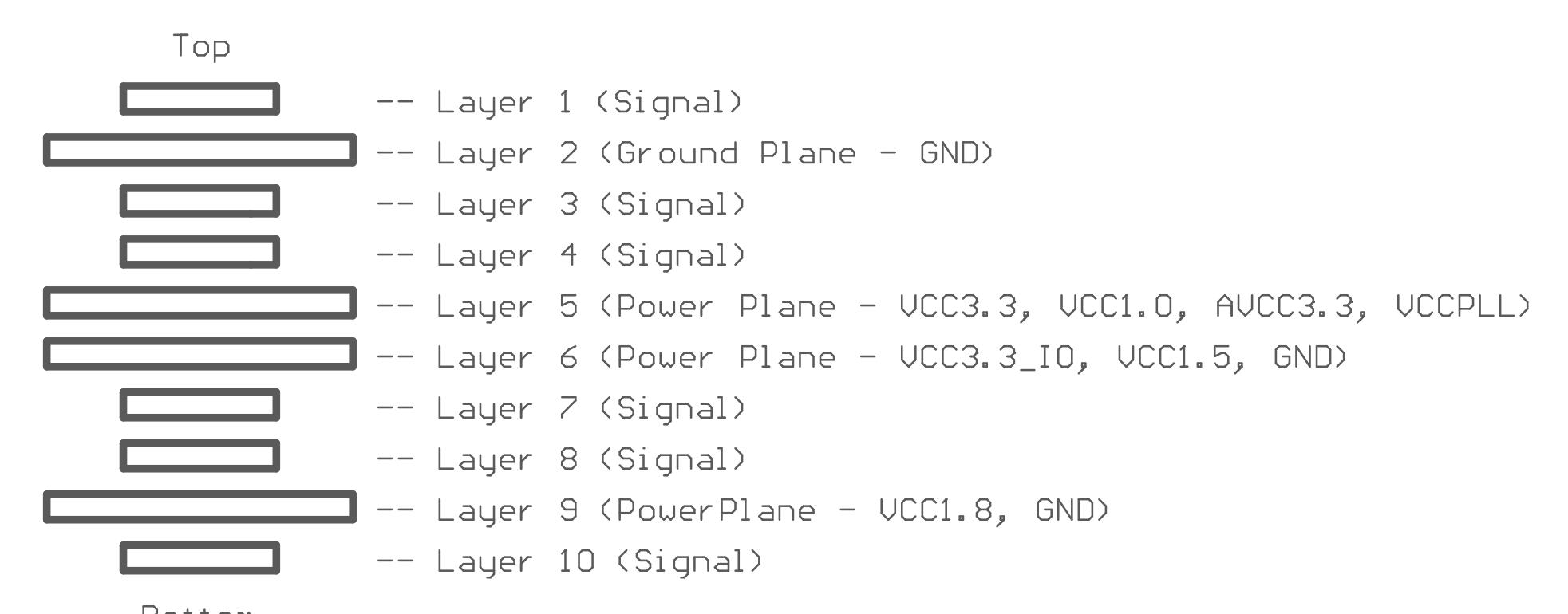
Layer 4 - Signal (Copper)

**Specifications:**

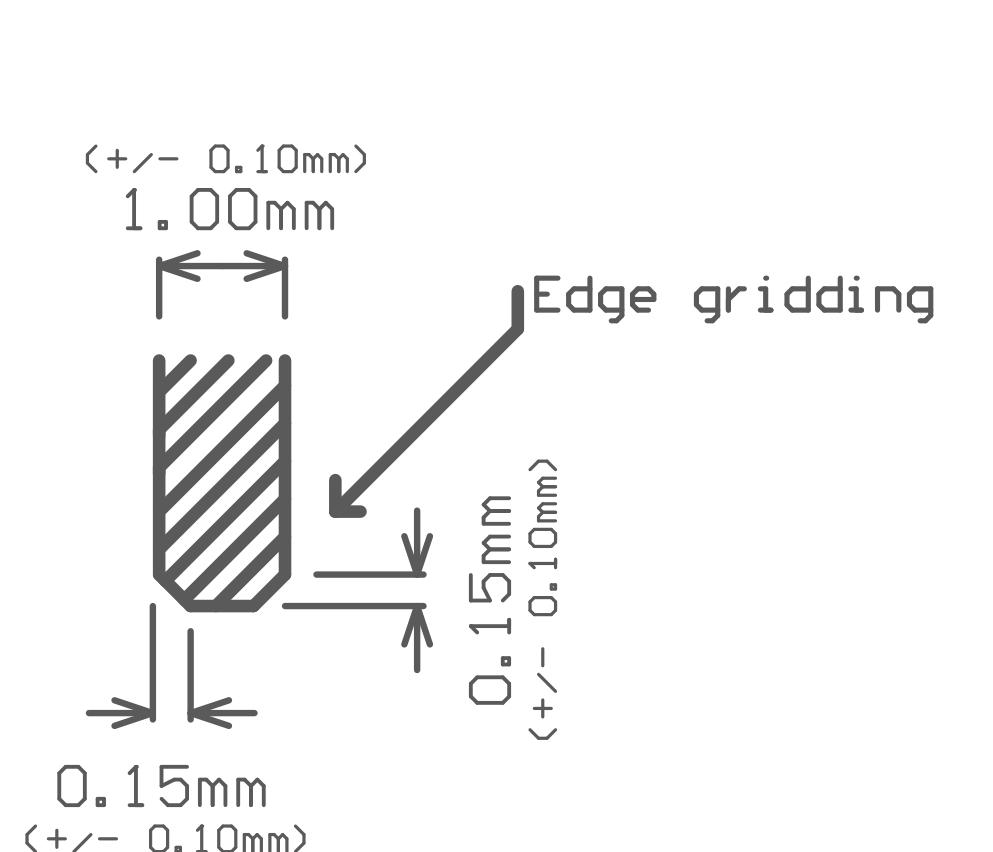
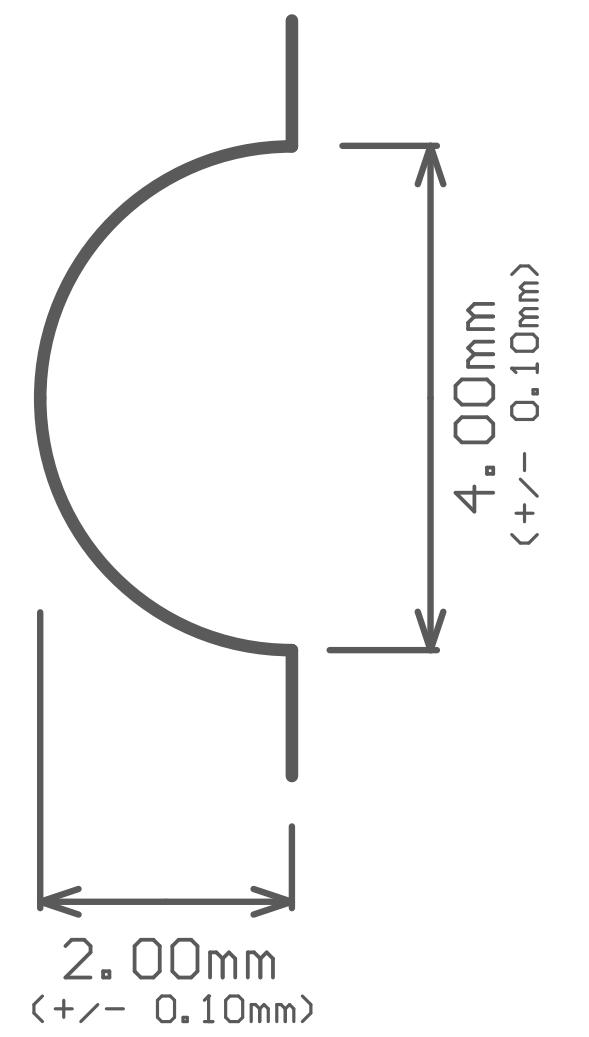
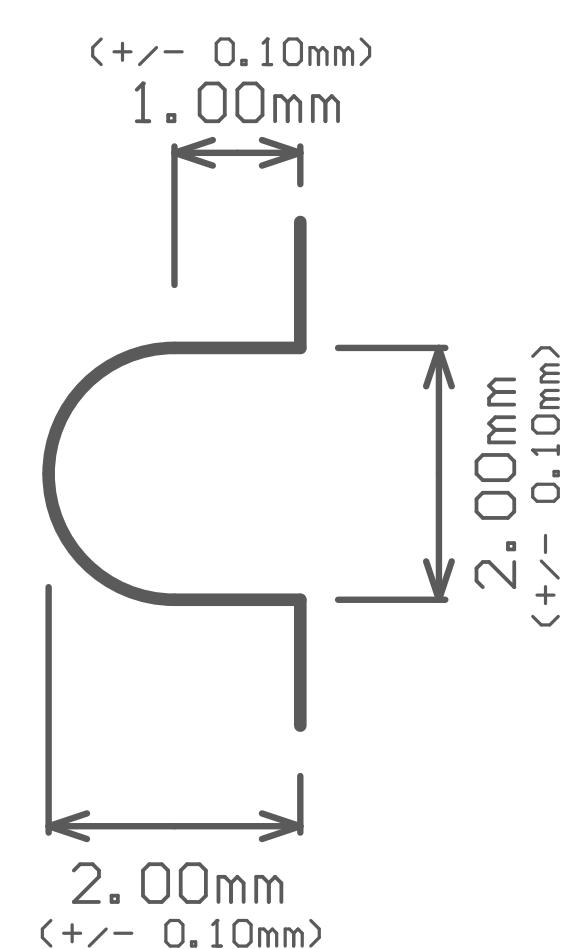
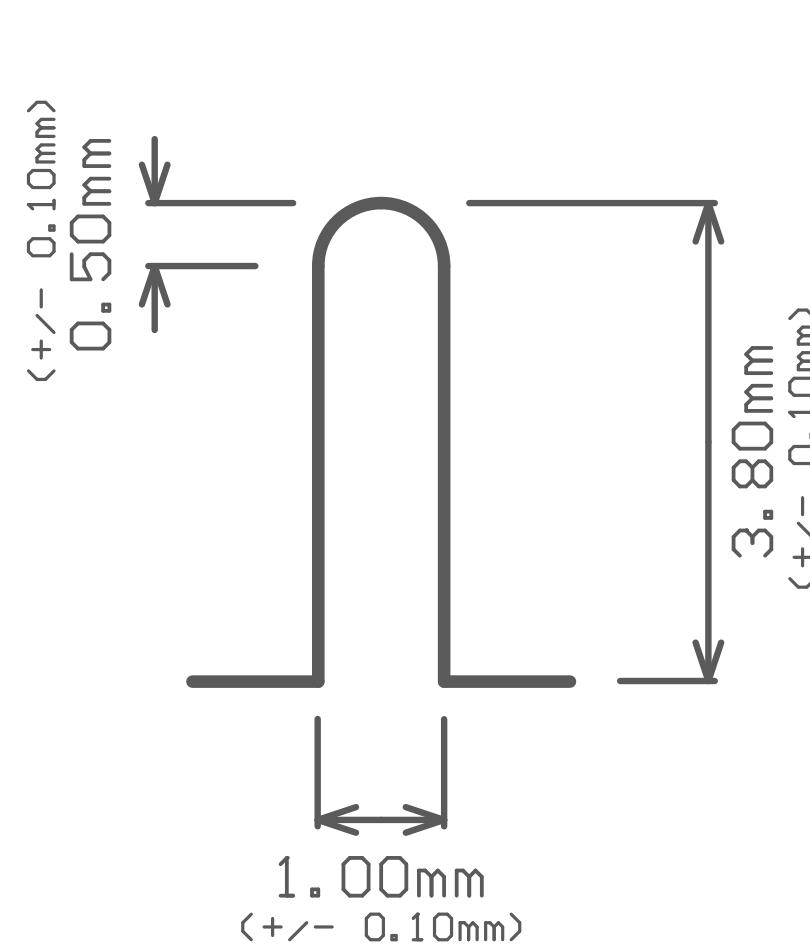
1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170$ C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Board dimensions are 82 by 30mm with tolerances of +/- 0.15mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

Internal layers (3, 4, 7, 8):	External Layers (1 and 10):
40 Ohm: 6 mil tracks in artwork	40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup

Univ. of Wisconsin—Madison Madison, WI 53706	ENGINEER: Vicente, M. PCB DESIGNER: Vicente, M.	TITLE: ZYNQ-IPMC
	DATE: 06JUN2019	PART NO.: REV: revB1
	FILE NAME: ZYNQ_IPMC.PCBDOC	DWG NO.: SCALE: 1:1



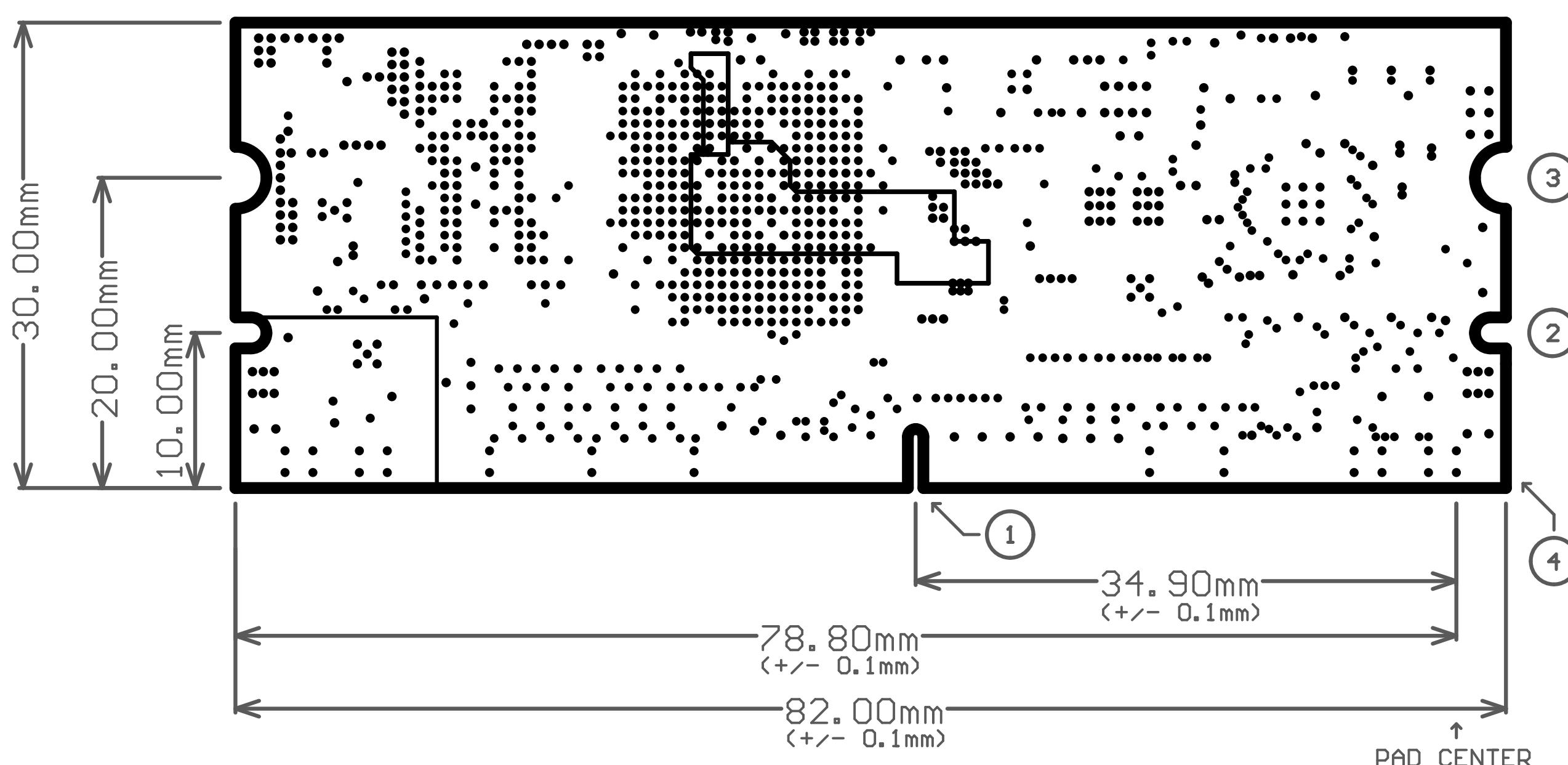
Detail 1

Detail 2

Detail 3

Detail 4
(PCB side view)**UW-IPMC MEZZANINE (revB)**

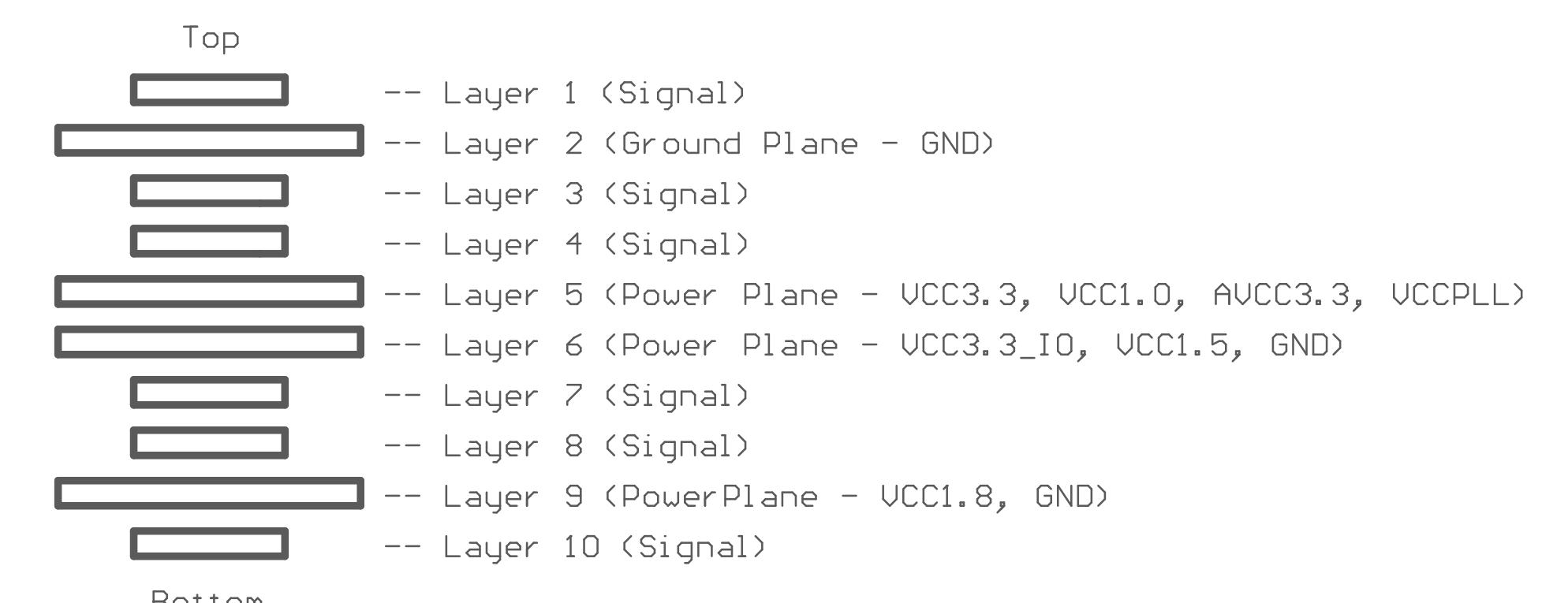
Layer 5 – Power Plane (Copper, Mask)

**Specifications:**

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170$ C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Board dimensions are 82 by 30mm with tolerances of +/- 0.15mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

Internal layers (3, 4, 7, 8):	External Layers (1 and 10):
40 Ohm: 6 mil tracks in artwork	40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork	50 Ohm: 6.5 mil tracks in artwork

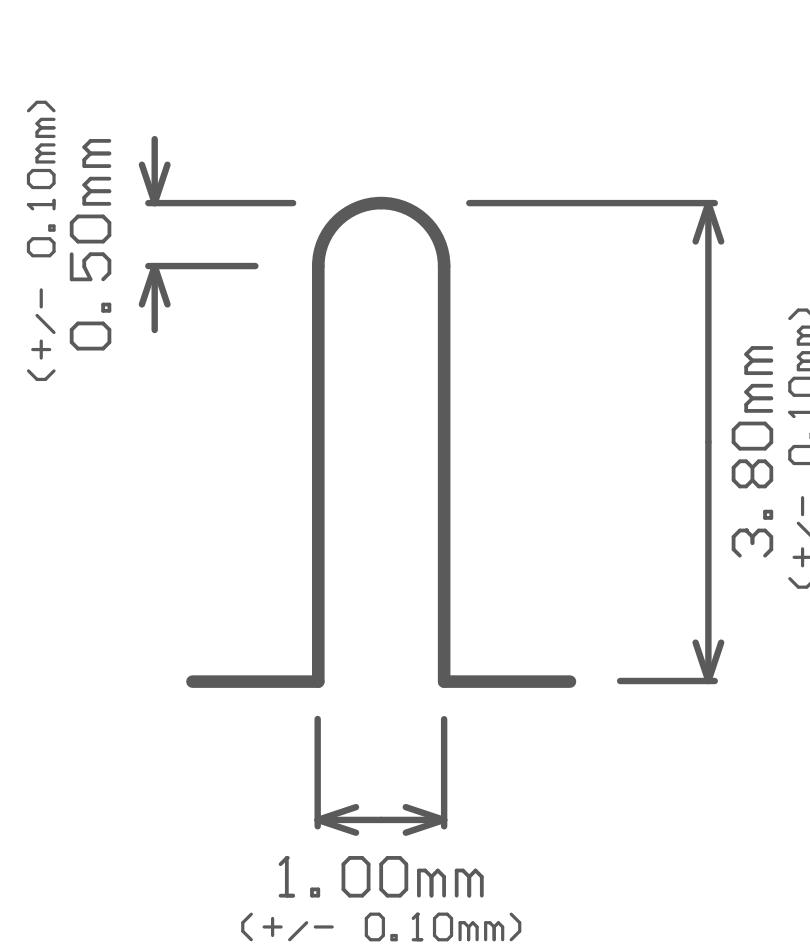
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer StackupUniv. of Wisconsin–Madison
Madison, WI 53706ENGINEER:
Vicente, M.TITLE:
ZYNQ-IPMCPCB DESIGNER:
Vicente, M.

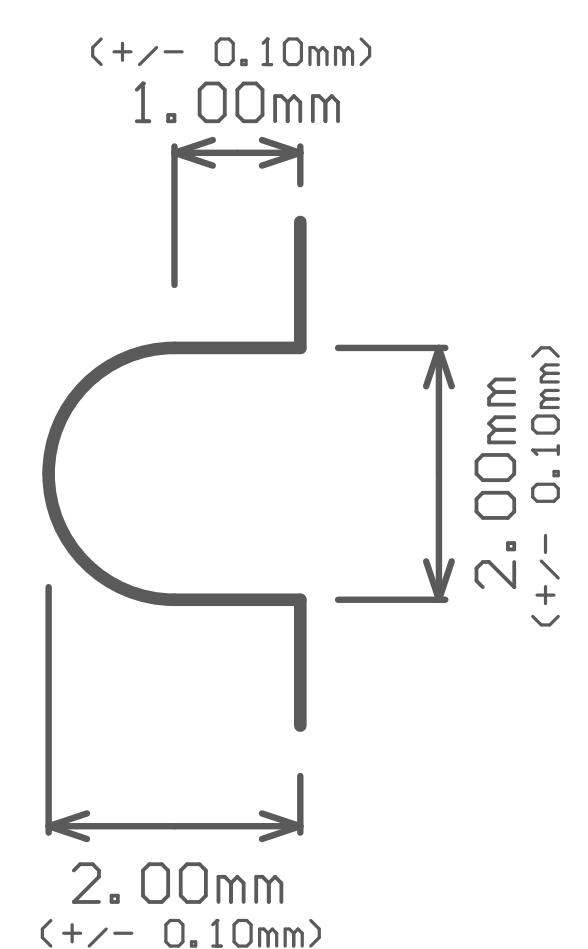
PART NO.:

REV:
revB1DATE:
06JUN2019SCALE:
1:1FILE NAME:
ZYNQ_IPMC.PCBDOC

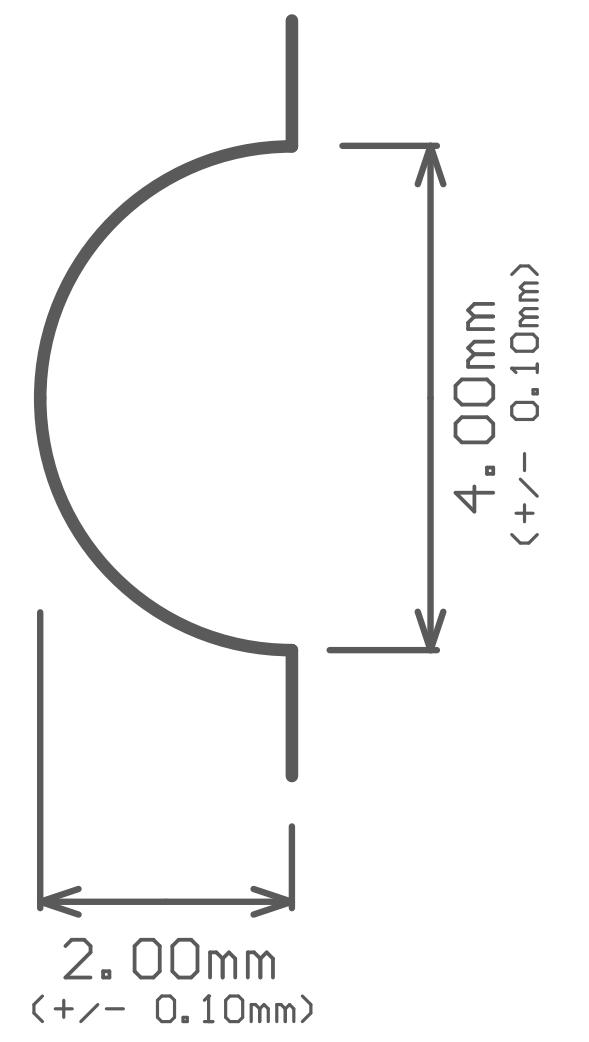
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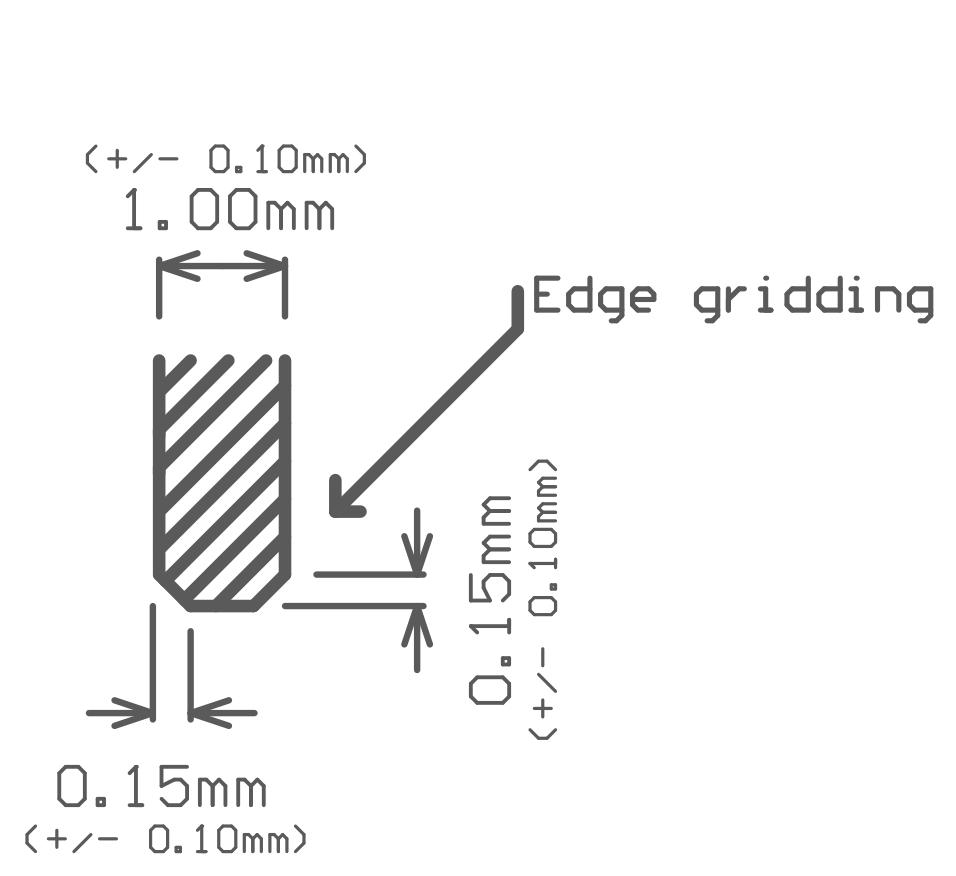
Detail 1



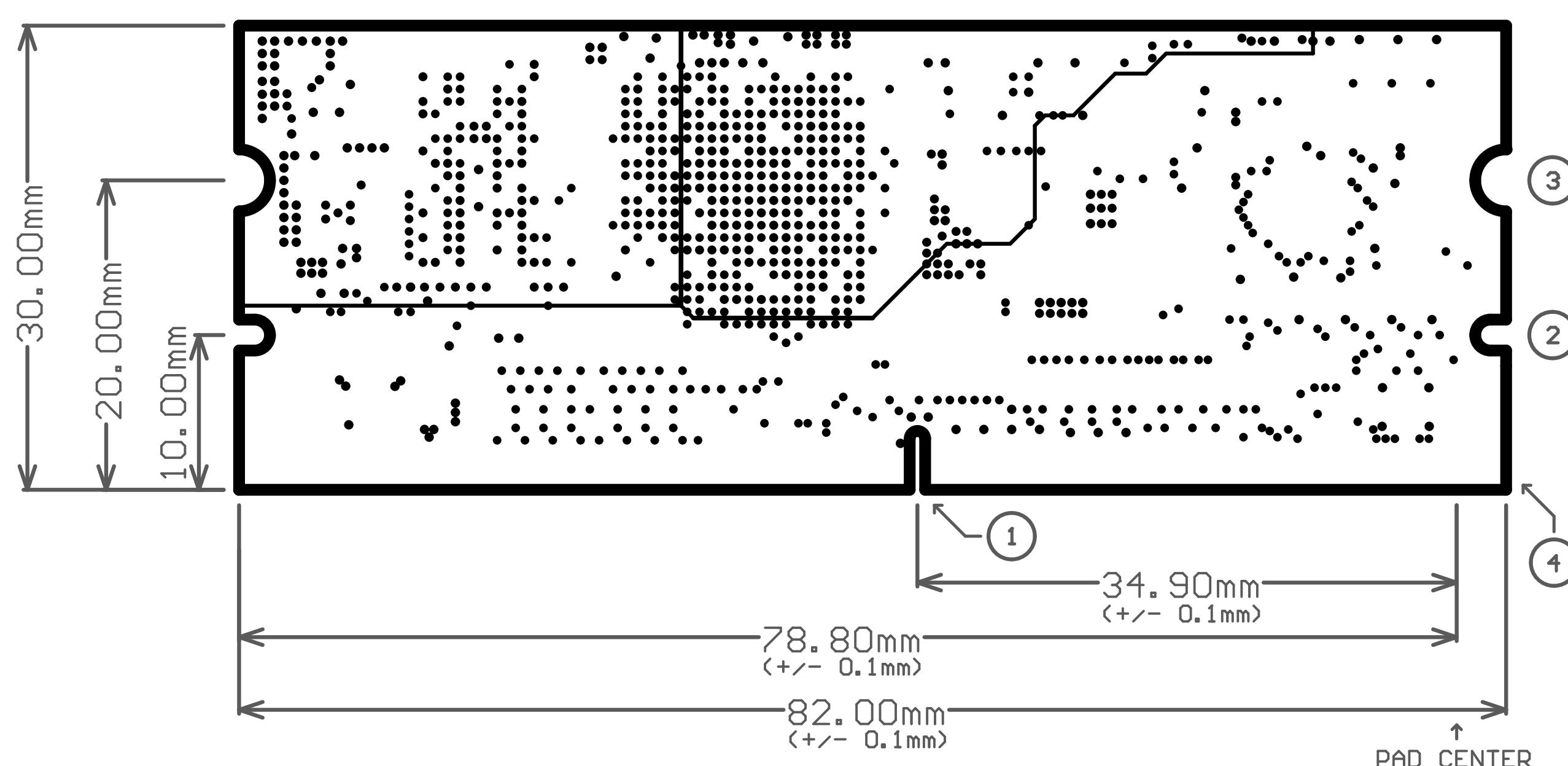
Detail 2



Detail 3

Detail 4
(PCB side view)**UW-IPMC MEZZANINE (revB)**

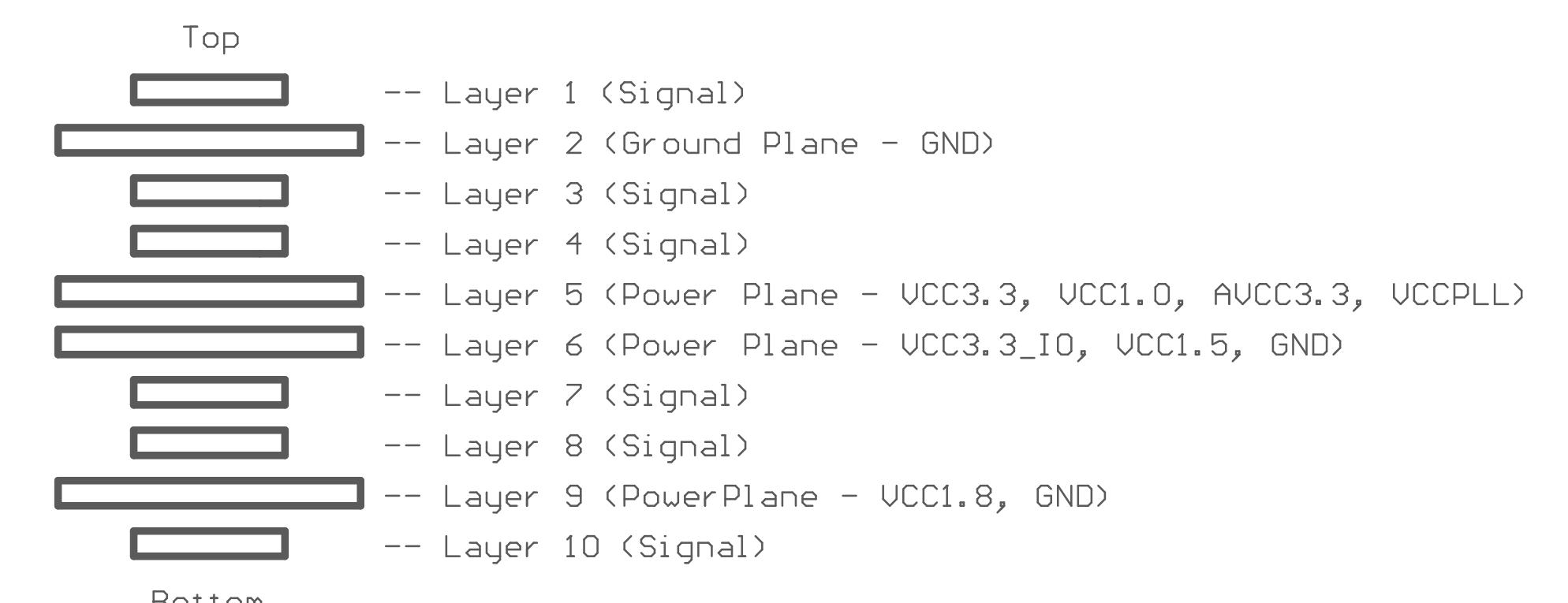
Layer 6 - Power Plane (Copper, Mask)

**Specifications:**

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

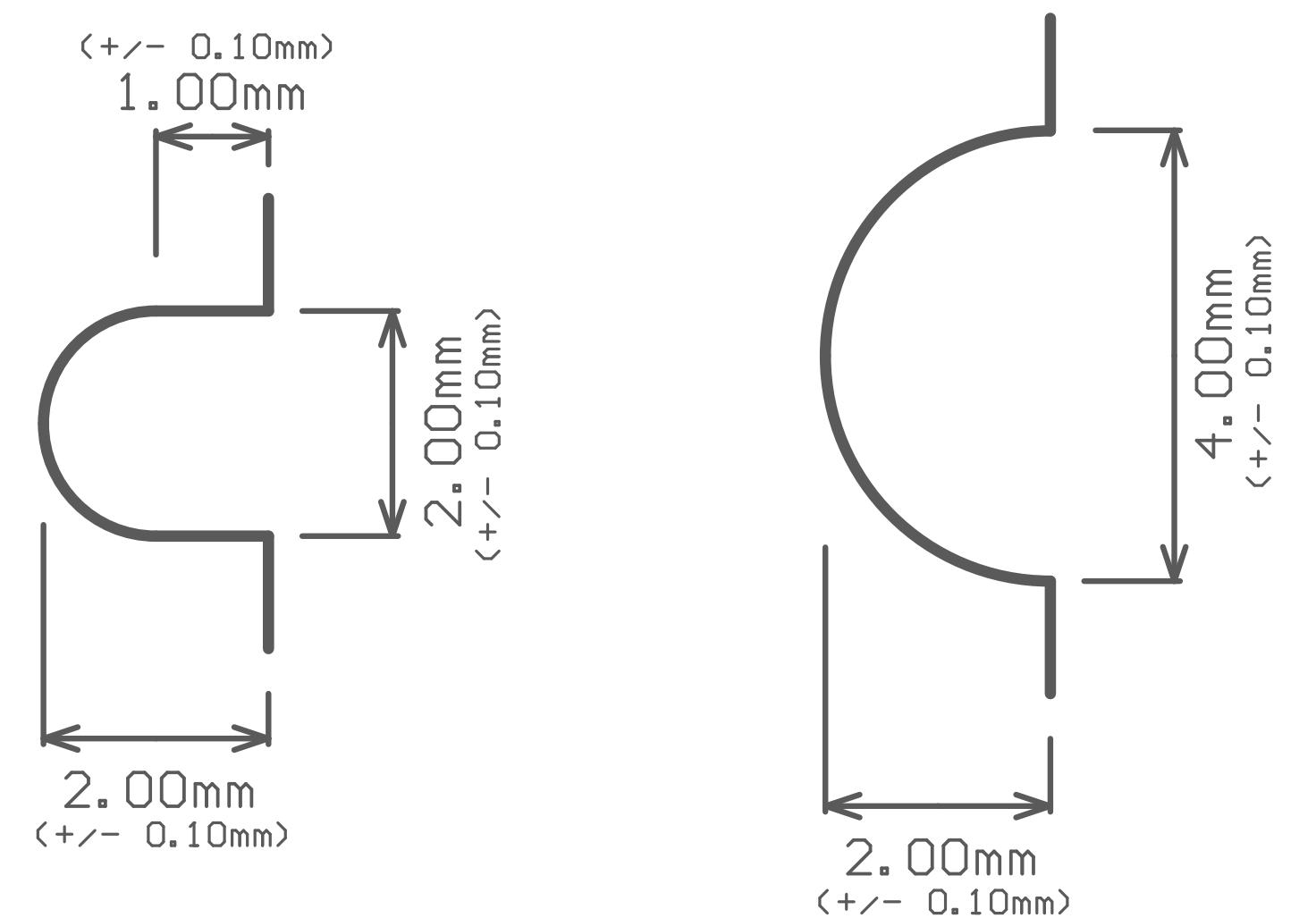
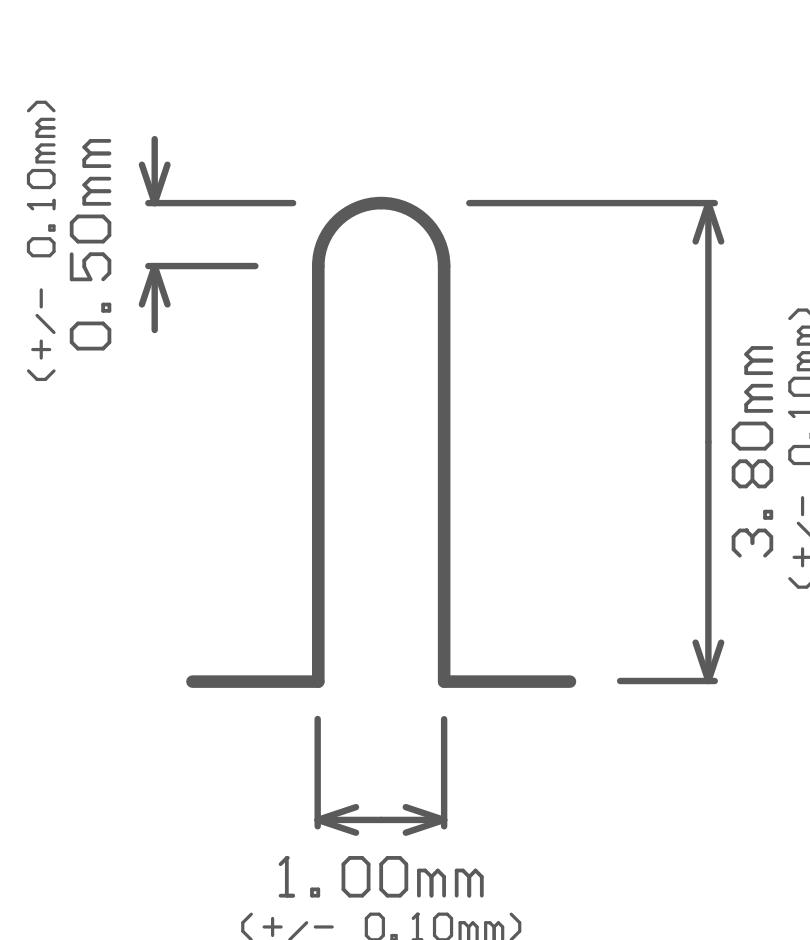
Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork 50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork 50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

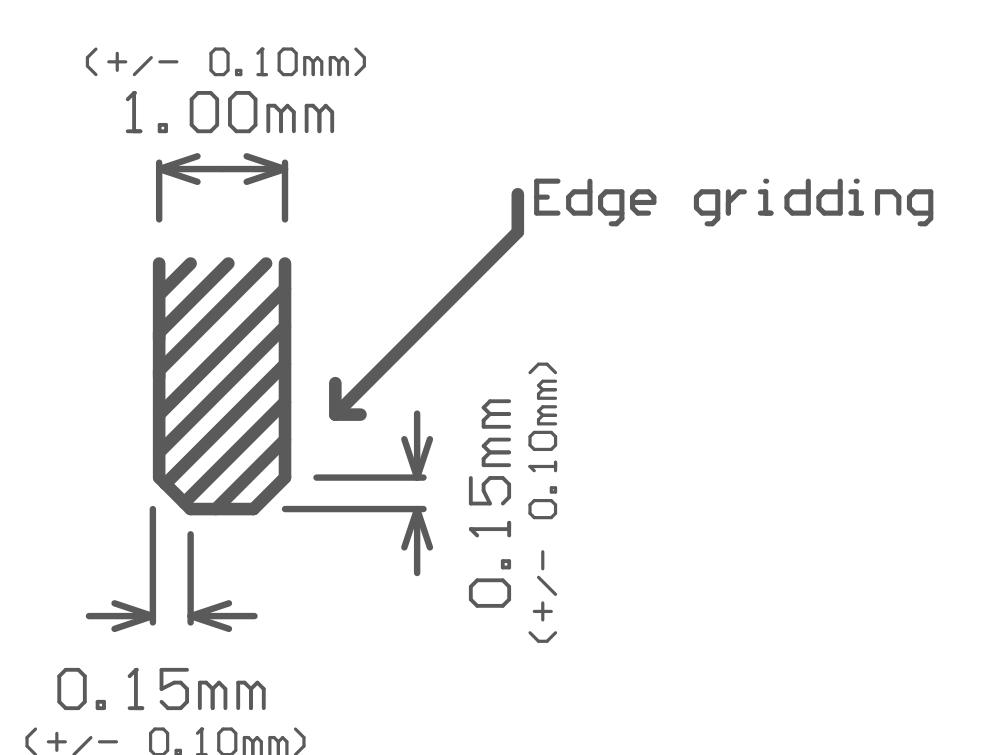
Layer StackupUniv. of Wisconsin-Madison
Madison, WI 53706ENGINEER:
Vicente, M.PCB DESIGNER:
Vicente, M.DATE:
06JUN2019FILE NAME:
ZYNQ_IPMC.PCBDOCTITLE:
ZYNQ-IPMC

PART NO.:

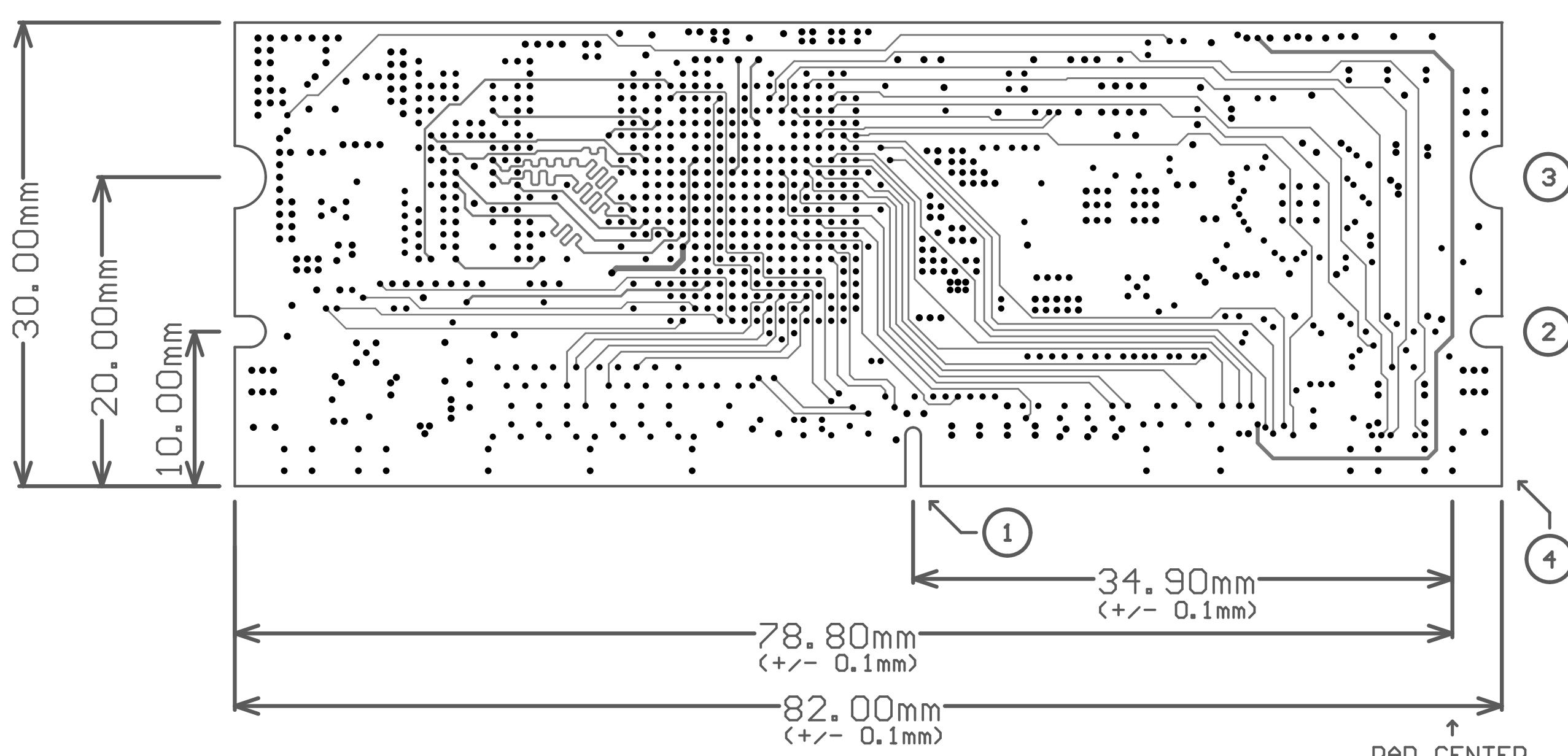
REV:
revB1SCALE:
1:1



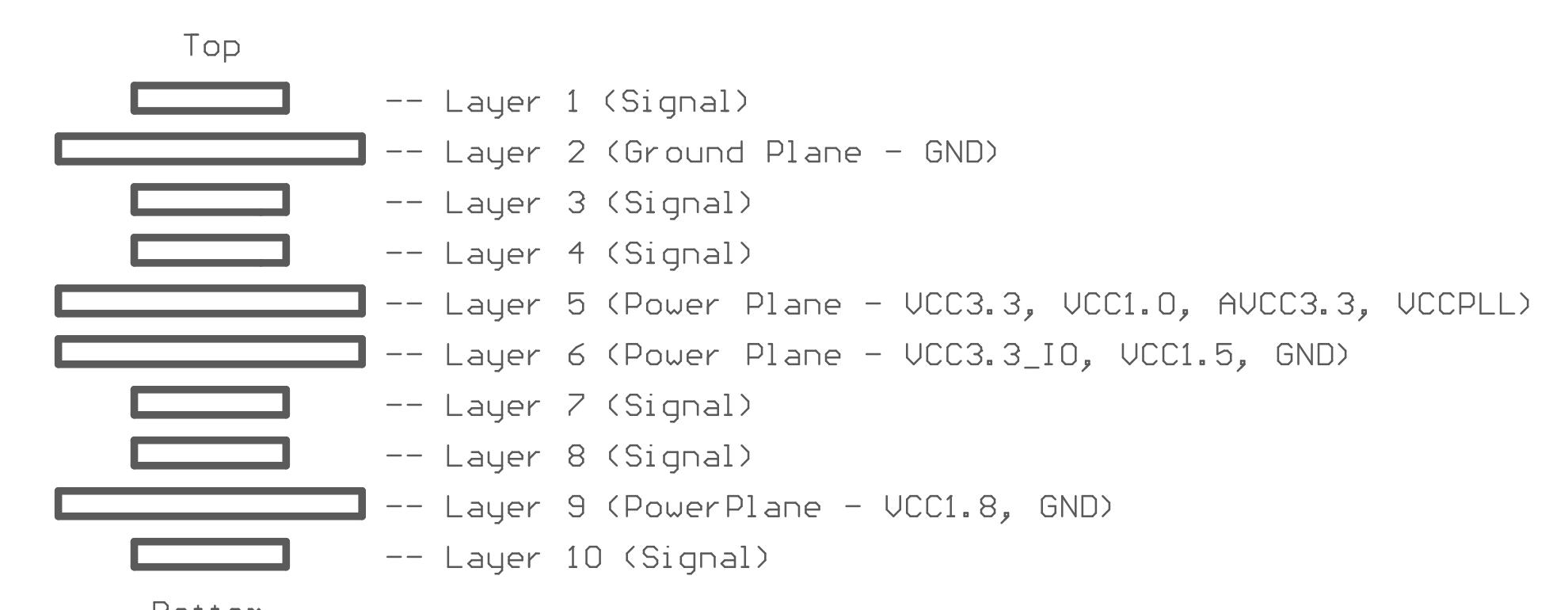
Detail 3

Detail 4
(PCB side view)**UW-IPMC MEZZANINE (revB)**

Layer 7 - Signal (Copper)

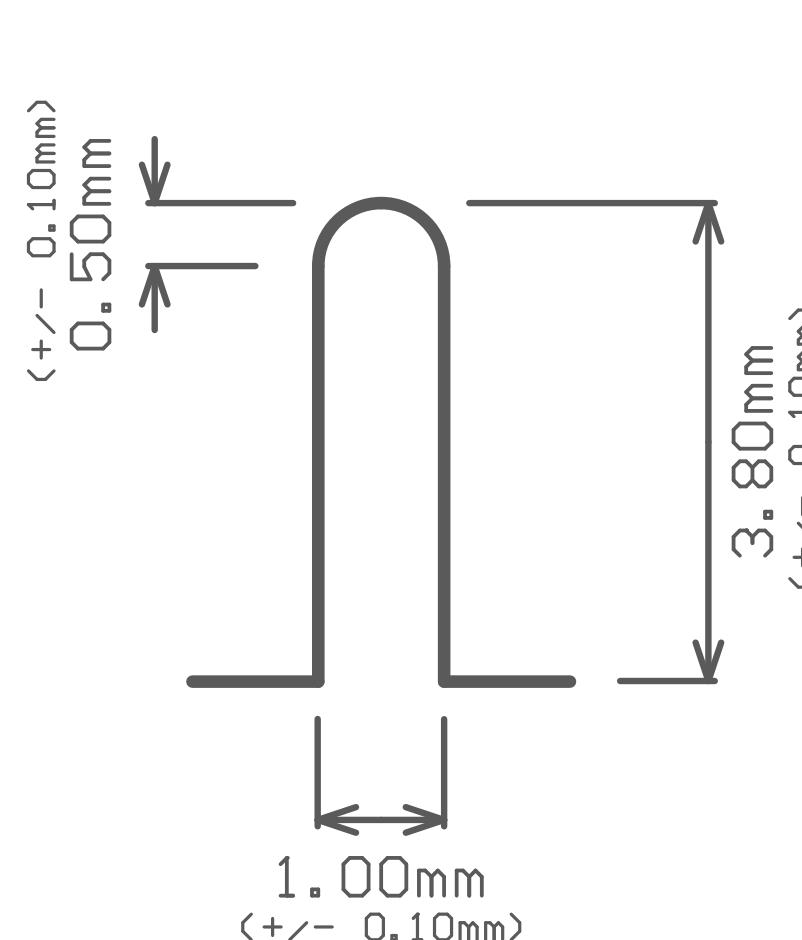
**Specifications:**

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170$ C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Board dimensions are 82 by 30mm with tolerances of +/- 0.15mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork
Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

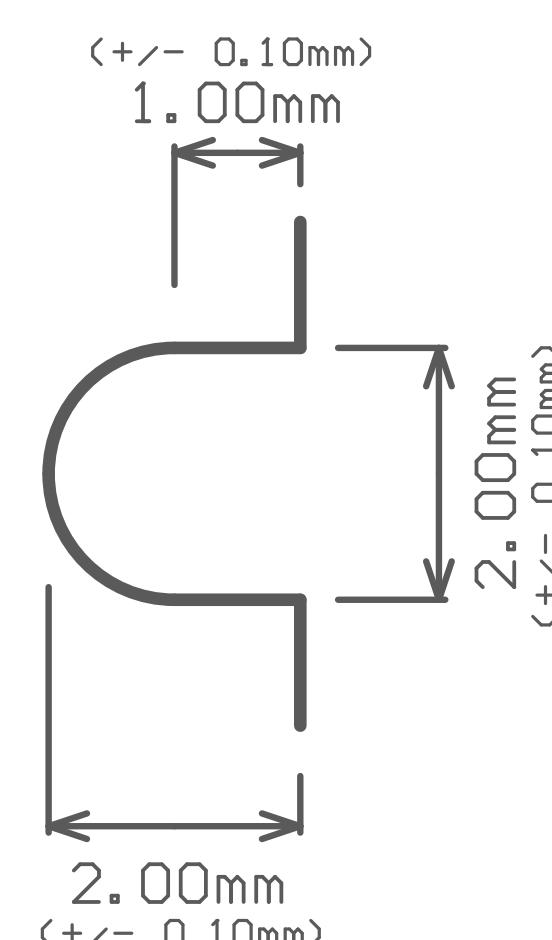
Layer StackupUniv. of Wisconsin-Madison
Madison, WI 53706ENGINEER:
Vicente, M.PCB DESIGNER:
Vicente, M.DATE:
06JUN2019FILE NAME:
ZYNQ_IPMC.PCBDOCTITLE:
ZYNQ-IPMC

PART NO.:

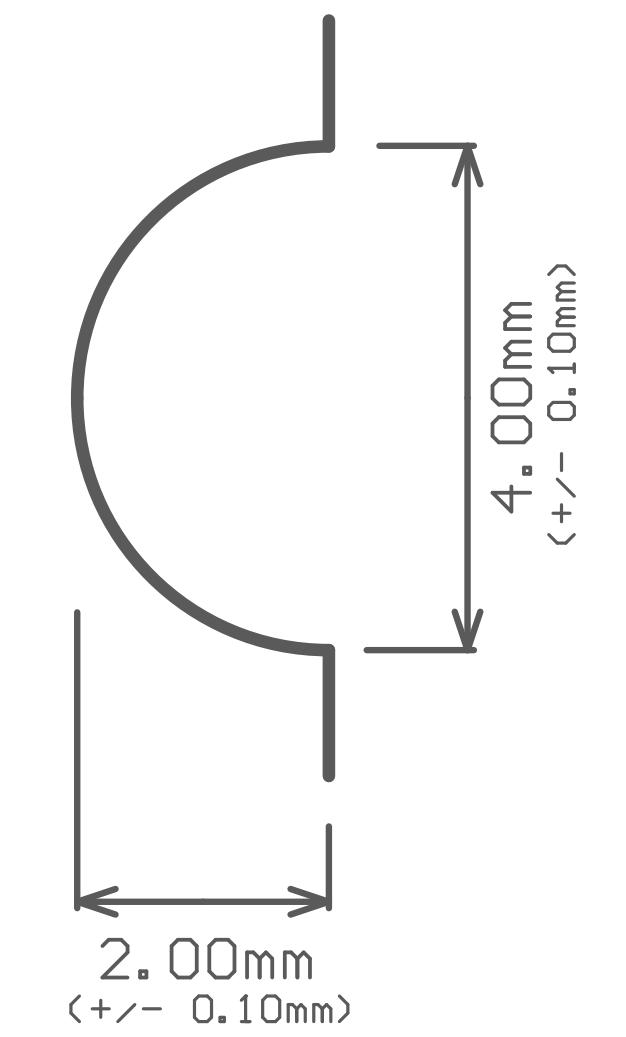
REV:
revB1SCALE:
1:1



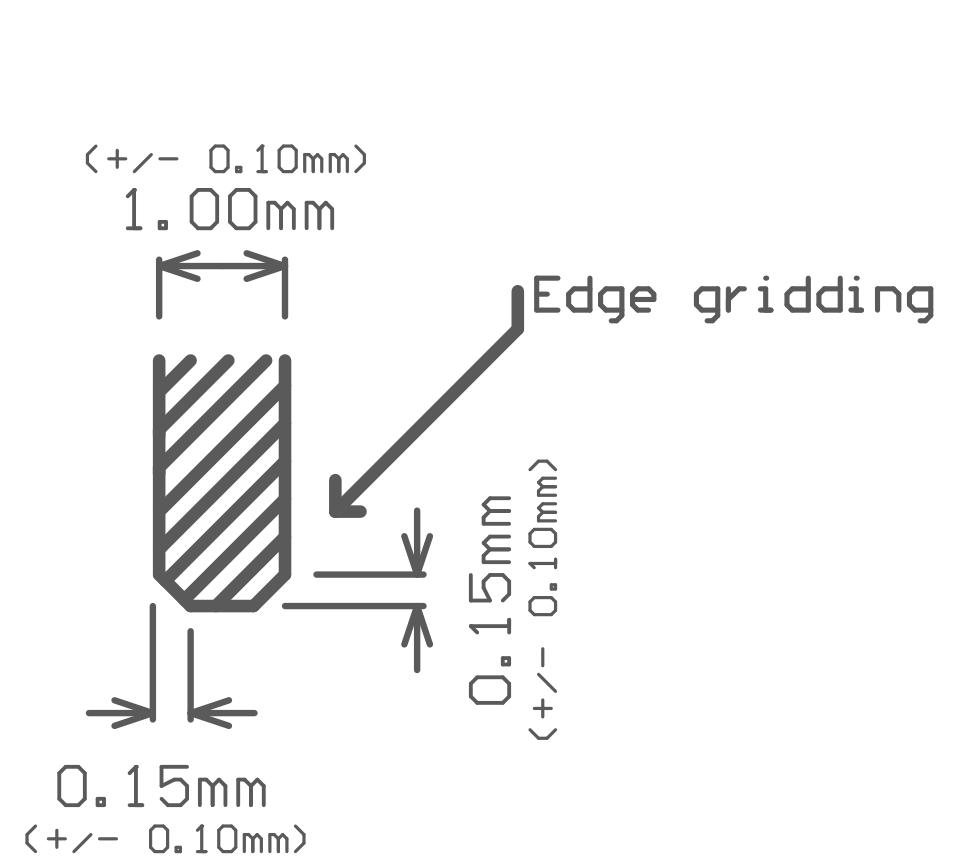
Detail 1



Detail 2



Detail 3

Detail 4
(PCB side view)**Specifications:**

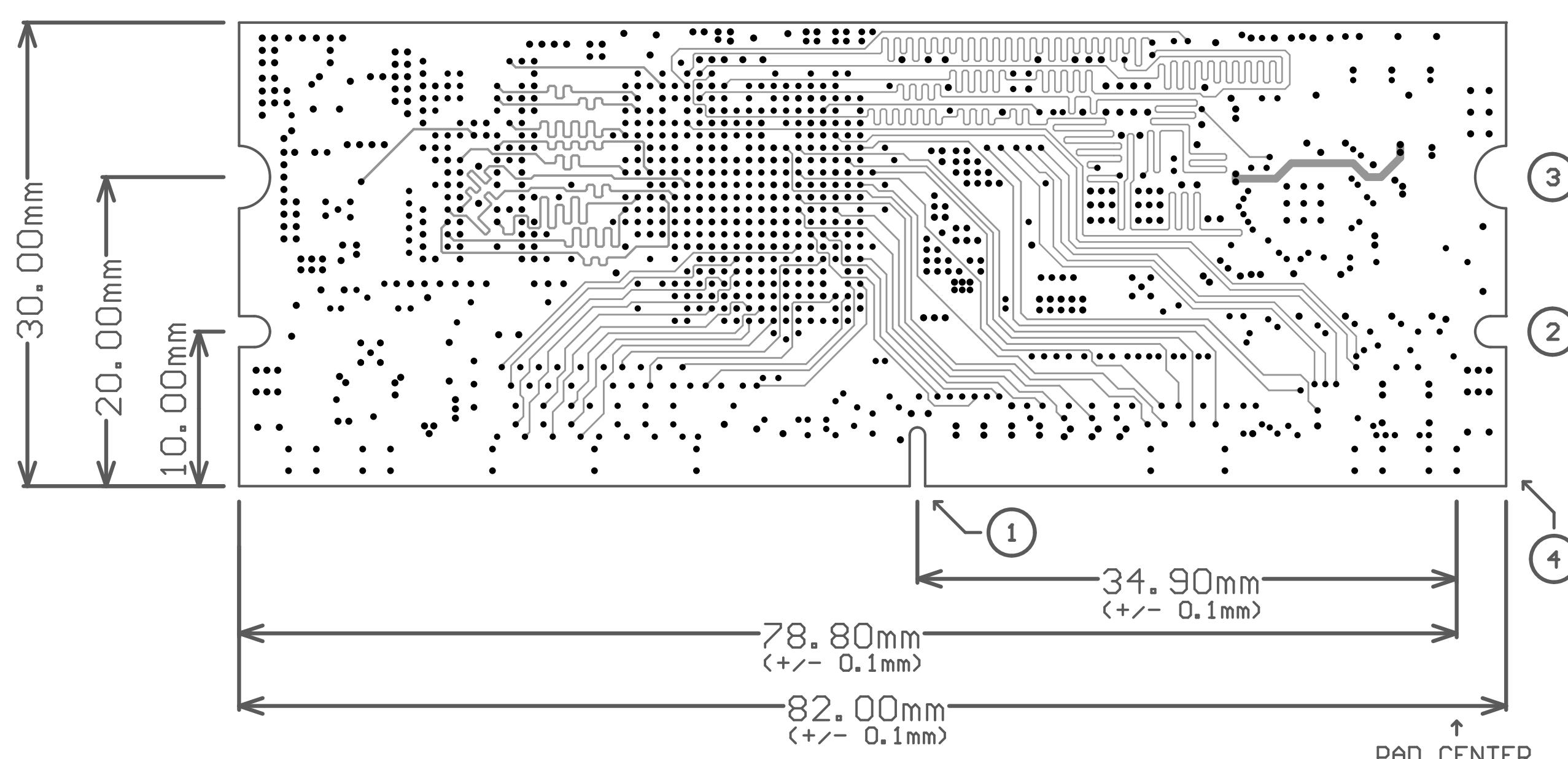
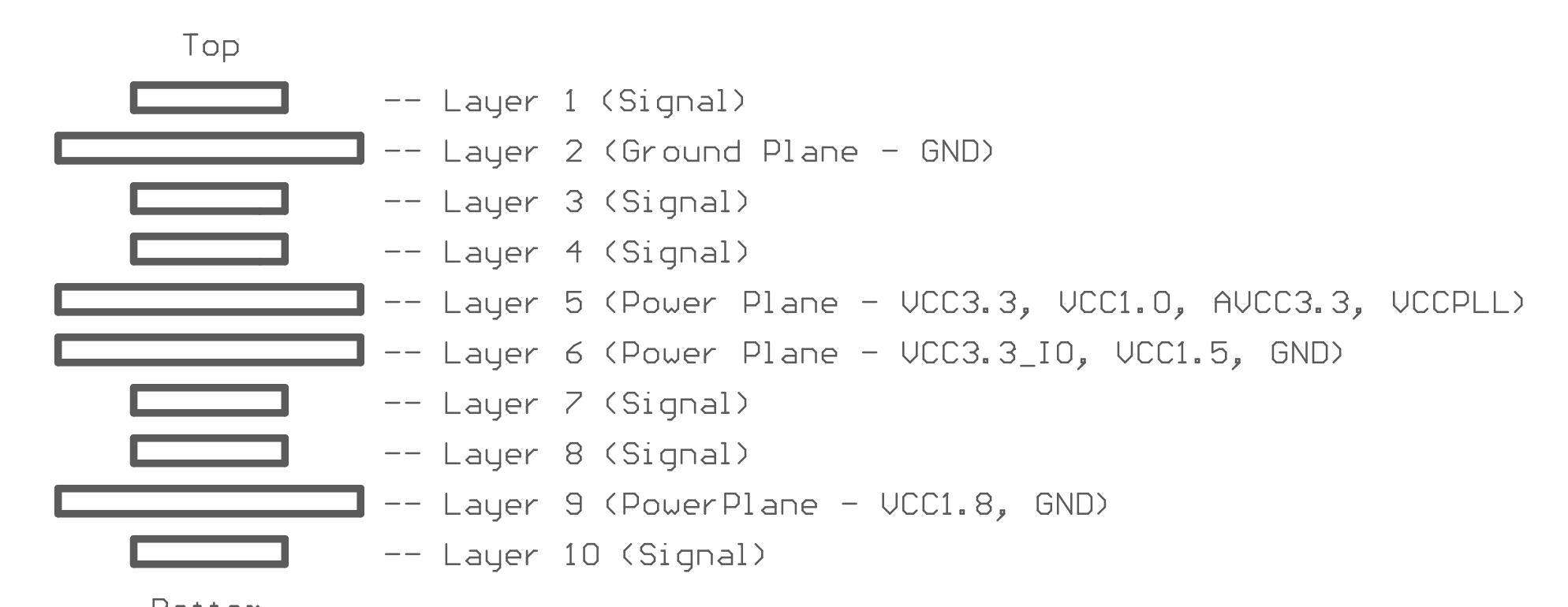
1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

Internal layers (3, 4, 7, 8):	External Layers (1 and 10):
40 Ohm: 6 mil tracks in artwork	40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

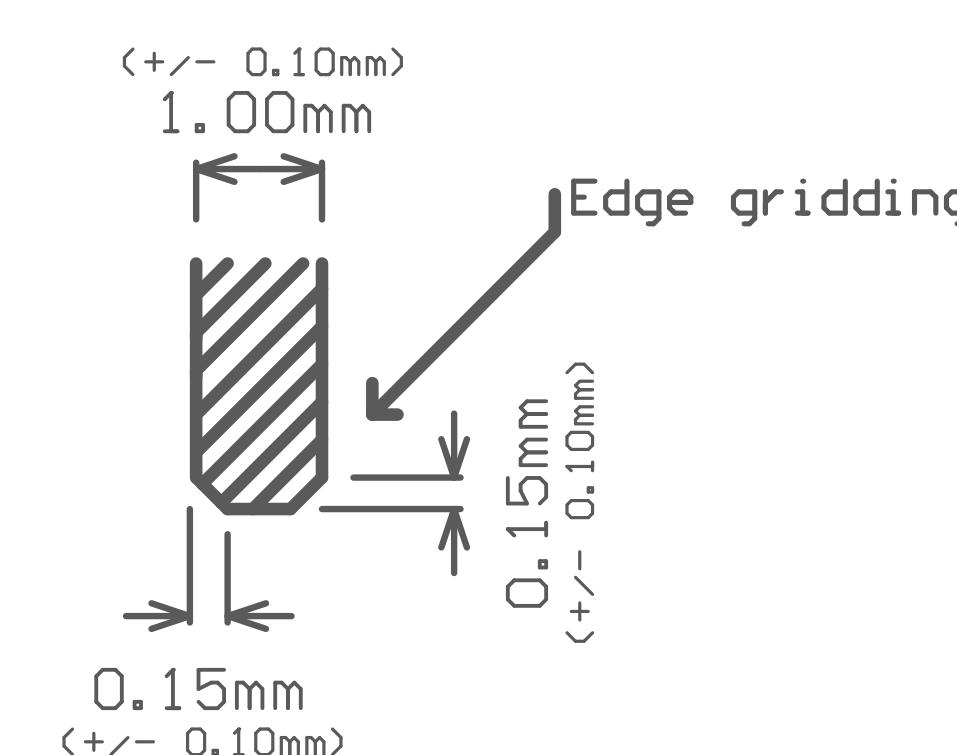
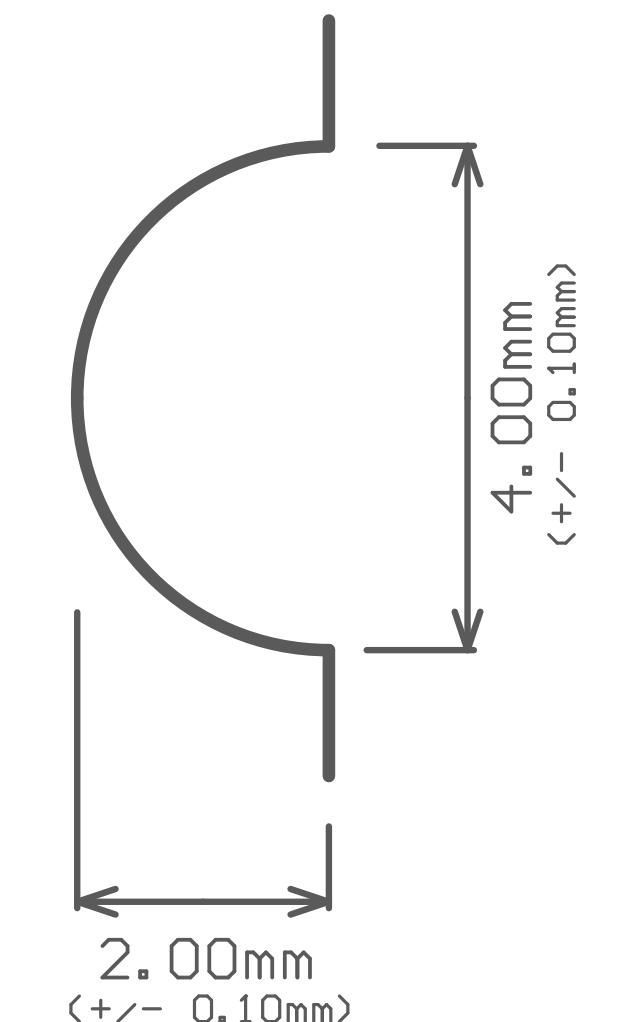
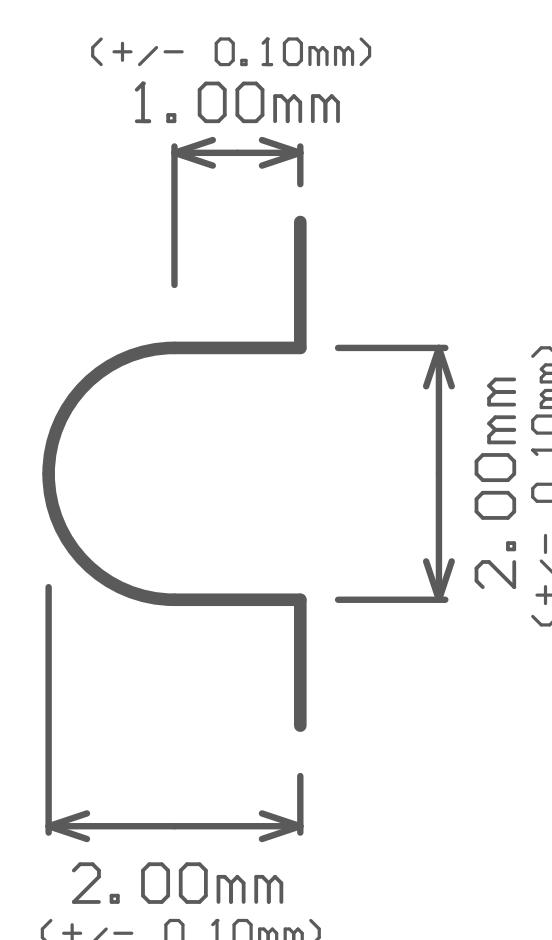
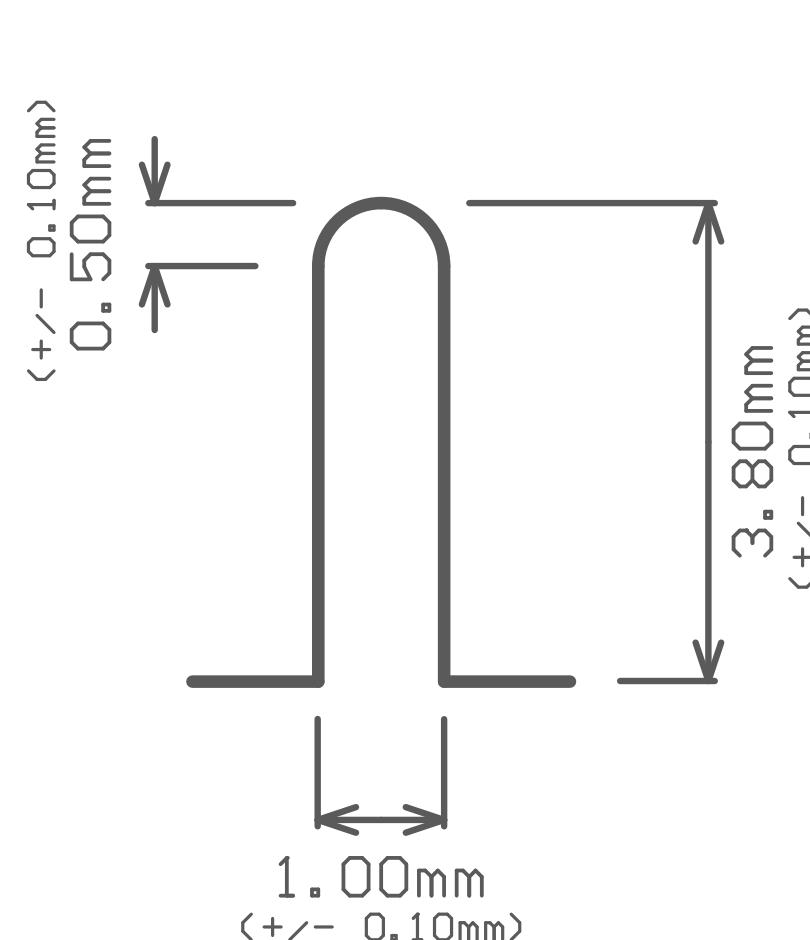
UW-IPMC MEZZANINE (revB)

Layer 8 - Signal (Copper)

**Layer Stackup**Univ. of Wisconsin-Madison
Madison, WI 53706ENGINEER:
Vicente, M.PCB DESIGNER:
Vicente, M.DATE:
06JUN2019FILE NAME:
ZYNQ_IPMC.PCBDOCTITLE:
ZYNQ-IPMC

PART NO.:

REV:
revB1SCALE:
1:1



Specifications:

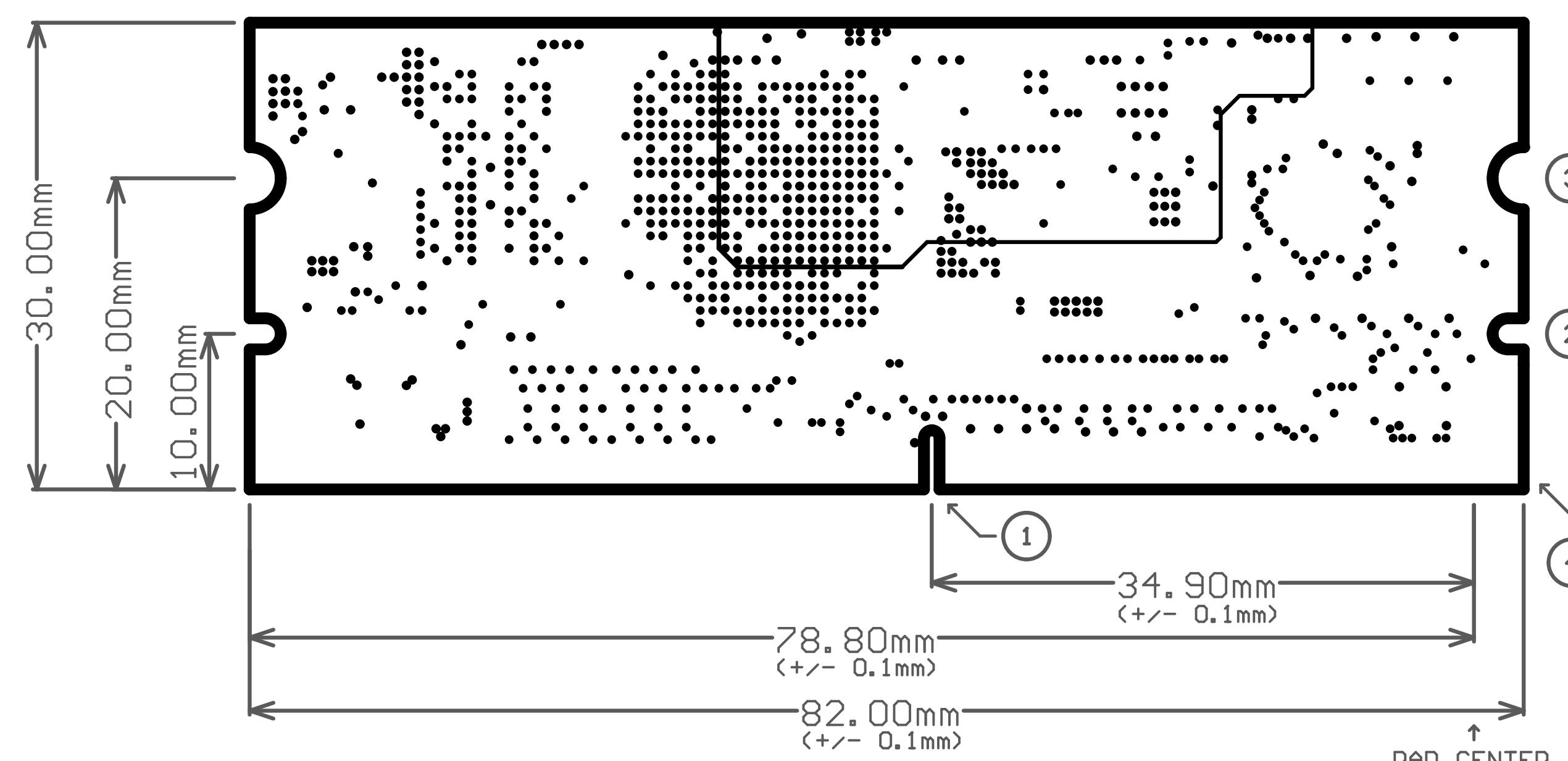
1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170$ C
2. Overall thickness is 1.0mm ± 0.10 mm
3. Board dimensions are 82 by 30mm with tolerances of ± 0.15 mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

Internal layers (3, 4, 7, 8):	
40 Ohm:	6 mil tracks in artwork
50 Ohm:	4.0 mil tracks in artwork
External Layers (1 and 10):	
40 Ohm:	9.5 mil tracks in artwork
50 Ohm:	6.5 mil tracks in artwork

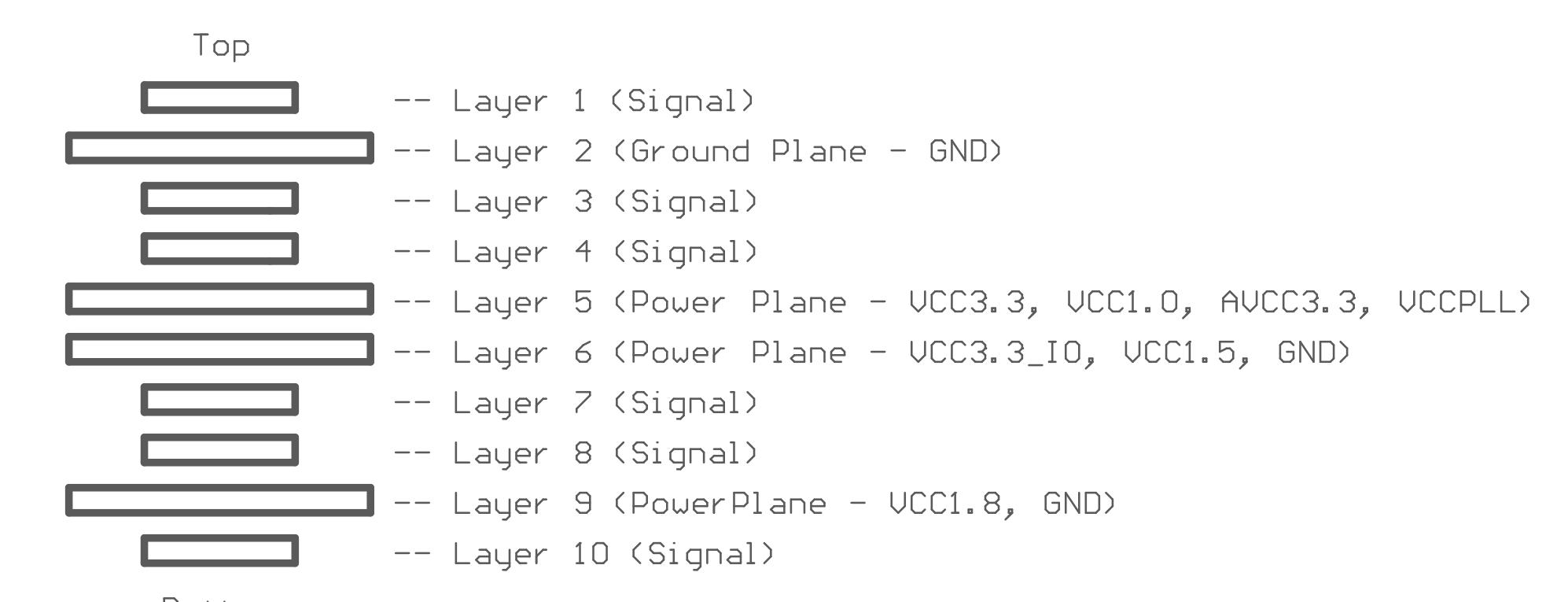
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating ± 3 mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

UW-IPMC MEZZANINE (revB)

Layer 9 - Power Plane (Copper, Mask)



Layer Stackup



Univ. of Wisconsin-Madison
Madison, WI 53706

ENGINEER:
Vicente, M.

PCB DESIGNER:
Vicente, M.

DATE:
06JUN2019

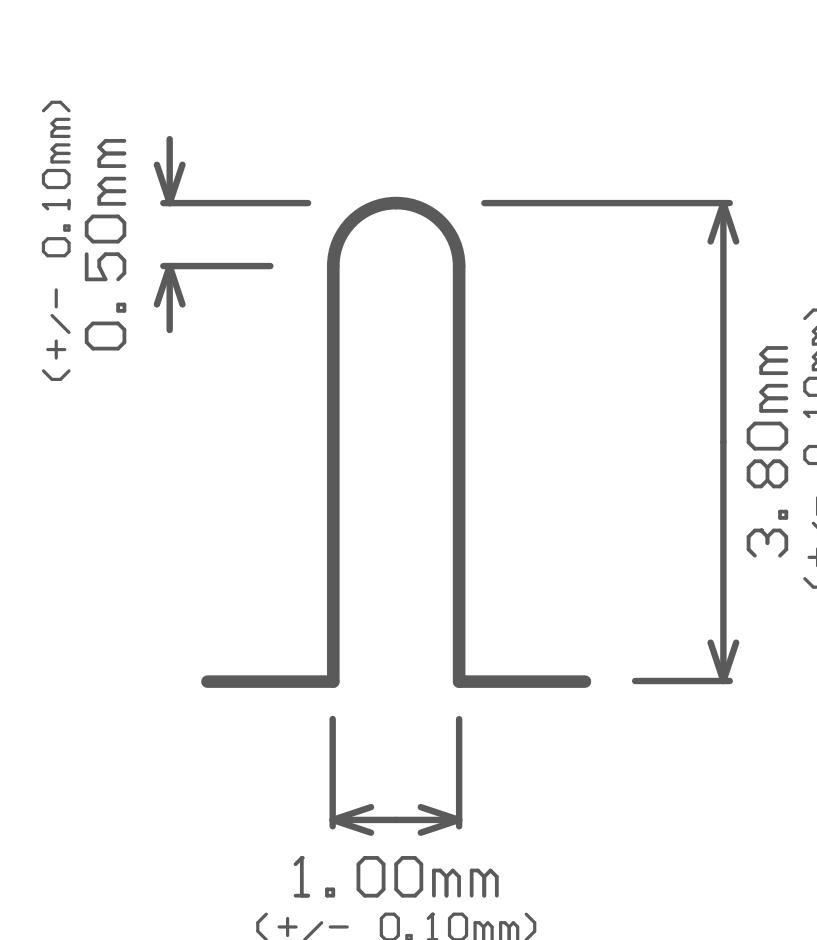
FILE NAME:
ZYNQ_IPMC.PCBDOC

TITLE:
ZYNQ-IPMC

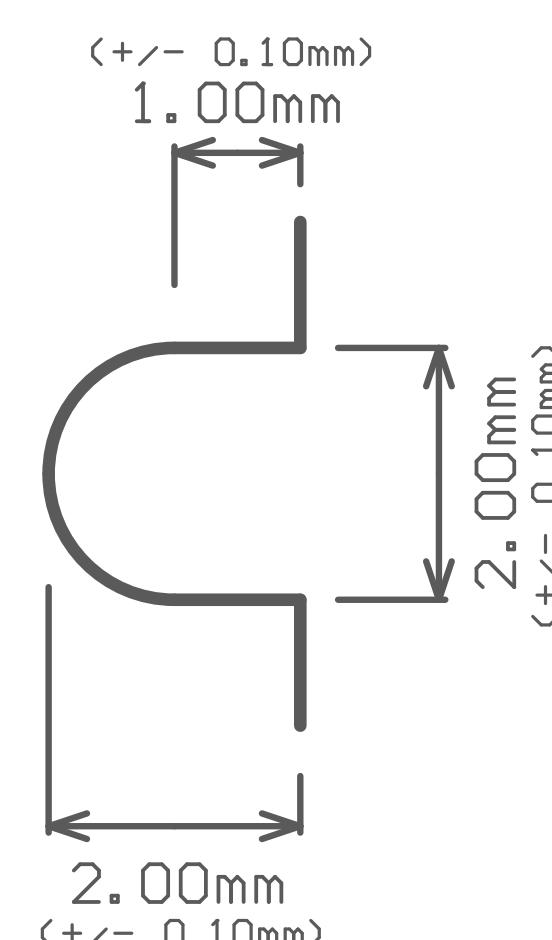
PART NO.:

REV:
revB1

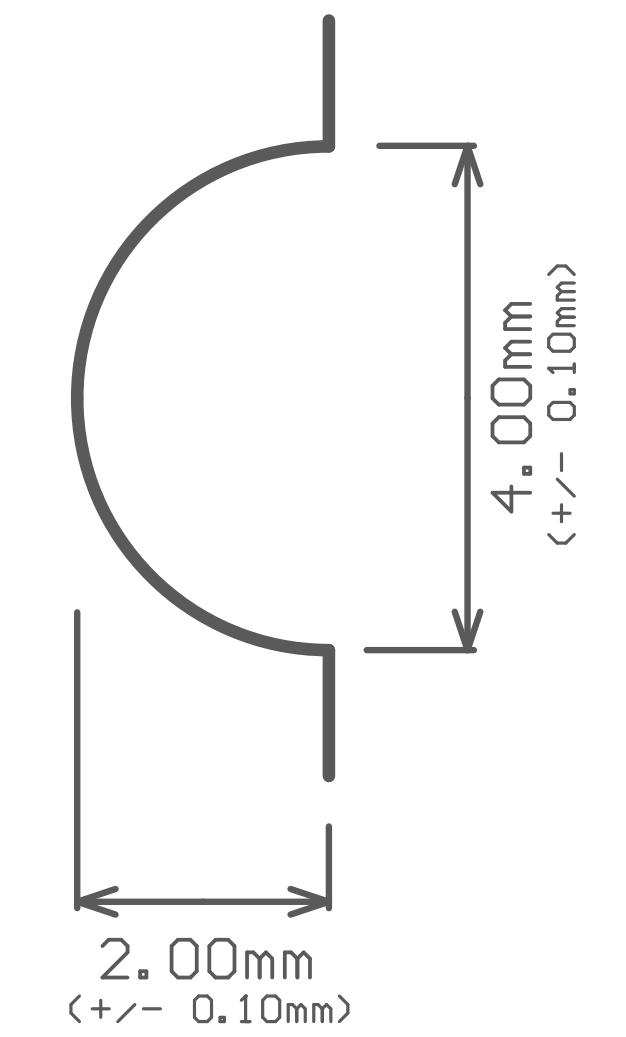
SCALE:
1:1



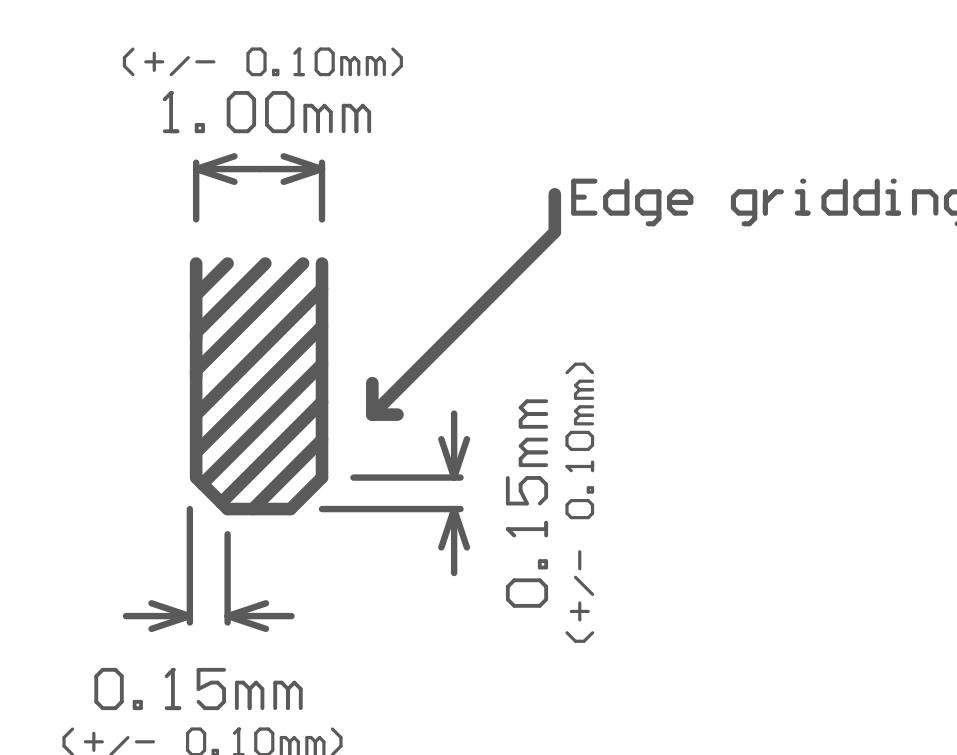
Detail 1



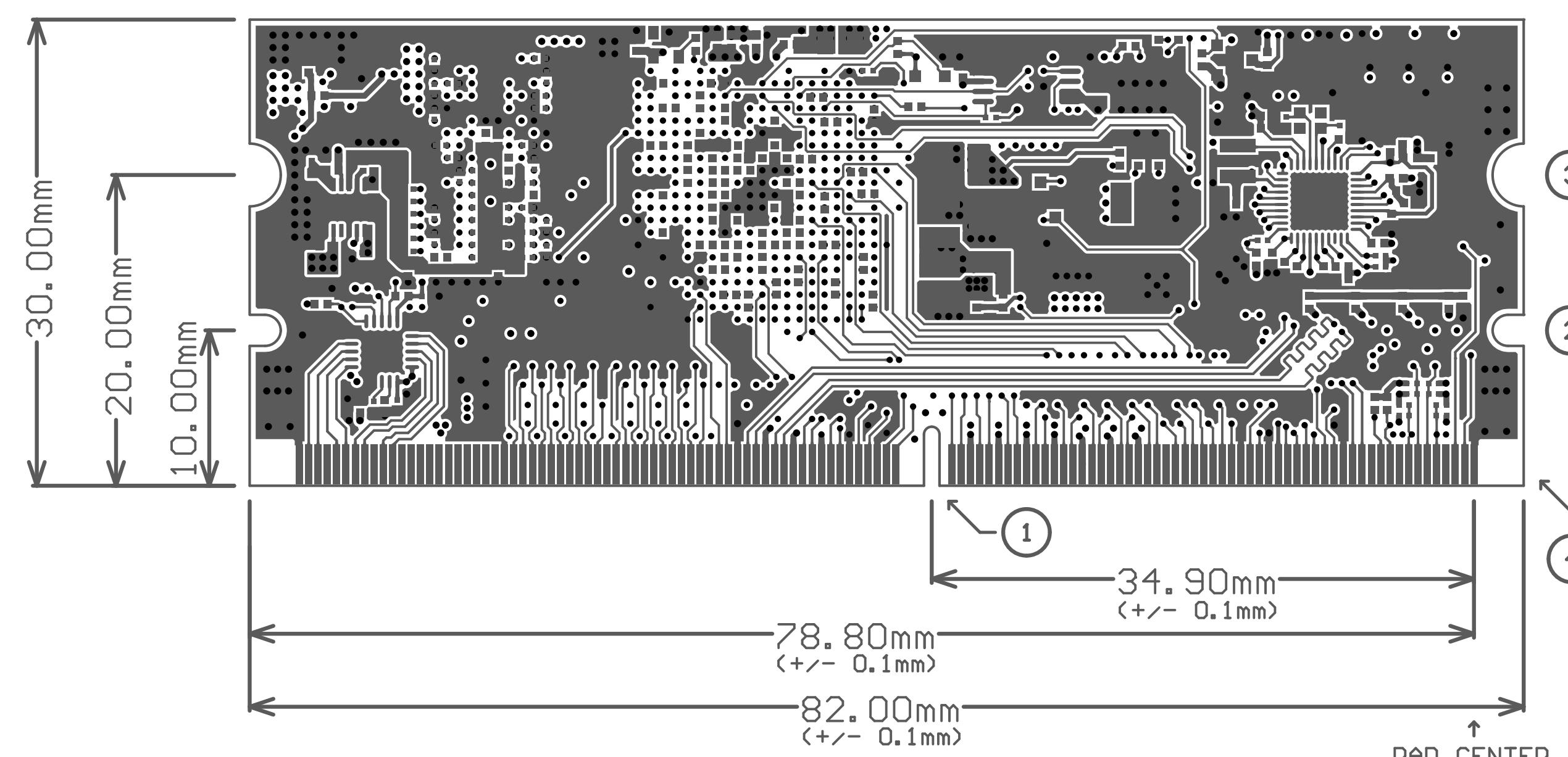
Detail 2



Detail 3

Detail 4
(PCB side view)**UW-IPMC MEZZANINE (revB)**

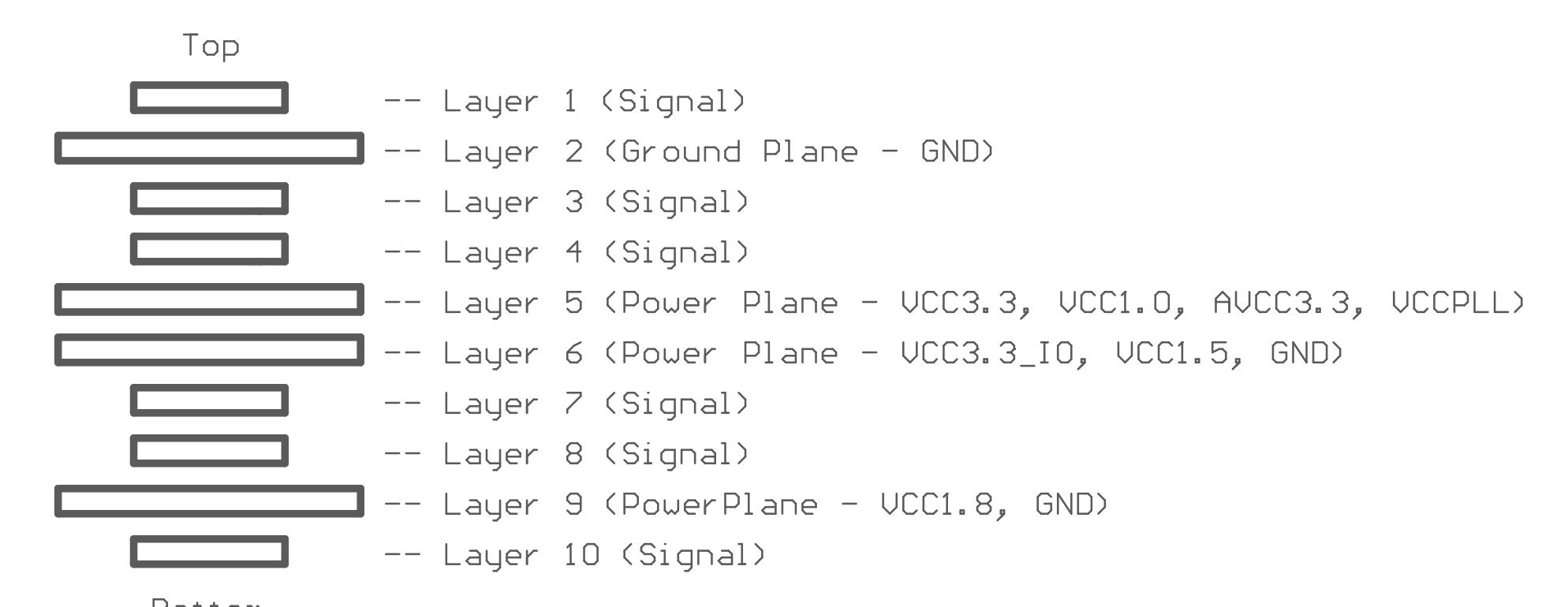
Layer 10 - Signal (Copper)

**Specifications:**

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm +/- 0.10mm
3. Board dimensions are 82 by 30mm with tolerances of +/- 0.15mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

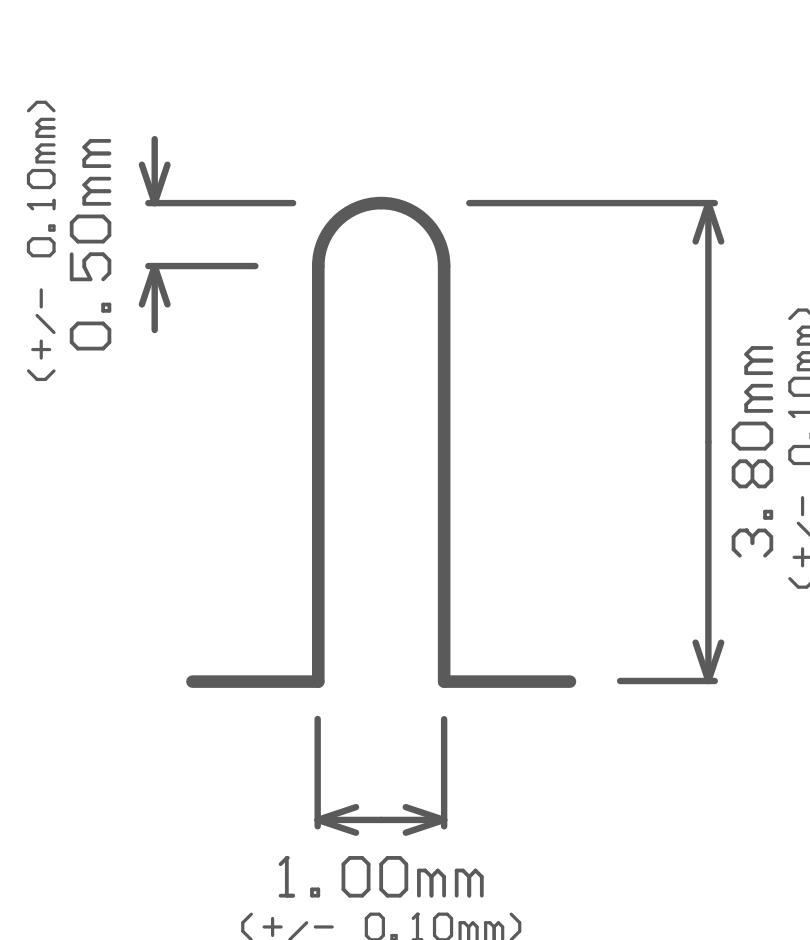
Internal layers (3, 4, 7, 8):	External Layers (1 and 10):
40 Ohm: 6 mil tracks in artwork	40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

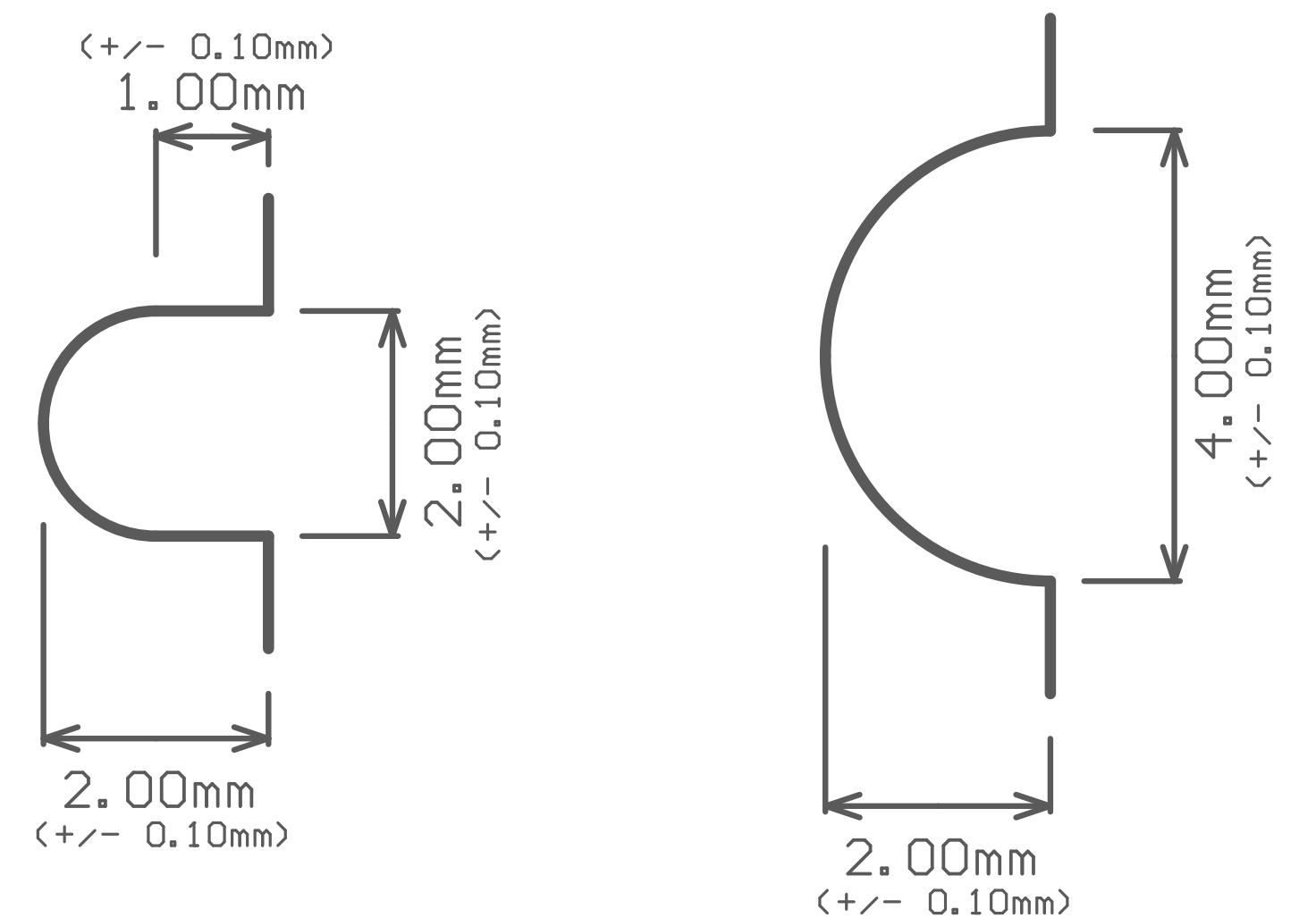
Layer StackupUniv. of Wisconsin—Madison
Madison, WI 53706ENGINEER:
Vicente, M.PCB DESIGNER:
Vicente, M.DATE:
06JUN2019FILE NAME:
ZYNQ_IPMC.PCBDOCTITLE:
ZYNQ-IPMC

PART NO.:

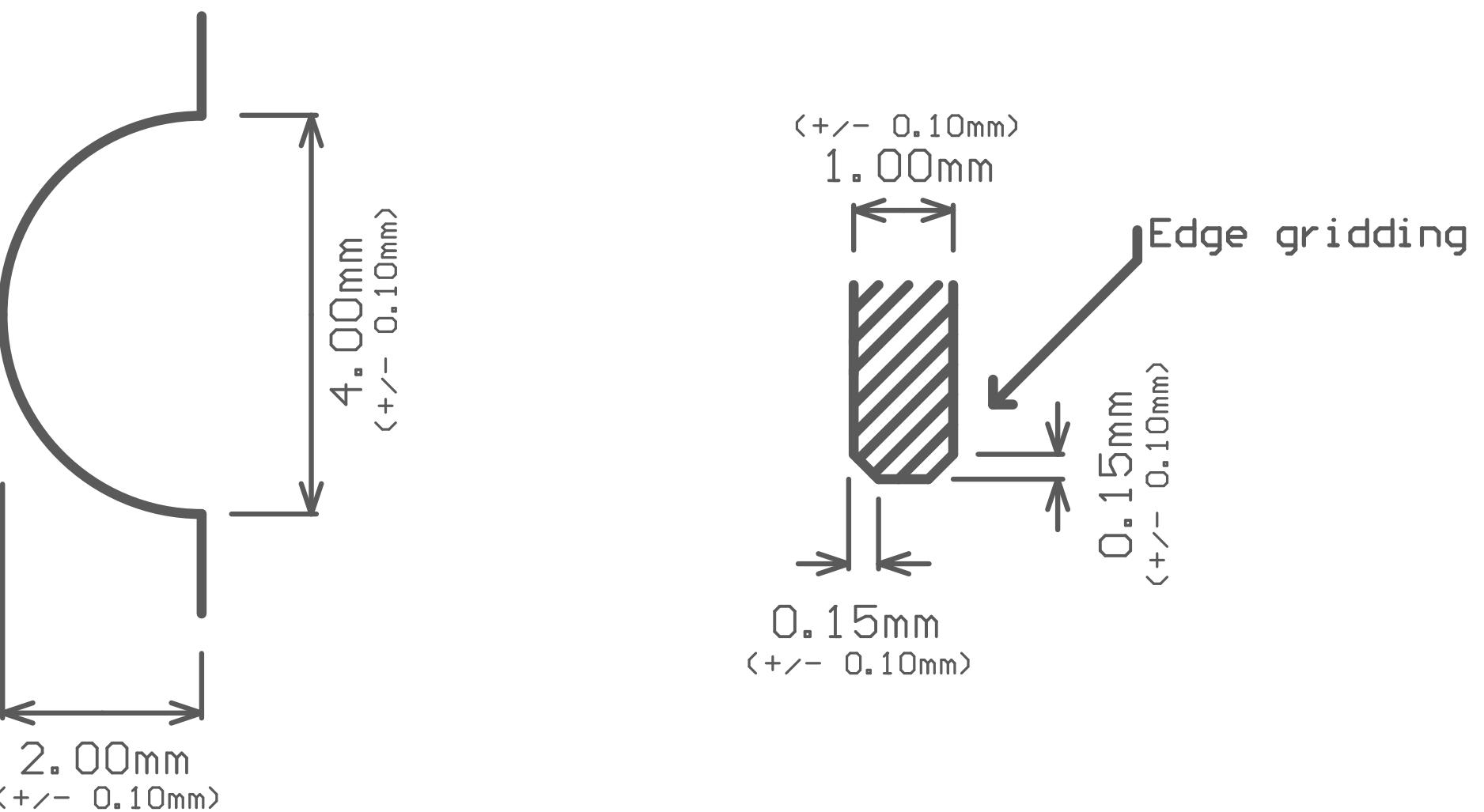
REV:
revB1SCALE:
1:1



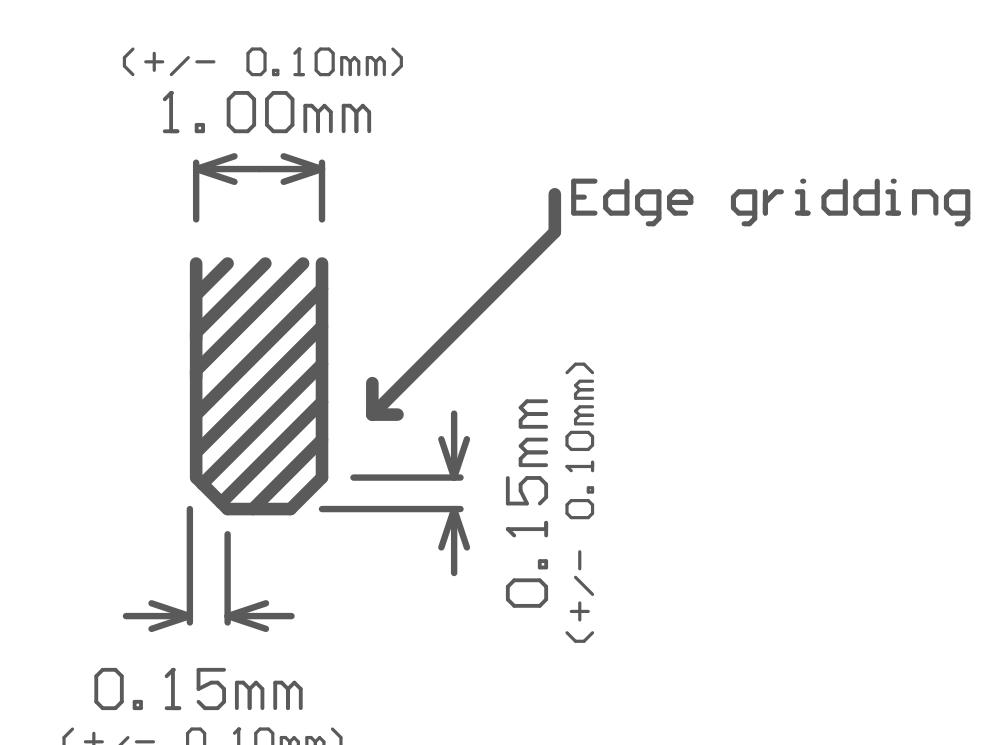
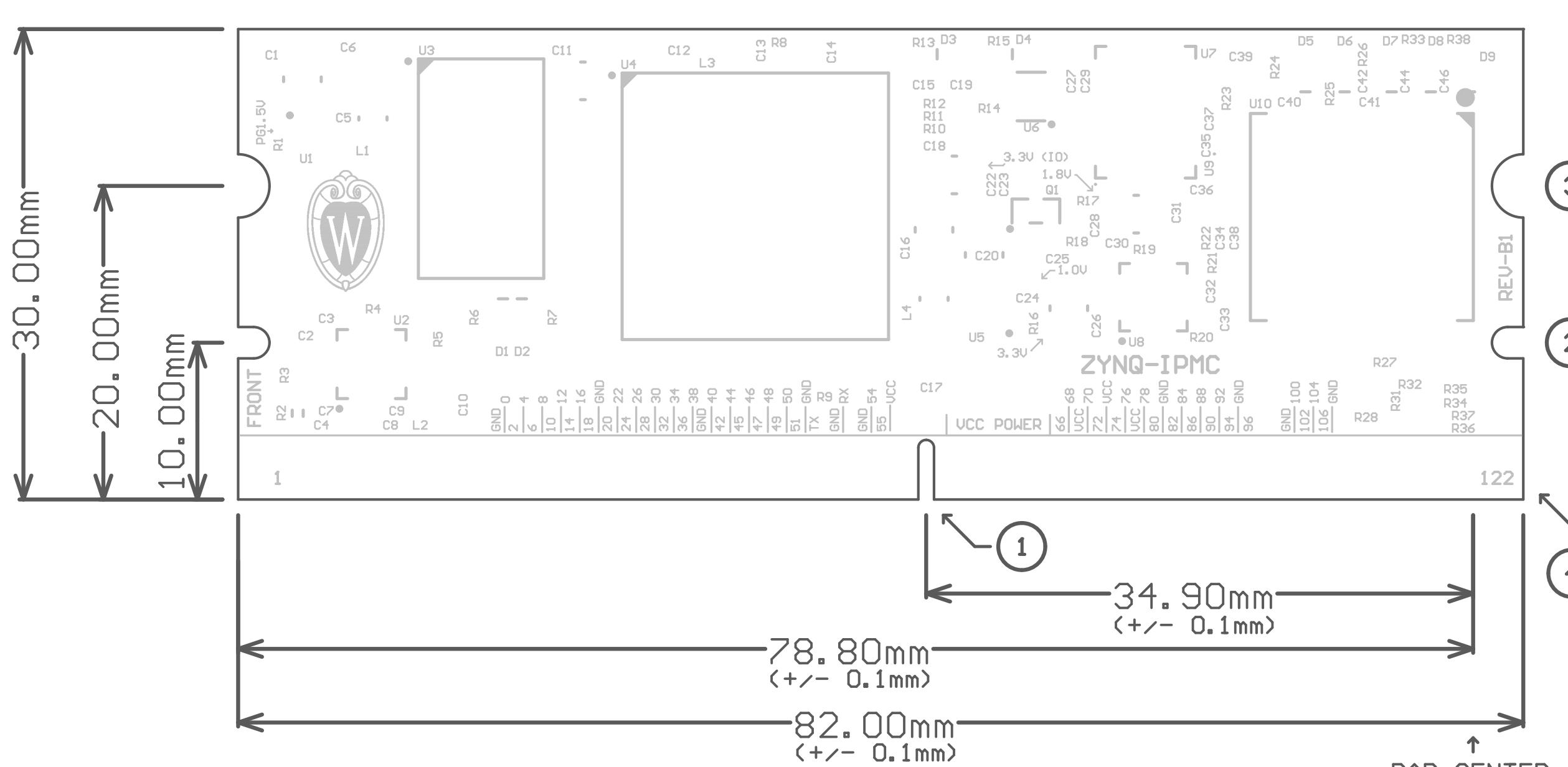
Detail 1



Detail 2



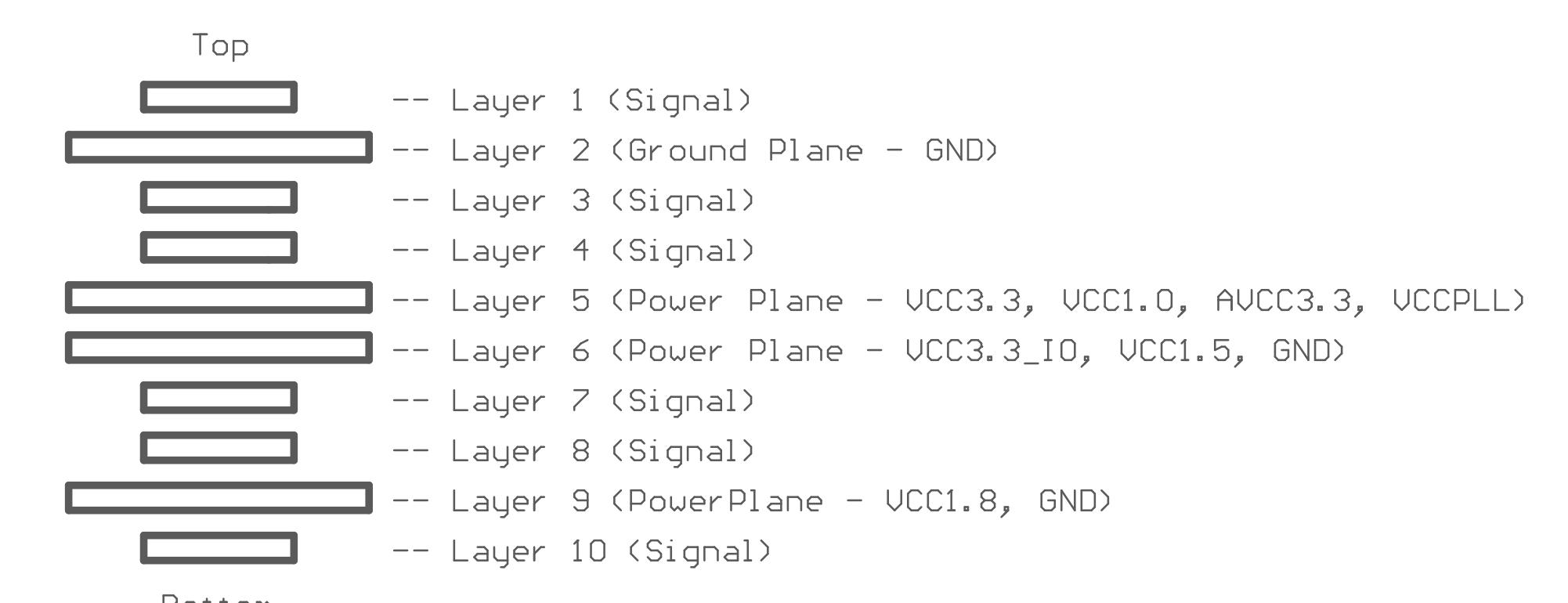
Detail 3

Detail 4
(PCB side view)**UW-IPMC MEZZANINE (revB)**

Top Overlay (Ink)

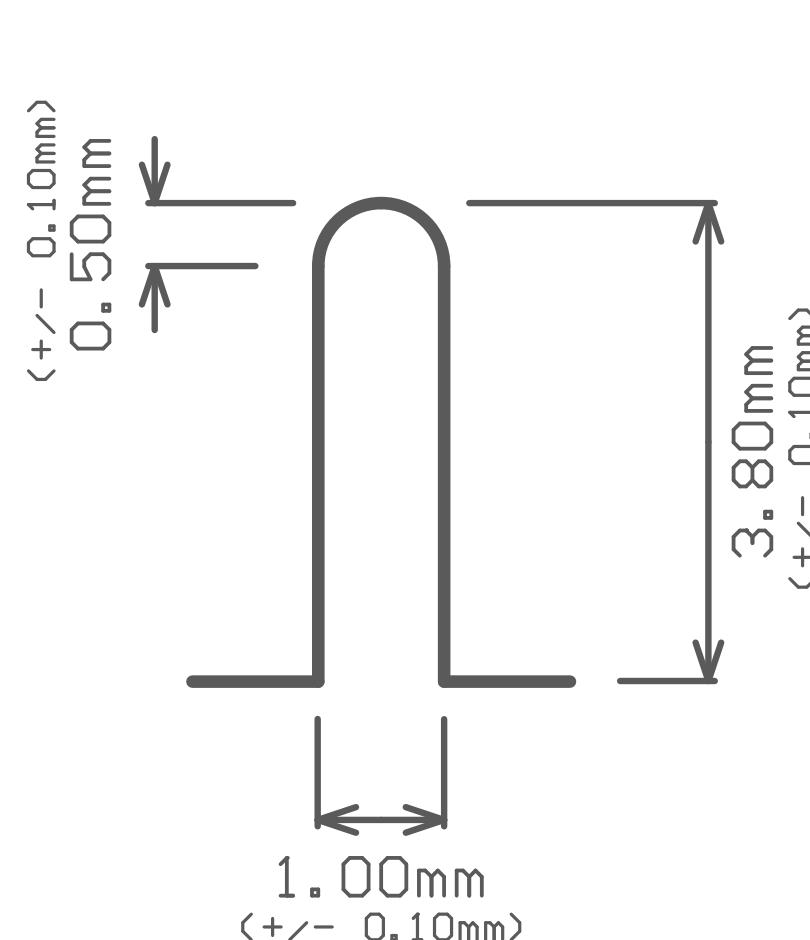
Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm +/- 0.10mm
3. Board dimensions are 82 by 30mm with tolerances of +/- 0.15mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 - Internal layers (3, 4, 7, 8):
 - 40 Ohm: 6 mil tracks in artwork
 - 50 Ohm: 4.0 mil tracks in artwork
 - External Layers (1 and 10):
 - 40 Ohm: 9.5 mil tracks in artwork
 - 50 Ohm: 6.5 mil tracks in artwork
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

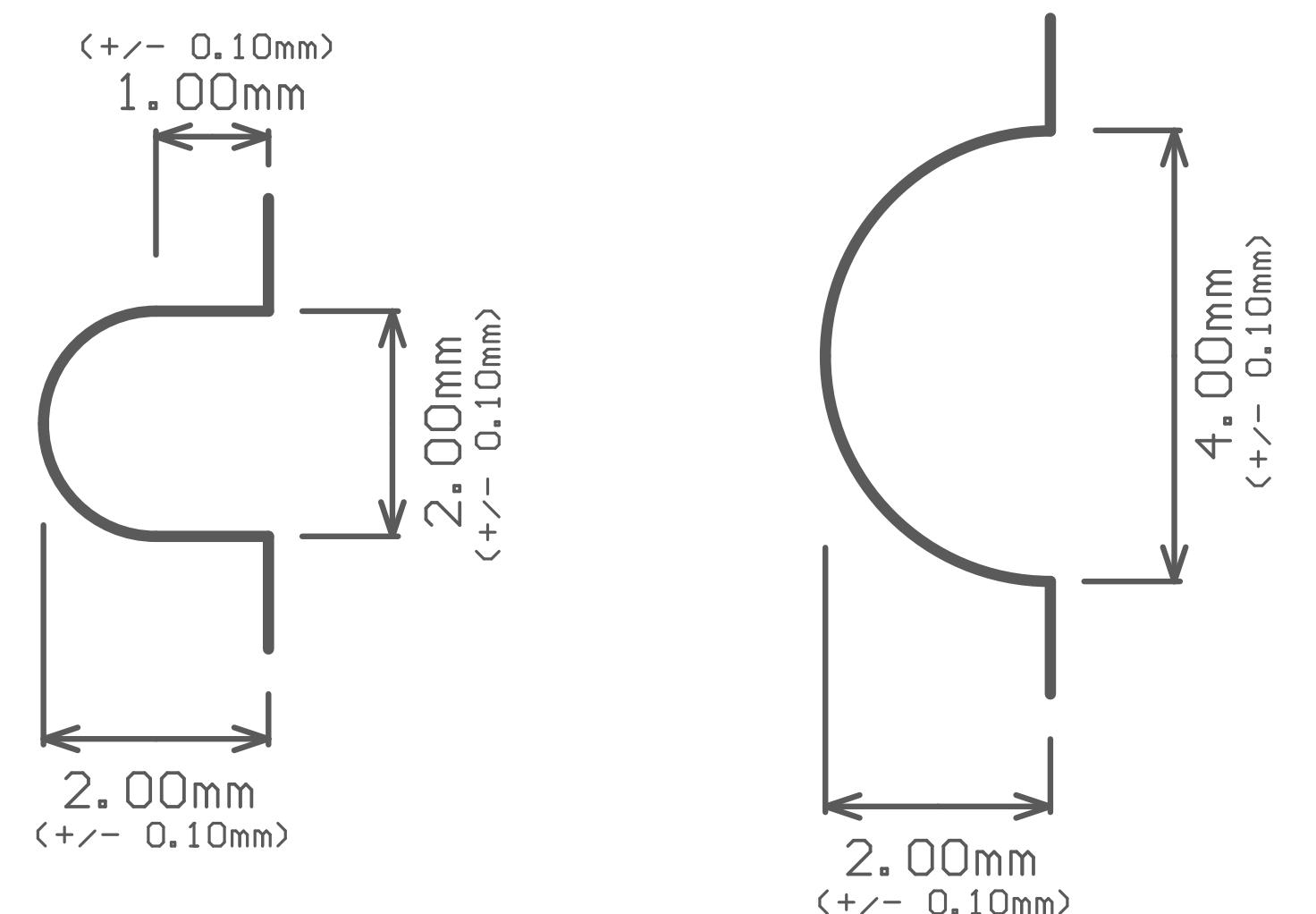
Layer StackupUniv. of Wisconsin—Madison
Madison, WI 53706ENGINEER:
Vicente, M.PCB DESIGNER:
Vicente, M.DATE:
06JUN2019FILE NAME:
ZYNQ_IPMC.PCBDOCTITLE:
ZYNQ-IPMC

PART NO.:

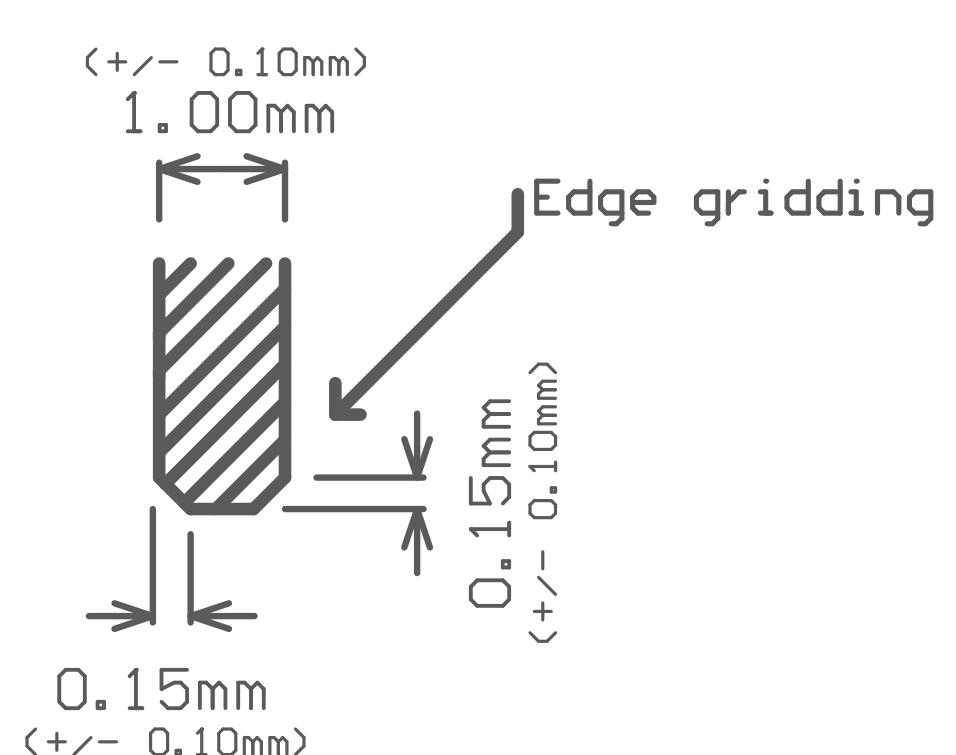
REV:
revB1SCALE:
1:1



Detail 1



Detail 2



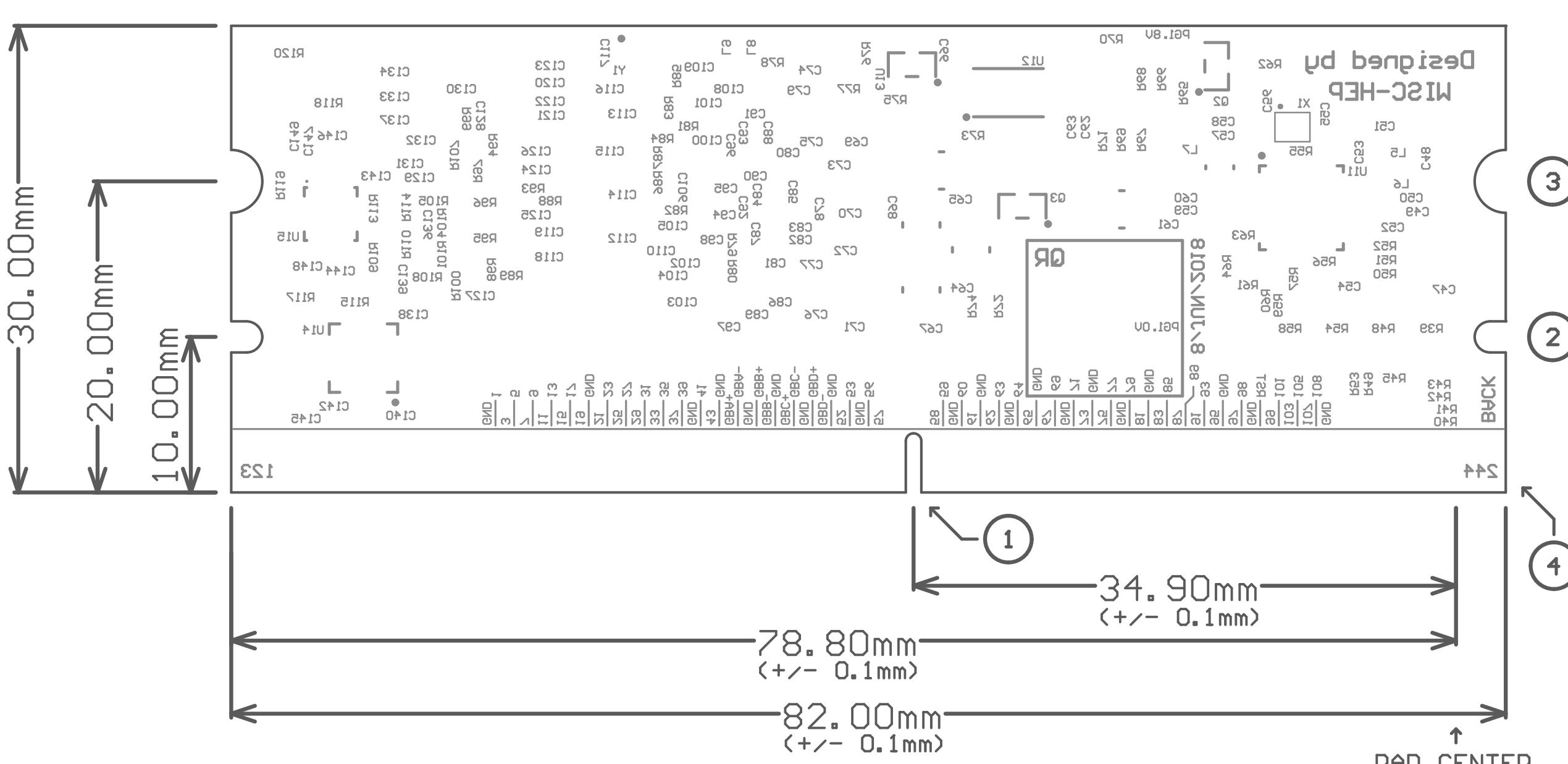
Detail 3

Detail 4
(PCB side view)**Specifications:**

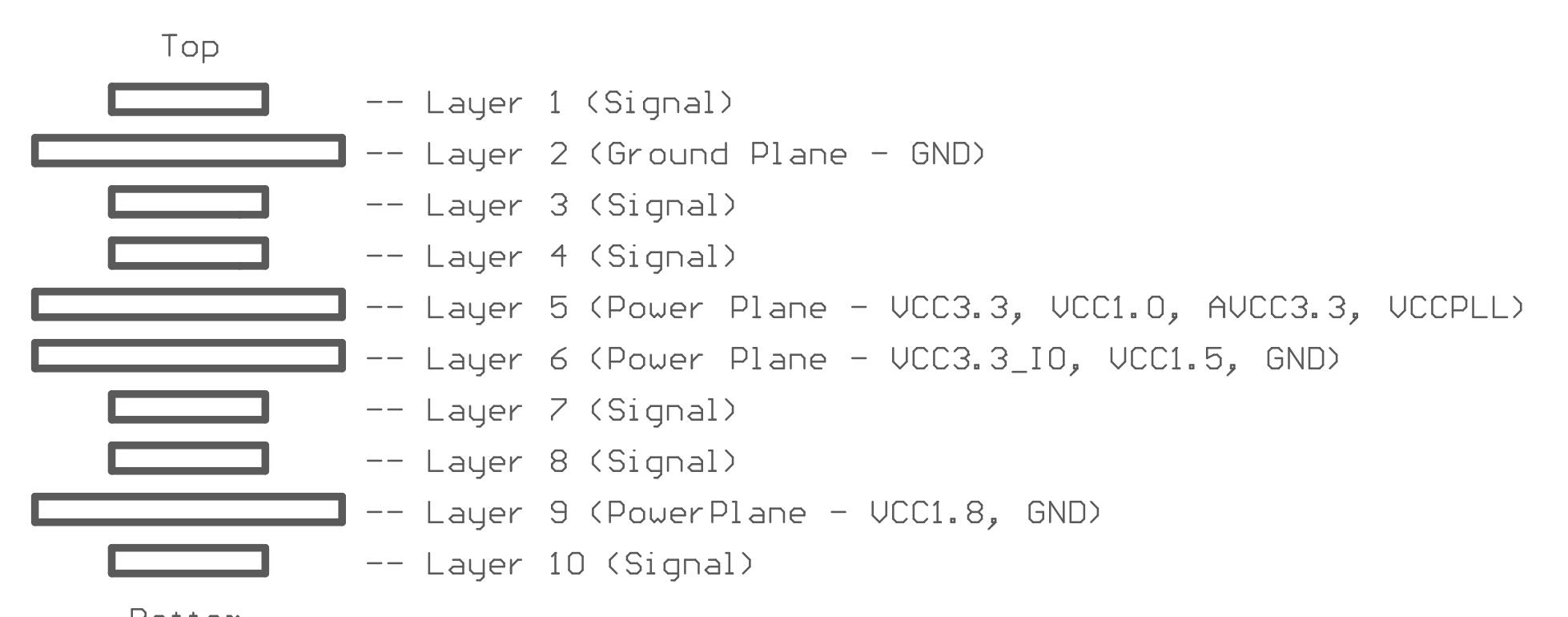
1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

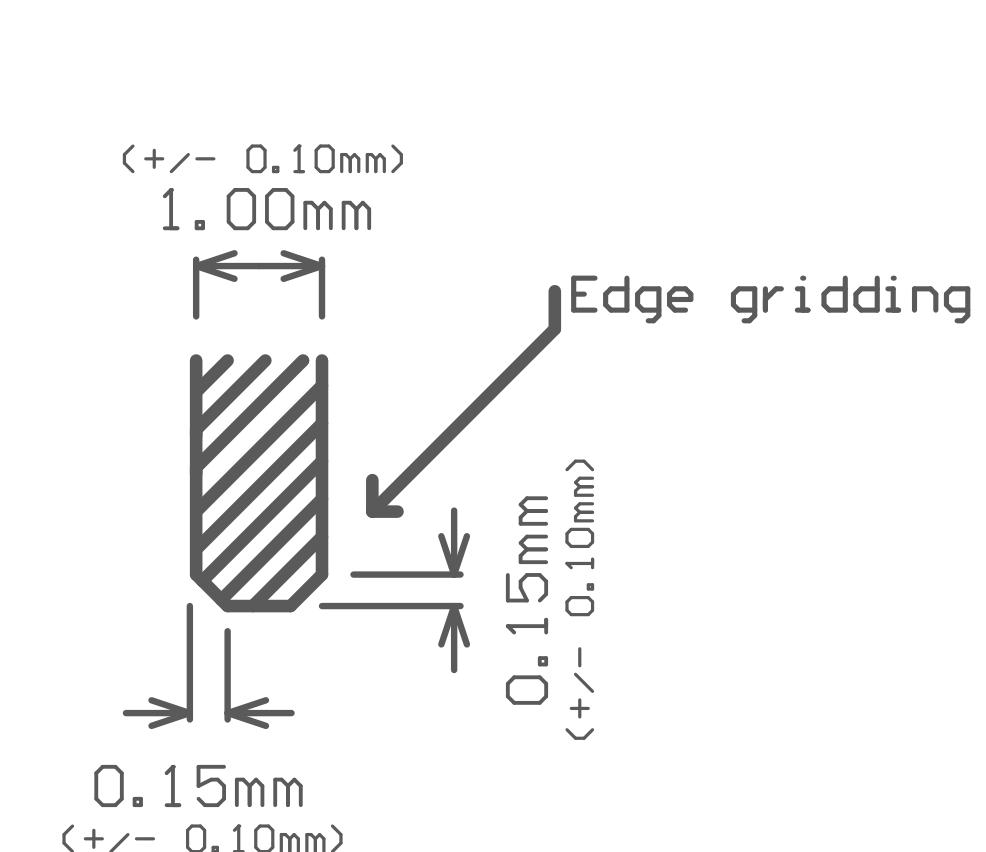
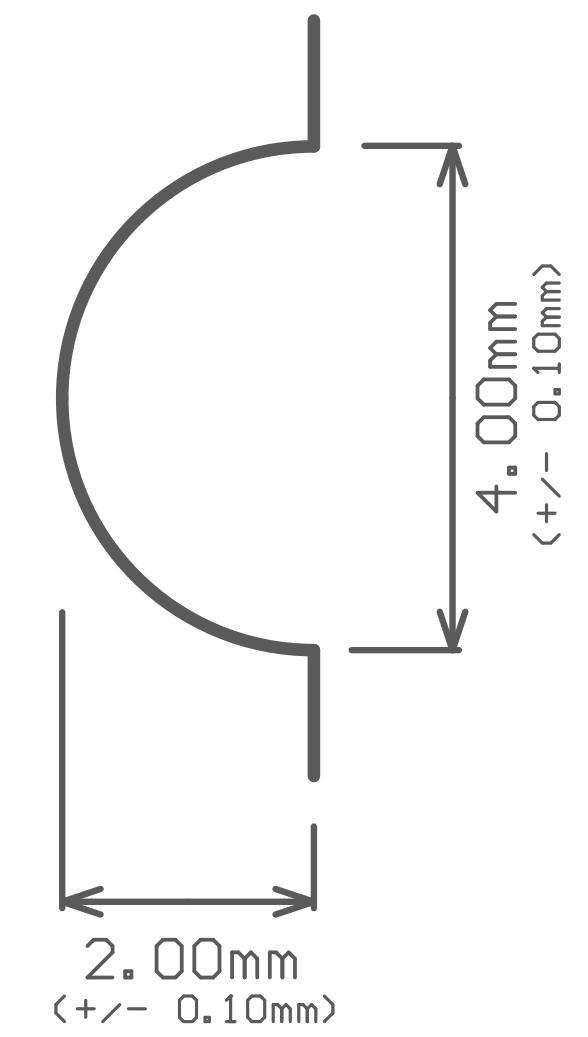
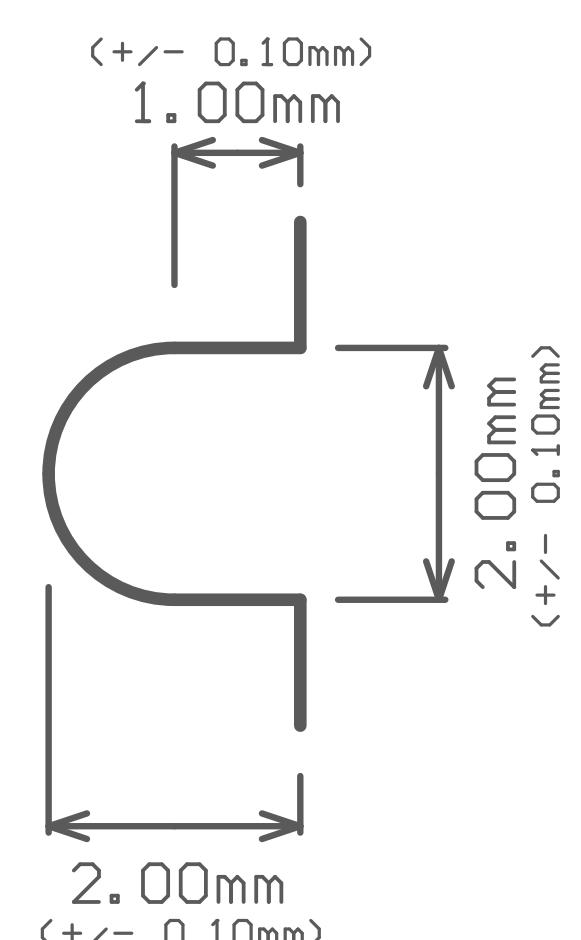
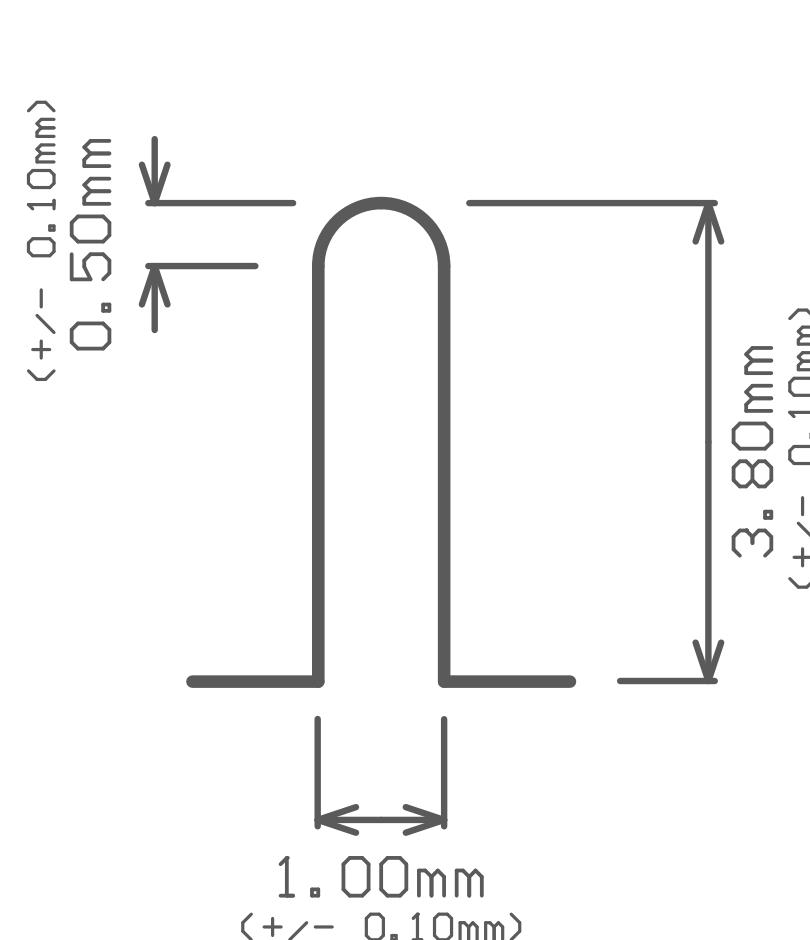
UW-IPMC MEZZANINE (revB)

Bottom Overlay (Ink)

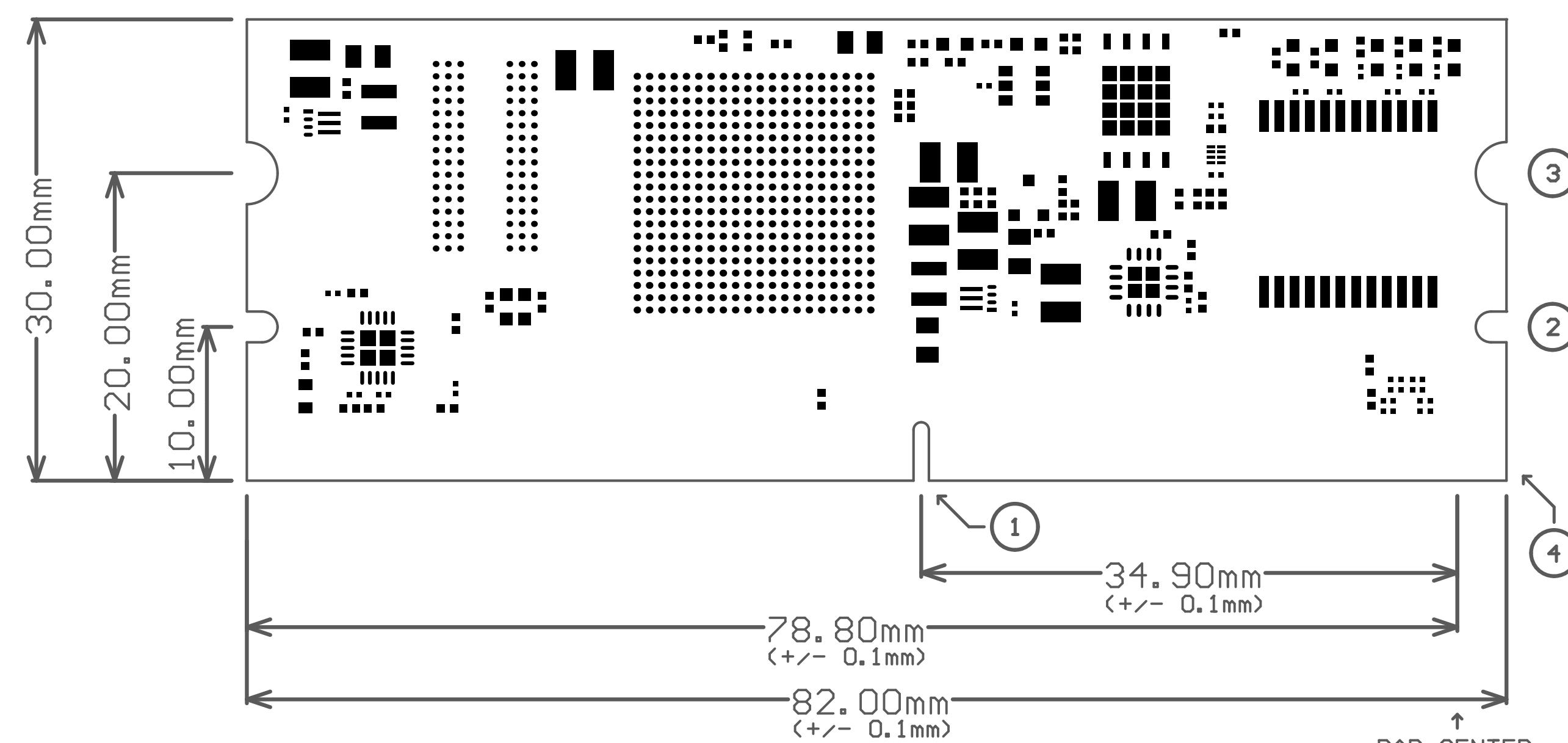
Layer StackupUniv. of Wisconsin—Madison
Madison, WI 53706ENGINEER:
Vicente, M.
PCB DESIGNER:
Vicente, M.TITLE:
ZYNQ-IPMCDATE:
06JUN2019
FILE NAME:
ZYNQ_IPMC.PCBDOC

PART NO.:

REV:
revB1
SCALE:
1:1



UW-IPMC MEZZANINE (revB)



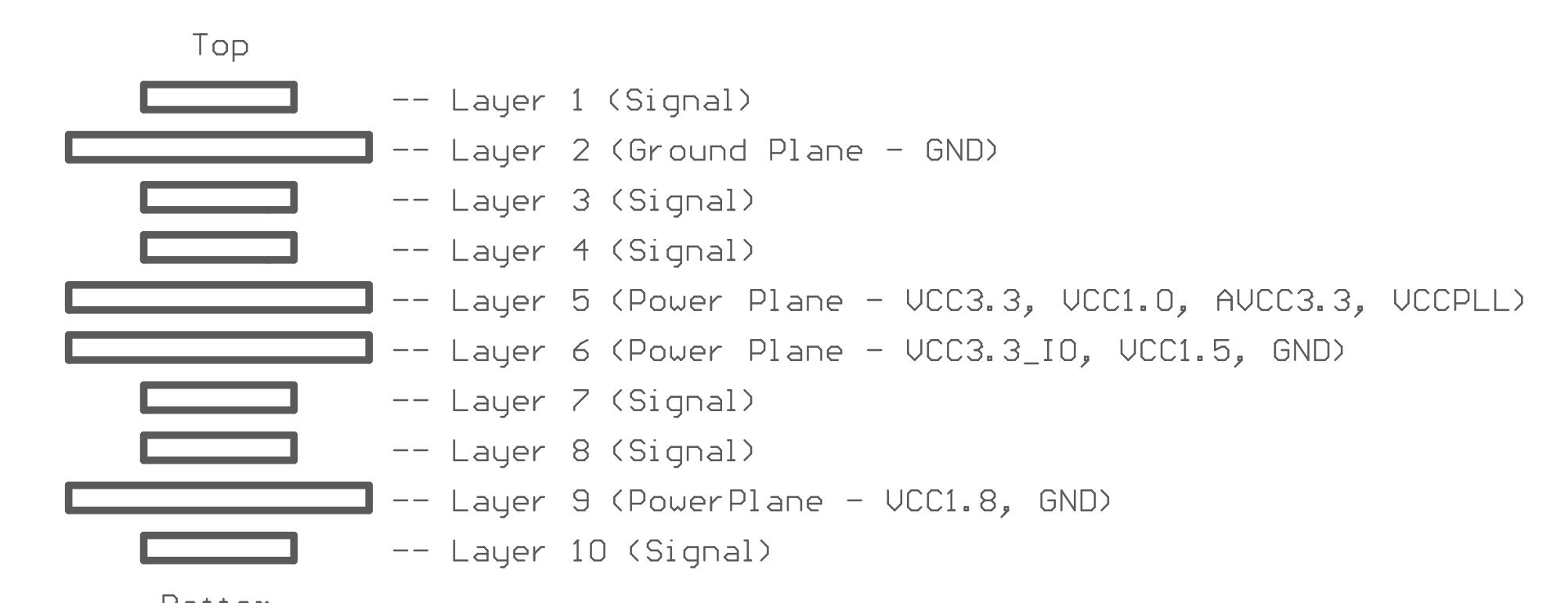
Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170$ C
2. Overall thickness is 1.0mm ± 0.10 mm
3. Board dimensions are 82 by 30mm with tolerances of ± 0.15 mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating ± 3 mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup



Univ. of Wisconsin—Madison
Madison, WI 53706

ENGINEER:
Vicente, M.

TITLE:
ZYNQ-IPMC

PCB DESIGNER:
Vicente, M.

DATE:
06JUN2019

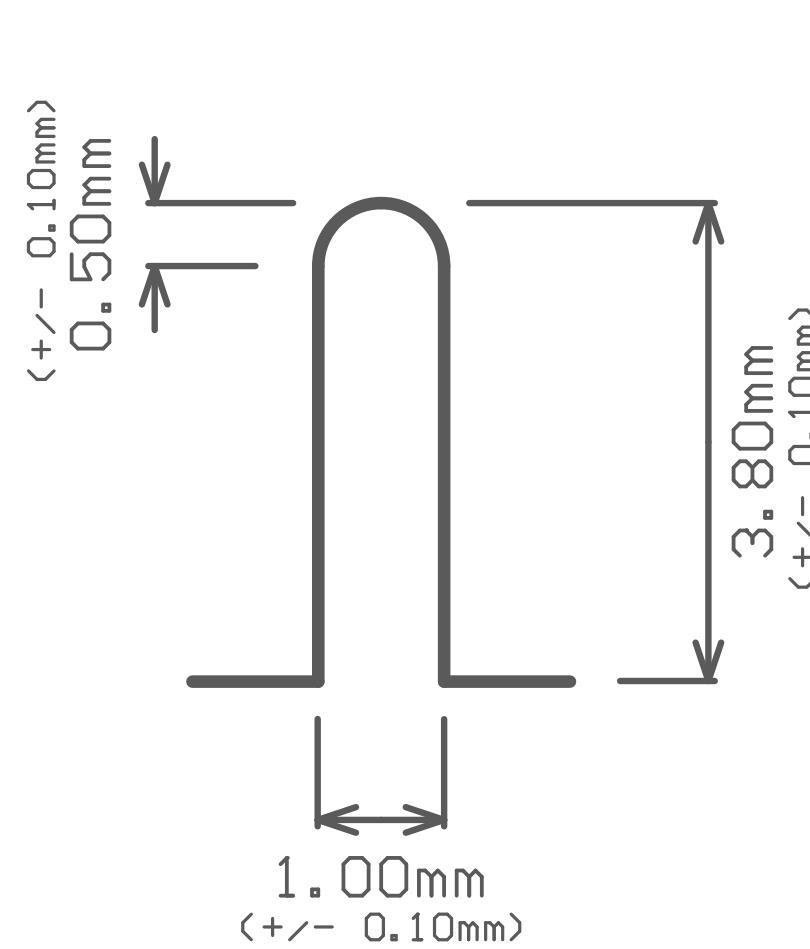
PART NO.:

REV:
revB1

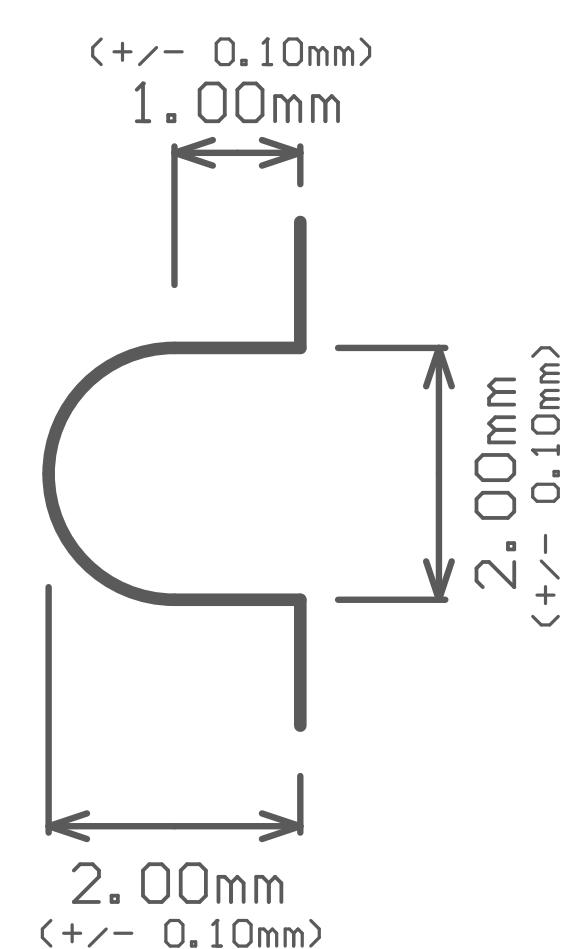
FILE NAME:
ZYNQ_IPMC.PCBDOC

DWG NO.:

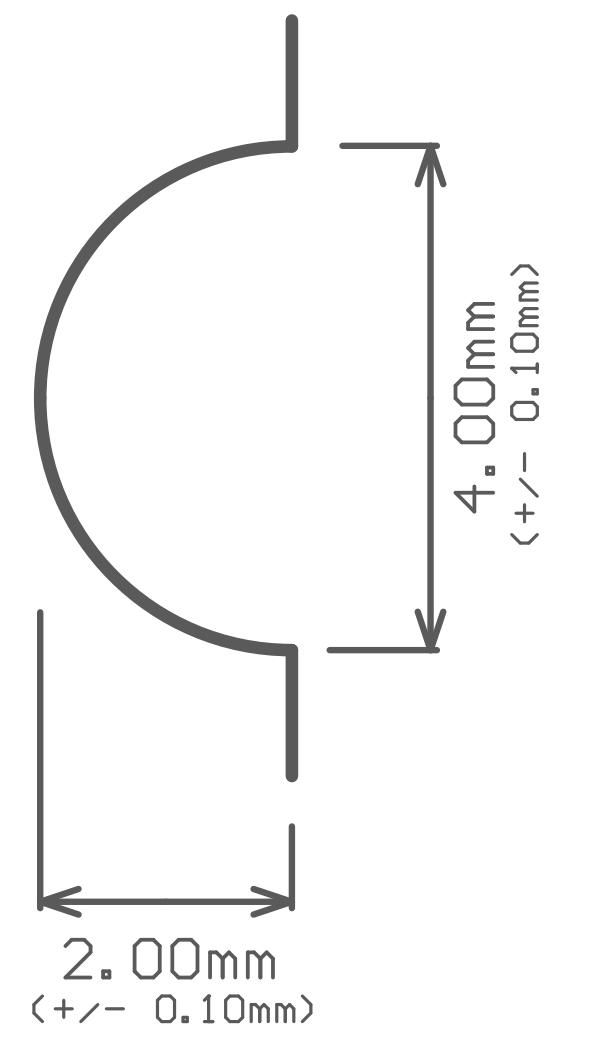
SCALE:
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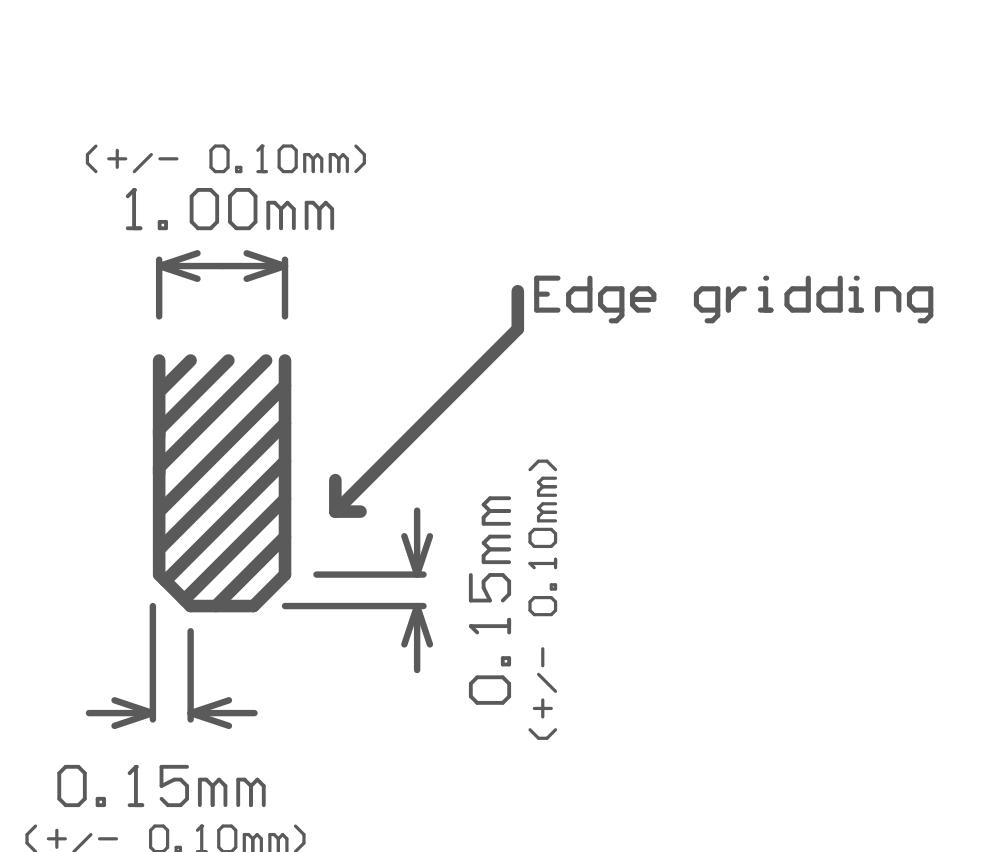
Detail 1



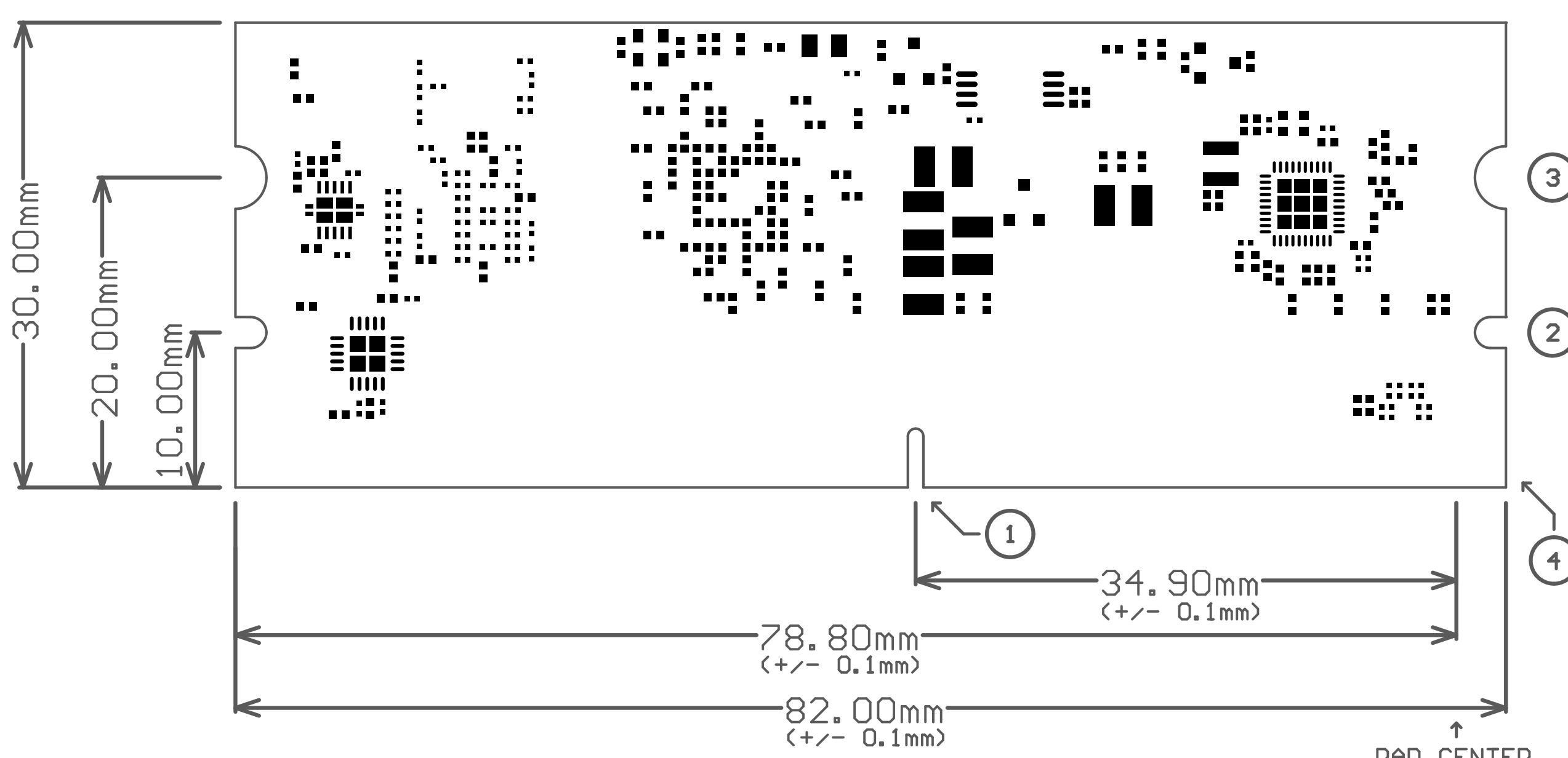
Detail 2



Detail 3

Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)

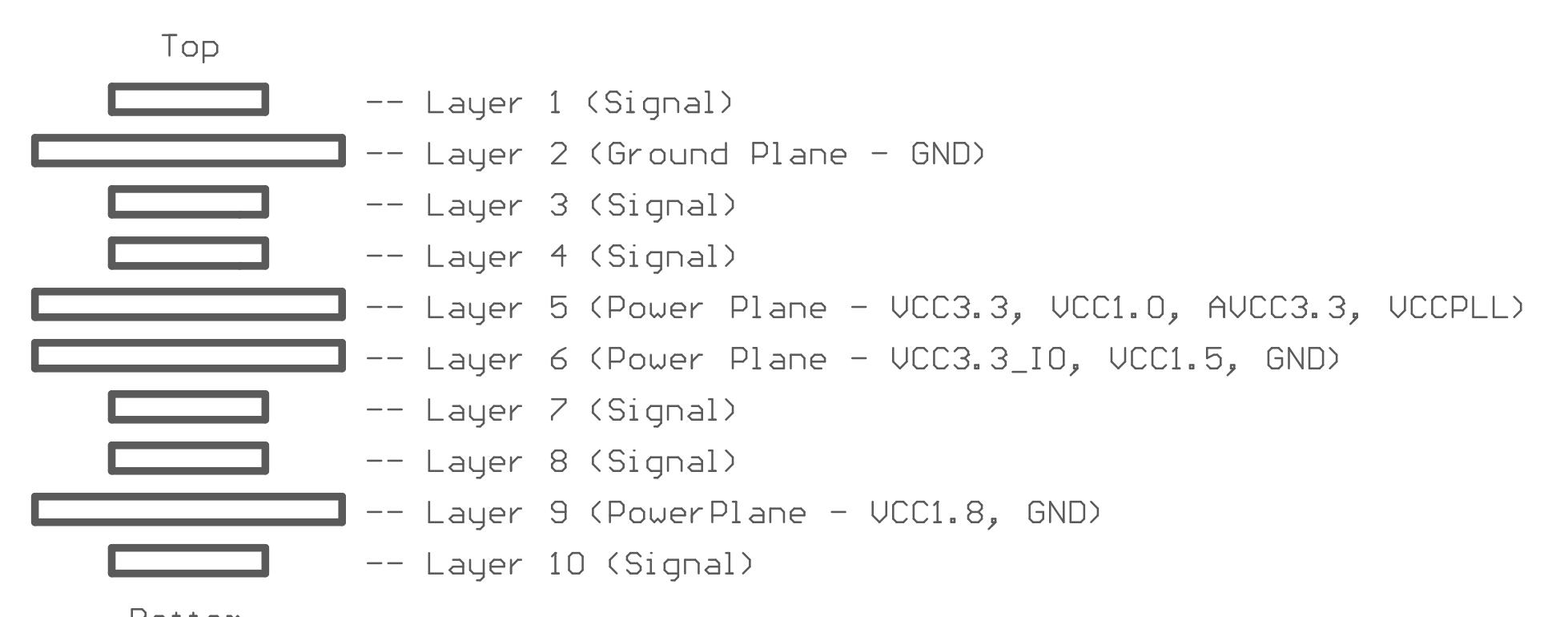


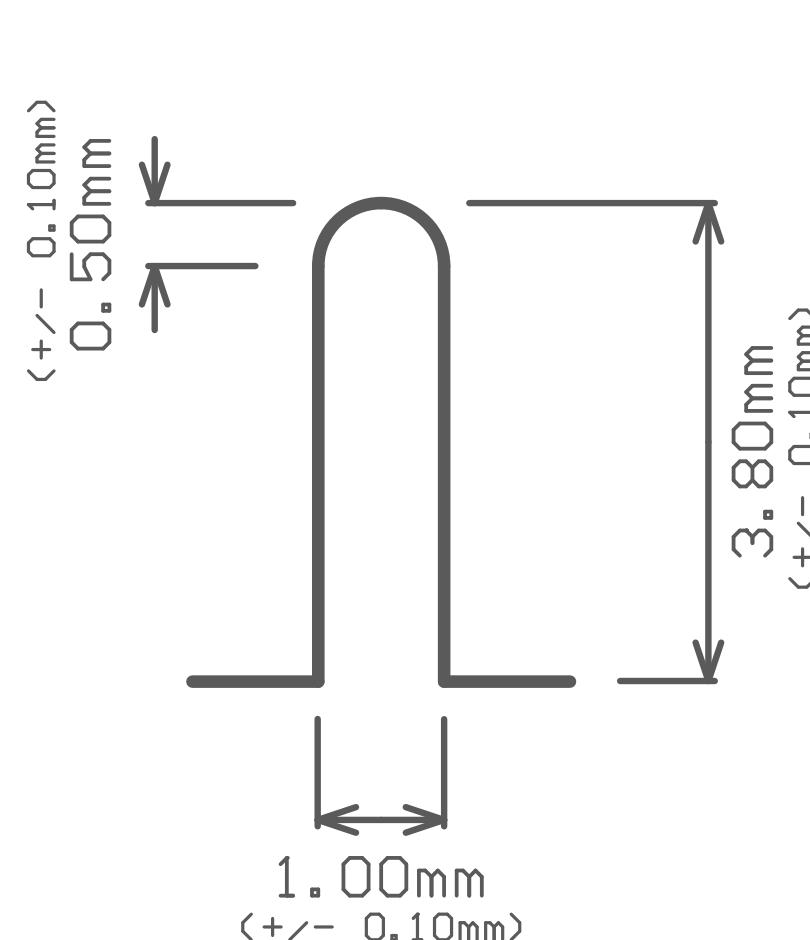
Bottom Paste (Paste)

Specifications:

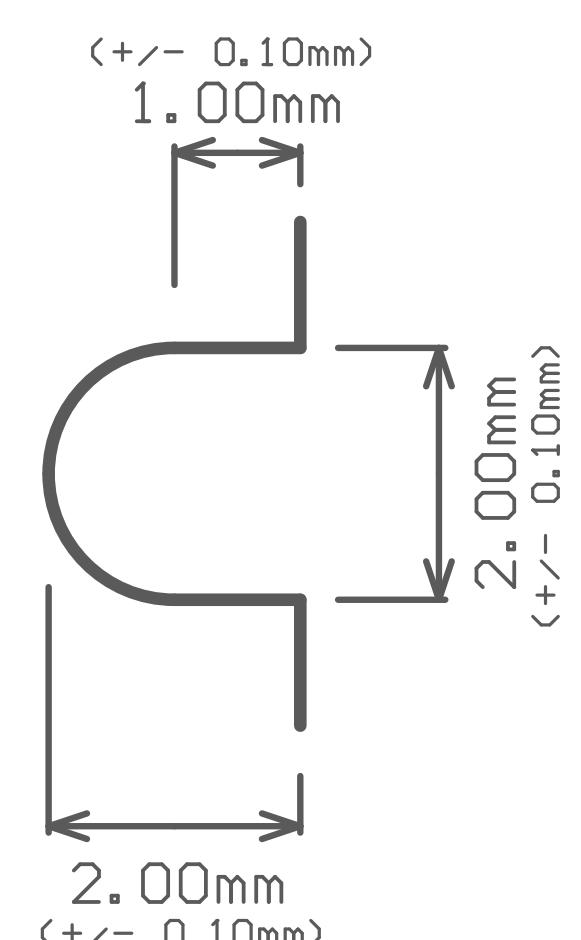
1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170$ C
2. Overall thickness is 1.0mm +/- 0.10mm
3. Board dimensions are 82 by 30mm with tolerances of +/- 0.15mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 - Internal layers (3, 4, 7, 8):
 - 40 Ohm: 6 mil tracks in artwork
 - 50 Ohm: 4.0 mil tracks in artwork
 - External Layers (1 and 10):
 - 40 Ohm: 9.5 mil tracks in artwork
 - 50 Ohm: 6.5 mil tracks in artwork
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup

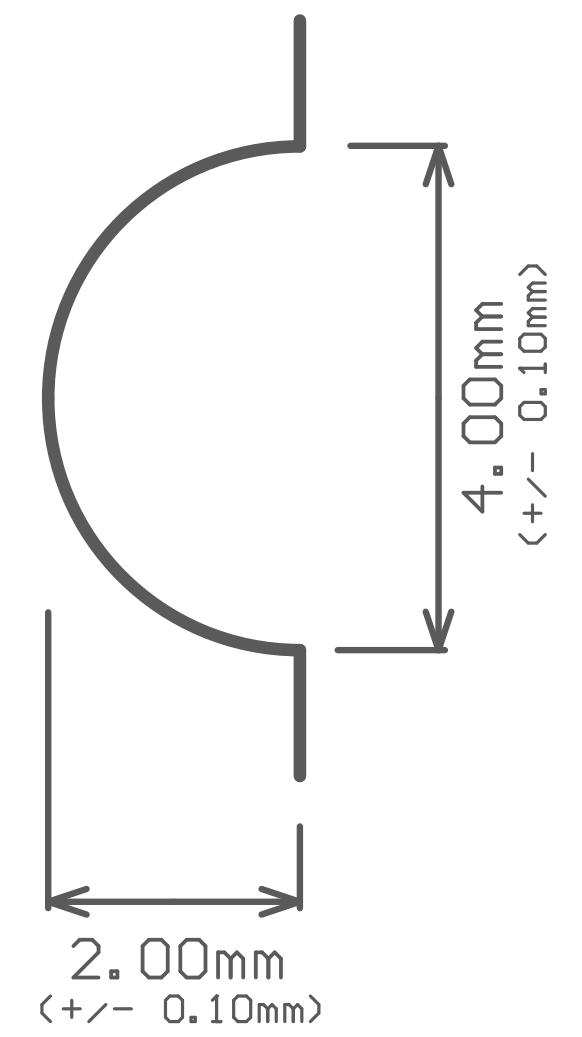
Univ. of Wisconsin—Madison
Madison, WI 53706ENGINEER:
Vicente, M.
PCB DESIGNER:
Vicente, M.TITLE:
ZYNQ-IPMCDATE:
06JUN2019
FILE NAME:
ZYNQ_IPMC.PCBDOCPART NO.:
DWG NO:
SCALE:REV:
revB1
1:1



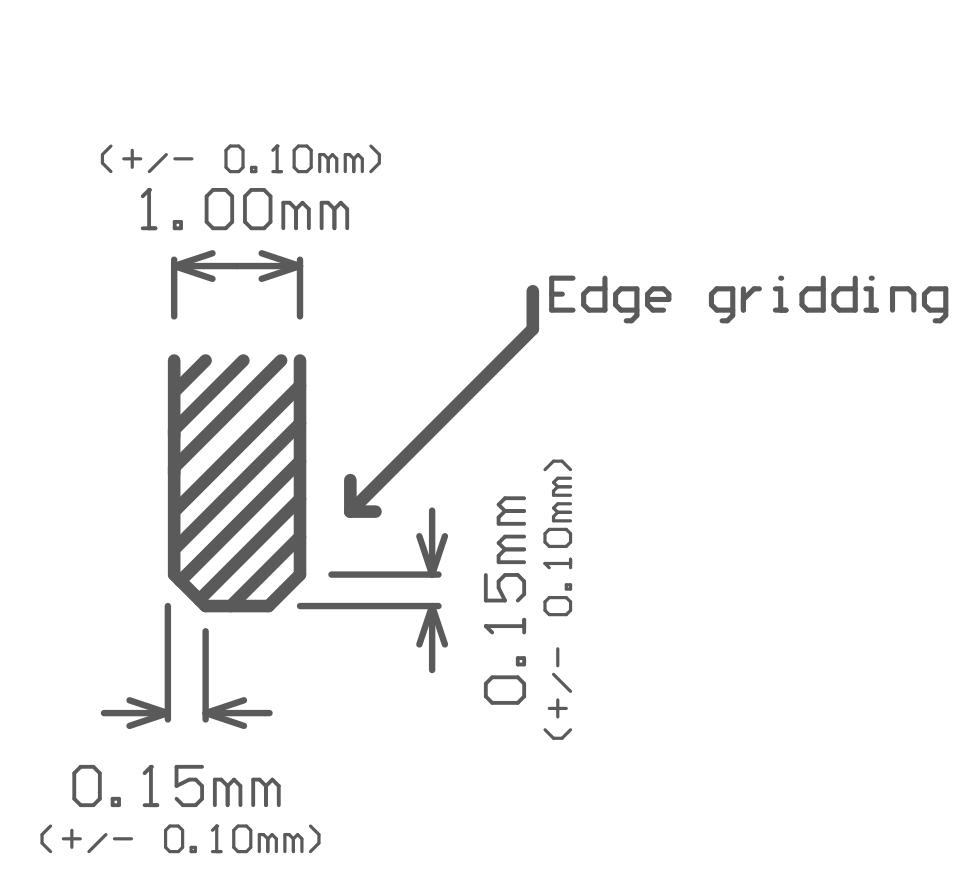
Detail 1



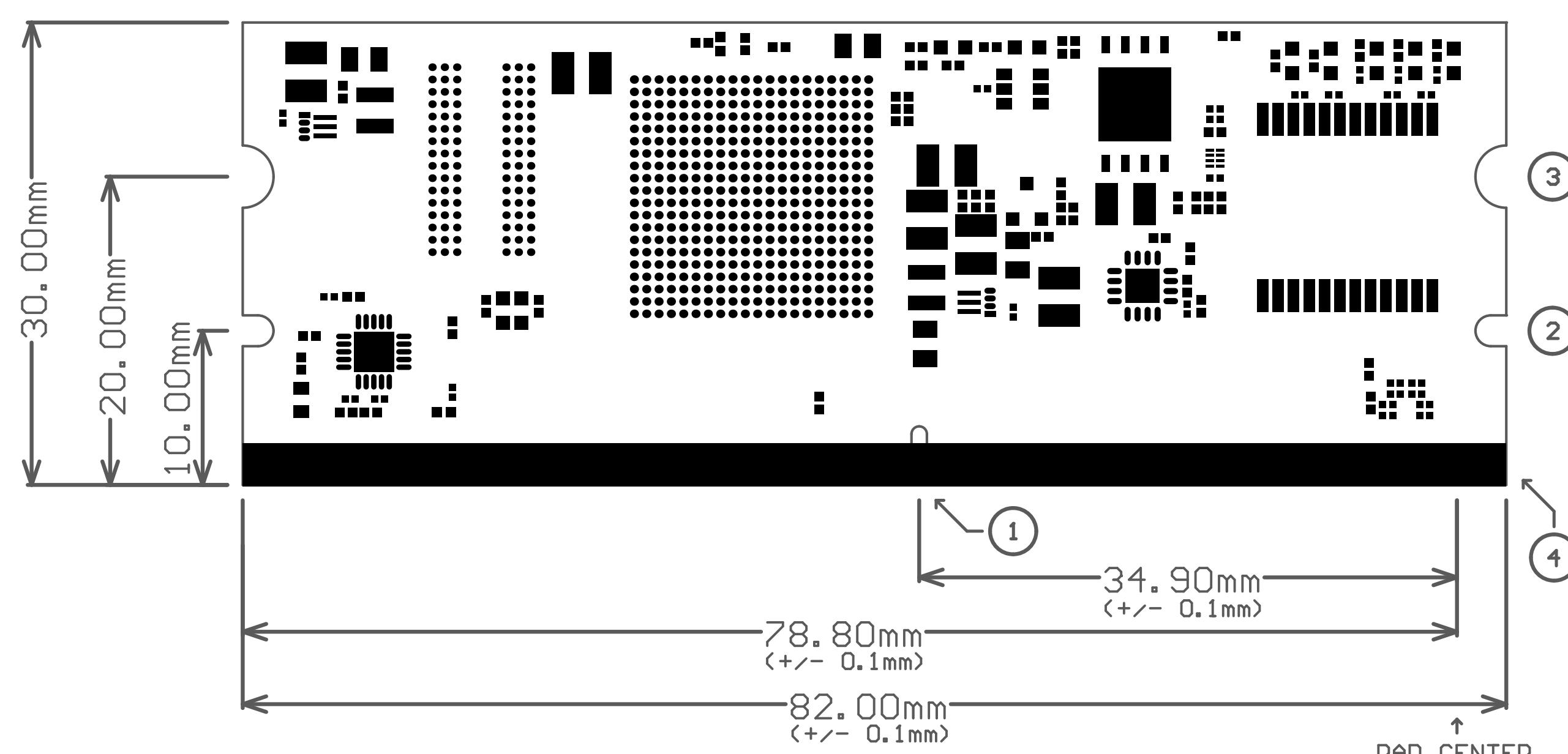
Detail 2



Detail 3

Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)



Top Solder (Mask)

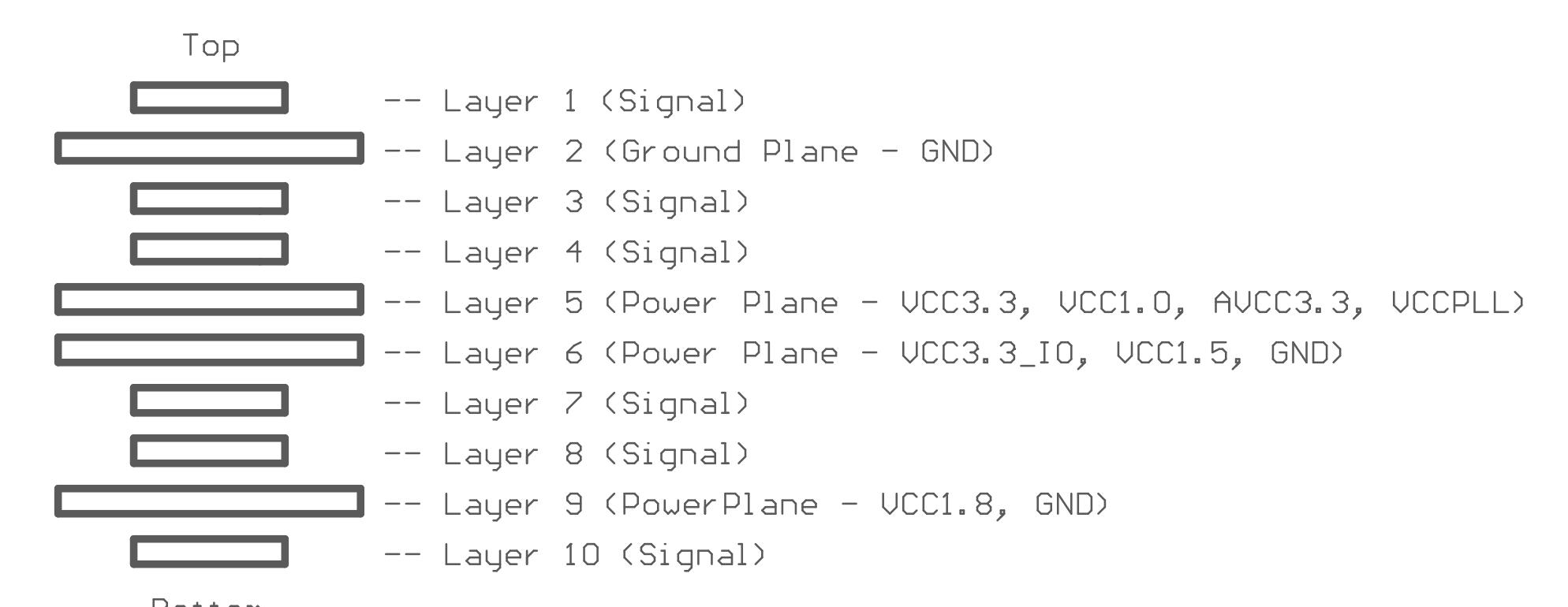
Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170$ C
2. Overall thickness is 1.0mm ± 0.10 mm
3. Board dimensions are 82 by 30mm with tolerances of ± 0.15 mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

Internal layers (3, 4, 7, 8):
40 Ohm: 6 mil tracks in artwork
50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):
40 Ohm: 9.5 mil tracks in artwork
50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating ± 3 mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup

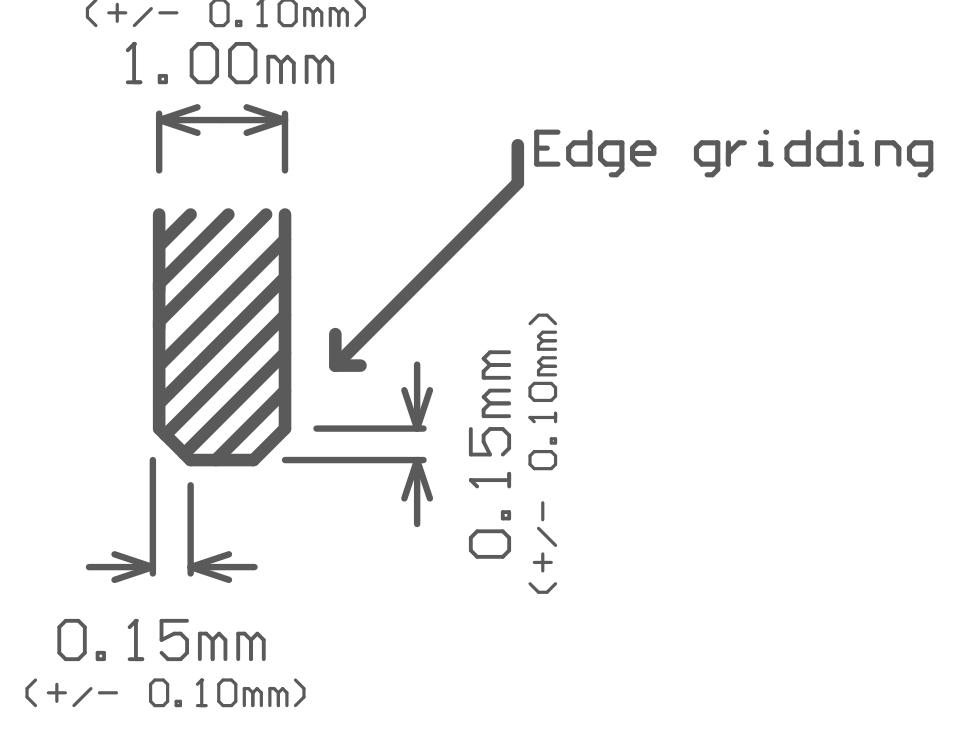
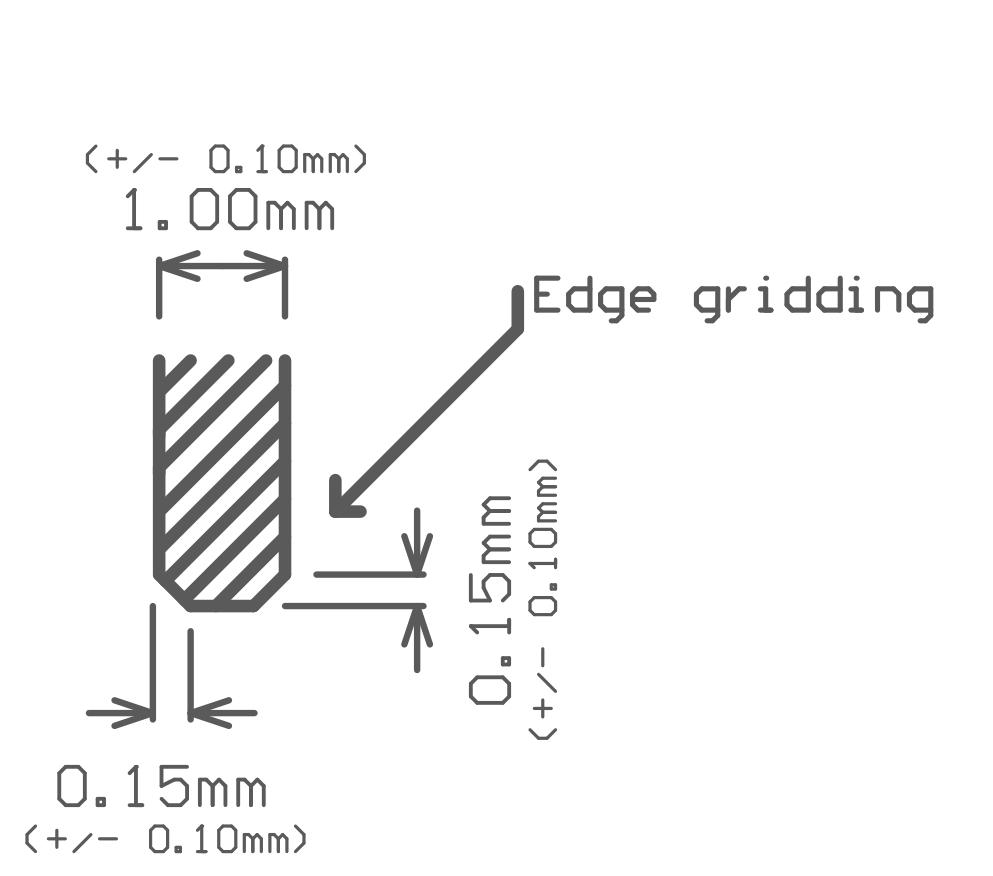
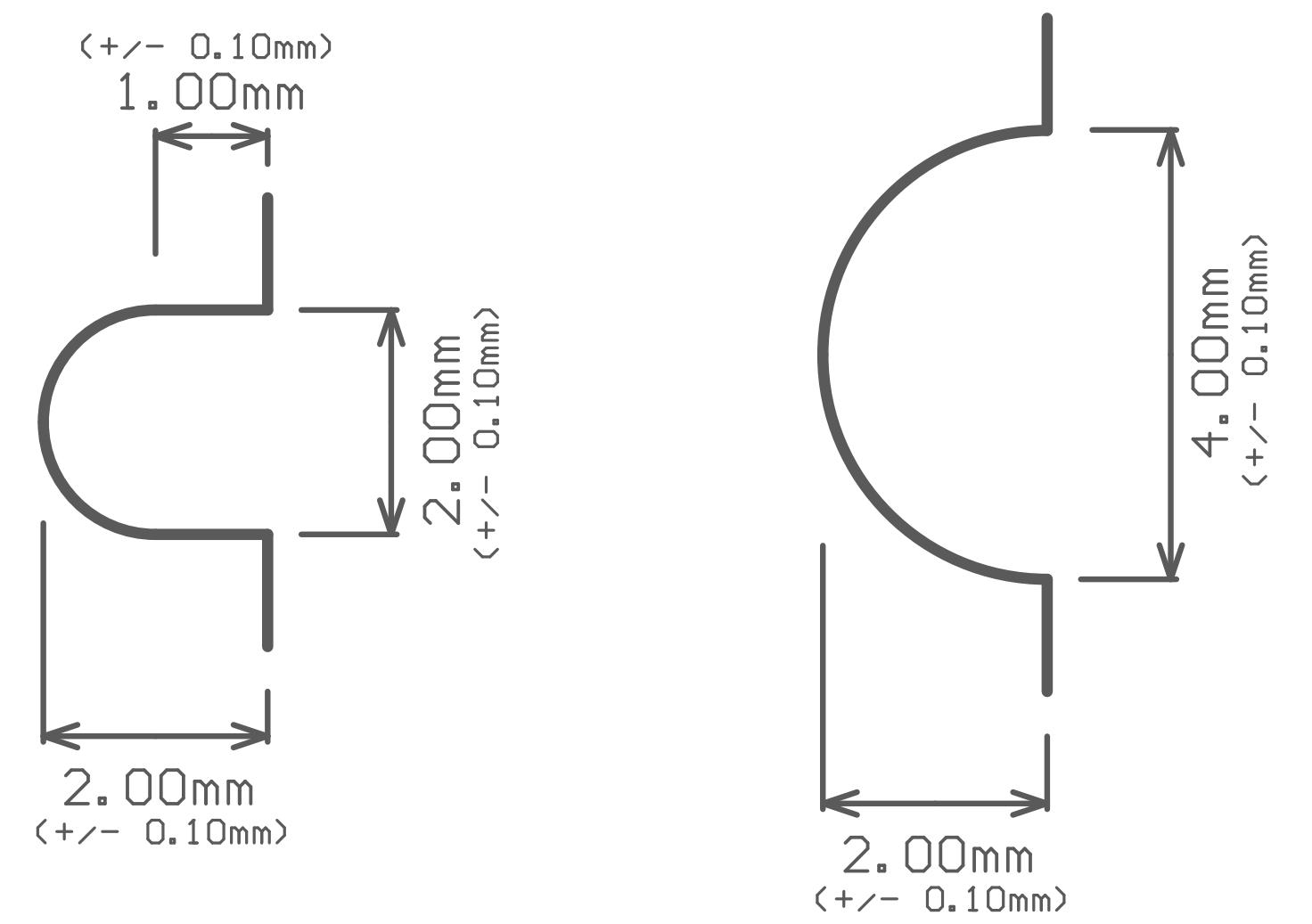
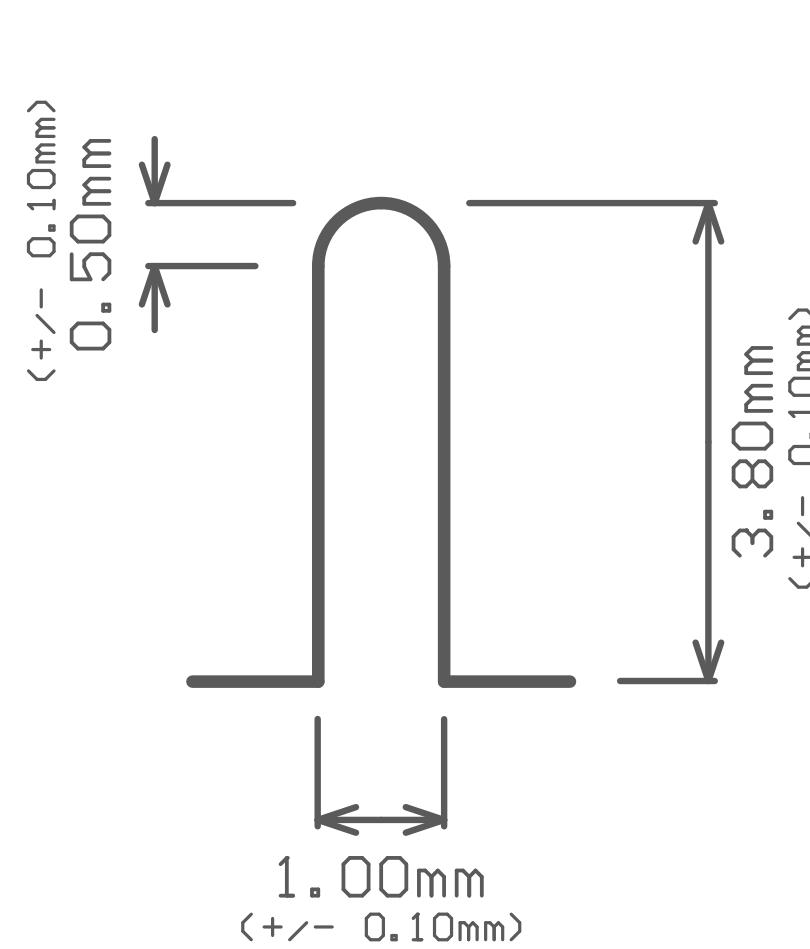
Univ. of Wisconsin—Madison
Madison, WI 53706ENGINEER:
Vicente, M.TITLE:
ZYNQ-IPMCPCB DESIGNER:
Vicente, M.DATE:
06JUN2019

PART NO.:

REV:
revB1FILE NAME:
ZYNQ_IPMC.PCBDOC

DWG NO.:

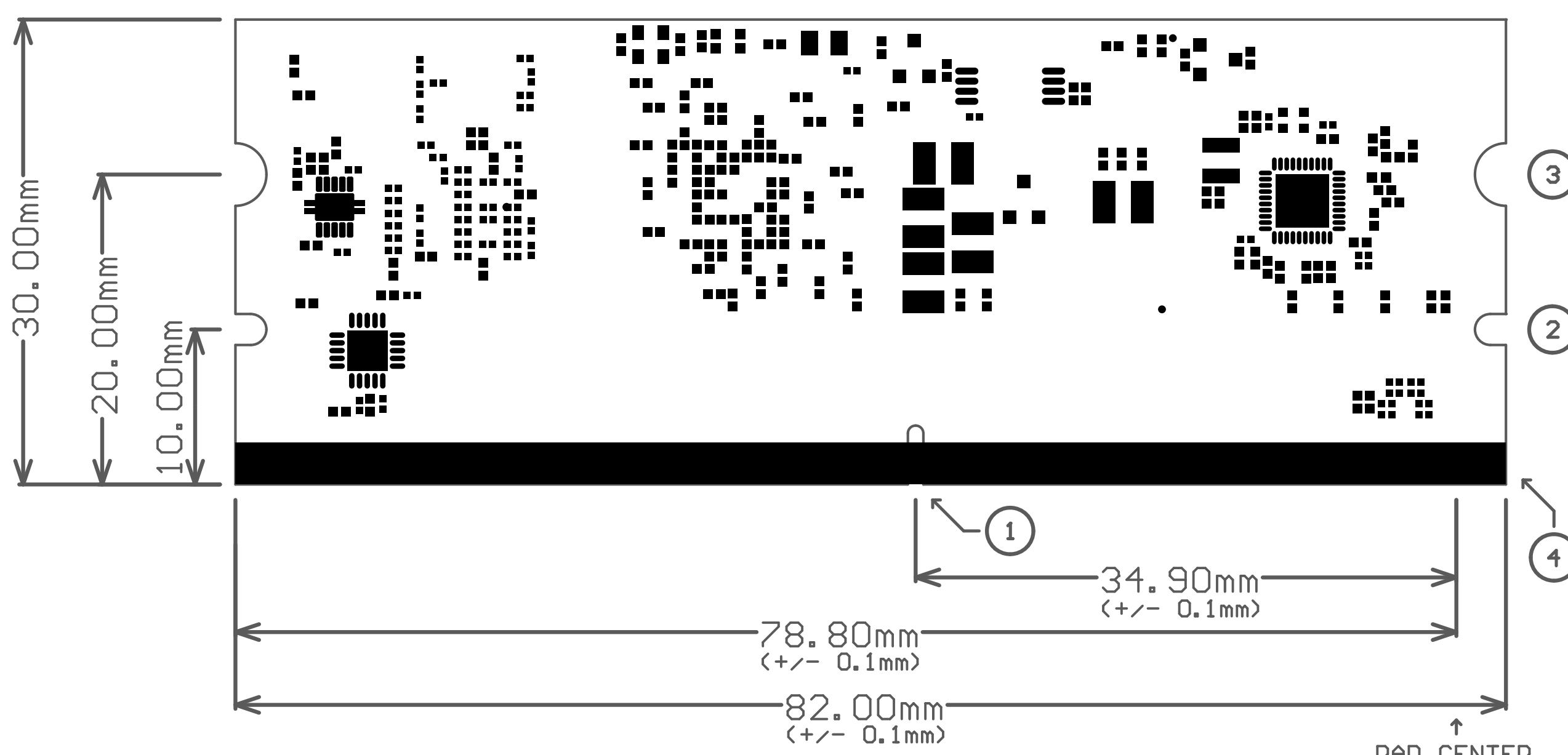
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Detail 1

Detail 2

Detail 3

Detail 4
(PCB side view)**UW-IPMC MEZZANINE (revB)**

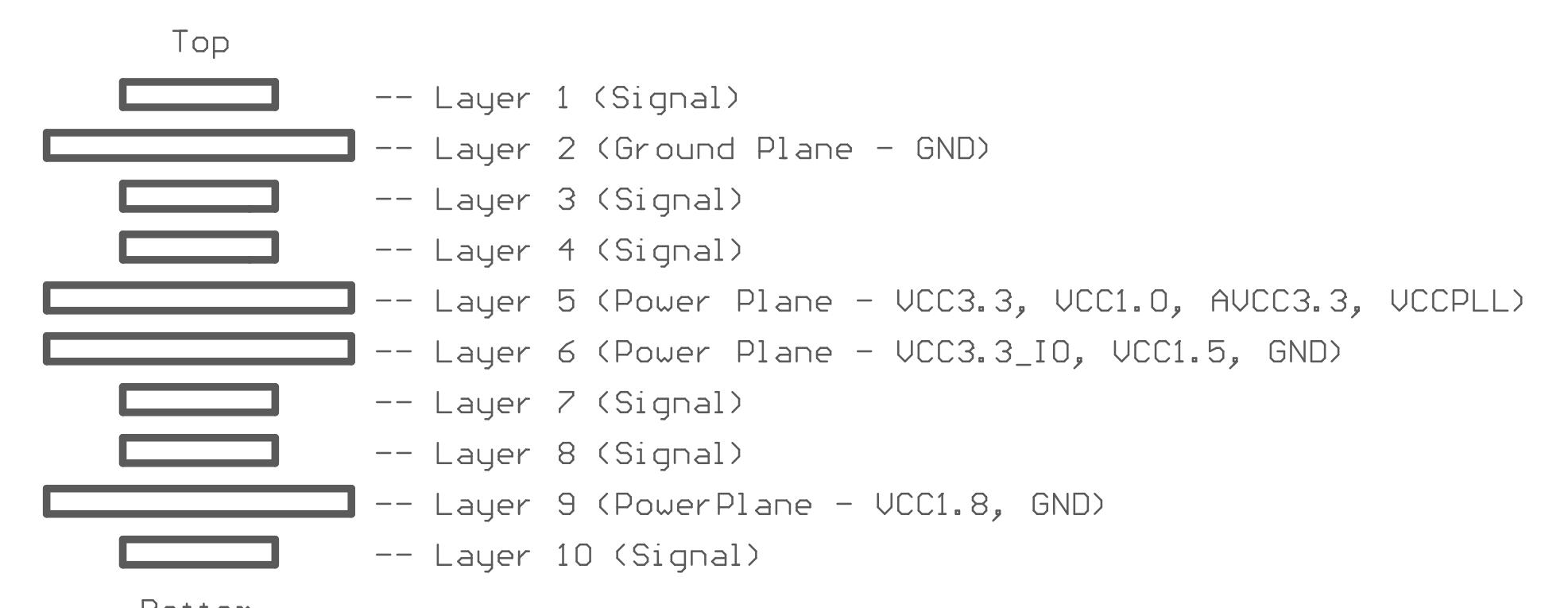
Bottom Solder (Mask)

Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm +/- 0.10mm
3. Board dimensions are 82 by 30mm with tolerances of +/- 0.15mm unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork
	50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork
	50 Ohm: 6.5 mil tracks in artwork

 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within +/- 10%. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating +/- 3mils, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
 - b. Overall board finish is immersion gold.
9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) +/- 10%. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

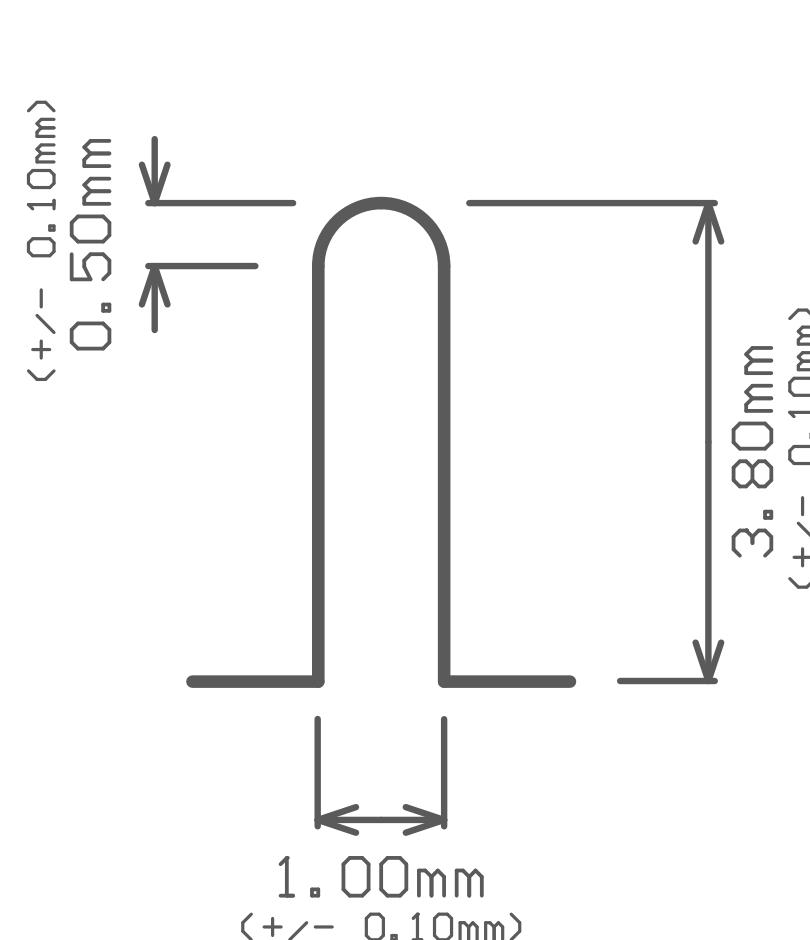
Layer StackupUniv. of Wisconsin—Madison
Madison, WI 53706ENGINEER:
Vicente, M.TITLE:
ZYNQ-IPMCPCB DESIGNER:
Vicente, M.DATE:
06JUN2019

PART NO.:

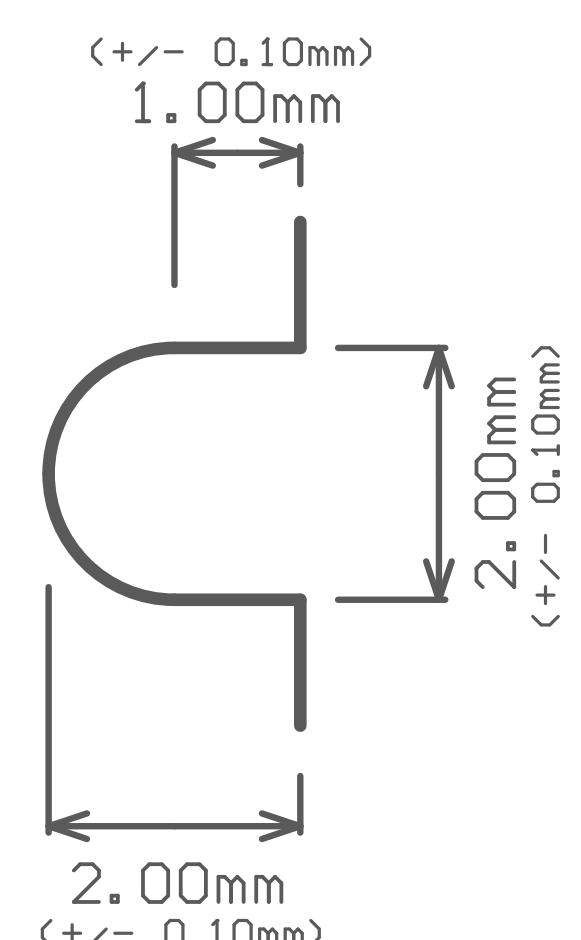
REV:
revB1FILE NAME:
ZYNQ_IPMC.PCBDOC

DWG NO.:

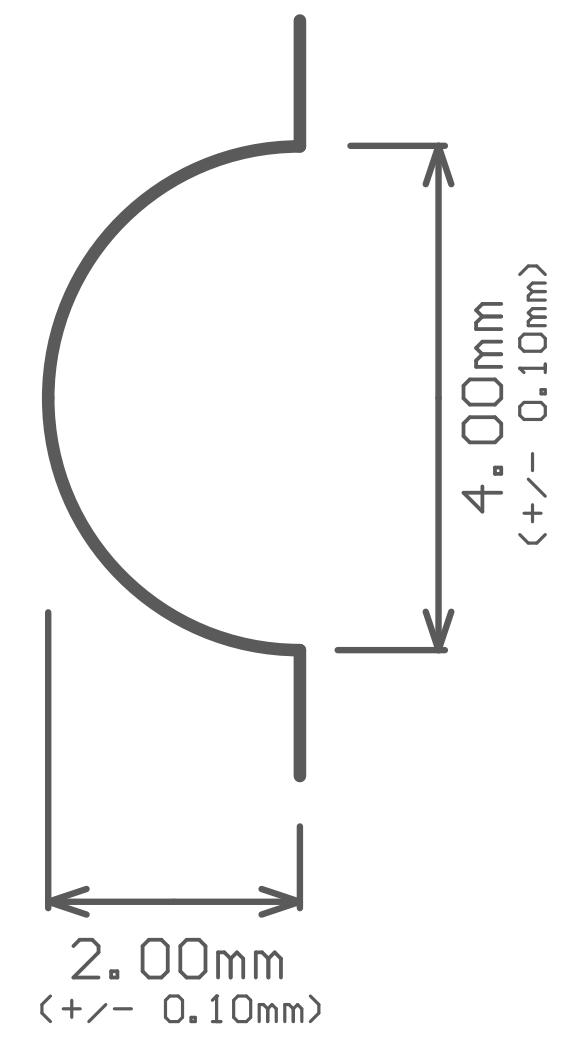
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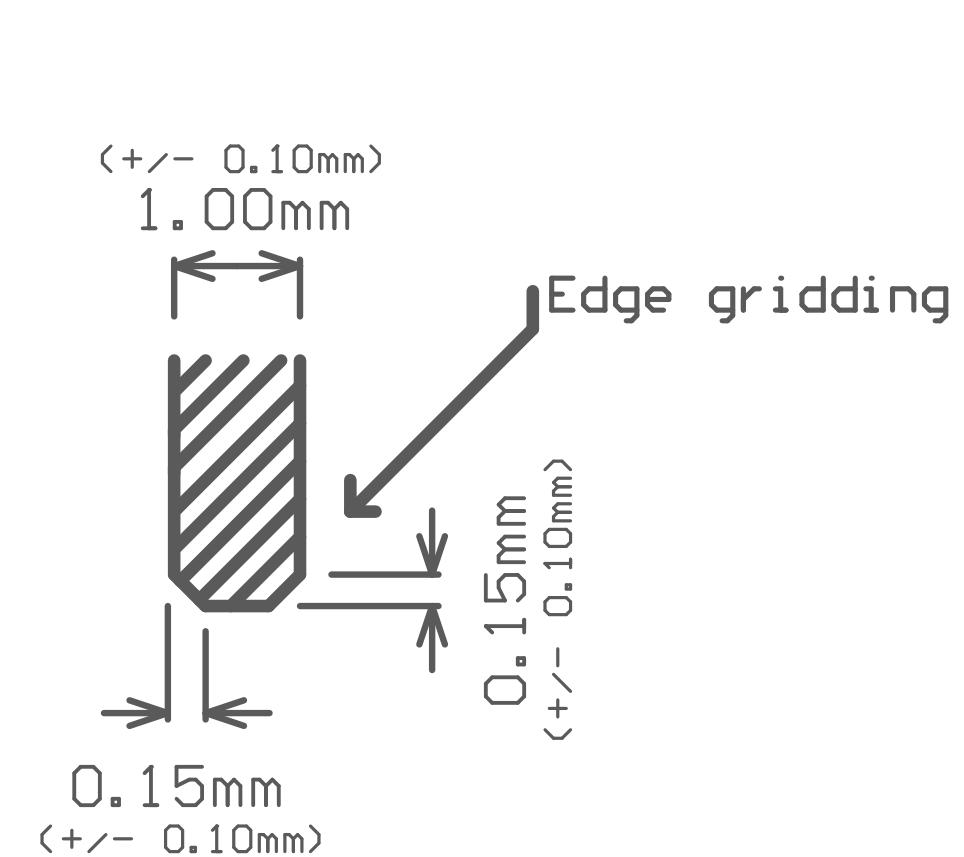
Detail 1



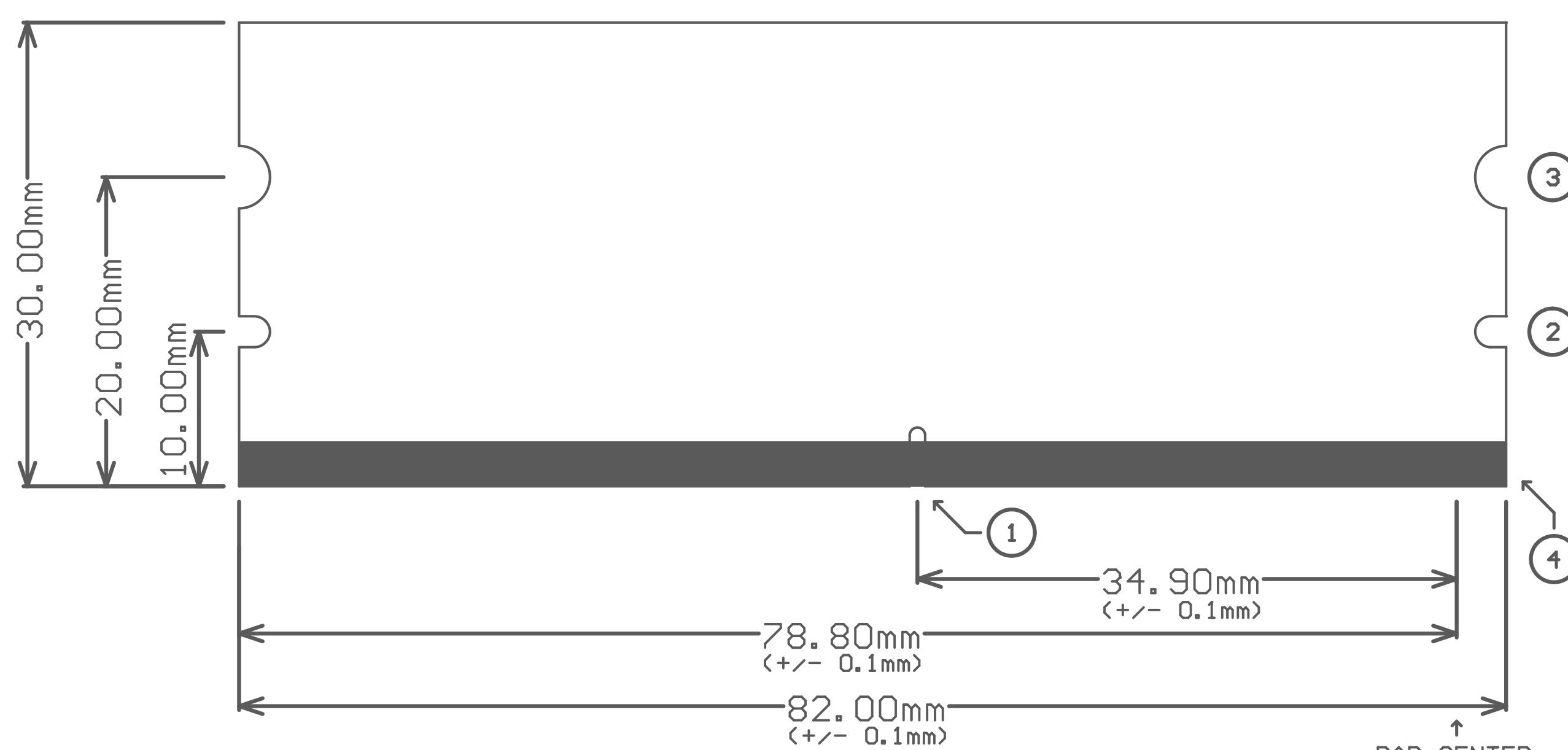
Detail 2



Detail 3

Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)



Top Hard Gold (Mask)

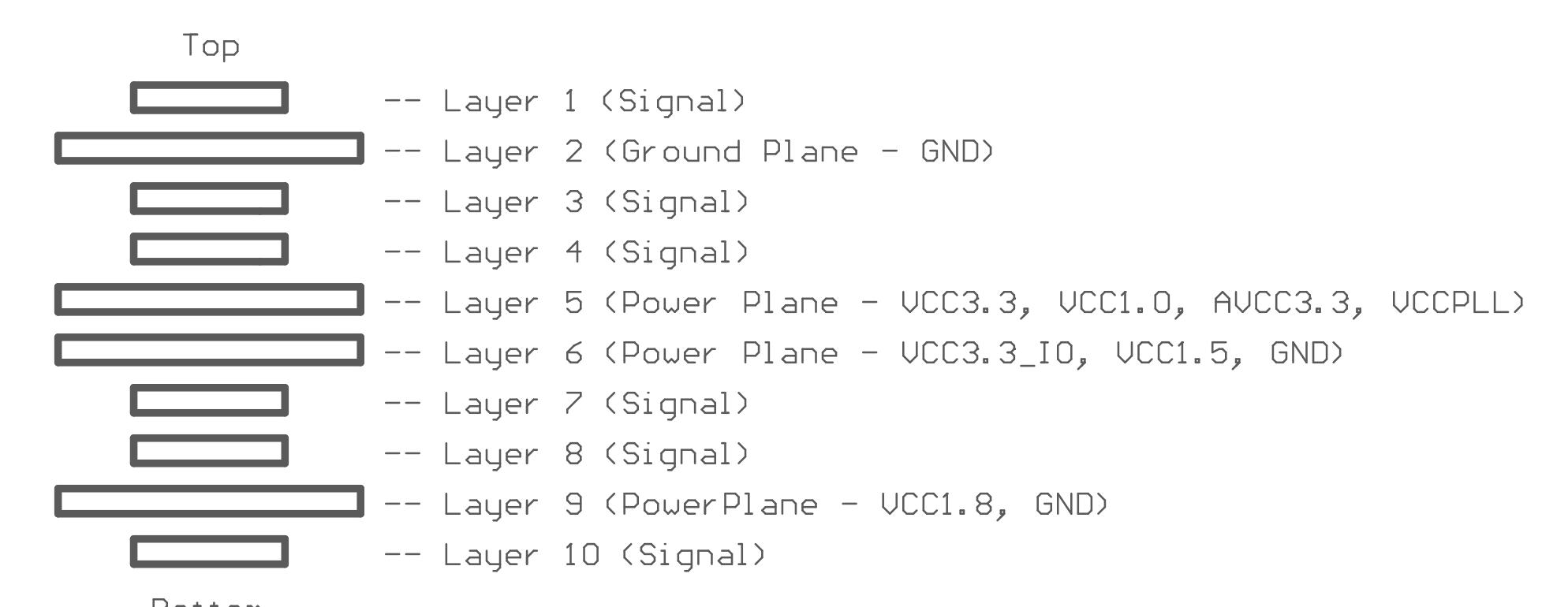
Specifications:

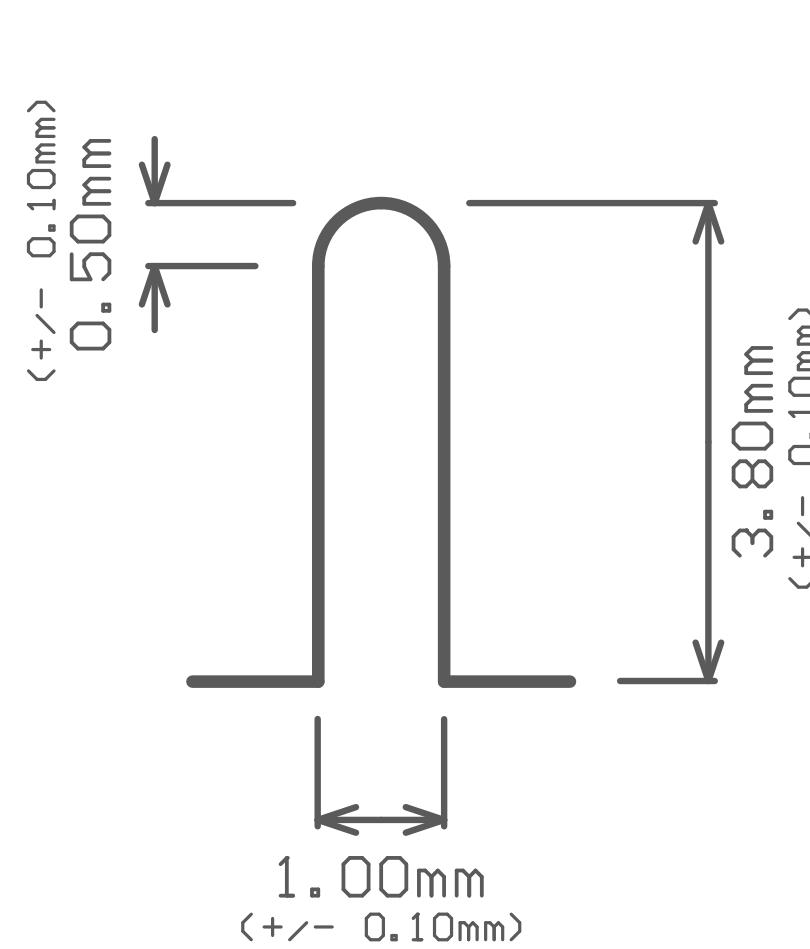
1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:

Internal layers (3, 4, 7, 8):	40 Ohm: 6 mil tracks in artwork 50 Ohm: 4.0 mil tracks in artwork
External Layers (1 and 10):	40 Ohm: 9.5 mil tracks in artwork 50 Ohm: 6.5 mil tracks in artwork

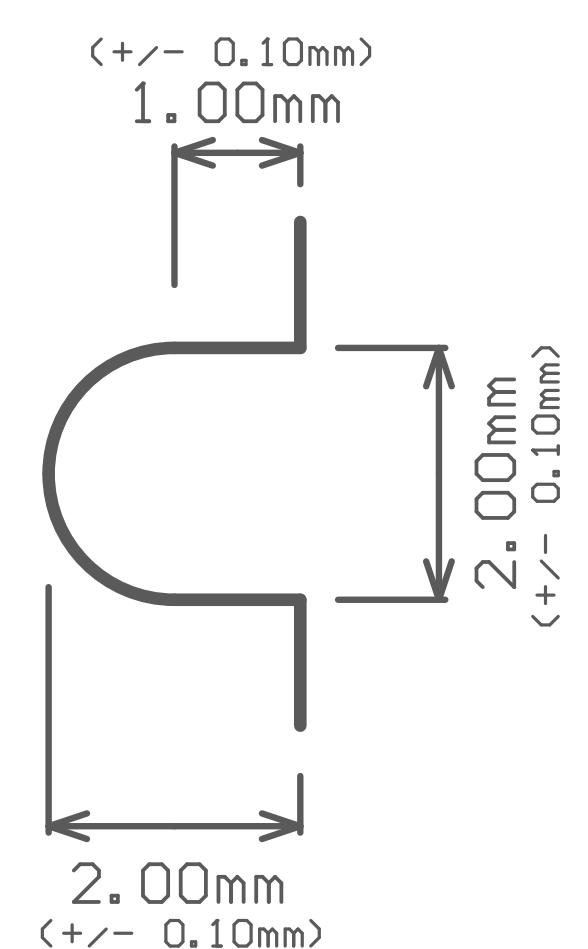
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
 - c. All plated through holes must be plated over to facilitate assembly as a via-in-pad design
 - d. Drills are plated-through holes and their locations are given in a separate drill file.
8. Finish:
 - a. Board contains a hard gold finish area on the south edge of the top and bottom surface. Area to receive hard gold finish is identified in two separate photoplot layers. Area gold finish is minimum 0.75 microns gold over minimum 2.54 microns nickel.
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9. Minimum observed signal layer clearances is 4 mils (layers 1, 3, 4, 7, 8 and 10)
10. Red colored solder mask shall be applied to both top and bottom surfaces. Mask shall be photoimagable, with maximum thickness of 3 mils
11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
12. Silkscreen to be applied to both top and bottom sides. Silkscreen shall be white ink
13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
 - c. Resistance between planes and non-connected plated through holes and vias shall be 10 Megaohms or larger
 - d. Impedance of all signal layers shall be checked with TDR. Finish impedance shall be to the nominal value (40 or 50 ohm) $\pm 10\%$. Vendor shall provide appropriate coupons for testing. Testing report to be enclosed with the quality control documentation shipped with the boards.
17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup

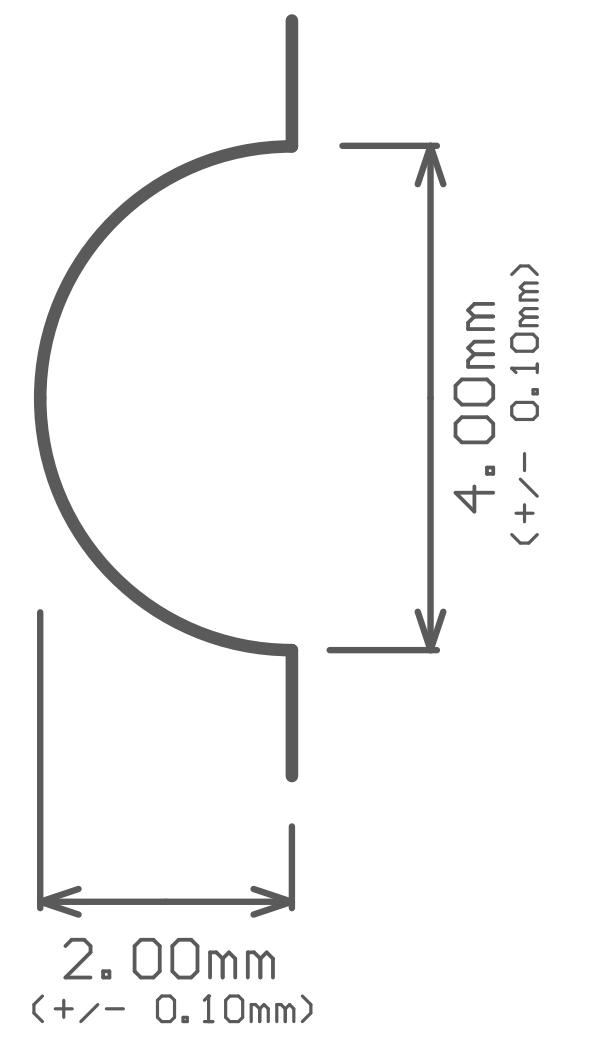
Univ. of Wisconsin—Madison
Madison, WI 53706ENGINEER:
Vicente, M.
PCB DESIGNER:
Vicente, M.TITLE:
ZYNQ-IPMCDATE:
06JUN2019
FILE NAME:
ZYNQ_IPMC.PCBDOCPART NO.:
DWG NO:REV:
revB1
SCALE:
1:1



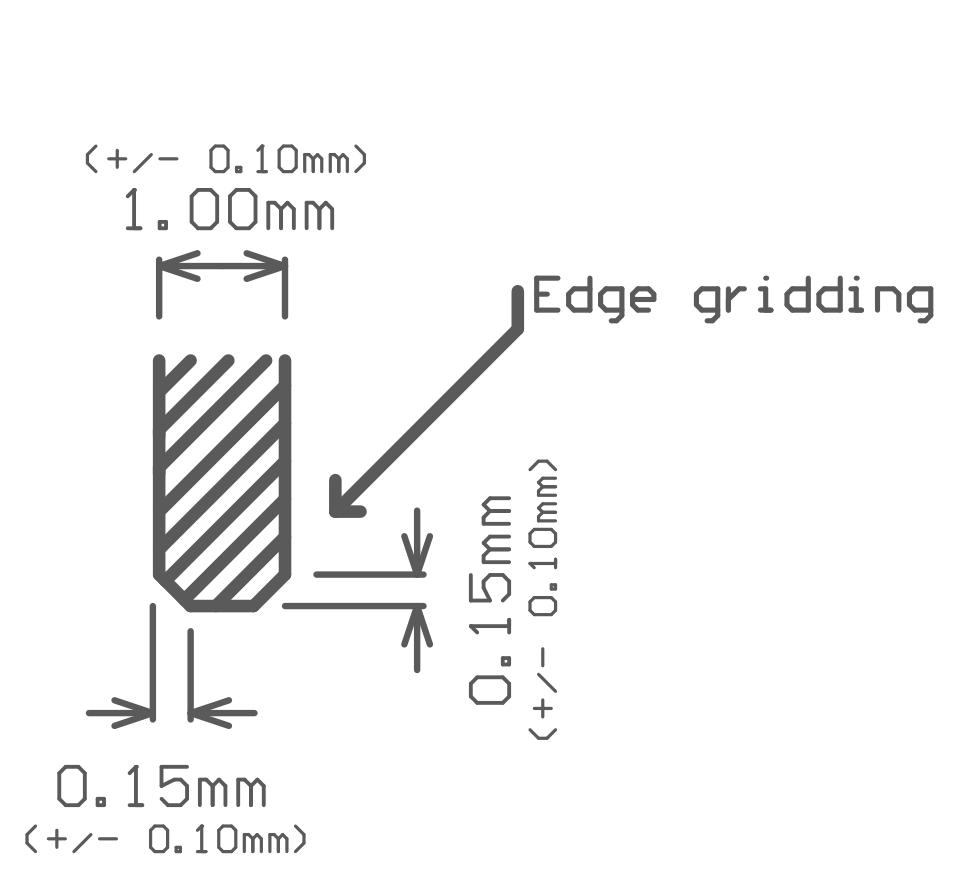
Detail 1



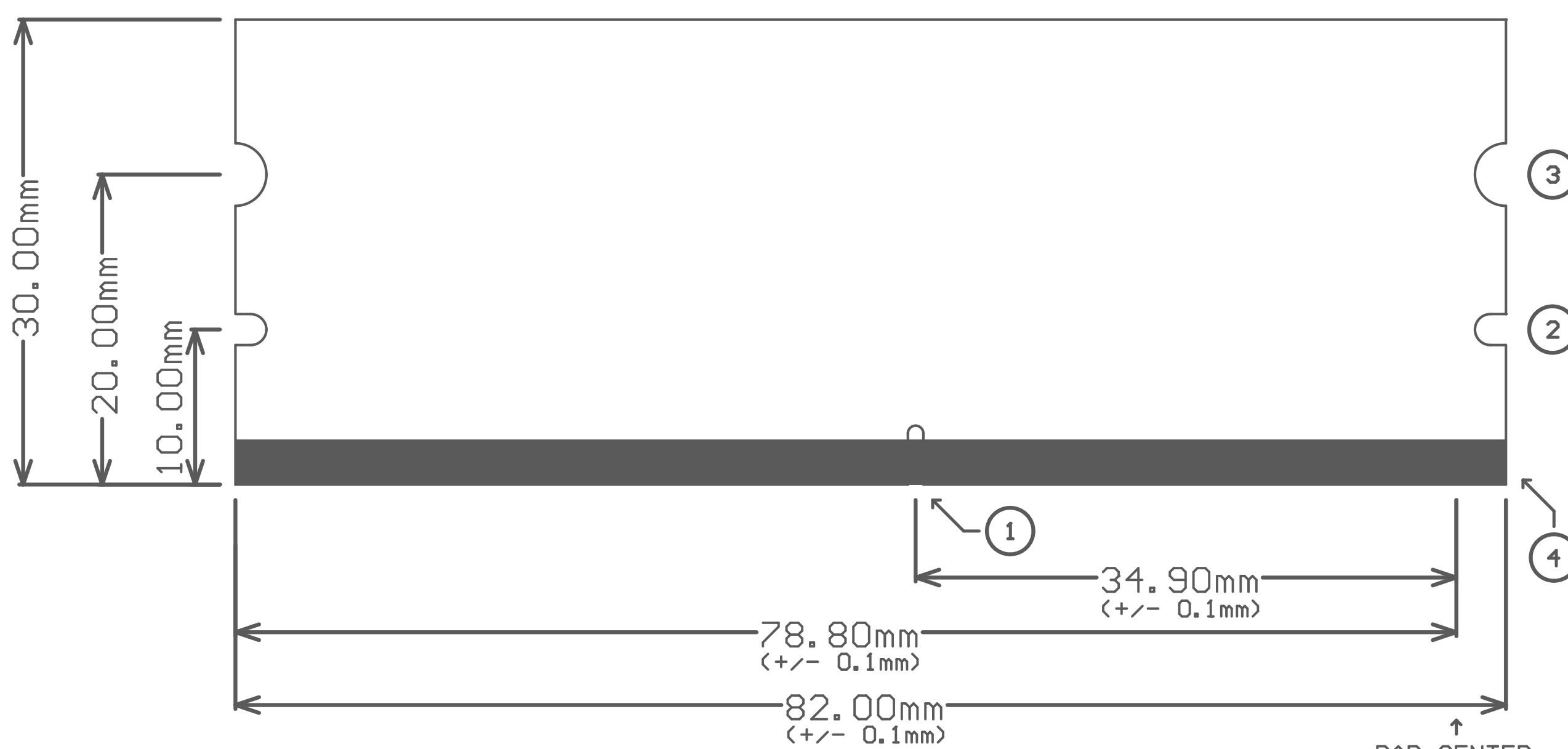
Detail 2



Detail 3

Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)

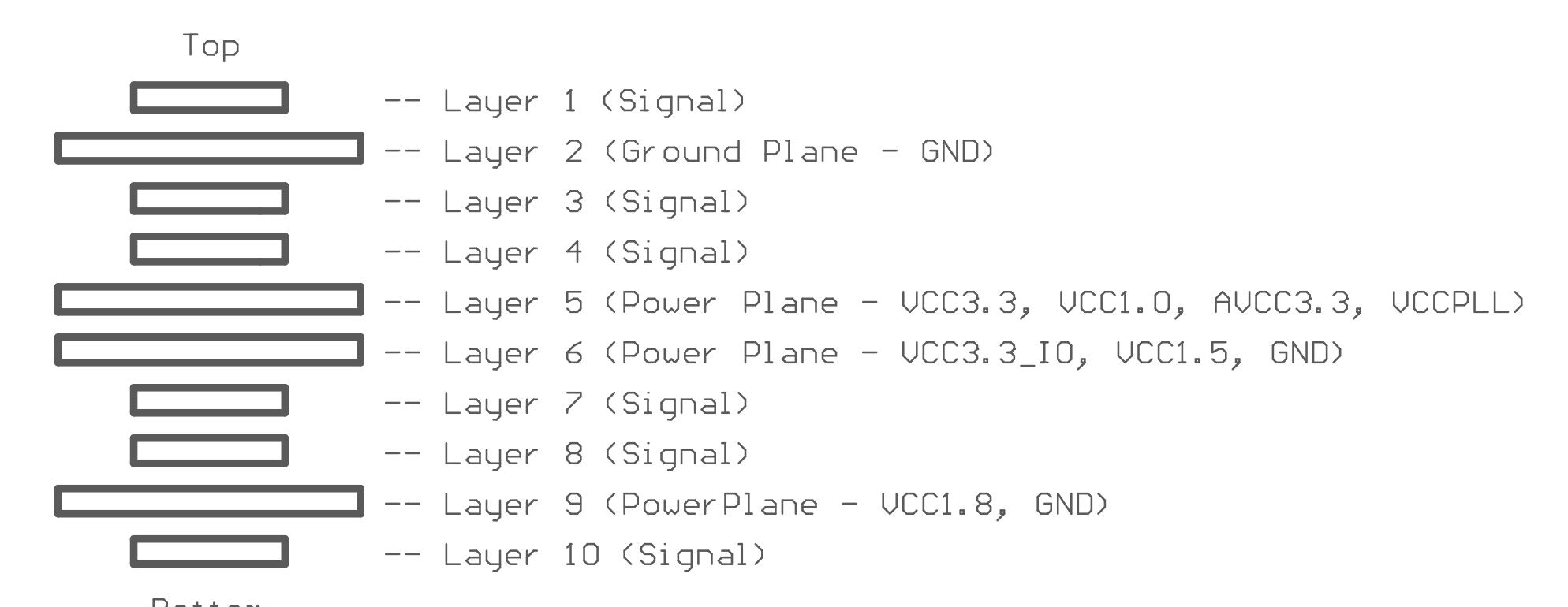


Bottom Hard Gold (Mask)

Specifications:

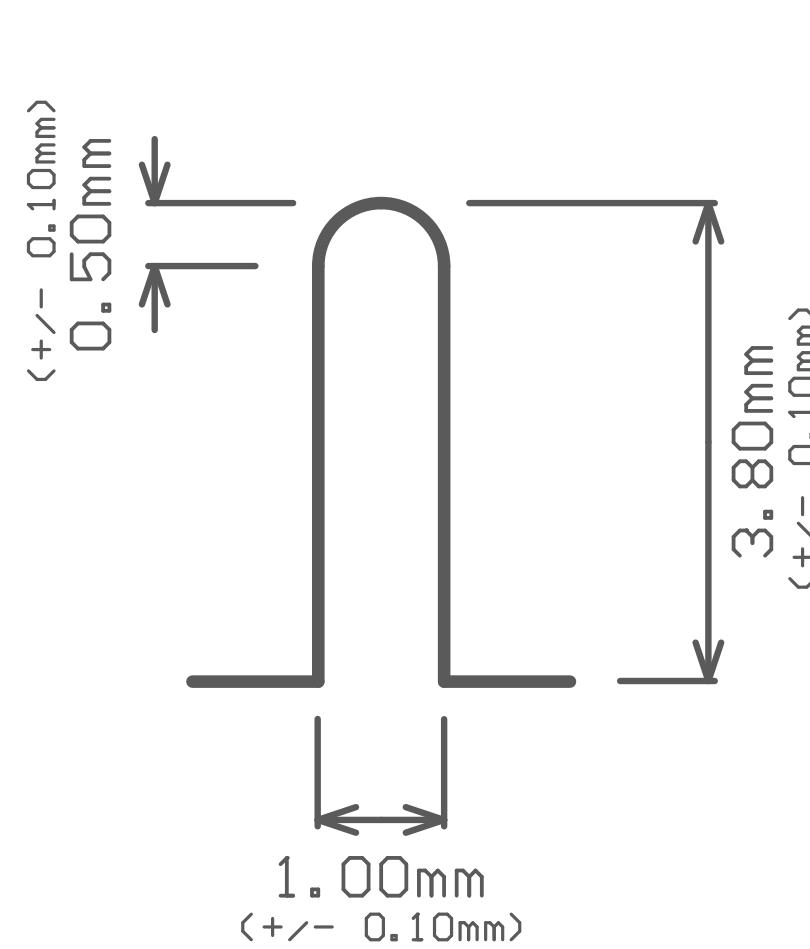
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2. Overall thickness is 1.0mm $\pm 0.10\text{mm}$
3. Board dimensions are 82 by 30mm with tolerances of $\pm 0.15\text{mm}$ unless specified in drawing.
4. Panelization
 - a. Cards should be left in panels (at least 3 sides) for breakout after solder reflow
 - b. Panels should contain fiducial marks for X,Y alignment
5. Controlled impedance: 40 and 50 ohm single-ended traces on internal/external layers as follows:
 - Internal layers (3, 4, 7, 8):
 - 40 Ohm: 6 mil tracks in artwork
 - 50 Ohm: 4.0 mil tracks in artwork
 - External Layers (1 and 10):
 - 40 Ohm: 9.5 mil tracks in artwork
 - 50 Ohm: 6.5 mil tracks in artwork
 Width of above-listed track/layer combinations may be adjusted by vendor to obtain desired impedance within $\pm 10\%$. All other track widths in the artwork are given as before-etching.
6. All layers use 1/2 oz. copper (before plating)
7. Holes:
 - a. Hole diameters are given as after plating $\pm 3\text{mils}$, except as noted on drill drawing
 - b. Drill files are in Excellon Format, 2.4 Absolute Inches, with leading zeros suppressed
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11. Layers 2, 5, 6 and 9 are power planes and are INVERTED
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13. Board shall be manufactured in accordance with IPC-6011 and IPC-6012 (class 2)
14. Combination of bow and twist shall not exceed 10 mils/inch along any direction
15. Design origin is at the bottom-left corner of the PCB
16. Testing:
 - a. All layers to undergo optical inspection (machine-based) of all layers before lamination
 - b. Boards will receive a full electrical test based on Gerber and IPC-D-356A data. DC resistance shall be 10 ohms or less
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17. Locations in IPC-D-356A file are given in 2.4 English units
18. South edge-to-edge connector details:
 - a. Details present in page 2 of the Molex 87783-0301 datasheet (included).

Layer Stackup

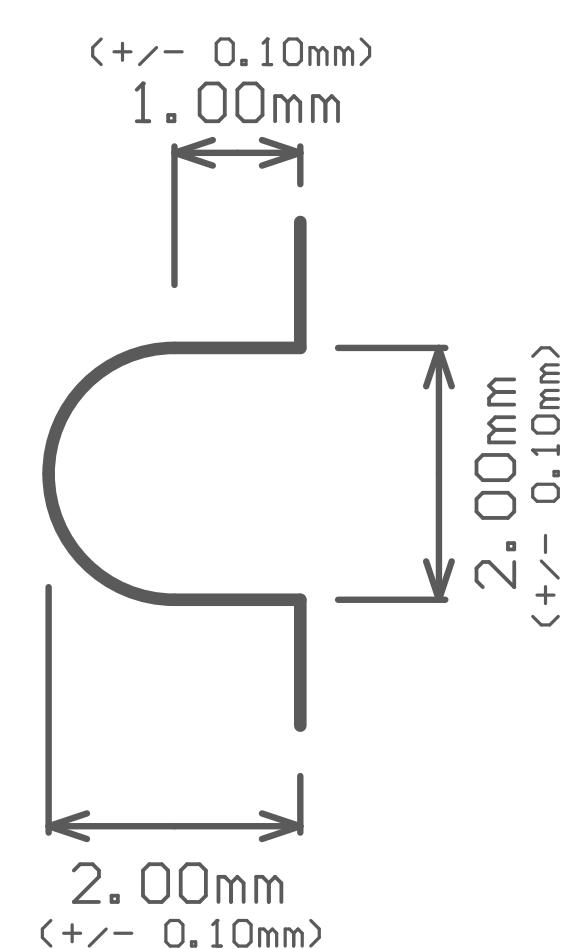
Univ. of Wisconsin—Madison
Madison, WI 53706ENGINEER:
Vicente, M.TITLE:
ZYNQ-IPMCPCB DESIGNER:
Vicente, M.DATE:
06JUN2019
FILE NAME:
ZYNQ_IPMC.PCBDOC

PART NO.:

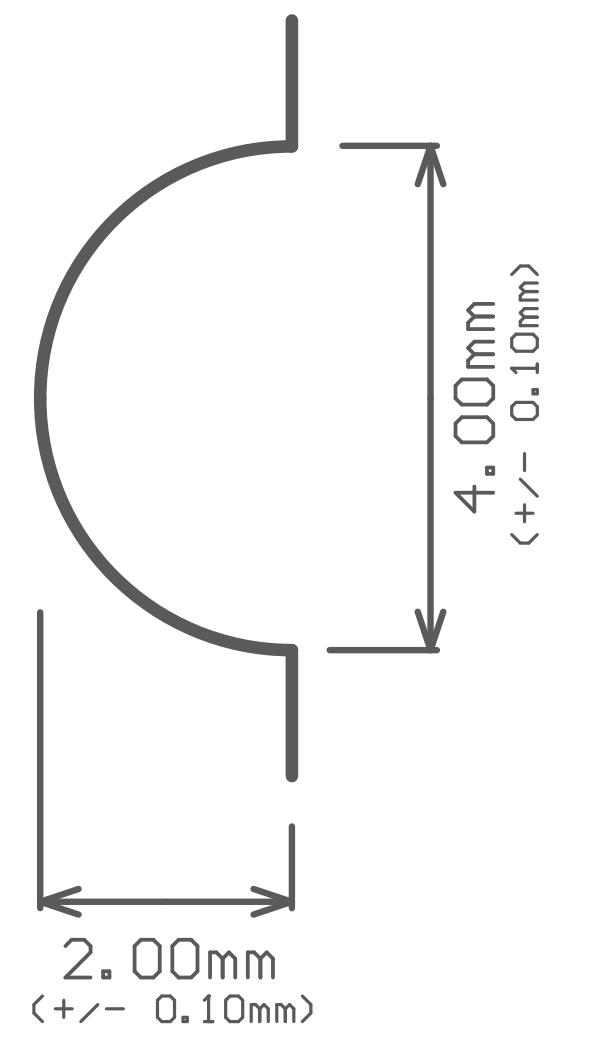
REV:
revB1
SCALE:
1:1



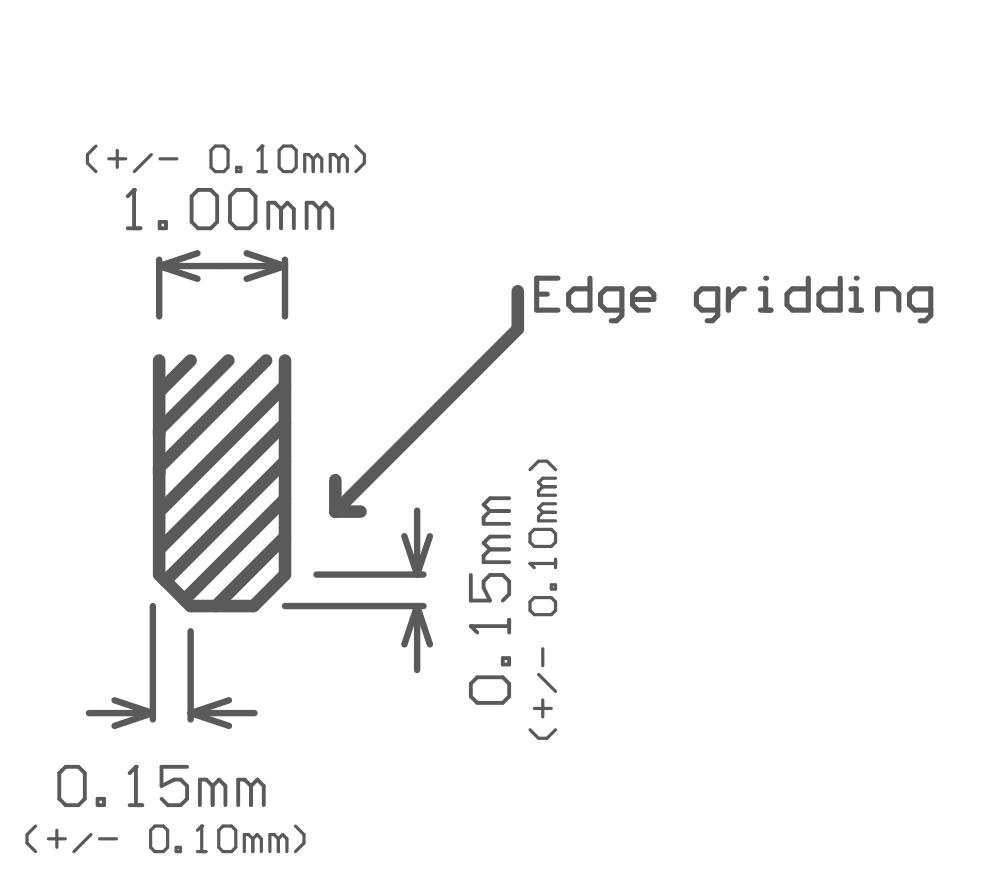
Detail 1



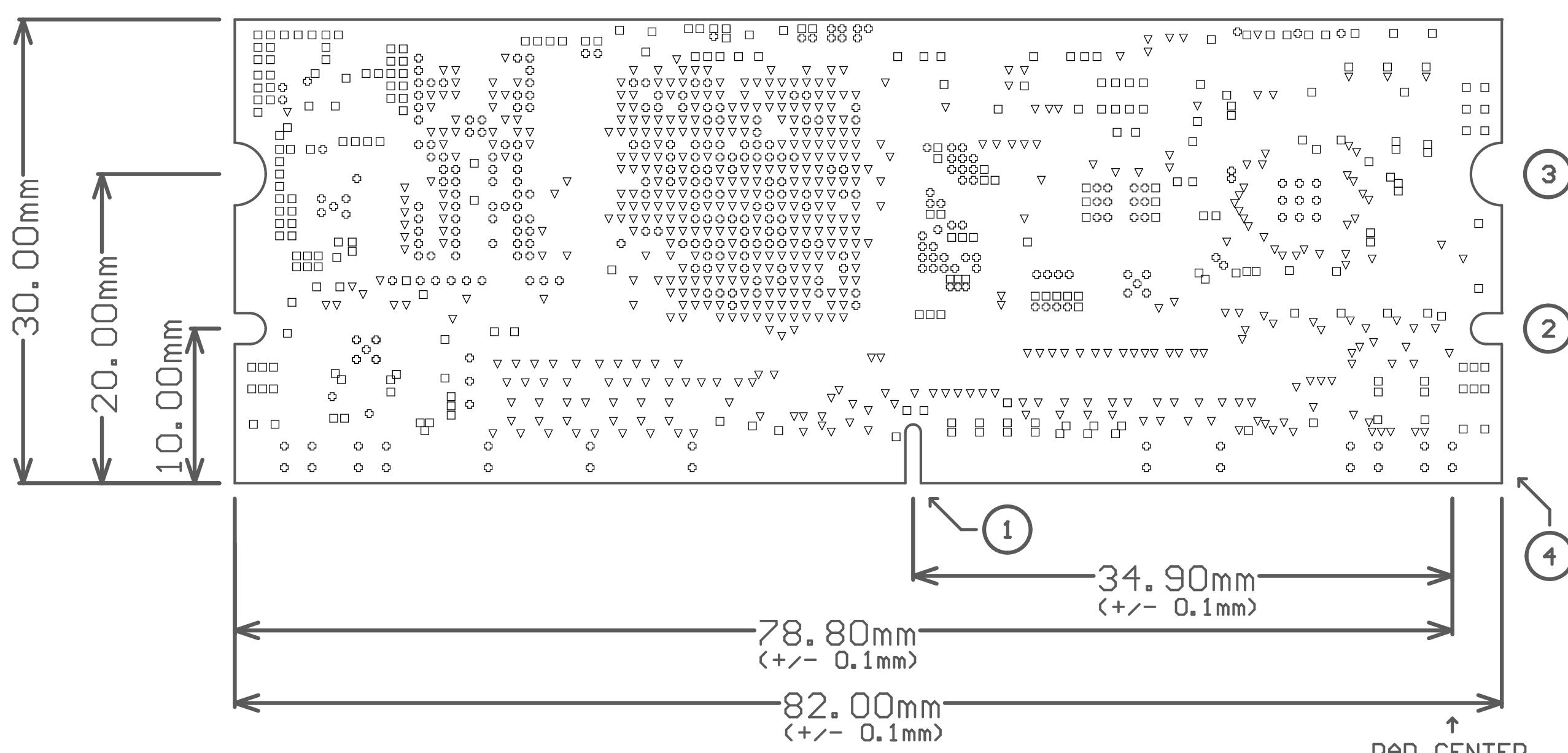
Detail 2



Detail 3

Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)



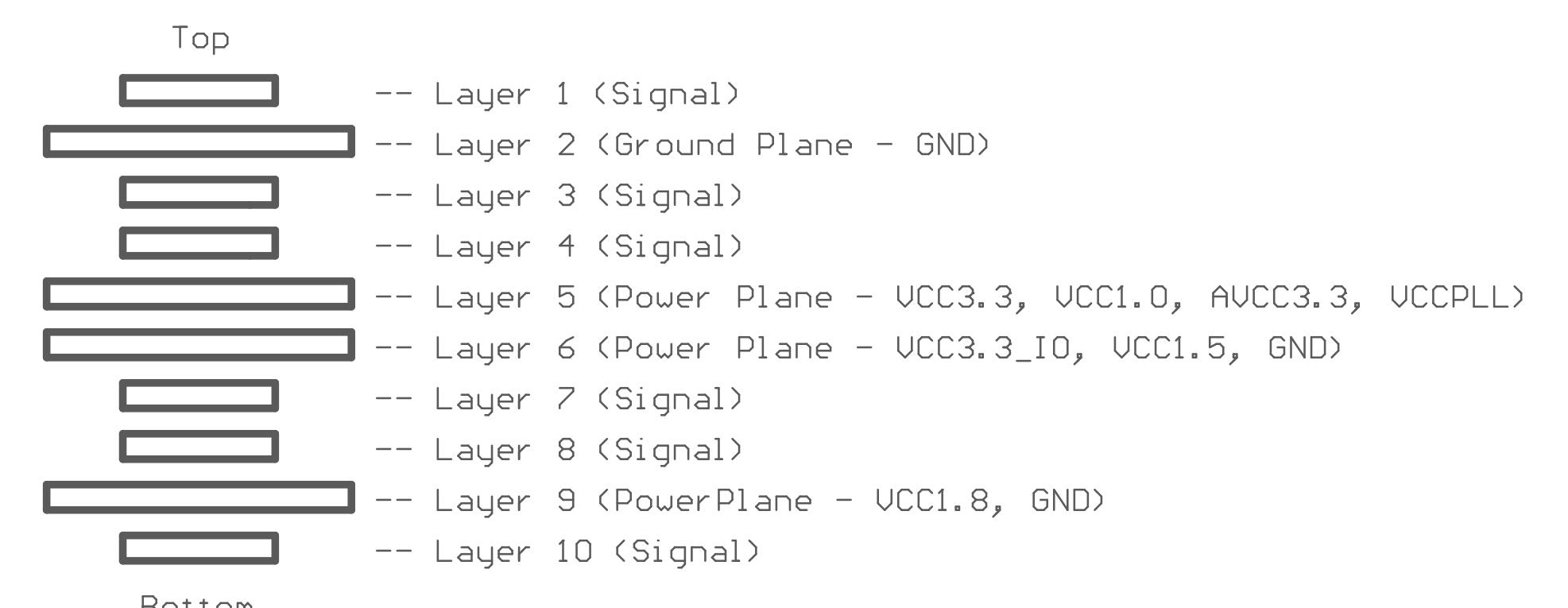
Drill Guide

Symbol	Hit Count	Finished Hole Size	Plated	Hole Type	Physical Length	Rout Path Length
□	268	8.00mil (0.203mm)	PTH	Round	-	-
⊕	315	7.00mil (0.178mm)	PTH	Round	-	-
▽	530	6.00mil (0.152mm)	PTH	Round	-	-
1113 Total						

Specifications:

1. Dielectric material is Tetrafunctional FR-4 with $T_g > 170^{\circ}\text{C}$
2. Overall thickness is 1.0mm +/- 0.10mm
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Layer Stackup

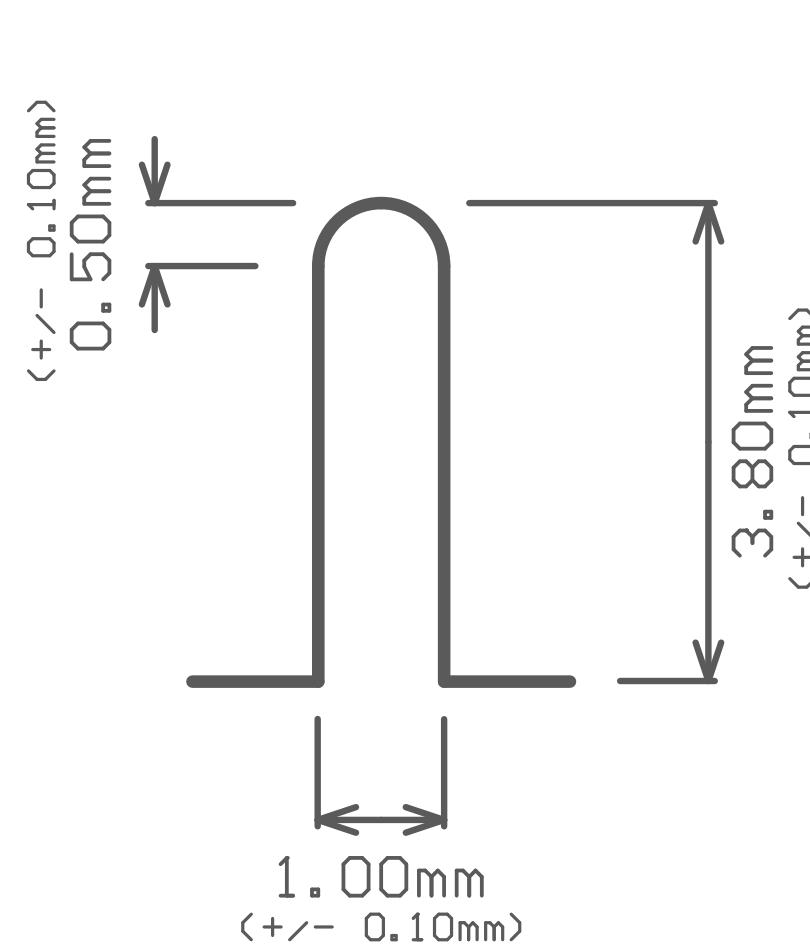
Univ. of Wisconsin—Madison
Madison, WI 53706ENGINEER:
Vicente, M.TITLE:
ZYNQ-IPMCPCB DESIGNER:
Vicente, M.

PART NO.:

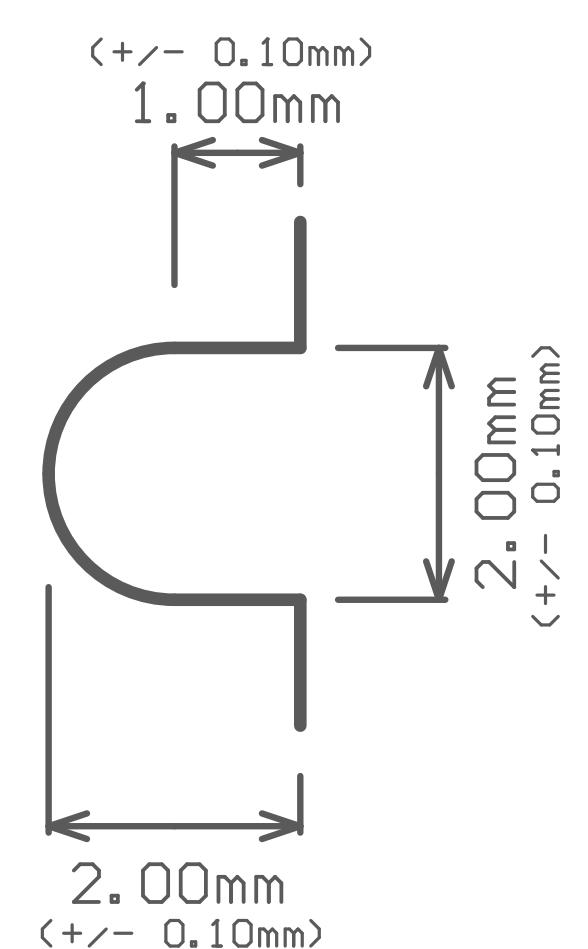
REV:
revB1DATE:
06JUN2019FILE NAME:
ZYNQ_IPMC.PCBDOCSCALE:
1:1

Board Stack Report

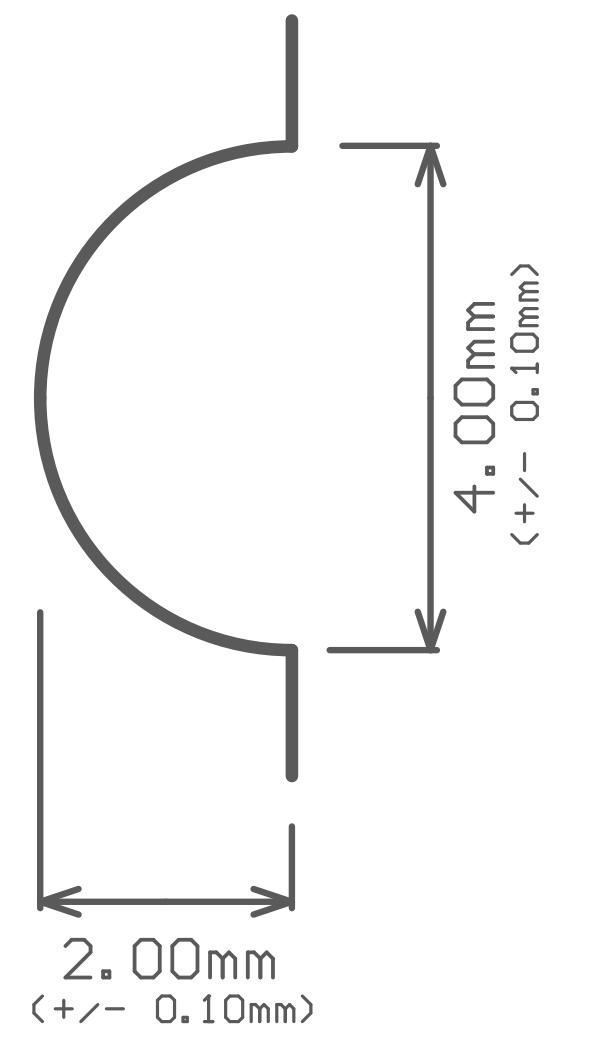
Stack Up		Layer Stack					
Layer	Board Layer Stack	Board Layer Stack	Name	Material	Thickness	Constant	
1			Top Paste				
2			Top Overlay				
3			Top Solder	Solder Resist	1.00mil	4.15	
4			Component Side	Copper	2.83mil		
5			Dielectric 1		3.59mil	3.5	
6			Ground Plane 1 (GND)	Copper	0.70mil		
7			Dielectric 2	FR-4	3.00mil	3.5	
8			Inner Layer 1	Copper	0.70mil		
9			Dielectric 3		2.88mil	3.5	
10			Inner Layer 2	Copper	0.70mil		
11			Dielectric 4		3.00mil	3.5	
12			Power Plane 1	Copper	0.70mil		
13			Dielectric 5		3.58mil	3.5	
14			Power Plane 2	Copper	0.70mil		
15			Dielectric 6		3.00mil	3.5	
16			Inner Layer 3	Copper	0.70mil		
17			Dielectric 7		2.88mil	3.5	
18			Inner Layer 4	Copper	0.70mil		
19			Dielectric 8		3.00mil	3.5	
20			Power Plane 3	Copper	0.70mil		
21			Dielectric 9		3.59mil	3.5	
22			Solder Side	Copper	2.83mil		
23			Bottom Solder	Solder Resist	1.00mil	4.15	
24			Bottom Overlay				
25			Bottom Paste				
	Height : 41.78mil		Height : 41.78mil				



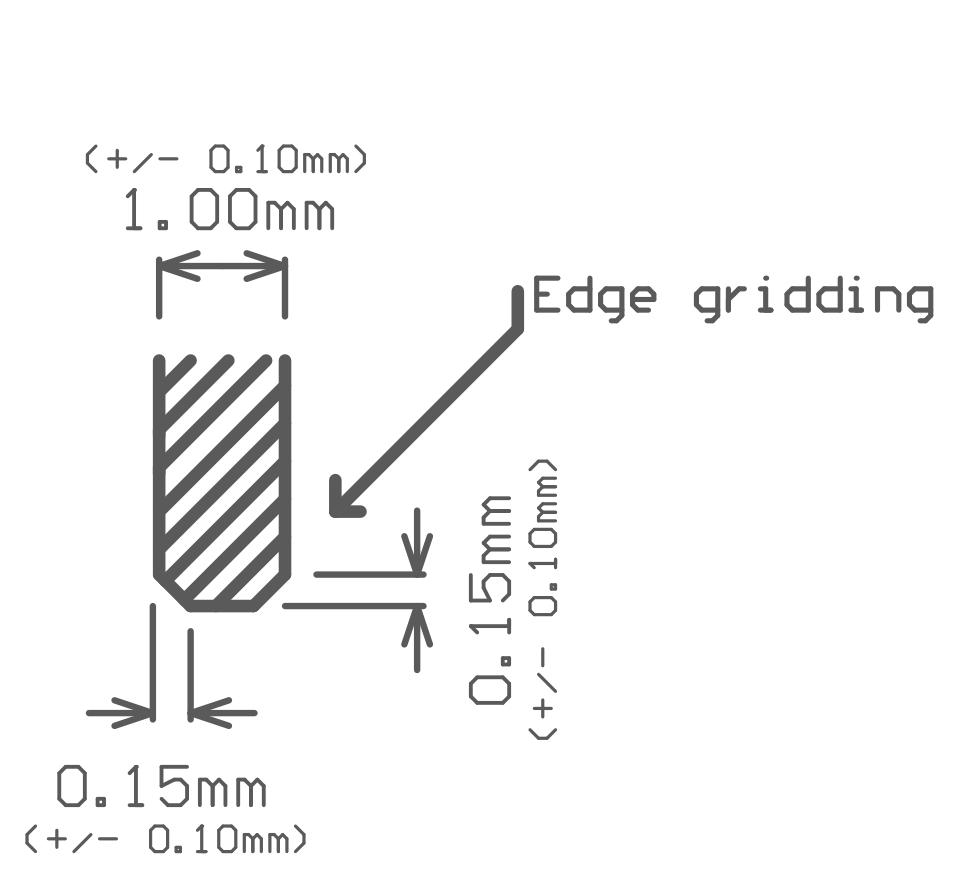
Detail 1



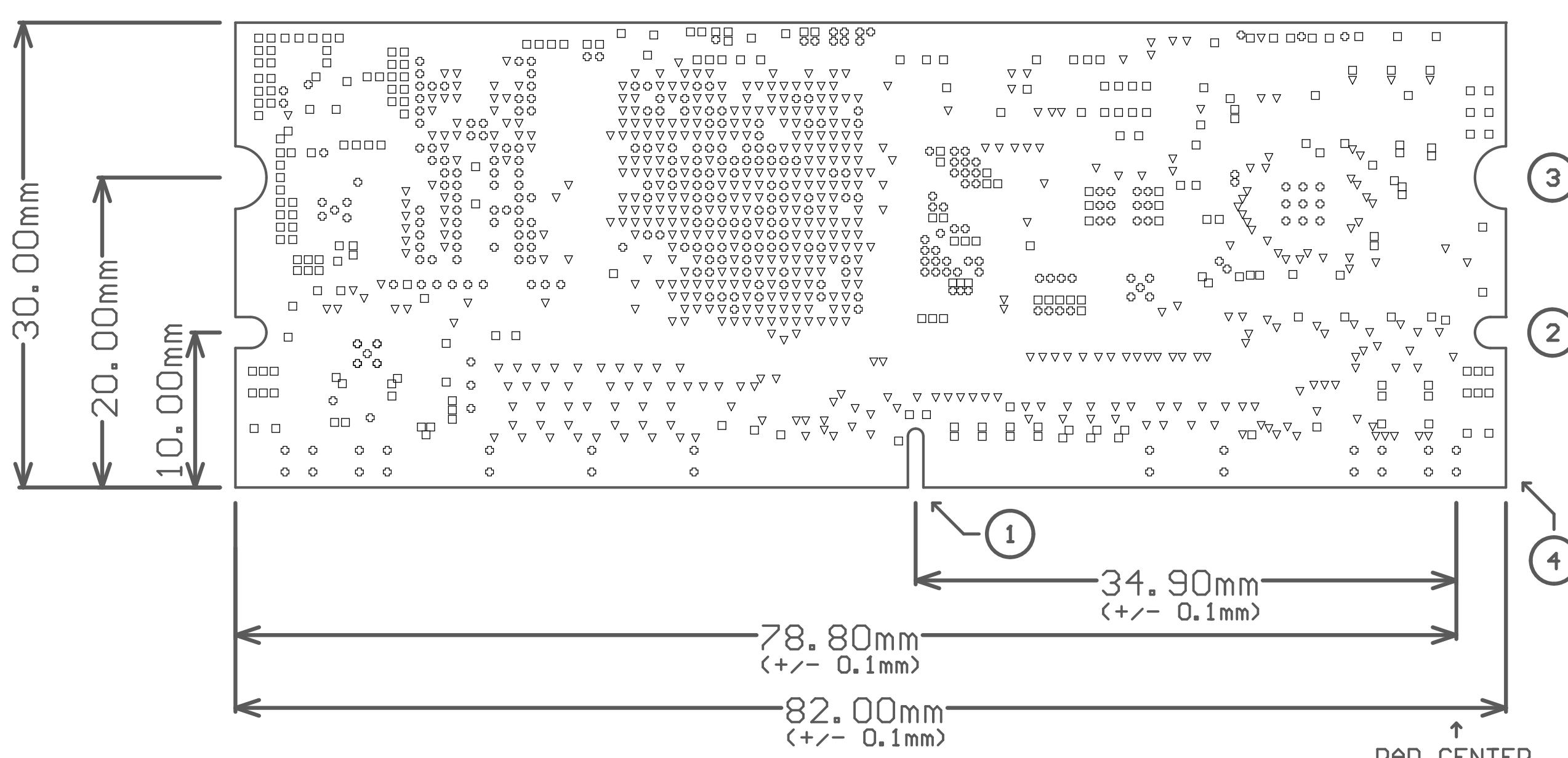
Detail 2



Detail 3

Detail 4
(PCB side view)

UW-IPMC MEZZANINE (revB)



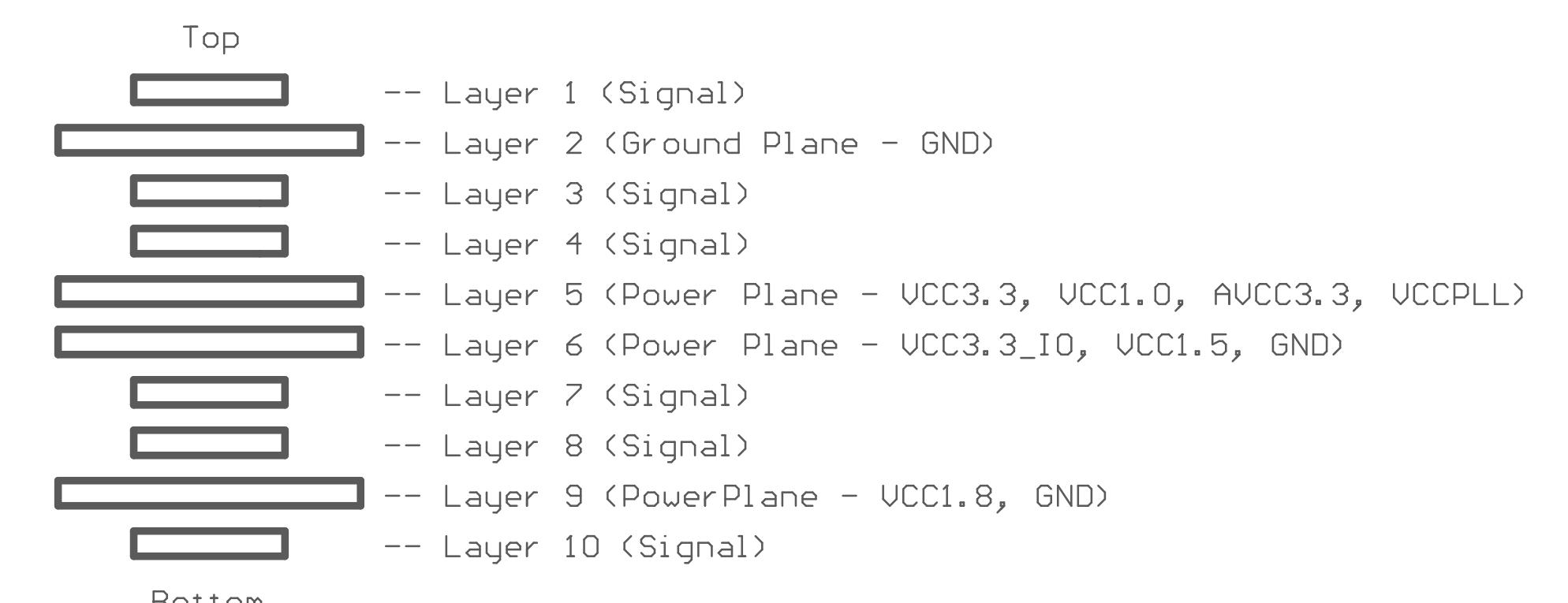
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Layer Stackup

Univ. of Wisconsin—Madison
Madison, WI 53706ENGINEER:
Vicente, M.TITLE:
ZYNQ-IPMCPCB DESIGNER:
Vicente, M.

PART NO.:

REV:
revB1DATE:
06JUN2019FILE NAME:
ZYNQ_IPMC.PCBDOC

DWG NO.:

SCALE:
1:1