Appendix B. Design Examples Synthesis Results

The synthesis results for all examples can be easily reproduced for the Quartus version installed on your computer by using the script `qvhdl.tcl` for VHDL or `qv.tcl` for Verilog available in the source code directories of the CD-ROM. Run the VHDL TCL script with

```
quartus_sh -t qvhdl.tcl
```

to compile all designs. The next step is to run the resource and timing analysis with

```
quartus_sta -t fmax4all.tcl
```

The script produces four parameters for each design. For the `trisc0.vhd`, for instance, we get the following:

```
....
----------------------------------------------------
trisc0 (Clock clk) : Fmax = 92.66 (Restricted Fmax = 92.66)
trisc0 LEs: 171 / 114,480 ( < 1 % )
trisc0 M9K bits: 256 / 3,981,312 ( < 1 % )
trisc0 9-bit DSP blocks: 1 / 532 ( < 1 % )
----------------------------------------------------
....
```

then use a utility like `grep` through the report `qvhdl.txt` file using `Fmax`, `LEs:` etc.

From the script you will notice that the following special options of Quartus II web edition 12.1 were used:

- `Device` set `Family` to `Cyclone IV E` and then under `Available devices` select `EP4CE115F29C7`.
- For `Timing Analysis Settings` set `Default required fmax:` to 1 ns.
- For `Analysis & Synthesis Settings` from the `Assignments` menu
  – set `Optimization Technique` to `Speed`
  – Deselect `Power-Up Don't Care`
- In the `Fitter Settings` select as `Fitter effort Standard Fit (highest effort)`

The table below displays the results for all VHDL and Verilog examples given in this book. The table is structured as follows. The first column shows the entity or module name of the design. Columns 2 to 6 are data for the VHDL designs: the number of LEs shown in the report file; the number of 9×9-bit multipliers; the number of M9K memory blocks; the registered performance `Fmax` using the `TimeQuest` slow 85C model; and the page with the source code. The same data are provided for the Verilog design examples, shown in columns 7 to 9. Note that VHDL and Verilog produce the same data for a number of 9×9-bit multipliers most of the time, except for the four designs `ica` (Verilog 184 multiplier), `pca` (Verilog 138 multiplier), `iir5para` (Verilog 58 multiplier), and `iir5lwdf` (Verilog 18 multiplier). LEs and registered performance never match. The number of M9K memory blocks do not match for the three designs `fft256`, `fun_text`, and `trisc0`. In Verilog the ROM LUTs are synthesized to M9K blocks, while in VHDL LEs are used. An `fpu` design is not available in Verilog. A few designs don't use registers and a registered performance cannot be measured.

Design	LEs	9 × 9 Mult. vhd/v	VHDL M9Ks vhd/v	f_{MAX} MHz	Page	LEs	Verilog f_{MAX} MHz	Page
add1p	125	0	0	350.63	83	77	336.25	797
add2p	233	0	0	243.43	83	143	318.17	798
add3p	372	0	0	231.43	83	228	278.47	799
adpcm	531	0	0	49.5	618	510	56.0	870
ammod	264	0	0	197.39	512	222	298.78	859
arctan	106	3	0	32.71	145	105	33.05	806
cic3r32	341	0	0	282.49	321	339	280.11	831
cic3s32	209	0	0	290.02	330	206	294.2	833
cmoms	549	3	0	95.27	369	421	102.81	841
cmul7p8	48	0	0	-	63	48	–	797
cordic	276	0	0	209.6	137	172	317.97	804
dapara	39	0	0	205.17	212	39	205.17	819
dasign	52	0	0	258.4	204	39	331.56	817
db4latti	420	0	0	58.11	390	248	99.02	845
db4poly	167	0	0	618.43	310	156	554.32	829
div_aegp	45	4	0	124.91	103	44	129.28	801
div_res	106	0	0	263.5	96	89	269.25	803
dwtden	879	0	1	120.93	406	889	164.28	847
example	33	0	0	267.24	17	32	457.67	795
farrow	363	3	0	39.82	358	268	58.25	839
fft256	34,340	8	0/2	31.12	442	33,926	31.16	854
fir4dlms	106	4	0	261.57	568	105	260.62	862
fir_gen	93	4	0	157.38	182	93	153.66	813
fir_lms	51	4	0	69.26	561	51	70.2	861
fir_srg	109	0	0	88.35	193	79	99.81	814
fpu	8112	7	0	-	120	–	–	–
fun_text	180	0	0/1	250.63	33	32	306.65	796
g711alaw	70	0	0	–	358	97	–	869
ica	2275	172/184	0	17.87	605	2091	17.84	866
iir	62	0	0	147.3	227	30	224.82	820
iir5lwdf	764	12/18	0	55.97	296	611	52.46	828
iir5para	624	51/58	0	87.69	267	513	86.72	825
iir5sfix	2474	128	0	46.99	255	2474	47.08	824
iir_par	236	0	0	479.39	247	185	430.29	822
iir_pipe	123	0	0	215.05	241	75	350.14	821
lfsr	6	0	0	944.29	495	6	944.29	858
lfsr6s3	6	0	0	931.97	497	6	931.97	858
ln	88	10	0	29.2	156	88	29.2	807
magnitude	96	0	0	119.59	167	145	107.34	812
pca	2447	180/138	0	18.46	596	1609	23.82	864
rader7	428	0	0	138.45	429	403	151.56	851
rc_sinc	880	0	0	59.53	350	847	78.52	835
reg_file	226	0	0	-	653	226	–	874
sqrt	261	2	0	86.23	161	244	112.1	809
trisc0	171	1	1/2	92.66	701	140	85.59	875