USC_12nm_Release_Jan21_2019

1. User is required to have Cadence ICADV12.3 or later to read the schematics.
2. User needs the standard libraries that are distributed by Cadence to read the schematics (US_8ths, basic, analogLib, functional, cdsDefTechLib)
3. User needs the 12nm technology libraries in order to be able to see the device symbols and properties. This requires an NDA between the user and Global Foundries, which is the responsibility of the user.
4. The 12nm library has technology properties for the selected metal stack option of **13M_3Mx_2Cx_4Kx_2Hx_2Gx_LB**, whose meaning is defined in the PDK to be obtained under NDA. The libraries and design are valid at PDK version V1.6.0 (Rev 11). The user is advised that selecting a different metal-stack option for tapeout will require the above variable to be changed. At the schematic level, this will affect the metal-oxide-metal capacitors used in the designs.
5. Simulation testbenches are provided for toplevel cells.
6. Simulation is using adexl and Spectre. Adexl views and Spectre states are provided.
7. Layout cells are not provided at this time.
8. The library has one top-level cell – TIADC (8 bit SAR ADC). Layout cells will be provided to the user under NDA for these cells.
9. Design Corners: Process Corners, -55C to 125C, Vdd nominal +/- 10%
   a. **Toplevel cell 1: TIADC:**
      8-bit, 7.68 GS/s SAR ADC with 3.84 GHz sampling clock
         ADC has 8 8-bit parallel outputs.

      Typical Current consumption specifications from 0.8V supply at room temperature:
      Analog circuit current consumption: 26.45mA
      Digital circuit current consumption: 37.5uA
      Current consumption from 0.8V reference input: 78.7uA

Total current consumption: 26.56mA

The tabular description below corresponds to the structure of the design library as seen in Cadence. The "/" character indicates a subcategory under the category preceding the "/" character.

#	Category	CellName	Description
1	Top level	TIADC	8-bit, 7.68GS/s SAR ADC
		INTL_v3	Interleaver
		INTL_RANK2	Interleaver rank2
2	Single channel ADC	ADC_v2	Single channel ADC
		Bsw_10b	Bootstrapped switch
		DAC_8b_v2	Capacitor DAC for single channel ADC
		CompStrongArm_rvt	Comparator for single channel ADC
		DCDL_20	Delay line for single channel ADC
		cap	Capacitor cell
4	Digital Cells	SC7P5T_INVX1_SSC14R	1x strength inverter
		SC7P5T_NR1_SSC14R	1x strength nor2 gate