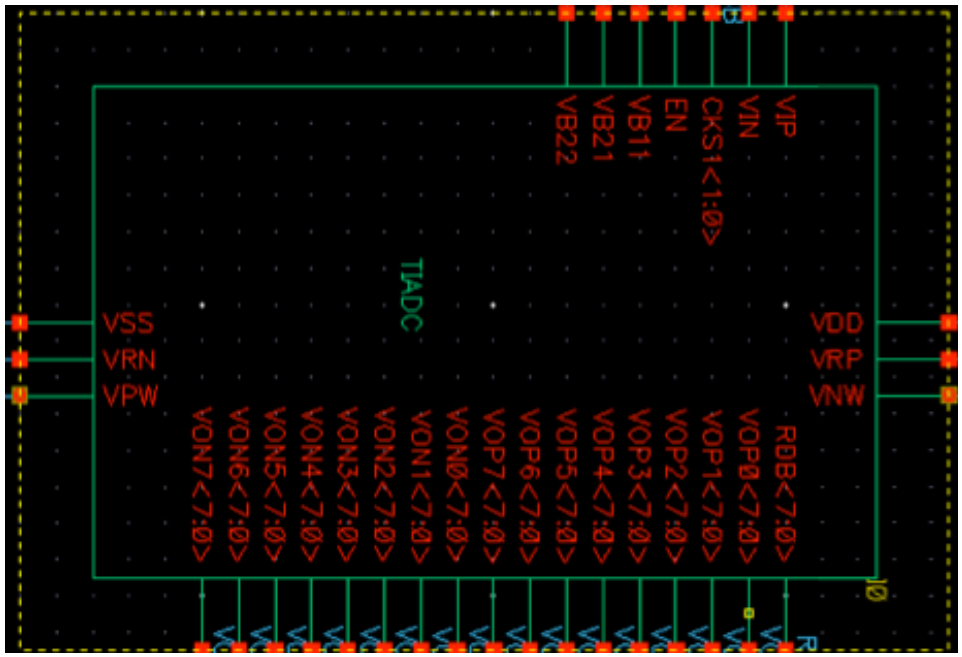
GF12nm 8b Time-Interleaved SAR ADC

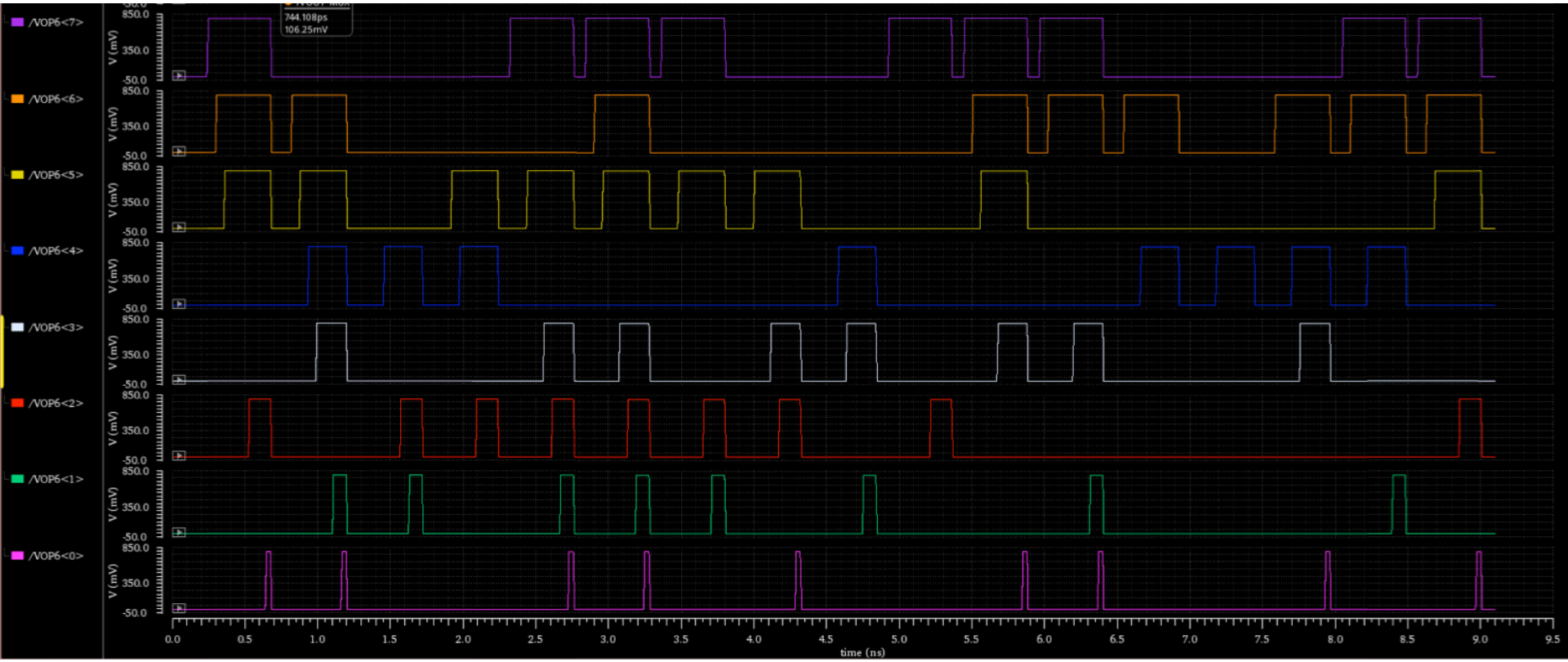
ADC Simulation Results

ADC pin out definitions



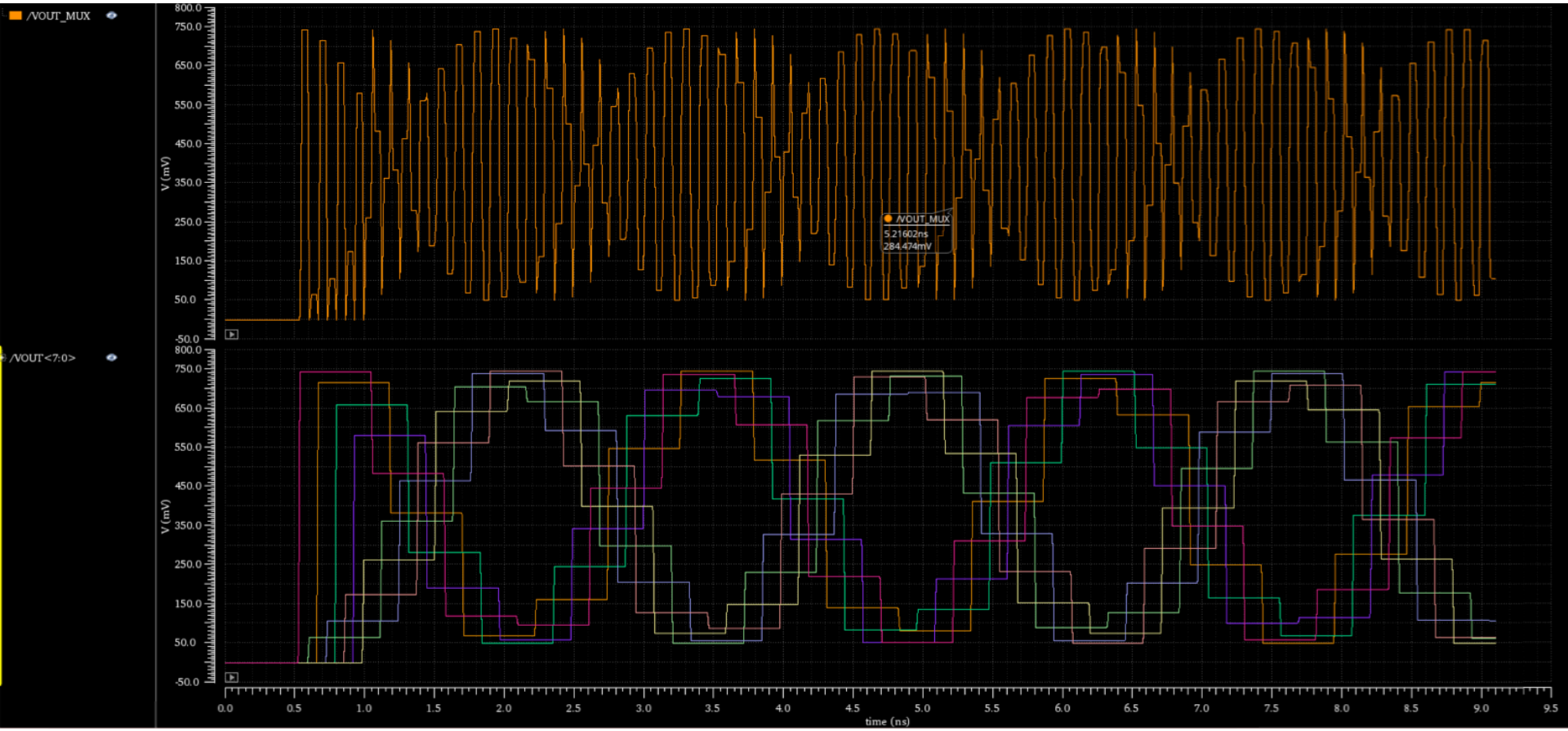
- VIP & VIN: differential input; EN: logic 1 to turn on ADC
- CKS1<1:0>: clock input; VB11, VB21, VB22: bias voltages
- VRP & VRN: differential reference inputs (refp = 0.8V & refm = 0V)
- VSS: ground; VDD: 0.8V analog supply; VNW: pfet substrate; VPW: nfet substrate
- RDB: serial data sync signal; VOP&VON: ADC serial data output

Top Level Test Result (I): output



- VOP: output of each SAR ADC channel

Top Level Test Result (II): output



- VOUT: serialized output of SAR ADC
- VOUT_MUX: VOUT converted to analog value

Top Level Test Result (III): output spectrum

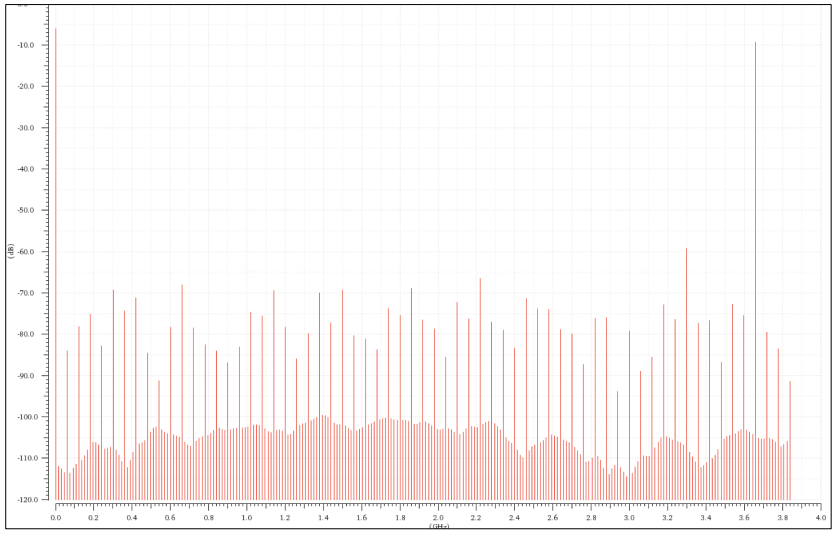


Fig. 1 Spectrum of ADC output

VIppd	600mV
Input frequency	3.66GHz
Clock frequency	7.68GHz
Duty cycle	0.16
Sampling time	60ps
DAC capacitance	128fF
ENOB	7.07bits
SINAD	43.23dB
SNR	44.56dB
SFDR	46.81dB

Interleaver Test Result

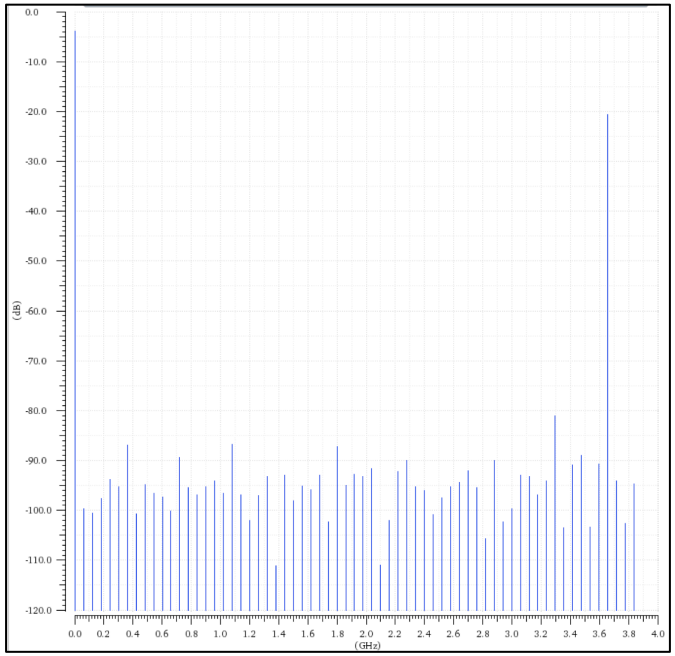


Fig. 1 Spectrum of Interleaver output

Input frequency	3.66GHz
Clock frequency	7.68GHz
Duty cycle	0.16
Sampling time	60ps
DAC capacitance	128fF
ENOB	8.67bits
SINAD	54.00dB
SFDR	60.43dBc

Single Channel SAR ADC Test Result (best spec)

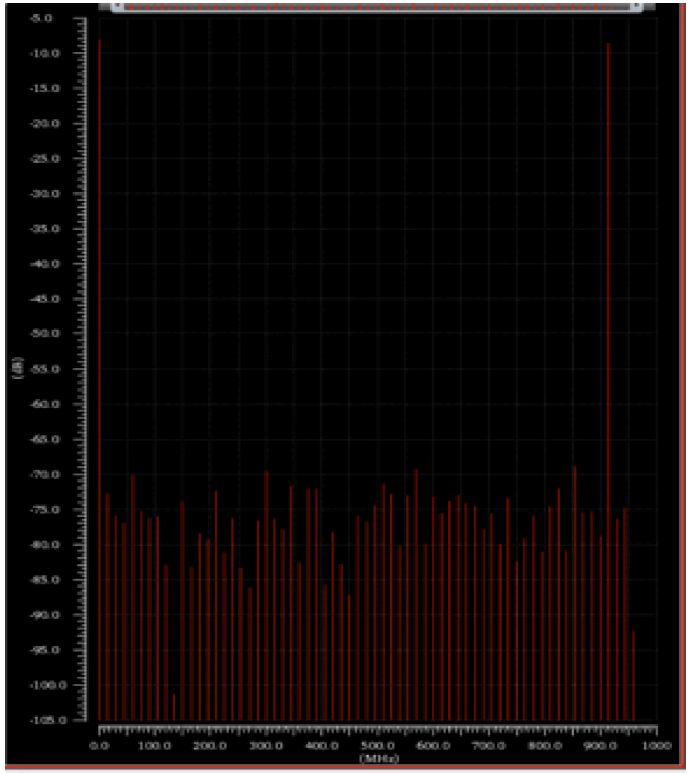


Fig. 1 Spectrum of Interleaver output

Input frequency	0.915GHz
Clock frequency	1.92GHz
Duty cycle	0.08
DAC capacitance	128fF
ENOB	7.78bits
SINAD	48.3dB
SFDR	60.23dBc