ECE-124 Lab-3 Submission Form – Winter 2018

GROUP NUMBER: 20	Lab3 Demo	Lab3 Report	
SESSION NUMBER: 201	Out of 10	Out of 10	

NAME: (Print)	UW User ID (not Student ID)	Signature
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LAB3 DESIGN DEMO	Marks Allotted	A	B
Desired Temp (sw[7..4]) is displayed on Digit1?	1	1	1
Current Temp (sw[3..0]) is displayed on Digit2?	1	1	1
Doors/Windows (PB[2..0]) displayed on LEDs[6..4]?	1	1	1
Furnace, Blower, System At Temp, A/C, Blower Indicators LEDs?	1	1	1
A/C ON & Blower ON when Current Temp > Desired Temp?	1	1	1
Furnace ON & Blower ON when Current Temp < Desired Temp?	1	1	1
A/C, Furnace, Blower turn OFF when Doors/Windows Open?	1	1	1
DISCUSSION: Comment on your VHDL Implementation?	3	3	3

LAB3 DESIGN REPORT (see rubric on LEARN for details)	Marks Allotted	TEAM	
All VHDL files (not the sevenseg_decoder or seg7_mux files). Structural VHDL design must be used at the Top Level. Comparator must have a **Boolean equation** per each output.	2		
Truth Table for 4-Bit Comparator Design with all entries inserted	2		
Part A Simulations of Comparator showing A>B, A=B, A<B	2		
RTL View of the Logic design (just of the Top Level)	2		
Total Design Logic Elements Used /8064	2		
Delay in Report Submission (-1 per day) x number of days:			
LAB3 REPORT MARK	**Out of 10**		

Top Level Code

```
1   library ieee;
2   use ieee.std_logic_1164.all;
3   use ieee.numeric_std.all;
4
5
6   entity LogicalStep_Lab3_top is port (
7      clkin_50    : in  std_logic;
8      pb          : in  std_logic_vector(3 downto 0);
9      sw          : in  std_logic_vector(7 downto 0); -- The switch inputs
10     leds        : out std_logic_vector(7 downto 0); -- for displaying the switch content
11     seg7_data   : out std_logic_vector(6 downto 0); -- 7-bit outputs to a 7-segment
12     seg7_char1  : out std_logic                     -- seg7 digi selectors
13     seg7_char2  : out std_logic                     -- seg7 digi selectors
14
15  );
16  end LogicalStep_Lab3_top;
17
18  architecture Energy_Monitor of LogicalStep_Lab3_top is
19  --
20  -- Components Used
21  ------------------------------------------------------------------
22  component Compx4 port (
23            A           : in  std_logic_vector(3 downto 0);
24            B           : in  std_logic_vector(3 downto 0);
25            Greater     : out std_logic;
26            Equal       : out std_logic;
27            Lesser      : out std_logic
28
29     );
30     end component;
31
32  component SevenSegment port (
33     hex         :  in  std_logic_vector(3 downto 0);   -- The 4 bit data to be displayed
34     sevenseg    :  out std_logic_vector(6 downto 0)    -- 7-bit outputs to a 7-segment
35     );
36     end component;
37
38     component segment7_mux port (
39        clk       : in std_logic := '0';
40        DIN2      : in std_logic_vector(6 downto 0);
41        DIN1      : in std_logic_vector(6 downto 0);
42        DOUT      : out std_logic_vector(6 downto 0);
43        DIG2      : out std_logic;
44        DIG1      : out std_logic
45     );
46     end component;
47
48  ------------------------------------------------------------------
```

```
-- Create any signals, or temporary variables to be used

   signal seg7_A     : std_logic_vector(6 downto 0); -- right digit, current temp
   signal seg7_B     : std_logic_vector(6 downto 0); -- left digit, desired temp
   signal cur_grtr   : std_logic; -- current is greater than desired
   signal cur_equa   : std_logic; -- current is equal to desired
   signal cur_less   : std_logic; -- current is less than desired
   signal AC         : std_logic; -- State A/C
   signal FUR        : std_logic; -- State Furance
   signal SYS        : std_logic; -- State System
   signal BLOW       : std_logic; -- State Blower ON


-- Here the circuit begins

begin

   INST1: Compx4 port map(sw(3 downto 0), sw(7 downto 4), cur_grtr, cur_equa, cur_less); -- comparing desired and current temps

   INST2: SevenSegment port map(sw(3 downto 0), seg7_A);             -- display the current temp
   INST3: SevenSegment port map(sw(7 downto 4), seg7_B);             -- display the  desired temp
   INST4: segment7_mux port map(clkin_50, seg7_A, seg7_B, seg7_data, seg7_char2, seg7_char1);


   leds(4) <= Not pb(0); --Backdoor open
   leds(5) <= Not pb(1); -- window(s) open
   leds(6) <= Not pb(2); -- Frontdoor open

   AC <= cur_grtr AND pb(0) AND pb(1) AND pb(2); -- if all of the doors and windows are closed, and the current is greater than desired
   FUR <= cur_less AND pb(0) AND pb(1) AND pb(2); -- if all of the doors and windows are closed, and the current is less than desired
   SYS <= cur_equa;                              --System at temp if temps are equal
   BLOW <= pb(0) AND pb(1) AND pb(2) AND (cur_grtr OR cur_less); --IF A/C is on or Furance is on and all the window(s) are closed

   leds(3) <= BLOW; --send signals to appropriate leds
   leds(2) <= AC;
   leds(1) <= SYS;
   leds(0) <= FUR;


end Energy_Monitor;
```

One Bit Comparator

```
 1  library IEEE;
 2  use IEEE.std_logic_1164.all;
 3  use IEEE.numeric_std.all;
 4
 5
 6  entity Compx1 is
 7     port (
 8           A           : in  std_logic; -- first one bit number
 9           B           : in  std_logic; -- second one bit number
10           Greater     : out std_logic; -- possible states
11           Equal       : out std_logic;
12           Lesser      : out std_logic
13        );
14  end entity Compx1;
15
16  architecture Comparison of Compx1 is
17
18  begin
19
20     Equal <= NOt (A XOR B); -- logic behind comparisons
21     Lesser <= (NOT A) AND B;
22     Greater <= A AND (Not B);
23
24
25  end Comparison;
26
27
```

Four Bit Comparator

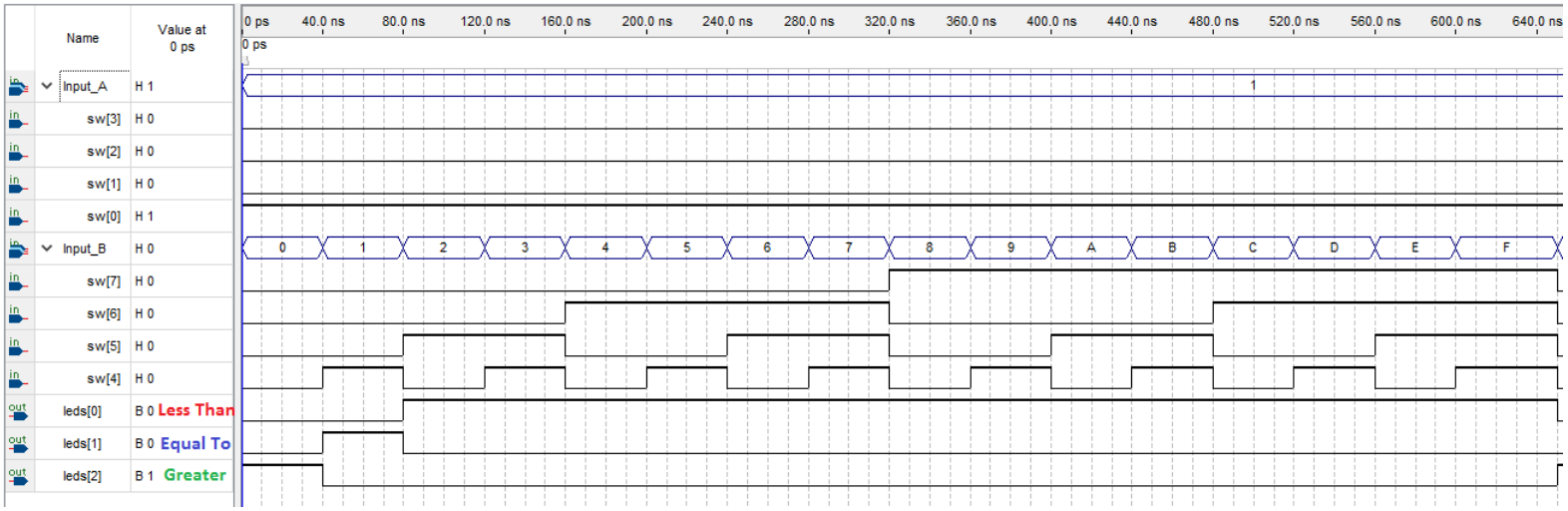
```vhdl
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;


entity Compx4 is
   port (
           A          : in  std_logic_vector(3 downto 0); --first four bit number
           B          : in  std_logic_vector(3 downto 0); -- second four bit number
           Greater    : out std_logic; --Possible States
           Equal      : out std_logic;
           Lesser     : out std_logic
       );
end entity Compx4;

architecture Comparison of Compx4 is

component Compx1 port (
           A          : in  std_logic;
           B          : in  std_logic;
           Greater    : out std_logic;
           Equal      : out std_logic;
           Lesser     : out std_logic

   );
   end component;

   signal E    : std_logic_vector(3 downto 0); --Equal to state (for each seperate bit)
   signal G    : std_logic_vector(3 downto 0); -- Greater than state (for each seperate bit)
   signal L    : std_logic_vector(3 downto 0); -- Less than state (for each seperate bit)

begin

   INST1: Compx1 port map(A(3), B(3), G(3), E(3), L(3)); -- initiating the four one bit comparators
   INST2: Compx1 port map(A(2), B(2), G(2), E(2), L(2));
   INST3: Compx1 port map(A(1), B(1), G(1), E(1), L(1));
   INST4: Compx1 port map(A(0), B(0), G(0), E(0), L(0));

   Equal <= E(3) AND E(2) AND E(1) AND E(0);                                                    --logic behind all of the comparisons
   Greater <= G(3) OR (E(3) AND G(2)) OR (E(3) AND E(2) AND G(1)) OR (E(3) AND E(2) AND E(1) AND G(0));
   Lesser <= L(3) OR (E(3) AND L(2)) OR (E(3) AND E(2) AND L(1)) OR (E(3) AND E(2) AND E(1) AND L(0));


end Comparison;
```

Truth Table

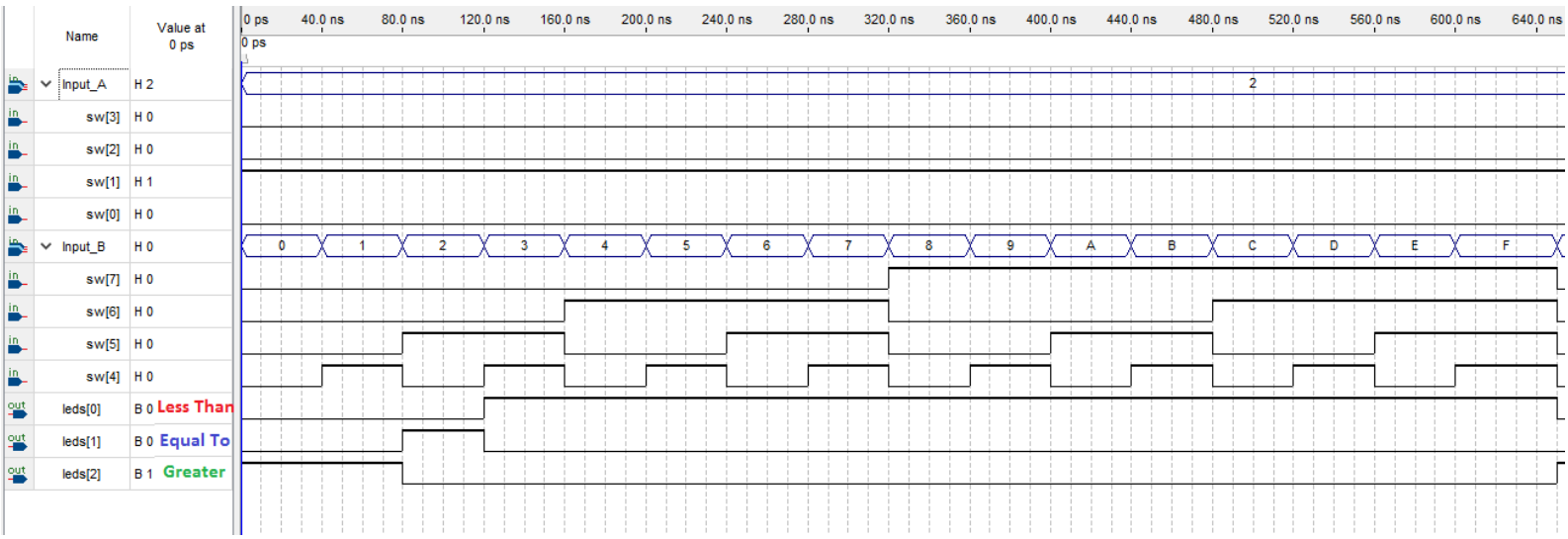
Comparison Inputs from 1- Bit Comparators												4-Bit Compartor Outputs		
A3 < B3	A3 = B3	A3 > B3	A2< B2	A2=B2	A2> B2	A1< B1	A1= B1	A1> B1	A0< B0	A0 =B0	A0 > B0	A<B	A = B	A > B
0	0	1	X	X	X	X	X	X	X	X	X	0	0	1
1	0	0	X	X	X	X	X	X	X	X	X	1	0	0
0	1	0	0	0	1	X	X	X	X	X	X	0	0	1
0	1	0	1	0	0	X	X	X	X	X	X	1	0	0
0	1	0	0	1	0	0	0	1	X	X	X	0	0	1
0	1	0	0	1	0	1	0	0	X	X	X	1	0	0
0	1	0	0	1	0	0	1	0	0	0	1	0	0	1
0	1	0	0	1	0	0	1	0	1	0	0	1	0	0
0	1	0	0	1	0	0	1	0	0	1	0	0	1	0

Simulations

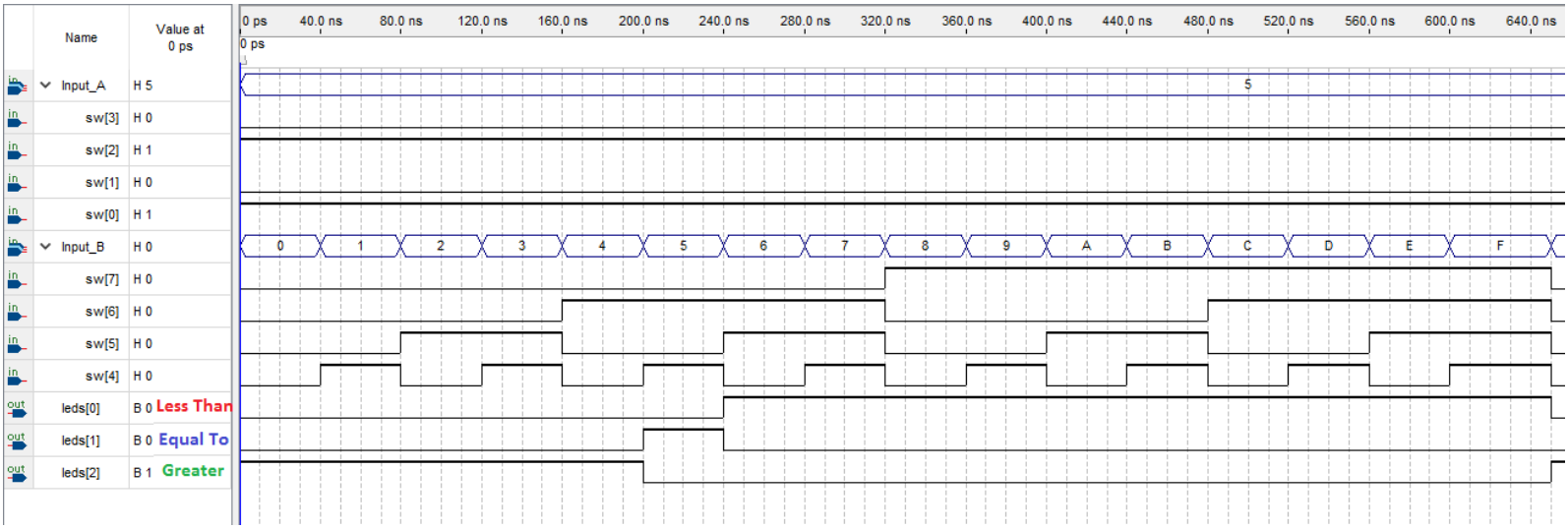
Input_A fixed at Hex 1



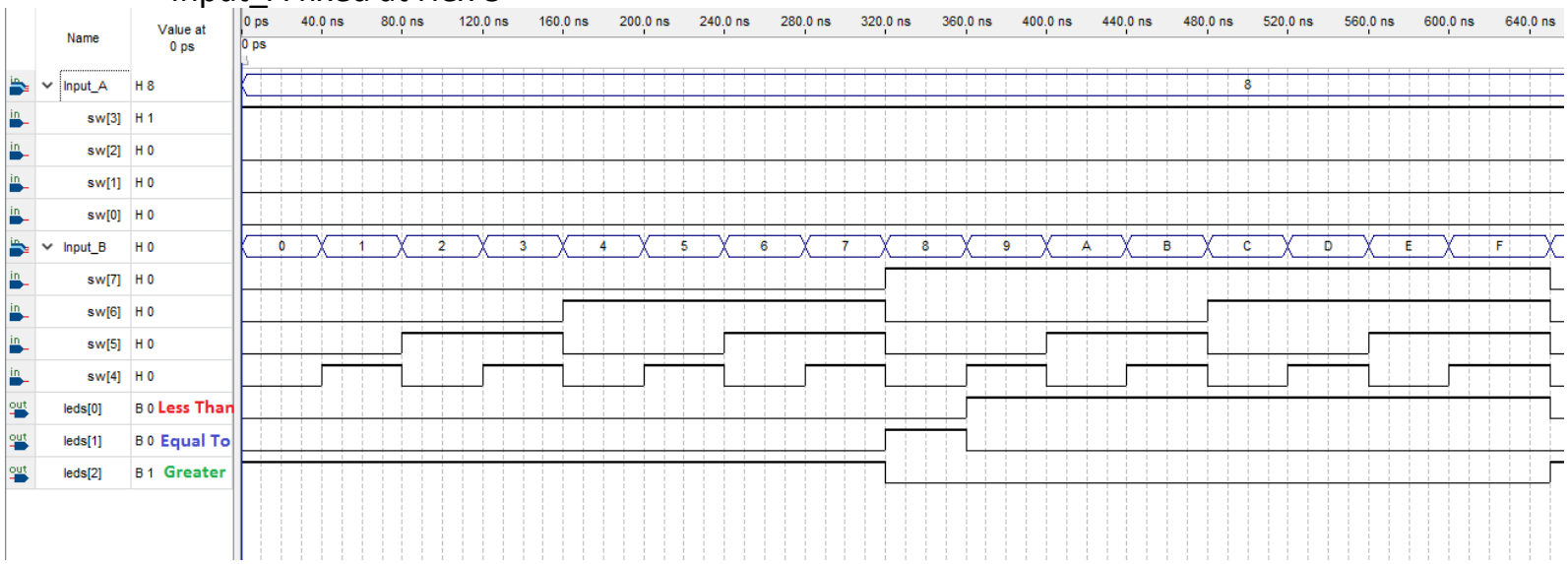
Input_A fixed at Hex 2



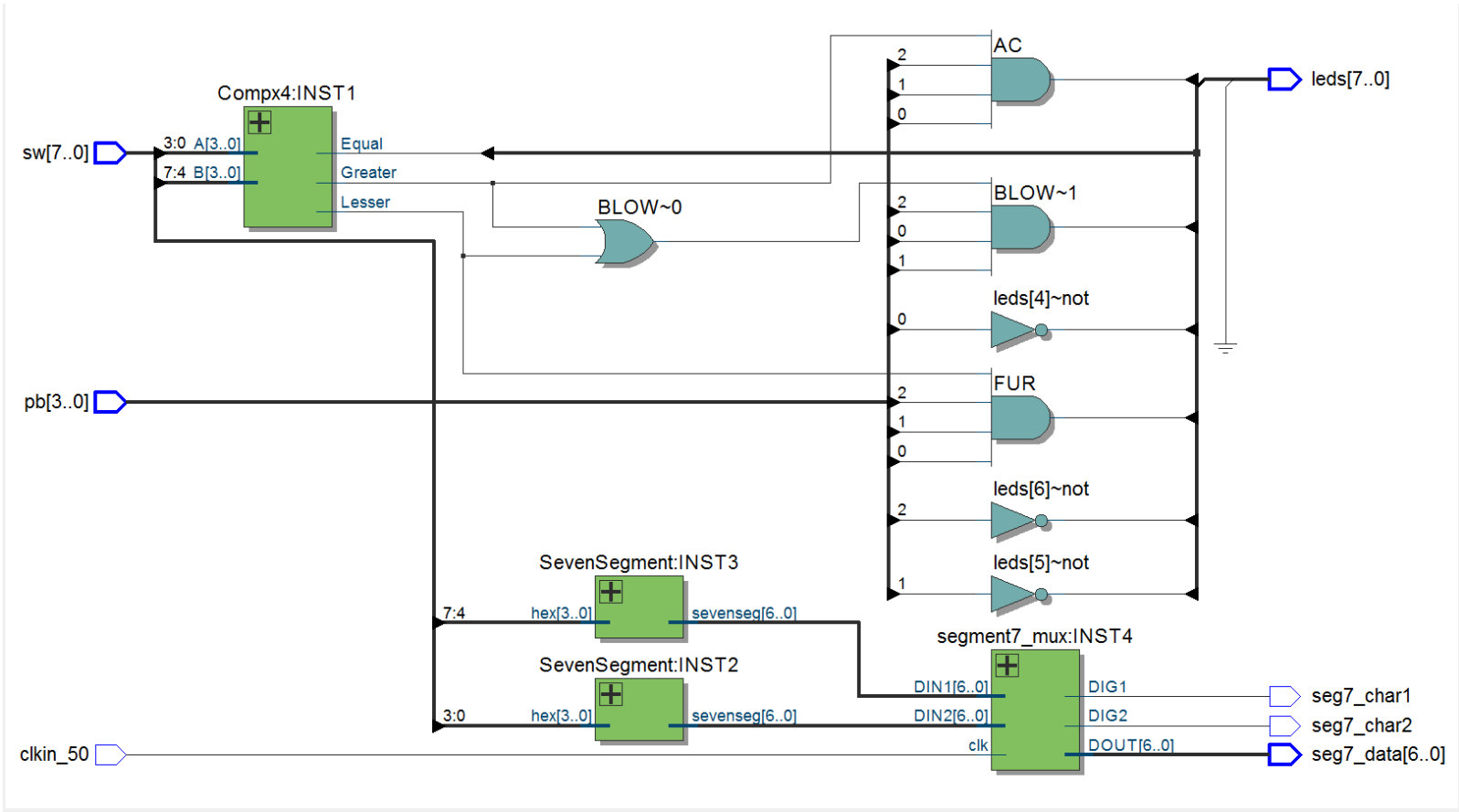
Input_A fixed at Hex 5



Input_A fixed at Hex 8



RTL View of Top Design



Compilation Report

Flow Summary	
Flow Status	Successful - Fri Mar 02 19:54:59 2018
Quartus Prime Version	15.1.0 Build 185 10/21/2015 SJ Standard Edition
Revision Name	LogicalStep_Lab3_top
Top-level Entity Name	LogicalStep_Lab3_top
Family	MAX 10
Device	10M08SAE144C8G
Timing Models	Final
Total logic elements	45 / 8,064 (< 1 %)
Total combinational functions	45 / 8,064 (< 1 %)
Dedicated logic registers	11 / 8,064 (< 1 %)
Total registers	11
Total pins	30 / 101 (30 %)
Total virtual pins	0
Total memory bits	0 / 387,072 (0 %)
Embedded Multiplier 9-bit elements	0 / 48 (0 %)
Total PLLs	0 / 1 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 1 (0 %)

Total Elements