8-bit Shift Register

Project Report

Submitted To:

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Submitted By:

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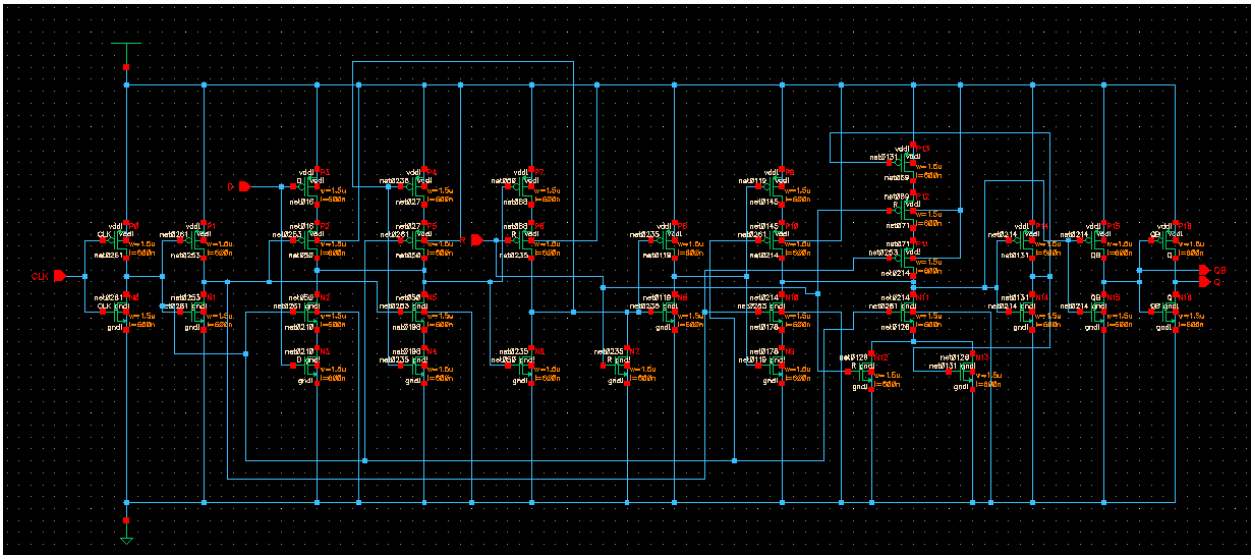
Dated : May 23, 2016

DELIVERABLES:

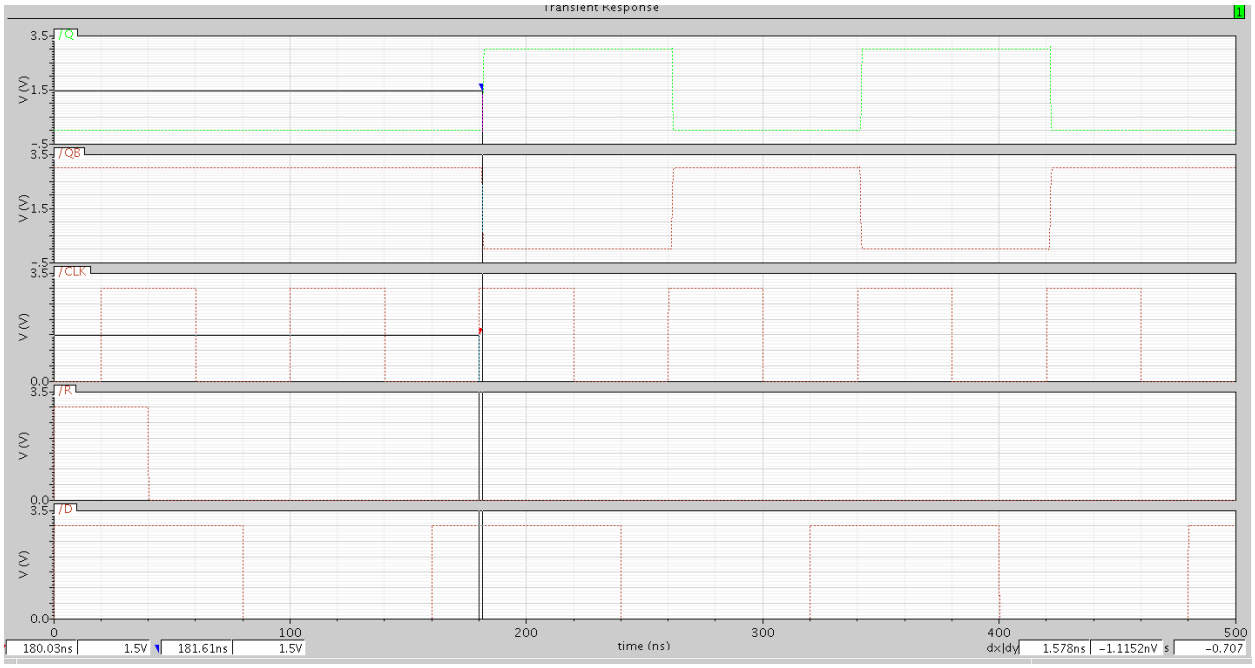
Schematic of DFFR cells:



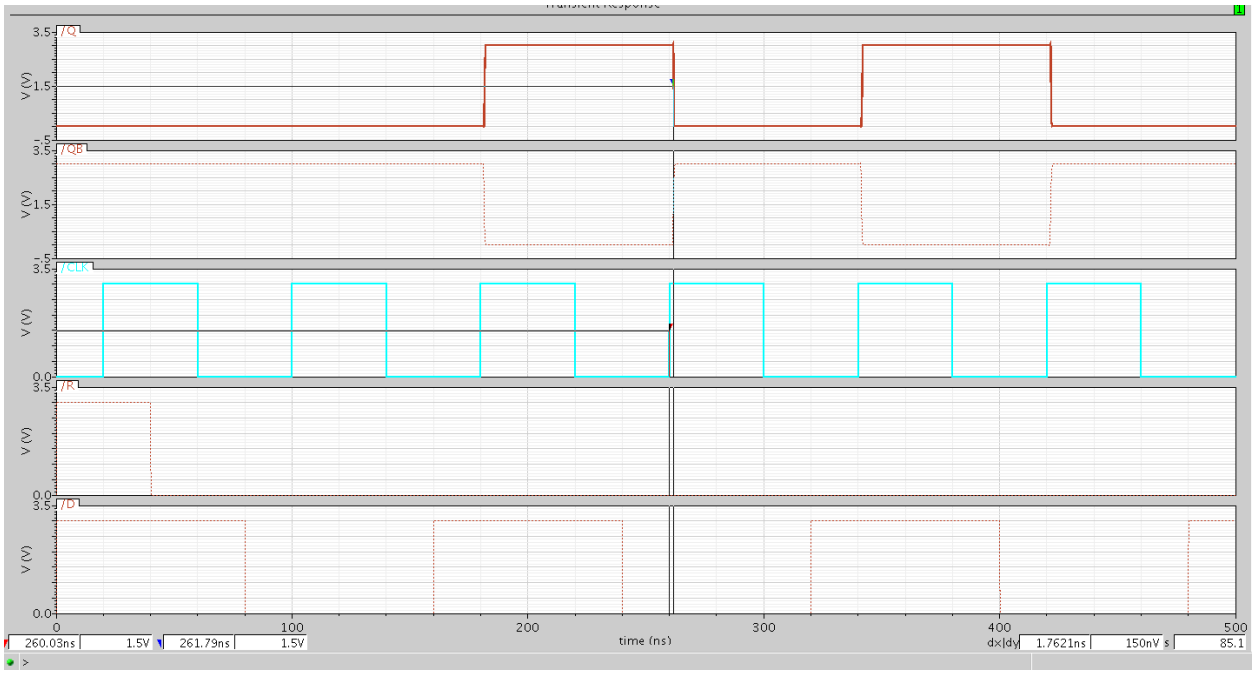
Post Layout Simulation:

Timing Delays:

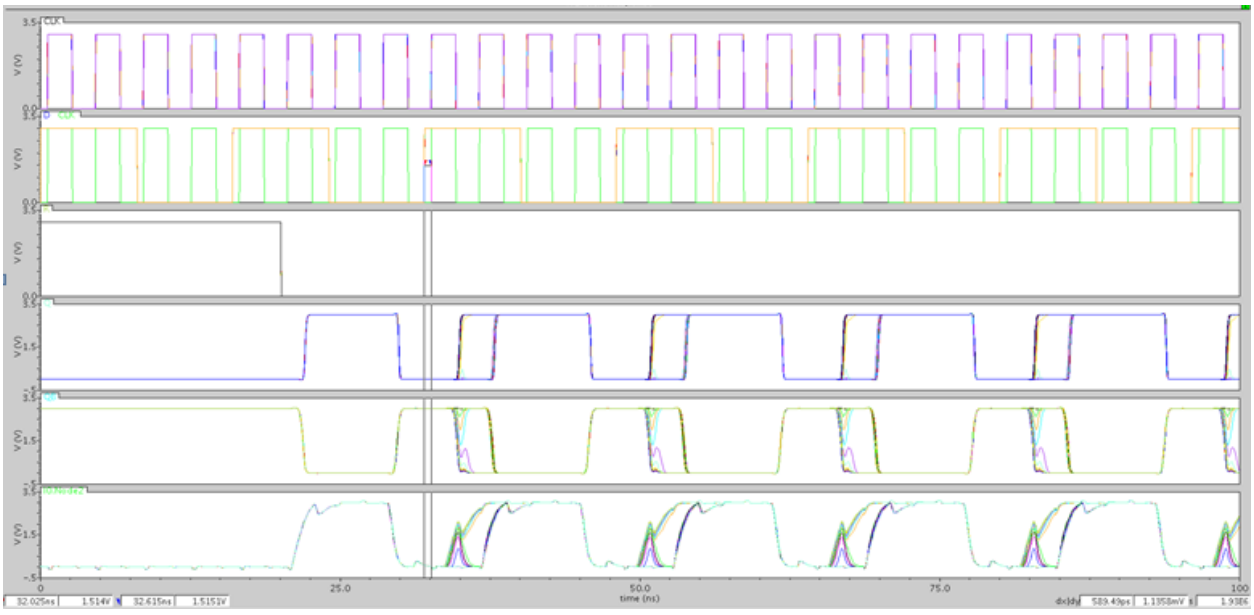
Propagation Delay Low to High (tpLH=1.578ns)



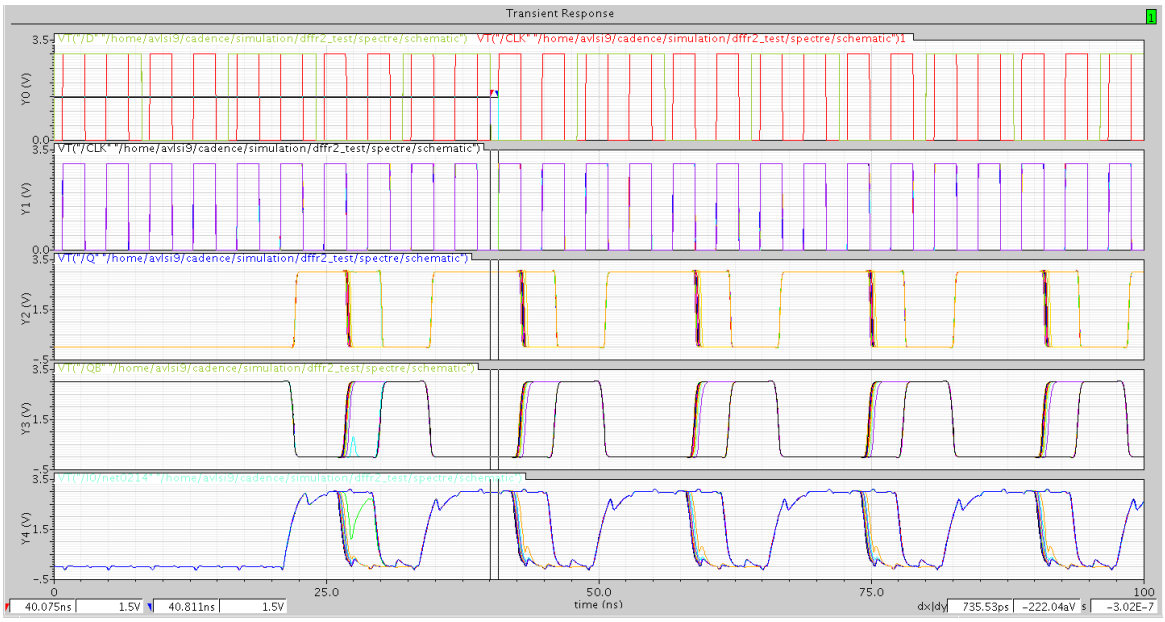
Propagation Delay (tpHL 1.7621ns)



Setup time for Rising edge(589.4ps)



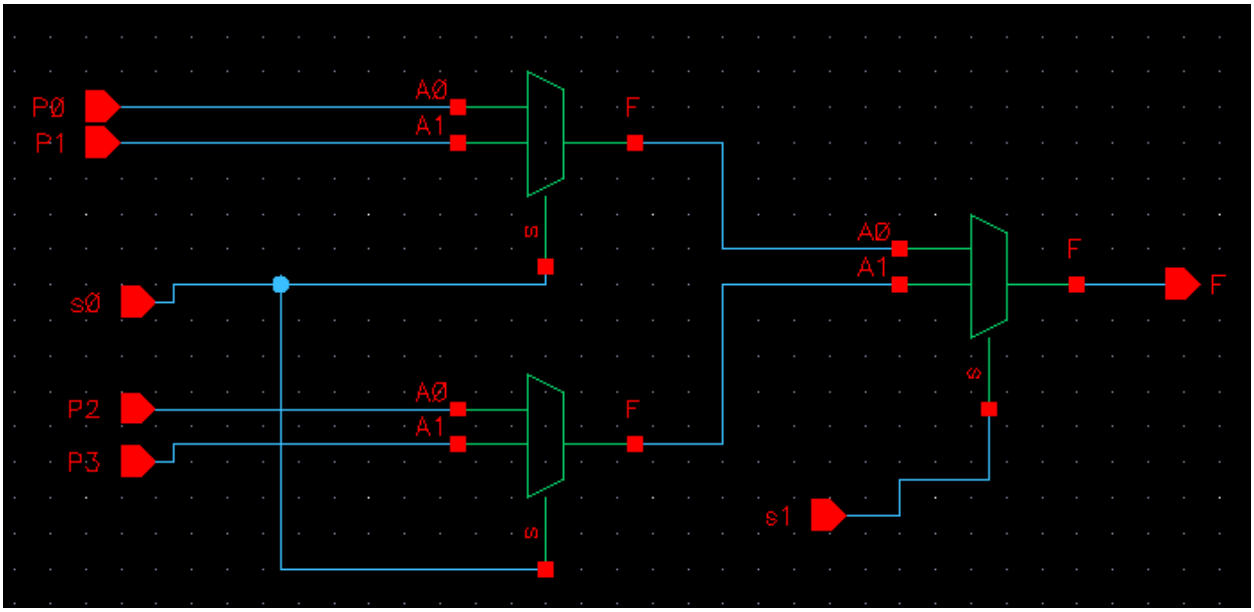
Setup time for falling edge(735.3ps)



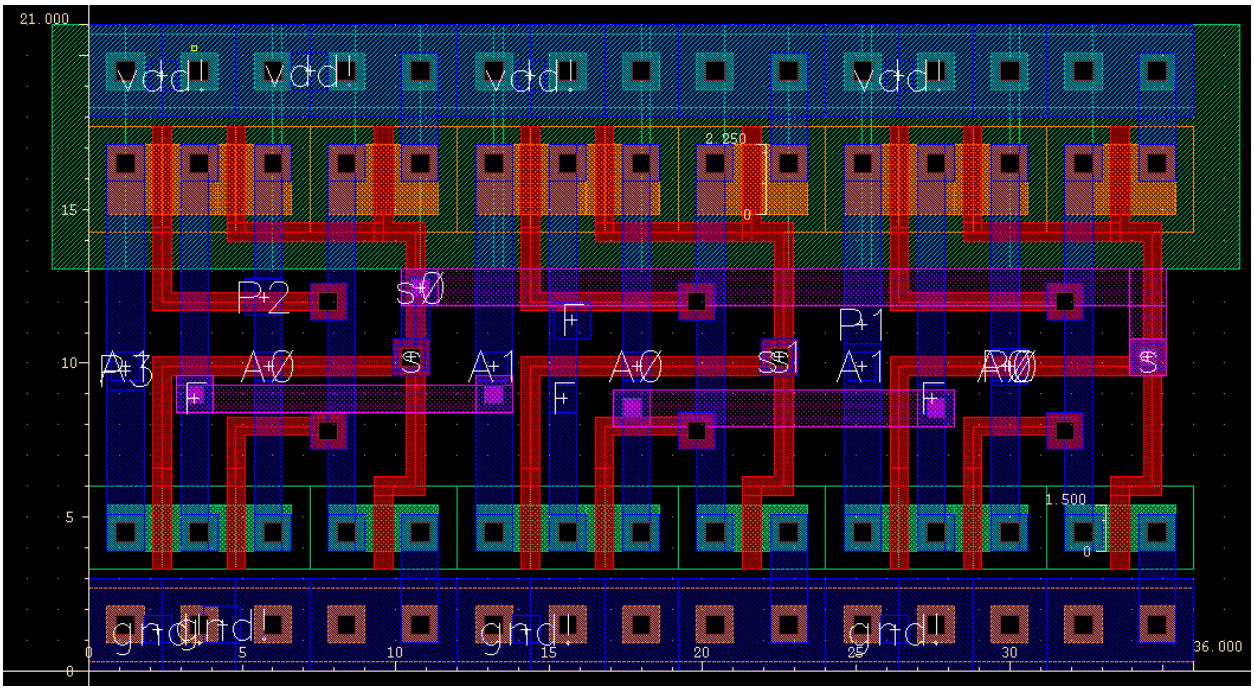
LVS RESULTS OF DFFR:

```
@(#)$CDS: LVS.exe version 5.1.0 06/20/2007 02:10 (cicln03) $

Command line: /usr/Cadence/tools.lnx86/dfII/bin/32bit/LVS.exe -dir /home/avlsi9/Group9_n/LVS -l -s -t /home/avlsi9/Group9_n/L
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

    Net-list summary for /home/avlsi9/Group9_n/LVS/layout/netlist
       count
         24               nets
         7                terminals
         17               pmos
         17               nmos

    Net-list summary for /home/avlsi9/Group9_n/LVS/schematic/netlist
       count
         24               nets
         7                terminals
         17               pmos
         17               nmos


    Terminal correspondence points
    N17         N16         CLK
    N13         N11         D
    N12         N9          Q
    N23         N25         QB
    N9          N8          R
    N16         N1          gnd!
    N0          N0          vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        nfet pfet nmos4 pmos4 cap

The net-lists match.

                              layout  schematic
                                 instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                    34      34
        total                     34      34
```

SCHEMATICS OF 4X1 MUX:



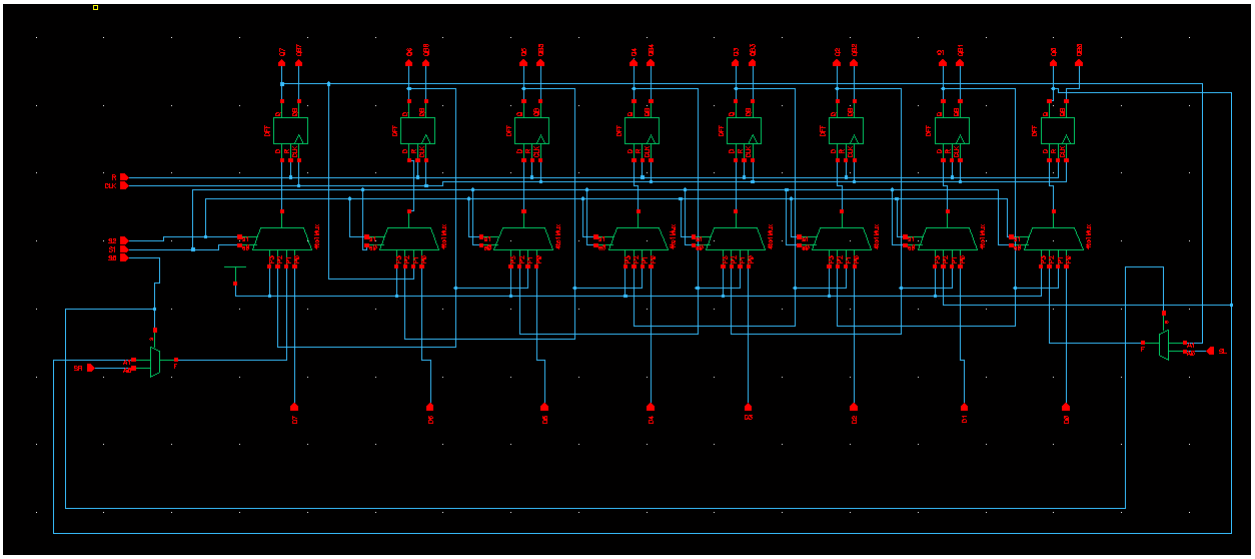
LAYOUT OF 4X1 MUX:



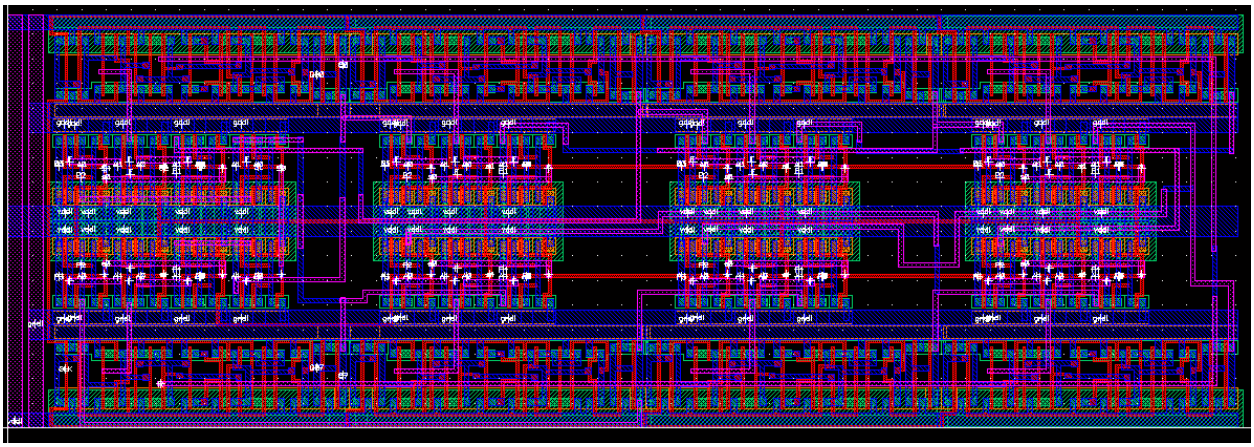
LVS OF 4X1 MUX:

```
@(#)$CDS: LVS.exe version 5.1.0 06/20/2007 02:10 (cicln03) $

Command line: /usr/Cadence/tools.lnx86/dfII/bin/32bit/LVS.exe -dir /home/avlsi9/Group9_n/LVS -l -s -t /home/avlsi9/Group9_n/LVS/layout /home/avlsi9/Group9_n/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

    Net-list summary for /home/avlsi9/Group9_n/LVS/layout/netlist
        count
         14               nets
         9                terminals
         9                pmos
         9                nmos

    Net-list summary for /home/avlsi9/Group9_n/LVS/schematic/netlist
        count
         14               nets
         9                terminals
         9                pmos
         9                nmos


    Terminal correspondence points
    N1          N4          F
    N13         N9          P0
    N11         N3          P1
    N0          N2          P2
    N6          N8          P3
    N4          N1          gnd!
    N7          N7          s0
    N5          N6          s1
    N2          N0          vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        nfet pfet nmos4 pmos4 cap

The net-lists match.

                              layout  schematic
                                 instances
        un-matched               0       0
        rewired                  0       0
        size errors              0       0
        pruned                   0       0
```

SCHEMATICS OF 8 BIT SHIFT REGISTER:



LAYOUT OF 8 BIT SHIFT REGISTER:



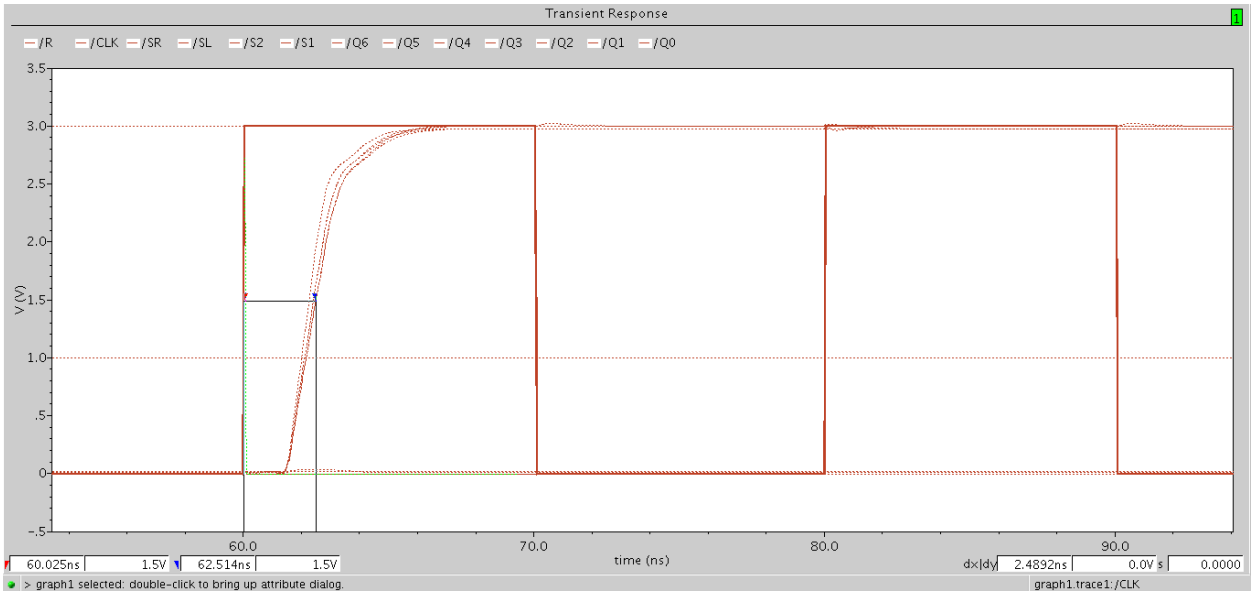
LVS OF 8 BIT SHIFT REGISTER:

```
@(#)$CDS: LVS.exe version 5.1.0 06/20/2007 02:10 (cicln03) $

Command line: /usr/Cadence/tools.lnx86/dfII/bin/32bit/LVS.exe -dir /home/avlsi9/Group9_n/LVS -l -s -t /home/avlsi9/Group9_n/LVS/layout /home/avlsi9/Group9_n/LVS/schemat
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

    Net-list summary for /home/avlsi9/Group9_n/LVS/layout/netlist
       count
        221             nets
        33              terminals
        214             pmos
        214             nmos

    Net-list summary for /home/avlsi9/Group9_n/LVS/schematic/netlist
       count
        221             nets
        33              terminals
        214             pmos
        214             nmos


    Terminal correspondence points
    N131        N19         CLK
    N206        N33         D0
    N72         N15         D1
    N93         N30         D2
    N2          N2          D3
    N86         N23         D4
    N67         N9          D5
    N9          N12         D6
    N186        N20         D7
    N114        N42         Q0
    N43         N26         Q1
    N180        N13         Q2
    N71         N17         Q3
    N146        N27         Q4
    N70         N14         Q5
    N66         N8          Q6
    N167        N4          Q7
    N217        N43         QB0
    N122        N6          QB1
    N148        N28         QB2
    N7          N11         QB3
    N41         N24         QB4
    N75         N18         QB5
    N171        N5          QB6
    N159        N38         QB7
    N50         N32         R
    N107        N37         S0
    N149        N34         S1
    N88         N25         S2
    N136        N21         SL
    N62         N7          SR
    N28         N1          gnd!
    N1          N0          vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        nfet pfet nmos4 pmos4 cap

The net-lists match.

                               layout  schematic
                                  instances
        un-matched                0       0
        rewired                   0       0
        size errors               0       0
        pruned                    0       0
        active                    428     428
        total                     428     428

                                    nets
        un-matched                0       0
        merged                    0       0
        pruned                    0       0
        active                    221     221
        total                     221     221

                                  terminals
        un-matched                0       0
        matched but
        different type            0       0
        total                     33      33


Probe files from /home/avlsi9/Group9_n/LVS/schematic

devbad.out:
```

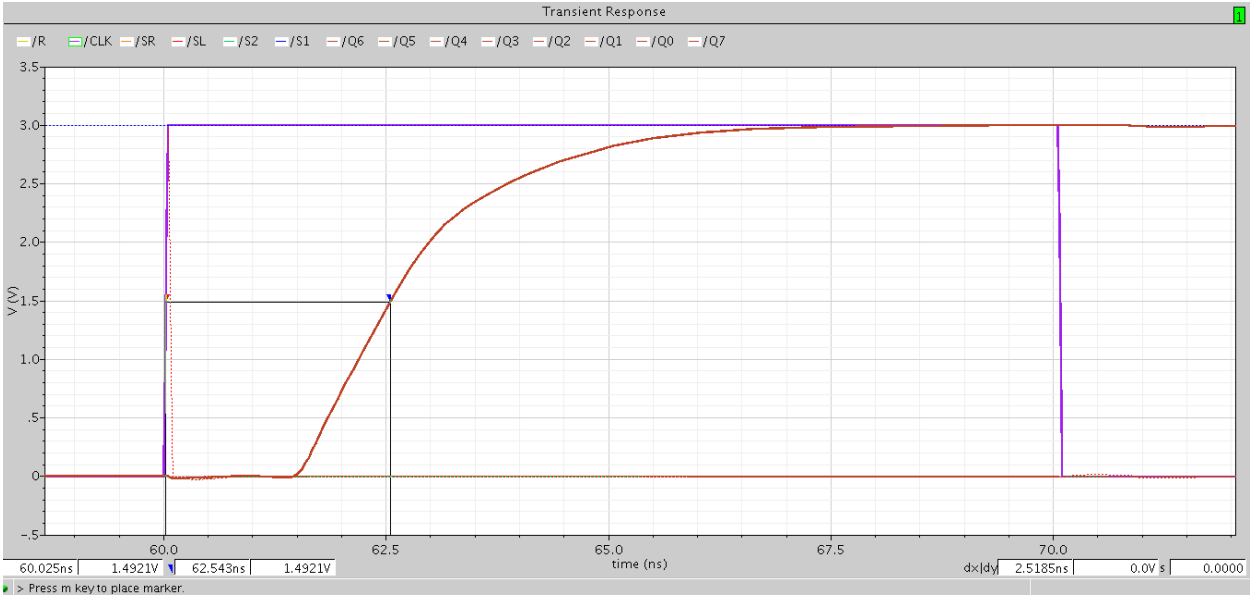
Truth Table for Shift Register:

S2	S1	S0	Function	Delay (ns)
0	0	X	Parallel Load	2.489
0	1	0	Shift Right	2.5185
0	1	1	Rotate Right	2.7024
1	0	0	Shift Left	2.412
1	0	1	Rotate Left	2.7231
1	1	X	Set (data output bit go to 1)	2.532
X	X	X	Reset (When Reset =1, all data output goes to zero)	

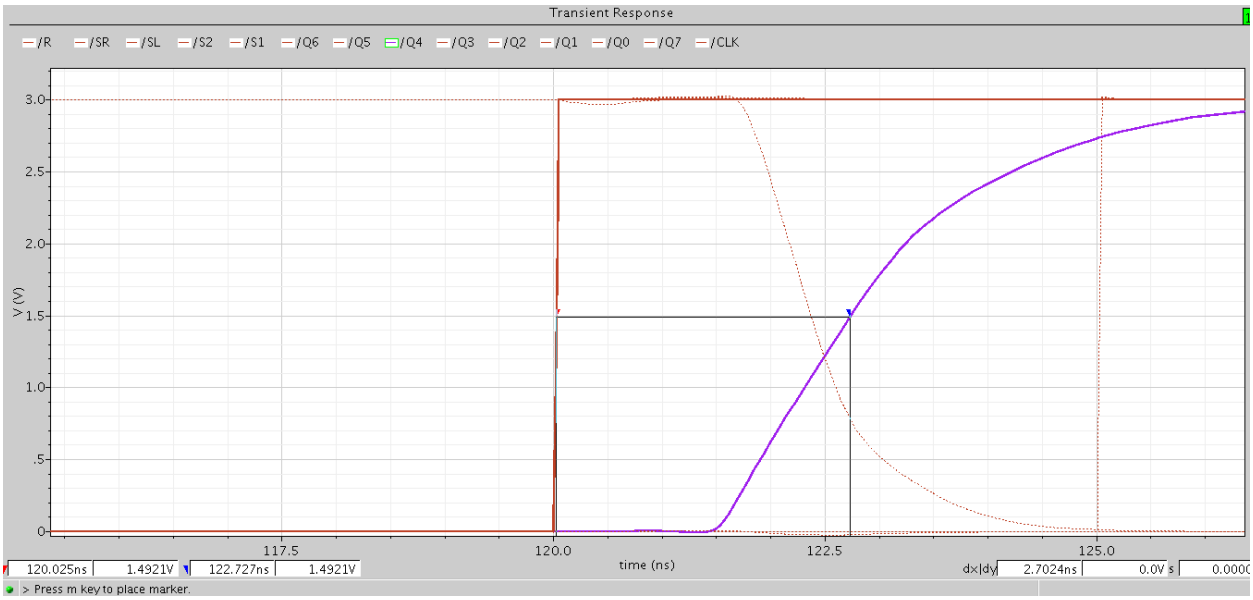
Delay for State 000:



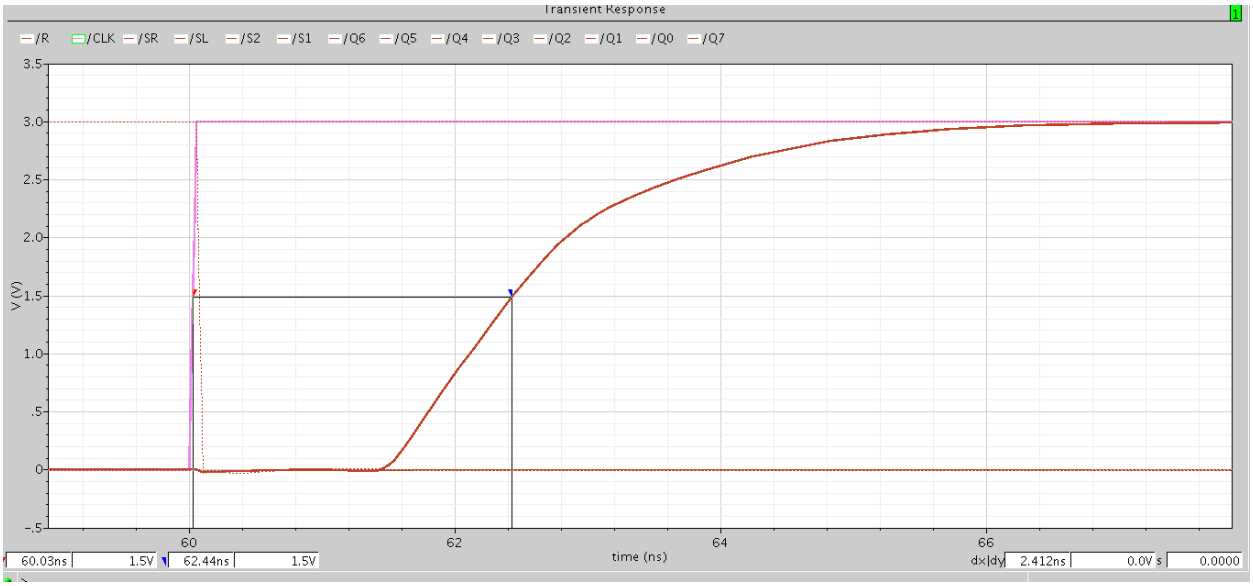
Delay for State 010:



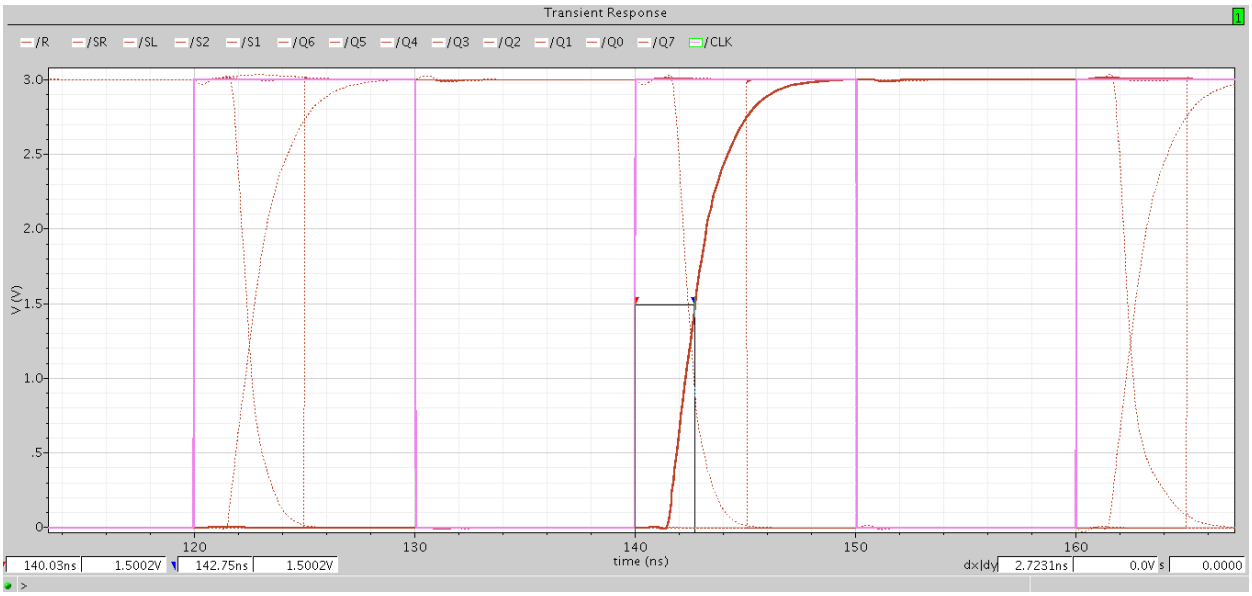
Delay for State 011:



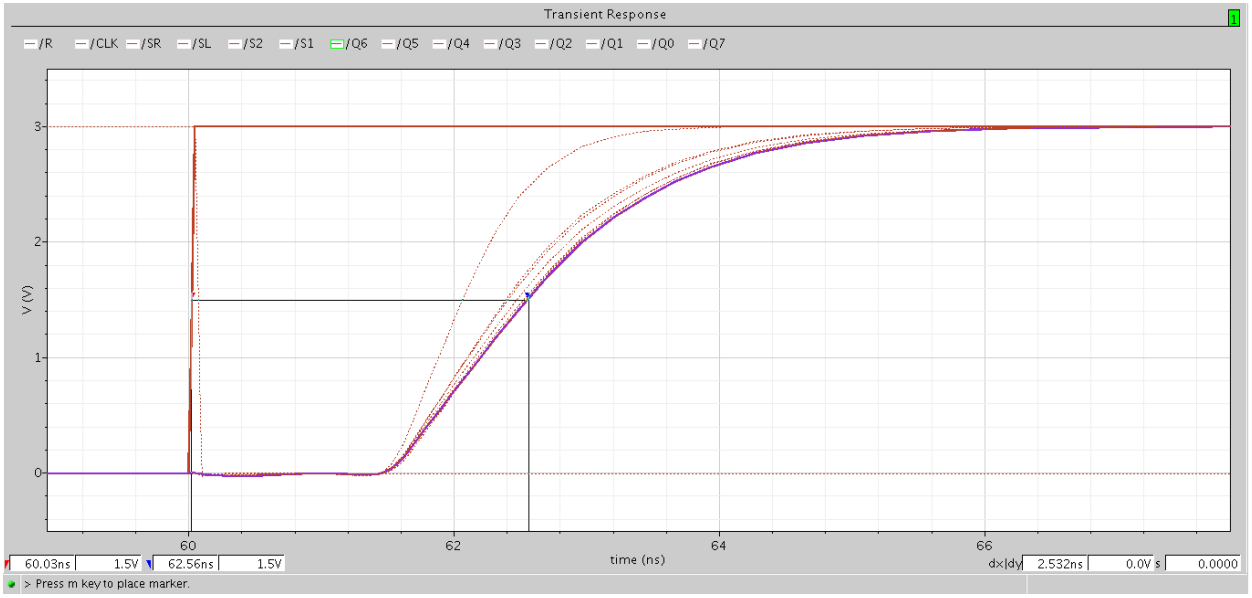
Delay for State 100:



Delay for State 101:

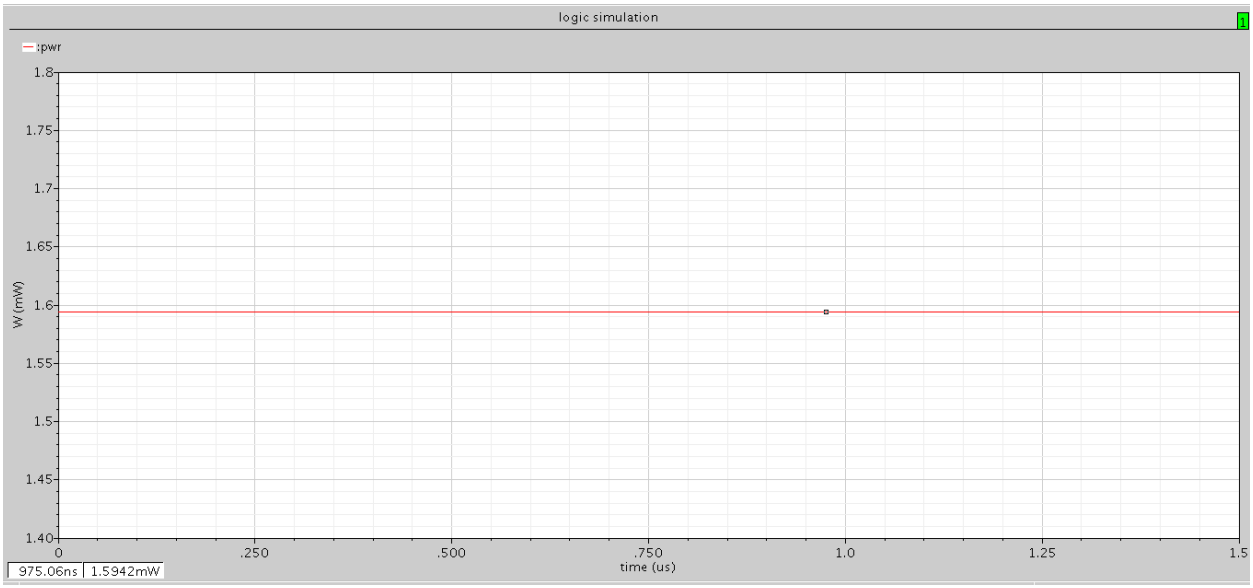


Delay for State 110:

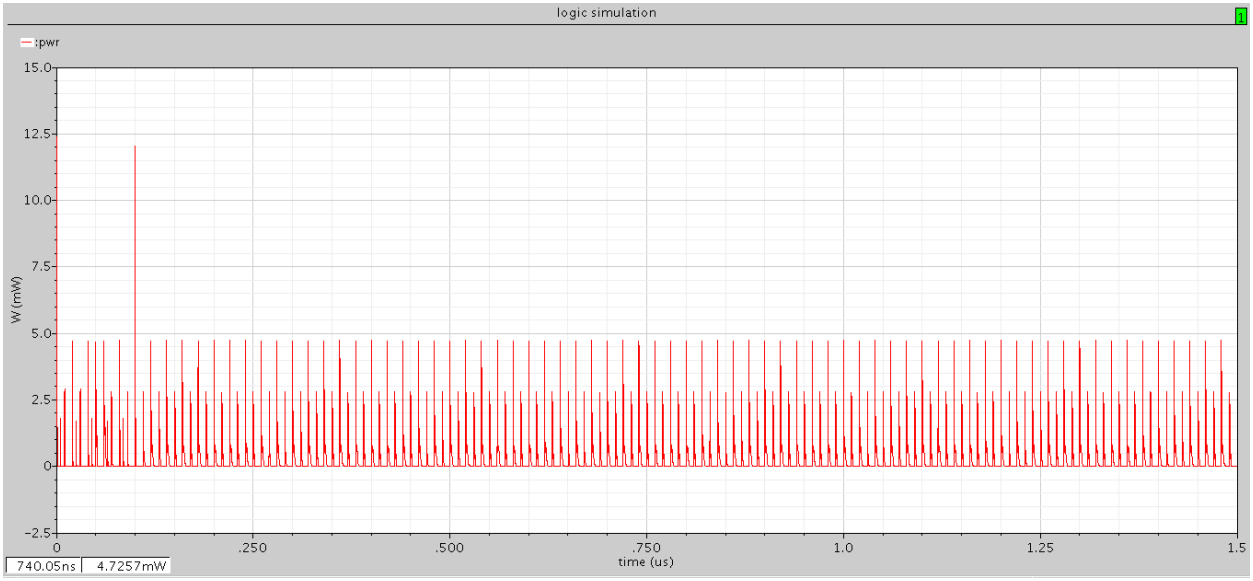


POWER MEASUREMENT:

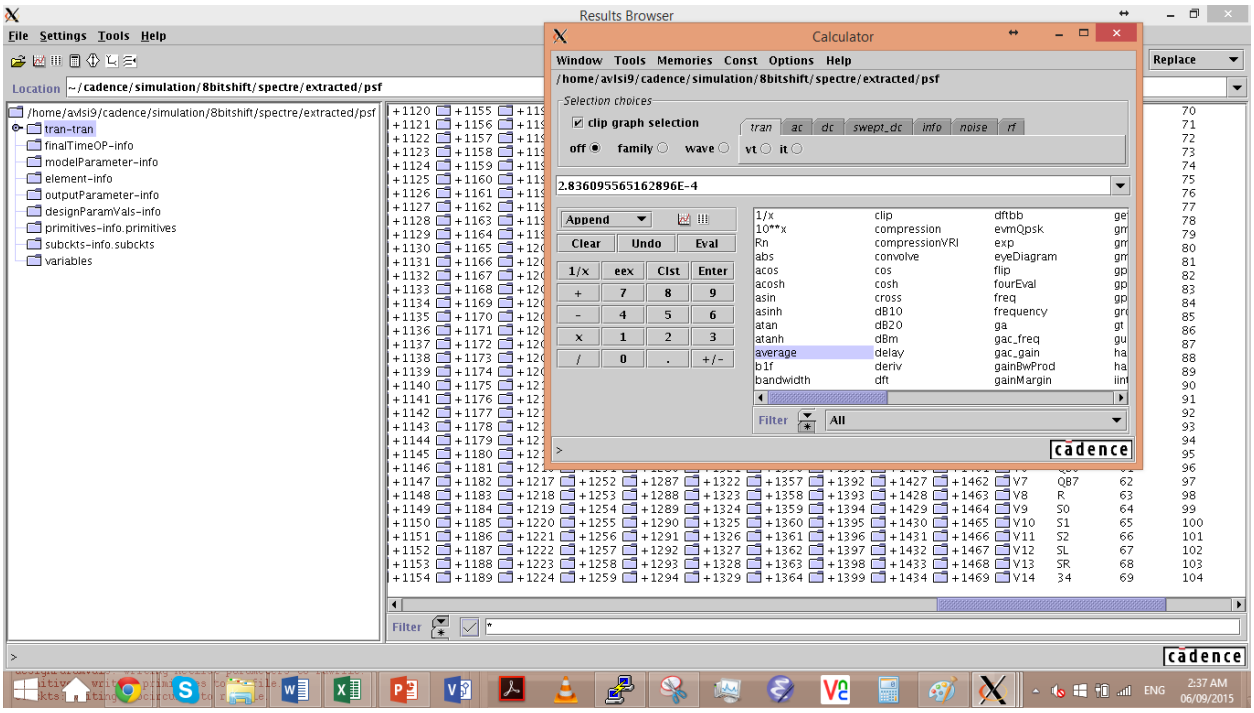
Static Power:



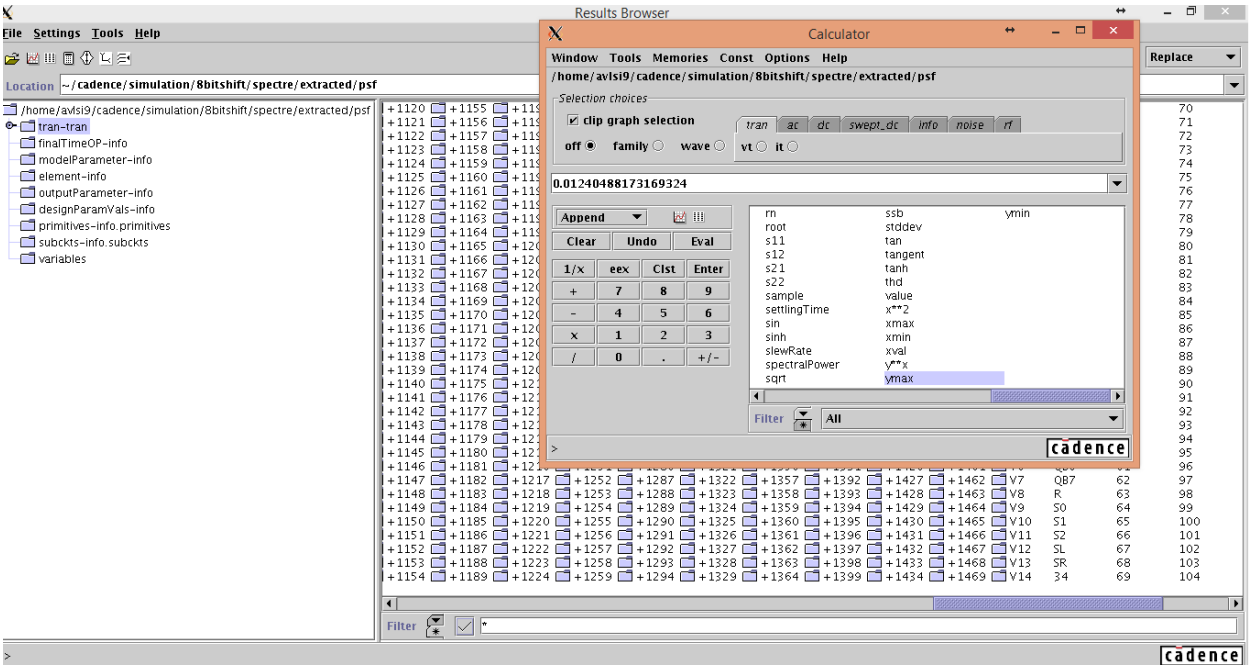
Transient Power/ Dynamic Power:



Average Power :(2.8369 E-4)

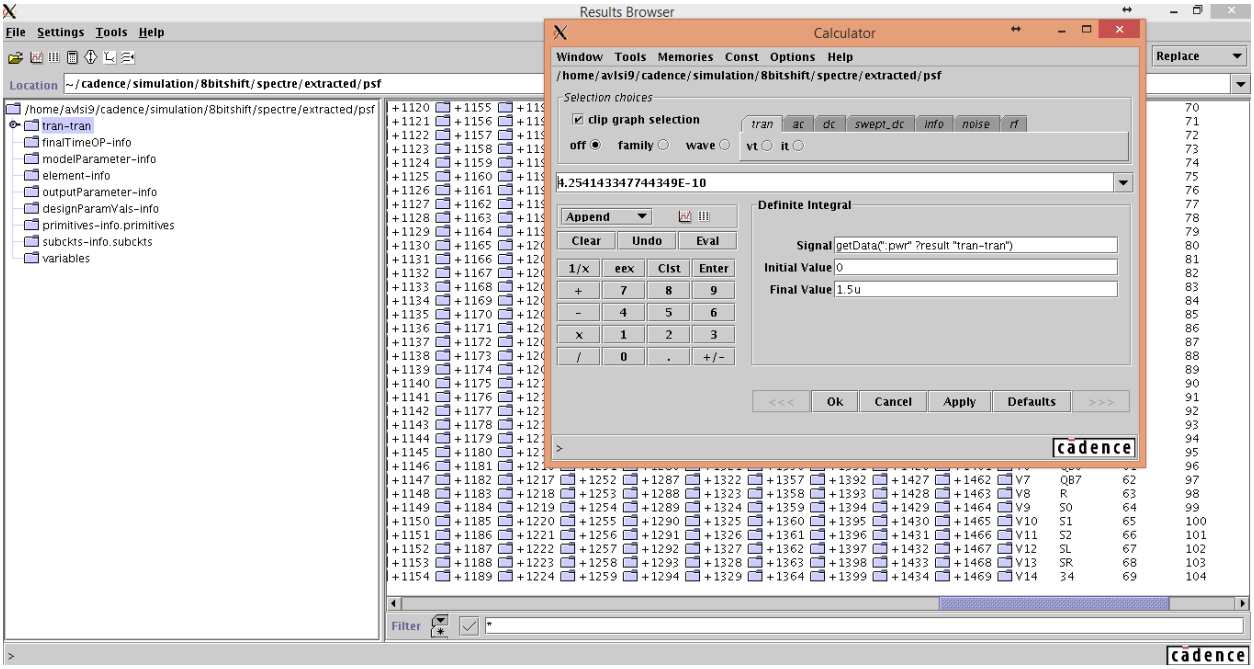


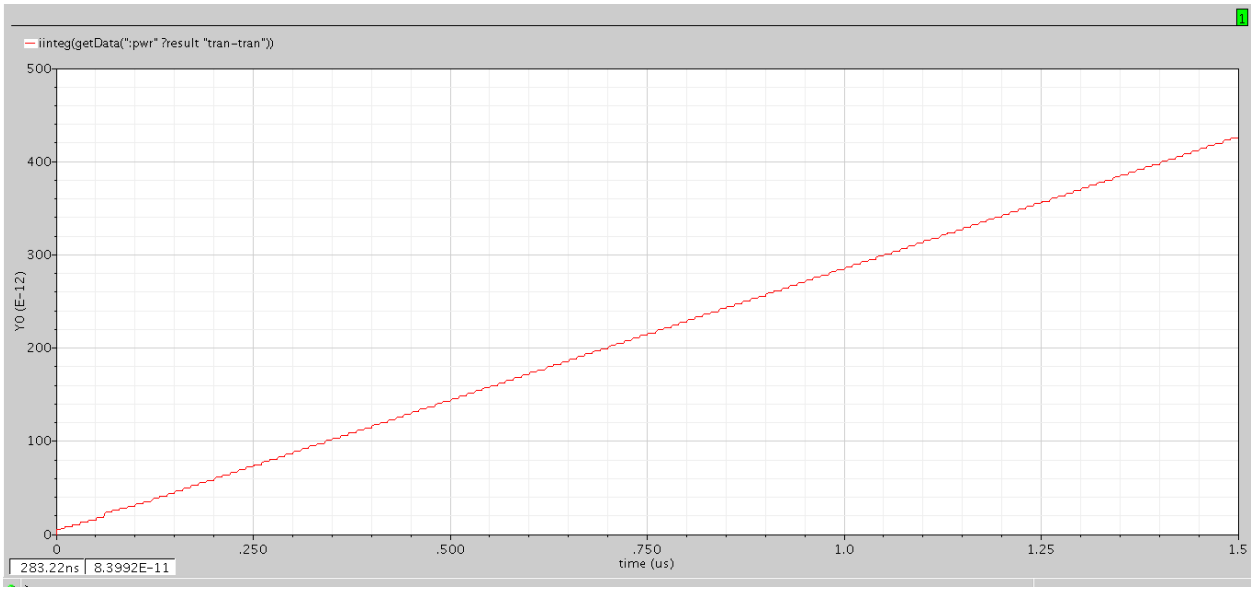
Peak Power: (0.0124)



Energy Consumption:

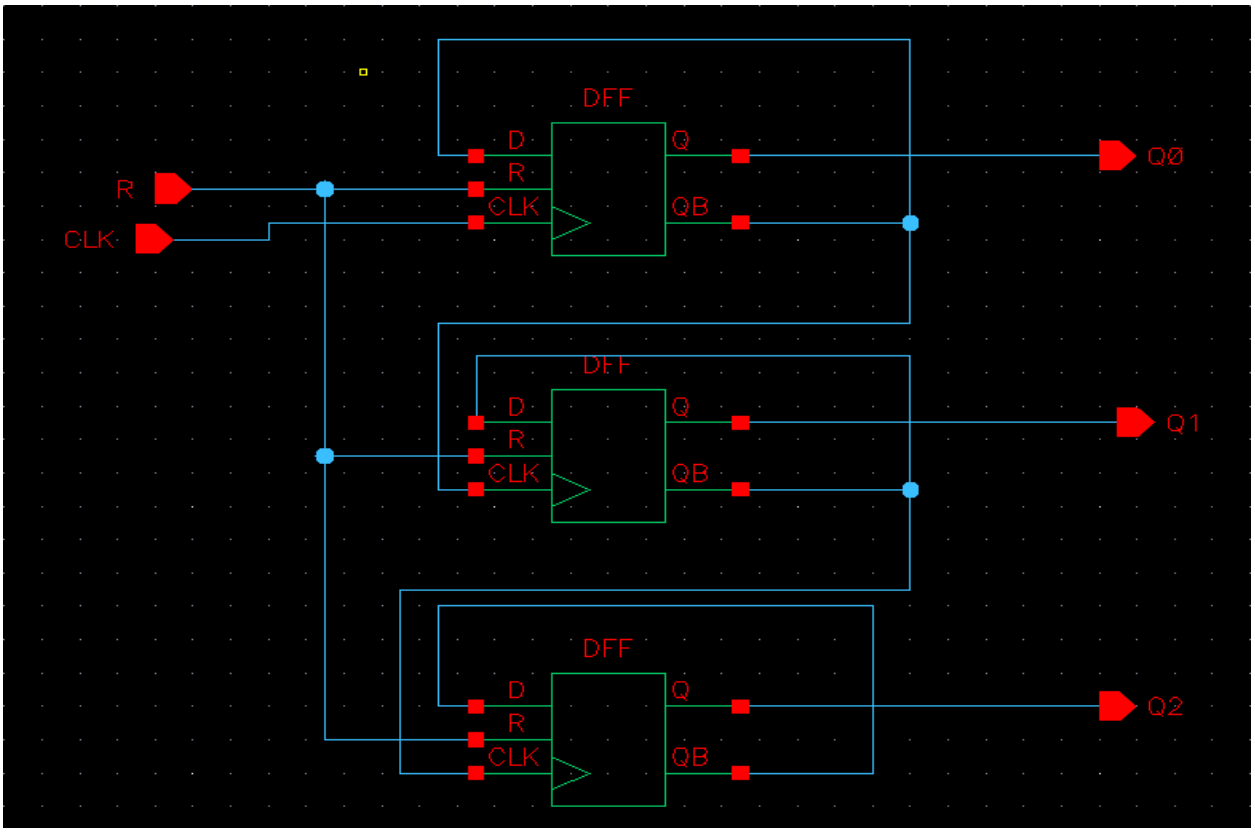
For T=0 → 1.5us =>4.25414E-10



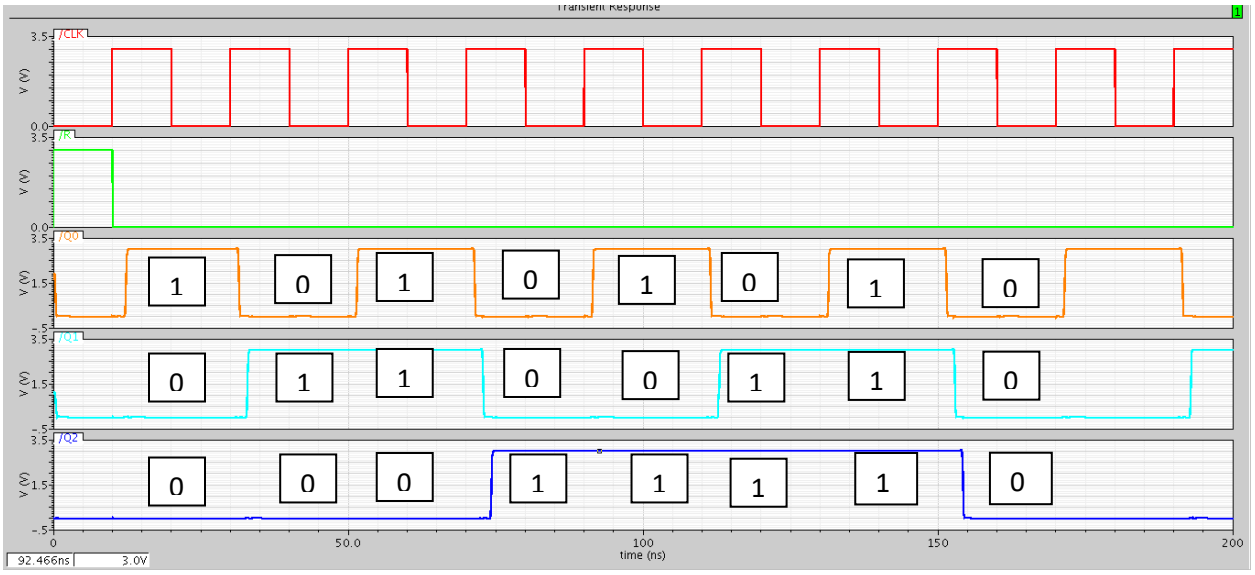


Extra Credit:

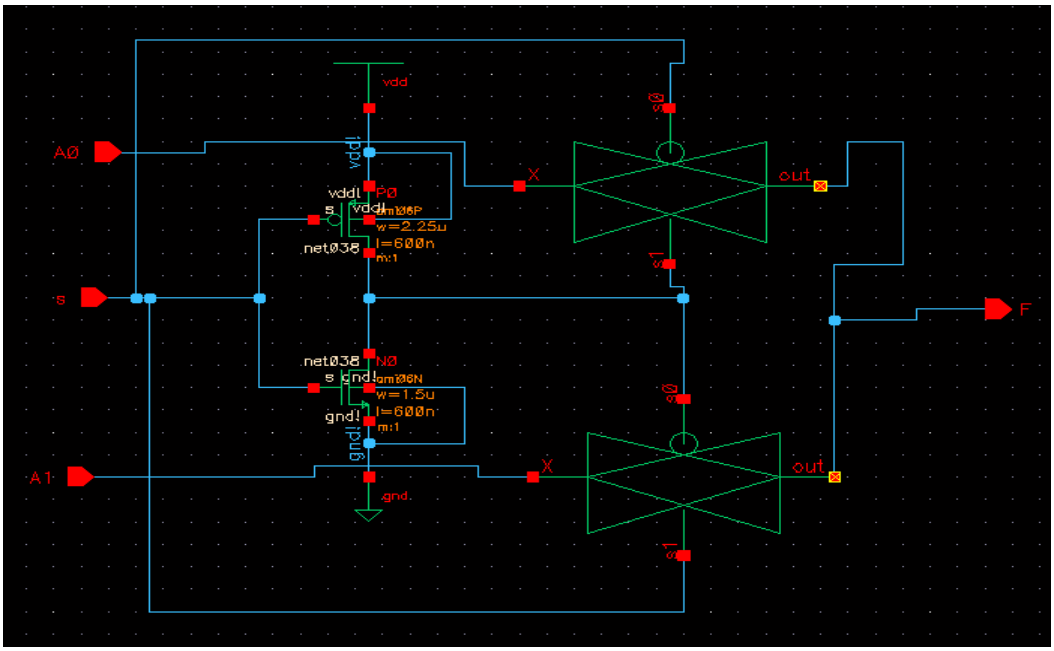
SCHEMATICS OF COUNTER:



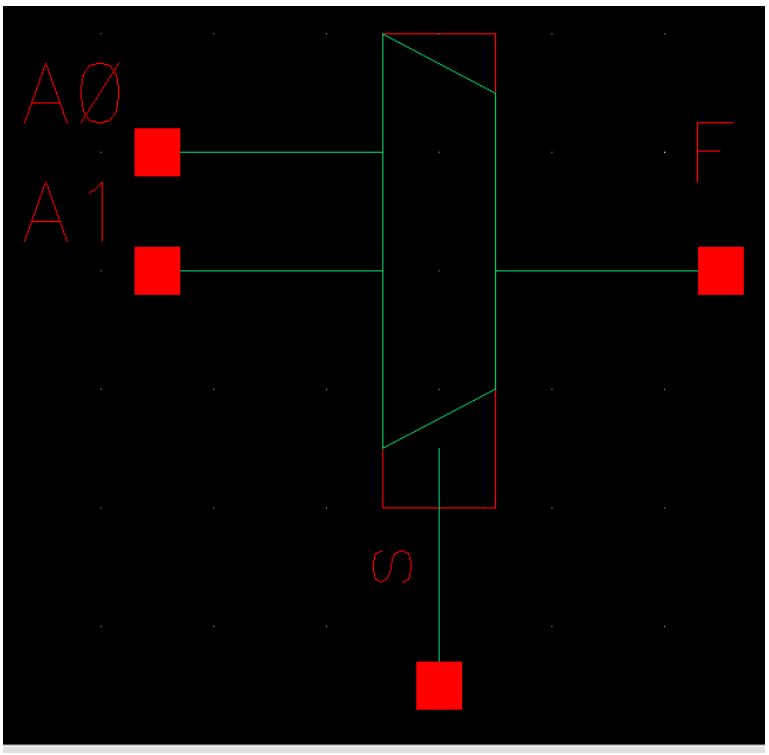
SIMULATION RESULTS OF COUNTER:



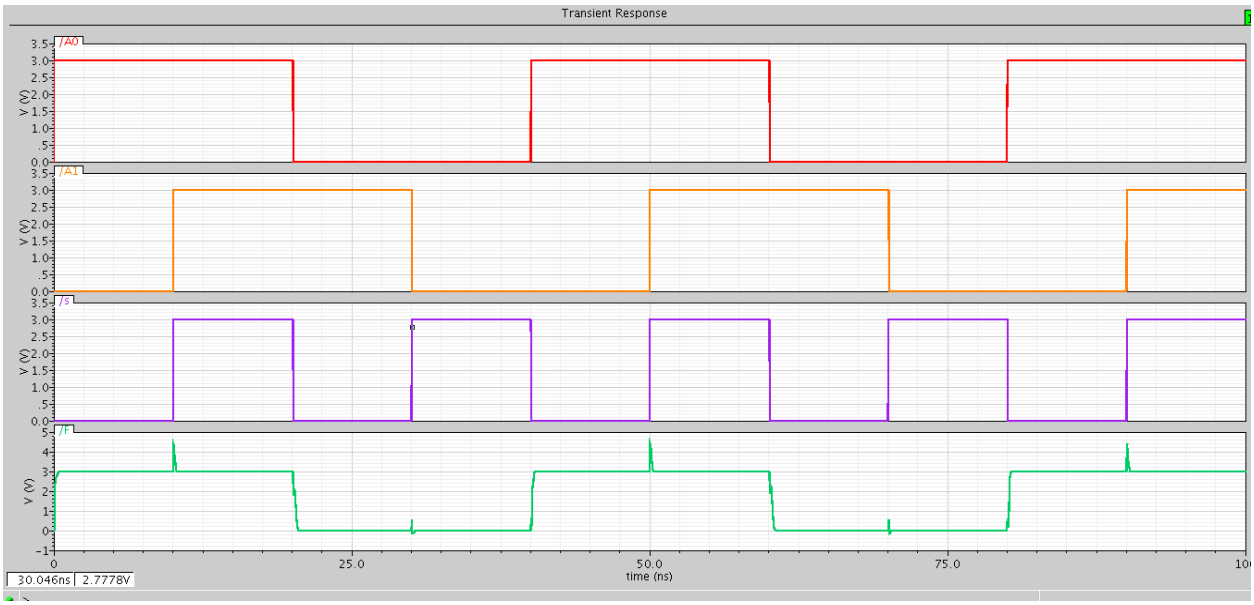
SCHEMATICS OF 2X1 MUX:



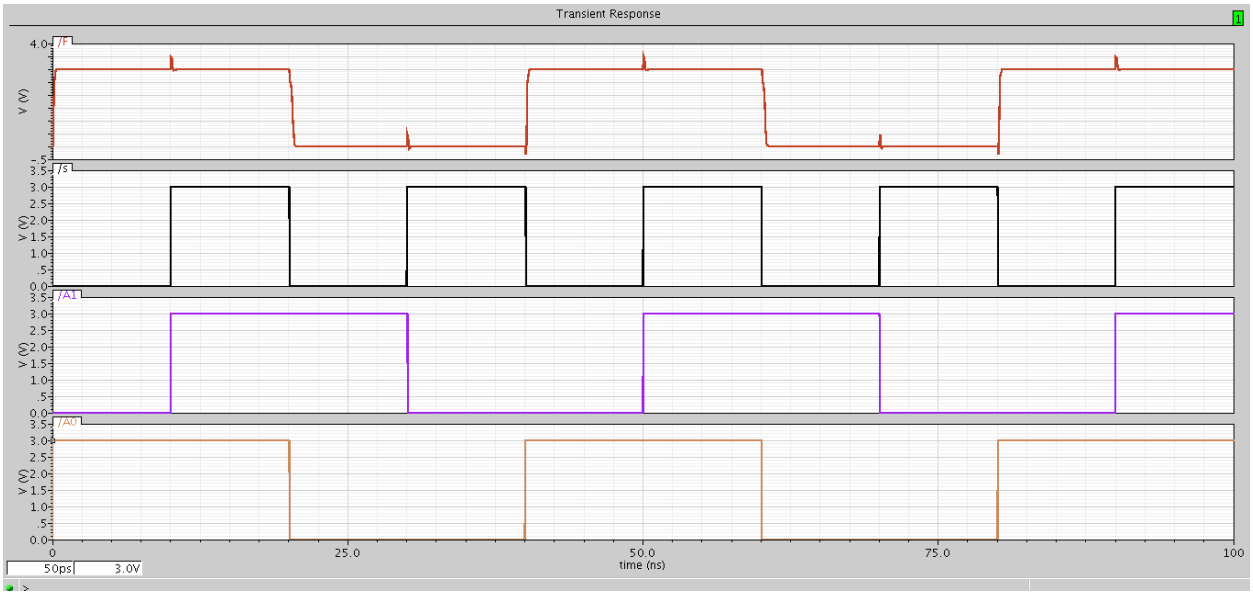
SYMBOL OF 2X1 MUX:



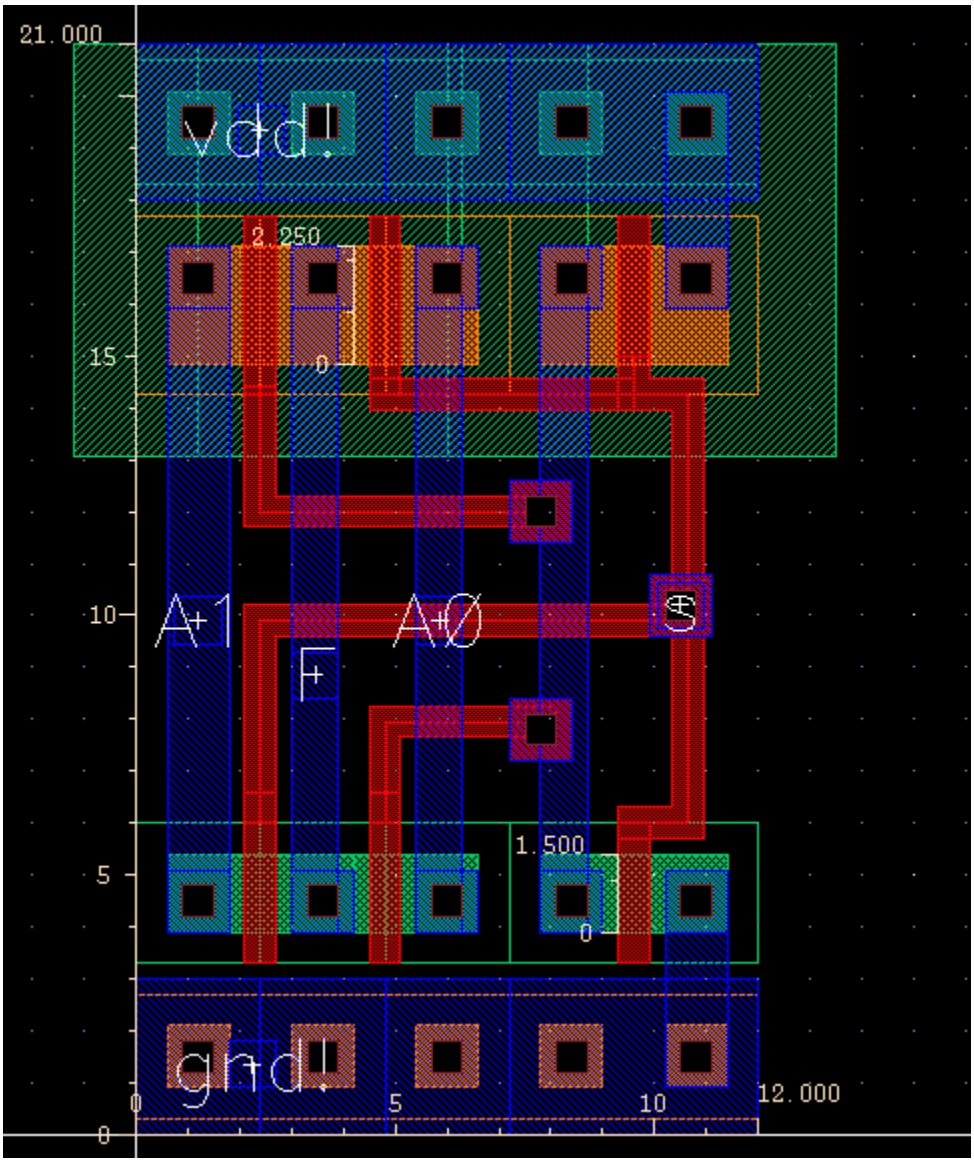
Simulation of Schematics of MUX 2x1:



Post Layout (Extracted) Simulation of MUX 2x1:



LAYOUT OF 2X1 MUX:



Widths of NMOS = 1.500

Widths of PMOS = 2.250

LVS OF 2X1 MUX:

```
@(#)$CDS: LVS.exe version 5.1.0 06/20/2007 02:10 (cicln03) $

Command line: /usr/Cadence/tools.lnx86/dfII/bin/32bit/LVS.exe -dir /home/avlsi9/Group9_n/LVS -l -s -t /home/avlsi9/Grou
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

    Net-list summary for /home/avlsi9/Group9_n/LVS/layout/netlist
       count
         7               nets
         6               terminals
         3               pmos
         3               nmos

    Net-list summary for /home/avlsi9/Group9_n/LVS/schematic/netlist
       count
         7               nets
         6               terminals
         3               pmos
         3               nmos


    Terminal correspondence points
    N6          N8          A0
    N5          N6          A1
    N0          N2          F
    N2          N1          gnd!
    N3          N4          s
    N1          N0          vdd!

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        nfet pfet nmos4 pmos4 cap

The net-lists match.

                              layout  schematic
```

LVS OF Transmission Gate:

```
@(#)$CDS: LVS.exe version 5.1.0 06/20/2007 02:10 (cicln03) $

Command line: /usr/Cadence/tools.lnx86/dfII/bin/32bit/LVS.exe -dir /home/avlsi9/Group9_n/LVS -l -s -t /home/avlsi9/Group9_n/LVS/layout /home/avlsi9/Group9_n/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.

    Net-list summary for /home/avlsi9/Group9_n/LVS/layout/netlist
       count
         6               nets
         4               terminals
         1               pmos
         1               nmos

    Net-list summary for /home/avlsi9/Group9_n/LVS/schematic/netlist
       count
         6               nets
         6               terminals
         1               pmos
         1               nmos


    Terminal correspondence points
    N2          N6          X
    N5          N7          out
    N3          N5          s0
    N1          N4          s1

Devices in the netlist but not in the rules:
        pcapacitor
Devices in the rules but not in the netlist:
        nfet pfet nmos4 pmos4 cap

The net-lists match.

                             layout  schematic
                               instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                 2       2
        total                  2       2

                                 nets
        un-matched             0       0
```

Discussion Topics:

Q1.) Is the DFFR a positive-edge-triggered for negative-edge-triggered FF? Briefly describe the hold time for a d-type flip flop and estimate its value.

The DFFR that was used in LAB was positive edge triggered. Hold time is the time after the clock edge has occurred for which the data on register input must not change. Mux based DFFR has zero hold time. In Mux based DFFR, the input D on MUX based negative latch doesn't change when positive clock edge has occurred. i.e. the first mux is holding the value. Thus no hold time exists.

Q2.) Briefly define two of the rules for multi-cell layouts that you feel are most important.

1. VDD and ground are used in a fashion that they are common for two rows. To accomplish this, we can label each VDD and ground individually and join these using virtual connections. In this way single rail is not needed in cells.
2. It is preferable to have VDD/ground within a cell physically joined together. This requires the knowledge if high level hierarchy.

Q3.) Briefly discuss the worst-case function of the shift register. Is it what you expected? Why or why not?

Worst case function of shift register is rotate left/right. This is same as what we expected because the values require the longest path for rotation in any of rotate operation whether left or right.

Q4.) Briefly discuss the pros and cons of the asynchronous counter verses a synchronous counter.

• Asynchronous counter: Asynchronous counter is a serial counter i.e. the input signal is applied to the clock input of the first FF, and the output of each FF is connected directly to the clock input of the next.

• Synchronous counter: Synchronous counters are parallel counters since all flip-flops are controlled by a common clock. Logic gates between each stage of the circuit control dataflow from stage to stage so that the desired count behaviour is realized.

The pros and cons are as shown in the table:

	Asynchronous	**Synchronous**
Circuit	The logic circuit of this type of counters is simple to design and we feed output of one FF to clock of next FF	The circuit diagram for type of counter becomes difficult as number of states increase in the counter
Propagation Time	Propagation time delay of this type of counter is : Tp = N * (Delay of 1 FF) which is quiet high N is number of FFS	Propagation time delay of this type of counter is: Tp = (Delay of 1 FF)
Maximum operating frequency	And hence operating frequency is Low	And hence operating frequency is Higher

Q5.) A 2:1 MUX could be implemented with 2 AND logic gates and 1 NOR logic gate. How many transistors would this require for a CMOS implementation? Compare this to the number of transistors required for the transmission gate implementation.

Single AND/OR gate is implemented by six transistors. Thus a mux requires2 AND gates, one OR gate and one NOT gate. Which makes a total of 20 transistor. For CMOS implementation we need 4 transistor of Pull Up logic and 4 resistor for pull down and 2 for not gate. Thus for CMOS implementation a total of 10transistors are required. While when using transmission gate, total of 6 transistors are required. (4 for transmission gate, 2 for NOT gate).

Q6.) What layout widths (as defined in Lab 2) did you achieve for the MUX21?

In 2 to 1 MUX the acquired width in design is 12um.While PMOS width is 2.25um and NMOS width is 1.5um