

**Preview - temp\_summary.pdf**

**Resource Usage Report for Ripple Carry Adder**

### Parameter Value: 1

Module	wire_count	port_count	wire_bits	cell_count	port_bits	hierarchy_depth	\$_XOR_	full_adder	\$_OR_	half_adder	\$_AND_
full_adder	8	5	8	3	5	1	2	0	1	2	2
full_adder -> half_adder	4	4	4	2	4	0	1	0	0	0	1
half_adder	4	4	4	2	4	0	1	0	0	0	1
ripple_carry_adder	6	5	10	2	8	2	4	2	2	0	4
ripple_carry_adder -> full_adder	8	5	8	3	5	1	2	0	1	2	2

### Parameter Value: 2

Module	wire_count	port_count	wire_bits	cell_count	port_bits	hierarchy_depth	\$_XOR_	full_adder	\$_OR_	half_adder	\$_AND_
full_adder	8	5	8	3	5	1	2	0	1	2	2
full_adder -> half_adder	4	4	4	2	4	0	1	0	0	0	1
half_adder	4	4	4	2	4	0	1	0	0	0	1
ripple_carry_adder	6	5	10	2	8	2	6	3	3	0	6
ripple_carry_adder -> full_adder	8	5	8	3	5	1	2	0	1	2	2

### Parameter Value: 3

Module	wire_count	port_count	wire_bits	cell_count	port_bits	hierarchy_depth	\$_XOR_	full_adder	\$_OR_	half_adder	\$_AND_
full_adder	8	5	8	3	5	1	2	0	1	2	2
full_adder -> half_adder	4	4	4	2	4	0	1	0	0	0	1
half_adder	4	4	4	2	4	0	1	0	0	0	1
ripple_carry_adder	6	5	10	2	8	2	8	4	4	0	8
ripple_carry_adder -> full_adder	8	5	8	3	5	1	2	0	1	2	2

### Parameter Value: 4

Module	wire_count	port_count	wire_bits	cell_count	port_bits	hierarchy_depth	\$_XOR_	full_adder	\$_OR_	half_adder	\$_AND_
full_adder	8	5	8	3	5	1	2	0	1	2	2
full_adder -> half_adder	4	4	4	2	4	0	1	0	0	0	1
half_adder	4	4	4	2	4	0	1	0	0	0	1
ripple_carry_adder	6	5	10	2	8	2	10	5	5	0	10
ripple_carry_adder -> full_adder	8	5	8	3	5	1	2	0	1	2	2

### Parameter Value: 5

Module	wire_count	port_count	wire_bits	cell_count	port_bits	hierarchy_depth	\$_XOR_	full_adder	\$_OR_	half_adder	\$_AND_
full_adder	8	5	8	3	5	1	2	0	1	2	2
full_adder -> half_adder	4	4	4	2	4	0	1	0	0	0	1
half_adder	4	4	4	2	4	0	1	0	0	0	1
ripple_carry_adder	6	5	10	2	8	2	12	6	6	0	12
ripple_carry_adder -> full_adder	8	5	8	3	5	1	2	0	1	2	2

### Parameter Value: 6

Module	wire_count	port_count	wire_bits	cell_count	port_bits	hierarchy_depth	\$_XOR_	full_adder	\$_OR_	half_adder	\$_AND_
full_adder	8	5	8	3	5	1	2	0	1	2	2
full_adder -> half_adder	4	4	4	2	4	0	1	0	0	0	1
half_adder	4	4	4	2	4	0	1	0	0	0	1
ripple_carry_adder	6	5	10	2	8	2	14	7	7	0	14
ripple_carry_adder -> full_adder	8	5	8	3	5	1	2	0	1	2	2

### Parameter Value: 7

Module	wire_count	port_count	wire_bits	cell_count	port_bits	hierarchy_depth	\$_XOR_	full_adder	\$_OR_	half_adder	\$_AND_
full_adder	8	5	8	3	5	1	2	0	1	2	2
full_adder -> half_adder	4	4	4	2	4	0	1	0	0	0	1
half_adder	4	4	4	2	4	0	1	0	0	0	1
ripple_carry_adder	6	5	10	2	8	2	16	8	8	0	16
ripple_carry_adder -> full_adder	8	5	8	3	5	1	2	0	1	2	2

### Parameter Value: 8

Module	wire_count	port_count	wire_bits	cell_count	port_bits	hierarchy_depth	\$_XOR_	full_adder	\$_OR_	half_adder	\$_AND_
full_adder	8	5	8	3	5	1	2	0	1	2	2
full_adder -> half_adder	4	4	4	2	4	0	1	0	0	0	1
half_adder	4	4	4	2	4	0	1	0	0	0	1
ripple_carry_adder	6	5	10	2	8	2	18	9	9	0	18
ripple_carry_adder -> full_adder	8	5	8	3	5	1	2	0	1	2	2