Preview - temp_summary.pdf

Benchmarking Report for Ripple Carry Adder

Testbench Summary

Component	Total Tests	Passed	Failed
ripple_carry_adder	2	1	1
full_adder	1	1	0
half_adder	1	0	1

Parameter N=1

Simulation completed. Results saved to generated/ripple_carry_adder/ripple_carry_adder_N1_simulation_output.txt

Test Case	Expected	Actual
a=1, b=1, cin=0	sum=0, cout=1	sum=0, cout=1

Parameter N=2

Simulation completed. Results saved to generated/ripple_carry_adder/ripple_carry_adder_N2_simulation_output.txt

Test Case	Expected	Actual
a=0, b=1, cin=1	sum=0, cout=1	sum=1, cout=0

Submodule: Full Adder

This section contains the test results for the Full Adder submodule.

Parameter N=1

Simulation completed. Results saved to generated/full_adder/full_adder_N1_simulation_output.txt

Test Case	Expected	Actual
a=1, b=0, cin=0	sum=1, cout=0	sum=1, cout=0

Submodule: Half Adder

This section contains the test results for the Half Adder submodule.

Parameter N=1

Simulation completed. Results saved to generated/half_adder/half_adder_N1_simulation_output.txt

Test Case	Expected	Actual
a=1, b=1	sum=0, cout=1	sum=1, cout=0

Failed test cases:

Test 1: Expected: [sum=0, cout=1], Actual: [sum=1, cout=0]

Total tests: 8

Passed tests: 8

Failed tests: 0

Test Case	Input a	Input b	Input cin	Output sum (Actual)	Expected sum	Output cout (Actual)	Expected cout	Status
0	1 (bin) / 1 (dec)	1 (bin) / 1 (dec)	1 (bin) / 1 (dec)	1 (bin) / 1 (dec)	1 (dec)	1 (bin) / 1 (dec)	1 (dec)	Passed
1	1 (bin) / 1 (dec)	0 (bin) / 0 (dec)	0 (bin) / 0 (dec)	1 (bin) / 1 (dec)	1 (dec)	0 (bin) / 0 (dec)	0 (dec)	Passed
2	0 (bin) / 0 (dec)	0 (bin) / 0 (dec)	0 (bin) / 0 (dec)	0 (bin) / 0 (dec)	0 (dec)	0 (bin) / 0 (dec)	0 (dec)	Passed
3	1 (bin) / 1 (dec)	1 (bin) / 1 (dec)	1 (bin) / 1 (dec)	1 (bin) / 1 (dec)	1 (dec)	1 (bin) / 1 (dec)	1 (dec)	Passed
4	1 (bin) / 1 (dec)	1 (bin) / 1 (dec)	1 (bin) / 1 (dec)	1 (bin) / 1 (dec)	1 (dec)	1 (bin) / 1 (dec)	1 (dec)	Passed
5	1 (bin) / 1 (dec)	0 (bin) / 0 (dec)	1 (bin) / 1 (dec)	0 (bin) / 0 (dec)	0 (dec)	1 (bin) / 1 (dec)	1 (dec)	Passed
6	0 (bin) / 0 (dec)	1 (bin) / 1 (dec)	0 (bin) / 0 (dec)	1 (bin) / 1 (dec)	1 (dec)	0 (bin) / 0 (dec)	0 (dec)	Passed
7	0 (bin) / 0 (dec)	1 (bin) / 1 (dec)	0 (bin) / 0 (dec)	1 (bin) / 1 (dec)	1 (dec)	0 (bin) / 0 (dec)	0 (dec)	Passed

Logs

Simulation started for component full_adder

Simulation completed successfully for component full_adder

All tests passed for component full_adder

Error: Simulation failed for component half_adder