

**Preview - temp\_summary.pdf**

**Resource Usage Report for skip\_logic**

Parameter Value: 1

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_
skip_logic	11	9	13	5	0	19	2	4	2	1	2	4	2	1

Parameter Value: 2

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_
skip_logic	11	9	13	5	0	19	2	4	2	1	2	4	2	1

Parameter Value: 3

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_
skip_logic	11	9	13	5	0	19	2	4	2	1	2	4	2	1

Parameter Value: 4

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_
skip_logic	11	9	13	5	0	19	2	4	2	1	2	4	2	1

Parameter Value: 5

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_
skip_logic	11	9	13	5	0	19	2	4	2	1	2	4	2	1

Parameter Value: 6

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_
skip_logic	11	9	13	5	0	19	2	4	2	1	2	4	2	1

Parameter Value: 7

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_
skip_logic	11	9	13	5	0	19	2	4	2	1	2	4	2	1

Parameter Value: 8

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_	\$_ORNOT_	\$_NOR_	\$_OR_	\$_ANDNOT_
skip_logic	11	9	13	5	0	19	2	4	2	1	2	4	2	1