

Preview - temp_summary.pdf

Resource Usage Report for carry_select_adder

Parameter Value: 1

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_XOR_	\$_AND_	\$_MUX_	full_adder	half_adder	\$_OR_	\$_OR_	\$_XOR_	\$_AND_	\$_MUX_
carry_select_adder	26	25	9	5	2	60	32	32	9	16	0	16	16	32	32	9
carry_select_adder -> full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder -> half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0
half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0

Parameter Value: 2

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_XOR_	\$_AND_	\$_MUX_	full_adder	half_adder	\$_OR_	\$_OR_	\$_XOR_	\$_AND_	\$_MUX_
carry_select_adder	26	25	9	5	2	60	32	32	9	16	0	16	16	32	32	9
carry_select_adder -> full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder -> half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0
half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0

Parameter Value: 3

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_XOR_	\$_AND_	\$_MUX_	full_adder	half_adder	\$_OR_	\$_OR_	\$_XOR_	\$_AND_	\$_MUX_
carry_select_adder	26	25	9	5	2	60	32	32	9	16	0	16	16	32	32	9
carry_select_adder -> full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder -> half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0
half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0

Parameter Value: 4

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_XOR_	\$_AND_	\$_MUX_	full_adder	half_adder	\$_OR_	\$_OR_	\$_XOR_	\$_AND_	\$_MUX_
carry_select_adder	26	25	9	5	2	60	32	32	9	16	0	16	16	32	32	9
carry_select_adder -> full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder -> half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0
half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0

Parameter Value: 5

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_XOR_	\$_AND_	\$_MUX_	full_adder	half_adder	\$_OR_	\$_OR_	\$_XOR_	\$_AND_	\$_MUX_
carry_select_adder	26	25	9	5	2	60	32	32	9	16	0	16	16	32	32	9
carry_select_adder -> full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder -> half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0
half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0

Parameter Value: 6

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_XOR_	\$_AND_	\$_MUX_	full_adder	half_adder	\$_OR_	\$_OR_	\$_XOR_	\$_AND_	\$_MUX_
carry_select_adder	26	25	9	5	2	60	32	32	9	16	0	16	16	32	32	9
carry_select_adder -> full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder -> half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0
half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0

Parameter Value: 7

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_XOR_	\$_AND_	\$_MUX_	full_adder	half_adder	\$_OR_	\$_OR_	\$_XOR_	\$_AND_	\$_MUX_
carry_select_adder	26	25	9	5	2	60	32	32	9	16	0	16	16	32	32	9
carry_select_adder -> full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder -> half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0
half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0

Parameter Value: 8

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_XOR_	\$_AND_	\$_MUX_	full_adder	half_adder	\$_OR_	\$_OR_	\$_XOR_	\$_AND_	\$_MUX_
carry_select_adder	26	25	9	5	2	60	32	32	9	16	0	16	16	32	32	9
carry_select_adder -> full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder	5	3	8	5	1	8	2	2	0	0	2	1	1	2	2	0
full_adder -> half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0
half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	1	1	0