Resource Usage Report for Ripple Carry Adder

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Resource Usage Analysis for ripple_carry_adder

Parameter Value: 1

| ule | port_bits | cell_count | wire_count | port_count | hierarchy_depth | wire_bits | \$_XOR_ | \$_AND_ | full_adder | half_adder | \$_OR_ | \$_XOR_ |
|------------------|-----------|------------|------------|------------|-----------------|-----------|---------|---------|------------|------------|--------|---------|
| dder | 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 |
| half_adder | 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 |
| dder | 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 |
| y_adder | 8 | 2 | 6 | 5 | 2 | 10 | 4 | 4 | 2 | 0 | 2 | 4 |
| er -> full_adder | 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 |

| ule | port_bits | cell_count | wire_count | port_count | hierarchy_depth | wire_bits | \$_XOR_ | \$_AND_ | full_adder | half_adder | \$_OR_ | \$_XOR_ \$ |
|------------------|-----------|------------|------------|------------|-----------------|-----------|---------|---------|------------|------------|--------|------------|
| dder | 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 |
| half_adder | 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 |
| dder | 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 |
| y_adder | 8 | 2 | 6 | 5 | 2 | 10 | 6 | 6 | 3 | 0 | 3 | 6 |
| er -> full_adder | 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 |
| | | | | | | | | | | | | |

Parameter Value: 3

| ule | port_bits | cell_count | wire_count | port_count | hierarchy_depth | wire_bits | \$_XOR_ | \$_AND_ | full_adder | half_adder | \$_OR_ | \$_XOR_ | \$. |
|------------------|-----------|------------|------------|------------|-----------------|-----------|---------|---------|------------|------------|--------|---------|-----|
| dder | 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 | |
| half_adder | 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 | |
| dder | 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 | |
| y_adder | 8 | 2 | 6 | 5 | 2 | 10 | 8 | 8 | 4 | 0 | 4 | 8 | |
| er -> full_adder | 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 | |

| ule | port_bits | cell_count | wire_count | port_count | hierarchy_depth | wire_bits | \$_XOR_ | \$_AND_ | full_adder | half_adder | \$_OR_ | \$_XOR_ \$ |
|------------------|-----------|------------|------------|------------|-----------------|-----------|---------|---------|------------|------------|--------|------------|
| dder | 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 |
| half_adder | 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 |
| dder | 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 |
| y_adder | 8 | 2 | 6 | 5 | 2 | 10 | 10 | 10 | 5 | 0 | 5 | 10 |
| er -> full_adder | 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 |

Parameter Value: 5

| port_bits | cell_count | wire_count | port_count | hierarchy_depth | wire_bits | \$_XOR_ | \$_AND_ | full_adder | half_adder | \$_OR_ | \$_XOR_ | \$ |
|-----------|------------|------------|------------|-----------------|-----------|---|---|---|---|---|---|-------------------------|
| 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 | |
| 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 | |
| 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 | |
| 8 | 2 | 6 | 5 | 2 | 10 | 12 | 12 | 6 | 0 | 6 | 12 | |
| 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 | |
| | 5 | 5 3 | 5 3 8 | 5 3 8 5 | 5 3 8 5 1 | 5 3 8 5 1 8 4 2 4 4 0 4 4 2 4 4 0 4 | 5 3 8 5 1 8 2 4 2 4 4 0 4 1 4 2 4 4 0 4 1 | 5 3 8 5 1 8 2 2 4 2 4 4 0 4 1 1 4 2 4 4 0 4 1 1 | 5 3 8 5 1 8 2 2 0 4 2 4 4 0 4 1 1 0 4 2 4 4 0 4 1 1 0 | 5 3 8 5 1 8 2 2 0 2 4 2 4 4 0 4 1 1 0 0 4 2 4 4 0 4 1 1 0 0 | 5 3 8 5 1 8 2 2 0 2 1 4 2 4 4 0 4 1 1 0 0 0 4 2 4 4 0 4 1 1 0 0 0 | 4 2 4 4 0 4 1 1 0 0 0 1 |

| ule | port_bits | cell_count | wire_count | port_count | hierarchy_depth | wire_bits | \$_XOR_ | \$_AND_ | full_adder | half_adder | \$_OR_ | \$_XOR_ \$ |
|------------------|-----------|------------|------------|------------|-----------------|-----------|---------|---------|------------|------------|--------|------------|
| dder | 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 |
| half_adder | 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 |
| dder | 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 |
| y_adder | 8 | 2 | 6 | 5 | 2 | 10 | 14 | 14 | 7 | 0 | 7 | 14 |
| er -> full_adder | 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 |

Parameter Value: 7

| ule | port_bits | cell_count | wire_count | port_count | hierarchy_depth | wire_bits | \$_XOR_ | \$_AND_ | full_adder | half_adder | \$_OR_ | \$_XOR_ | \$ |
|------------------|-----------|------------|------------|------------|-----------------|-----------|---------|---------|------------|------------|--------|---------|----|
| dder | 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 | |
| half_adder | 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 | |
| dder | 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 | |
| y_adder | 8 | 2 | 6 | 5 | 2 | 10 | 16 | 16 | 8 | 0 | 8 | 16 | |
| er -> full_adder | 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 | |

| port_bits | cell_count | wire_count | port_count | hierarchy_depth | wire_bits | \$_XOR_ | \$_AND_ | full_adder | half_adder | \$_OR_ | \$_XOR_ | \$ |
|-----------|------------|--|---|--|--|---|---|---|---|---|---|---|
| 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 | |
| 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 | |
| 4 | 2 | 4 | 4 | 0 | 4 | 1 | 1 | 0 | 0 | 0 | 1 | |
| 8 | 2 | 6 | 5 | 2 | 10 | 18 | 18 | 9 | 0 | 9 | 18 | |
| 5 | 3 | 8 | 5 | 1 | 8 | 2 | 2 | 0 | 2 | 1 | 2 | |
| | 5 4 4 8 5 | port_bits cell_count 5 3 4 2 4 2 8 2 5 3 | port_bits cell_count wire_count 5 3 8 4 2 4 4 2 4 8 2 6 5 3 8 | port_bits cell_count wire_count port_count 5 3 8 5 4 2 4 4 4 2 4 4 8 2 6 5 5 3 8 5 | port_bits cell_count wire_count port_count hierarchy_depth 5 3 8 5 1 4 2 4 4 0 4 2 4 4 0 8 2 6 5 2 5 3 8 5 1 | 5 3 8 5 1 8 4 2 4 4 0 4 4 2 4 4 0 4 | 5 3 8 5 1 8 2 4 2 4 4 0 4 1 4 2 4 4 0 4 1 | 5 3 8 5 1 8 2 2 4 2 4 4 0 4 1 1 4 2 4 4 0 4 1 1 | 5 3 8 5 1 8 2 2 0 4 2 4 4 0 4 1 1 0 4 2 4 4 0 4 1 1 0 | 5 3 8 5 1 8 2 2 0 2 4 2 4 4 0 4 1 1 0 0 4 2 4 4 0 4 1 1 0 0 | 5 3 8 5 1 8 2 2 0 2 1 4 2 4 4 0 4 1 1 0 0 0 4 2 4 4 0 4 1 1 0 0 0 | 5 3 8 5 1 8 2 2 0 2 1 2 4 2 4 4 0 4 1 1 0 0 0 1 4 2 4 4 0 4 1 1 0 0 0 1 |