

Resource Usage Report for carry_skip_adder

Table of Contents

Parameter Value: 8 6

Parameter Value: 7 5

Parameter Value: 6 5

Parameter Value: 5 4

Parameter Value: 4 4

Parameter Value: 3 3

Parameter Value: 2 3

Parameter Value: 1 3

Parameter Value: 1

[illegible]

Parameter Value: 2

Module	port_bits	cell_count	wire_count	port_count	hierarchy_depth	wire_bits	\$_XOR_	\$_AND_	full_adder	\$paramod\$skip_logic\N=s32'00000000000000000000000000000100	\$_ANDNOT_	\$_ORNOT_	\$paramod\$ripple_carry_adder\N=s32'00000000000000000000000000000100	half_adder	\$_NOR_	\$_OR_	\$_XOR_	\$_AND_	\$_ANDNOT_	\$_ORNOT_	\$_NOR_	\$_OR_
\$paramod\$ripple_carry_adder\N=s32'00000000000000000000000000000100	14	4	6	5	2	18	8	8	4	0	0	0	0	0	0	4	8	8	0	0	0	4
\$paramod\$ripple_carry_adder\N=s32'00000000000000000000000000000100 -> full_adder	5	3	8	5	1	8	2	2	0	0	0	0	0	2	0	1	2	2	0	0	0	1
\$paramod\$skip_logic\N=s32'00000000000000000000000000000100	11	9	13	5	0	19	0	0	0	0	1	2	0	0	4	2	0	0	1	2	4	2
carry_skip_adder	26	4	7	5	3	30	16	16	0	2	2	4	2	0	8	12	16	16	2	4	8	12
carry_skip_adder -> \$paramod\$ripple_carry_adder\N=s32'00000000000000000000000000000100	14	4	6	5	2	18	8	8	4	0	0	0	0	0	0	4	8	8	0	0	0	4
carry_skip_adder -> \$paramod\$skip_logic\N=s32'00000000000000000000000000000100	11	9	13	5	0	19	0	0	0	0	1	2	0	0	4	2	0	0	1	2	4	2
full_adder	5	3	8	5	1	8	2	2	0	0	0	0	0	2	0	1	2	2	0	0	0	1
full_adder -> half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0
half_adder	4	2	4	4	0	4	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Parameter Value: 3

