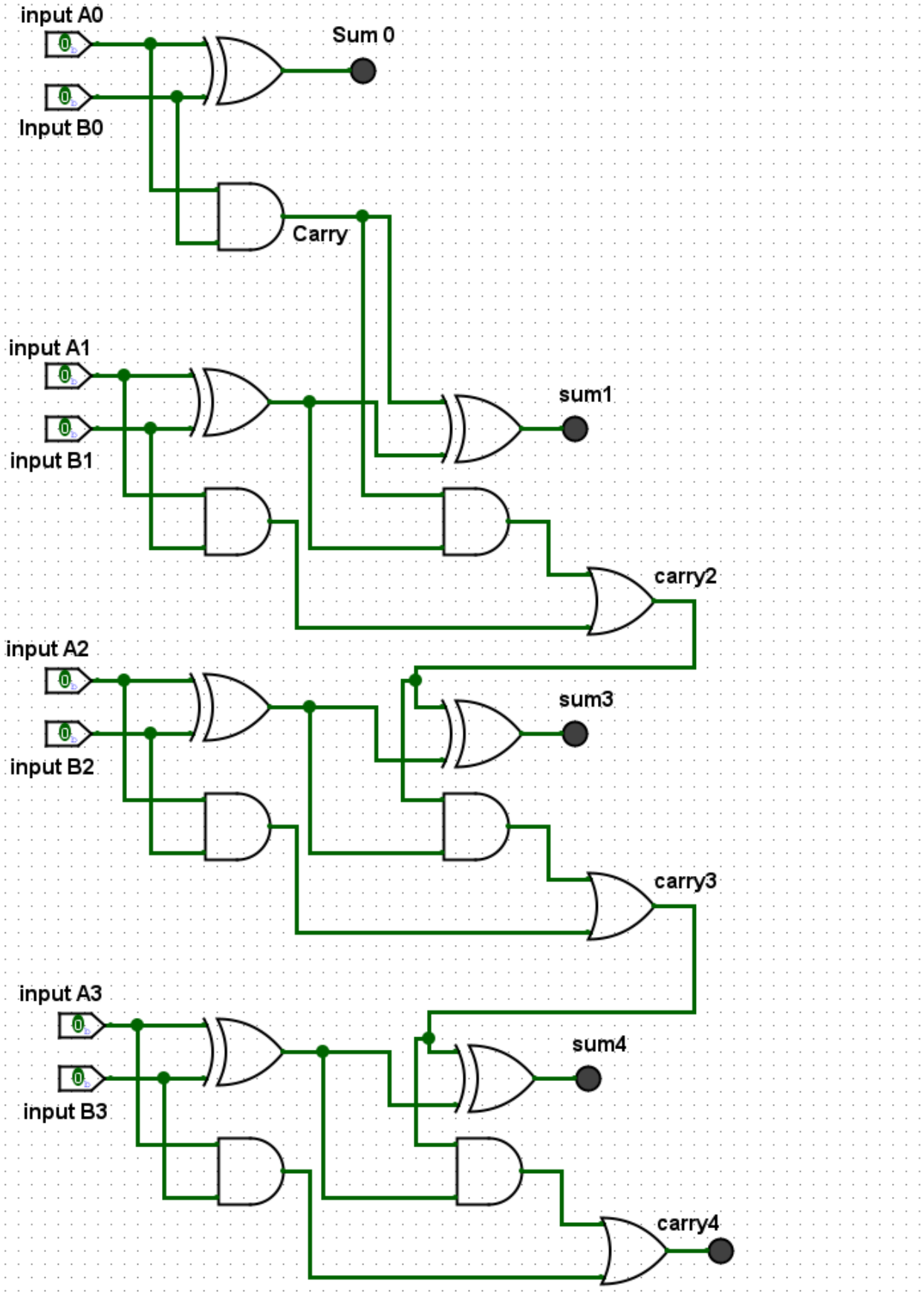
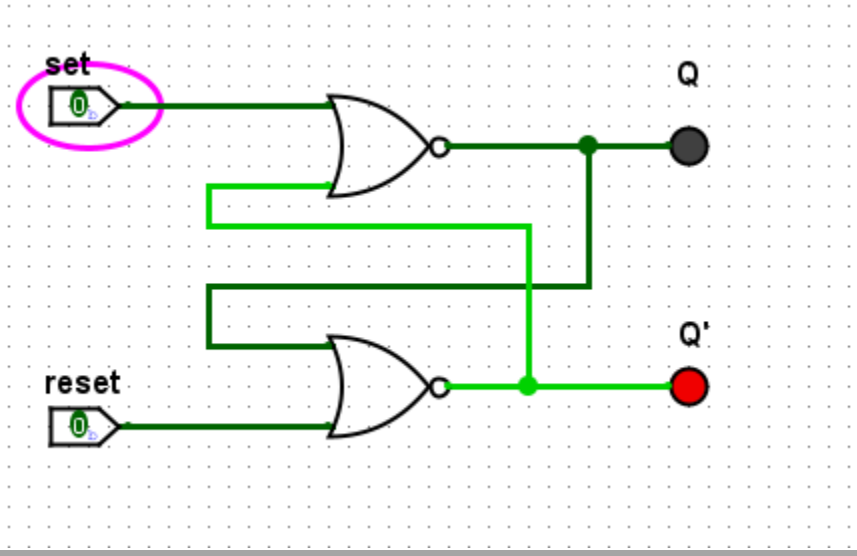
Lab 2 – Computer Systems (Shafi Uzman Fassy)

1. **2 4-bit adders**



Input A	Input B	Output
0101	0000	0101
0101	0001	0110
0101	0010	0111
0101	0011	1000
0101	0100	1001
0101	0101	1010
0101	0110	1011
0101	0111	1100
0101	1000	1101
0101	1001	1110
0101	1010	1111
0101	1011	0000
0101	1100	0001
0101	1101	0010
0101	1110	0011
0101	1111	0100

2. **R-S Flip Flop**

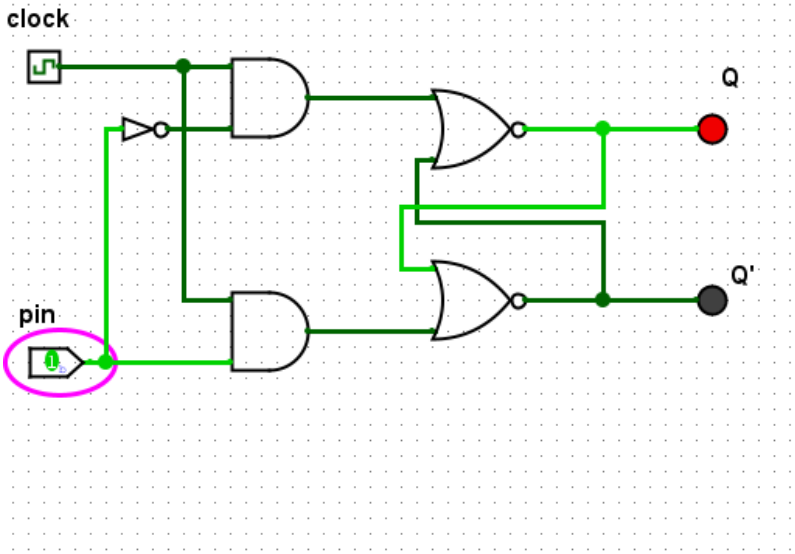


Set	Reset	Q	Q’
1	**0**	**0**	**1**
1	**1**	**0**	**0**
0	**1**	**1**	**0**
1	**1**	**0**	**0**

11. Because when set input is 1 and reset input is 0 the output for Q is ff and Q’ is on. This is because RS flip flops help to store a particular state in a digital circuit.

12. When both inputs are set to 1 both outputs are off which puts our R-S flip flop into a forbidden state.

13. D-Flip Flop



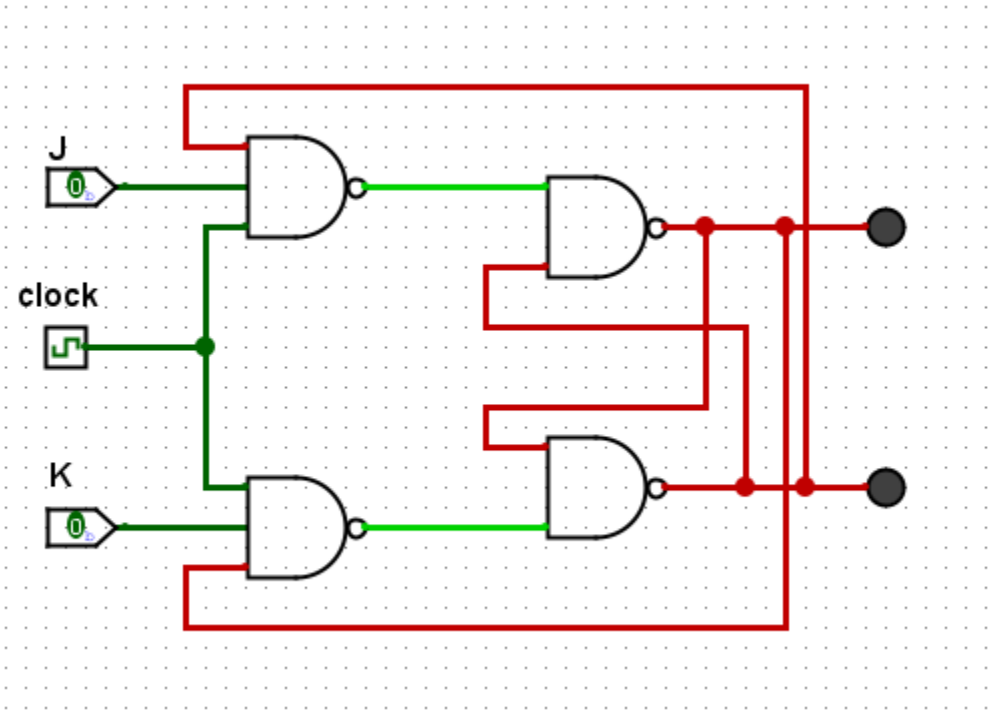
Clock	Pin	Q	Q’
0	**0**	**1**	**0**
0	**1**	**1**	**0**
1	**1**	**1**	**0**
1	**0**	**0**	**1**

15. In D-Flip flops, it uses a clock to allow information to pass through on a time duration / synchronous timing which avoids racing the in circuit. Also, clocks can be seen as a control buffer as if the clock is not pulsing then nothing has changed in the state of the circuit. D Flip flops are used to store data at a programmed time until it is needed to function.

16. clocks helps in avoiding racing in circuits and when clocks are pulsing it changes the states of Q and Q’ from turning on and off.

17. Since R-S flip flops can cause a forbidden state it is not preferred, and D flip flops already consists of R and S inputs.

18. J-K Flip Flops



J	K	Q (WHEN CLOCKED)	Q’ (WHEN CLOCKED)
0	0	No change	No change
1	0	1	0
0	1	0	1
1	1	Toggles	Toggles

20. JK Flip-Flop can be converted as a D-Flipflop by taking the j and k inputs with another input taken from the negation of the first input.

21. when j and k are made into 1 input it turns to a T- flip flop.