

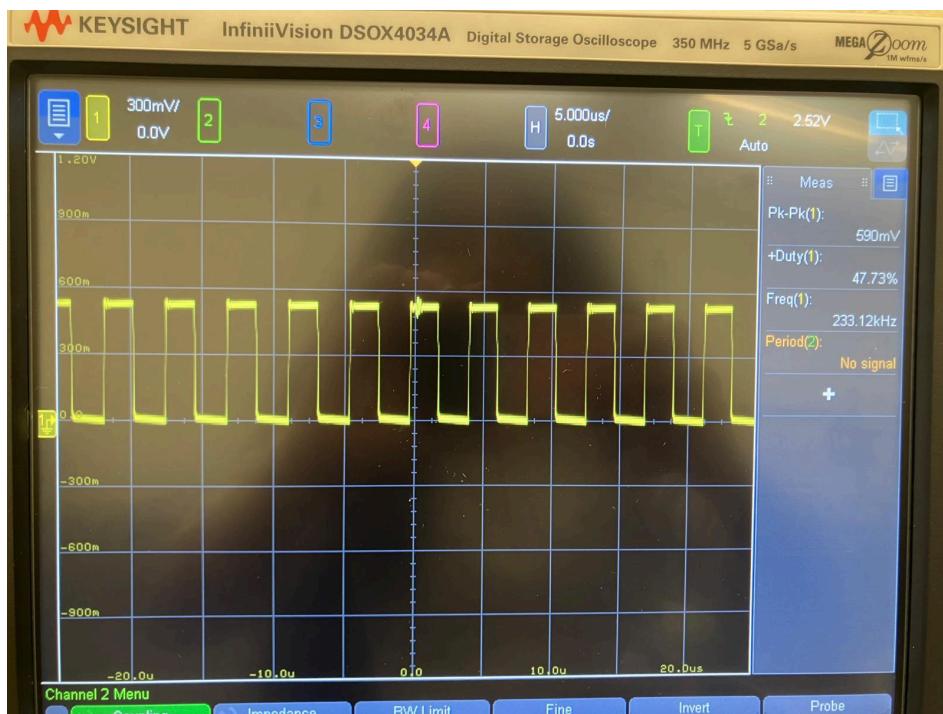
Lab Report 3: A/D and D/A Converters

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Question 1

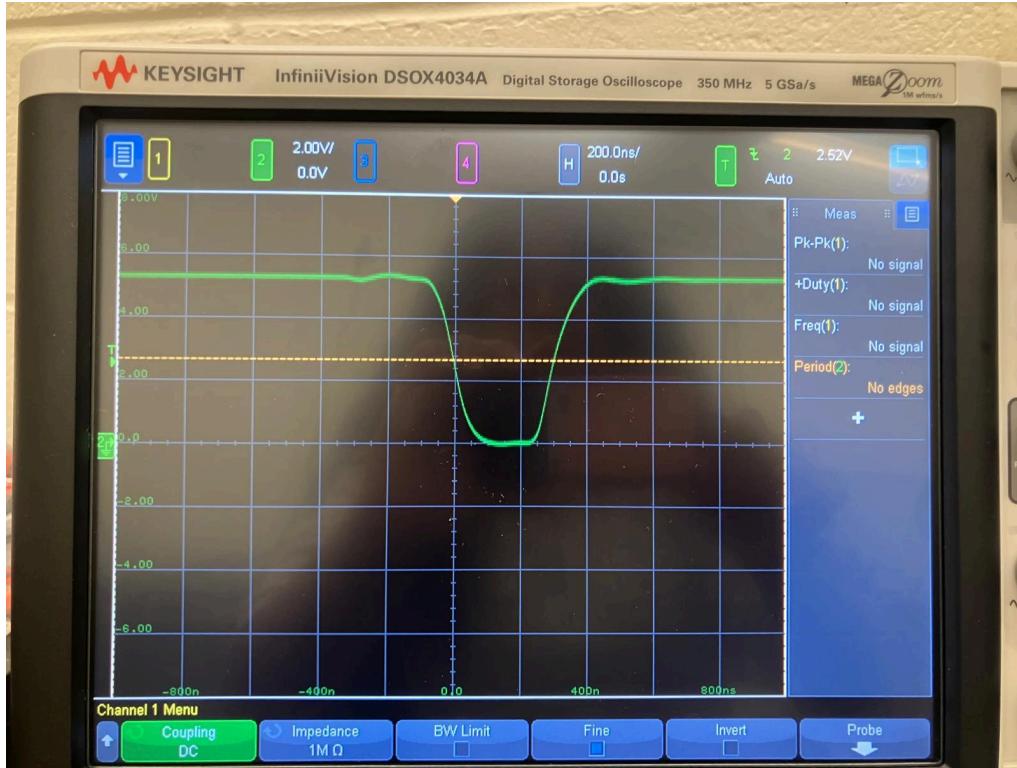
1. The clock frequency at pin 19 is **233 kHz**.
2. The conversion time by measuring the period of the waveform at pin 5 is **310 μ s**.
3. At 233 kHz, one clock cycle is approximately $1/233,000 = 4.29 \mu\text{s}$. Dividing the conversion time by the clock period gives: $310 \mu\text{s} / 4.29 \mu\text{s} = 72 \text{ clock cycles}$.
4. The conversion time **does not** depend on the value of the voltage being converted because the ADC is a successive-approximation one, the conversion time is fixed. Thus, it always takes the same number of clock cycles regardless of the input voltage. (Our apologies for not getting a photo of this, we somehow rushed passed this in the lab.)

Waveform for the Clock Period

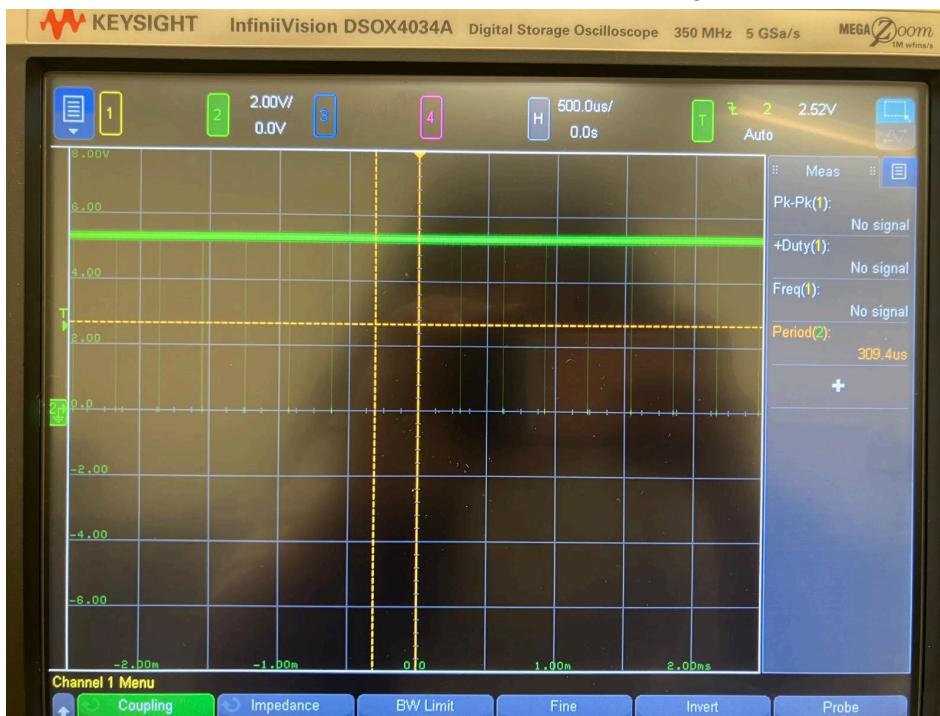


Waveform for the clock period at pin 19.

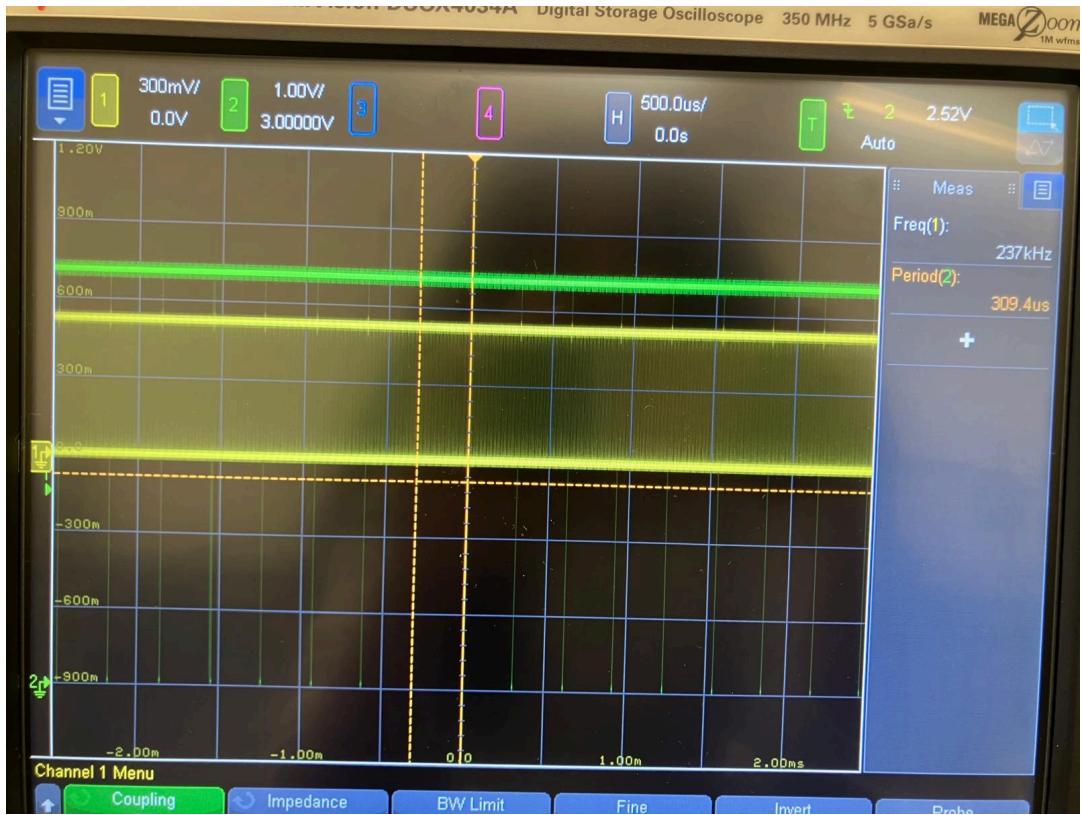
Waveform for the interrupt signal



Zoomed in picture for the waveform of the interrupt signal at pin 5.

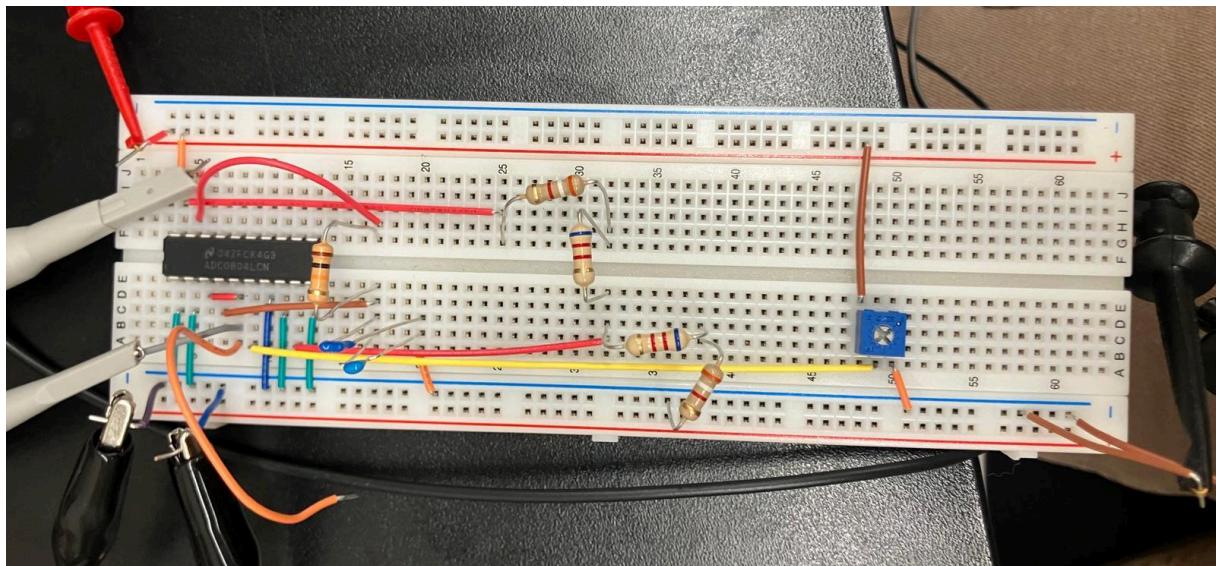


This is a slightly more zoomed out picture of the waveform at Pin 5. As we can see, the period of this is 309.4 microseconds.



Waveforms at Pin 19 and Pin 5 put together.

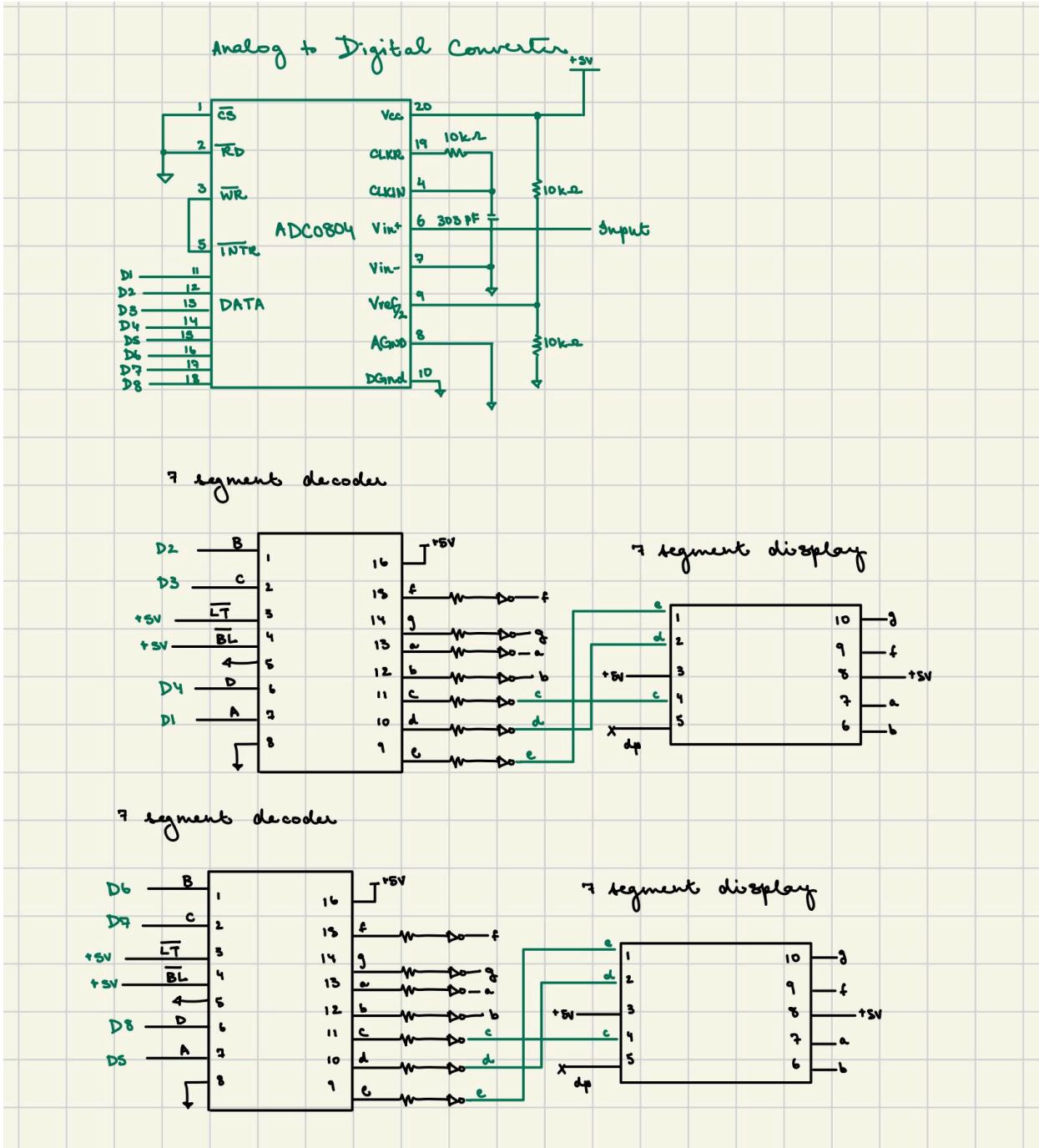
Circuit for Q1



A picture of the circuit.

Design 1

Circuit Schematic



Description and Explanation

The circuit schematic is composed of the ADC0804 chip, the 7-segment decoder, and the 7 segment display. The ADC is set up similarly to Q1, except that pin 6, instead of being hooked up to the potentiometer, is connected to the input voltage instead. The data output feeds into the data pins of the 7 segment decoder, which is connected to the 7 segment display. Here, we have the circuit take the ADC's output, and scale it to the reference voltage of 5V (ie: if the ADC outputs 0 we get 0V and if it outputs 255 we get 5V).

Table of 5 tests:

Tests:	1	2	3	4	5
Input Voltage (V):	1.18	1.69	2.34	3.99	4.52
Output in Octal:	17	26	36	63	72
Output Converted to Decimal:	15	22	30	51	58
Expected Output in Decimal:	14.87	21.29	29.48	50.27	56.95
Error (expected - actual):	0.13	0.71	0.52	0.73	1.05

Voltmeter Design Working

Link to video:

https://docs.google.com/presentation/d/1IYbTYMs_90f1L2k_EbucdJl3cxymKKWEqvm3UEvKO8/edit#slide=id.p

Question 2

1. The sampling frequency = $1/(conversion\ time) = 1/(310\ \mu s) = 3.2\text{kHz}$.

Amplitude

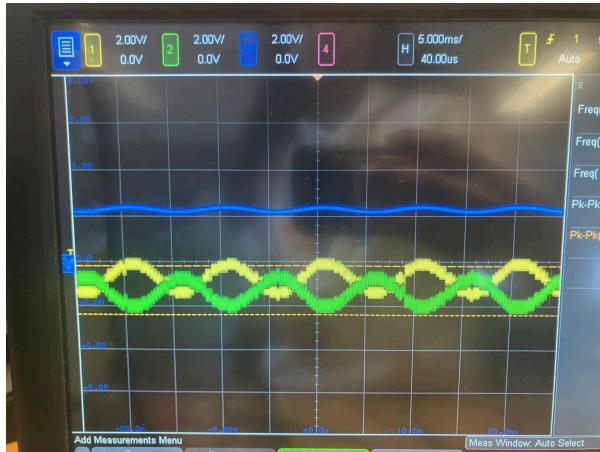
In green: DAC output, or also known as V_{out+}

In yellow: Inverse of DAC output, also known as V_{out-}

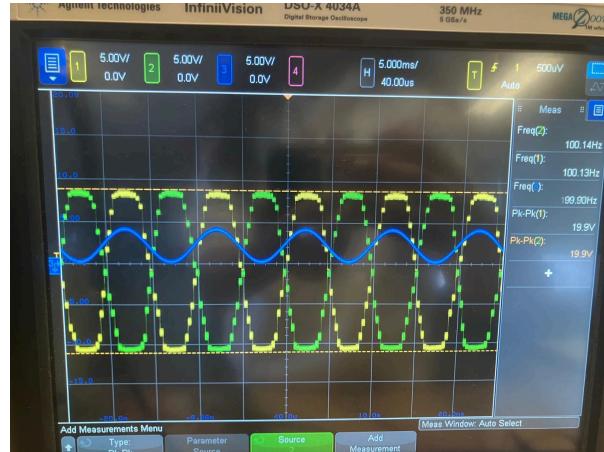
X axis: time, each grid square is 5ms long

Y axis: voltage, each grid square starts at a height of 2V then later becomes 5V to accommodate the waveform

.1



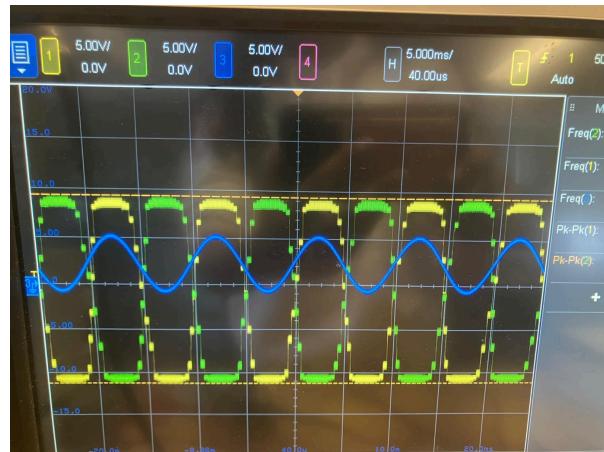
.2



.25



.3

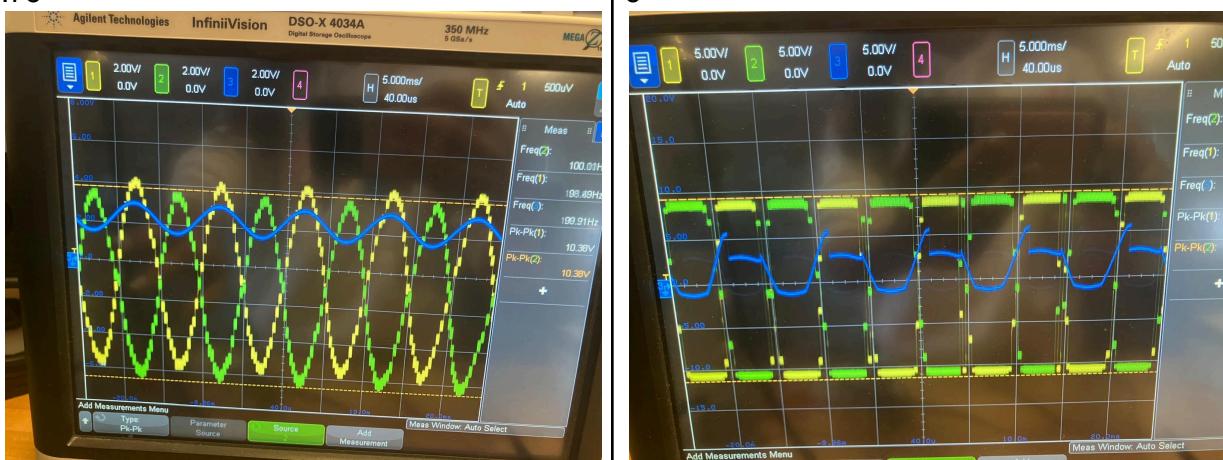


.5

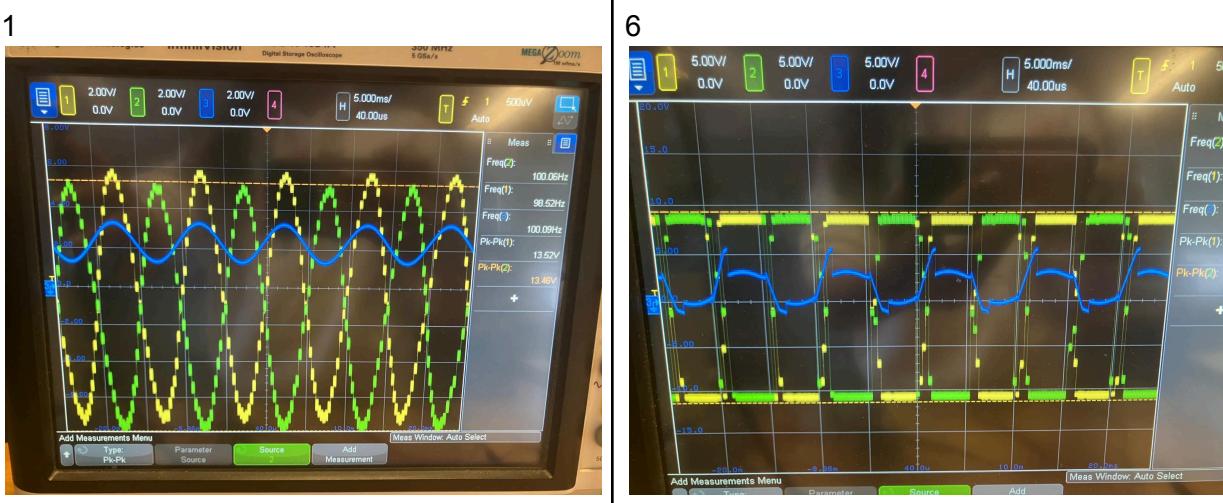
4



.75



5



As the ADC input increases in amplitude so does the DAC output. The DAC output is much larger than ADC input. As the ADC input amplitude gets to 2V, the DAC output's peaks and

troughs flatten. This is probably because of saturation. The DAC becomes unable to produce any higher output voltage. This is not an example of aliasing because we are changing amplitude, not frequency.

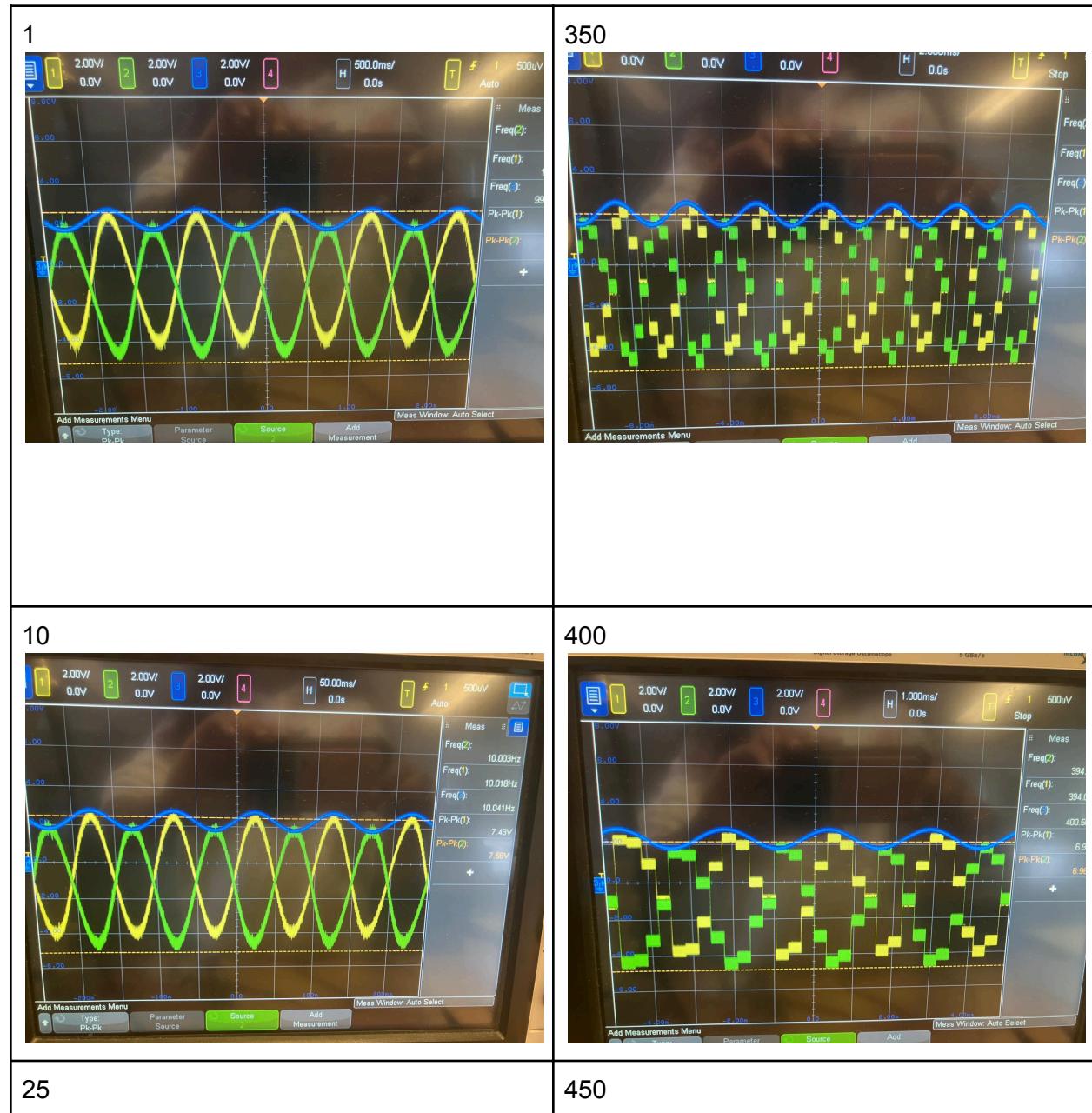
Frequency

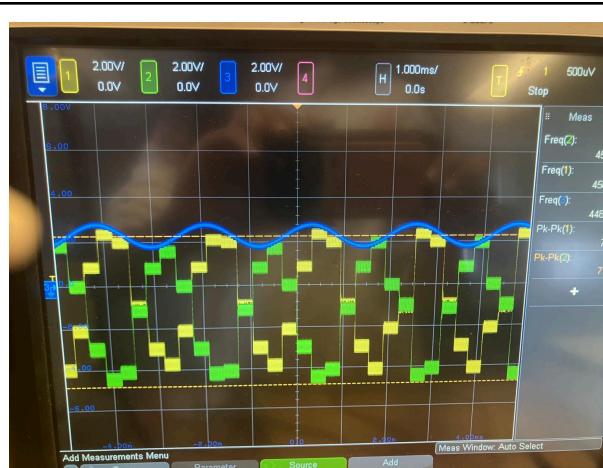
In green: DAC output, or also known as V_{out+}

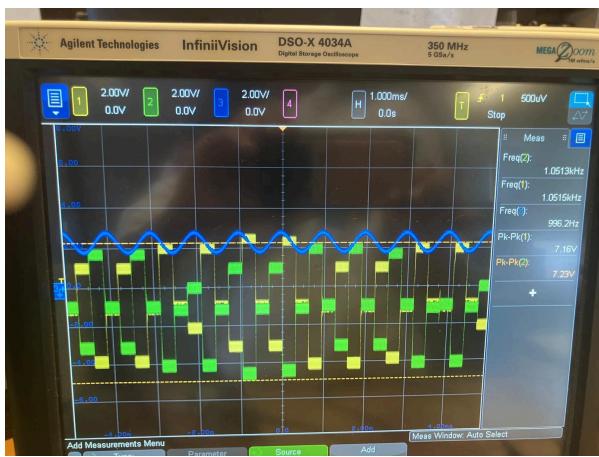
In yellow: Inverse of DAC output, also known as V_{out-}

X axis: time, each grid square is 5ms long

Y axis: voltage, each grid square starts at a height of 2V then later becomes 5V to accommodate the waveform







150



2000



200

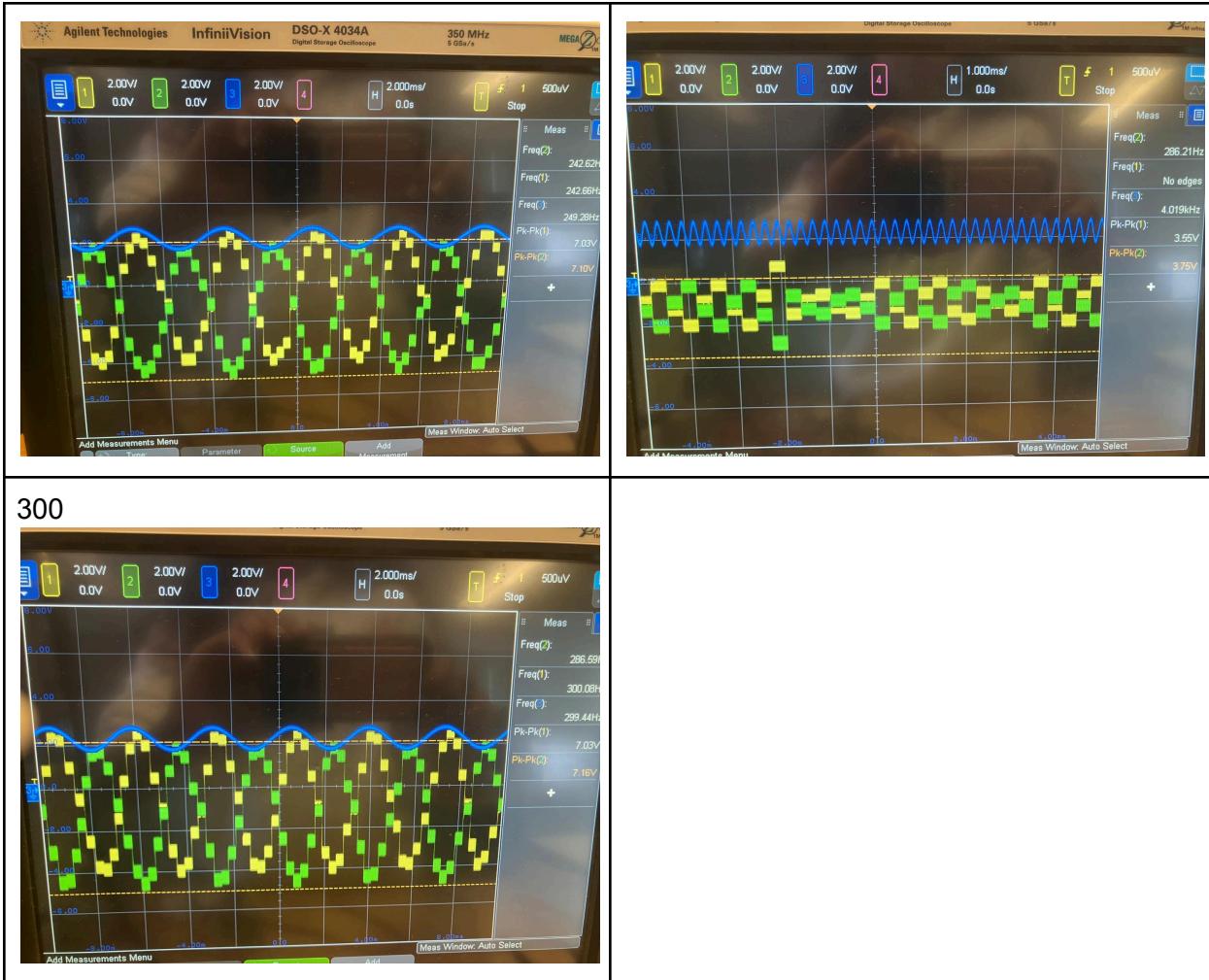


3000



250

4000



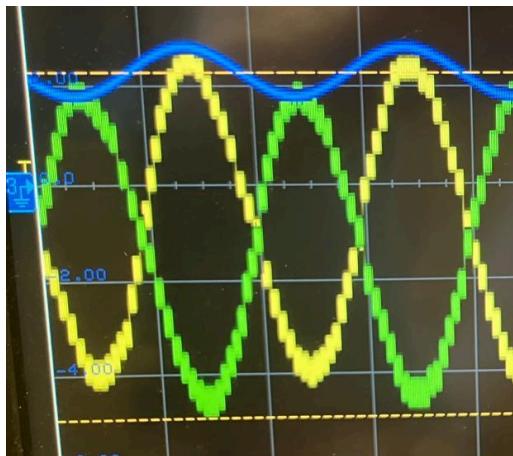
The sampling frequency as determined above is 3.2kHz. That means if we have an input waveform frequency of 3.2kHz, we sample it once a cycle. This gives a bad reconstruction of the original signal. The Nyquist Theorem says that a signal's sample frequency must be twice as much as the signal's highest frequency to avoid losing information. So if our sampling frequency is 3.2kHz, the max frequency we can give to our input waveform is 1.6kHz. **After 1.6kHz, aliasing occurs.** Still, with an input waveform frequency of 1.6kHz, we are sampling it twice a cycle. Sampling a sine wave twice a cycle still gives a horrible reconstruction.

In other words, the Nyquist rule gives us the bare minimum amount of information. It is really only useful for observing signals that repeat many times without changing much, not a sine wave. It doesn't give you an accurate picture of the sine wave's shape or amplitude, only of the wave's frequency.

A decent number is about 10 times a cycle. This means an input waveform of frequency 320 Hz. We see a figure pretty close to this in our table at 300Hz. Like we have mathematically calculated, we see 10 points produced per cycle.



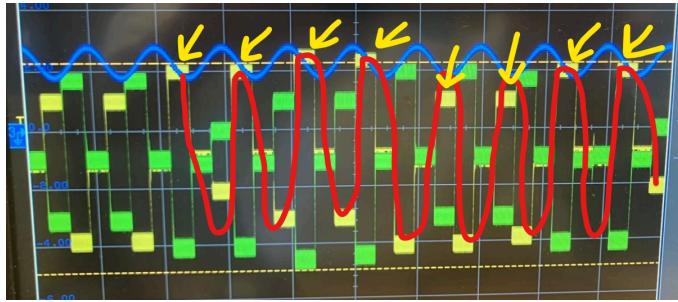
A more realistic number, used by audio engineers, is about 30 times per second. This means an input waveform of around 100Hz, which is the suggested frequency in the lab spec.



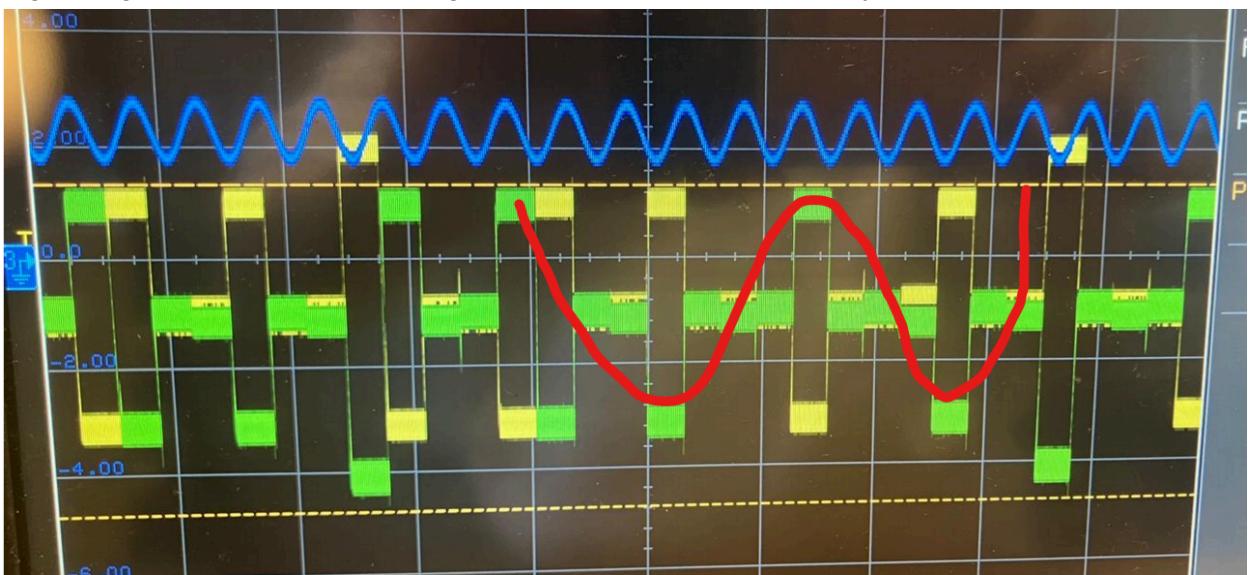
We see at low frequencies between 1Hz and 50Hz, the shape of the output signal is identical to the input signal. From 75 to 300 Hz, we can clearly see sampling happen. Still, we can draw a line through the handful of points per cycle and reconstruct an accurate output signal. At 350 to 750 Hz, the output gets a pretty horrible resolution.

However, horrible resolution doesn't mean that aliasing is happening. It means that when you try to reconstruct the signal you produce a signal that has an entirely different frequency. Ie, even if you tried to draw a line through the output points, you would not get an accurate reconstruction of the original signal because the higher frequencies are misinterpreted as lower frequencies in the digitized signal.

Here is an example. As we can see at 1000 Hz, when we draw a line through the output and reconstruct the original signal, the resolution is horrible, but the reconstructed signal still has the original frequency of 1000Hz. The yellow data points at the top still synchronize with the input waveform frequency.



As we can see at 2000Hz, when we draw a line through the green output and reconstruct the original signal, the reconstructed signal has a much lower frequency.



We mathematically know aliasing occurs at 1600Hz. And we have proof in our pictures that the system crosses from properly sampled to undersampled from 1000 to 2000Hz. Thus, as best as we can tell, evidence of aliasing does begin at the frequency we expect.

Circuit for Q2

