

Untitled*
 main
 Wiring
 Gates
 NOT Gate
 Buffer
 AND Gate
 OR Gate
 NAND Gate
 NOR Gate
 XOR Gate
 XNOR Gate
 Odd Parity
 Even Parity
 Controlled Buffer
 Controlled Inverter
 Plexers

Pin	
Leading	East
Output?	No
Data Bits	1
Free-state?	No
UI Behavior	Unchanged
Label	
Label Location	West
Label Font	SansSerif Plain 12

