Enabling AMD SEV in Xen

Xen Summit, 2024

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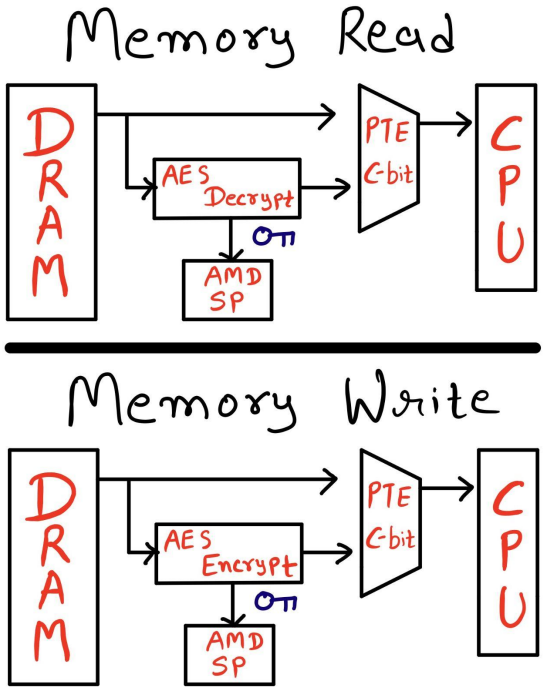
Agenda

- Overview of AMD Memory Encryption Technologies
- How AMD SEV works?
- AMD SEV and Xen
- Conclusion

AMD Memory Encryption Technologies

- **AMD Secure Memory Encryption [SME]**
  - Hardware AES engine located in the memory controller



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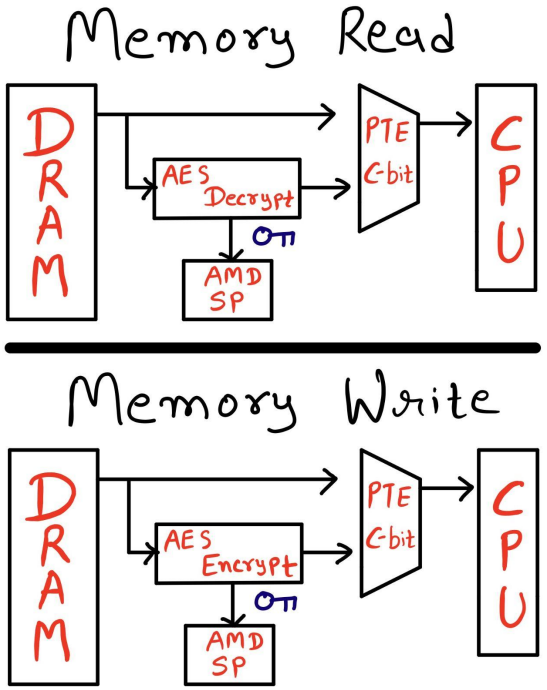

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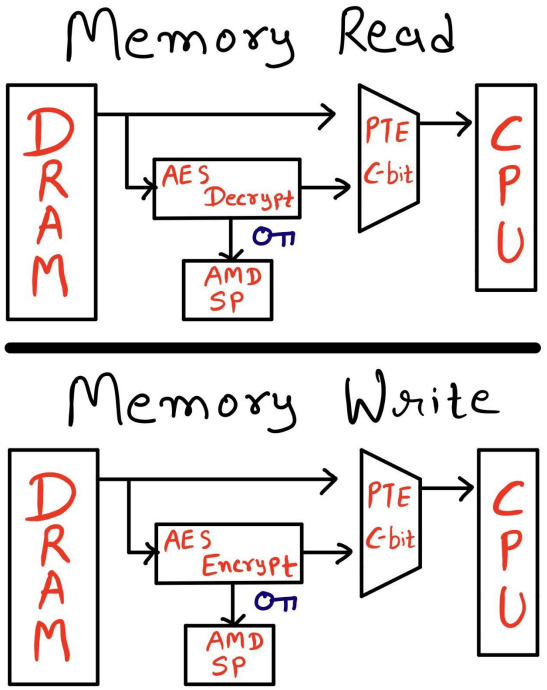

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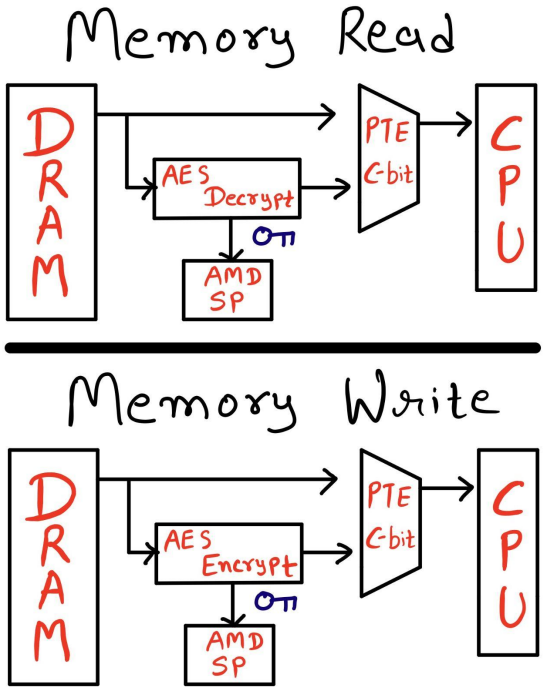

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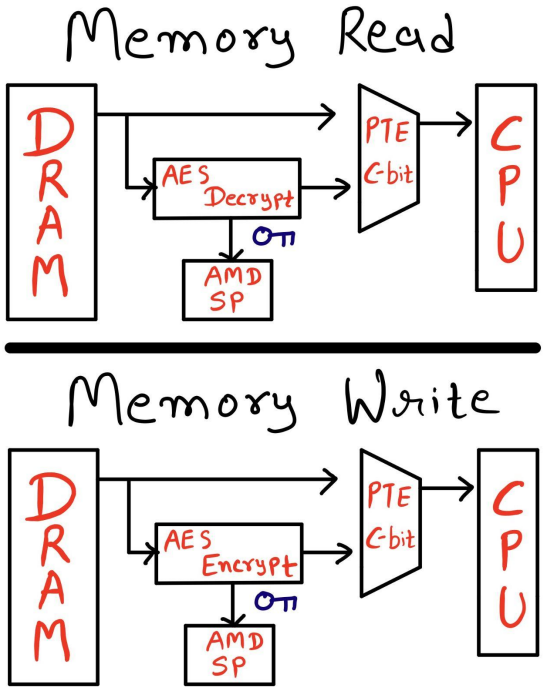

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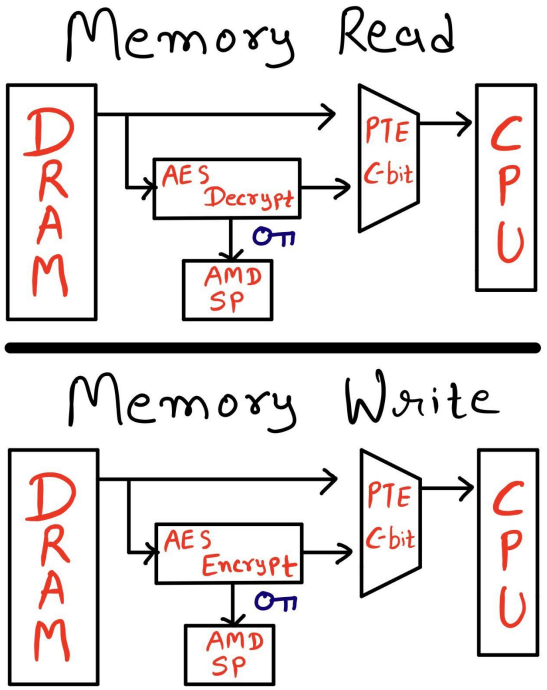
- ➢ AMD SME Demo



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  - Some restrictions on data in shared pages

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  - White paper on AMD SEV-ES

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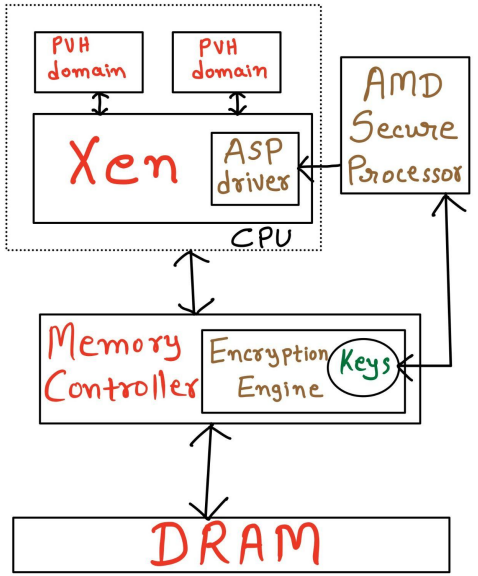
  - AMD SEV/SEV-ES/SEV-SNP Enablement Plan

How AMD SEV works?

❖ AMD SEV Architecture

- ➢ AMD Secure Processor



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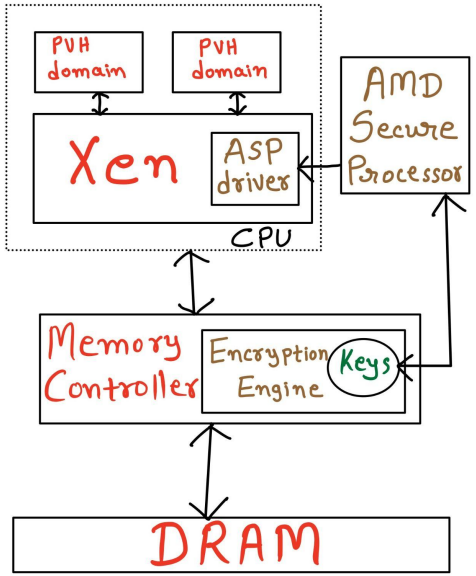

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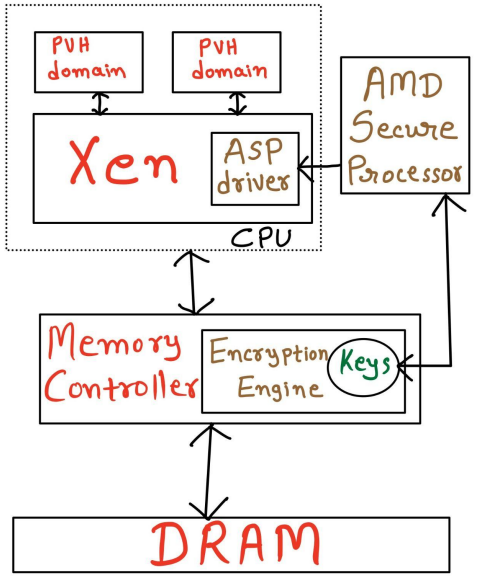

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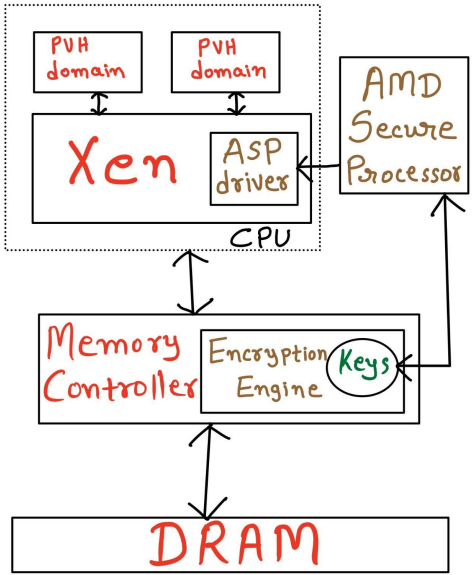

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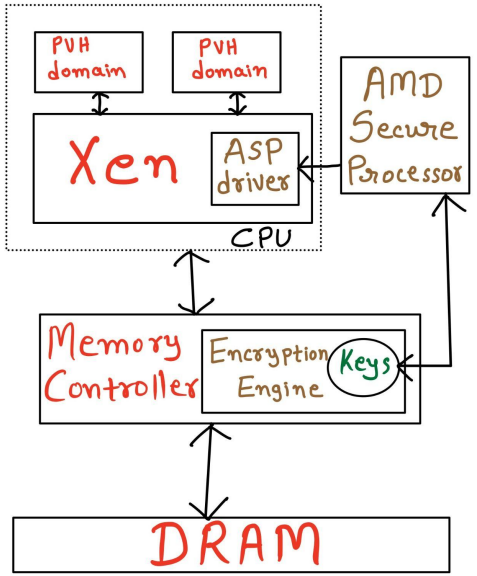

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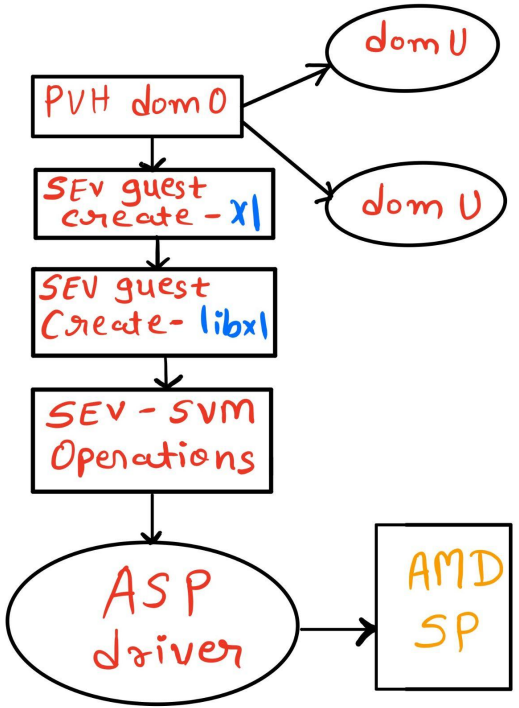

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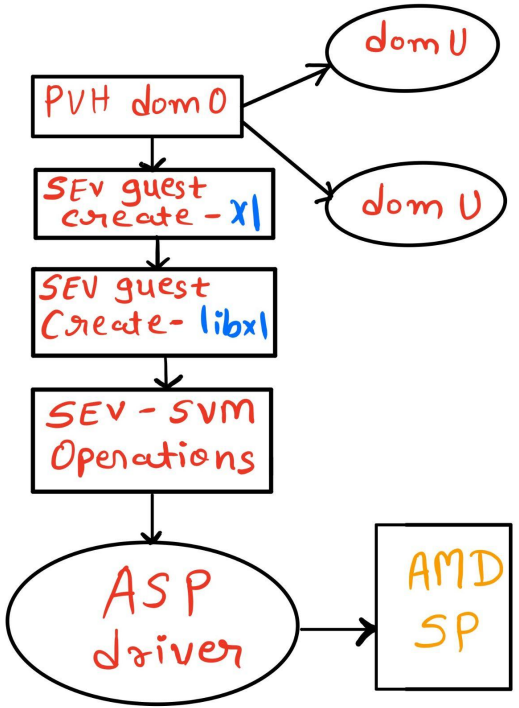

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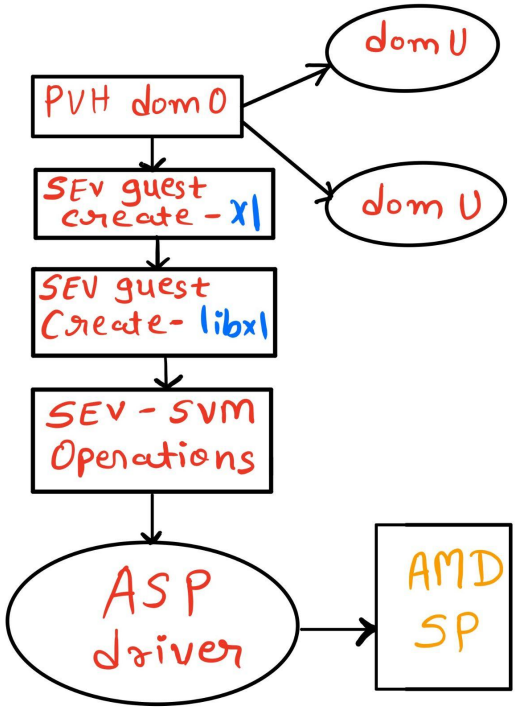

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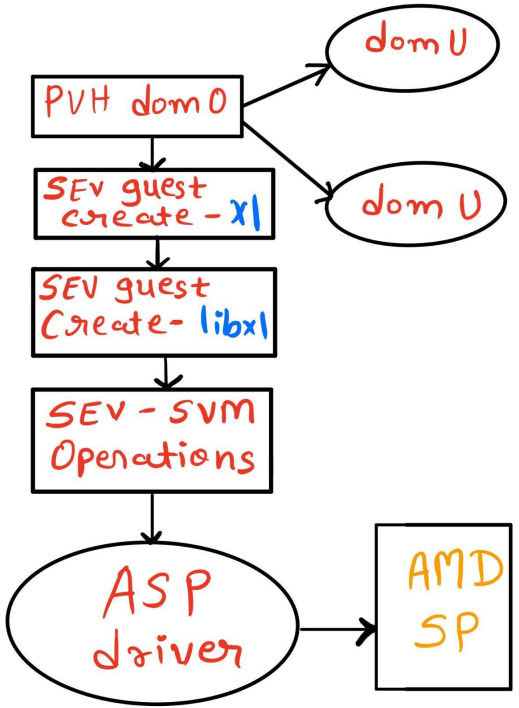

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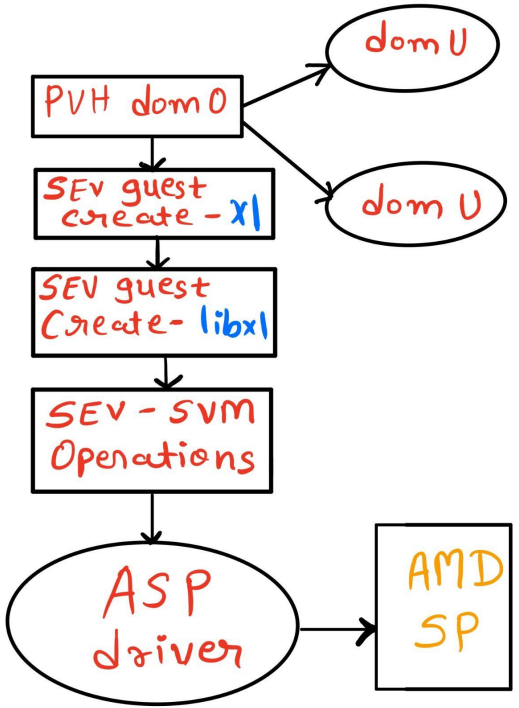

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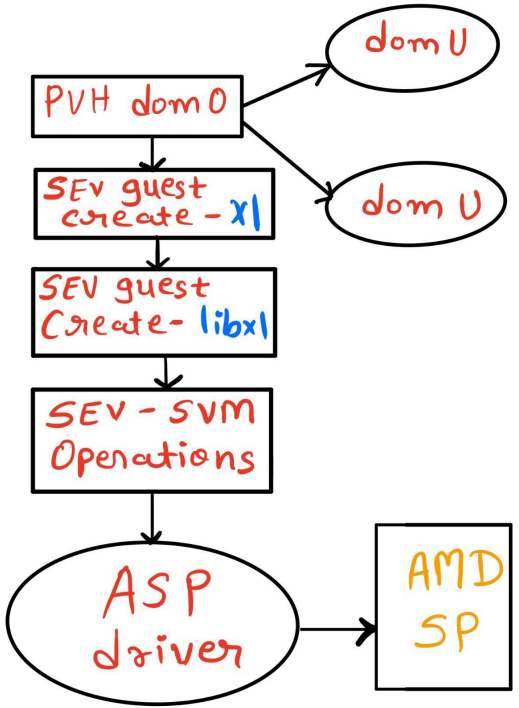

Upstream status

- RFC for implementing AMD Secure Processor (ASP) driver (Andrei)
  - Infrastructure improvements for AMD SEV and SVM leaves (Andrew)
- RFC for introducing the xen-wide ASID allocator (Vaishali)

Questions?

References

- AMD SME and SEV white paper
- Talk by Brijesh from AMD @ Xen Summit, 2016
- Blogpost on how ASID allocator works in Xen
- AMD architecture manual: Section 15.34
- AMD ASP Firmware code