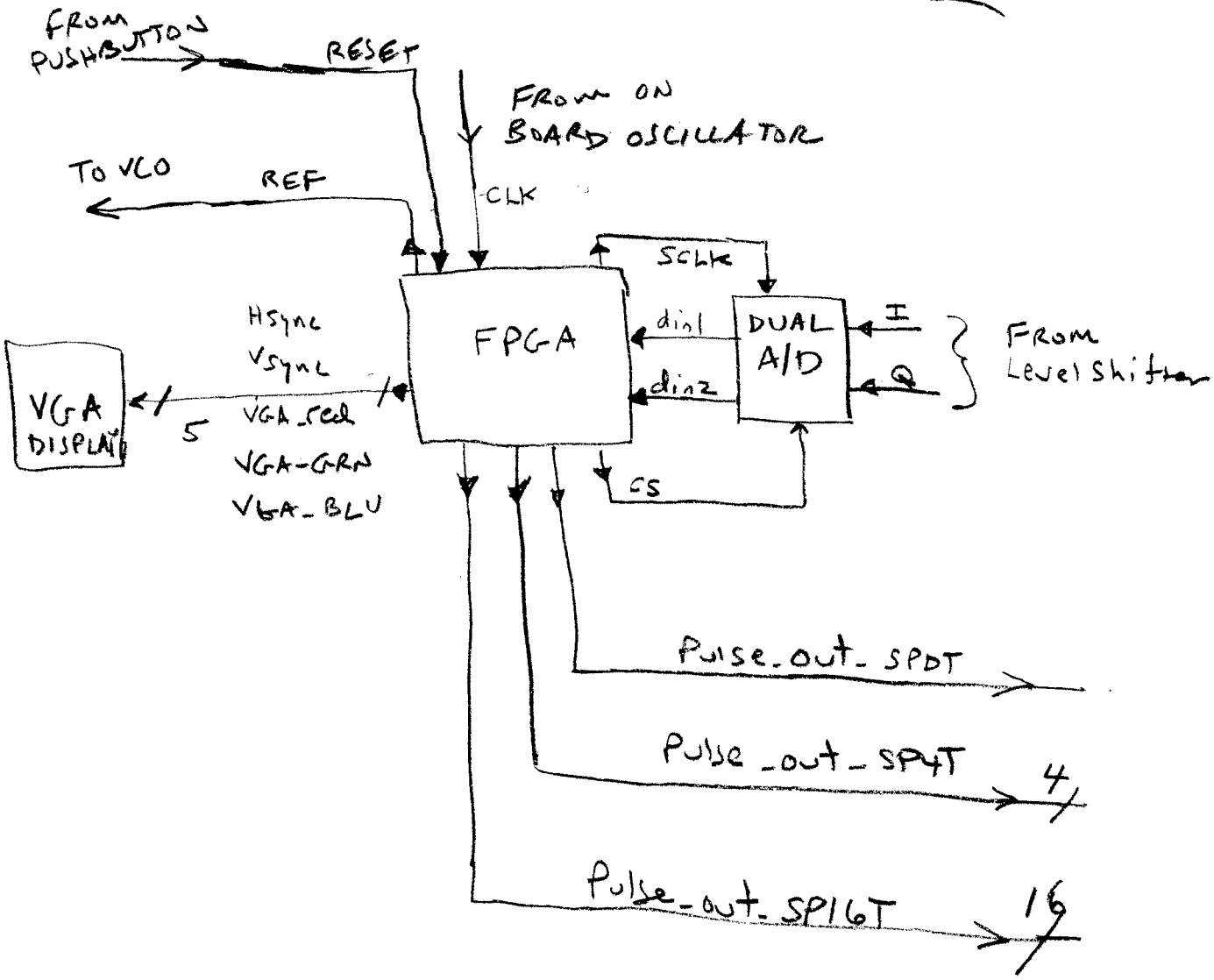
IMAGER FPGA PORT DEFINITION

1/16/15



IMAGER VHDL CODE FRAMEWORK 1/16/15

- Libraries Defined
- entity imager is port (
  define ports)
- architecture top of imager is
- type State_imag is (idle, readIQ, calcimag);
- Define signals
- TR_sw : Process -- SPDT
- Txhornsw : Process -- SP4T
- Rx hornSW : Process -- SP16T
- VGA25MHz : Process -- clock for VGA
- VGA_hor_vert : Process -- Hsync, Vsync.
- main : process
- Idle
- ReadIQ
- calcimag