I/O Advanced Programmable Interrupt Controller

From XOmB wiki

Contents

Memory-Mapped Registers

There are two memory-mapped registers that are used to communicate with the IOAPIC: a **selection register** and a **window register**. The selection register (IOREGSEL) is used to determine which field to manipulate using the window register (IOWIN). The locations of these registers are at an arbitrary address, but the first IOAPIC is typically located at `0xfec00000`. To determine the exact address (of each IOAPIC, if there are more than one), the BIOS provided MP or ACPI tables should be parsed.

IOREGSEL

- **APIC Register Address** - Specifies the IOAPIC register to be read/written via the IOWIN register.

IOWIN

- **APIC Register Data** - Memory references to this register are mapped to the APIC register specified by the IOREGSEL register.

IOAPIC Registers

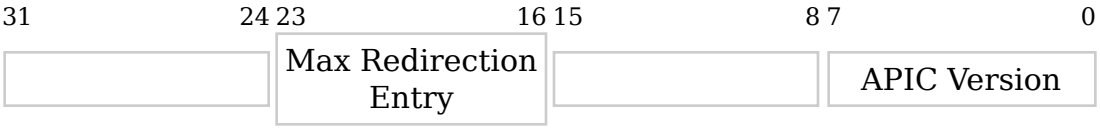
IOAPICID (0x00)

This rewritable register provides an identification number for the IOAPIC that can be used to distinguish it among the other IOAPICs in a system.

- **IOAPIC ID** - This contains a value which can identify this particular IOAPIC.

IOAPICVER (0x01)

This read-only register gives the version of the APIC hardware. Use this field to provide compatibility among various APIC implementations. It also gives the number of input pins for which this IOAPIC is responsible for controlling.



- **Max Redirection Entry** - This field contains the entry number (0 being the lowest) of the highest entry in this IOAPIC's IO redirection table. That is, this value is equal to the number of interrupt input pins minus one. The range of values is from 0 to 239.
- **APIC Version** - Identifies the implementation version for this IOAPIC. For the IOAPIC, the version is 0x11.

IOAPICARB (0x02)

This read-only register contains the arbitration identifier for this IOAPIC. This value is a priority number that determines how the bus is assigned the APIC. A higher value indicates a higher priority.

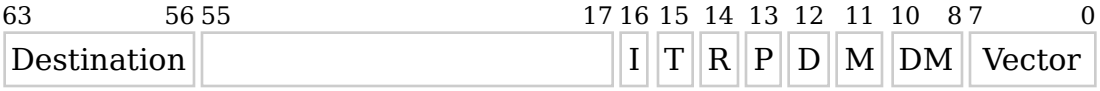
The highest priority is not always the winner, however when an arbitration takes place, this winner is then assigned 0, the lowest priority. All other agents participating on this bus increment their values by 1 (except the agent with priority 15, who take the winner's priority + 1).

The arbitration identifier is always loaded with the IOAPIC ID when it receives a level-triggered INIT with de-assert message.

- **Priority** - Indicates the bus arbitration priority of this IOAPIC.

IOREDTBL (0x10..0x27)

The IOAPIC has a table of registers that indicate how interrupts that occur on interrupt pins are routed and handled by the system. There are 12 redirection table entries each of which is 64 bits wide and selected via two registers (a high and low). That is, the lower 32 bits of the field are selected by the LO register and the higher 32 bits by the HI register.



- **Destination** - This determines which CPU the interrupt will be issued upon. It depends on the *Destination Mode* field. If that bit is set (Logical Mode), then this field is a bitmap which indicate a set of processors that should receive the interrupt. Identification of which processors within this set receive the interrupt is decided also by the *Delivery Mode* field. Otherwise, if the bit is clear (Physical Mode), then the first 4 bits of this field indicate an APIC ID that identify a Local APIC that should respond to this interrupt.
- **I** - *Interrupt Mask* - When set, this indicates that the interrupt is masked. An interrupt that occurs on this pin will be ignored.
- **T** - *Trigger Mode* - Indicates the type of signal that will trigger an interrupt on the pin. When set, this pin is level triggered, otherwise it is edge triggered.
- **R** - *Remote Interrupt Request Register* - Only defined for level triggered interrupts. When set, this indicates that the local APIC has accepted the interrupt sent by this IOAPIC for this pin. It is cleared when the local APIC receives an EOI that matches this interrupt vector.
- **P** - *Interrupt Pin Polarity* - Specifies the pin polarity of the interrupt. When set, indicates that it is low active, otherwise it is high active. That is, if level triggered and low active, the interrupt fires when there is no signal instead of when there is a pulse on the line.
- **D** - *Delivery Status* - Contains the current status of the interrupt delivery. When set, this indicates that a send is pending. This means that it is being delivered, but the APIC receiving it is busy. When cleared, this indicates that delivery is idle.

- **M** - *Destination Mode* - This affects the interpretation of the *Destination* field. Read more above.
- **DM** - *Delivery Mode* - Specifies how the APICs should interpret the interrupts upon reception.
  - **0x0** Fixed - Deliver to all cores listed in *Destination*.
  - **0x1** Lowest Priority - Among the set of processors listed in *Destination*, send to the one executing with lowest priority.
  - **0x2** System Management Interrupt - Requires an edge *Trigger Mode*. Also requires that *Vector* is 0 (it won't actually fire vector 0, it is ignored). Specifies a SMI.
  - **0x4** Non Masked Interrupt - Always acts like an edge triggered interrupt (regardless of *Trigger Mode*), therefore always program the pin to edge triggered. As for SMI above, *Vector* should be 0 and will be ignored. Fires an NMI.
  - **0x5** INIT - For the same reason as NMI above, always set Trigger Mode to 'edge'. Delivery to all cores in the set given by *Destination* with an INIT assert. This will put all specified cores into an INIT state, which is used to boot the auxiliary cores.
  - **0x7** ExtINT - Requires *Trigger Mode* to be 'edge'. Deliver to all cores given by *Destination* as an interrupt that originated by some external interrupt controller (for instance a 8259A or 8259A compatible controller). The external controller is expected to specify a vector by other means.
- **Vector** - The vector that is used to deliver the interrupt on the actual core. Valid values range from 0x10 to 0xFE.