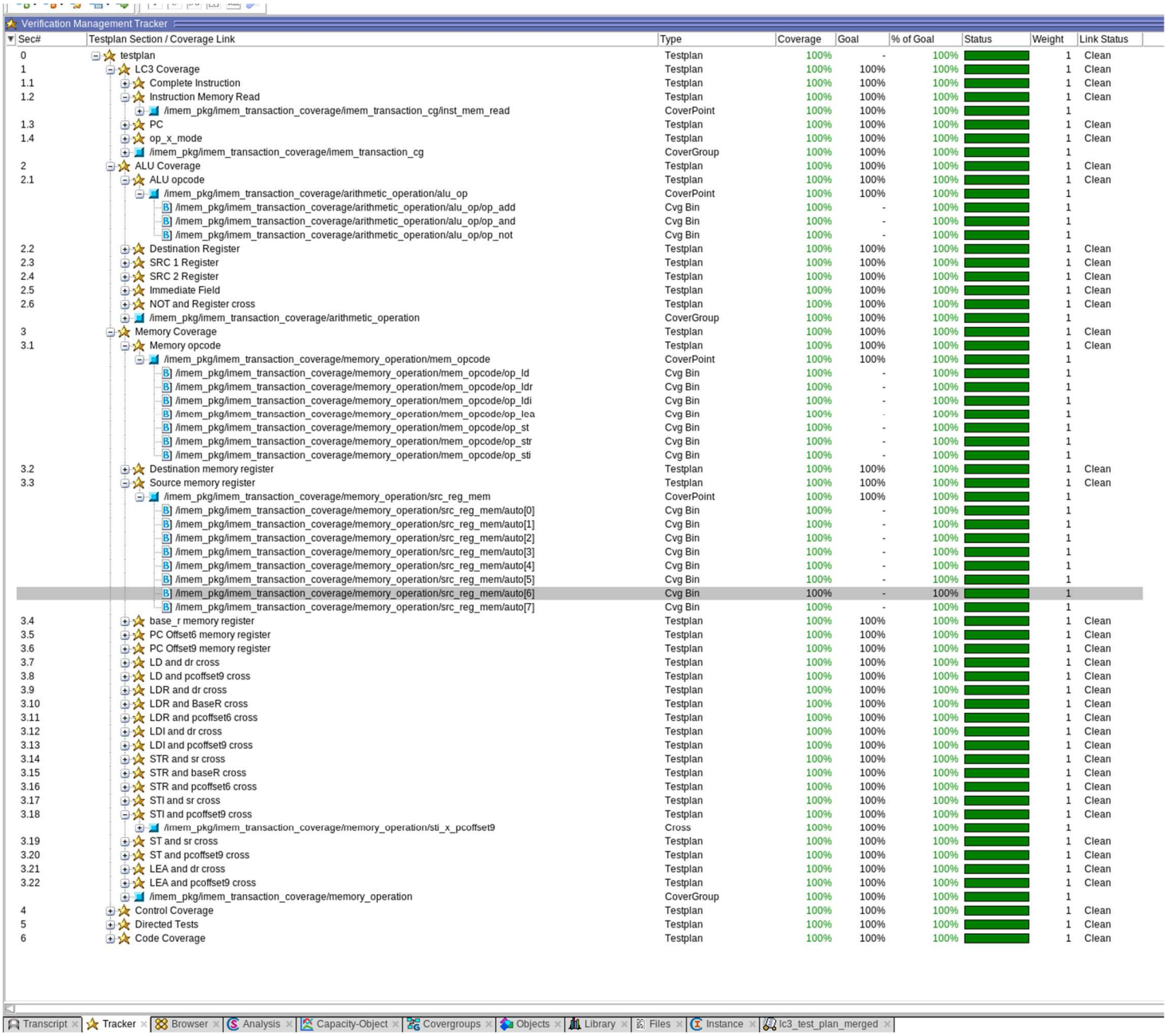
Coverage Report – Group 17



Verification Management Tracker

Sec#	Testplan Section / Coverage Link	Type	Coverage	Goal	% of Goal	Status	Weight	Link Status
0	testplan	Testplan	100%	-	100%		1	Clean
1	LC3 Coverage	Testplan	100%	100%	100%		1	Clean
1.1	Complete Instruction	Testplan	100%	100%	100%		1	Clean
1.2	Instruction Memory Read	Testplan	100%	100%	100%		1	Clean
	/imem_pkg/imem_transaction_coverage/imem_transaction_cg/inst_mem_read	CoverPoint	100%	100%	100%		1	
1.3	PC	Testplan	100%	100%	100%		1	Clean
1.4	op_x_mode	Testplan	100%	100%	100%		1	Clean
	/imem_pkg/imem_transaction_coverage/imem_transaction_cg	CoverGroup	100%	100%	100%		1	
2	ALU Coverage	Testplan	100%	100%	100%		1	Clean
2.1	ALU opcode	Testplan	100%	100%	100%		1	Clean
	/imem_pkg/imem_transaction_coverage/arithmetic_operation/alu_op	CoverPoint	100%	100%	100%		1	
	/imem_pkg/imem_transaction_coverage/arithmetic_operation/alu_op/op_add	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/arithmetic_operation/alu_op/op_and	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/arithmetic_operation/alu_op/op_not	Cvg Bin	100%	-	100%		1	
2.2	Destination Register	Testplan	100%	100%	100%		1	Clean
2.3	SRC 1 Register	Testplan	100%	100%	100%		1	Clean
2.4	SRC 2 Register	Testplan	100%	100%	100%		1	Clean
2.5	Immediate Field	Testplan	100%	100%	100%		1	Clean
2.6	NOT and Register cross	Testplan	100%	100%	100%		1	Clean
	/imem_pkg/imem_transaction_coverage/arithmetic_operation	CoverGroup	100%	100%	100%		1	
3	Memory Coverage	Testplan	100%	100%	100%		1	Clean
3.1	Memory opcode	Testplan	100%	100%	100%		1	Clean
	/imem_pkg/imem_transaction_coverage/memory_operation/mem_opcode	CoverPoint	100%	100%	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/mem_opcode/op_ld	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/mem_opcode/op_ldr	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/mem_opcode/op_ldi	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/mem_opcode/op_lea	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/mem_opcode/op_st	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/mem_opcode/op_str	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/mem_opcode/op_sti	Cvg Bin	100%	-	100%		1	
3.2	Destination memory register	Testplan	100%	100%	100%		1	Clean
3.3	Source memory register	Testplan	100%	100%	100%		1	Clean
	/imem_pkg/imem_transaction_coverage/memory_operation/src_reg_mem	CoverPoint	100%	100%	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/src_reg_mem/auto[0]	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/src_reg_mem/auto[1]	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/src_reg_mem/auto[2]	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/src_reg_mem/auto[3]	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/src_reg_mem/auto[4]	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/src_reg_mem/auto[5]	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/src_reg_mem/auto[6]	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/memory_operation/src_reg_mem/auto[7]	Cvg Bin	100%	-	100%		1	
3.4	base_r memory register	Testplan	100%	100%	100%		1	Clean
3.5	PC Offset6 memory register	Testplan	100%	100%	100%		1	Clean
3.6	PC Offset9 memory register	Testplan	100%	100%	100%		1	Clean
3.7	LD and dr cross	Testplan	100%	100%	100%		1	Clean
3.8	LD and pcoffset9 cross	Testplan	100%	100%	100%		1	Clean
3.9	LDR and dr cross	Testplan	100%	100%	100%		1	Clean
3.10	LDR and BaseR cross	Testplan	100%	100%	100%		1	Clean
3.11	LDR and pcoffset6 cross	Testplan	100%	100%	100%		1	Clean
3.12	LDI and dr cross	Testplan	100%	100%	100%		1	Clean
3.13	LDI and pcoffset9 cross	Testplan	100%	100%	100%		1	Clean
3.14	STR and sr cross	Testplan	100%	100%	100%		1	Clean
3.15	STR and baseR cross	Testplan	100%	100%	100%		1	Clean
3.16	STR and pcoffset6 cross	Testplan	100%	100%	100%		1	Clean
3.17	STI and sr cross	Testplan	100%	100%	100%		1	Clean
3.18	STI and pcoffset9 cross	Testplan	100%	100%	100%		1	Clean
	/imem_pkg/imem_transaction_coverage/memory_operation/sti_x_pcoffset9	Cross	100%	100%	100%		1	
3.19	ST and sr cross	Testplan	100%	100%	100%		1	Clean
3.20	ST and pcoffset9 cross	Testplan	100%	100%	100%		1	Clean
3.21	LEA and dr cross	Testplan	100%	100%	100%		1	Clean
3.22	LEA and pcoffset9 cross	Testplan	100%	100%	100%		1	Clean
	/imem_pkg/imem_transaction_coverage/memory_operation	CoverGroup	100%	100%	100%		1	
4	Control Coverage	Testplan	100%	100%	100%		1	Clean
5	Directed Tests	Testplan	100%	100%	100%		1	Clean
6	Code Coverage	Testplan	100%	100%	100%		1	Clean

Transcript | Tracker | Browser | Analysis | Capacity-Object | Covergroups | Objects | Library | Files | Instance | lc3_test_plan_merged

3	Memory Coverage	Testplan	100%	100%	100%		1	Clean
4	Control Coverage	Testplan	100%	100%	100%		1	Clean
4.1	Branch opcode	Testplan	100%	100%	100%		1	Clean
	/imem_pkg/imem_transaction_coverage/control_operation/br_opcode	CoverPoint	100%	100%	100%		1	
	/imem_pkg/imem_transaction_coverage/control_operation/br_opcode/op_br	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/control_operation/br_opcode/op_jmp	Cvg Bin	100%	-	100%		1	
4.2	NZP Register	Testplan	100%	100%	100%		1	Clean
	/imem_pkg/imem_transaction_coverage/control_operation/NZP_reg	CoverPoint	100%	100%	100%		1	
	/imem_pkg/imem_transaction_coverage/control_operation/NZP_reg/zero_zero_zero	Cvg Ignore Bin	-	-	-		1	
	/imem_pkg/imem_transaction_coverage/control_operation/NZP_reg/auto[1]	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/control_operation/NZP_reg/auto[2]	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/control_operation/NZP_reg/auto[3]	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/control_operation/NZP_reg/auto[4]	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/control_operation/NZP_reg/auto[5]	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/control_operation/NZP_reg/auto[6]	Cvg Bin	100%	-	100%		1	
	/imem_pkg/imem_transaction_coverage/control_operation/NZP_reg/auto[7]	Cvg Bin	100%	-	100%		1	
4.3	PC control	Testplan	100%	100%	100%		1	Clean
4.4	base control	Testplan	100%	100%	100%		1	Clean
4.5	Jump Field Cross	Testplan	100%	100%	100%		1	Clean
4.6	BR Field Cross with nzp	Testplan	100%	100%	100%		1	Clean
4.7	BR Field Cross with pcoffset9	Testplan	100%	100%	100%		1	Clean
	/imem_pkg/imem_transaction_coverage/control_operation	CoverGroup	100%	100%	100%		1	
5	Directed Tests	Testplan	100%	100%	100%		1	Clean
5.1	ALU test	Testplan	100%	100%	100%		1	Clean
5.2	MEM test	Testplan	100%	100%	100%		1	Clean
	mem_test	Test	100%	100%	100%		-	
5.3	Control test	Testplan	100%	100%	100%		1	Clean
5.4	ALL opcode test	Testplan	100%	100%	100%		1	Clean
	test_top	Test	100%	100%	100%		-	
6	Code Coverage	Testplan	100%	100%	100%		1	Clean
6.1	RTL Core	Testplan	100%	100%	100%		1	Clean
	/hdl_top/DUT	Instance	100%	100%	100%		1	

Covergroups

Covergroups

Name	Class Type	Coverage	Goal	% of Goal	Status	Included	Merge_instances	Get_i
/imem_pkg/imem_transaction_coverage		100.00%						
TYPE imem_transaction_cg		100.00%	100	100.00%		✓	auto(1)	
TYPE arithmetic_operation		100.00%	100	100.00%		✓	auto(1)	
CVP arithmetic_operation::alu_op		100.00%	100	100.00%		✓		
bin op_add		537	1	100.00%		✓		
bin op_and		533	1	100.00%		✓		
bin op_not		537	1	100.00%		✓		
CVP arithmetic_operation::dest_reg		100.00%	100	100.00%		✓		
bin auto[0]		193	1	100.00%		✓		
bin auto[1]		204	1	100.00%		✓		
bin auto[2]		191	1	100.00%		✓		
bin auto[3]		207	1	100.00%		✓		
bin auto[4]		202	1	100.00%		✓		
bin auto[5]		199	1	100.00%		✓		
bin auto[6]		208	1	100.00%		✓		
bin auto[7]		203	1	100.00%		✓		
CVP arithmetic_operation::src1_reg		100.00%	100	100.00%		✓		
CVP arithmetic_operation::imm_bit		100.00%	100	100.00%		✓		
CVP arithmetic_operation::src2_reg		100.00%	100	100.00%		✓		
CVP arithmetic_operation::imm5_field		100.00%	100	100.00%		✓		
bin zero_to_31		518	1	100.00%		✓		
CVP arithmetic_operation::op_not		100.00%	100	100.00%		✓		
CVP arithmetic_operation::sr1		100.00%	100	100.00%		✓		
CROSS arithmetic_operation::not_x_sr1		100.00%	100	100.00%		✓		
TYPE memory_operation		100.00%	100	100.00%		✓	auto(1)	
CVP memory_operation::mem_opcode		100.00%	100	100.00%		✓		
bin op_ld		712	1	100.00%		✓		
bin op_ldr		484	1	100.00%		✓		
bin op_ldi		472	1	100.00%		✓		
bin op_lea		460	1	100.00%		✓		
bin op_st		502	1	100.00%		✓		
bin op_str		435	1	100.00%		✓		
bin op_sti		462	1	100.00%		✓		
CVP memory_operation::dest_reg_mem		100.00%	100	100.00%		✓		
CVP memory_operation::src_reg_mem		100.00%	100	100.00%		✓		
CVP memory_operation::base_r_reg_mem		100.00%	100	100.00%		✓		
CVP memory_operation::pcOffset_6_reg_mem		100.00%	100	100.00%		✓		
CVP memory_operation::pcOffset_9_reg_mem		100.00%	100	100.00%		✓		
CVP memory_operation::op_ldr		100.00%	100	100.00%		✓		
CVP memory_operation::op_ldi		100.00%	100	100.00%		✓		
CVP memory_operation::op_ld		100.00%	100	100.00%		✓		
CVP memory_operation::op_lea		100.00%	100	100.00%		✓		
CVP memory_operation::op_st		100.00%	100	100.00%		✓		
CVP memory_operation::op_str		100.00%	100	100.00%		✓		
CVP memory_operation::op_sti		100.00%	100	100.00%		✓		
CVP memory_operation::dreg_mem		100.00%	100	100.00%		✓		
CVP memory_operation::sreg_mem		100.00%	100	100.00%		✓		
CVP memory_operation::baser_mem		100.00%	100	100.00%		✓		

Test Ranking

```
#
# Ranking based on minimum number of tests.
# Ranking design tree path: "/*".
# Ranking 16 test(s).
#
# Rank   TotalCov  Testname
# -----  --------  --------------------
#     1     99.58  test_top
#     2     99.85  ctrl_test
#     3     99.96  alu_add_test
#     4    100.00  mem_ldr_test
# Reached set goal(s).
#
# Ranking summary:
#       Total Contributing Tests      = 4
#       Total Non-Contributing Tests  = 12
#       Total Coverage                = 100.00%
#       Testplan Coverage             = 100.00%
#       Total CPU Time                = 2.42 s
#       Total SIM Time                = 17440.00 ns

VSIM 3>
```