

# VLSI Project Report

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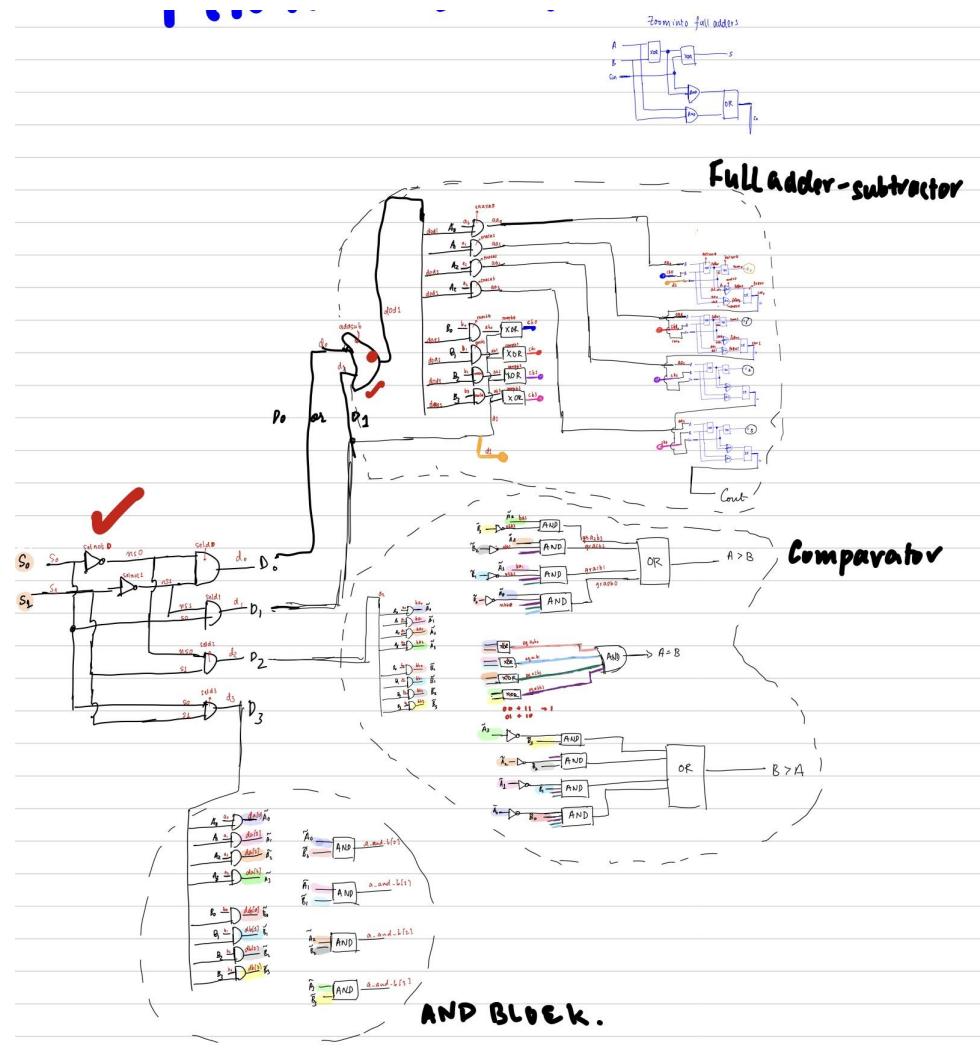
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This report is a comprehensive summary to the process of building an ALU circuit in verilog, ngspice and magic.

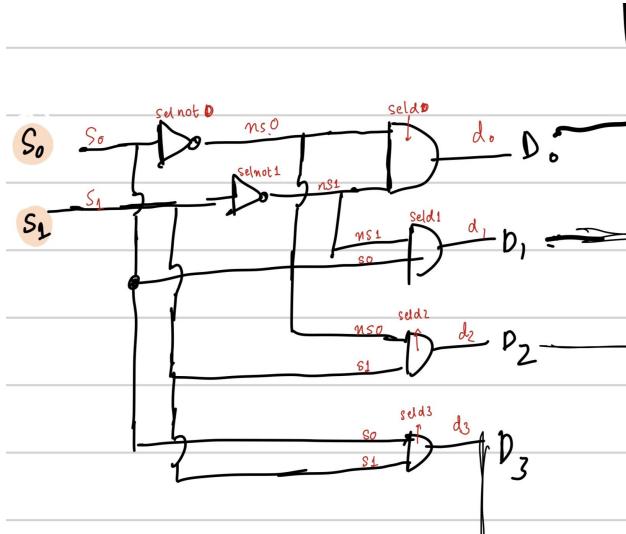
## Verilog Part:

The following are the gate diagrams required for the three components. I followed these gate diagrams to design my circuit

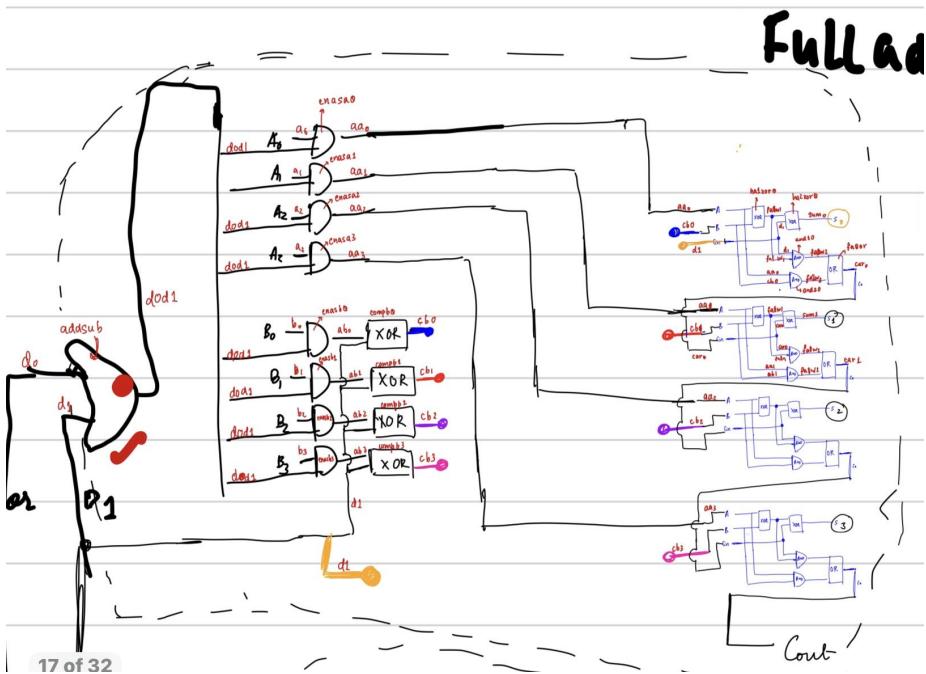
### Full Circuit.



## Decoder:

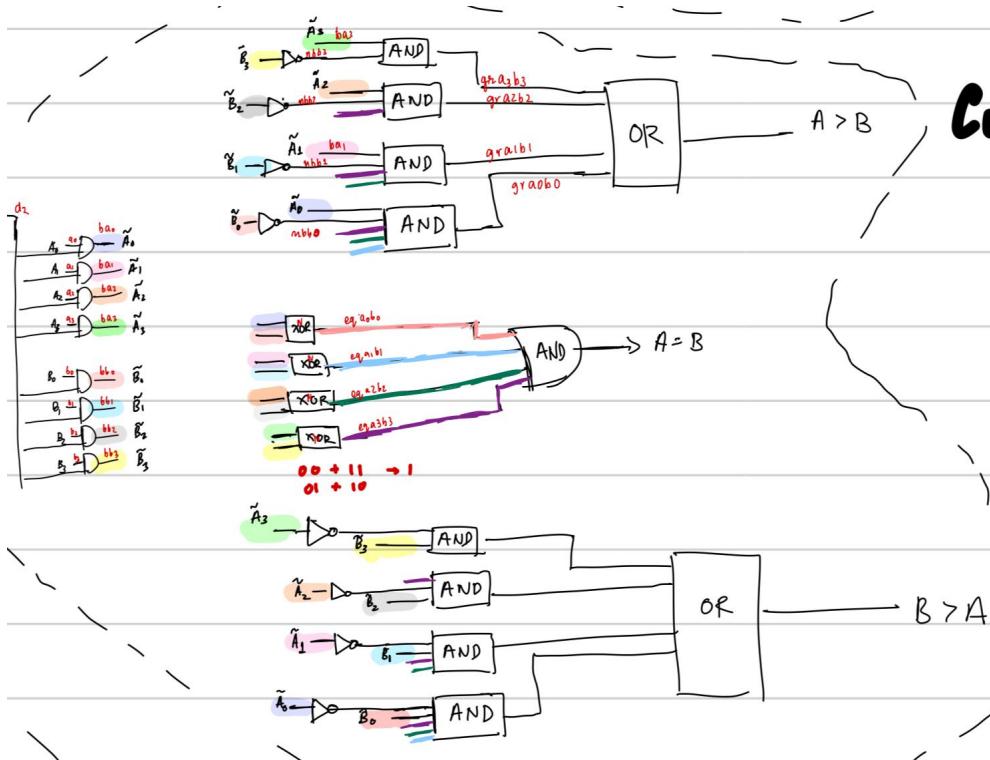


## Adder Subtractor:

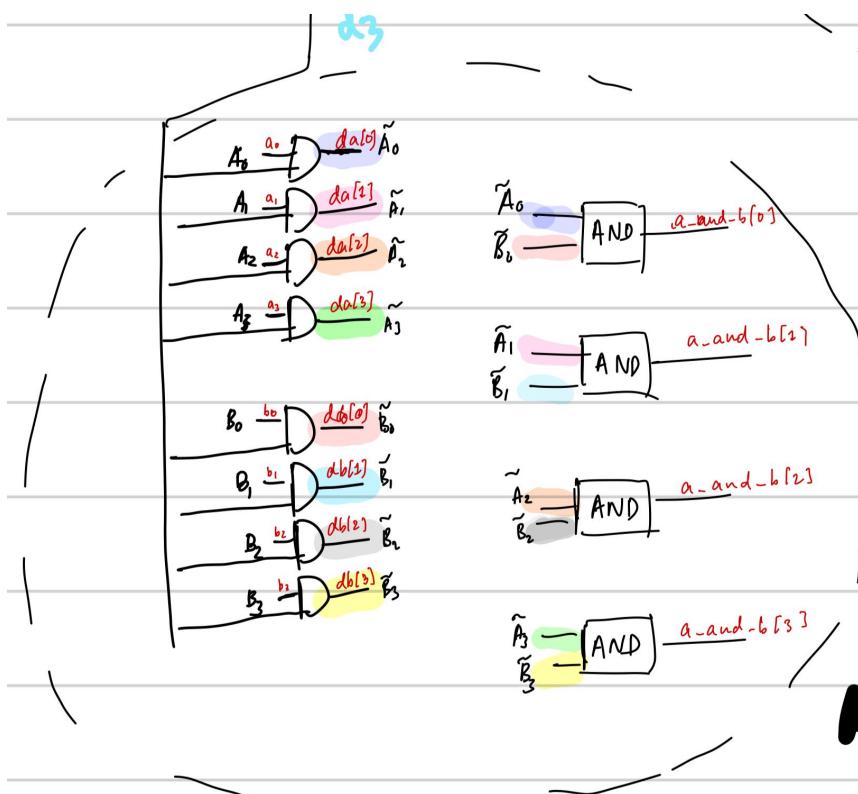


## Comparator:

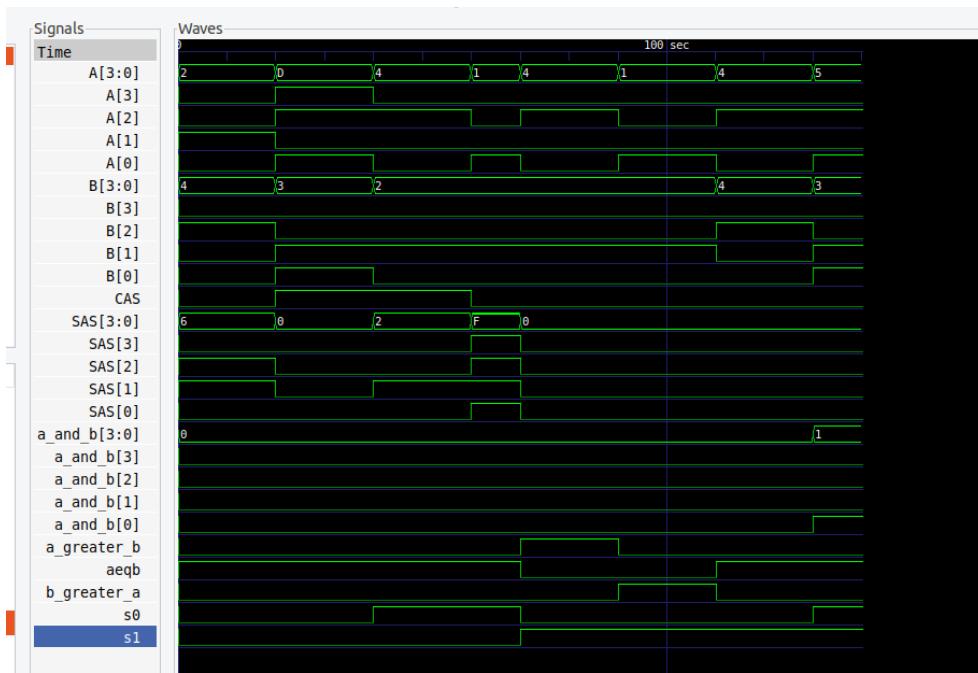
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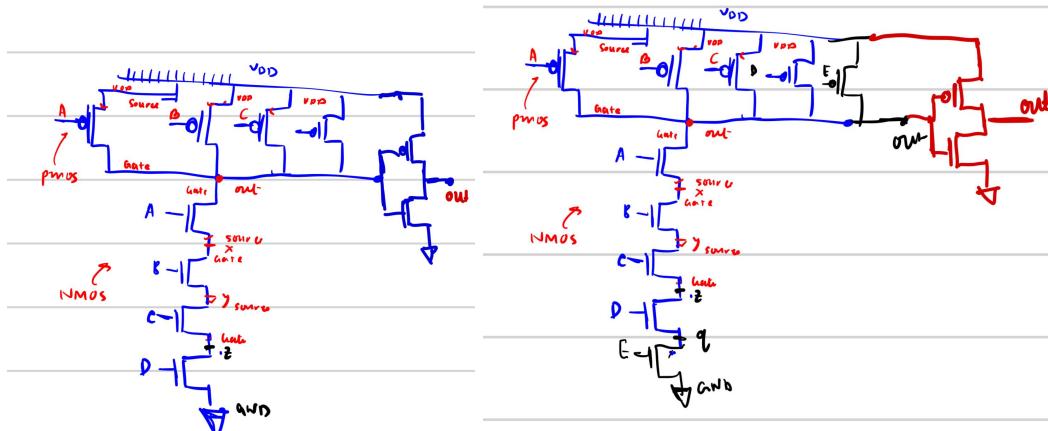
And:



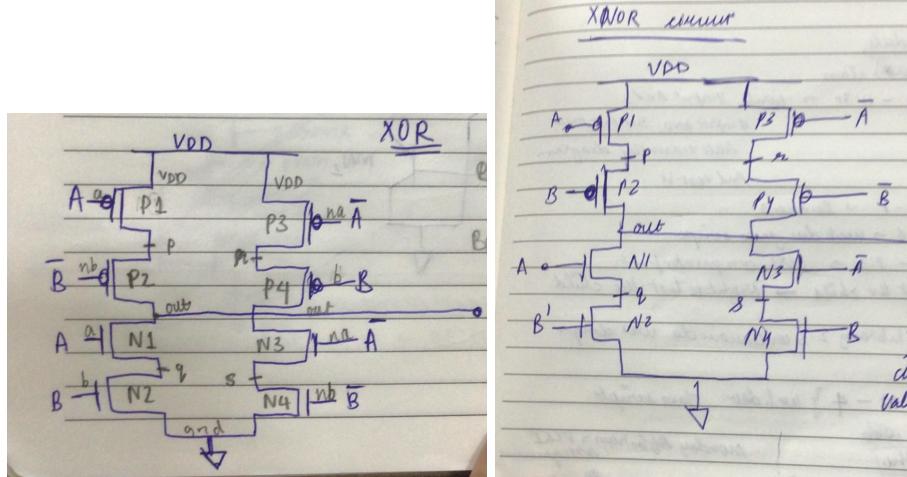
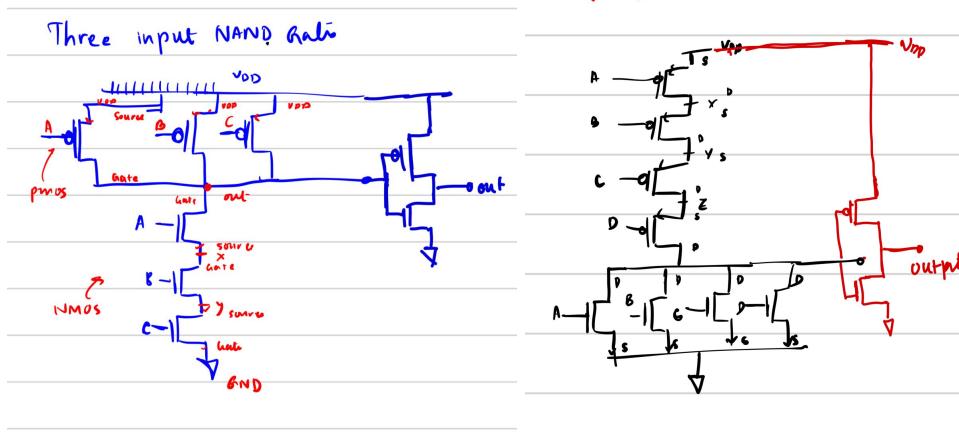
## Verilog plot:



## Ngspice Part:

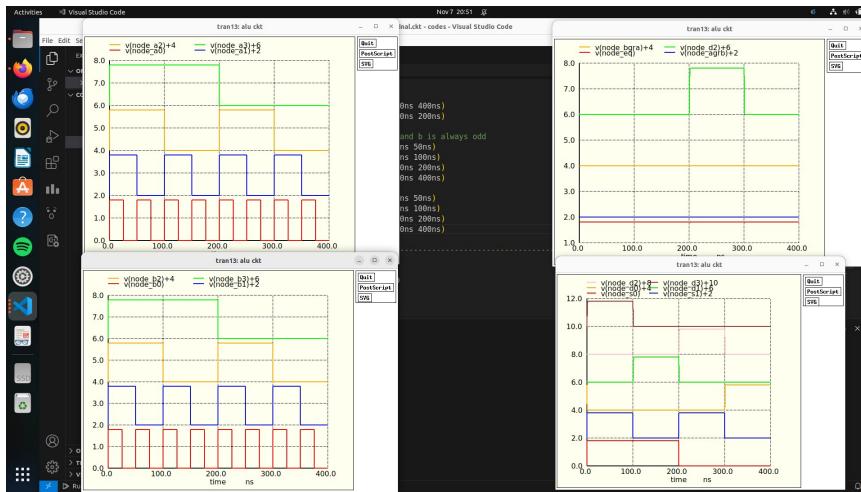


4 input NOR gates

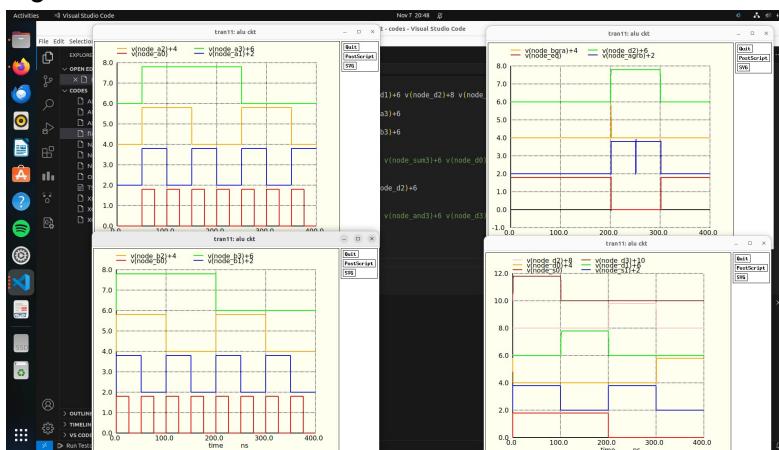


NGSPICE PLOTS:

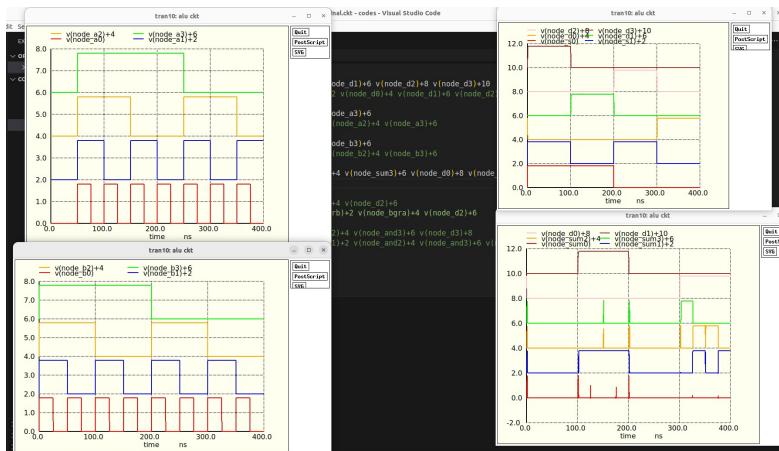
A equals B



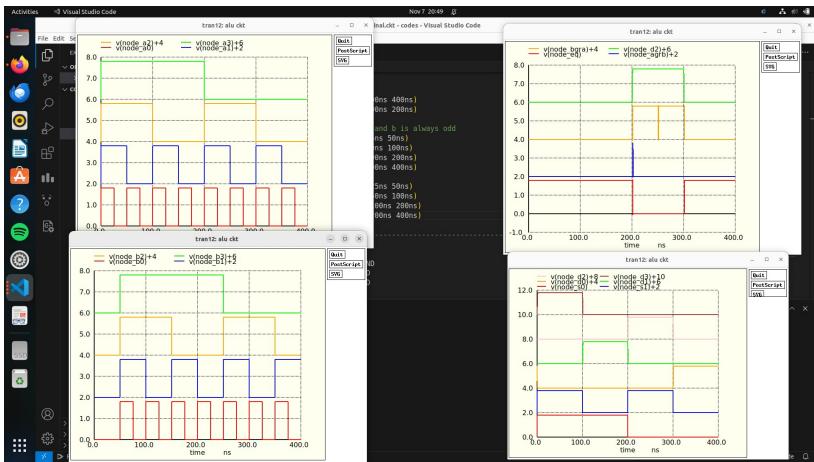
A greater than b



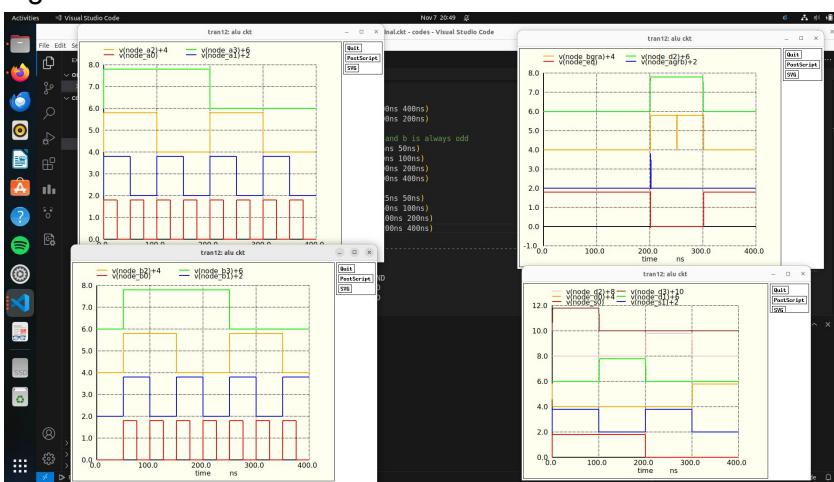
Adder subtractor outputs



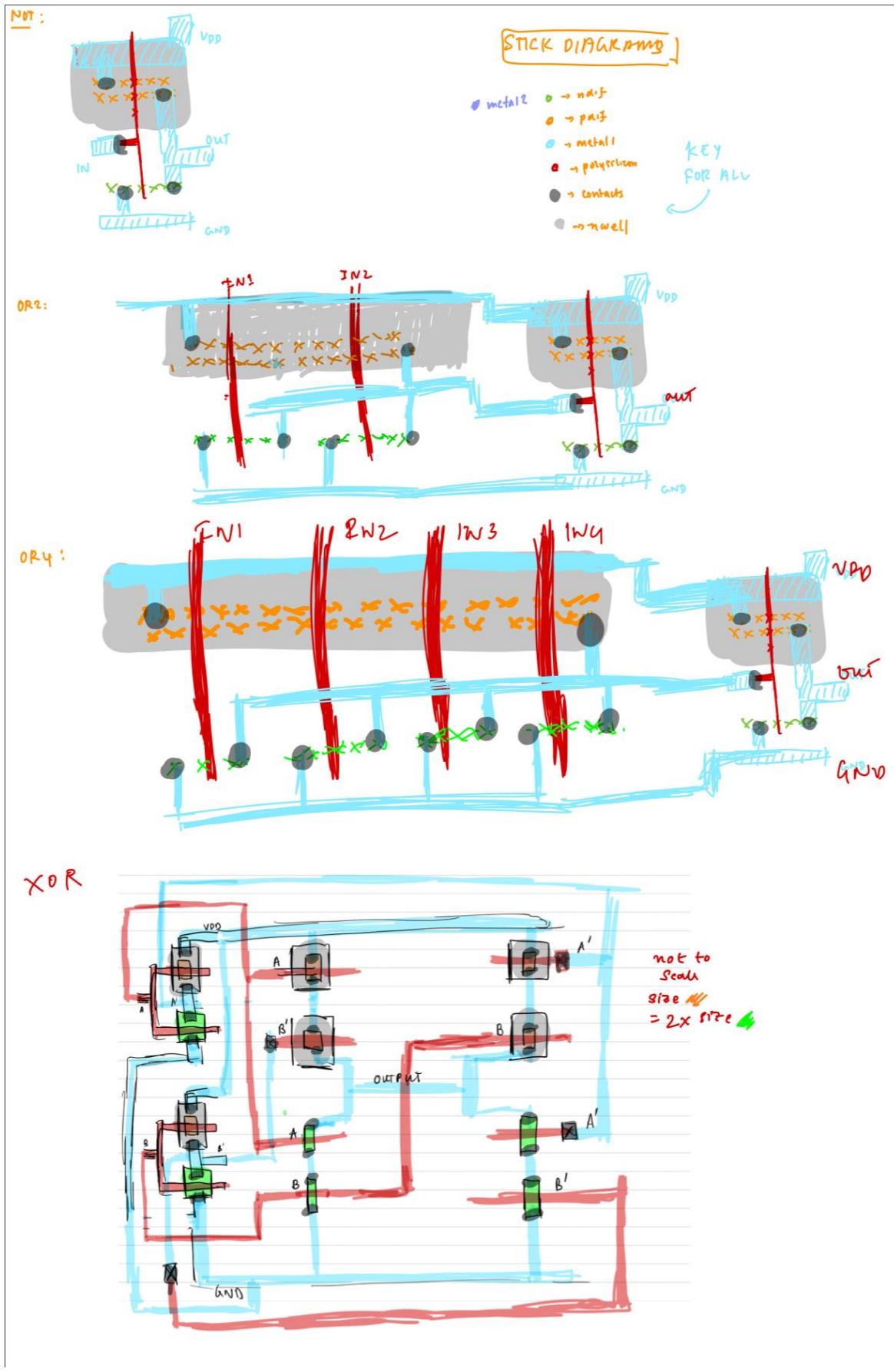
And outputs



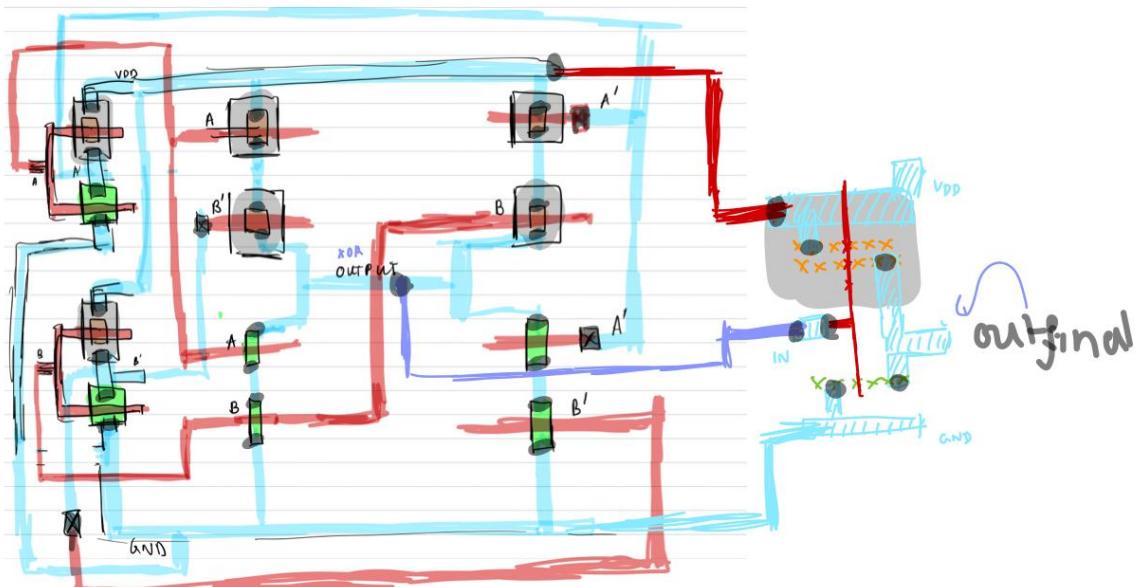
## B greater than A



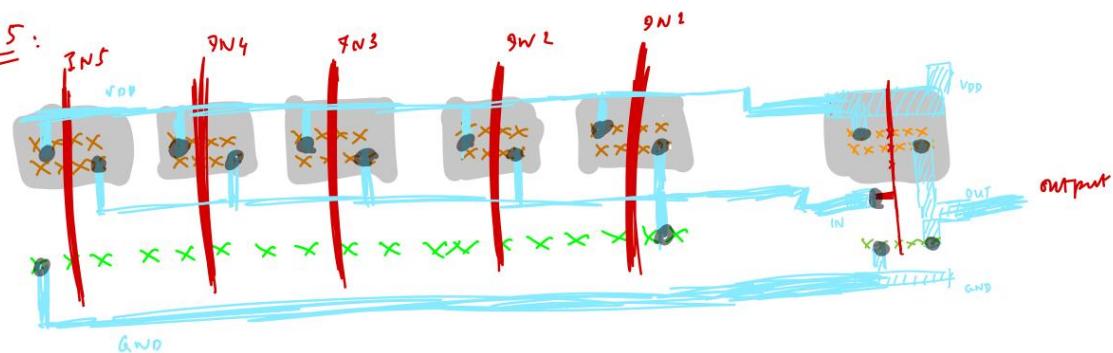
Magic Part: pto:



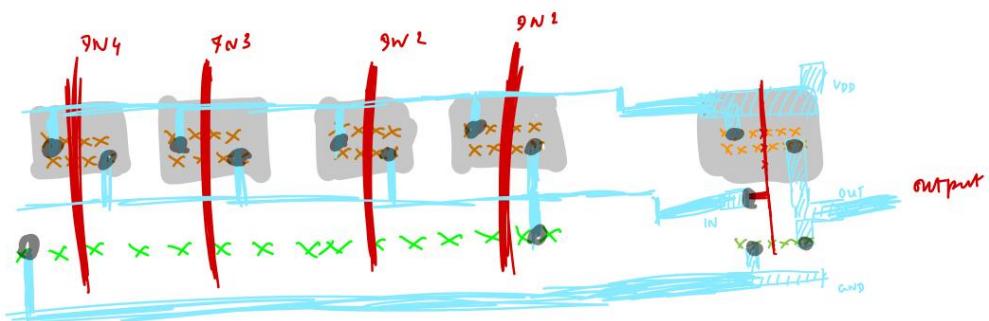
XNOR:



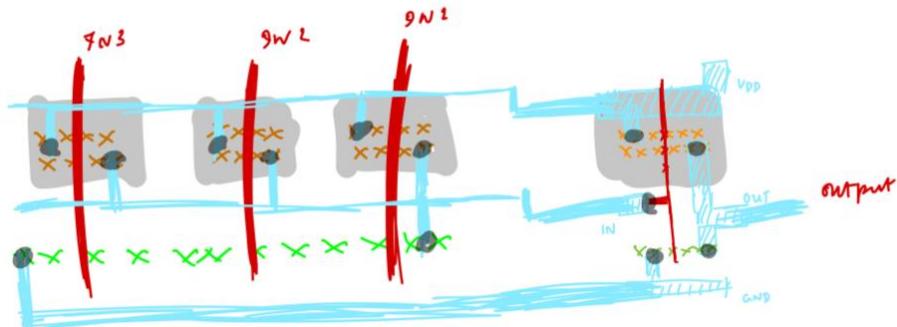
AND 5:



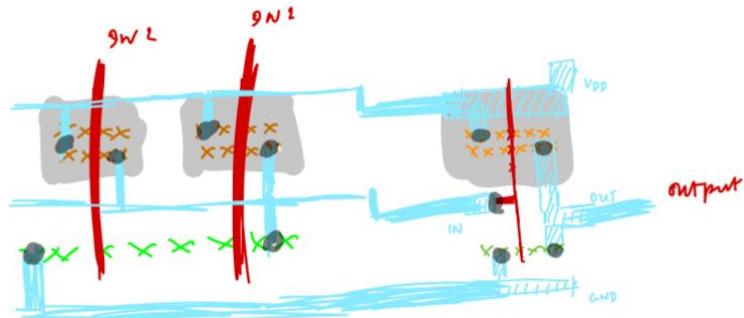
AND 4



AND3



AND2



Delay analysis:

Adder.txt contains maximum adder delay.

Subtracter.txt contains maximum subtracter delay

And.txt contains maximum delay in the and circuit

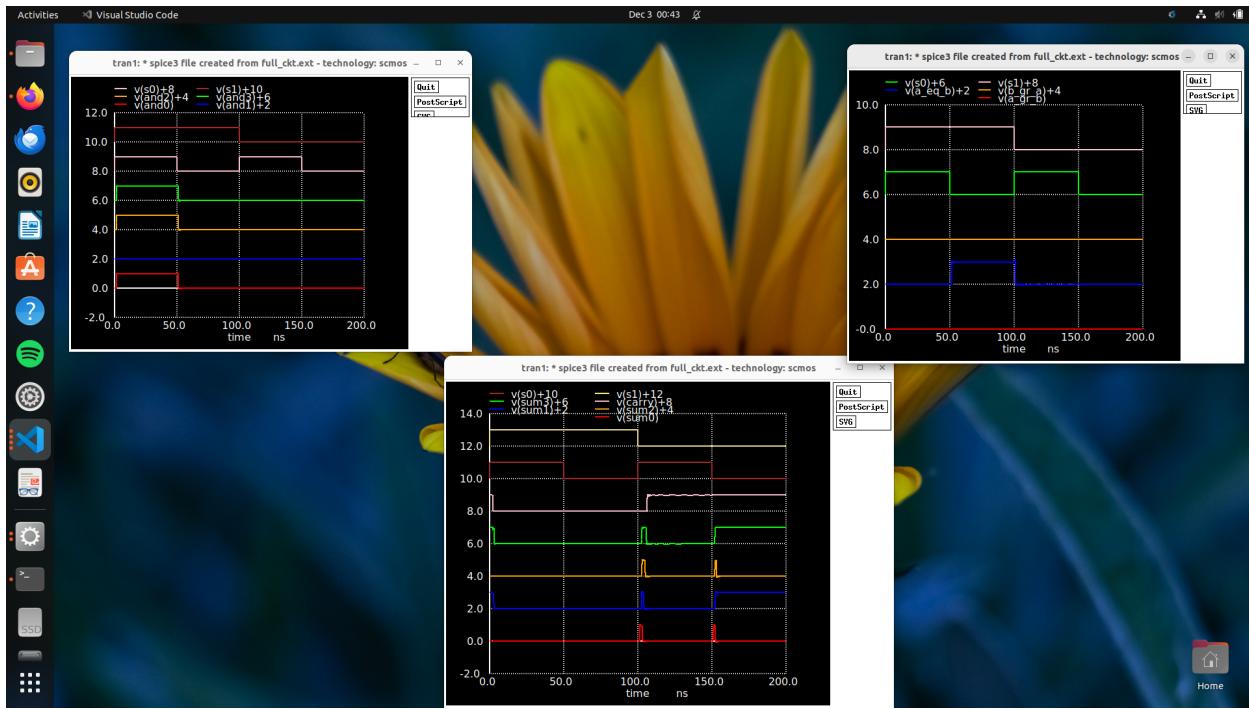
Greater.txt contains maximum delays between input and the  $a > b$  part of comparator

Lesser.txt contains maximum delays between input and the  $a < b$  part of the comparator

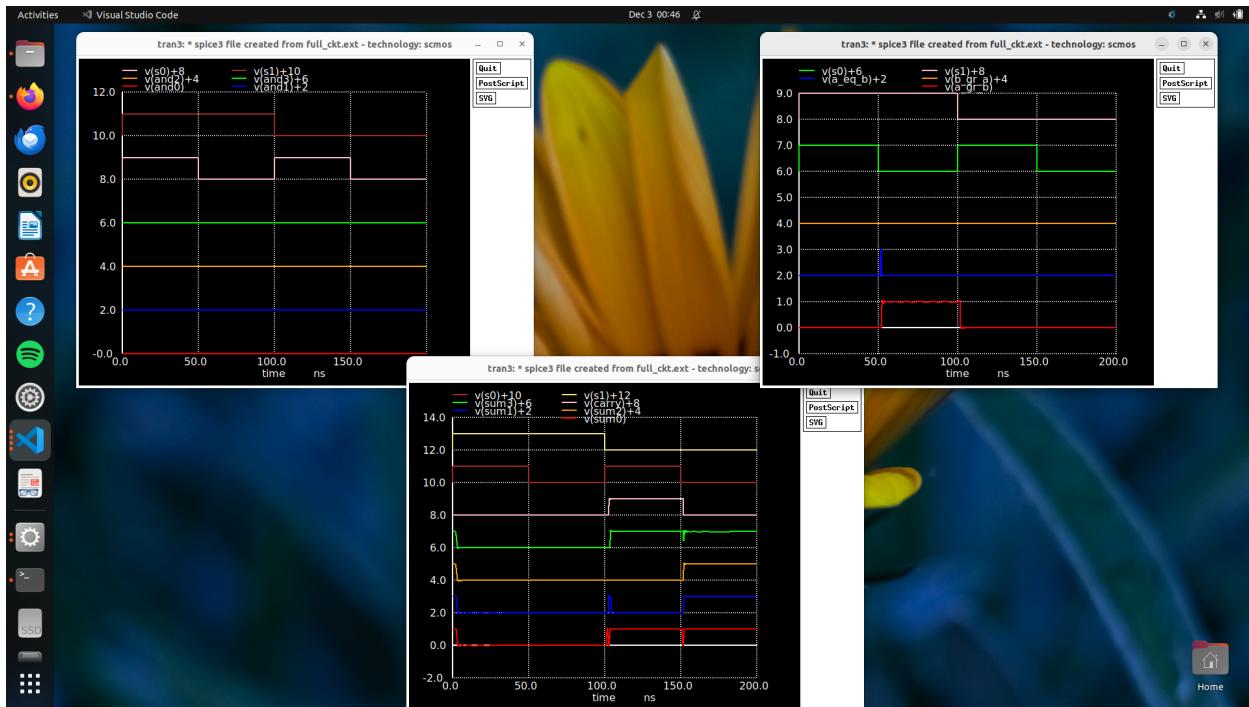
Equal.txt contains maximum delays between input and  $a = b$  part of the comparator

Magic Ngspice plots:

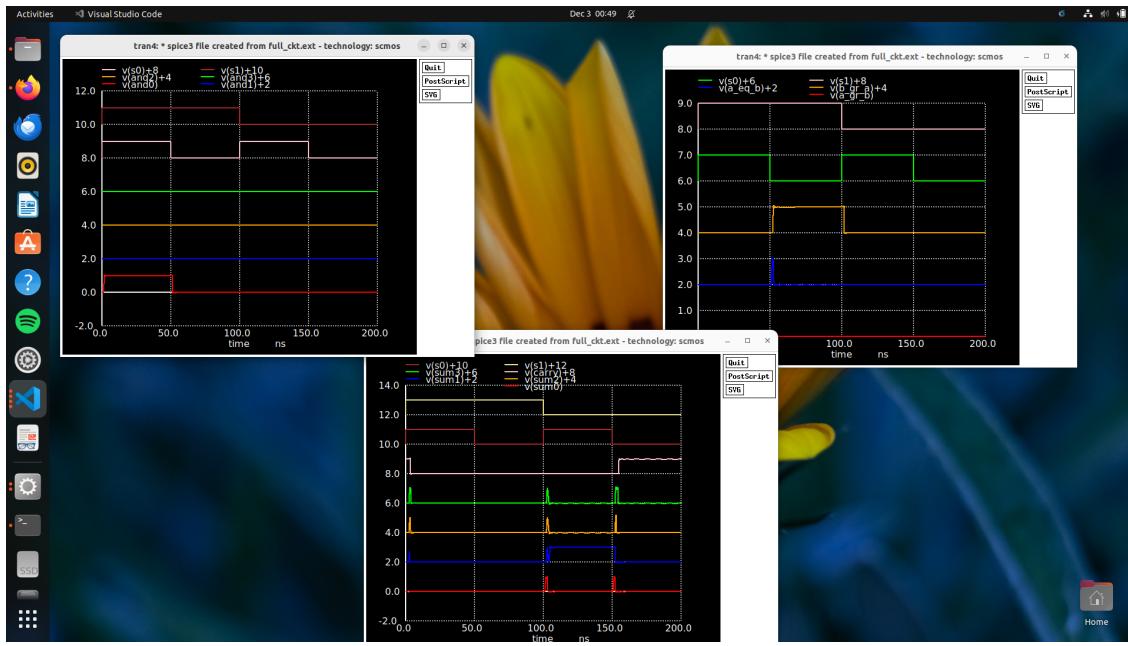
When A = 1101 B = 1101



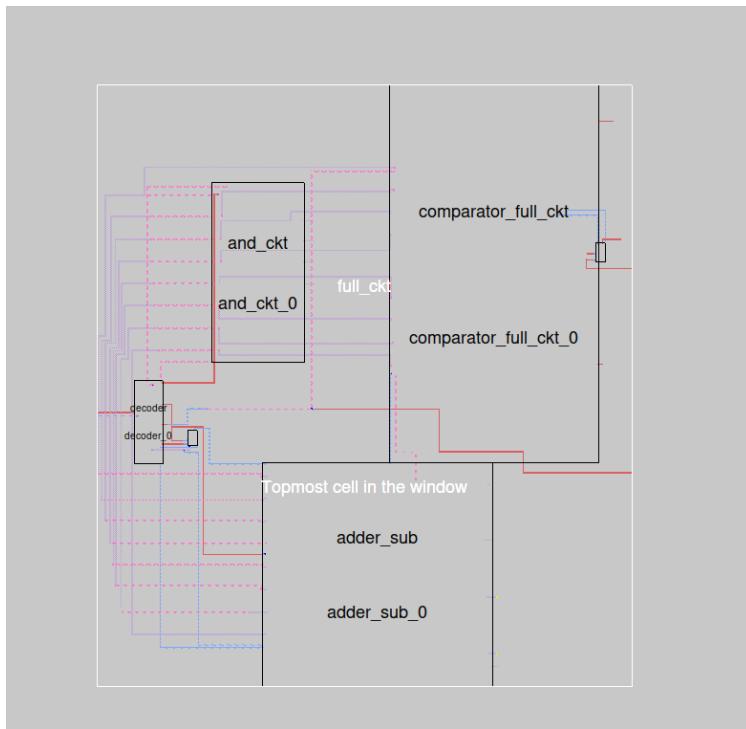
When A = 1100 B = 0011



When A = 0001 B = 1111

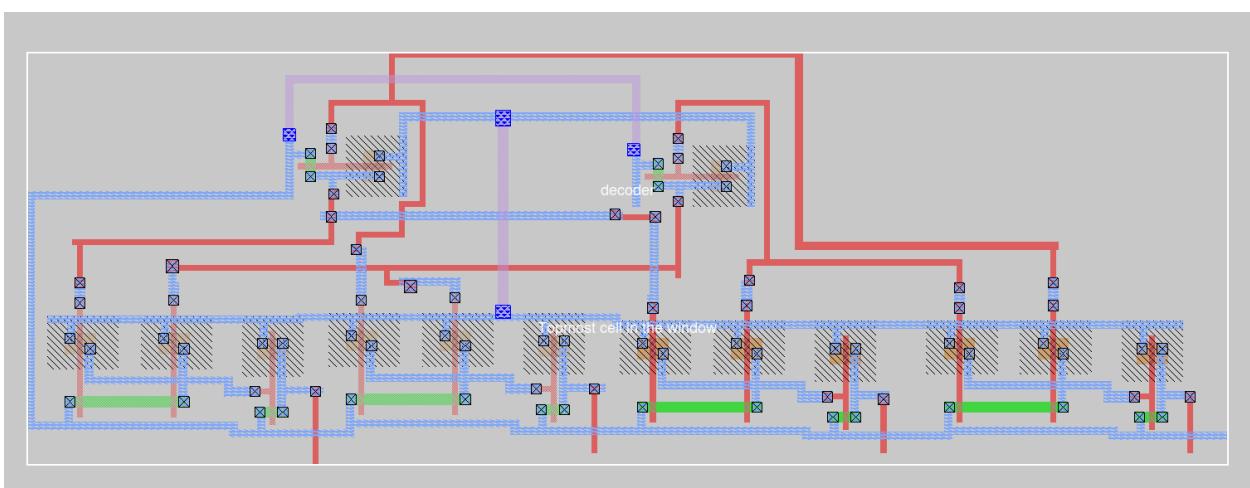


Magic diagrams:

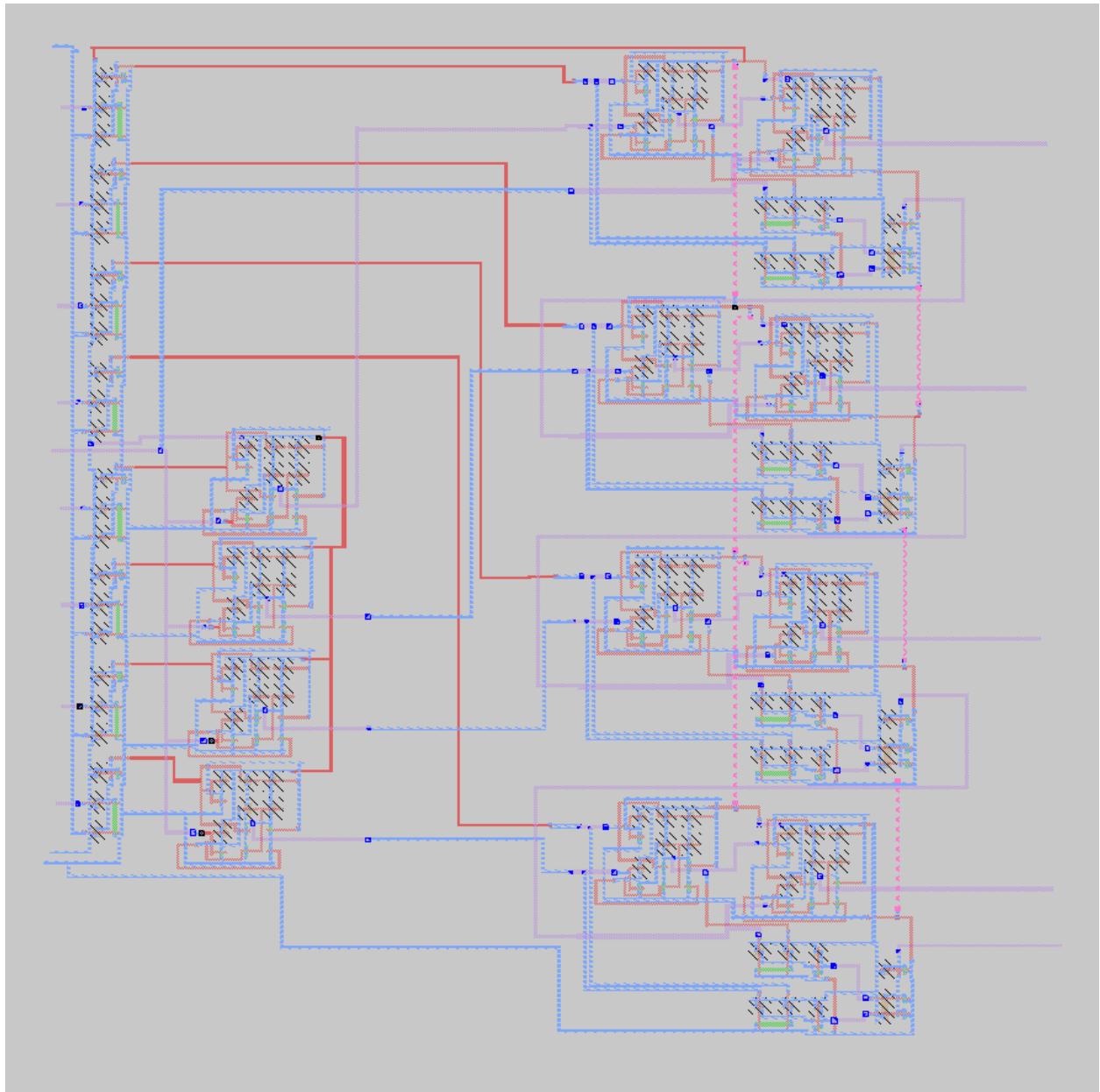




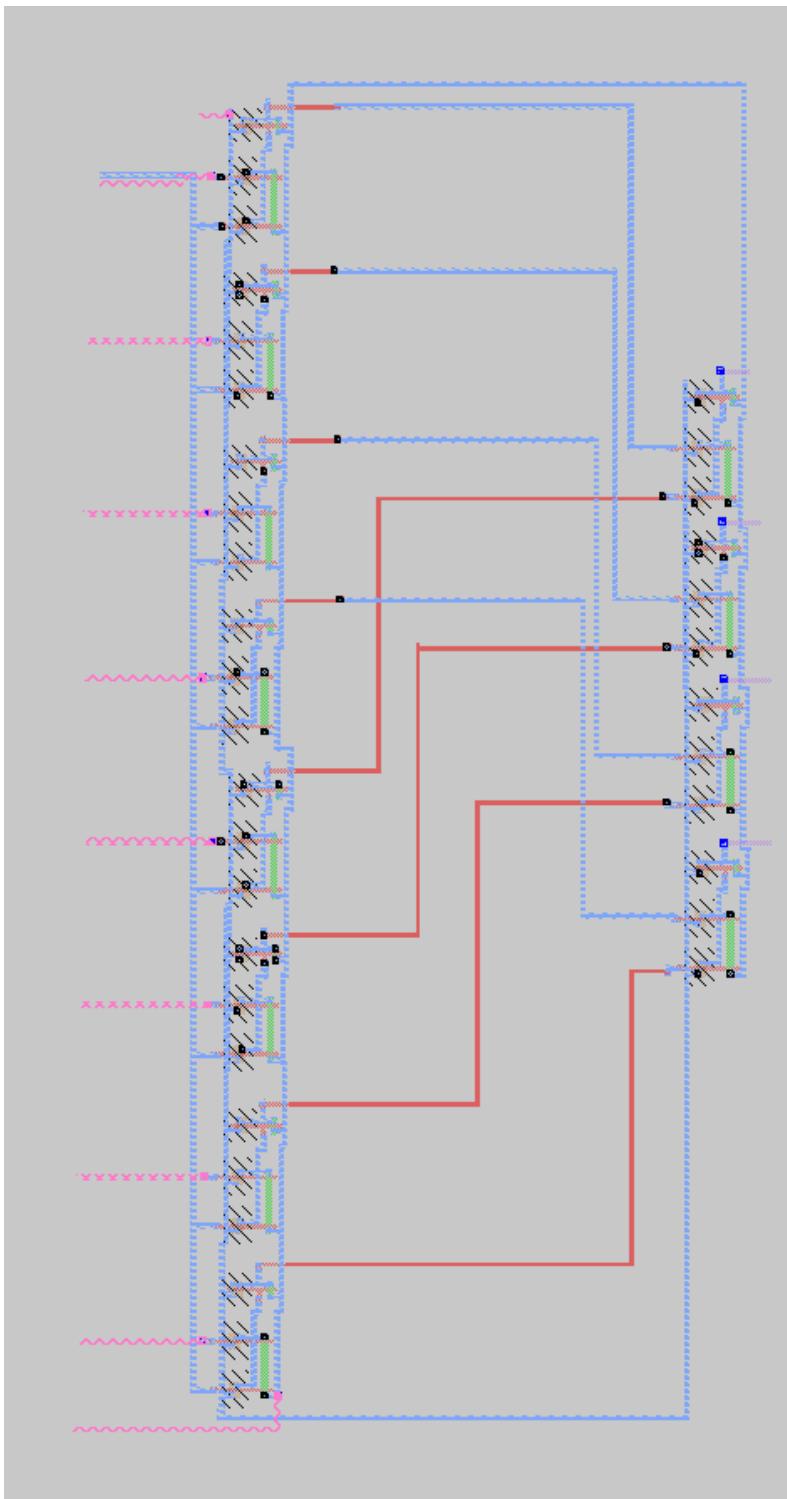
Decoder:



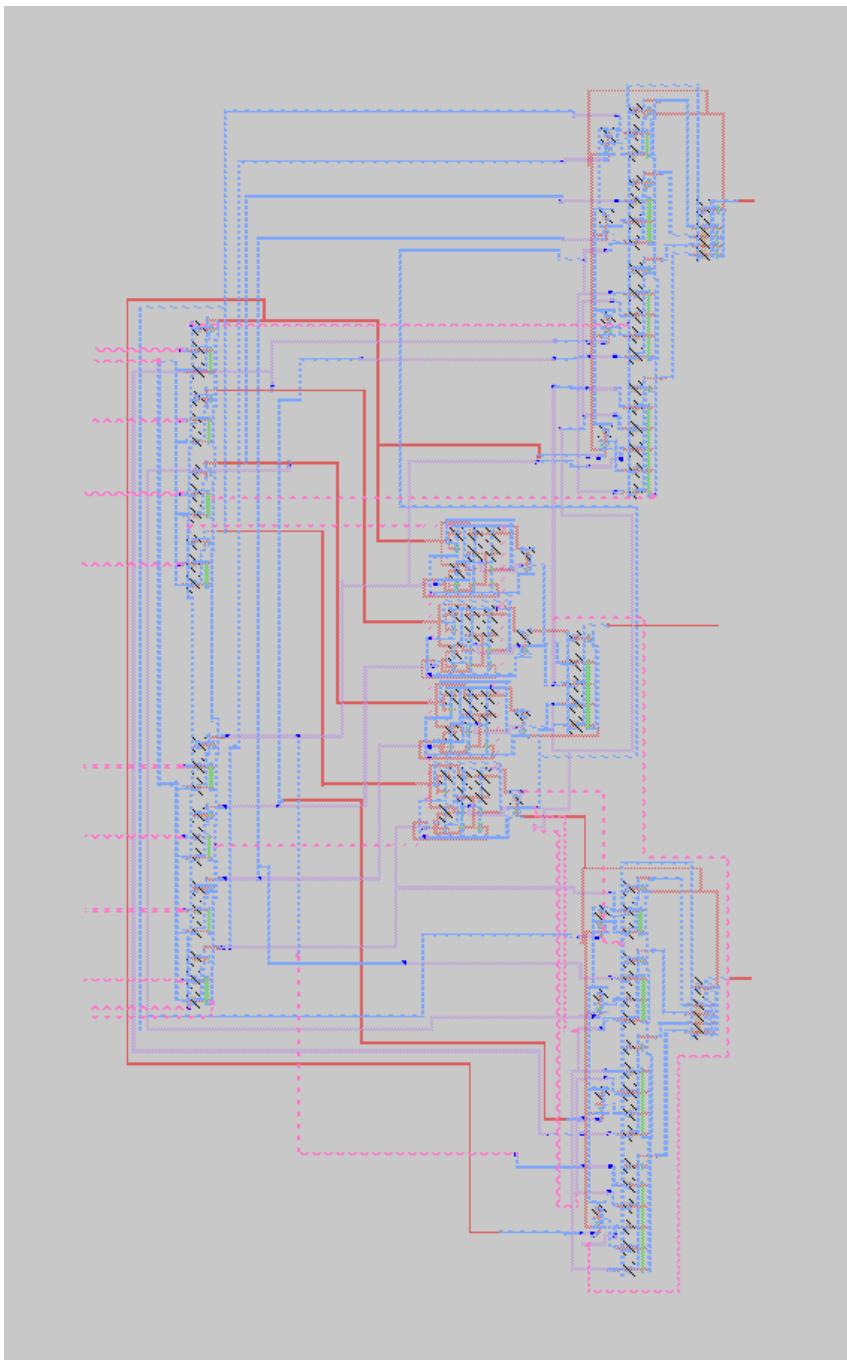
Adder Subtractor:



And circuit:



Comparator circuit:



#### Places of hardship and improvement:

- I realized during the midevals that my  $a=b$  was giving a high input even when the decoder is not switching on that circuit. I fixed that error by anding  $s_0 = \text{low}$   $s_1 = \text{high}$  and the final  $a==b$  output.
- Multiple times while I was building the magic circuit I saw that my output pulse was not reaching ground when it was supposed to. This is because the pull down circuit wasn't strong enough. I fixed this by usually checking for some ground connection errors. I

found that building the magic layout circuit actually helped me do error analysis using the vlsi concepts taught to us in class.

- I did not connect body to VDD using a contact in my magic layout circuit and this could be a source of error. Luckily, it seems to be default connected, or the voltage drop between the bodies and vdd is less enough that it isn't affecting my circuit in this ALU diagram. But this could be an area of concern
- My magic graphs has overshoots and prominent delays in some places. This could be fixed by changing the total capacitance of each of my gate transistor diagrams or subcircuits.