SONY

IMX709
MIPI D-PHY Global Timing parameters

Information on additional register settings to support MediaTek DX-1, DX-2, and DX-P

Both ($T_{HS-TRAIL}$ + $T_{CLK-POST}$ => 224 UI) &
($T_{HS-TRAIL}$ + $T_{HS-EXIT}$ => 224 UI + 70 ns)

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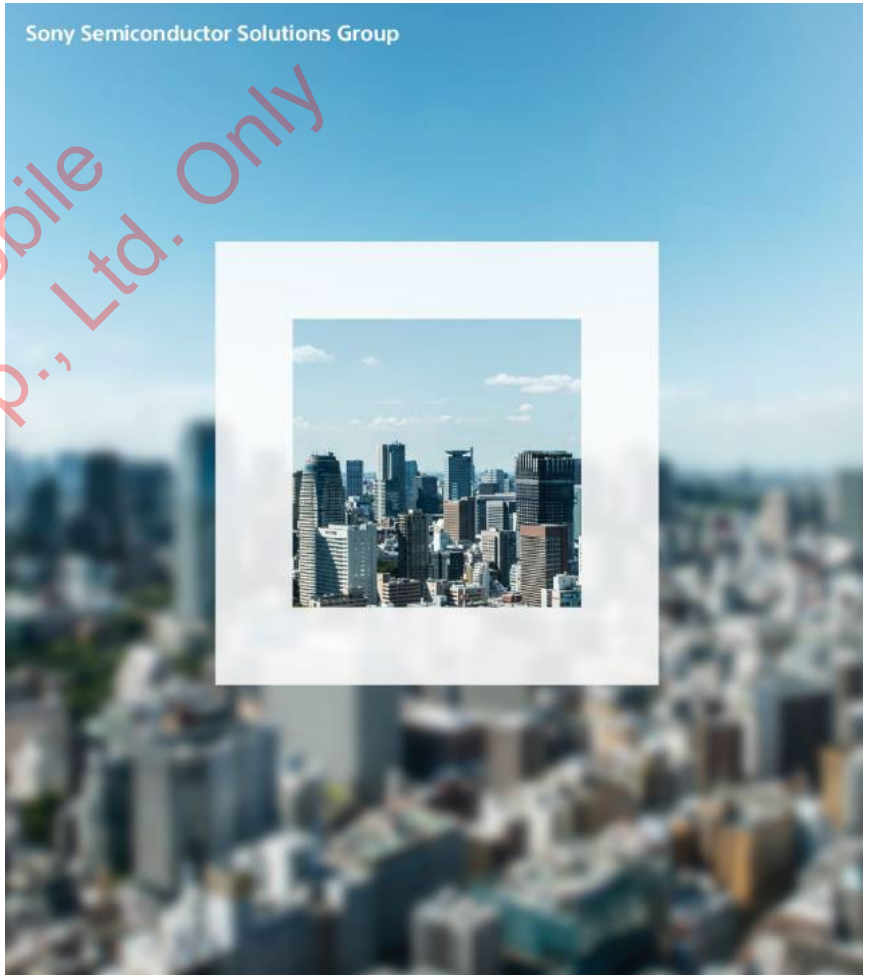
Mobile System Business Division
Sony Semiconductor Solutions Corporation



Revision History

Version	Date	Description
1.0	June 2, 2022	1st release
1.1	June 20, 2022	Additional information on reg_I9, reg_I9-1
1.2	July 29, 2022	reg_B3_1, reg_I5_1, reg_C5_1, reg_B3_2, and reg_B3_3 were added
1.3	Aug. 3, 2022	Name of register setting file was updated
1.4	Aug. 22, 2022	reg_I5_2, reg_C5_2, reg_C4-3-9, and reg_C4-3-11 were added
1.5	Aug. 25, 2022	Name of register setting file was revised
1.6	Sep. 1, 2022	reg_H2 was added
1.7	Sep. 28, 2022	reg_I5_2 and reg_C5_2 were updated
1.8	Nov. 24, 2022	reg_H3 was added
1.9	Feb. 16, 2023	reg_N-2, reg_N-3, reg_C4-3, reg_C4-5, and reg_C4-3-14 were added
1.91	Feb. 21, 2023	Name of register setting file was updated
2.0	Feb. 27, 2023	reg_H-4 was added
2.1	Mar. 3, 2023	reg_C-4-3-14 was updated
3.0	Apr. 28, 2023	reg_N-3-LLP was added
4.0	June 5, 2023	reg_N-4 was added
5.0	June 9, 2023	reg_H5 was added

Additional settings for MIPI D-PHY Global Operation Timing Parameters

Dedicated information for register settings in (MTK_NewAP)IMX709V_OPPO-DPHY-1.8V-24M_RegisterSetting_ver22.00-7.00_230608.xlsx.
Additional register settings in the table below support both $T_{HS-TRAIL} + T_{CLK-POST}$ => 224 UI & $T_{HS-TRAIL} + T_{HS-EXIT}$ => 224 UI + 70 ns.
(Reg_A_4, Reg_I9, and Reg_I9-1 meet the requirements without the additional register writes.)

I^2C Write address	I^2C Read address	Register Name	reg_G_2 1040 Mbps	reg_H 300 Mbps	reg_I3 1045 Mbps	reg_C3 1050 Mbps	reg_B6 1992 Mbps	reg_A_5 1303 Mbps	reg_B3 878 Mbps	reg_I5 1102 Mbps	reg_C5 1102 Mbps	reg_A_3 1310 Mbps	reg_E1_1 307 Mbps	reg_H1 307 Mbps	reg_B9 1435 Mbps
0x0808	0x0808	PHY_CTRL	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02
0x080A	0xD930	TCLK_POST_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080B	0xD931	TCLK_POST_EX[7:0]	0x97	0xC7	0x97	0x97	0xDF	0xAF	0x9F	0x8F	0x8F	0xAF	0xC7	0xC7	0xAF
0x080C	0xD932	THS_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080D	0xD933	THS_PREPARE_EX[7:0]	0x4F	0x17	0x4F	0x4F	0x87	0x5F	0x3F	0x4F	0x4F	0x5F	0x17	0x17	0x6F
0x080E	0xD934	THS_ZERO_MIN_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080F	0xD935	THS_ZERO_MIN_EX[7:0]	0x7F	0x2F	0x7F	0x7F	0xFF	0xAF	0x7F	0x8F	0x8F	0xAF	0x2F	0x2F	0xAF
0x0810	0xD936	THS_TRAIL_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0811	0xD937	THS_TRAIL_EX[7:0]	0x47	0x17	0x47	0x47	0x87	0x5F	0x3F	0x4F	0x4F	0x5F	0x17	0x17	0x67
0x0812	0xD938	TCLK_TRAIL_MIN_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0813	0xD939	TCLK_TRAIL_MIN_EX[7:0]	0x47	0x17	0x47	0x47	0x87	0x57	0x3F	0x47	0x47	0x57	0x17	0x17	0x5F
0x0814	0xD93A	TCLK_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0815	0xD93B	TCLK_PREPARE_EX[7:0]	0x4F	0x17	0x4F	0x4F	0x7F	0x57	0x3F	0x4F	0x4F	0x57	0x17	0x17	0x5F
0x0816	0xD93C	TCLK_ZERO_EX[9:8]	0x01	0x00	0x01	0x01	0x02	0x01	0x01	0x01	0x01	0x01	0x00	0x00	0x01
0x0817	0xD93D	TCLK_ZERO_EX[7:0]	0x1F	0x5F	0x1F	0x1F	0x3F	0x8F	0x0F	0x2F	0x2F	0x8F	0x5F	0x5F	0xAF
0x0818	0xD93E	TLPX_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0819	0xD93F	TLPX_EX[7:0]	0x3F	0x1F	0x3F	0x3F	0x6F	0x4F	0x3F	0x3F	0x3F	0x4F	0x1F	0x1F	0x4F
0x0824	0xD940	THS_EXIT_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0825	0xD941	THS_EXIT_EX[7:0]	0xE1	0xDD	0xE1	0xE1	0xE5	0xDF	0xE1	0xDD	0xDD	0xDF	0xDD	0xDD	0xDF
0x0826	0xD942	TCLK_PRE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0827	0xD943	TCLK_PRE_EX[7:0]	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F

Note 1: Any of register writes need to be done during SW-standby.
Note 2: Only during streaming, the reading registers can be accessed correctly.

Additional settings for MIPI D-PHY Global Operation Timing Parameters (cont'd)

Dedicated information for register settings in (MTK_NewAP)IMX709V_OPPO-DPHY-1.8V-24M_RegisterSetting_ver22.00-7.00_230608.xlsx.
Additional register settings in the table below support both $T_{HS-TRAIL}$ + $T_{CLK-POST}$ => 224 UI & $T_{HS-TRAIL}$ + $T_{HS-EXIT}$ => 224 UI + 70 ns.
(Reg_A_4, Reg_I9, and Reg_I9-1 meet the requirements without the additional register writes.)

I^2C Write address	I^2C Read address	Register Name	reg_M 300 Mbps	reg_B3_1 1052 Mbps	reg_I5_1 1118 Mbps	reg_C5_1 1118 Mbps	reg_B3_2 759 Mbps	reg_B3_3 1118 Mbps	reg_I5_2 1359 Mbps	reg_C5_2 1359 Mbps	reg_C4-3-9 1168 Mbps	reg_C4-3-11 1145 Mbps	reg_H2 926 Mbps	reg_H3 457 Mbps
0x0808	0x0808	PHY_CTRL	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02
0x080A	0xD930	TCLK_POST_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080B	0xD931	TCLK_POST_EX[7:0]	0xC7	0x8F	0x8F	0x8F	0xA7	0x8F	0xAF	0xAF	0x9F	0x9F	0x9F	0xB7
0x080C	0xD932	THS_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080D	0xD933	THS_PREPARE_EX[7:0]	0x17	0x4F	0x4F	0x4F	0x3F	0x4F	0x5F	0x5F	0x4F	0x4F	0x3F	0x27
0x080E	0xD934	THS_ZERO_MIN_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080F	0xD935	THS_ZERO_MIN_EX[7:0]	0x2F	0x7F	0x8F	0x8F	0x5F	0x8F	0xAF	0xAF	0x9F	0x9F	0x7F	0x3F
0x0810	0xD936	THS_TRAIL_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0811	0xD937	THS_TRAIL_EX[7:0]	0x17	0x4F	0x4F	0x4F	0x37	0x4F	0x5F	0x5F	0x4F	0x4F	0x3F	0x27
0x0812	0xD938	TCLK_TRAIL_MIN_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0813	0xD939	TCLK_TRAIL_MIN_EX[7:0]	0x17	0x47	0x47	0x47	0x37	0x47	0x57	0x57	0x4F	0x4F	0x3F	0x1F
0x0814	0xD93A	TCLK_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0815	0xD93B	TCLK_PREPARE_EX[7:0]	0x17	0x4F	0x4F	0x4F	0x2F	0x4F	0x57	0x57	0x4F	0x4F	0x3F	0x1F
0x0816	0xD93C	TCLK_ZERO_EX[9:8]	0x00	0x01	0x01	0x01	0x00	0x01	0x01	0x01	0x01	0x01	0x01	0x00
0x0817	0xD93D	TCLK_ZERO_EX[7:0]	0x5F	0x2F	0x3F	0x3F	0xDF	0x3F	0x8F	0x8F	0x4F	0x4F	0x0F	0x8F
0x0818	0xD93E	TLPX_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0819	0xD93F	TLPX_EX[7:0]	0x1F	0x3F	0x3F	0x3F	0x2F	0x3F	0x4F	0x4F	0x3F	0x3F	0x3F	0x1F
0x0824	0xD940	THS_EXIT_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0825	0xD941	THS_EXIT_EX[7:0]	0xDD	0xDB	0xDF	0xDF	0xDF	0xDF	0xDF	0xDF	0xE3	0xE3	0xE1	0xD9
0x0826	0xD942	TCLK_PRE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0827	0xD943	TCLK_PRE_EX[7:0]	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F

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(Reg_A_4, Reg_I9, and Reg_I9-1 meet the requirements without the additional register writes.)

I^2C Write address	I^2C Read address	Register Name	reg_N-2 1160 Mbps	reg_N-3 1160 Mbps	reg_C4-3 1198 Mbps	reg_C4-5 1198 Mbps	reg_C4-3-14 1112 Mbps	reg_H4 469 Mbps	reg_N-3-LLP 1160 Mbps	reg_N-4 1160 Mbps	reg_H5 1160 Mbps
0x0808	0x0808	PHY_CTRL	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02
0x080A	0xD930	TCLK_POST_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080B	0xD931	TCLK_POST_EX[7:0]	0x9F	0x9F	0x9F	0x9F	0x8F	0xB7	0x9F	0x9F	0x9F
0x080C	0xD932	THS_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080D	0xD933	THS_PREPARE_EX[7:0]	0x4F	0x4F	0x5F	0x5F	0x4F	0x27	0x4F	0x4F	0x4F
0x080E	0xD934	THS_ZERO_MIN_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080F	0xD935	THS_ZERO_MIN_EX[7:0]	0x9F	0x9F	0x9F	0x9F	0x8F	0x3F	0x9F	0x9F	0x9F
0x0810	0xD936	THS_TRAIL_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0811	0xD937	THS_TRAIL_EX[7:0]	0x4F	0x4F	0x57	0x57	0x4F	0x27	0x4F	0x4F	0x4F
0x0812	0xD938	TCLK_TRAIL_MIN_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0813	0xD939	TCLK_TRAIL_MIN_EX[7:0]	0x4F	0x4F	0x4F	0x4F	0x47	0x1F	0x4F	0x4F	0x4F
0x0814	0xD93A	TCLK_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0815	0xD93B	TCLK_PREPARE_EX[7:0]	0x4F	0x4F	0x4F	0x4F	0x4F	0x1F	0x4F	0x4F	0x4F
0x0816	0xD93C	TCLK_ZERO_EX[9:8]	0x01	0x01	0x01	0x01	0x01	0x00	0x01	0x01	0x01
0x0817	0xD93D	TCLK_ZERO_EX[7:0]	0x4F	0x4F	0x5F	0x5F	0x3F	0x8F	0x4F	0x4F	0x4F
0x0818	0xD93E	TLPX_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0819	0xD93F	TLPX_EX[7:0]	0x3F	0x3F	0x4F	0x4F	0x3F	0x1F	0x3F	0x3F	0x3F
0x0824	0xD940	THS_EXIT_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0825	0xD941	THS_EXIT_EX[7:0]	0xE3	0xE3	0xDF	0xDF	0xDF	0xDB	0xE3	0xE3	0xE3
0x0826	0xD942	TCLK_PRE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0827	0xD943	TCLK_PRE_EX[7:0]	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F

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