



GVI KXZ7C01 Zynq Connectivity Kit

GTX IBERT Design Creation: Fiber Loop Back QuickStart

December 2017

Order Hardware:

<https://detail.tmall.com/item.htm?id=562769965498>

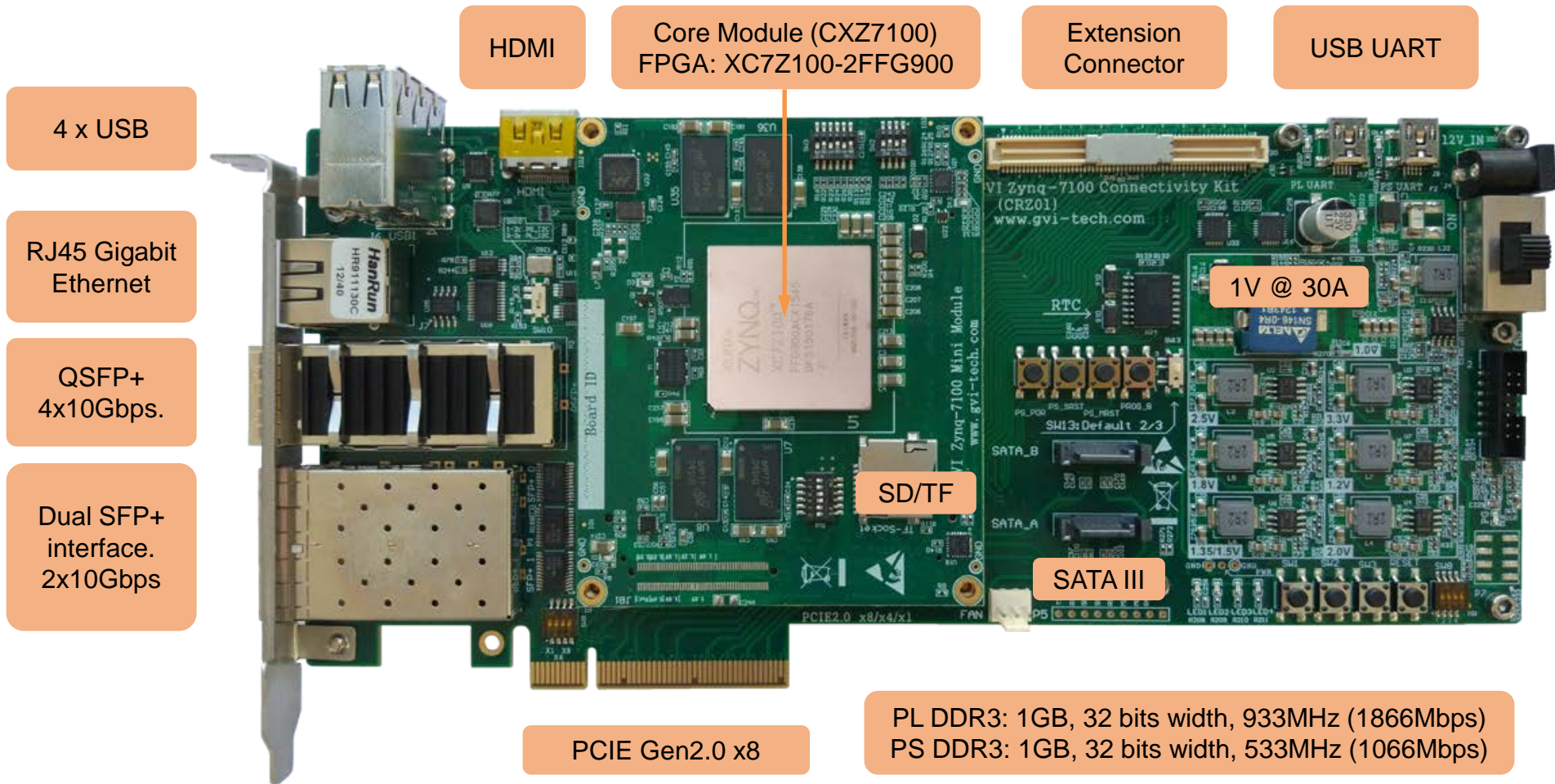
<http://www.gvi-tech.com/products-fpga-kits>

杭州言曼科技有限公司

Overview

- GVI KXZ7C01 Zynq Connectivity Kit Overview
- Software Requirements
- Create IBERT Design
- Hardware Setup
- Run IBERT with 10G Fiber Module
- References

GVI Zynq Connectivity Kit – KXZ7C01



Xilinx Software Requirement

- Xilinx Vivado Design Suite (version 2016.4 is used for development)



IBERT Overview

- Description

The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the GTX transceivers. A graphical user interface is provided through the Vivado Hardware Manager.

- Reference Design IP

LogiCORE IBERT Example Designs

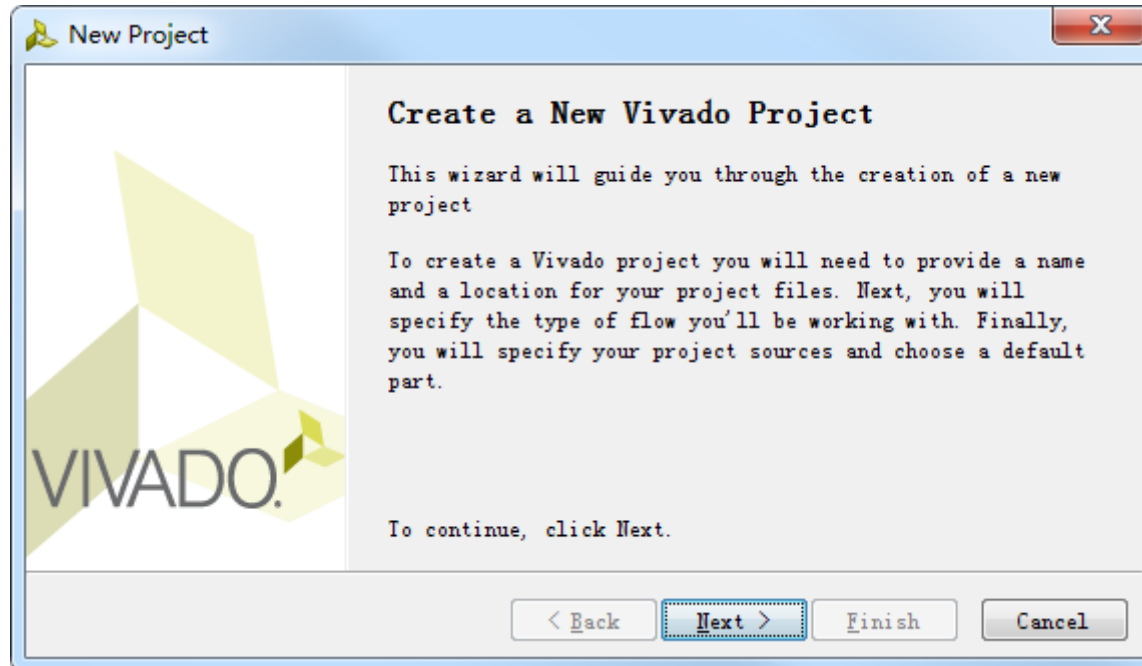
Create IBERT Design

- Open Vivado
 - Start → All Programs → Xilinx Design Tools → Vivado 2016.4 → Vivado
- Select Create New Project



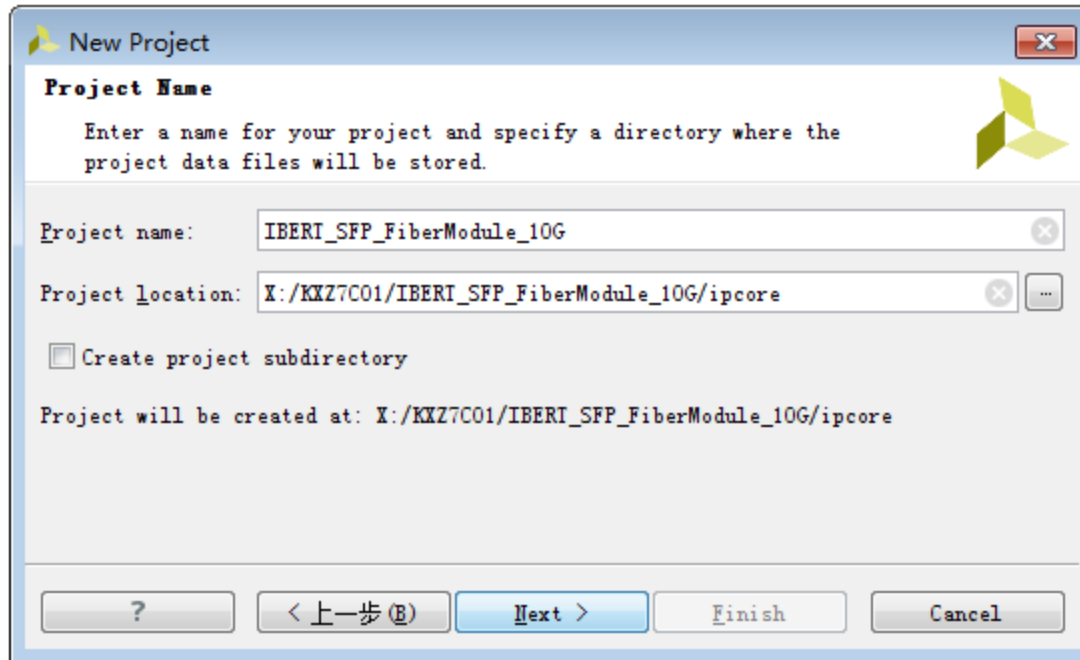
Create IBERT Design

- Click Next



Create IBERT Design

- Set the Project name and location; check Create project subdirectory



New Project

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

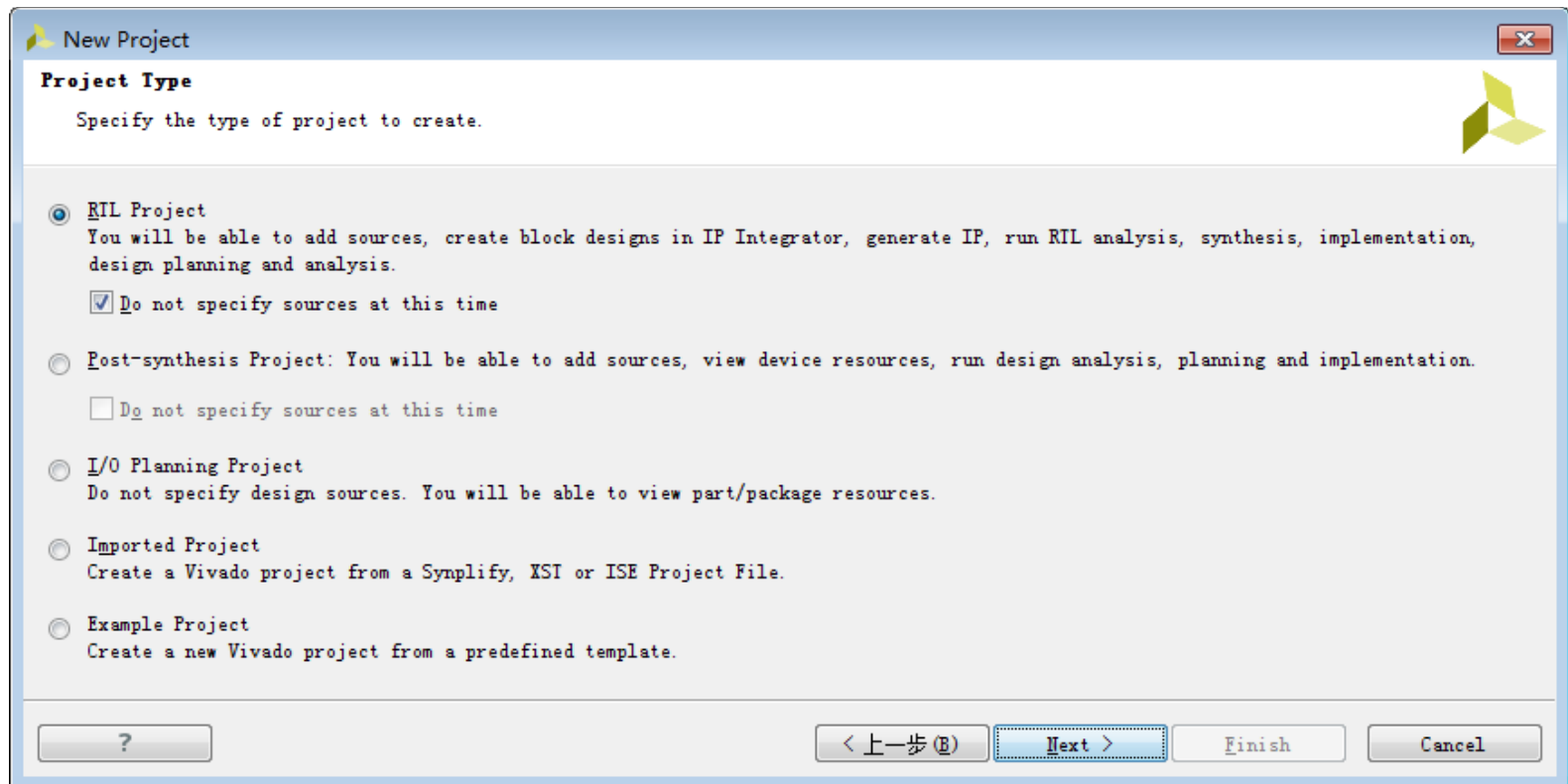
☐ Create project subdirectory

Project will be created at: X:/KXZ7C01/IBERI_SFP_FiberModule_10G/ipcore

? < 上一步(B) Next > Finish Cancel

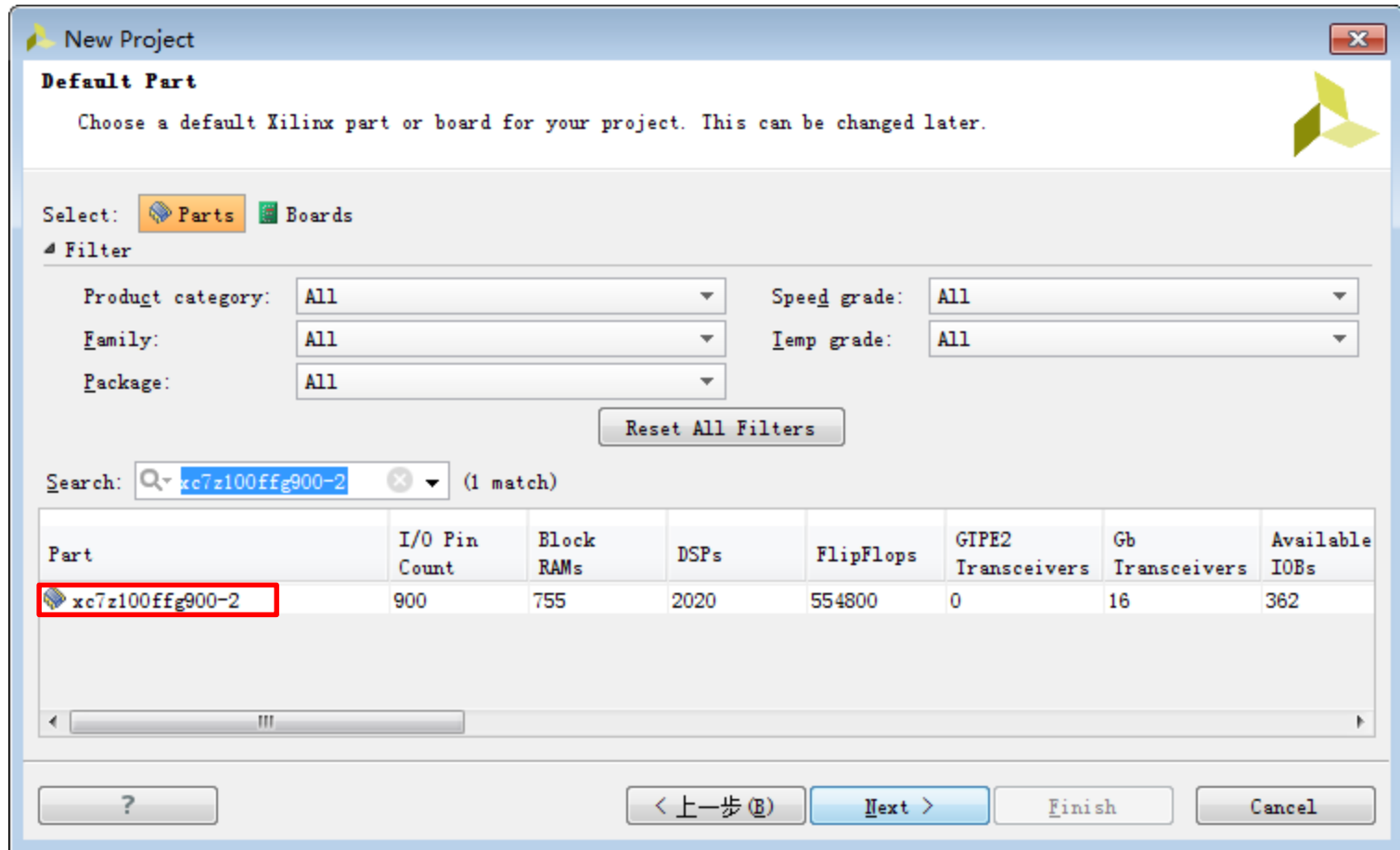
Create IBERT Design

- Select RTL Project
 - Select Do not specify sources at this time



Create IBERT Design

- Select the FPGA part number: xc7z100ffg900-2

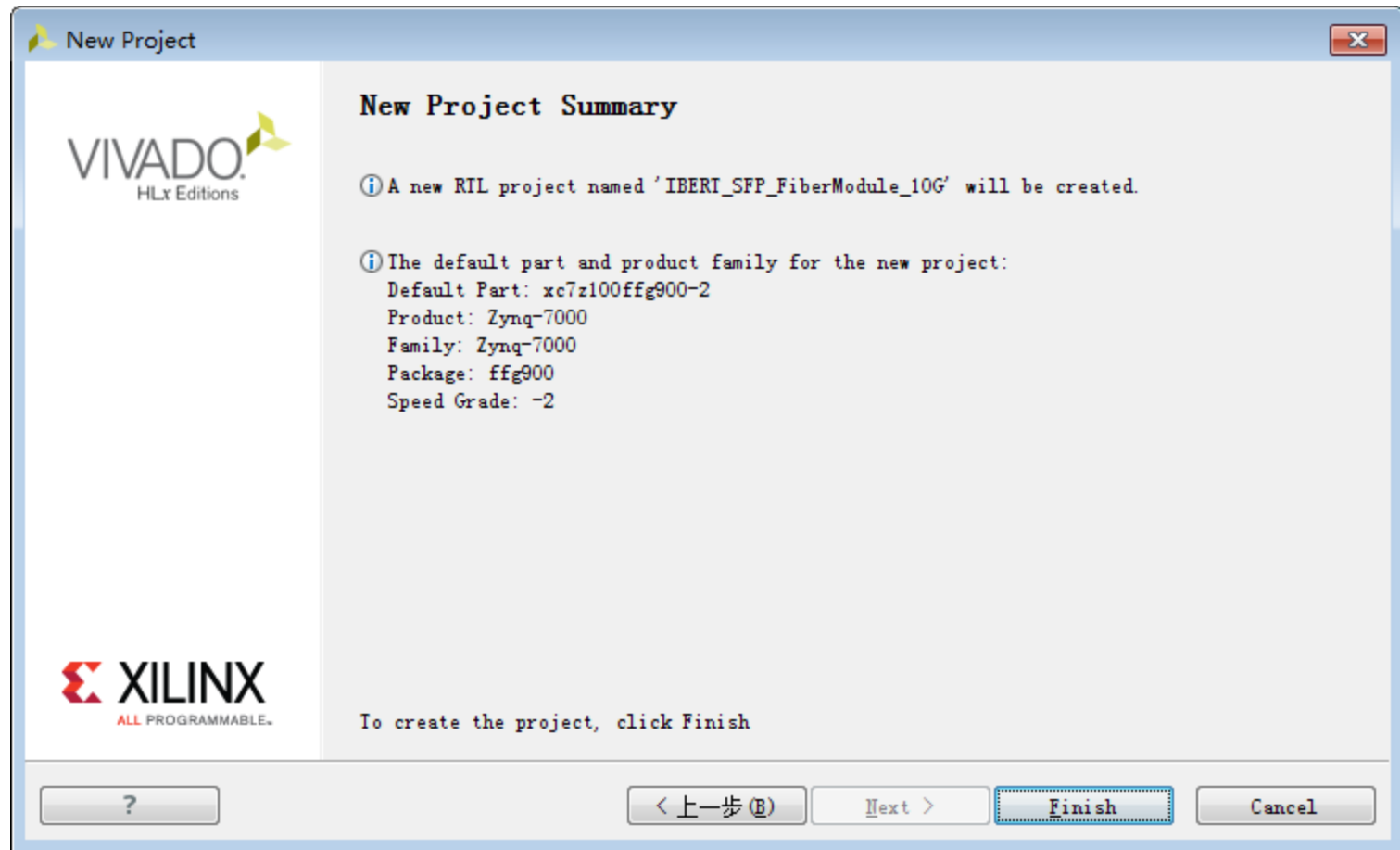


The image shows the 'New Project' dialog box in Xilinx IDE. The 'Default Part' section is active, and the 'Parts' tab is selected. The search bar contains 'xc7z100ffg900-2', and a table below shows the search results. The first result, 'xc7z100ffg900-2', is highlighted with a red box. The table columns are: Part, I/O Pin Count, Block RAMs, DSPs, FlipFlops, GPIPE2 Transceivers, Gb Transceivers, and Available IOBs.

Part	I/O Pin Count	Block RAMs	DSPs	FlipFlops	GPIPE2 Transceivers	Gb Transceivers	Available IOBs
xc7z100ffg900-2	900	755	2020	554800	0	16	362

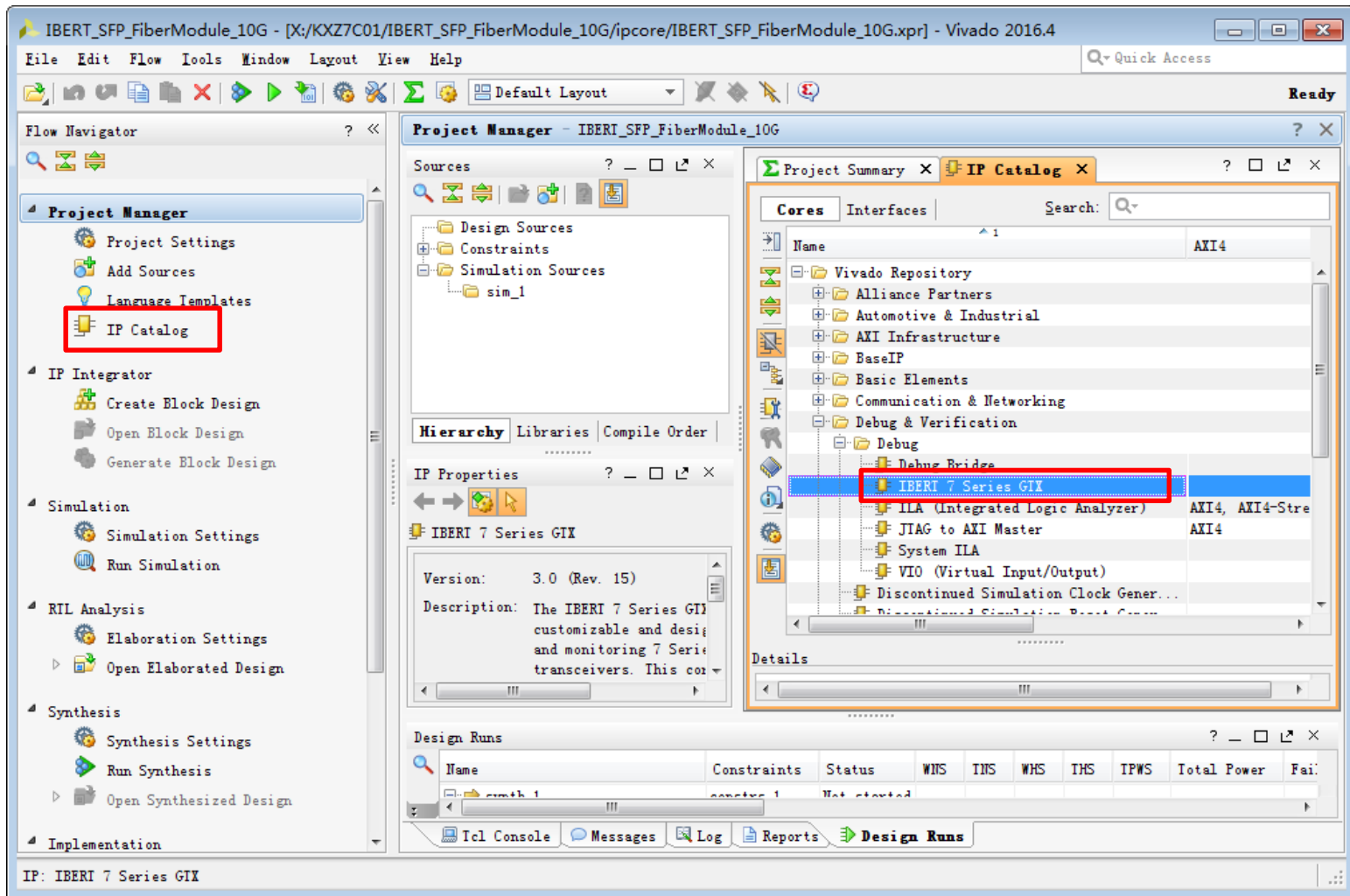
Create IBERT Design

- Click Finish



Create IBERT Design

- Click on IP Catalog, double click IBERT 7 Series GTX under Debug & Verification



Create IBERT Design

- Set the Component name: ibert_bank109
- Under the Protocol Definition tab, set the parameters as follows:

Customize IP

IBERT 7 Series GTX (3.0)

Documentation IP Location Switch to Defaults

☐ Show disabled ports

Component Name: ibert_bank109

Protocol Definition Protocol Selection Clock Settings Summary

Silicon Version

Silicon Version: General ES/Production

The maximum number of quads available for this device is 4

Number of Protocols: 1

Protocol	LineRate (Gbps)	DataWidth	Refclk (MHz)	Quad Count	Quad PLL
tenGBASE-R	10.3125	32	156.250	1	<input checked="" type="checkbox"/>

OK Cancel

Create IBERT Design

- Under the Protocol Selection tab, set the parameters as follows:

Customize IP

IBERT 7 Series GTX (3.0)

Documentation IP Location Switch to Defaults

Component Name: ibert_bank109

Protocol Definition **Protocol Selection** Clock Settings Summary

Please select Protocol-Quad combination

GTX Location	Protocol Selected	Refclk Selection	TXUSRCLK Source
QUAD_109	tenGBASE-R / 10.3125 Gbps	MGIREFCLK0 110	Channel 0
QUAD_110	None	None	Channel 0
QUAD_111	None	None	Channel 0
QUAD_112	None	None	Channel 0

OK Cancel

Ports:

- RXN_I[3:0]
- RXP_I[3:0] TXN_O[3:0]
- GTREFCLK0_I[0:0] TXP_O[3:0]
- GTREFCLK1_I[0:0] RXOUTCLK_0
- SYSCLK_I

Create IBERT Design

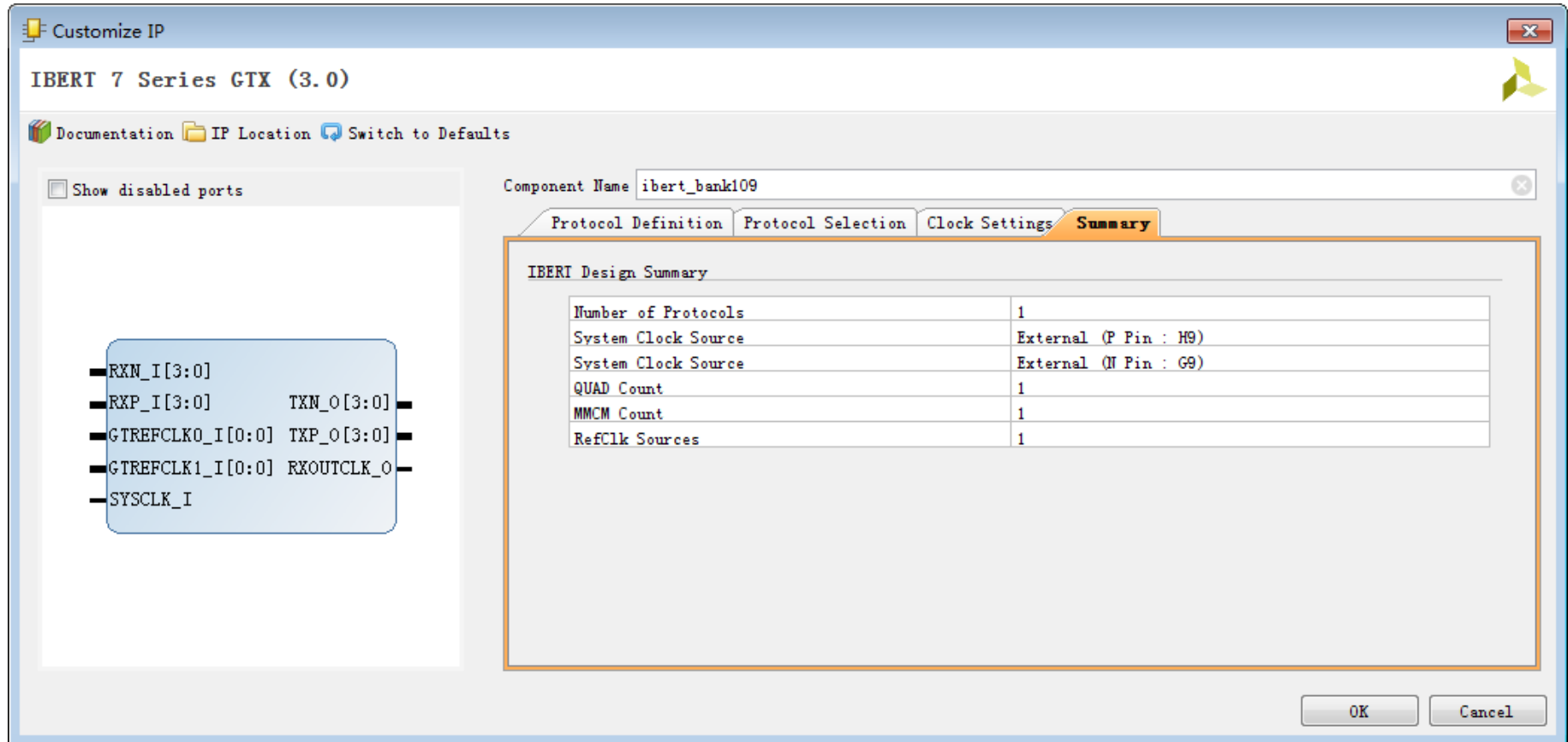
- Under the Protocol Selection tab, set the parameters as follows:

The screenshot shows the 'Customize IP' window for 'IBERT 7 Series GTX (3.0)'. The 'Clock Settings' tab is selected. On the left, a list of ports is shown: RXN_I[3:0], RXP_I[3:0], TXN_O[3:0], TXP_O[3:0], GTREFCLK0_I[0:0], GTREFCLK1_I[0:0], RXOUTCLK_O, and SYSCLK_I. The 'Component Name' is 'ibert_bank109'. The 'RXOUTCLK Probe' section has an unchecked 'Add RXOUTCLK Probes' checkbox. A table lists clock settings, with the 'System Clock' row highlighted by a red box. Below the table, the 'System Clock Termination Settings' section has an unchecked 'Enable DIFF Term' checkbox. The 'OK' and 'Cancel' buttons are at the bottom right.

Clock Type	Source	I/O Standard	P Package Pin	N Package Pin	Frequency (MHz)
System Clock	External	DIFF SSIL15	H9	G9	200.00

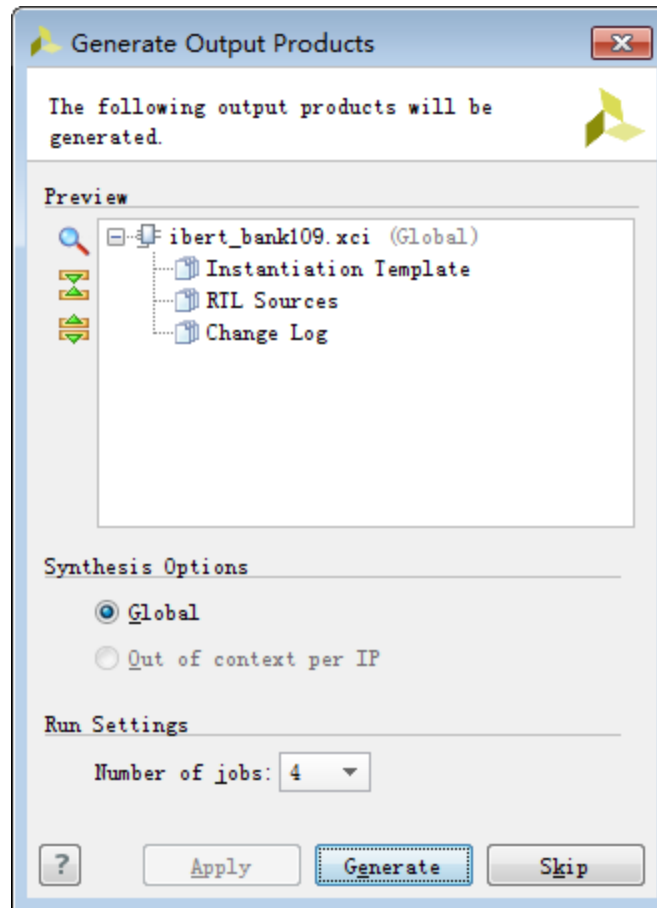
Create IBERT Design

- Review the summary and click OK



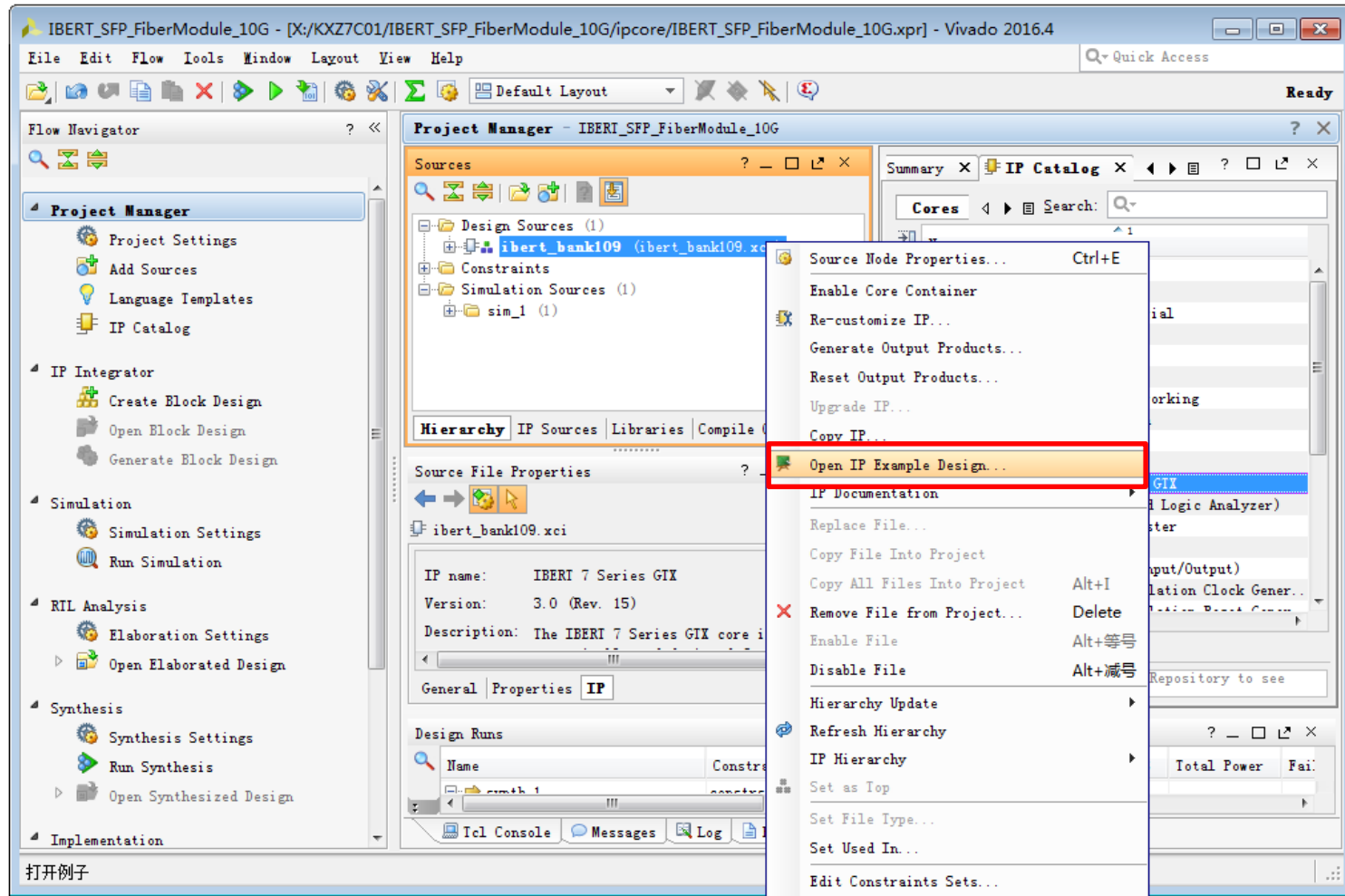
Create IBERT Design

- Click Generate



Compile Example Design

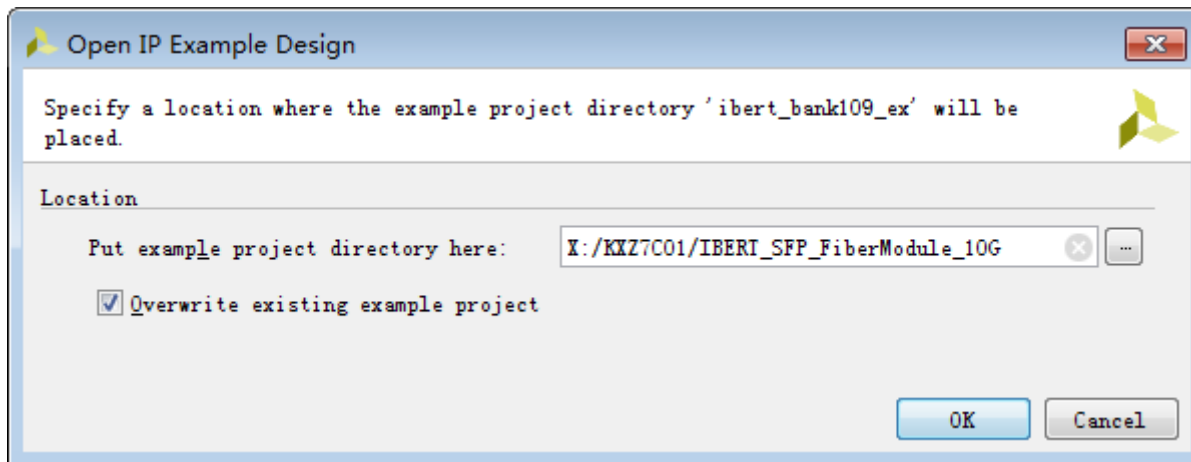
- Right click on ibert_bank109 and select Open IP Example Design...



打开例子

Compile Example Design

- Set the location and click OK



Modify the Source Code

- In order to enable the TX circuit of the SFP module, the pin “SFPx_TX_DISABLE” need to be driven LOW. Add the following code into the file “example_ibert_bank109.v”:

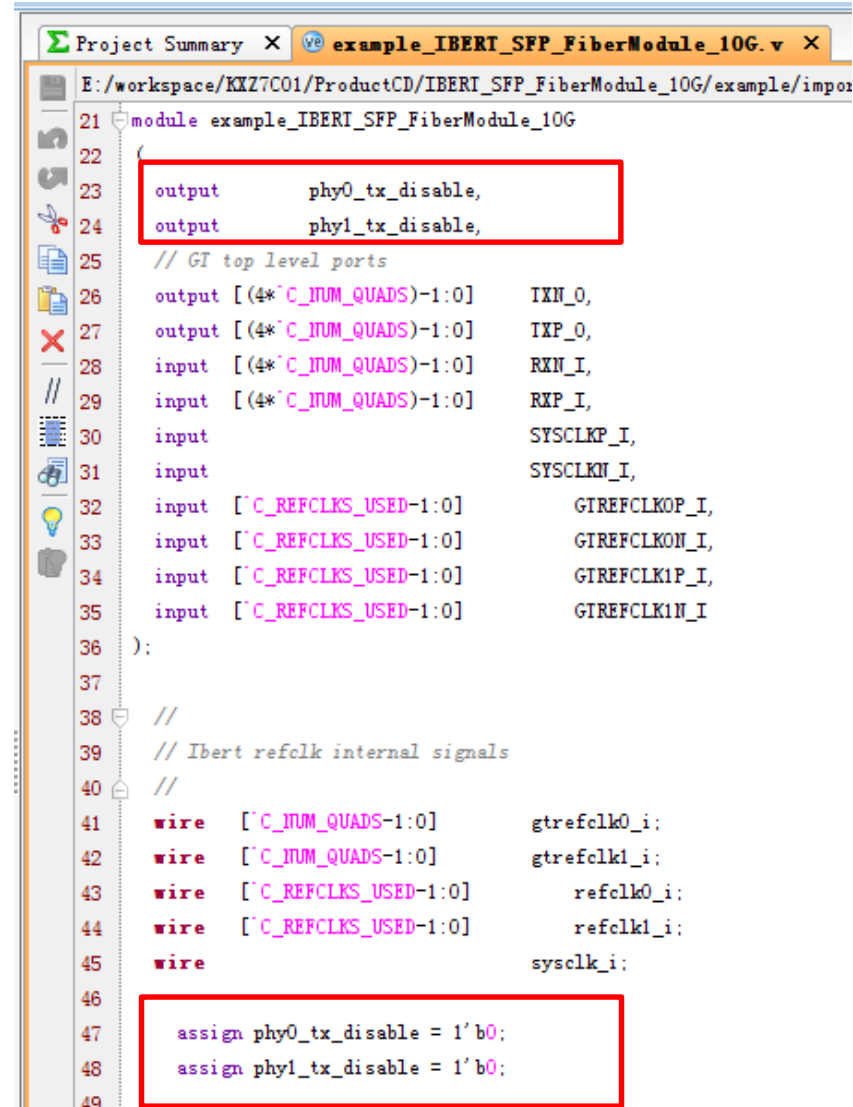
```
output phy0_tx_disable,
```

```
output phy1_tx_disable,
```

and

```
assign phy0_tx_disable = 1'b0;
```

```
assign phy1_tx_disable = 1'b0;
```



```
Project Summary X example_IBERT_SFP_FiberModule_10G.v X
E:/workspace/KXZ7C01/ProductCD/IBERT_SFP_FiberModule_10G/example/impor
21 module example_IBERT_SFP_FiberModule_10G
22 (
23     output    phy0_tx_disable,
24     output    phy1_tx_disable,
25     // GI top level ports
26     output [(4*`C_NUM_QUADS)-1:0] TXN_0,
27     output [(4*`C_NUM_QUADS)-1:0] TXP_0,
28     input  [(4*`C_NUM_QUADS)-1:0] RXN_I,
29     input  [(4*`C_NUM_QUADS)-1:0] RXP_I,
30     input                                SYSCLKP_I,
31     input                                SYSCLKN_I,
32     input [(`C_REFCLKS_USED)-1:0] GIREFCLKOP_I,
33     input [(`C_REFCLKS_USED)-1:0] GIREFCLKON_I,
34     input [(`C_REFCLKS_USED)-1:0] GIREFCLKIP_I,
35     input [(`C_REFCLKS_USED)-1:0] GIREFCLKIN_I
36 );
37
38 //
39 // Ibert refclk internal signals
40 //
41 wire [(`C_NUM_QUADS)-1:0] gtreclk0_i;
42 wire [(`C_NUM_QUADS)-1:0] gtreclk1_i;
43 wire [(`C_REFCLKS_USED)-1:0] refclk0_i;
44 wire [(`C_REFCLKS_USED)-1:0] refclk1_i;
45 wire                                sysclk_i;
46
47 assign phy0_tx_disable = 1'b0;
48 assign phy1_tx_disable = 1'b0;
49
```

Modify the Source Code

- Add the constraints of phy0_tx_disable and phy1_tx_disable into the “example_ibert_bank109.xdc” file:

```
set_property PACKAGE_PIN C7 [get_ports phy0_tx_disable]
```

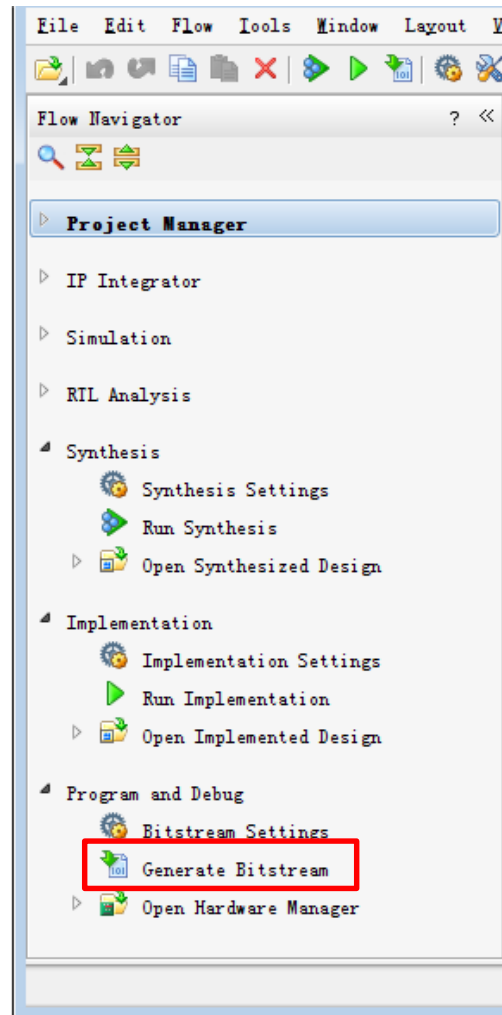
```
set_property IOSTANDARD LVCMOS15 [get_ports phy0_tx_disable]
```

```
set_property PACKAGE_PIN A9 [get_ports phy1_tx_disable]
```

```
set_property IOSTANDARD LVCMOS15 [get_ports phy1_tx_disable]
```

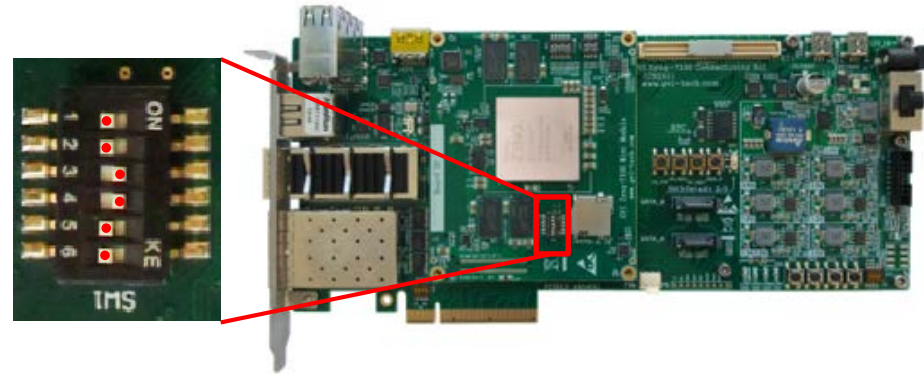
Compile Example Design

- Click Generate Bitstream.

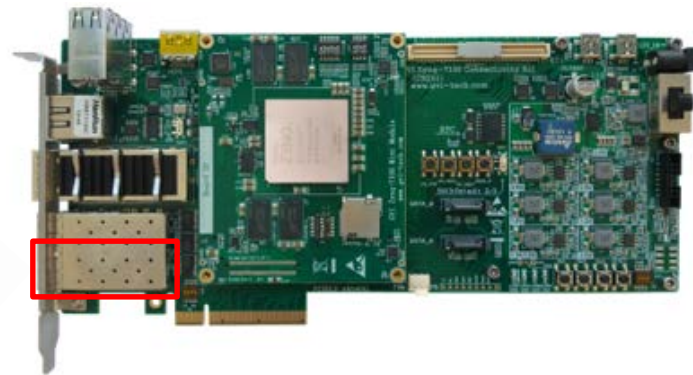


System Setup

- Set SW1 to OFF-OFF-ON-ON-OFF-OFF. This sets the frequency to 156.25MHz.



- Connect a loopback fiber into the 10G SFP+ module, and then plug the 10G SFP+ module into SFP+ 1 (in this demo, SFP+ 1 is used. It does not make difference to use SFP+ 0).



System Setup

- Connect the JTAG cable to the base board.



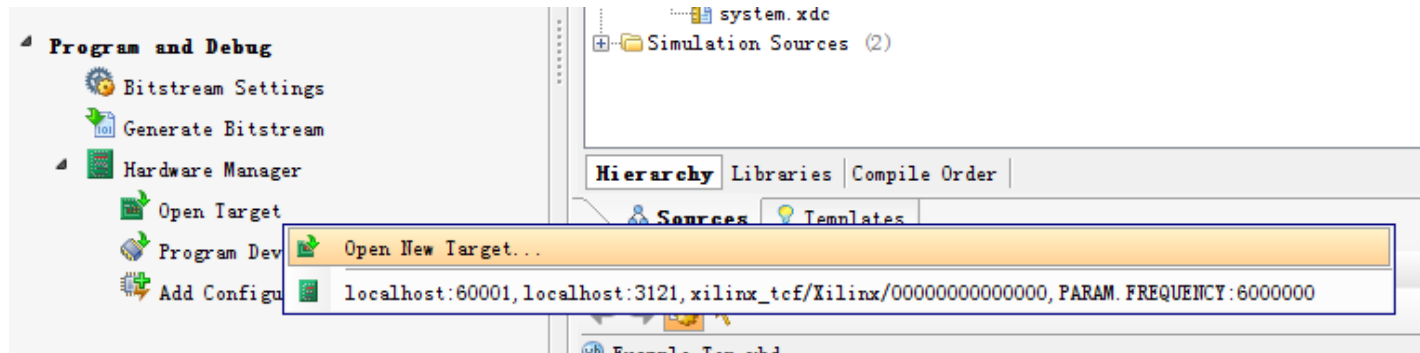
- Connect the power supplier.



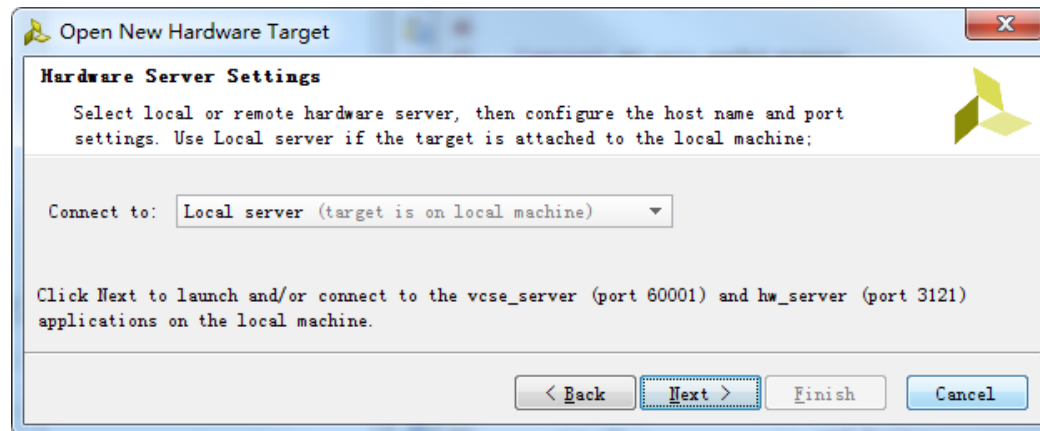
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Configure FPGA

- Click “Open Target”, and then click “Open New Target...”

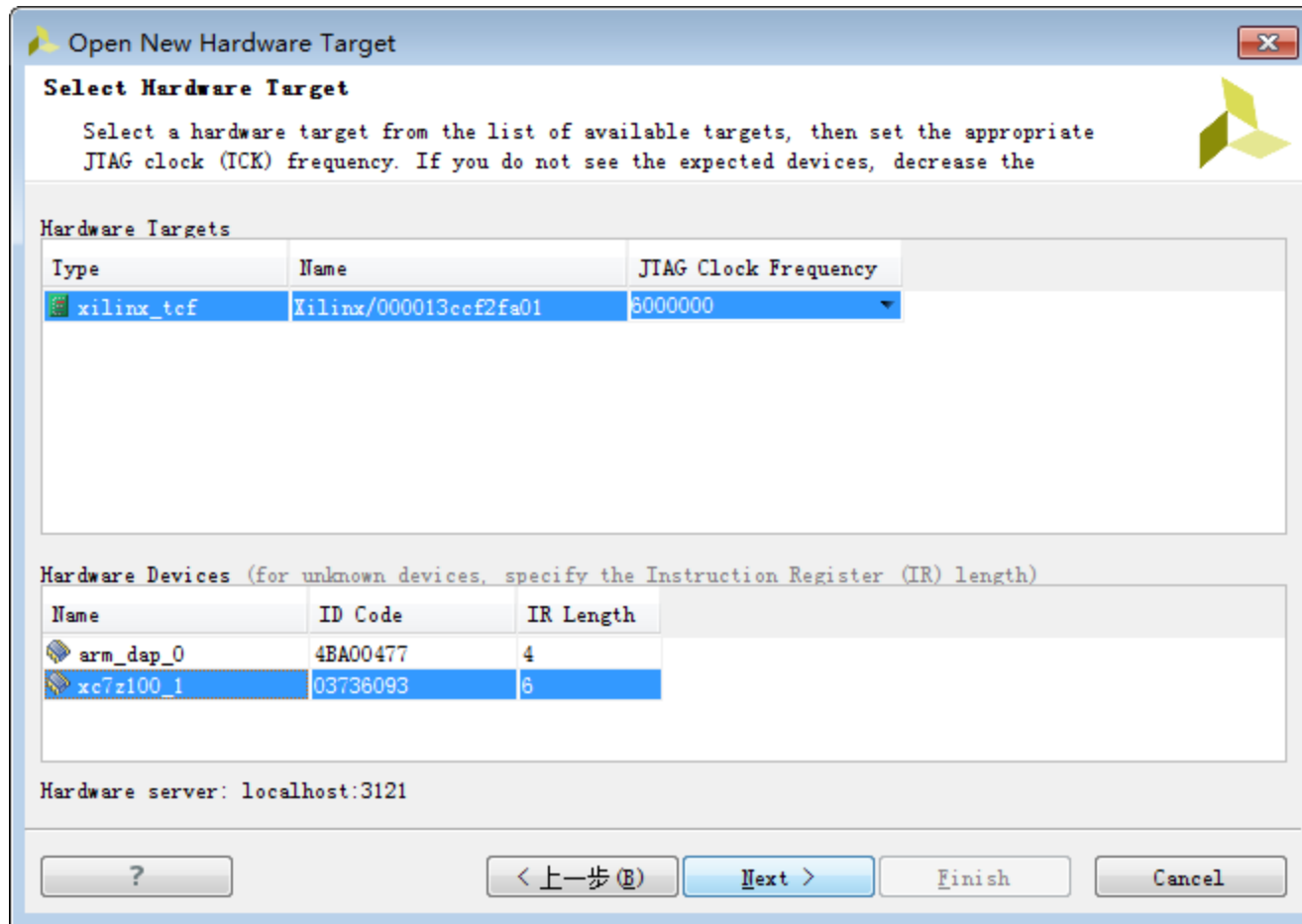


- In this dialog, choose “Local server”, and then click “Next”.



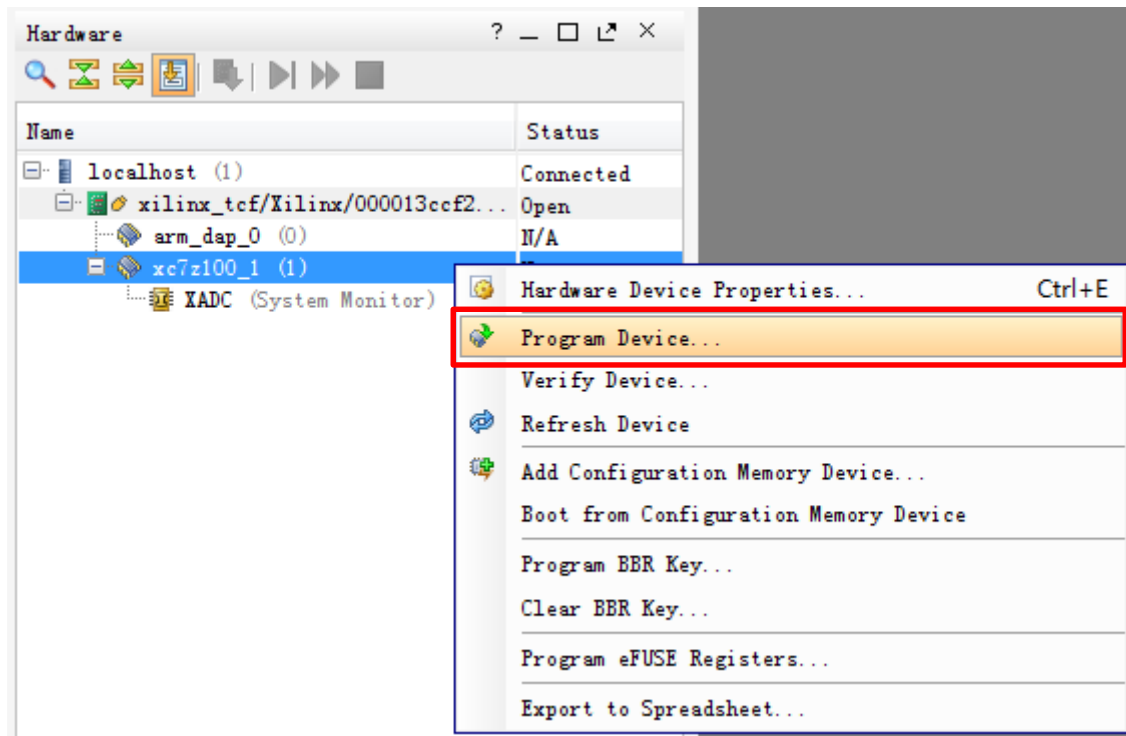
Configure FPGA

- Choose the target FPGA, and then click “Next”.



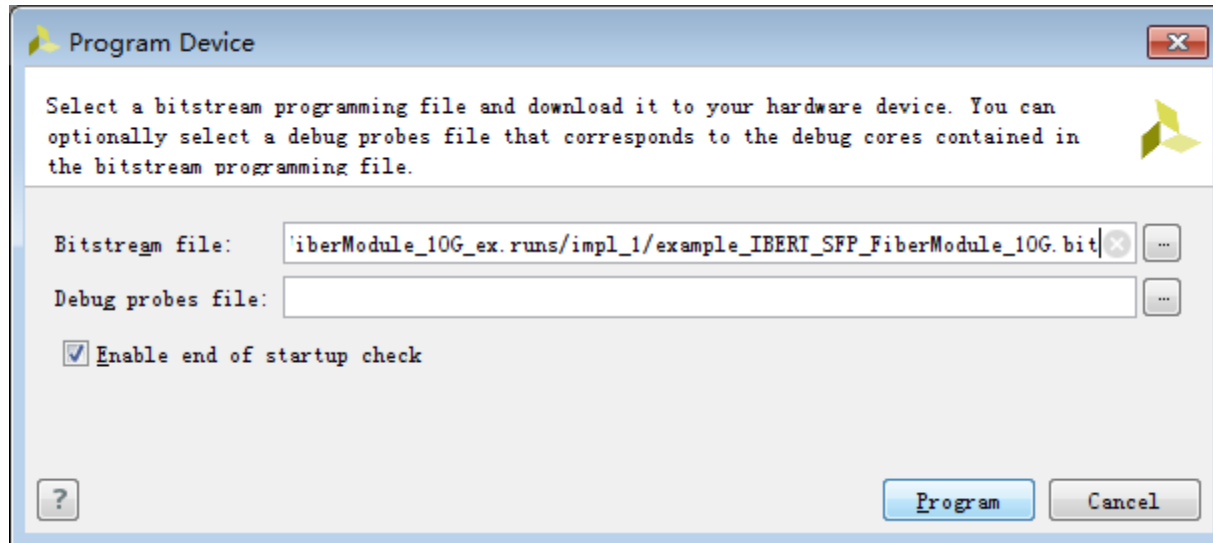
Configure FPGA

- Go to the “Hardware Manager” window.
- Right click on the FPGA, and then click “Program Device...”



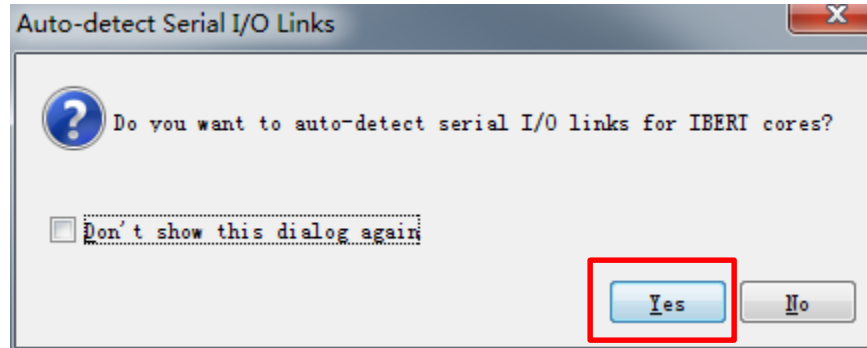
Configure FPGA

- In this dialog, choose the right bit file, and continue with “Program”.

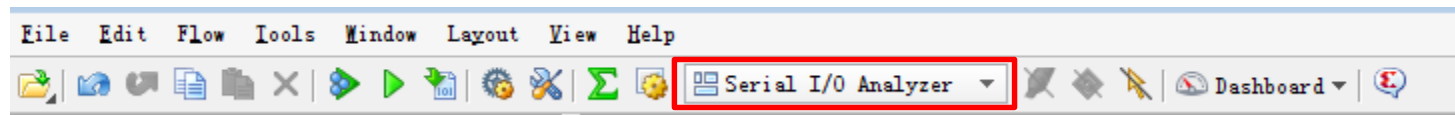


Configure FPGA

- At this step, click “Yes”.

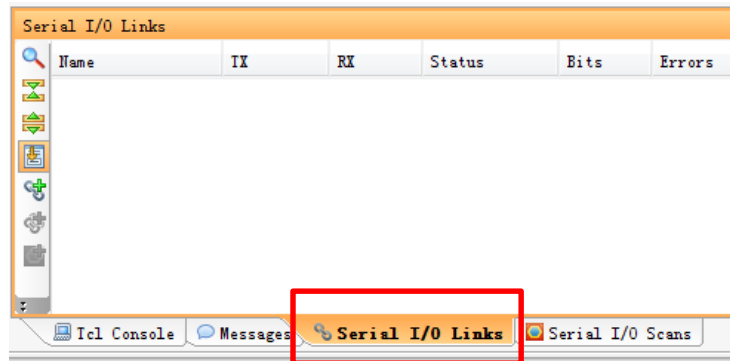


- If needed, set Vivado GUI layout to Serial I/O Analyzer



Configure “Serial I/O Analyzer” Window

- In the “Serial I/O Analyzer” window, select “Serial I/O Links” Tab.



Configure Serial Links

- Reset the BERT, and then check the detected errors. In normal case, no error should be detected.

Serial I/O Links													
Name	TX	RX	Status	Errors	Bits	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled
Ungrouped Links (0)													
Found Links (2)							Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)	<input checked="" type="checkbox"/>
Found 0	MGI_X0Y2/IX	MGI_X0Y2/RX	10.312 Gbps	OEO	9.50...	1.052...	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)	<input checked="" type="checkbox"/>
Found 1	MGI_X0Y3/IX	MGI_X0Y3/RX	10.312 Gbps	OEO	9.52...	1.049...	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)	<input checked="" type="checkbox"/>

Reference

- More design resources can be found :

www.gvi-tech.com

- How to Buy:

- <https://detail.tmall.com/item.htm?id=562769965498>

