



GVI KXZ7C01 Zynq Connectivity Kit

GTX IBERT Design Creation: QSFP+ 40G Fiber Loop Back QuickStart

December 2017

Order Hardware:

<https://detail.tmall.com/item.htm?id=562769965498>

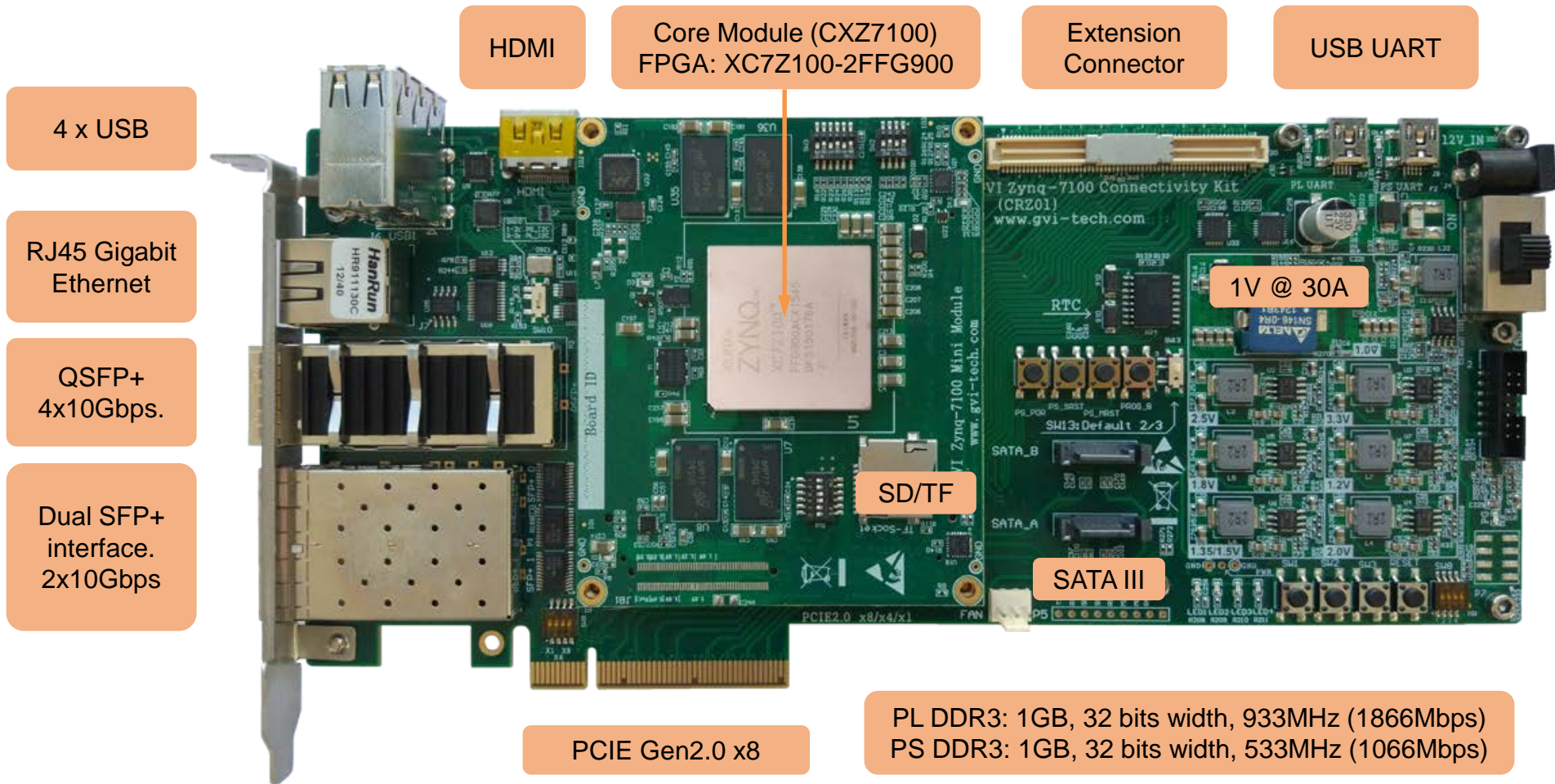
<http://www.gvi-tech.com/products-fpga-kits>

杭州言曼科技有限公司

Overview

- GVI KXZ7C01 Zynq Connectivity Kit Overview
- Software Requirements
- Create IBERT Design
- Hardware Setup
- Run IBERT with 40G QSFP+ Fiber Module
- References

GVI Zynq Connectivity Kit – KXZ7C01



Xilinx Software Requirement

- Xilinx Vivado Design Suite (version 2016.4 is used for development)



IBERT Overview

- Description

The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the GTX transceivers. A graphical user interface is provided through the Vivado Hardware Manager.

- Reference Design IP

LogiCORE IBERT Example Designs

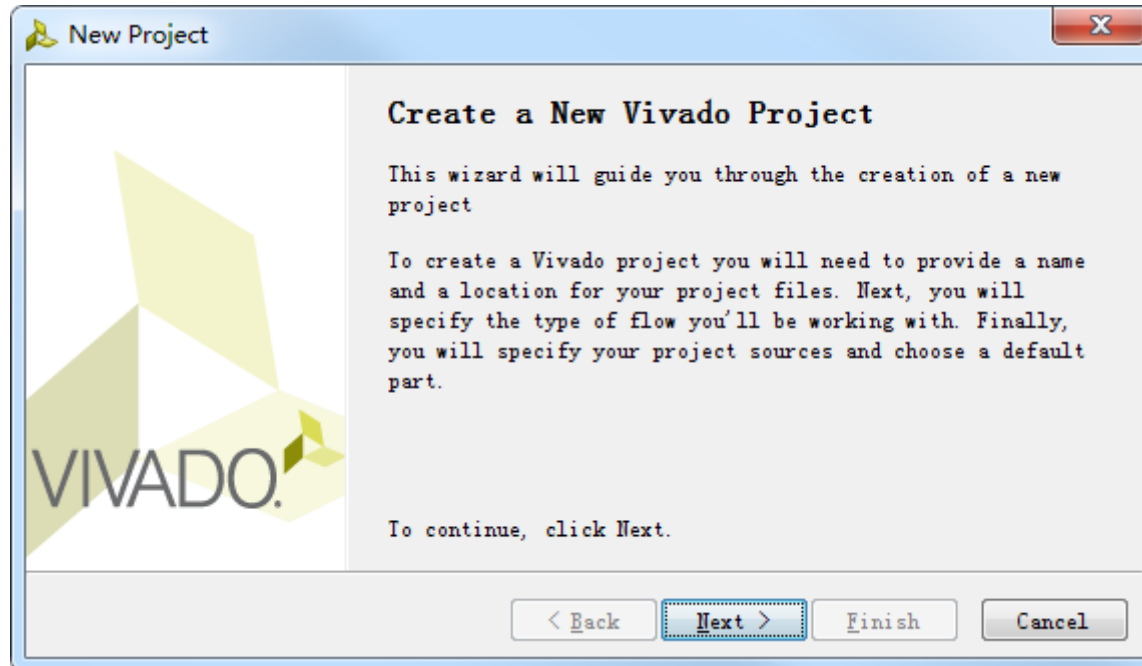
Create IBERT Design

- Open Vivado
 - Start → All Programs → Xilinx Design Tools → Vivado 2016.4 → Vivado
- Select Create New Project



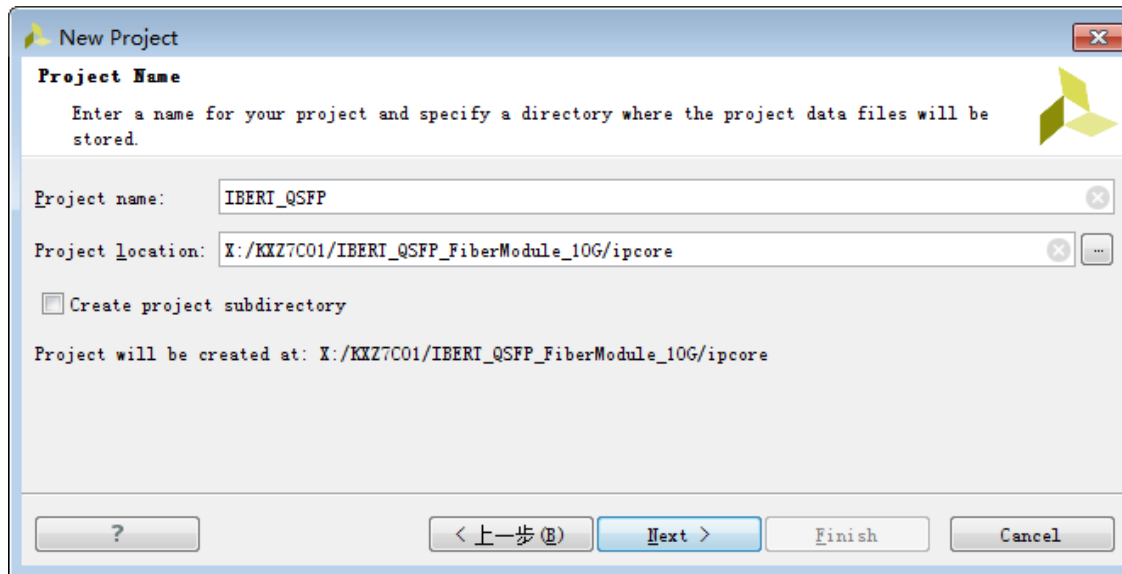
Create IBERT Design

- Click Next



Create IBERT Design

- Set the Project name and location.



New Project

Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

Project name:

Project location:

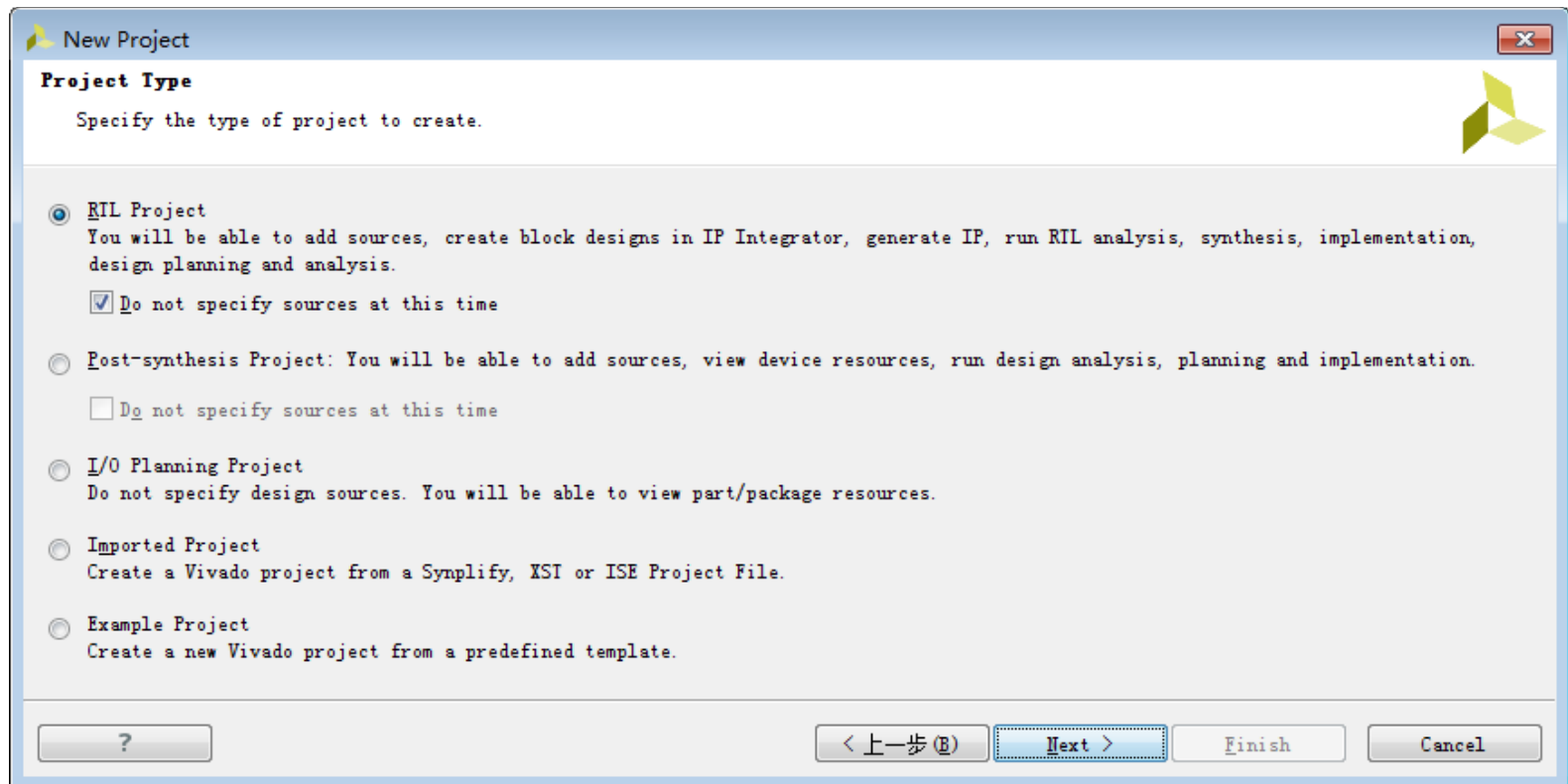
☐ Create project subdirectory

Project will be created at: X:/KXZ7C01/IBERI_QSFP_FiberModule_10G/ipcore

? < 上一步(B) Next > Finish Cancel

Create IBERT Design

- Select RTL Project
 - Select Do not specify sources at this time



Create IBERT Design

- Select the FPGA part number: xc7z100ffg900-2

The image shows the 'New Project' dialog box in Xilinx IDE. The 'Default Part' section is active, showing a search for 'xc7z100ffg900-2'. The search results table lists the selected part with its specifications. The 'xc7z100ffg900-2' part is highlighted with a red box.

New Project

Choose a default Xilinx part or board for your project. This can be changed later.

Select: ☒ Parts ☐ Boards

Filter

Product category: All Speed grade: All

Family: All Temp grade: All

Package: All

Reset All Filters

Search: (1 match)

Part	I/O Pin Count	Block RAMs	DSPs	FlipFlops	GPIO2 Transceivers	Gb Transceivers	Available IOBs
xc7z100ffg900-2	900	755	2020	554800	0	16	362

Navigation buttons: ? < 上一步 (B) Next > Finish Cancel

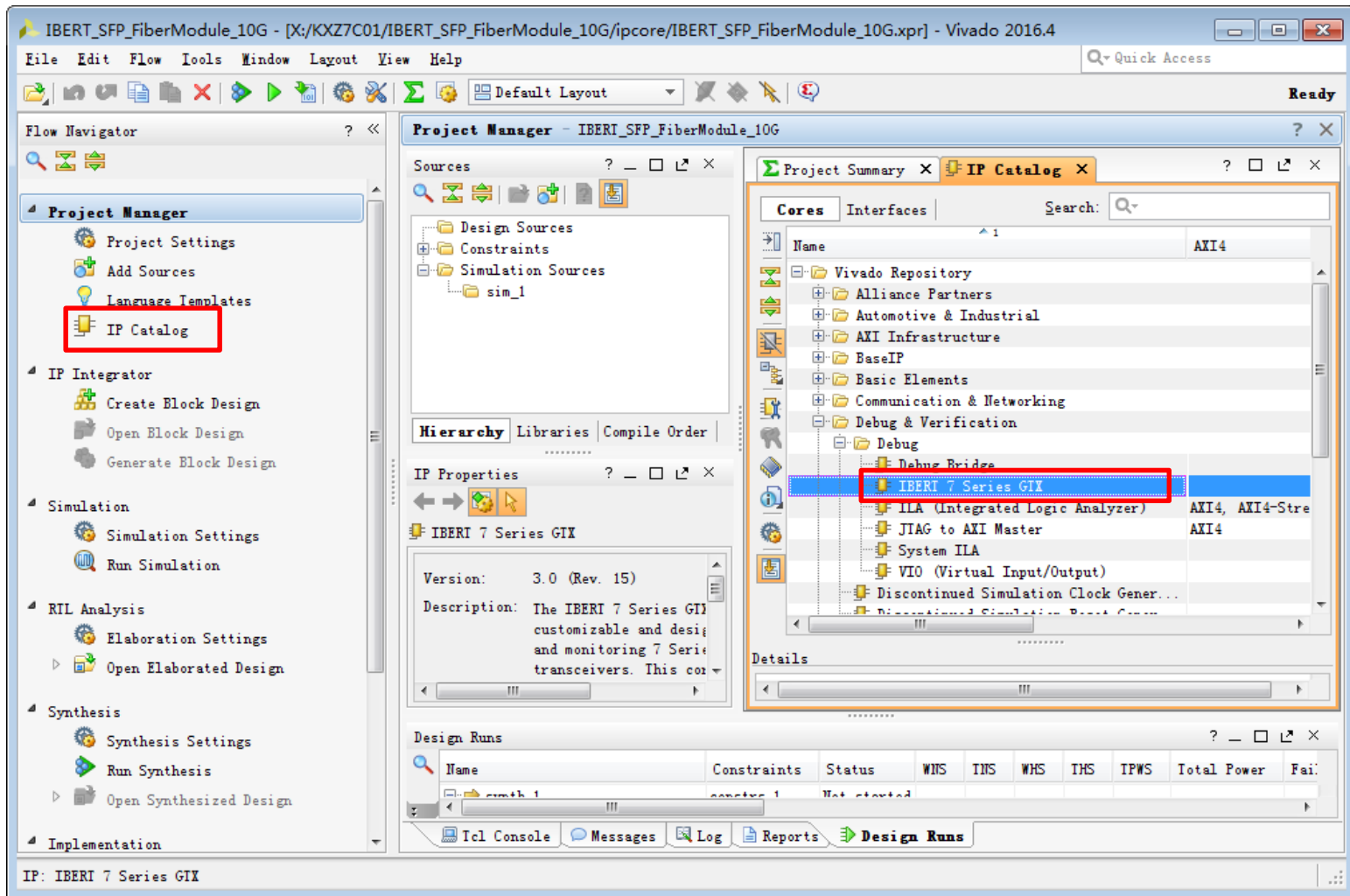
Create IBERT Design

- Click Finish



Create IBERT Design

- Click on IP Catalog, double click IBERT 7 Series GTX under Debug & Verification



Create IBERT Design

- Set the Component name: ibert_bank110
- Under the Protocol Definition tab, set the parameters as follows:

Customize IP

IBERT 7 Series GTX (3.0)

Documentation IP Location Switch to Defaults

☐ Show disabled Component Name: ibert_bank110

Protocol Definition Protocol Selection Clock Settings Summary

Silicon Version

Silicon Version: General ES/Production

The maximum number of quads available for this device is 4

Number of Protocols: 1

Protocol	LineRate (Gbps)	DataWidth	Refclk (MHz)	Quad Count	Quad PLL
tenGBASE-R	10.3125	32	156.250	1	<input checked="" type="checkbox"/>

OK Cancel

Create IBERT Design

- Under the Protocol Selection tab, set the parameters as follows:

Customize IP

IBERT 7 Series GTX (3.0)

Documentation IP Location Switch to Defaults

☐ Show disabled Component Name

Protocol Definition **Protocol Selection** Clock Settings Summary

Please select Protocol-Quad combination

GTX Location	Protocol Selected	Refclk Selection	TXUSRCLK Source
QUAD 109	None	None	Channel 0
QUAD_110	tenGBASE-R / 10.3125 Gbps	MGIREFCLK0 110	Channel 0
QUAD_111	None	None	Channel 0
QUAD_112	None	None	Channel 0

OK Cancel

Create IBERT Design

- Under the Protocol Selection tab, set the parameters as follows:

Customize IP

IBERT 7 Series GTX (3.0)

Documentation IP Location Switch to Defaults

☐ Show disabled Component Name

Protocol Definition Protocol Selection **Clock Settings** Summary

RXOUTCLK Probe

☐ Add RXOUTCLK Probes

Clock Type	Source	I/O Standard	P Package Pin	N Package Pin	Frequency (MHz)
System Clock	External	DIFF SSTL15	H9	G9	200.00

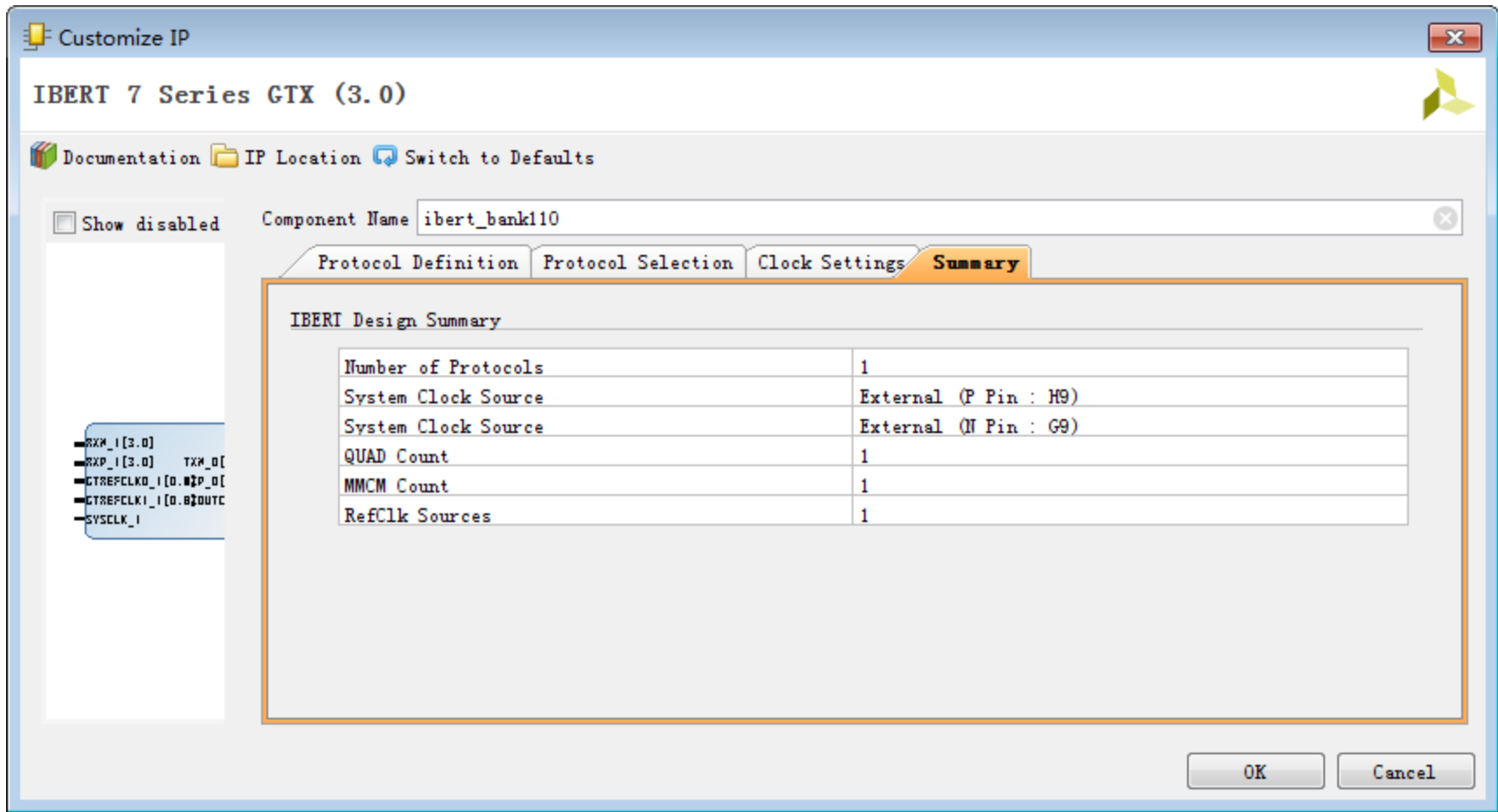
System Clock Termination Settings

☐ Enable DIFF Term

OK Cancel

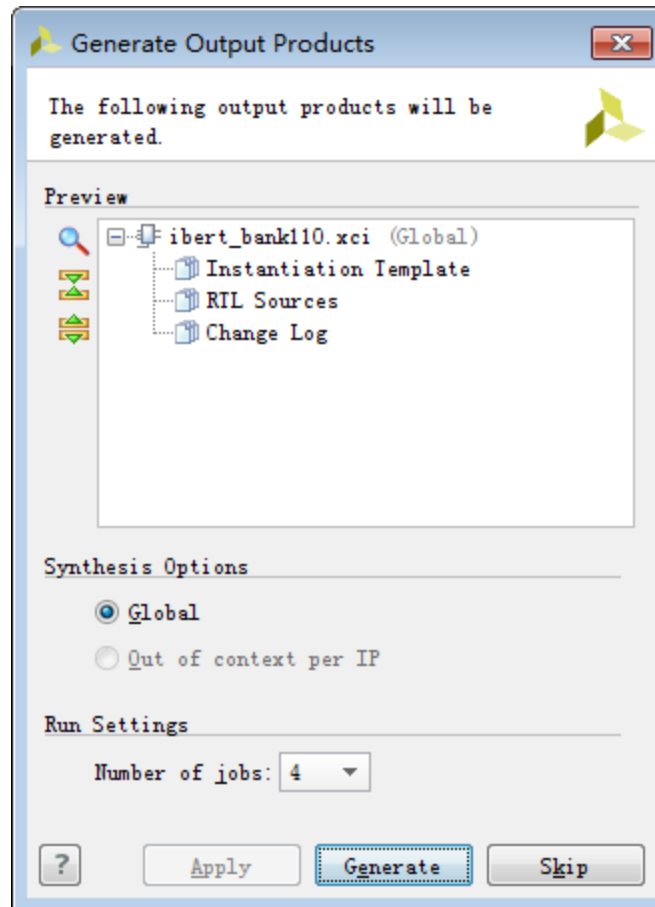
Create IBERT Design

- Review the summary and click OK



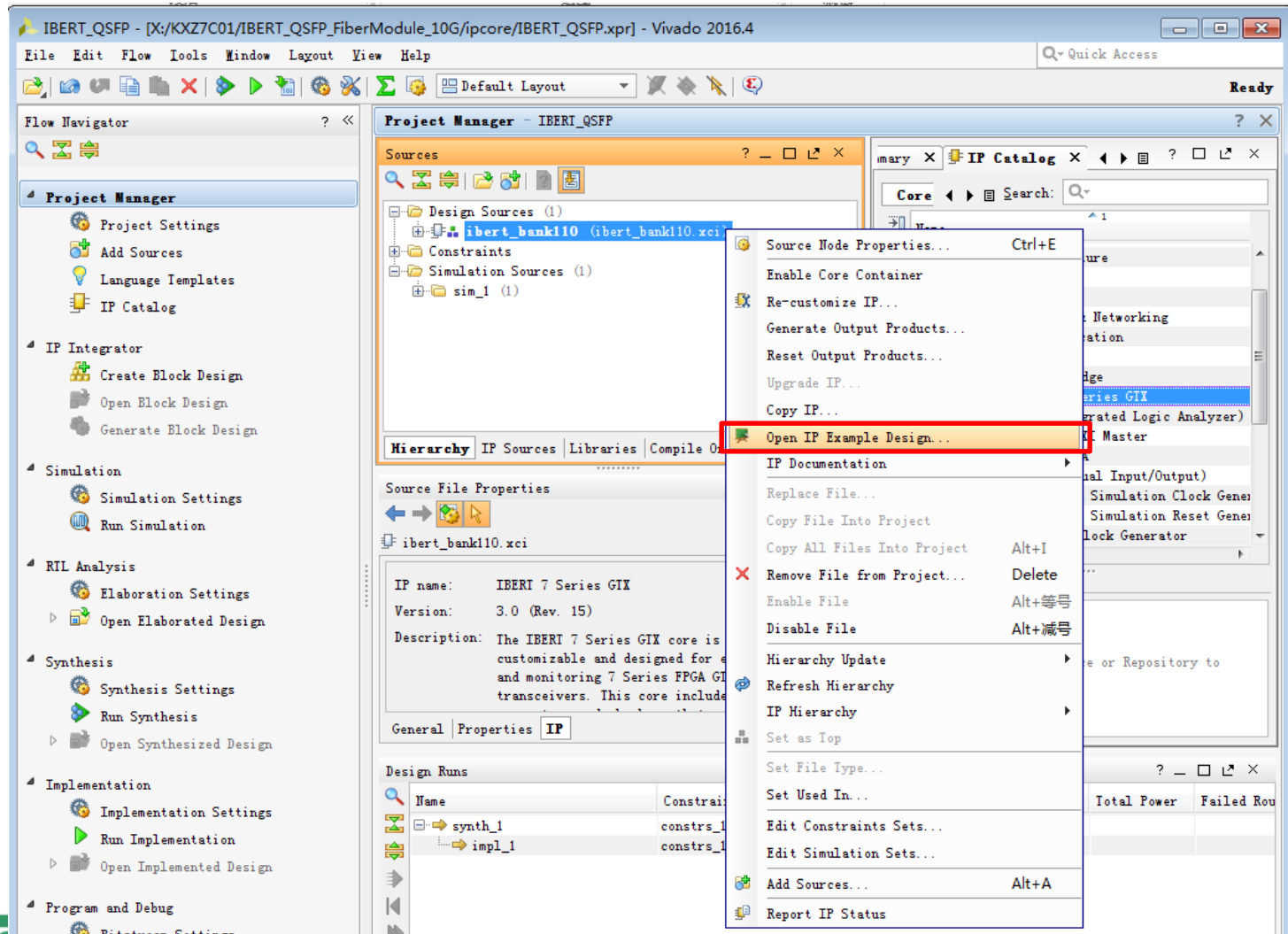
Create IBERT Design

- Click Generate



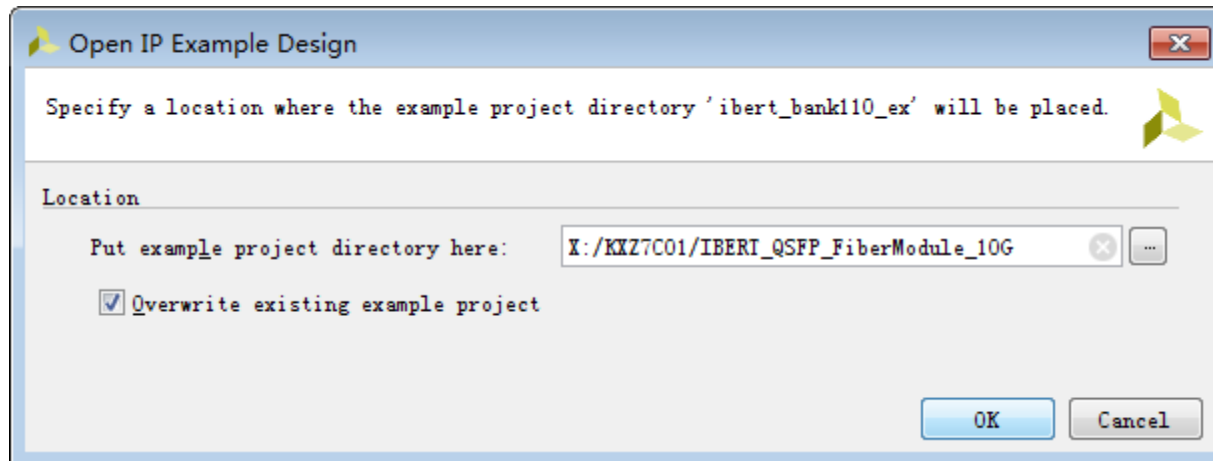
Compile Example Design

- Right click on ibert_bank110 and select Open IP Example Design...



Compile Example Design

- Set the location and click OK



Modify the Source Code

- In order to enable the TX circuit of the QSFP+ module, the following code need to be modified in the file “example_ibert_bank110.v”:

output phy_reset_n,

output ModSelL,

output LPMode,

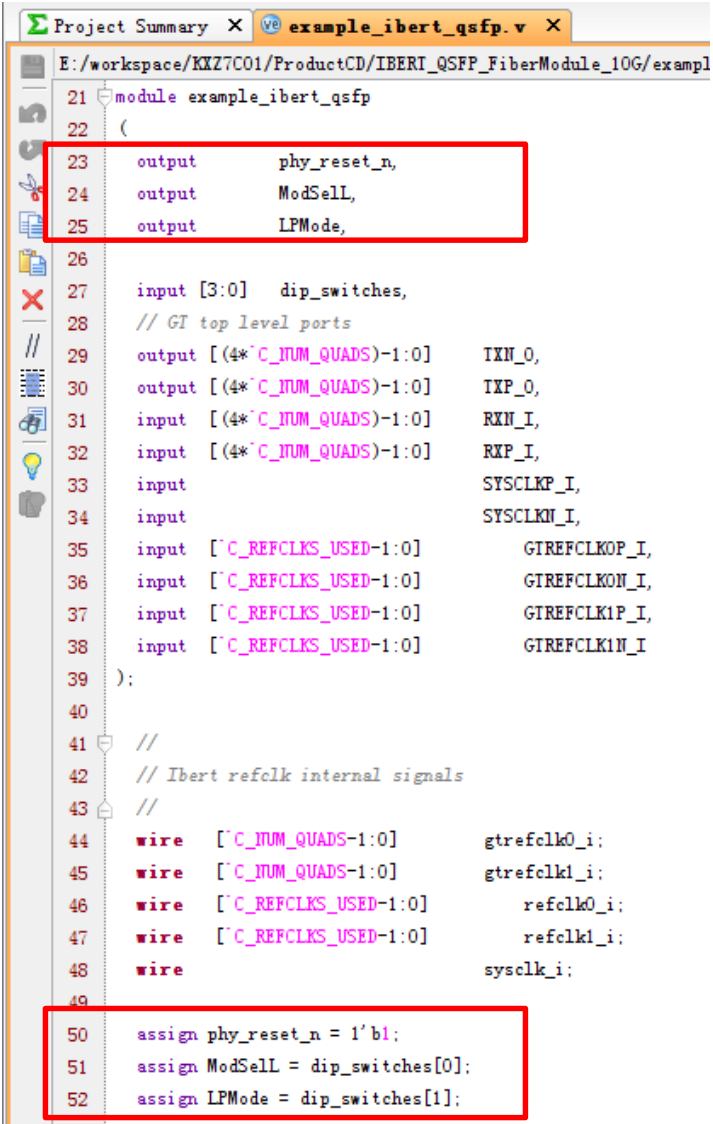
and

assign phy_reset_n = 1'b1;

assign ModSelL = dip_switches[0];

assign LPMode = dip_switches[1];

- 不需要关注拨码开关 SW8 1和2的开关位置，预留功能



```
21 module example_ibert_qsfp
22 (
23     output    phy_reset_n,
24     output    ModSelL,
25     output    LPMode,
26
27     input [3:0]  dip_switches,
28     // GI top level ports
29     output [(4*C_JTUM_QUADS)-1:0]  TXN_0,
30     output [(4*C_JTUM_QUADS)-1:0]  TXP_0,
31     input  [(4*C_JTUM_QUADS)-1:0]  RXN_I,
32     input  [(4*C_JTUM_QUADS)-1:0]  RXP_I,
33     input                                SYSCLKP_I,
34     input                                SYSCLKN_I,
35     input [(C_REFCLKS_USED)-1:0]    GIREFCLKOP_I,
36     input [(C_REFCLKS_USED)-1:0]    GIREFCLKON_I,
37     input [(C_REFCLKS_USED)-1:0]    GIREFCLKIP_I,
38     input [(C_REFCLKS_USED)-1:0]    GIREFCLKIN_I,
39 );
40
41 //
42 // Ibert refclk internal signals
43 //
44 wire [(C_JTUM_QUADS)-1:0]    gtrefclk0_i;
45 wire [(C_JTUM_QUADS)-1:0]    gtrefclk1_i;
46 wire [(C_REFCLKS_USED)-1:0]    refclk0_i;
47 wire [(C_REFCLKS_USED)-1:0]    refclk1_i;
48 wire                                sysclk_i;
49
50 assign phy_reset_n = 1'b1;
51 assign ModSelL = dip_switches[0];
52 assign LPMode = dip_switches[1];
```

Modify the Source Code

- Add the constraints of phy0_tx_disable and phy1_tx_disable into the “example_ibert_bank109.xdc” file:

```
set_property PACKAGE_PIN E12 [get_ports phy_reset_n]
```

```
set_property IOSTANDARD LVCMOS18 [get_ports phy_reset_n]
```

```
set_property PACKAGE_PIN G17 [get_ports ModSelL]
```

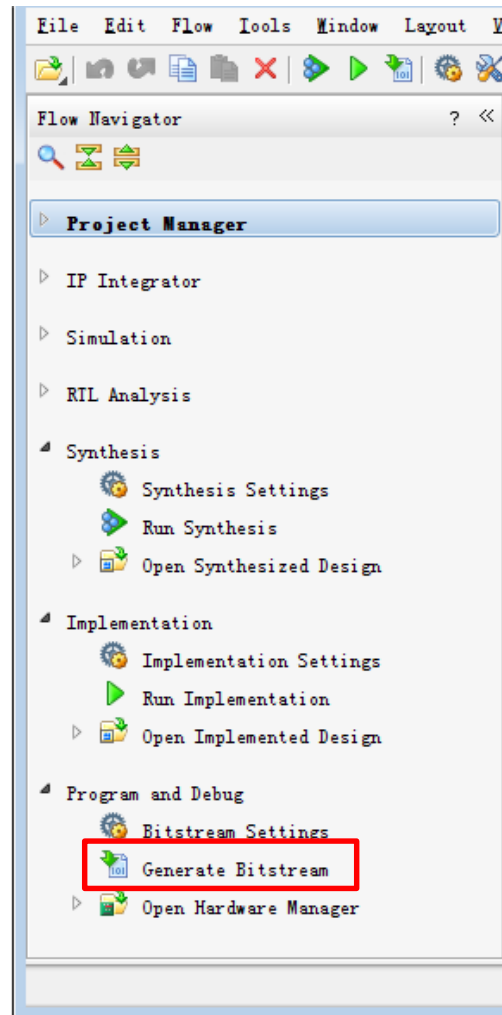
```
set_property IOSTANDARD LVCMOS18 [get_ports ModSelL]
```

```
set_property PACKAGE_PIN G16 [get_ports LPMode]
```

```
set_property IOSTANDARD LVCMOS18 [get_ports LPMode]
```

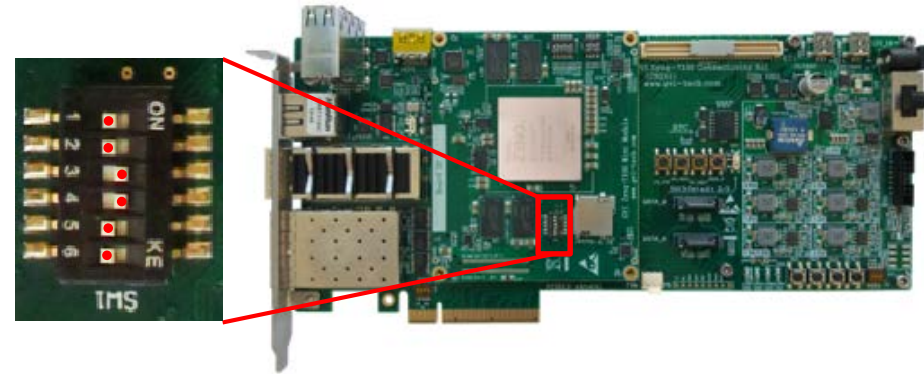
Compile Example Design

- Click Generate Bitstream.

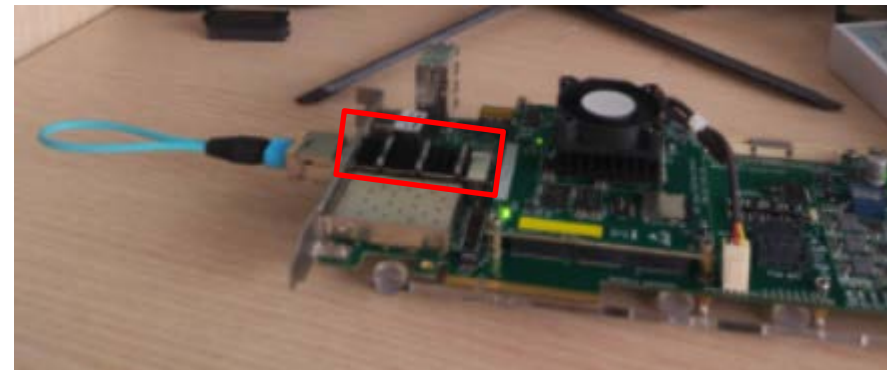


System Setup

- Set SW1 to OFF-OFF-ON-ON-OFF-OFF. This sets the frequency to 156.25MHz.



- Connect a loopback fiber into the 40G QSFP+ module, and then plug the 40G QSFP+ module into the QSFP+ connector.



System Setup

- Connect the JTAG cable to the base board.



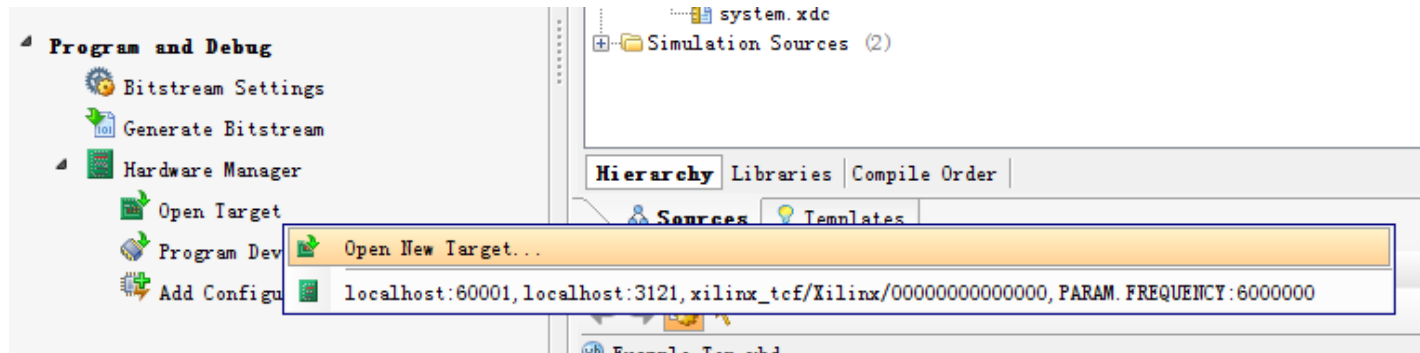
- Connect the power supplier.



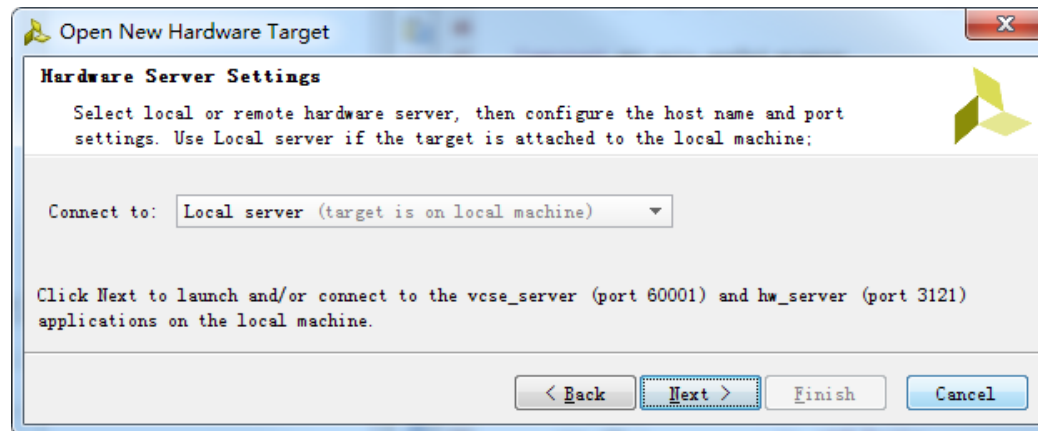
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Configure FPGA

- Click “Open Target”, and then click “Open New Target...”

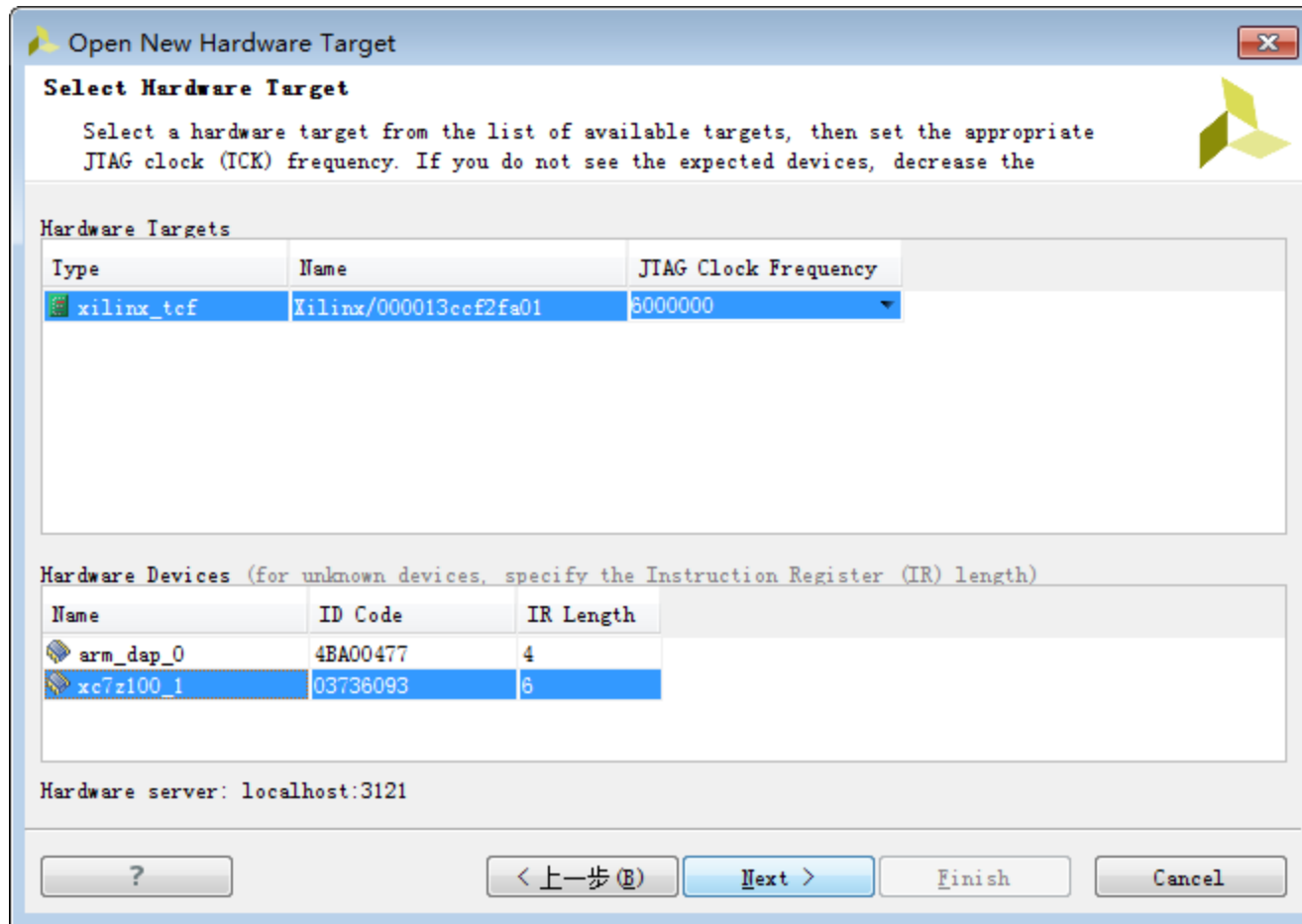


- In this dialog, choose “Local server”, and then click “Next”.



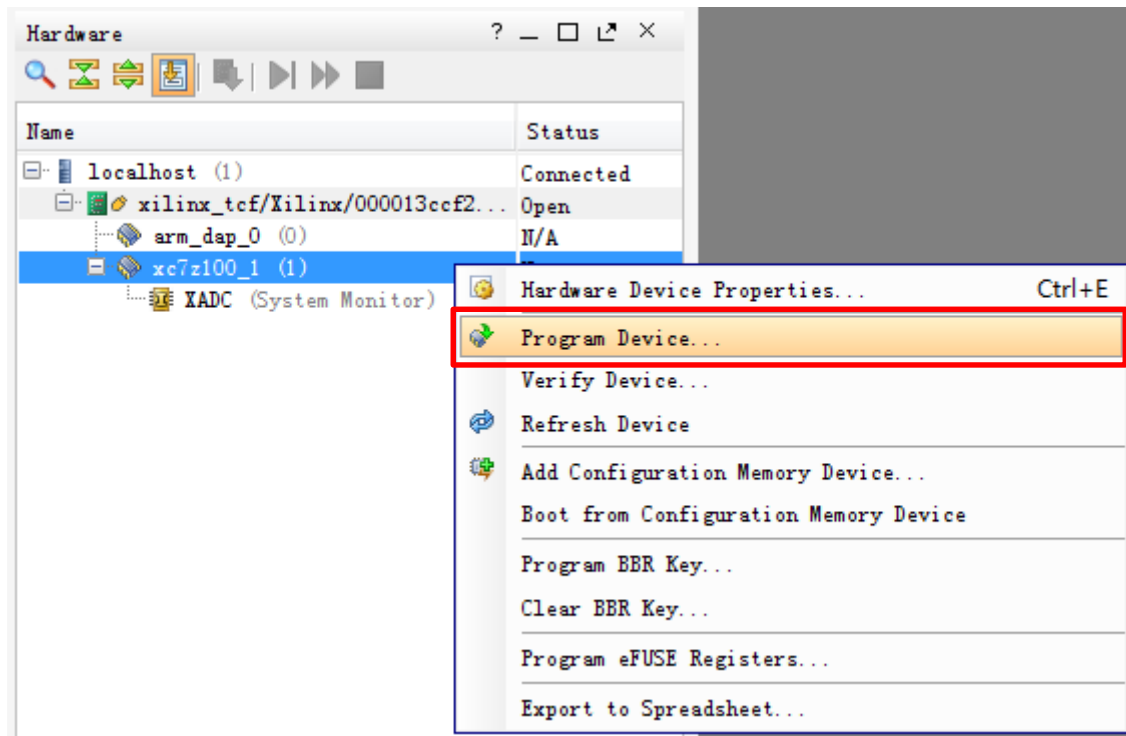
Configure FPGA

- Choose the target FPGA, and then click “Next”.



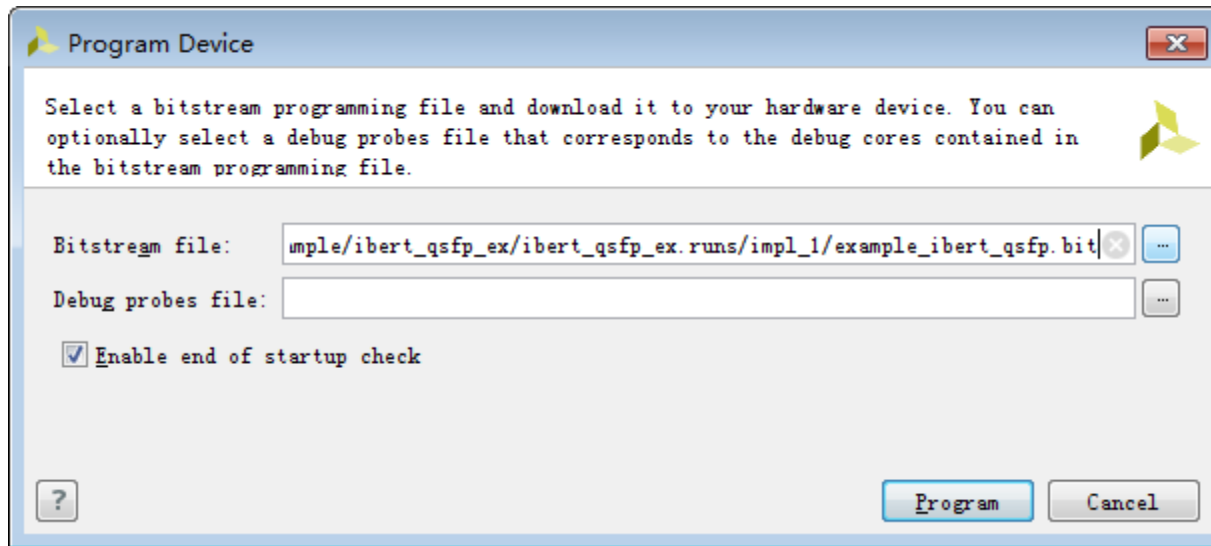
Configure FPGA

- Go to the “Hardware Manager” window.
- Right click on the FPGA, and then click “Program Device...”



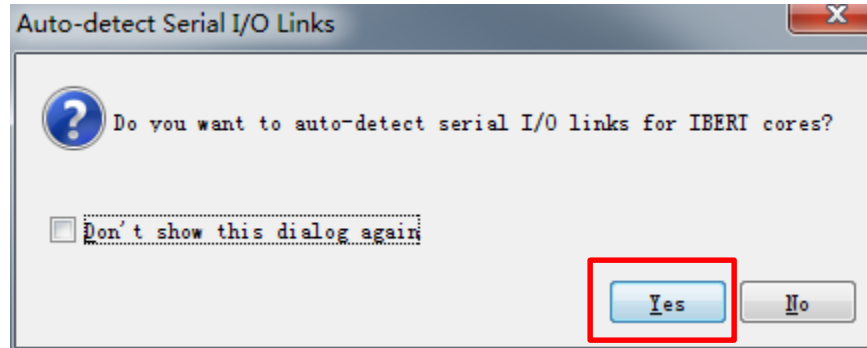
Configure FPGA

- In this dialog, choose the right bit file, and continue with “Program”.

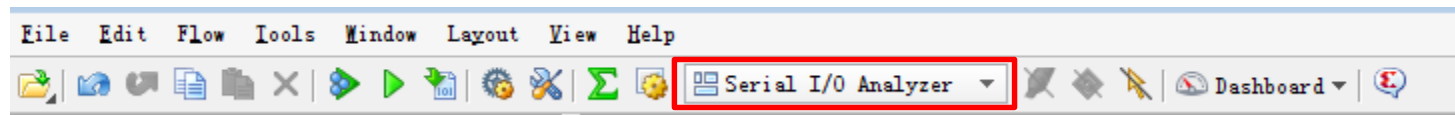


Configure FPGA

- At this step, click “Yes”.

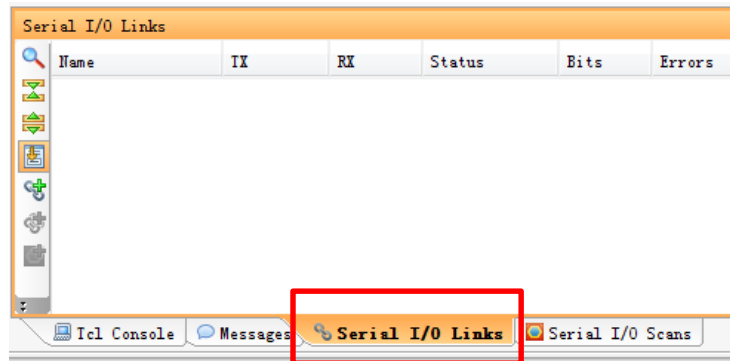


- If needed, set Vivado GUI layout to Serial I/O Analyzer



Configure “Serial I/O Analyzer” Window

- In the “Serial I/O Analyzer” window, select “Serial I/O Links” Tab.



Check Bit Error Rate of the Links

- Reset the BERT, and then check the detected errors. In normal case, no error should be detected.

	TX	RX	Status	Errors	Bits	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing
Ungrouped Links (0)												
Found Links (4)							Reset	PRBS 7-bit ▼	PRBS 7-bit ▼	1.67 dB (00111) ▼	0.68 dB (00011) ▼	1018 mV (1100) ▼
Found 0	MGT_X0Y4/TX	MGT_X0Y4/RX	10.313 Gbps	OE0	7.737E11	1.292E-12	Reset	PRBS 7-bit ▼	PRBS 7-bit ▼	1.67 dB (00111) ▼	0.68 dB (00011) ▼	1018 mV (1100) ▼
Found 1	MGT_X0Y5/TX	MGT_X0Y5/RX	10.313 Gbps	OE0	7.738E11	1.292E-12	Reset	PRBS 7-bit ▼	PRBS 7-bit ▼	1.67 dB (00111) ▼	0.68 dB (00011) ▼	1018 mV (1100) ▼
Found 2	MGT_X0Y6/TX	MGT_X0Y6/RX	10.313 Gbps	OE0	7.738E11	1.292E-12	Reset	PRBS 7-bit ▼	PRBS 7-bit ▼	1.67 dB (00111) ▼	0.68 dB (00011) ▼	1018 mV (1100) ▼
Found 3	MGT_X0Y7/TX	MGT_X0Y7/RX	10.313 Gbps	OE0	7.738E11	1.292E-12	Reset	PRBS 7-bit ▼	PRBS 7-bit ▼	1.67 dB (00111) ▼	0.68 dB (00011) ▼	1018 mV (1100) ▼

Reference

- More design resources can be found :

www.gvi-tech.com

- How to Buy:

- <https://detail.tmall.com/item.htm?id=562769965498>

