GVI KXZ7C01 Zynq Connectivity Kit

GTX IBERT Design Creation: QSFP+ 40G Fiber Loop Back

QuickStart

December 2017

Order Hardware:

https://detail.tmall.com/item.htm?id=562769965498

http://www.gvi-tech.com/products-fpga-kits

杭州言曼科技有限公司

Overview

- GVI KXZ7C01 Zynq Connectivity Kit Overview
- Software Requirements
- Create IBERT Design
- Hardware Setup
- Run IBERT with 40G QSFP+ Fiber Module
- References

GVI Zynq Connectivity Kit – KXZ7C01

HDMI

Core Module (CXZ7100)
FPGA: XC7Z100-2FFG900

Extension Connector

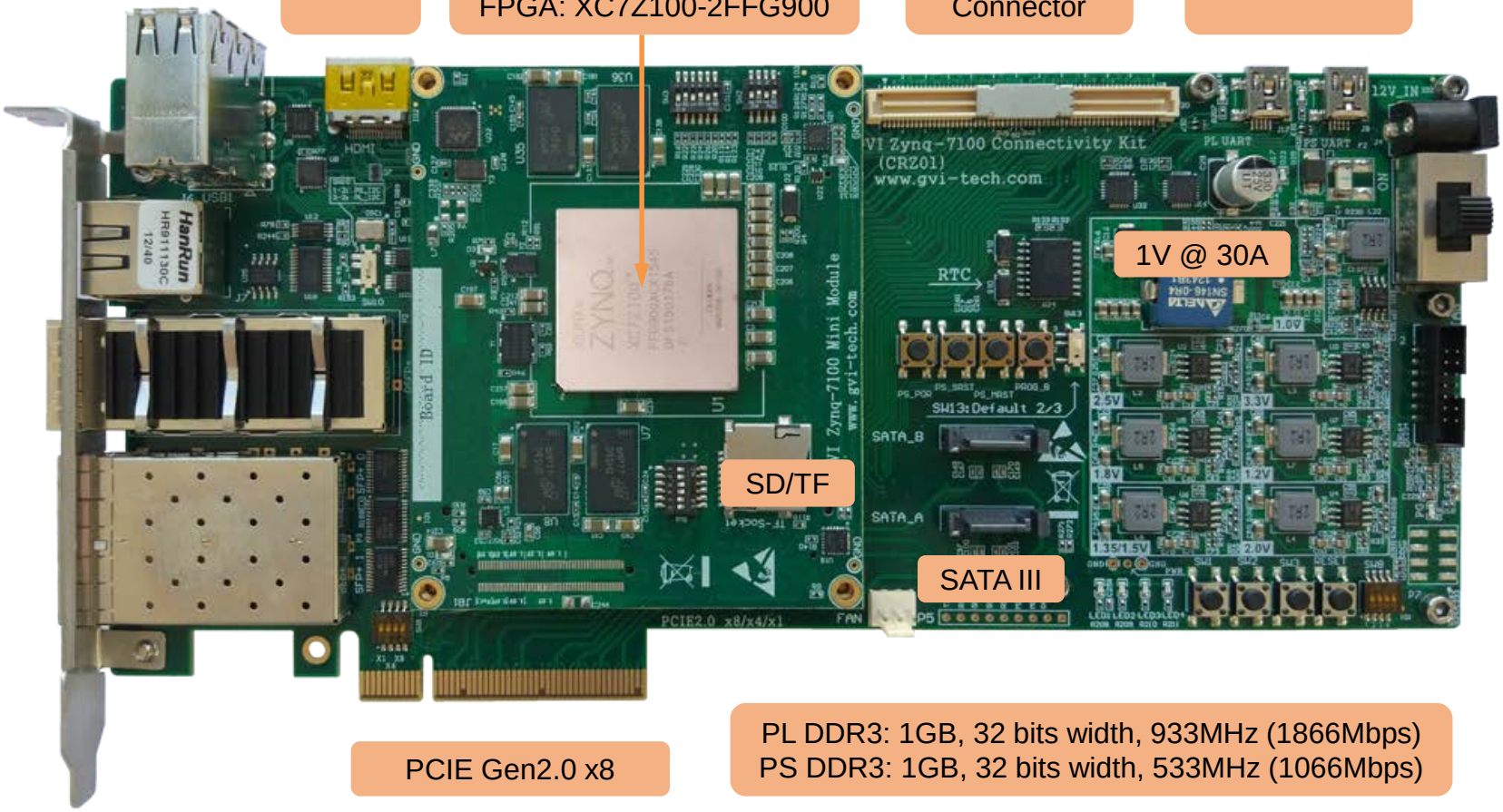
USB UART

4 x USB

RJ45 Gigabit Ethernet

QSFP+ 4x10Gbps.

Dual SFP+ interface. 2x10Gbps



PL DDR3: 1GB, 32 bits width, 933MHz (1866Mbps)
PS DDR3: 1GB, 32 bits width, 533MHz (1066Mbps)

Xilinx Software Requirement

- Xilinx Vivado Design Suite (version 2016.4 is used for development)

IBERT Overview

- Description

  The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the GTX transceivers. A graphical user interface is provided through the Vivado Hardware Manager.

- Reference Design IP

  LogiCORE IBERT Example Designs

Create IBERT Design

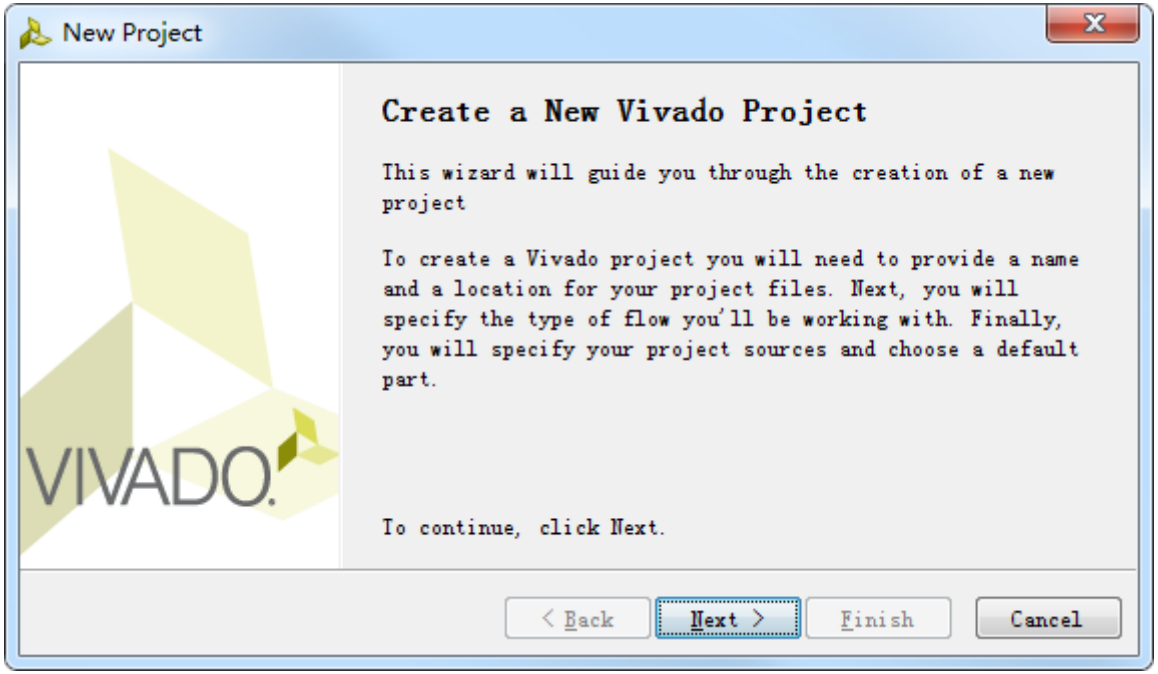
- Open Vivado

  Start → All Programs → Xilinx Design Tools → Vivado 2016.4 → Vivado

- Select Create New Project

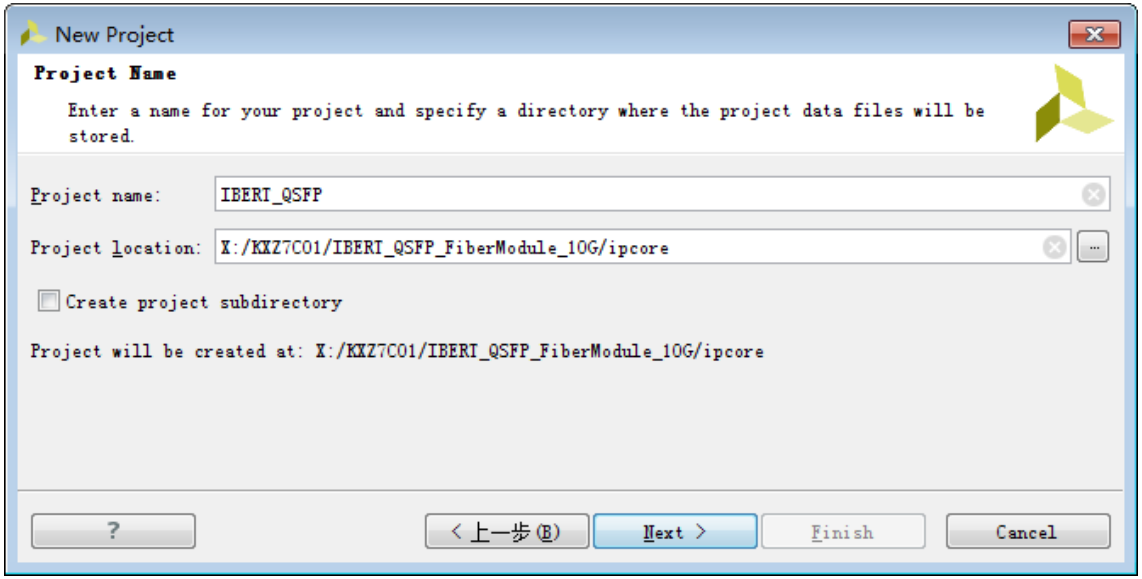
Create IBERT Design

- Click Next



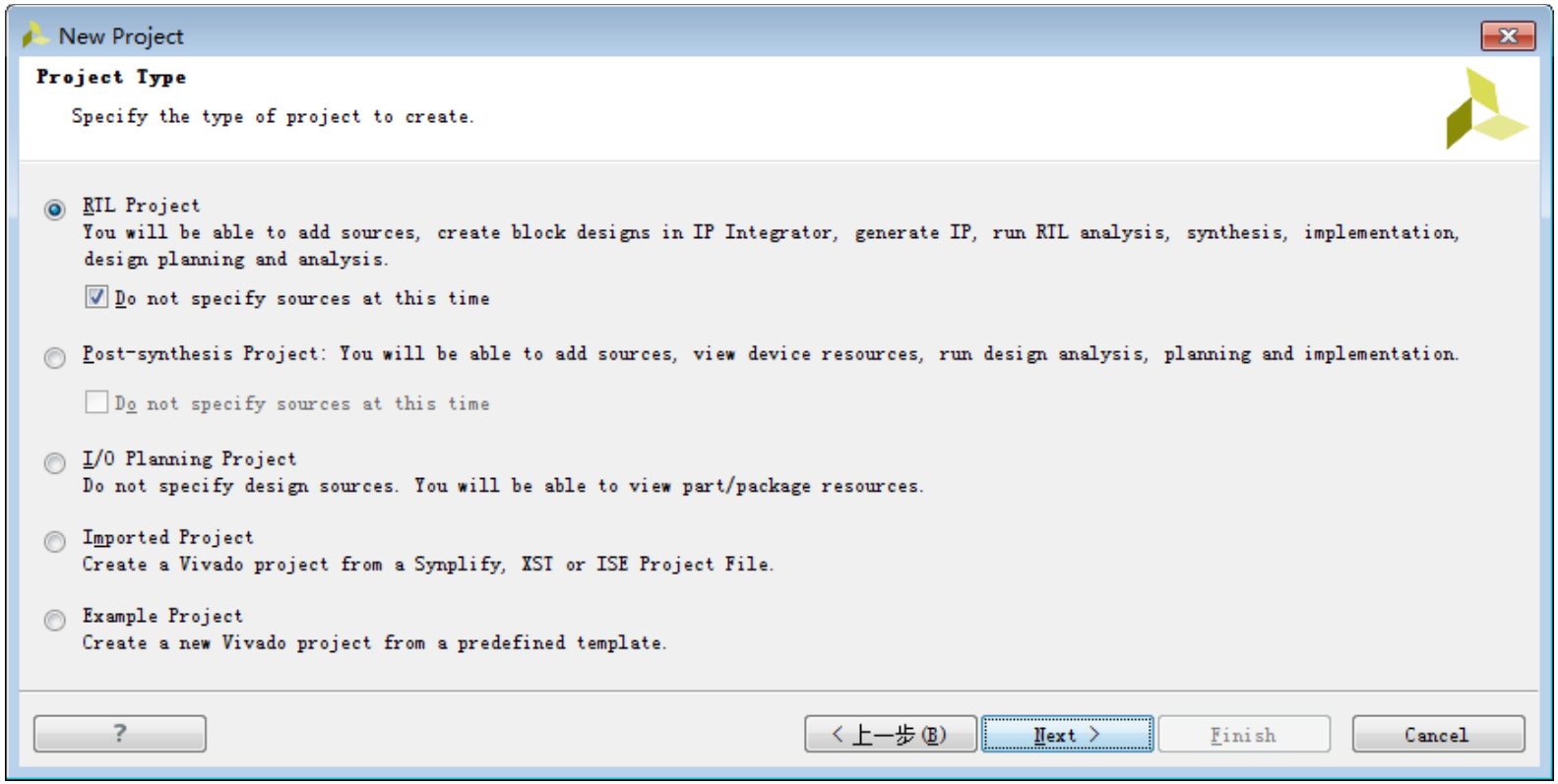
Create IBERT Design

- Set the Project name and location.



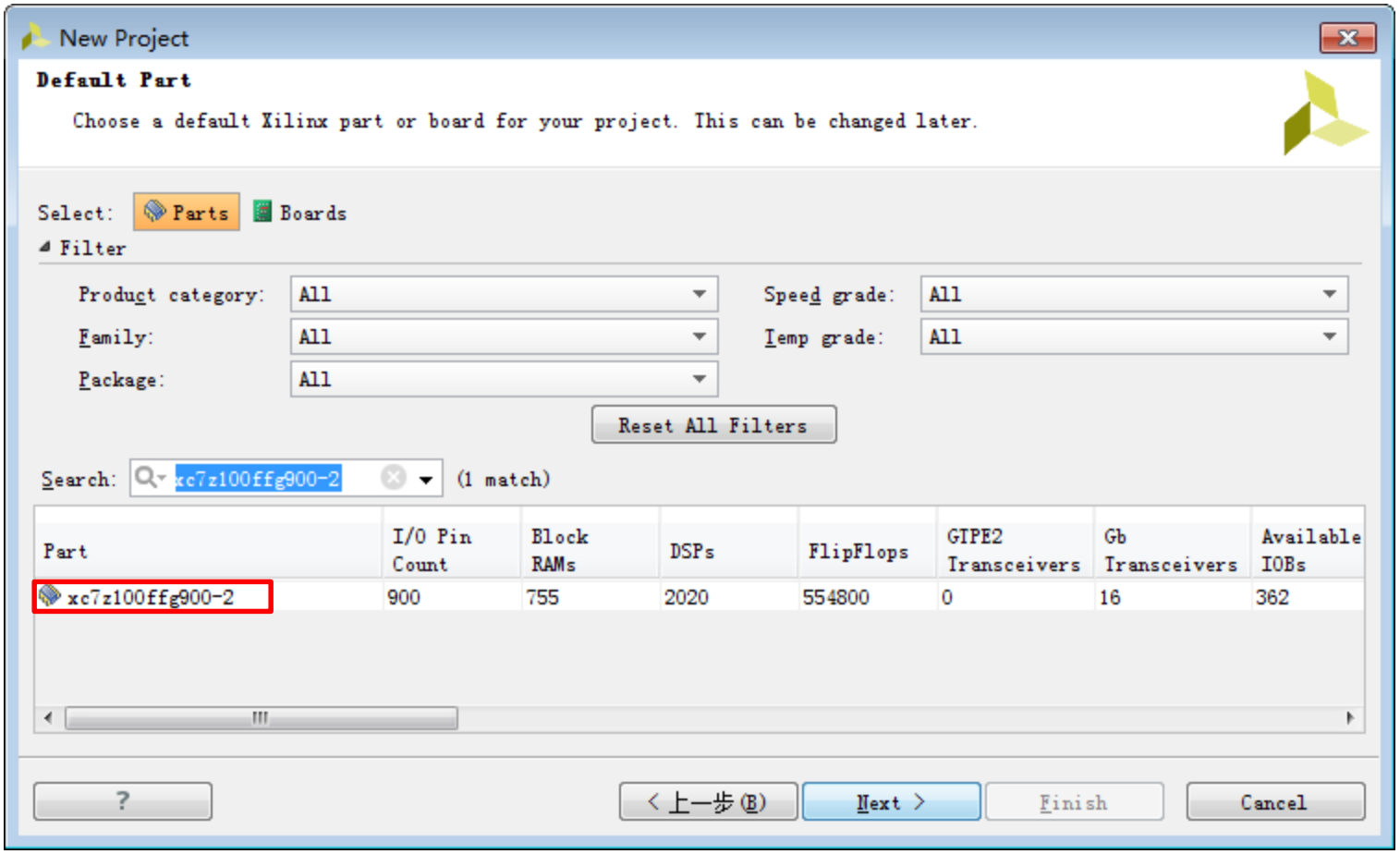
Create IBERT Design

- Select RTL Project
  - Select Do not specify sources at this time



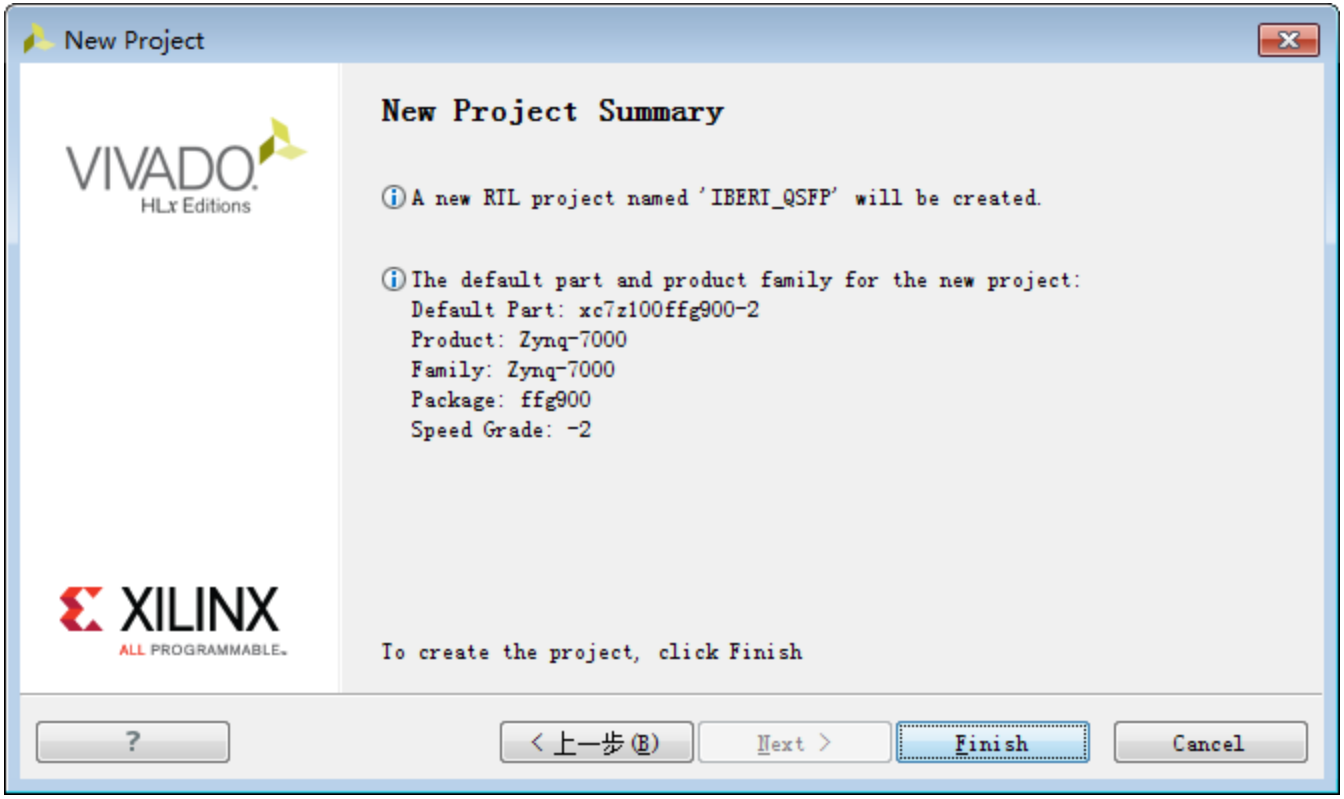
Create IBERT Design

- Select the FPGA part number: xc7z100ffg900-2



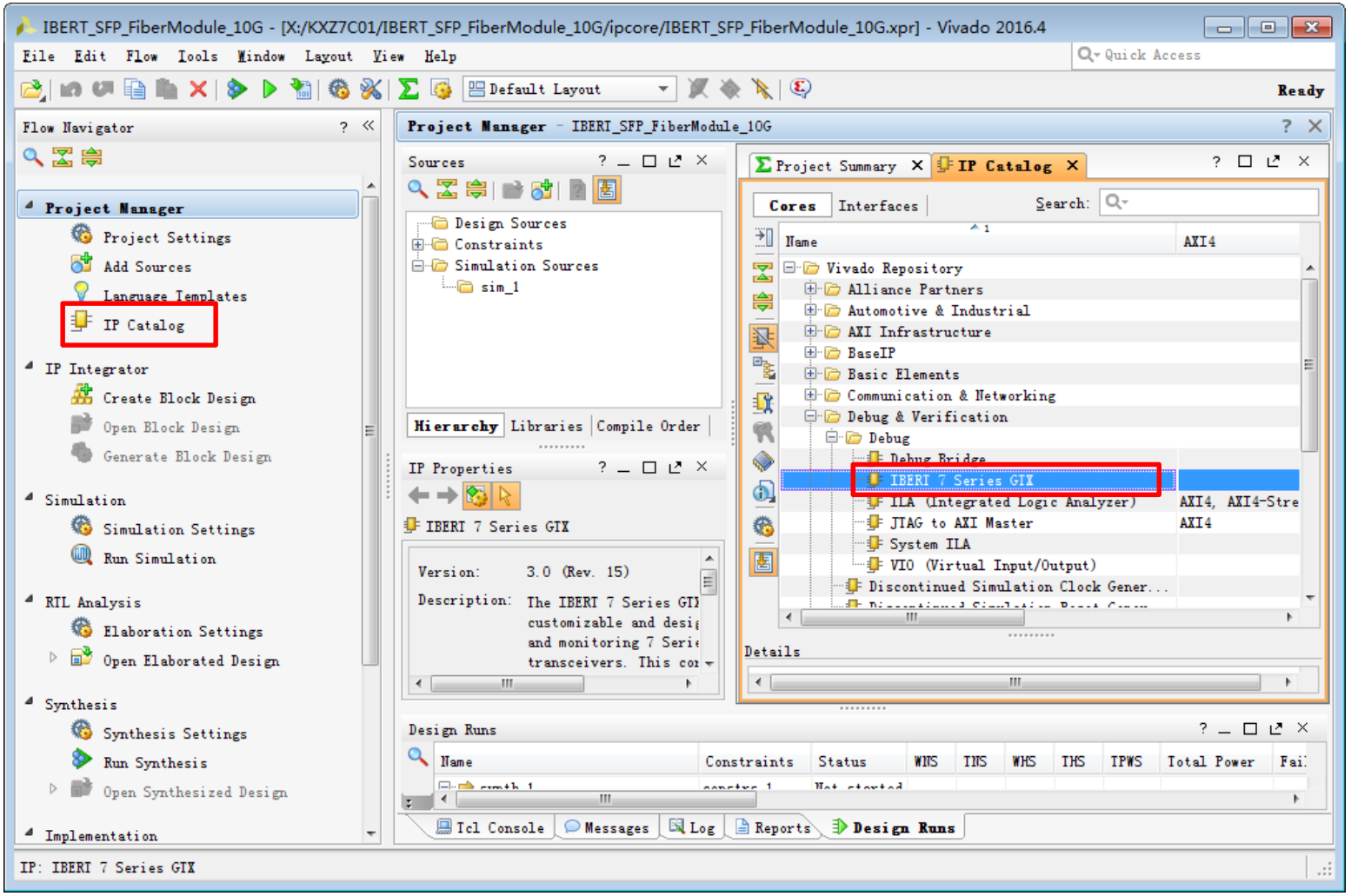
Create IBERT Design

- Click Finish



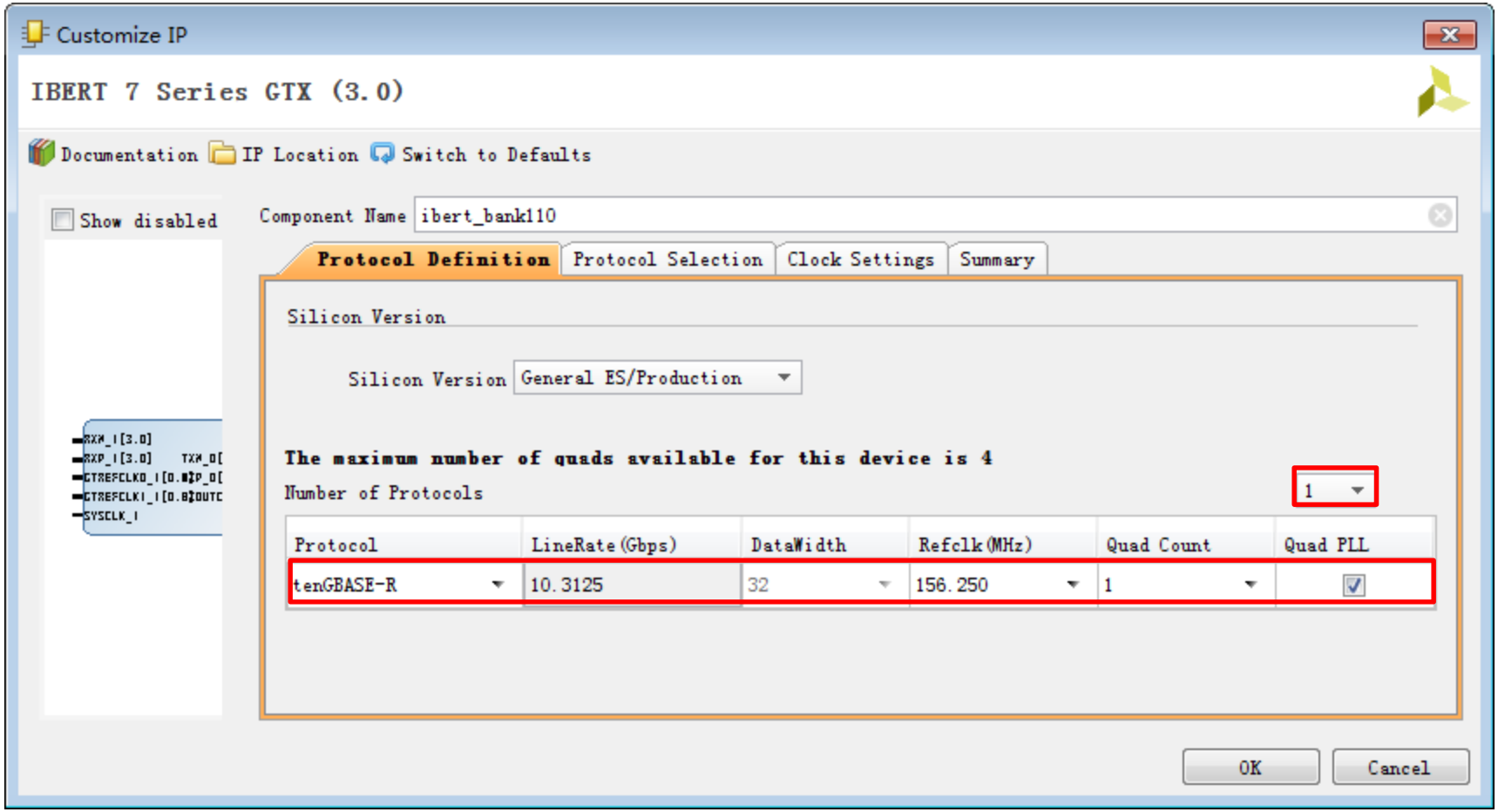
Create IBERT Design

- Click on IP Catalog, double click IBERT 7 Series GTX under Debug & Verification



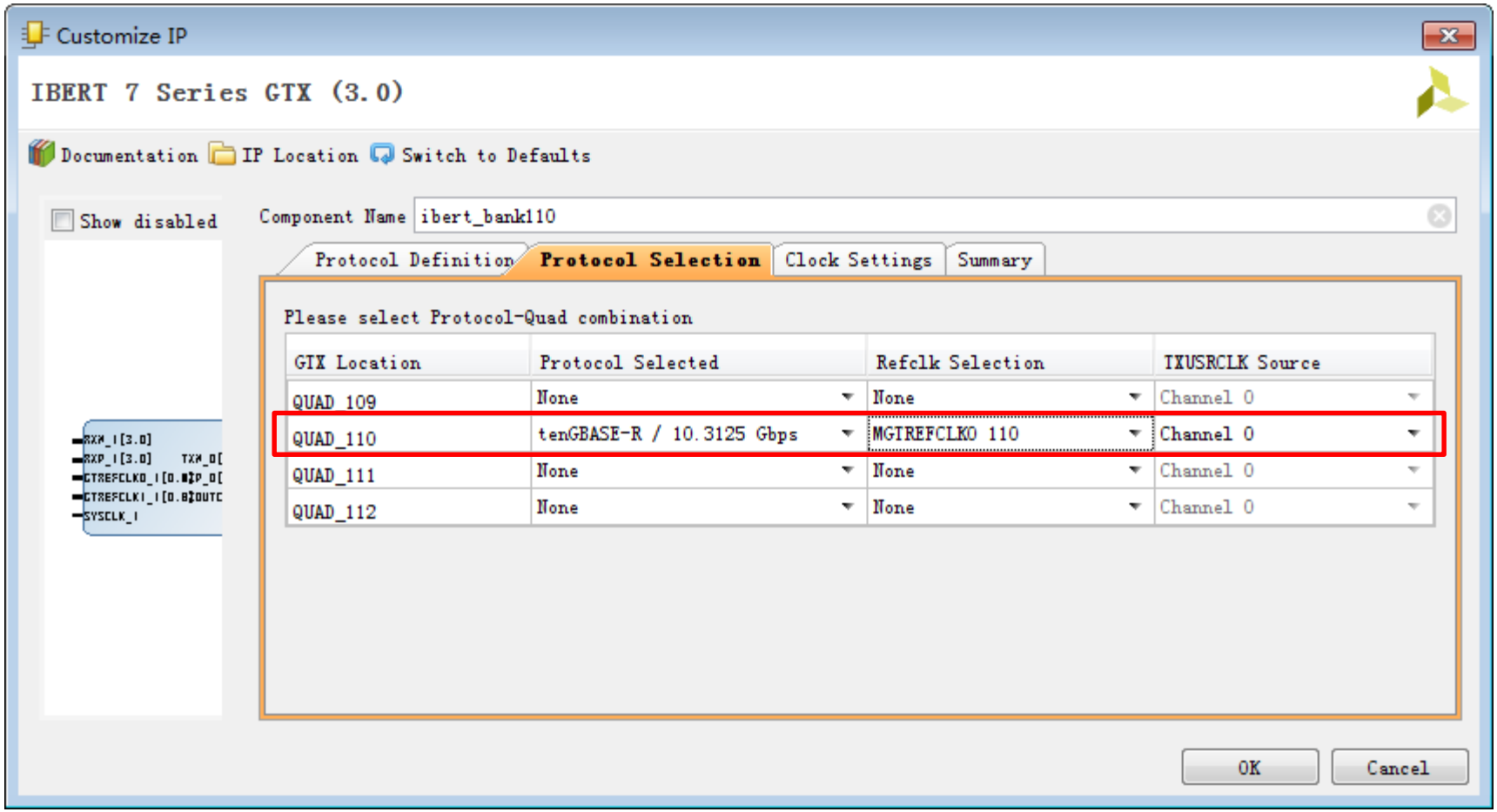
Create IBERT Design

- Set the Component name: ibert_bank110
- Under the Protocol Definition tab, set the parameters as follows:



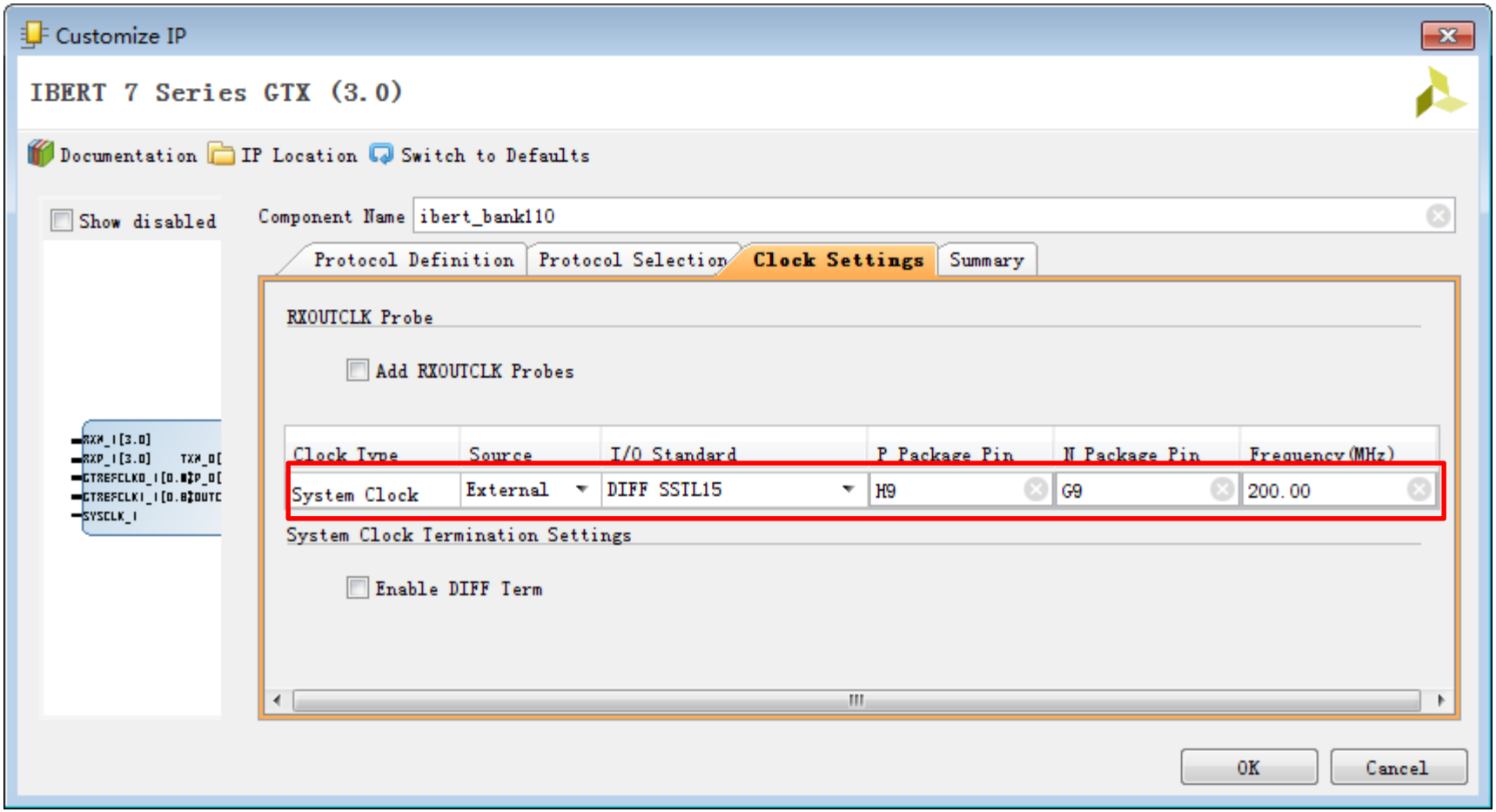
Create IBERT Design

- Under the Protocol Selection tab, set the parameters as follows:



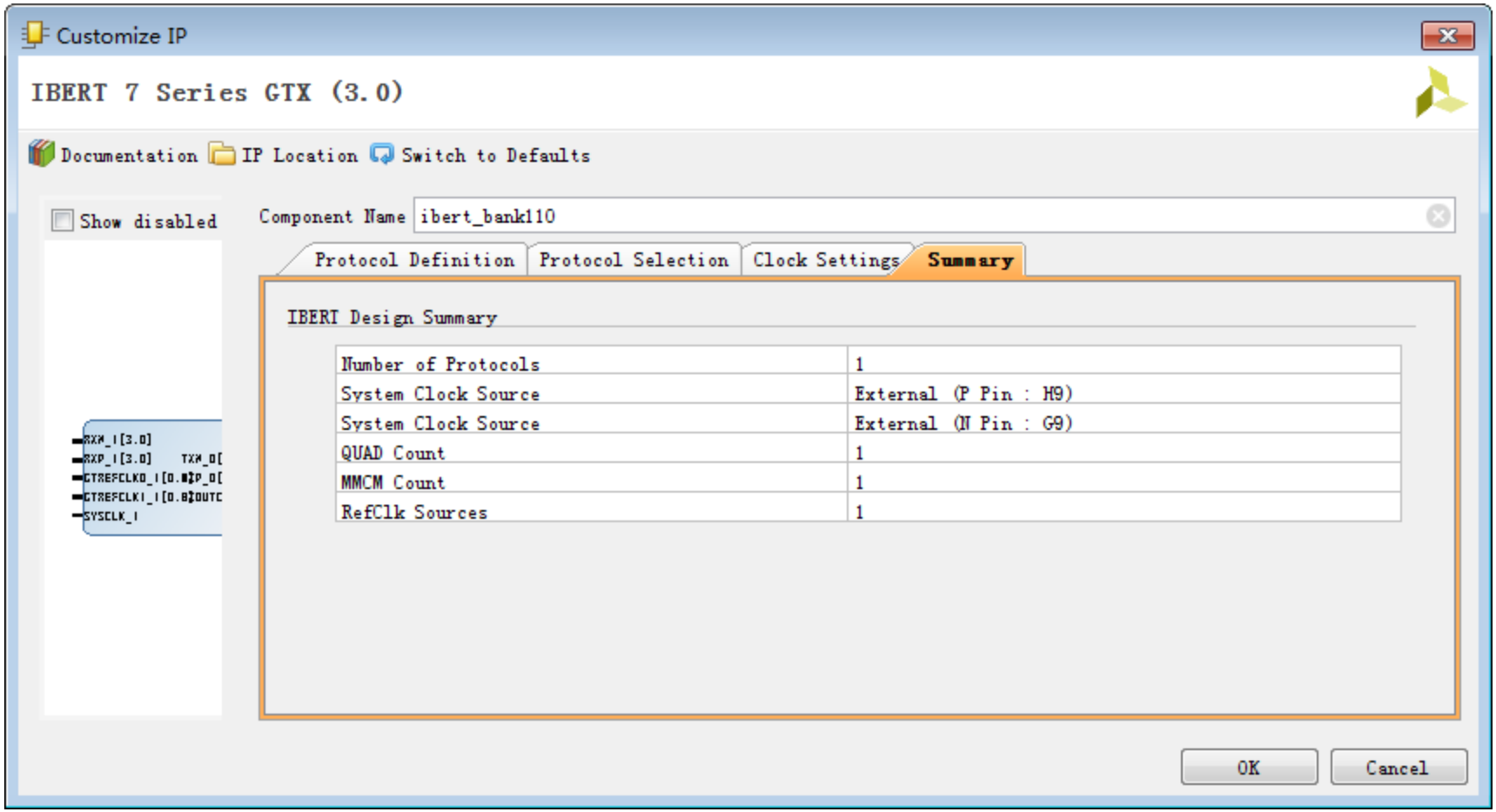
Create IBERT Design

- Under the Protocol Selection tab, set the parameters as follows:



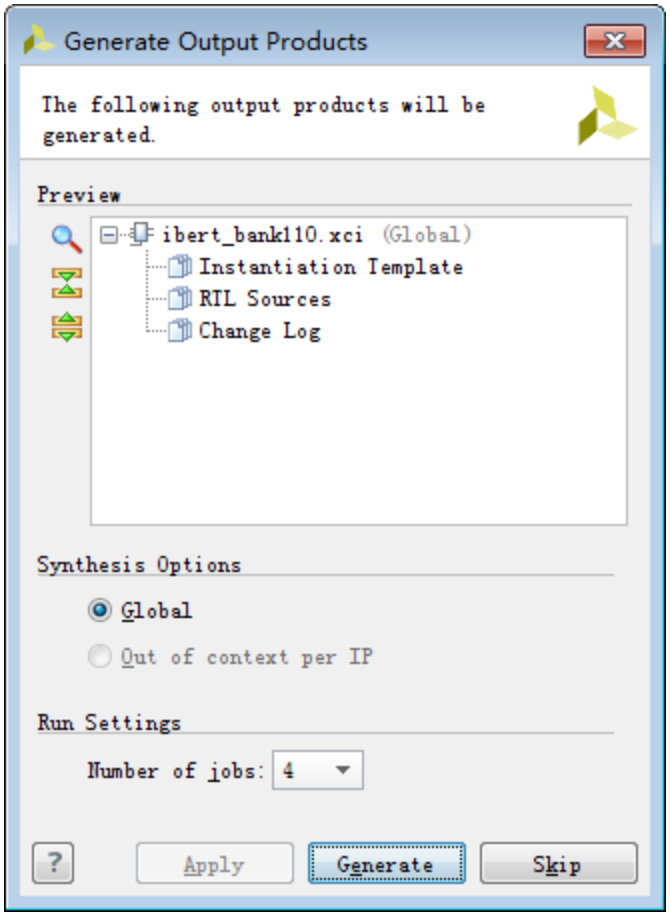
Create IBERT Design

- Review the summary and click OK



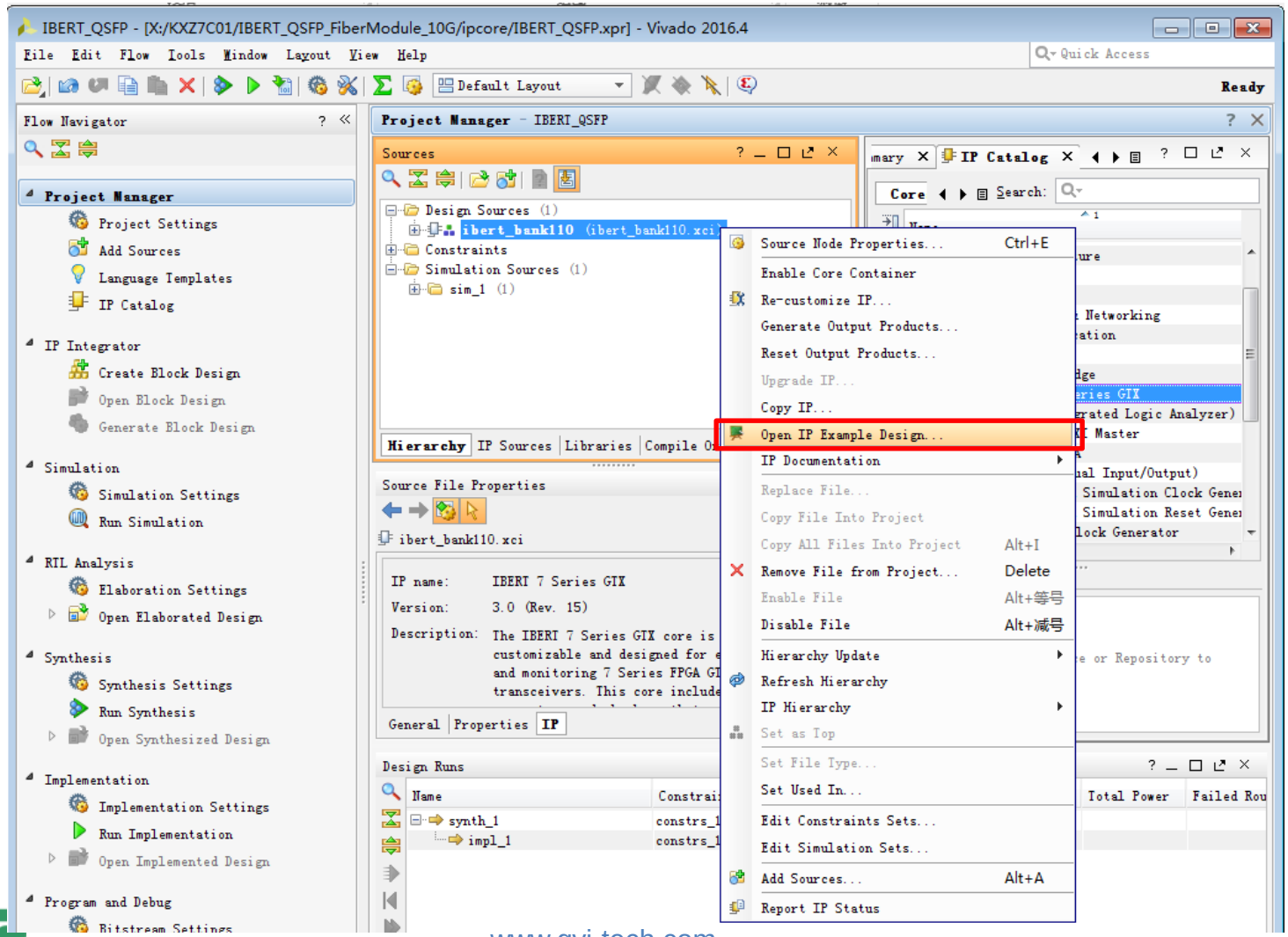
Create IBERT Design

- Click Generate



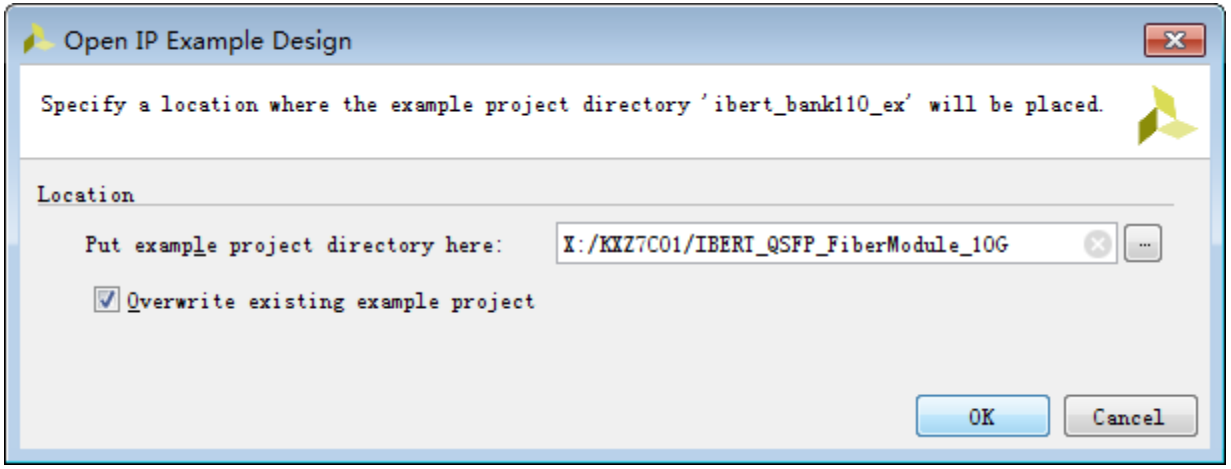
Compile Example Design

- Right click on ibert_bank110 and select Open IP Example Design...



Compile Example Design

- Set the location and click OK



Modify the Source Code

- In order to enable the TX circuit of the QSFP+ module, the following code need to be modified in the file “example_ibert_bank110.v”:

  output phy_reset_n,

  output ModSelL,

  output LPMode,

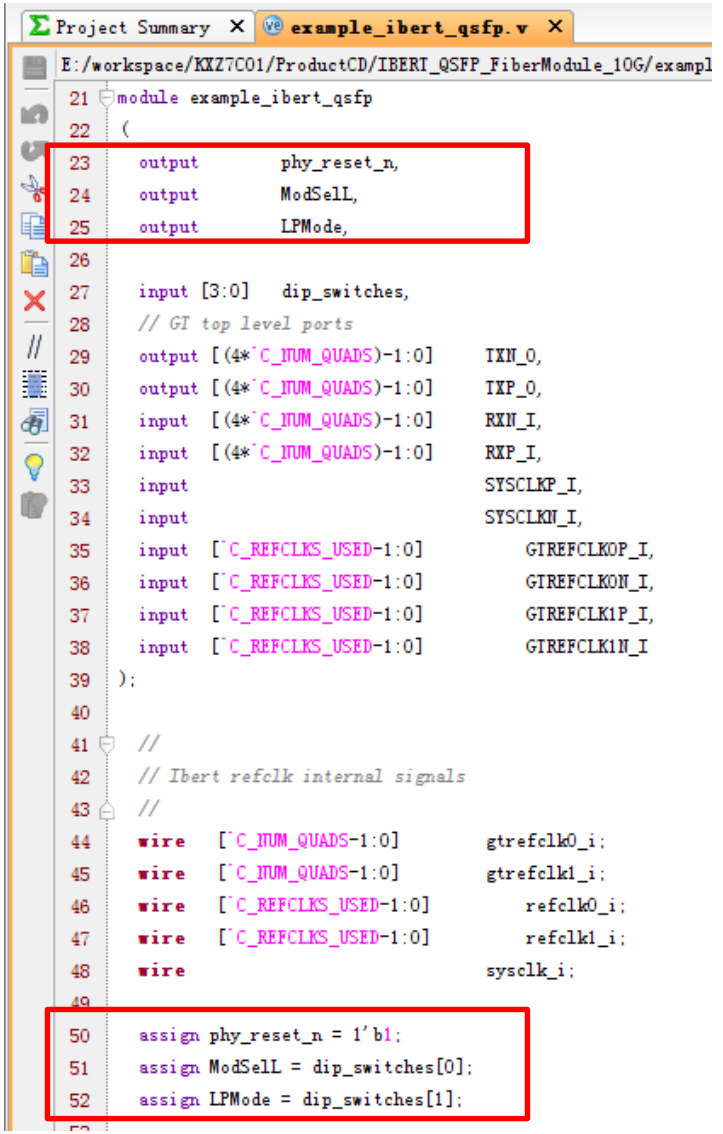
and

  assign phy_reset_n = 1'b1;

  assign ModSelL = dip_switches[0];

  assign LPMode = dip_switches[1];

- 不需要关注拨码开关 SW8 1和2的开关位置，预留功能



Modify the Source Code

- Add the constraints of phy0_tx_disable and phy1_tx_disable into the “example_ibert_bank109.xdc” file:

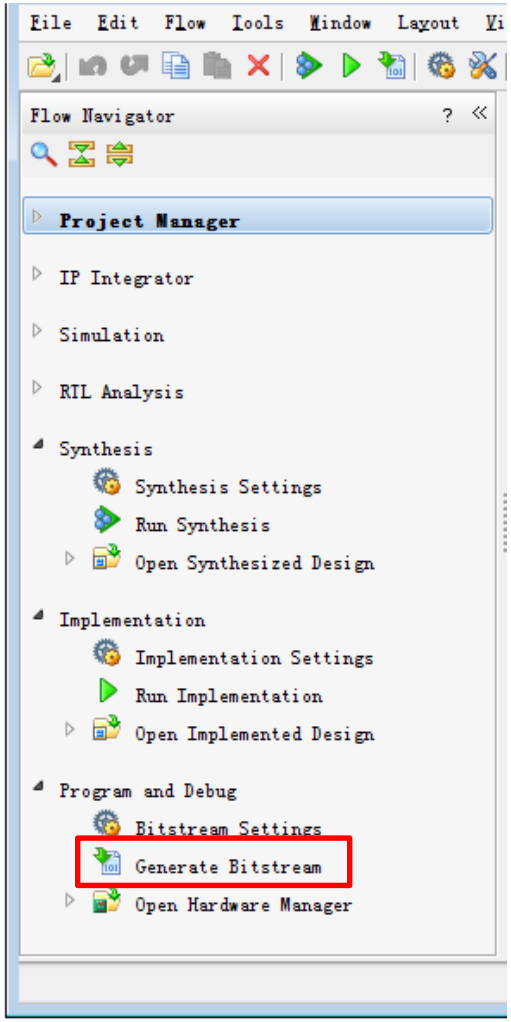
```
set_property PACKAGE_PIN E12 [get_ports phy_reset_n]
set_property IOSTANDARD LVCMOS18 [get_ports phy_reset_n]

set_property PACKAGE_PIN G17 [get_ports ModSelL]
set_property IOSTANDARD LVCMOS18 [get_ports ModSelL]

set_property PACKAGE_PIN G16 [get_ports LPMode]
set_property IOSTANDARD LVCMOS18 [get_ports LPMode]
```

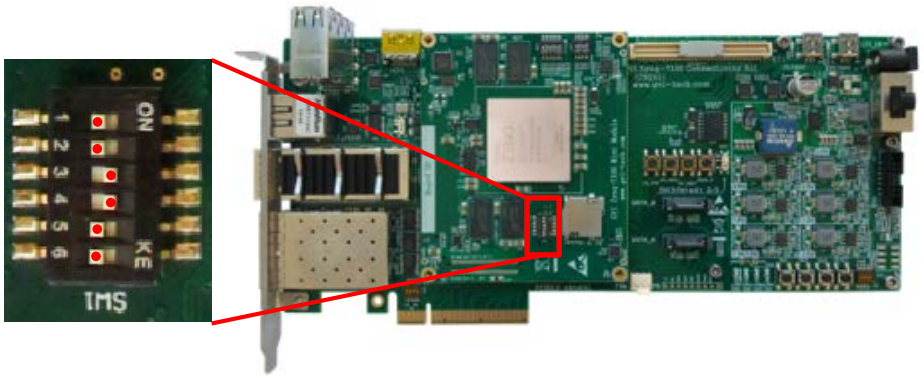
Compile Example Design

- Click Generate Bitstream.

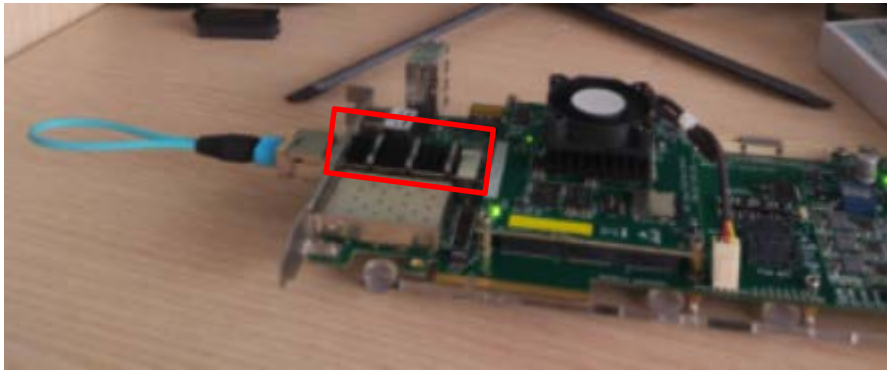


System Setup

- Set SW1 to
  OFF-OFF-ON-ON-OFF-OFF.
  This sets the frequency to 156.25MHz.



- Connect a loopback fiber into the 40G QSFP+ module, and then plug the 40G QSFP+ module into the QSFP+ connector.



System Setup

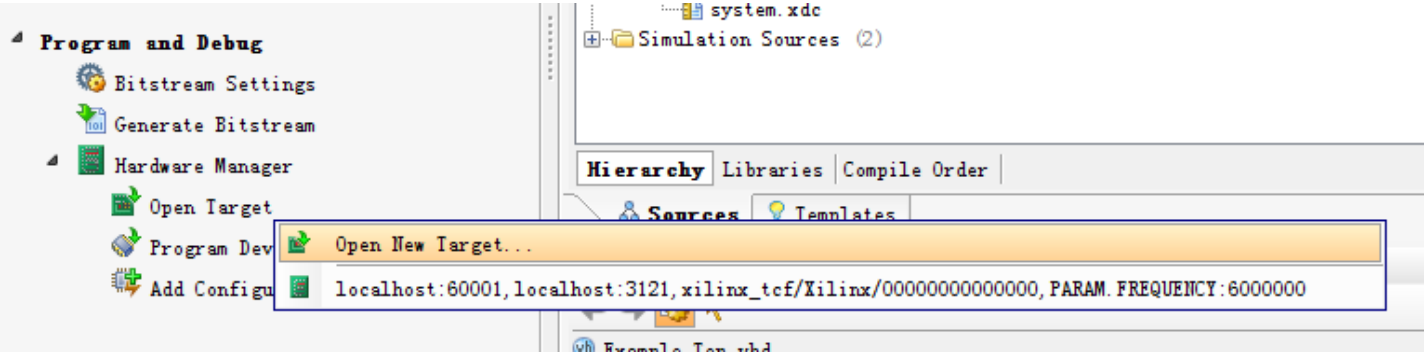
- Connect the JTAG cable to the base board.

- Connect the power supplier.

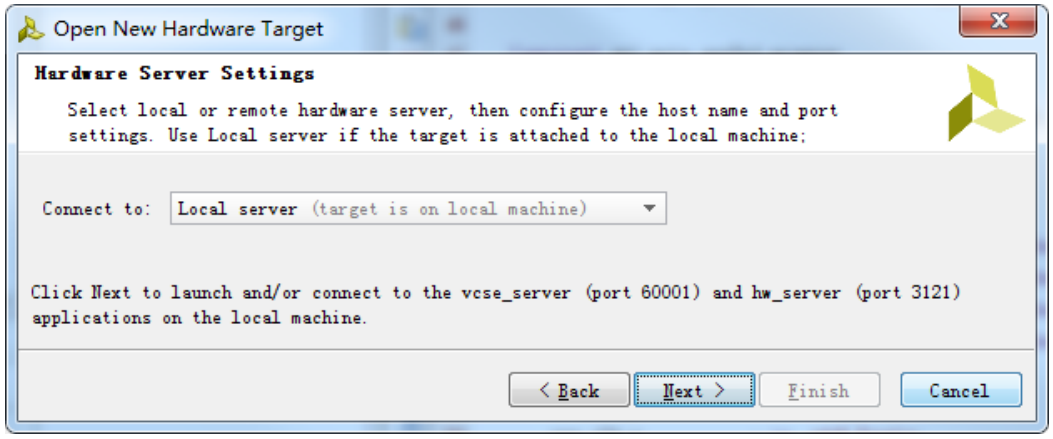
Order Hardware: https://detail.tmall.com/item.htm?id=562769965498

Configure FPGA

- Click “Open Target”, and then click “Open New Target…”

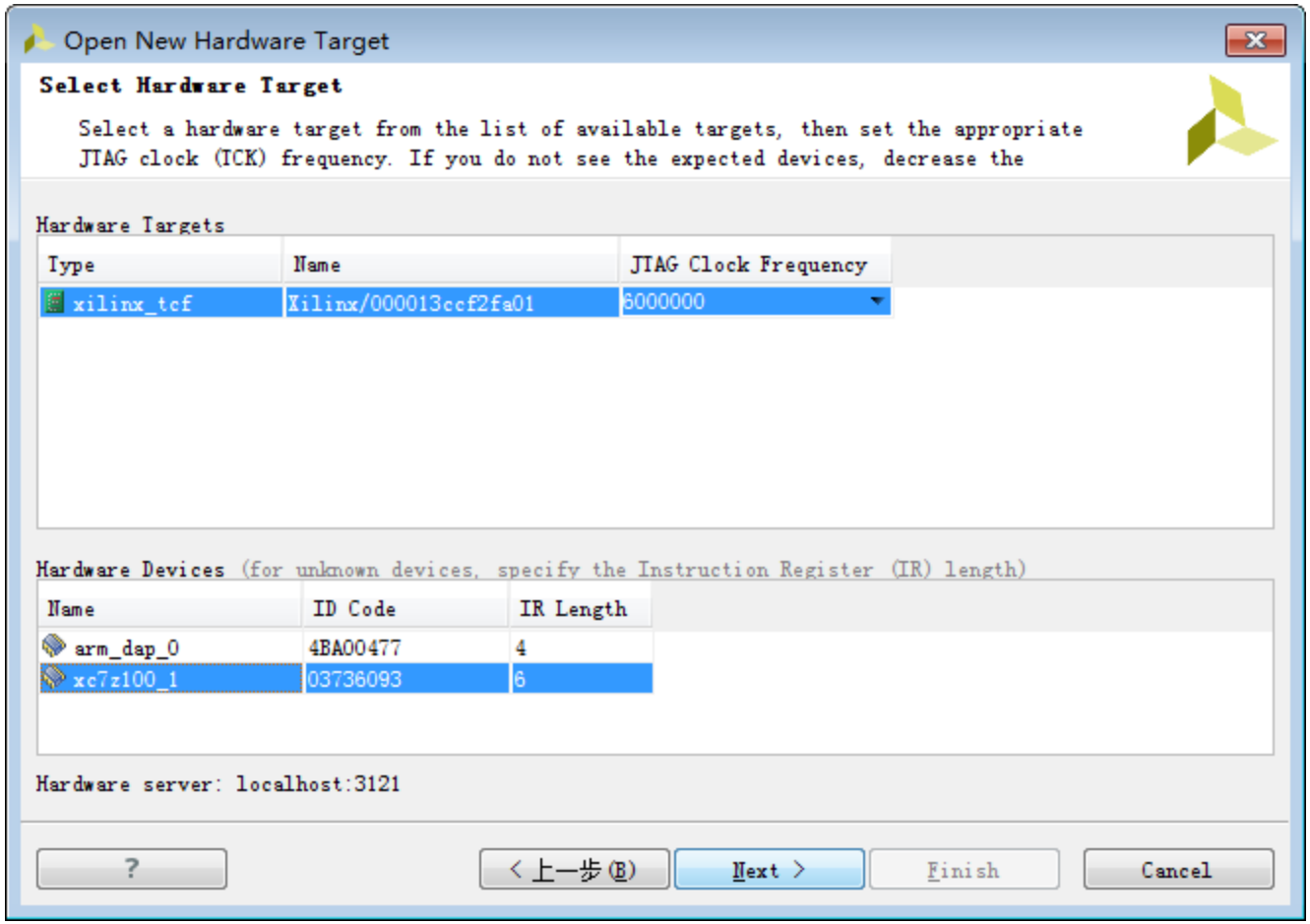


- In this dialog, choose “Local server”, and then click “Next”.



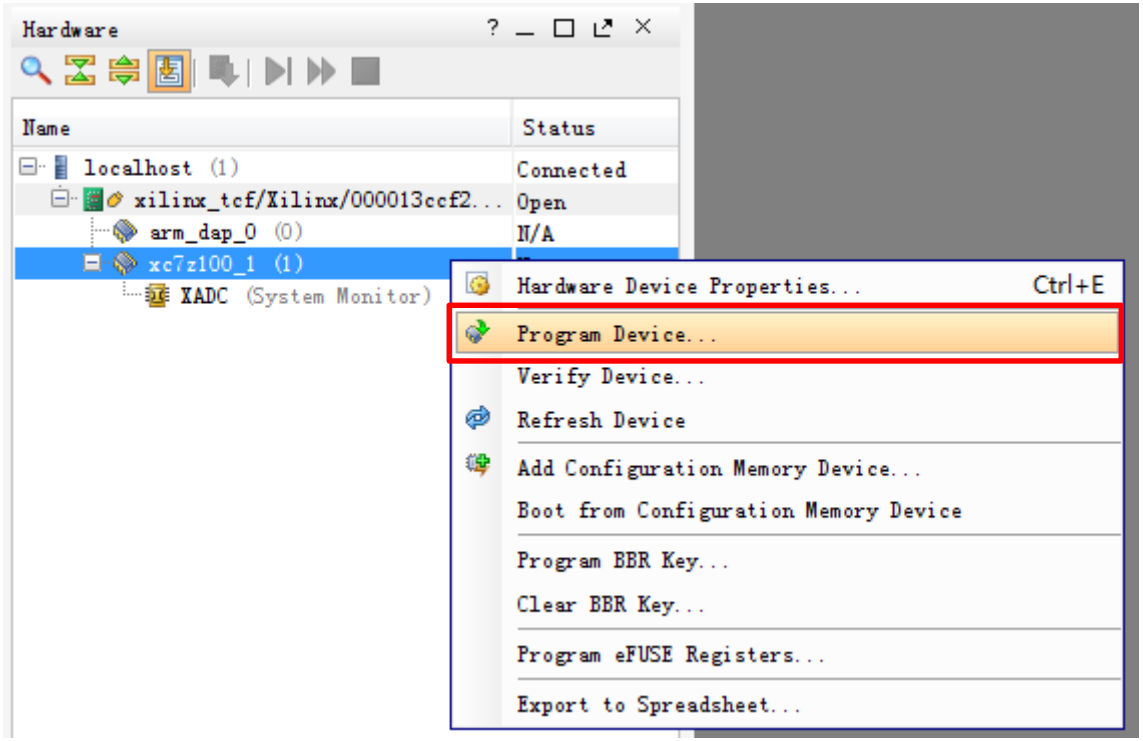
Configure FPGA

- Choose the target FPGA, and then click “Next”.



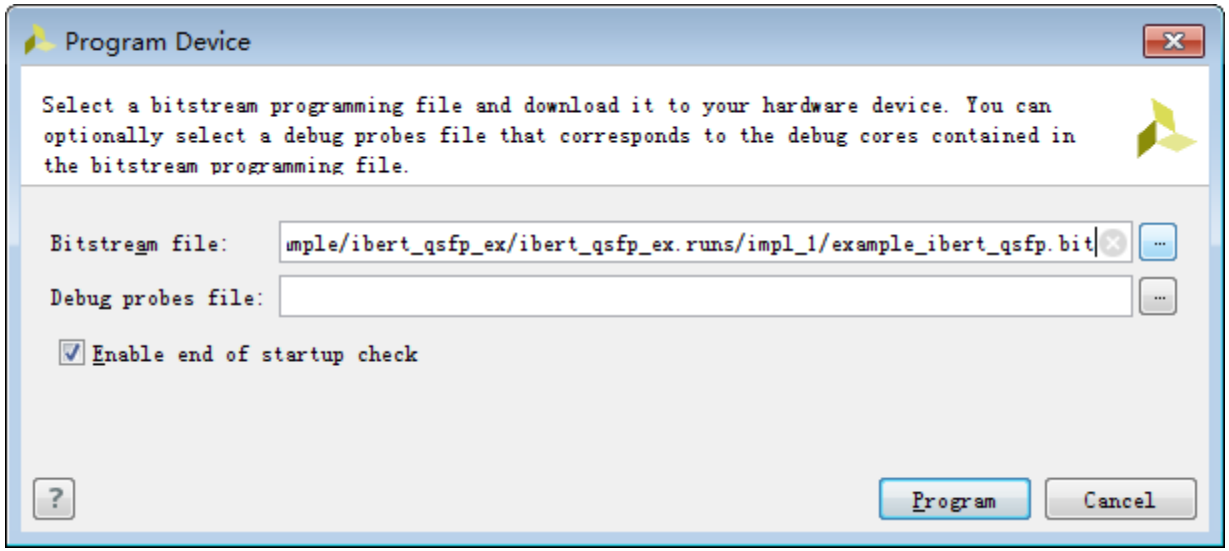
Configure FPGA

- Go to the “Hardware Manager” window.
- Right click on the FPGA, and then click “Program Device…”



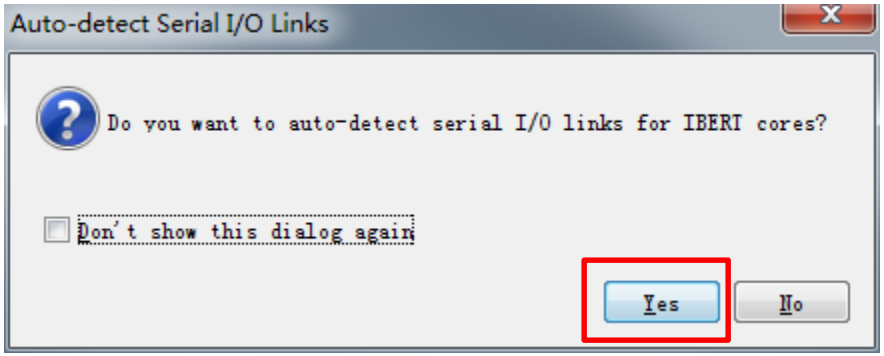
Configure FPGA

- In this dialog, choose the right bit file, and continue with “Program”.

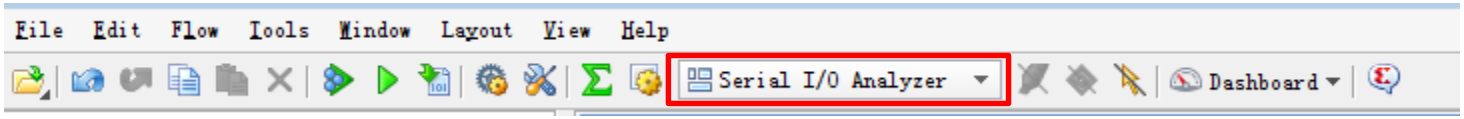


Configure FPGA

- At this step, click “Yes”.

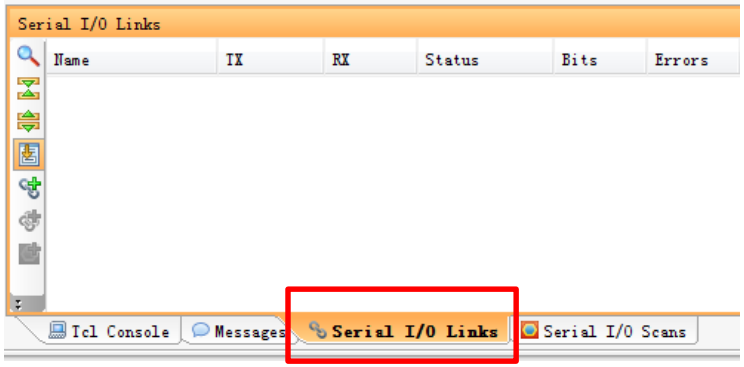


- If needed, set Vivado GUI layout to Serial I/O Analyzer



Configure “Serial I/O Analyzer” Window

- In the “Serial I/O Analyzer” window, select “Serial I/O Links” Tab.



Check Bit Error Rate of the Links

- Reset the BERT, and then check the detected errors. In normal case, no error should be detected.

ıe	TX	RX	Status	Errors	Bits	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing
Ungrouped Links (0)												
Found Links (4)							Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)
Found 0	MGI_X0Y4/TX	MGI_X0Y4/RX	10.313 Gbps	0E0	7.737E11	1.292E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)
Found 1	MGI_X0Y5/TX	MGI_X0Y5/RX	10.313 Gbps	0E0	7.738E11	1.292E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)
Found 2	MGI_X0Y6/TX	MGI_X0Y6/RX	10.313 Gbps	0E0	7.738E11	1.292E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)
Found 3	MGI_X0Y7/TX	MGI_X0Y7/RX	10.313 Gbps	0E0	7.738E11	1.292E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)

Reference

- More design resources can be found :

  www.gvi-tech.com

- How to Buy：
  - https://detail.tmall.com/item.htm?id=562769965498