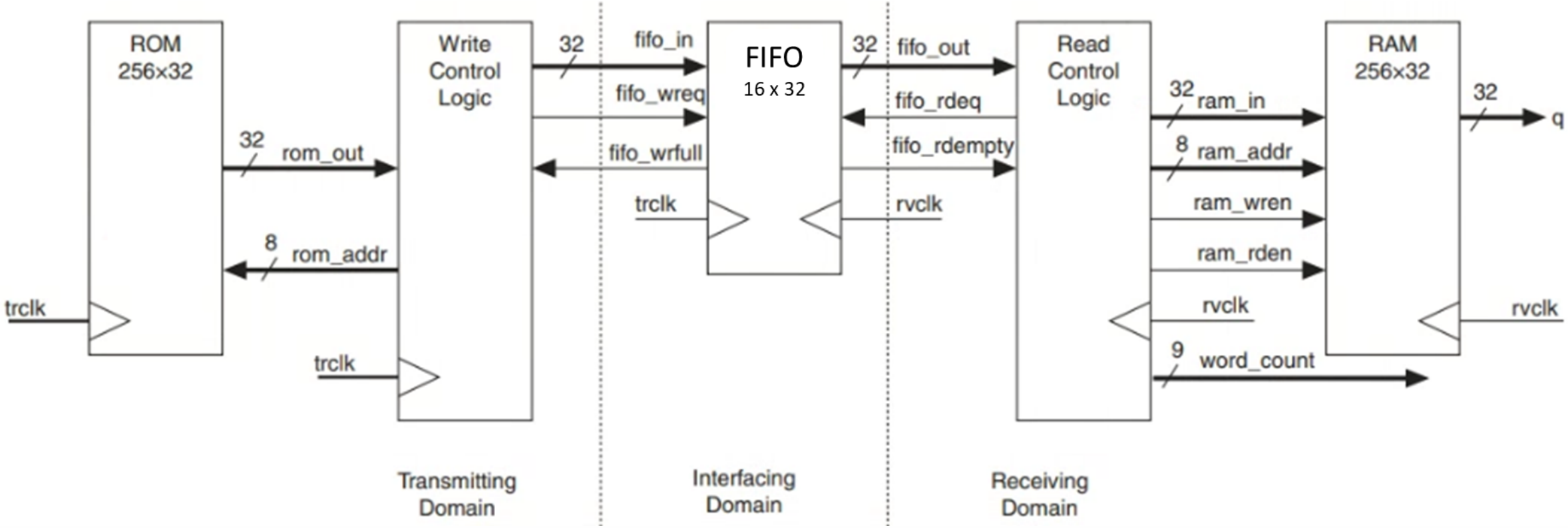
Reading & Writing Control of ROM to FIFO to RAM

XILINX.

Agenda

- Structure of Circuit
- Finite-State Machine
- Results of Simulation
- Timing Constraints
- Results of Synthesis

Structure of Circuit



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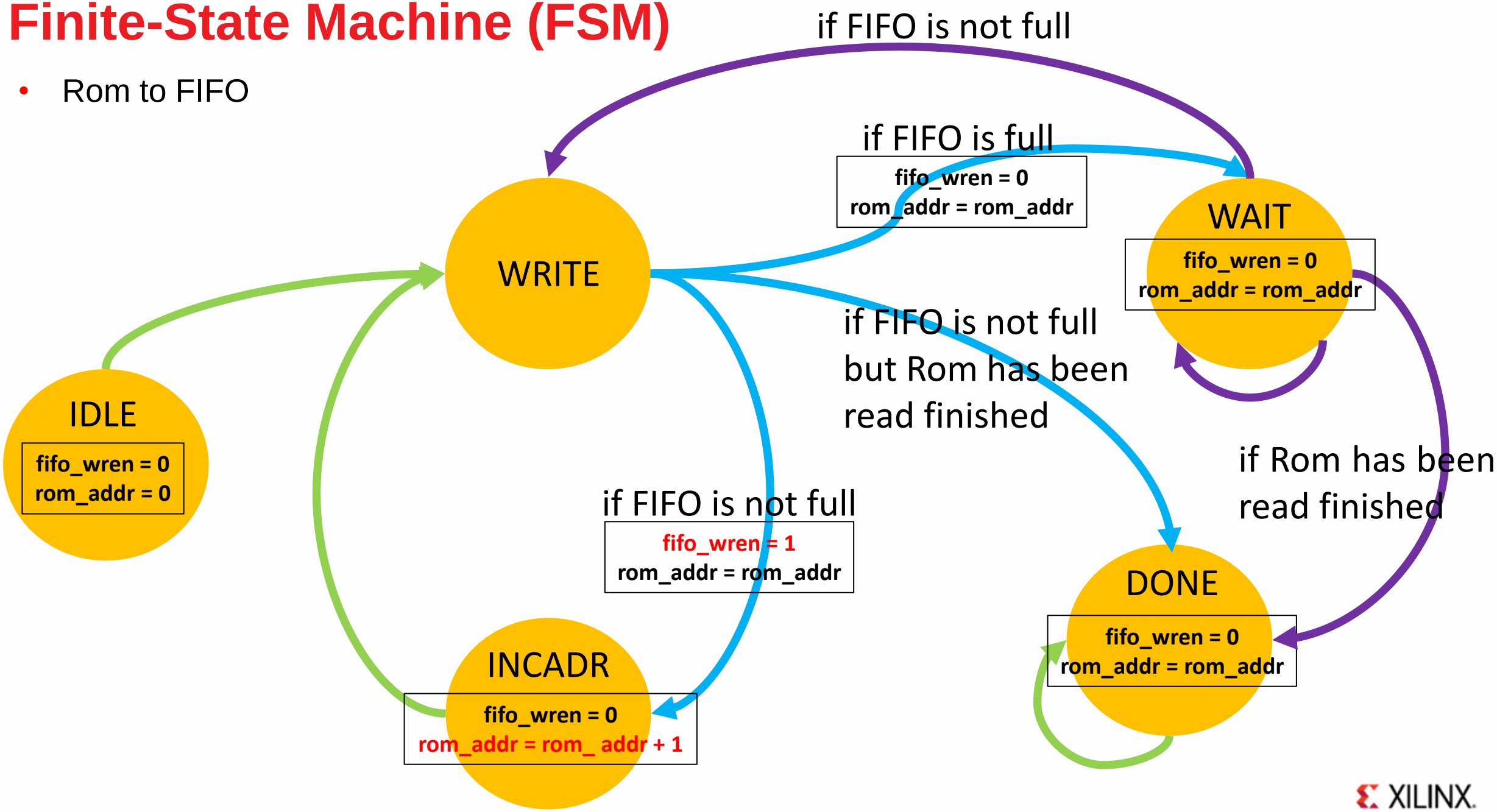
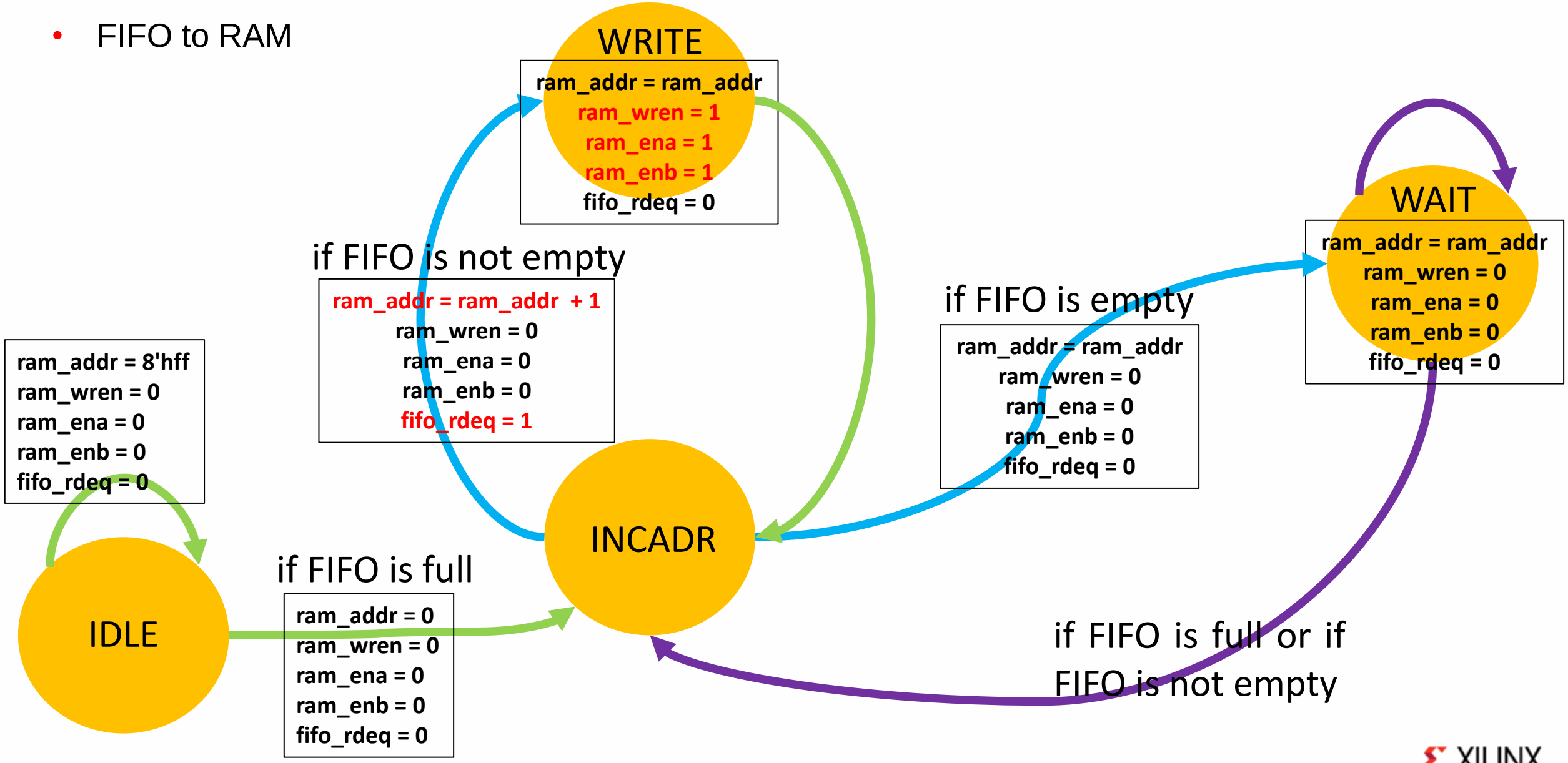
Finite-State Machine (FSM)

- Rom to FIFO

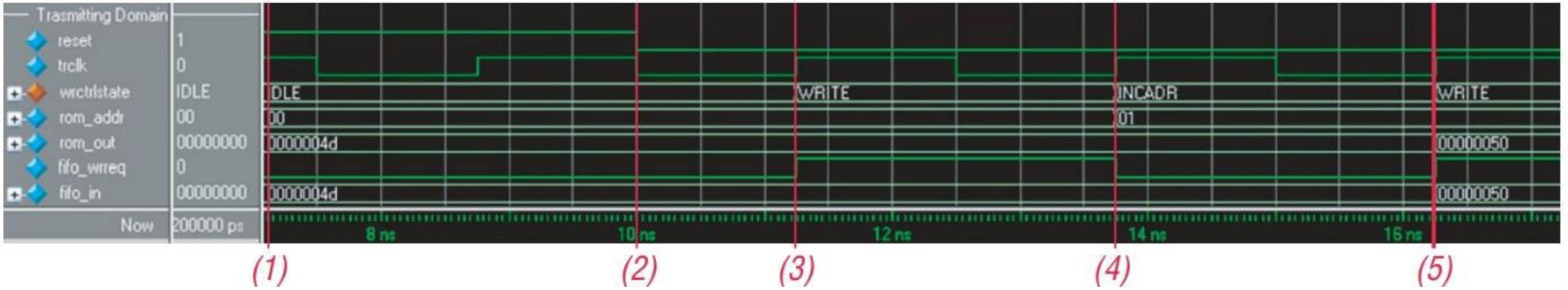


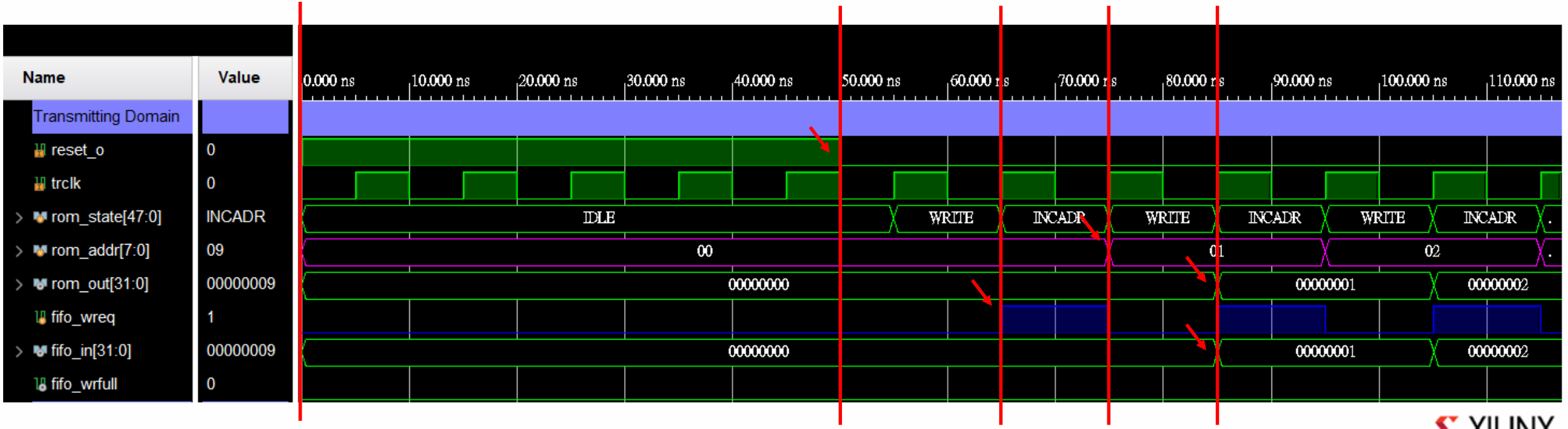
Finite-State Machine (FSM)

- FIFO to RAM



Results of Simulation – Transmitting Domain





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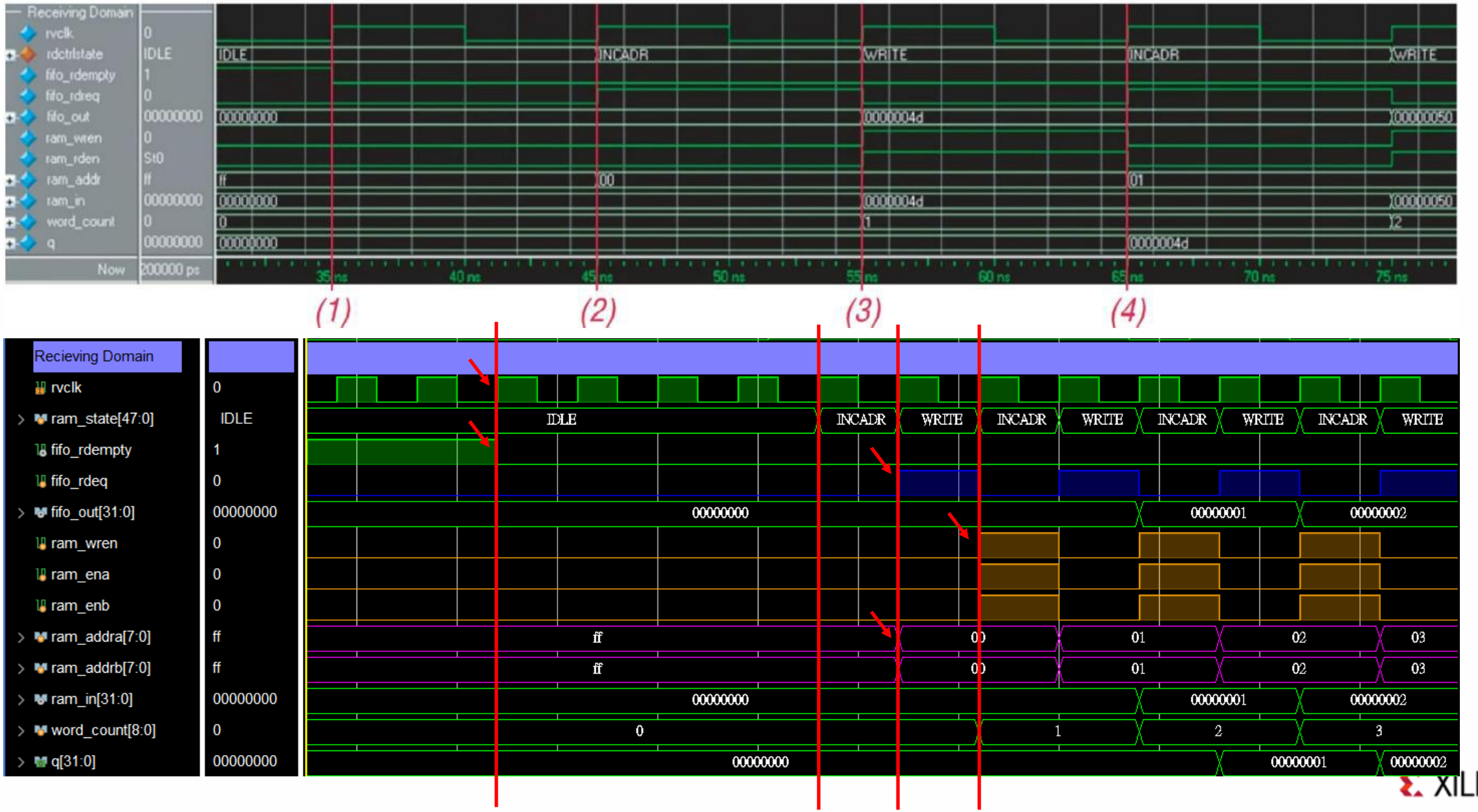
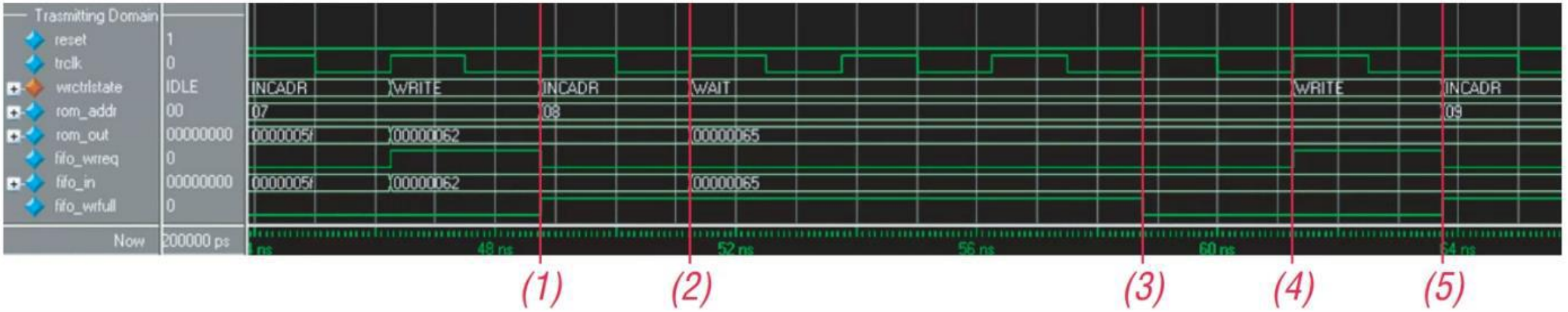
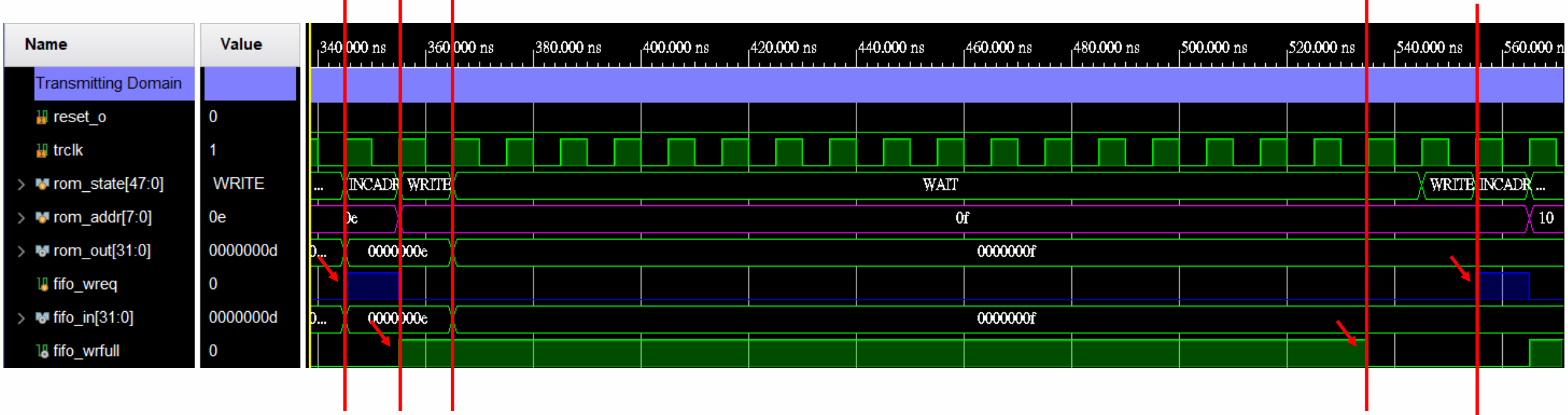
Results of Simulation – Receiving Domain



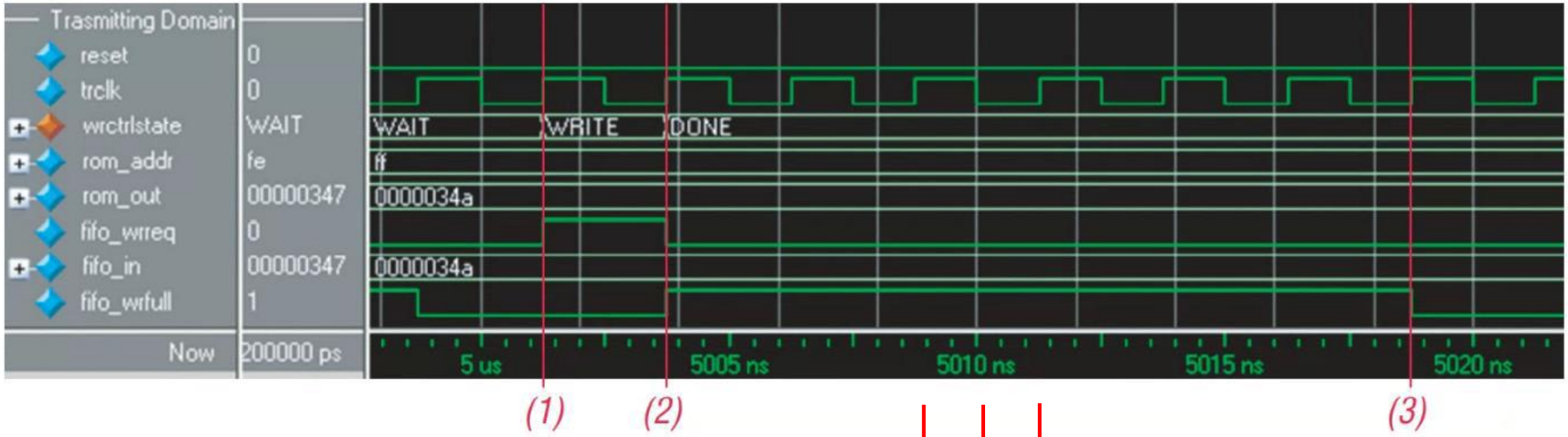
Results of Simulation – When FIFO is full

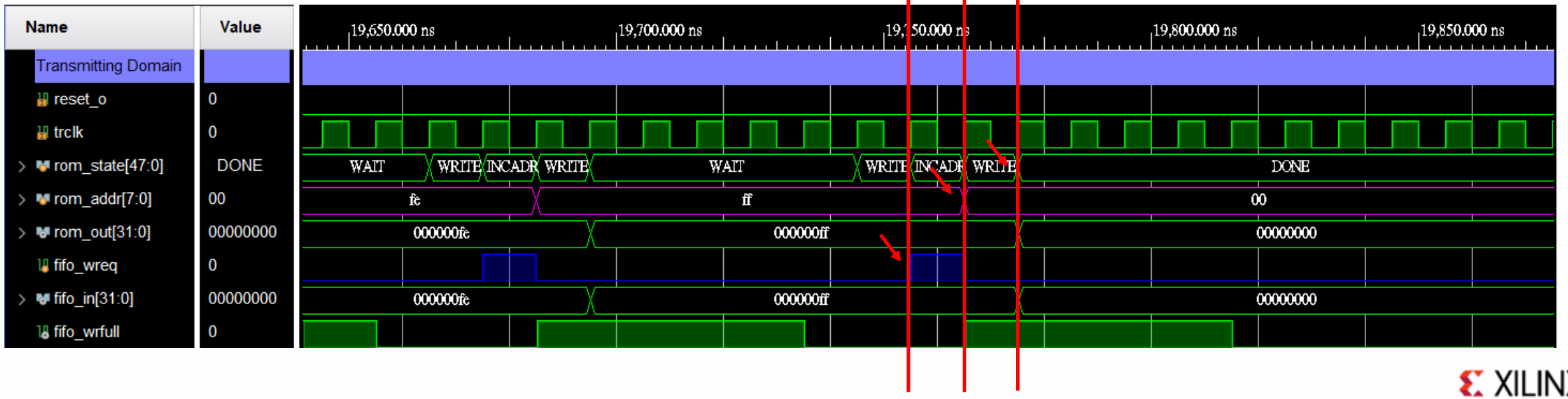




XILINX.

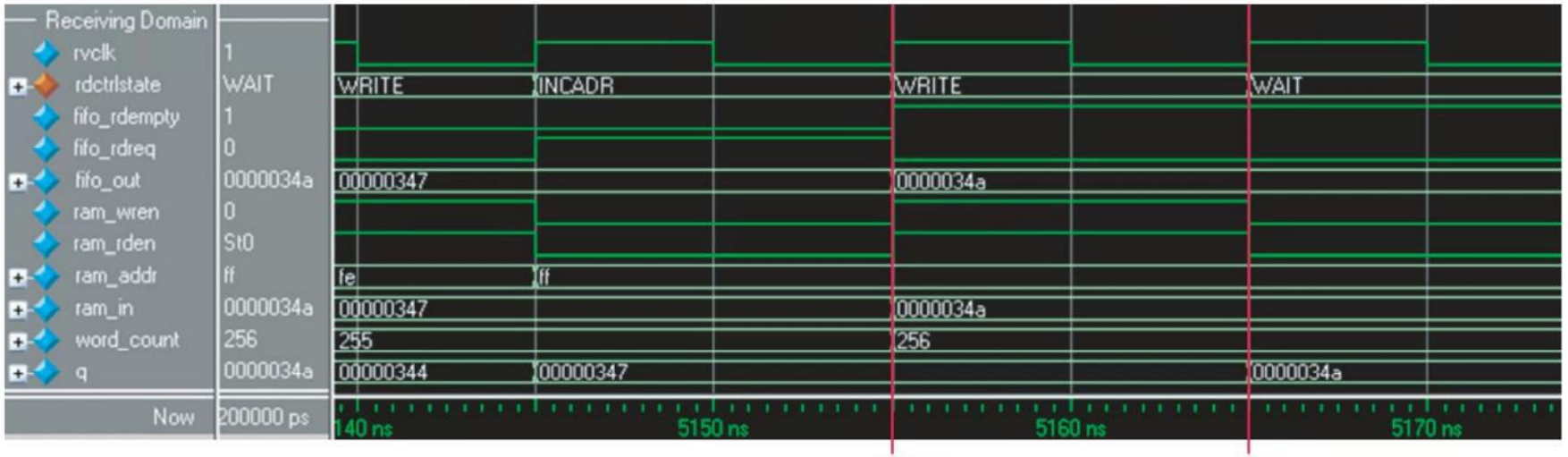
Results of Simulation – completion of ROM to FIFO

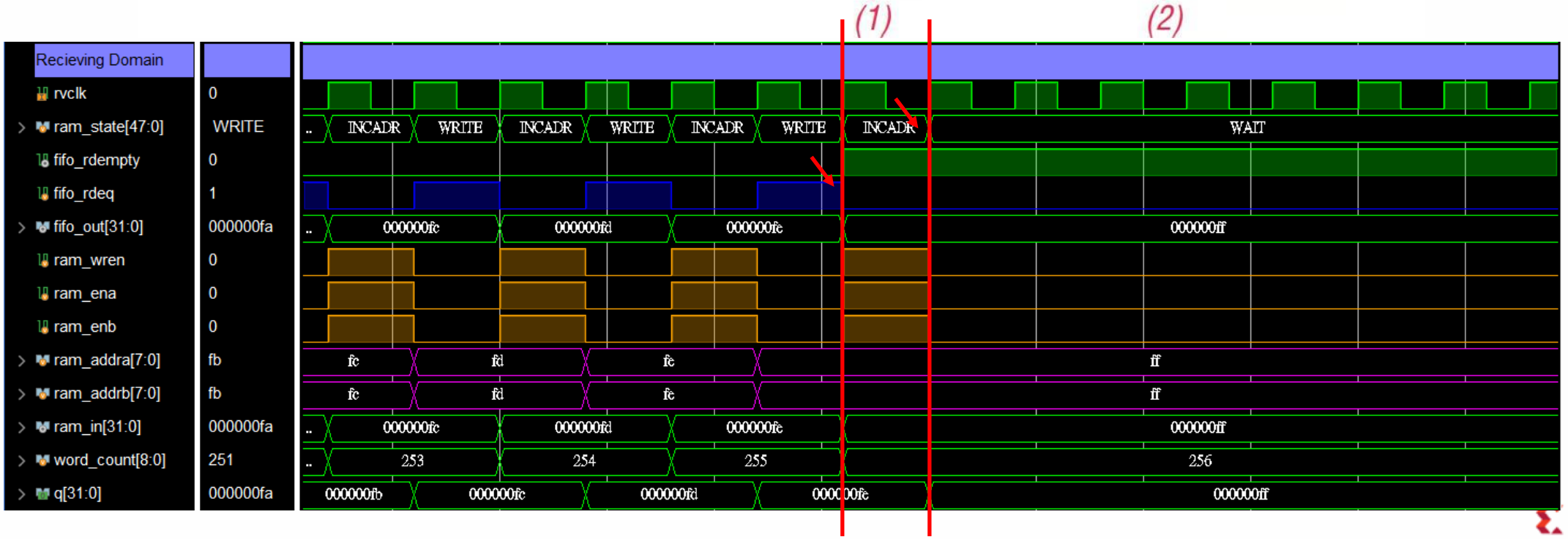




XILINX.

Results of Simulation – completion of FIFO to RAM





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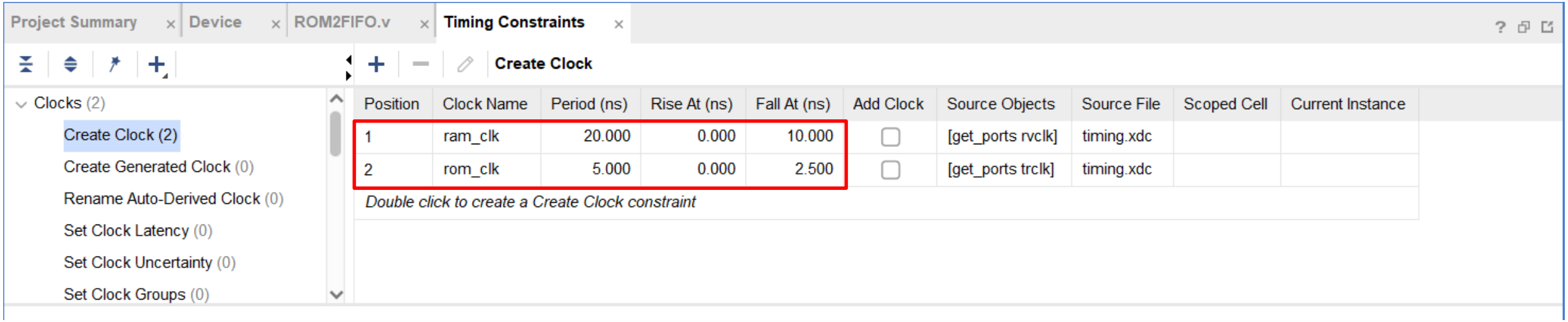
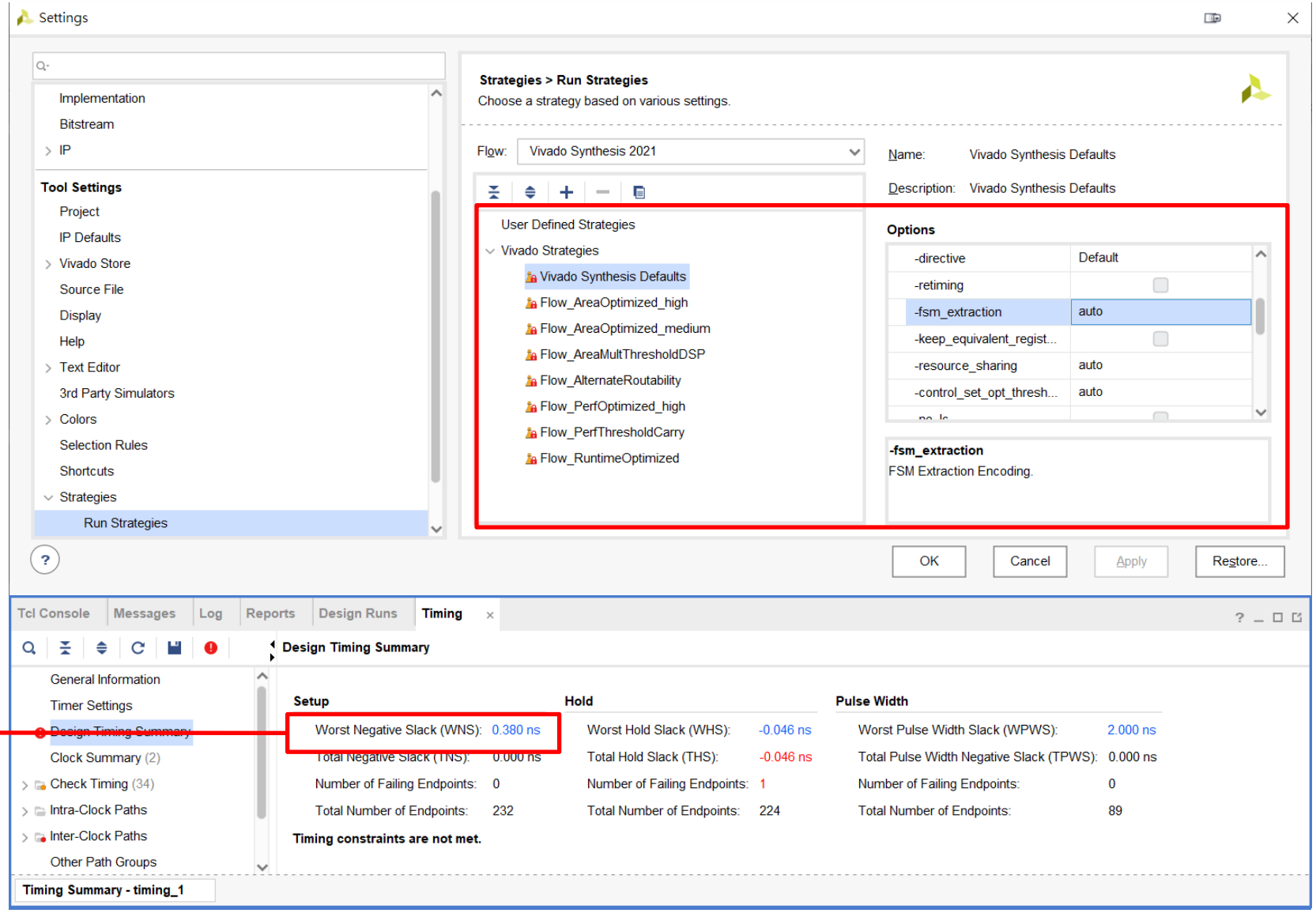
Timing Constraints

- trclk is 200MHz, and rvclk is 50MHz



Results of Synthesis

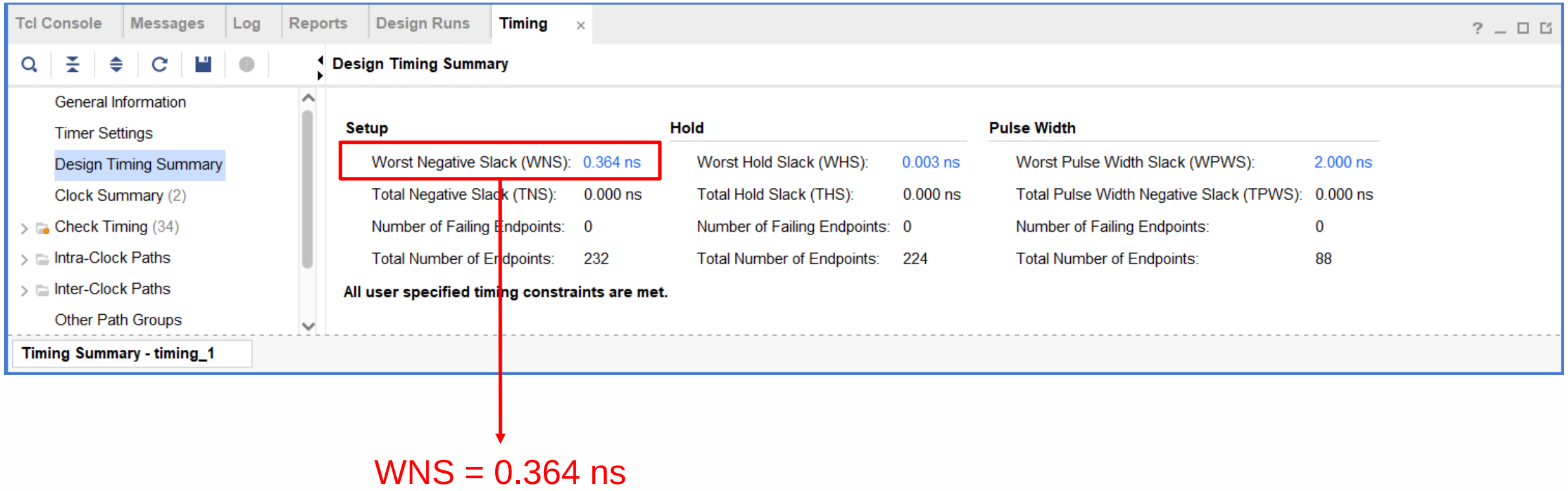
- fsm_extraction: auto



WNS = 0.380 ns

Results of Synthesis

- fsm_extraction: gray



WNS = 0.364 ns

Thank you very much for your attention!

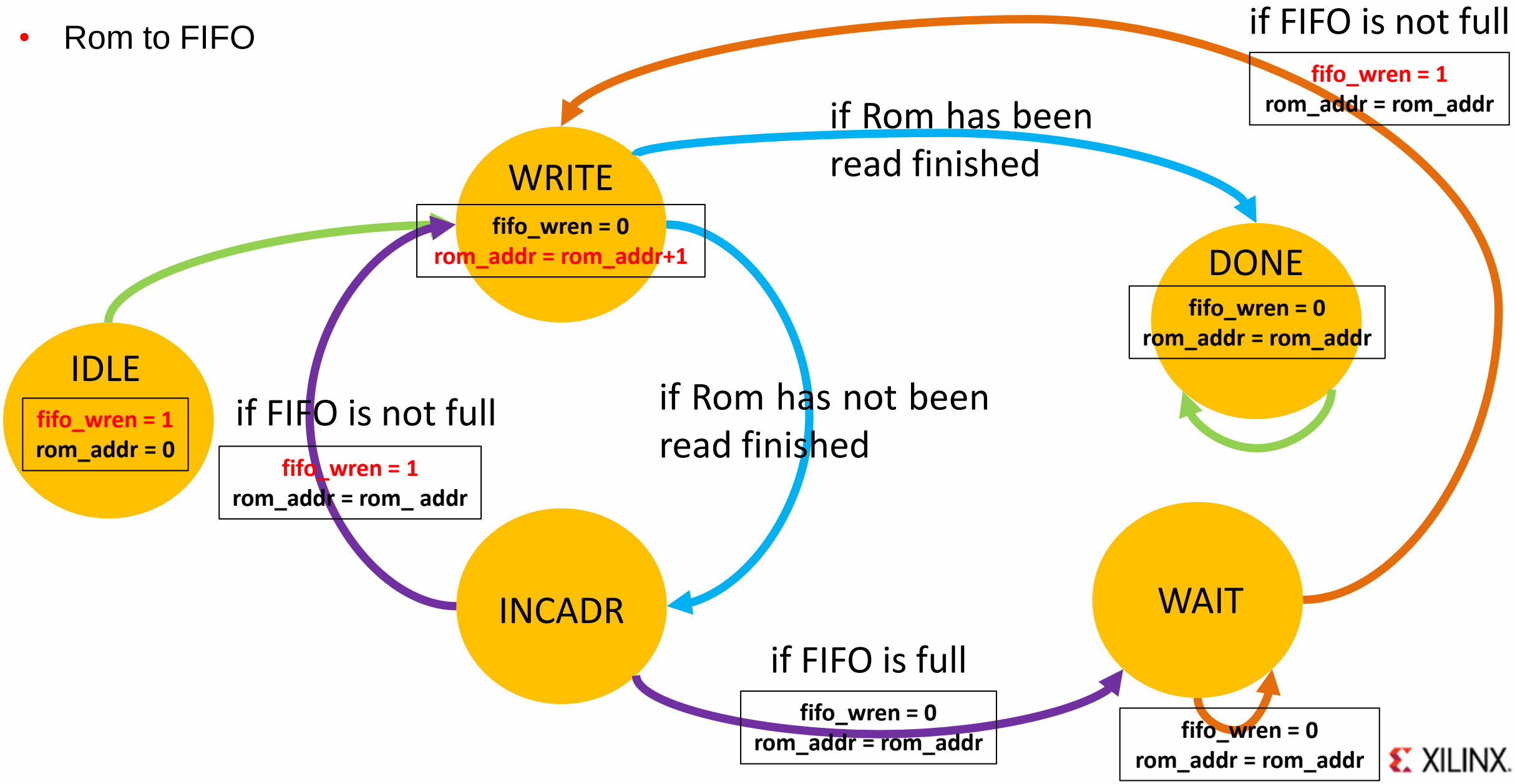
XILINX.

Appendix

XILINX.

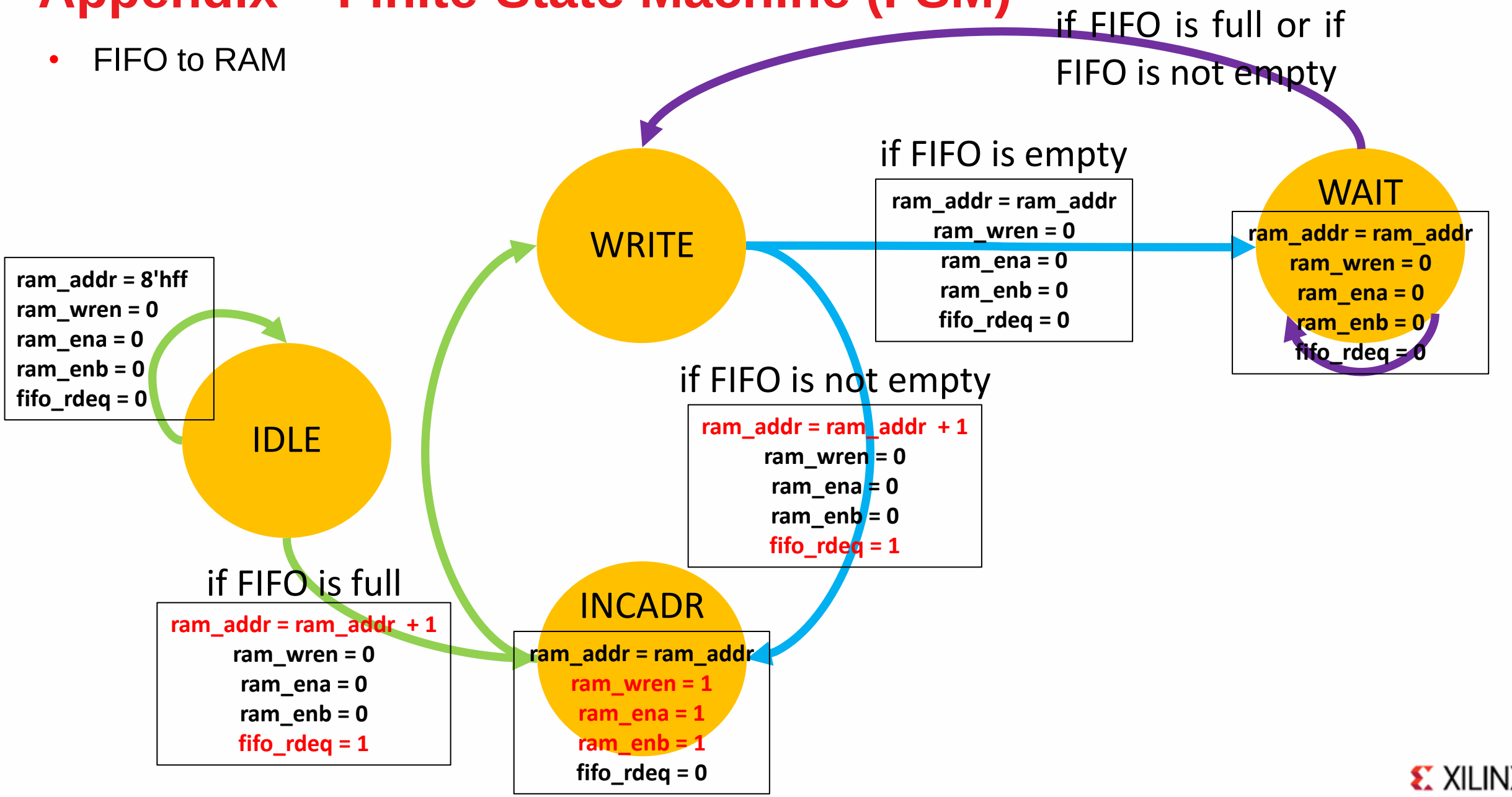
Appendix – Finite-State Machine (FSM)

- Rom to FIFO

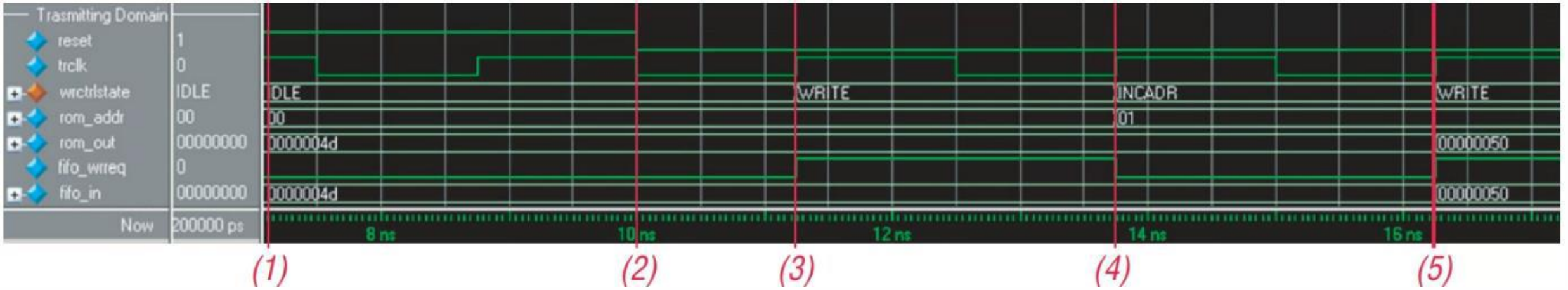


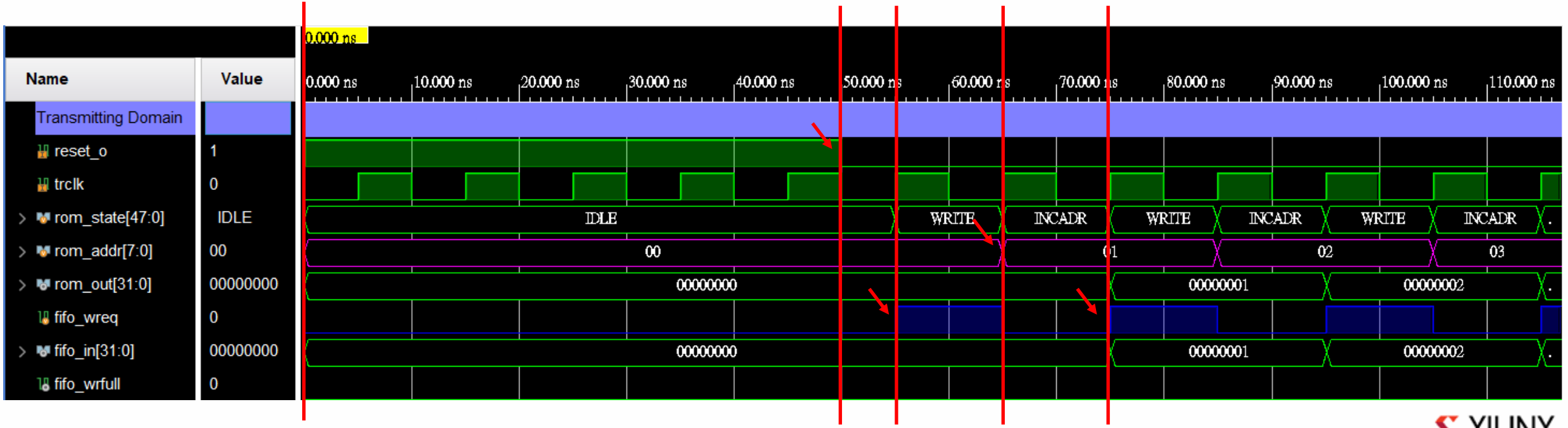
Appendix – Finite-State Machine (FSM)

- FIFO to RAM



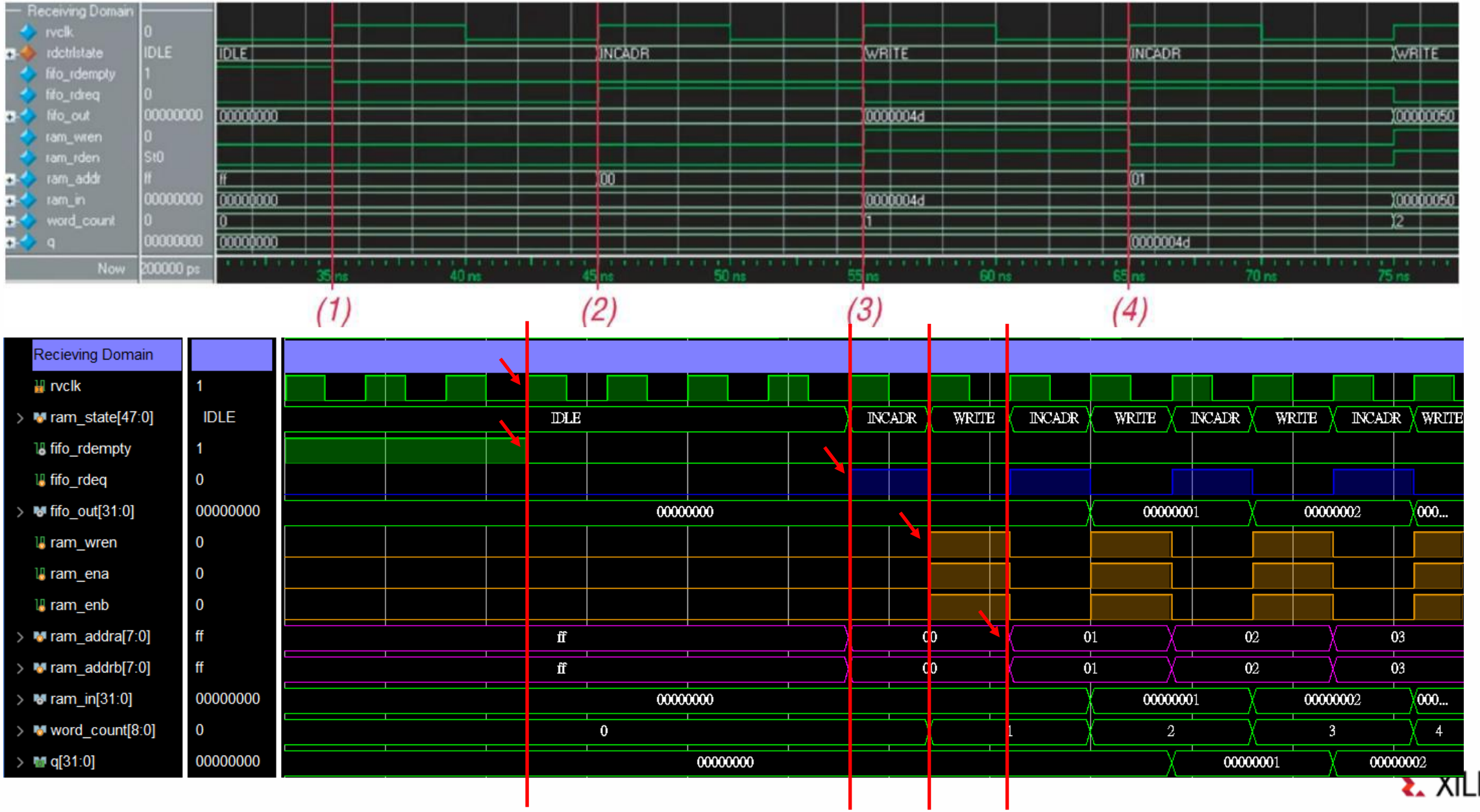
Appendix – Transmitting Domain



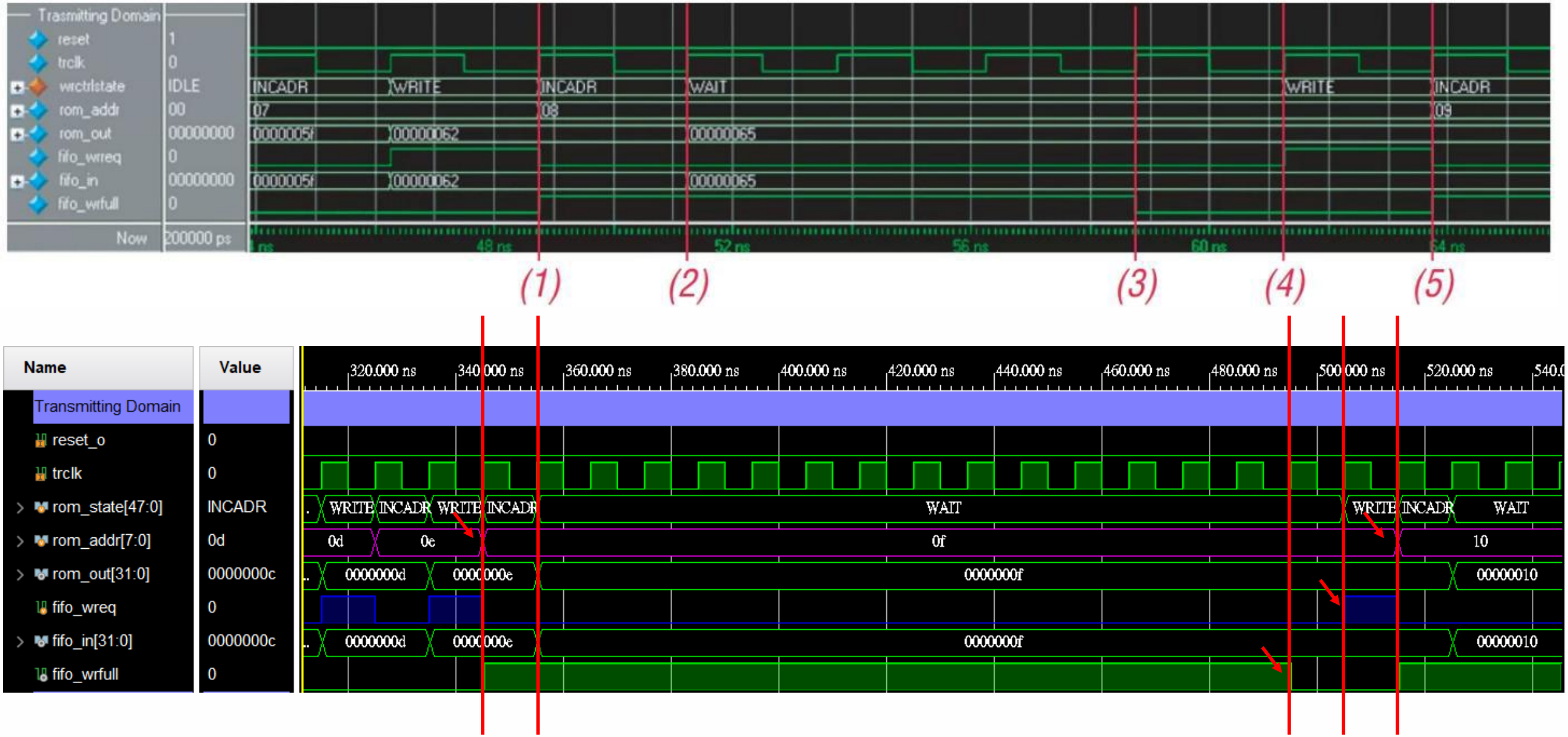


XILINX.

Appendix – Receiving Domain

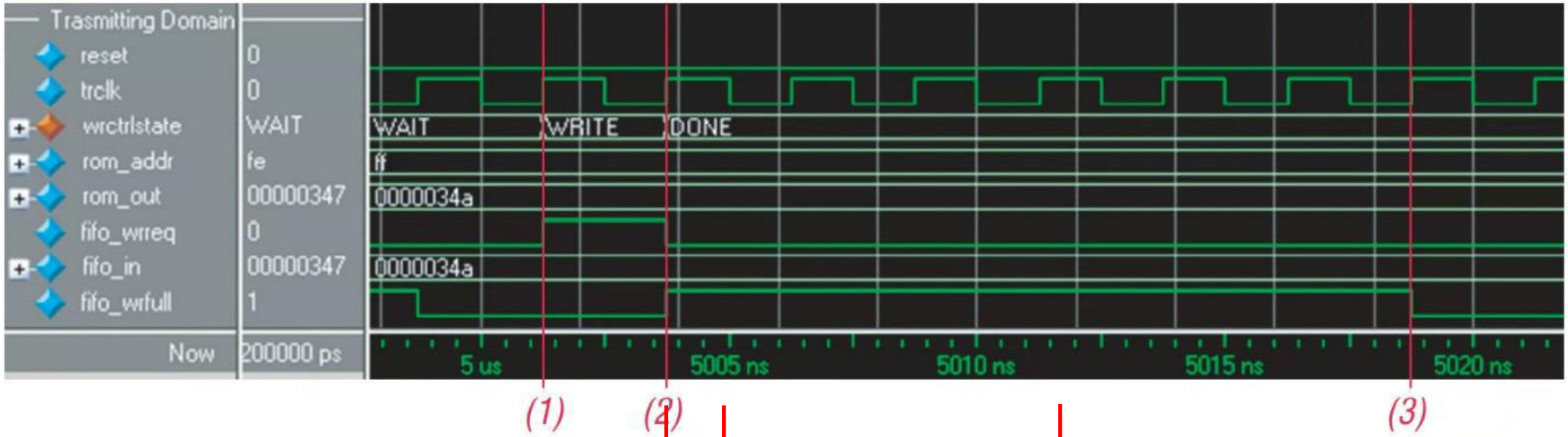


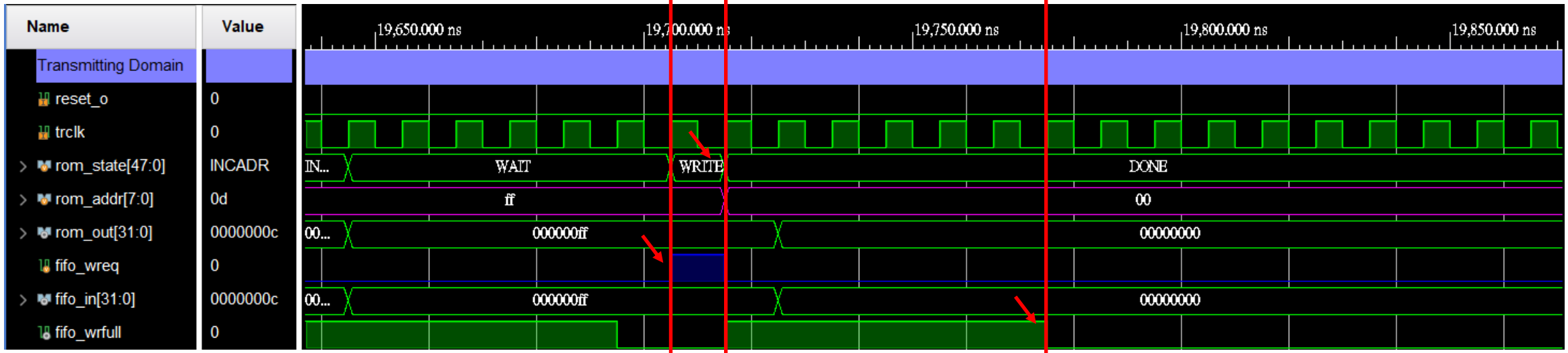
Appendix – When FIFO is full



XILINX.

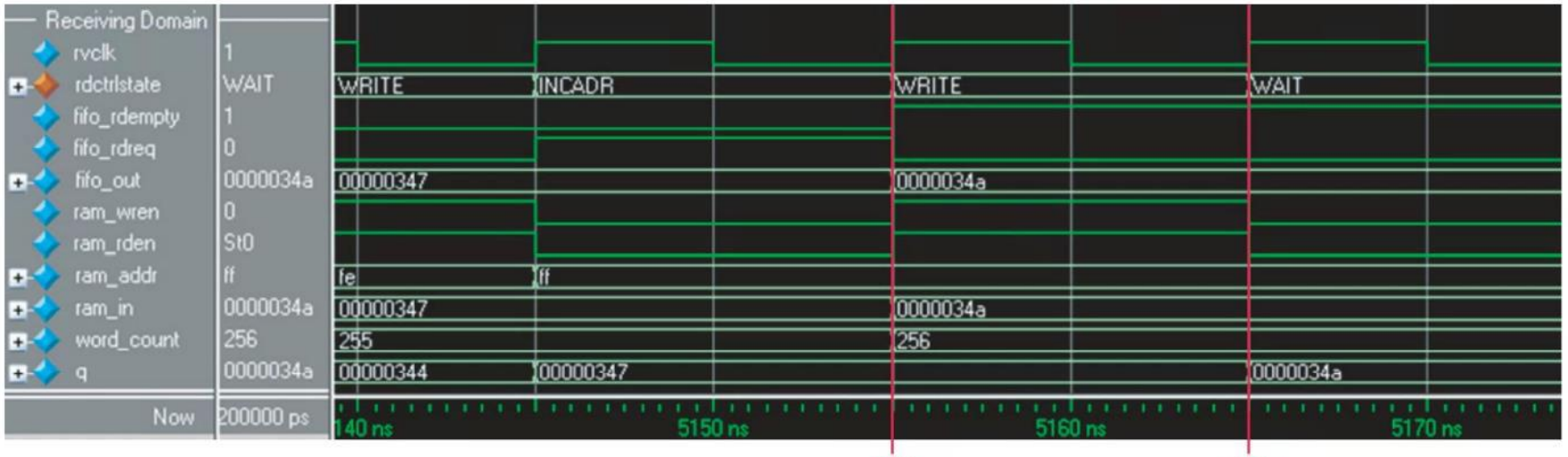
Appendix – completion of ROM to FIFO

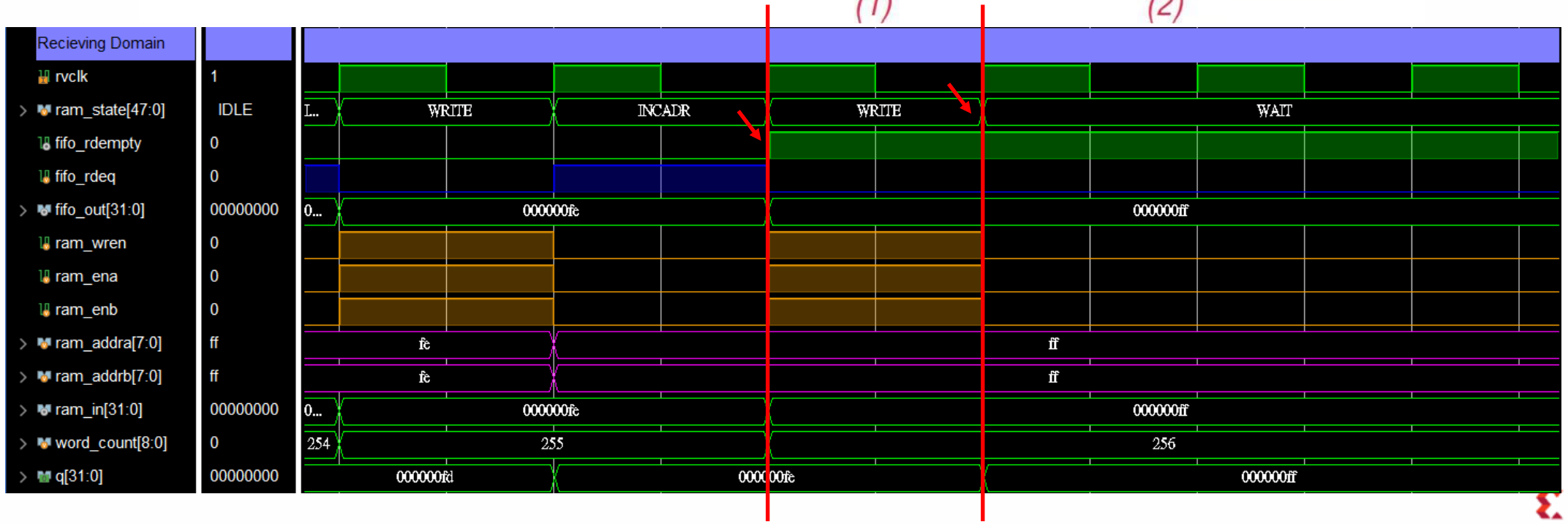




XILINX.

Appendix – completion of FIFO to RAM

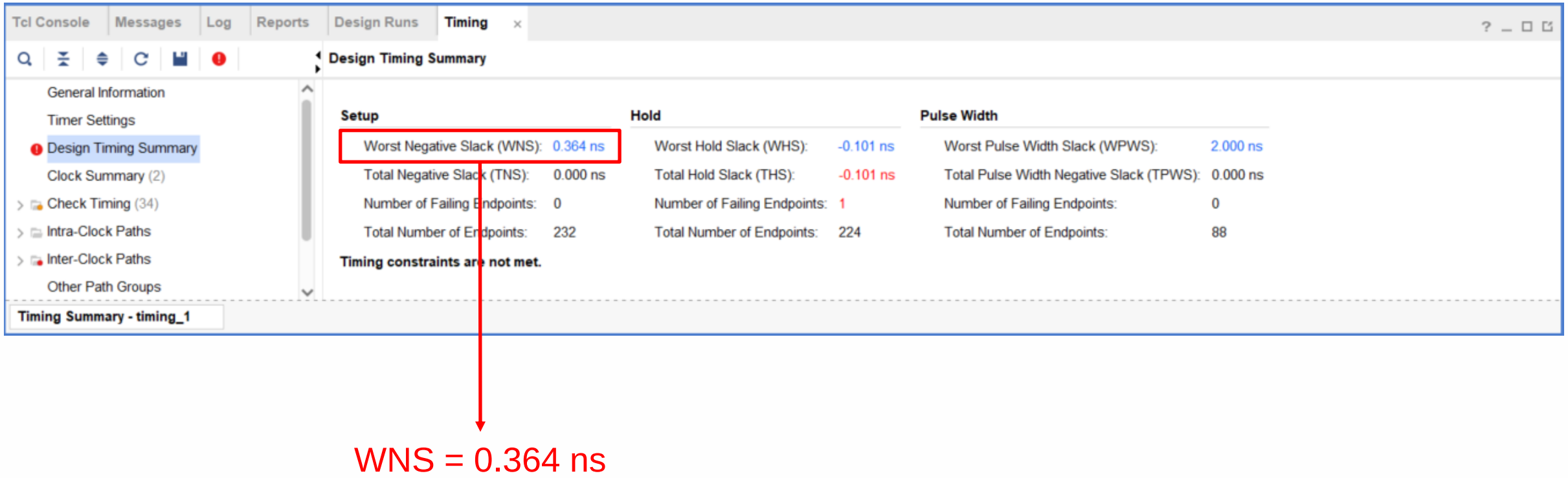




XILINX.

Results of Synthesis

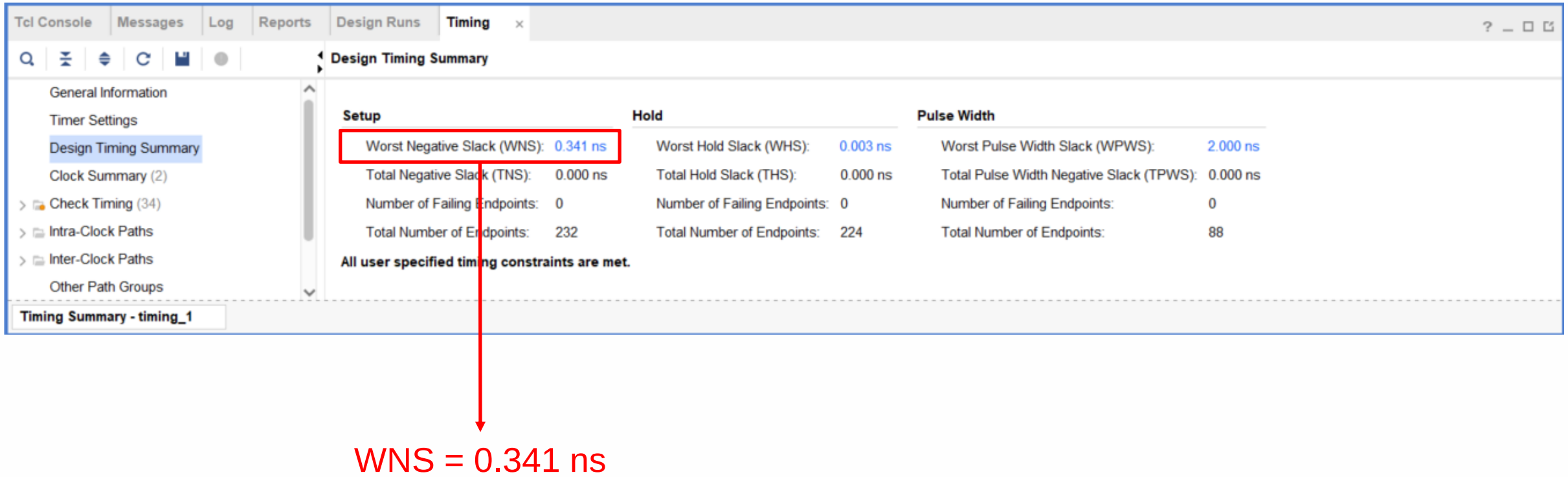
- fsm_extraction: auto



WNS = 0.364 ns

Results of Synthesis

- fsm_extraction: gray



WNS = 0.341 ns