

NOTES: (UNLESS OTHERWISE SPECIFIED)
THIS FAB SHOULD BE "ROHS COMPLIANT".

1. FABRICATE TO IPC-A-600, CURRENT REVISION

2. BOARD SHALL MEET THE INSPECTION CRITERIA OF
a- ACCEPTABILITY AS PER IPC-A-600 (LATEST REVISION) CLASS II
b- QUALIFICATION AND PERFORMANCE AS PER IPC-6012 (LATEST REVISION) CLASS II.

3. MATERIAL MEGTRONIC NCFP (ROHS COMPLIANT MATERIAL OR EQUIVALENT, GLASS
THE BOARD DESIGN IS NOT MEANT TO BE PREPARED FOR LEAD FREE AND
WITH HIGH TEMPERATURE PROCESS ASSOCIATED WITH LEAD FREE ASSEMBLY.

4. APPLY SOLDER MASK OVER BARE COPPER (SMOBC) IAW
IPC-SM-840, BOTH SIDES, USING LPI, COLOR GREEN.

5. LPI SOLDER MASK TAIYO PSR4000 (ROHS COMPLIANT MATERIAL) OR EQUIVALENT WILL BE USED ON BOTH
SIDES.

6. SOLDER MASK REQUIREMENTS FOR VIAS:

a) VIA DRILLS TENTED (COVERED) FROM TOP SIDE AND ENCRACED WITH SOLDER MASK RELIEF OF DRILL
PLUS 6MIL FROM BOTTOM.

b) PLUG TENTED VIA DRILLS FROM TOP SIDE ONLY AND FOLLOW GERBER FOR REST.

c) VIAS SHOWN IN DATA COVERED WITH SOLDER MASK ON BOTH SIDES SHALL BE PRE-PLUGGED WITH NON CONDUCTIVE EPOXY
(MAX HEIGHT NOT TO EXCEED 0.0025") AND COVERED WITH SOLDER MASK.

7. SOLDER MASK REGISTRATION TO BE WITHIN DIAMETRICAL TRUE POSITION OF + / - 0.002" WITH APPLICABLE
HOLE / PAD.

8. FINISH: GOLD IMMERSION.

HARD GOLD ON FINGERS, 30-50 MICRO INCHES OF GOLD OVER 150-200 MICRO INCHES OF NICKEL MINIMUM.

9. SILKSCREEN USING WHITE - HAVEN PC421 (NON-CONDUCTIVE OR EQUIVALENT ROHS COMPLIANT MATERIAL)
BOTH SIDES DISTORTION OF SILKSCREEN IS ACCEPTABLE OVER TRACES. EPOXY INK ON SOLDER LANDS IS
NOT ACCEPTABLE.

10. VENDOR LOGO AND DATE CODE TO BE MARKED SOLDER SIDE IN SILKSCREEN. MAXIMUM HEIGHT 0.12 INCHES.

11. 100% ELECTRICAL TEST REQUIRED FOR CONTINUITY. BOARD SHALL HAVE A
UL-RATING OF 94V-0. UL SYMBOL AND RATING SHALL BE MARKED SOLDER SIDE IN SILKSCREEN.

12. REMOVE ALL UNUSED PADS FROM INTERNAL LAYERS.

13. 274X GERBER/CDB+ USED FOR FAB MUST BE VERIFIED AGAINST THE PROVIDED IPC356 NETLIST. COPPER
SLIVERS THAT ARE LESS THAN .030" IN WIDTH BETWEEN ANTI-EDGE ANTI-PAD AND SPLIT
PLANE AND ANTI-EDGE ANTI-PAD MUST REMAIN. MANUFACTURING WORKS NETLIST
COMPARISON MUST BE PASSED WITH NO VIOLATION AFTER THE REMOVAL OF SLIVERS. ANY REQUIREMENT
FOR SLIVER REMOVAL ABOVE OR EQUAL TO THE 0.003" COPPER WIDTH MUST BE ADDRESSED AND APPROVED
IN WRITING BY SUPPLIER.

14. VIAS ARE SUPPOSED TO BE DIRECTLY CONNECTED TO RESPECTIVE PLANE.

15. ALL VIA IN PAD (10.0 AND 12.0 DRILLS) TO BE COMPLETELY FILLED.
PLANARIZED SMOOTH AND PLATED OVER ON SURFACE. USE SAME NON-CONDUCTIVE EPOXY OR
EQUIVALENT FILL MATERIALS. MINIMUM OF .0007 TO BE PLATED ON SURFACE.
VIA IN PAD MUST INCLUDE WRAP REQUIREMENTS PER IPC 6012B.

16. FOR IMPEDANCE CONTROL DETAILS REFER TO THE FILE HW-U1-KCU116_rev1.0_stackup.pdf

07. INTENTIONAL SHORT: HW-U1-KCU116_REV1.0_SHORTS.TXT

- * SURFACE - AIR 0 MIL
- * DIELECTRIC - CONFORMAL COAT 0.8 MIL
- L1: TOP CONDUCTOR - 050Z_COPPER 1.6 MIL
- * DIELECTRIC - MEG6_PREG_1078HRC 3.4 MIL
- L2: 02 GND1 PLANE - 050Z HVLP CU 0.6 MIL
- * DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
- L3: 03 SIG1 CONDUCTOR - 050Z HVLP CU 0.6 MIL
- * DIELECTRIC - MEG6_PREG_1078(72) 3.4 MIL
- L4: 04 GND2 PLANE - 050Z HVLP CU 0.6 MIL
- * DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
- L5: 05 SIG2 CONDUCTOR - 050Z HVLP CU 0.6 MIL
- * DIELECTRIC - MEG6_PREG_1078(72) 3.4 MIL
- L6: 06 GND3 PLANE - 050Z COPPER 0.6 MIL
- * DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
- L7: 07_PWR1 PLANE - 10Z_COPPER 1.2 MIL
- * DIELECTRIC - MEG6_PREG_1078(72) 3.4 MIL
- L8: 08_PWR2 PLANE - 10Z_COPPER 1.2 MIL
- * DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
- L9: 09_PWR3 PLANE - 10Z_COPPER 1.2 MIL
- * DIELECTRIC - MEG6_PREG_1078(72) 3.4 MIL
- L10: 10_PWR4 PLANE - 10Z_COPPER 1.2 MIL
- * DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
- L11: 11_GND4 PLANE - 050Z_COPPER 0.6 MIL
- * DIELECTRIC - MEG6_PREG_1078(72) 3.4 MIL
- L12: 12 SIG3 CONDUCTOR - 050Z HVLP CU 0.6 MIL
- * DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
- L13: 13_GND5 PLANE - 050Z HVLP CU 0.6 MIL
- * DIELECTRIC - MEG6_PREG_1078(72) 3.4 MIL
- L14: 14 SIG4 CONDUCTOR - 050Z HVLP CU 0.6 MIL
- * DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
- L15: 15_GND6 PLANE - 050Z HVLP CU 0.6 MIL
- * DIELECTRIC - MEG6_PREG_1078HRC 3.4 MIL
- L16: BOTTOM CONDUCTOR - 050Z_COPPER 1.6 MIL
- * DIELECTRIC - CONFORMAL_COAT 0.8 MIL
- * SURFACE - AIR 0 MIL

DESIGN CROSS SECTION CHART

TOTAL THICKNESS 62.0 MILS +/- 5 MILS

SINGLE ENDED	EDGE-COUPLED DIFFERENTIAL		DIFFERENTIAL(Neck Down)	
	TRACEWIDTH	GAP	TRACEWIDTH/AIRgap	GAP
LAYER 1 Foil	12.5 MIL	34	9.5 MIL/4 MIL	66
	10 MIL	34	9.5 MIL/4 MIL	66
	15 MIL	34	9.5 MIL/5 MIL	85
	20 MIL	34	9.5 MIL/6 MIL	100
	6.5 MIL	16	4.4 MIL/2.6 MIL	100
LAYER 3	7.2 MIL	34	9.5 MIL/5 MIL	76
	6.5 MIL	34	9.5 MIL/5 MIL	86
	4 MIL	34	4.5 MIL/5.5 MIL	85
	3.75MIL	50	4.5 MIL/5.5 MIL	100
	6 MIL	34	4.5 MIL/5.5 MIL	90
LAYER 5	7.2 MIL	34	7 MIL/5 MIL	66
	6.5 MIL	34	8.5 MIL/5 MIL	86
	4 MIL	34	4.4 MIL/4.8 MIL	85
	3.75MIL	50	4.5 MIL/5.5 MIL	100
LAYER 12	7.2 MIL	34	7 MIL/5 MIL	66
	6.5 MIL	34	8.5 MIL/5 MIL	86
	4 MIL	34	4.4 MIL/5.5 MIL	85
	3.75MIL	50	4.5 MIL/5.5 MIL	100
LAYER 14	7.2 MIL	34	7 MIL/5 MIL	66
	6.5 MIL	34	8.5 MIL/5 MIL	86
	4 MIL	34	4.4 MIL/5.5 MIL	85
	3.75MIL	50	4.5 MIL/5.5 MIL	100
LAYER 16 Foil	12.5 MIL	34	9.5 MIL/4 MIL	66
	10 MIL	34	9.5 MIL/4 MIL	76
	15 MIL	34	9.5 MIL/5 MIL	85
	20 MIL	34	9.5 MIL/6 MIL	100
	6.5 MIL	39	9.5 MIL/5.5 MIL	90
	5.5 MIL	50	9.5 MIL/5.5 MIL	100

REVISIONS				
REV	DESCRIPTION	DATE	APPROVED	
A	PROTOTYPE	11/30/16		
B	SFP FIXES	12/3/16		
C	SFP SWAPS PCIE SI FIX	02/13/17		
1.0	PRODUCTION RELEASE	04/04/17		

BACKDRILL: BOTTOM to 13 GND5				
ALL UNITS ARE IN MILS				
FIGURE	FHS	TOLERANCE	PLATED	QTY ADDITIONAL
.	10.0	+0.0/-10.0	PLATED	26

TOTAL HOLES: 34				
BACKDRILL: BOTTOM to 06 GND3				
ALL UNITS ARE IN MILS				

FIGURE	FHS	TOLERANCE	PLATED	QTY ADDITIONAL
.	10.0	+0.0/-10.0	PLATED	16

TOTAL HOLES: 16				
BACKDRILL: BOTTOM to 04 GND2				
ALL UNITS ARE IN MILS				

FIGURE	FHS	TOLERANCE	PLATED	QTY ADDITIONAL
.	10.0	+0.0/-10.0	PLATED	16

TOTAL HOLES: 18				
DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				

FIGURE	FHS	TOLERANCE	PLATED	QTY ADDITIONAL
.	8.0	+0.0/-8.0	PLATED	530
.	10.0	+0.0/-10.0	PLATED	3672
.	12.0	+0.0/-12.0	PLATED	665
.	32.0	+3.0/-3.0	PLATED	4
.	36.0	+2.0/-4.0	PLATED	12
▲	37.4	+2.0/-2.0	PLATED	20 PRESS FIT
▲	40.0	+3.0/-3.0	PLATED	117
■	40.0	+4.0/-2.0	PLATED	4
■	41.3	+2.0/-2.0	PLATED	14 PRESS FIT
●	46.0	+1.0/-3.0	PLATED	12
●	48.0	+3.0/-3.0	PLATED	6
◎	62.0	+3.0/-3.0	PLATED	2
●	63.0	+3.0/-3.		

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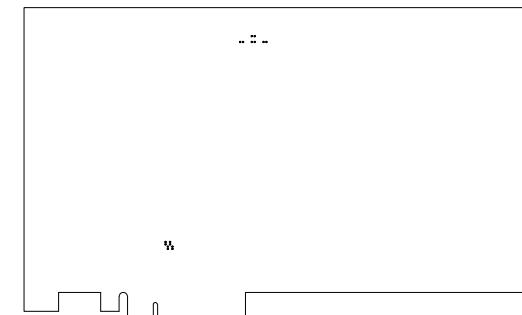
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BACKDRILL: BOTTOM to Q4 GND2					
ALL UNITS ARE IN MILS					
FIGURE	FHS	TOLERANCE	PLATED	QTY	ADDITIONAL
*	10.0	+0.0/-10.0	PLATED	16	
TOTAL HOLES: 16					

NOTES:
- DRILL SIZES LISTED IN LEGEND ARE CONSIDERED FINISHED.
- PLEASE USE 15.7 MILS DRILL BIT TOOLING FOR 10 MILS FHS OVERDRILLING.
- LEGEND DOES NOT SPECIFY DEPTH INTO ADJACENT DIELECTRIC LAYER.
- Q3_SIG1 IS MUST NOT CUT LAYER.



UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE	XILINX		
DIMENSIONS ARE IN INCHES	DRAWN Brian Forsse	04-04-17	2100 LOGIC DR.		
TOLERANCES ON;	CHECKED Brian Forsse		SAN JOSE, CA 95124		
2 PL DECIMALS +/- .010	ENGRG Brian Forsse	04-04-17	HWCP - HARDWARE & CONFIGURATION PLATFORMS		
3 PL DECIMALS +/- .005	ISSUED Steve Carey	04-04-17	FABRICATION DRAWING		
ANGLES +			PCB, ROHS COMPLIANT		
FRACTIONS +			HW-U1-KCU116		
			SIZE D	FSCM NO	DWG NO
			SCALE NONE	1280924	
					REV 1.0
					SHEET 2 OF 5

REVISIONS

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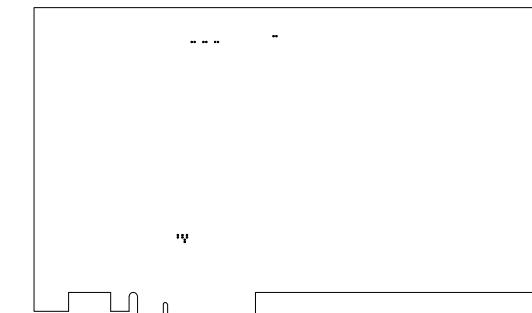
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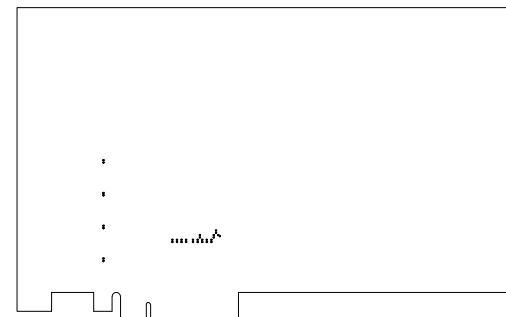
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BACKDRILL: BOTTOM to 06_GND3				
ALL UNITS ARE IN MILS				
FIGURE	FHS	TOLERANCE	PLATED	QTY
.	10.0	+0.0/-10.0	PLATED	16
TOTAL HOLES: 16				

NOTES:
- DRILL SIZES LISTED IN LEGEND ARE CONSIDERED FINISHED.
- PLEASE USE 15.7 MILS DRILL BIT TOOLING FOR 10 MILS FHS OVERRILLING.
- LEGEND DOES NOT SPECIFY DEPTH INTO ADJACENT DIELECTRIC LAYER.
- 05_SIG2 IS MUST NOT CUT LAYER.



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ANGLES +			PCB, ROHS COMPLIANT		
FRACTIONS +			HW-U1-KCU116		
			SIZE	FSCM NO	DWG NO
			D		1280924
	SCALE	NONE			REV
					1.0
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1.0	PRODUCTION RELEASE	04/04/17	

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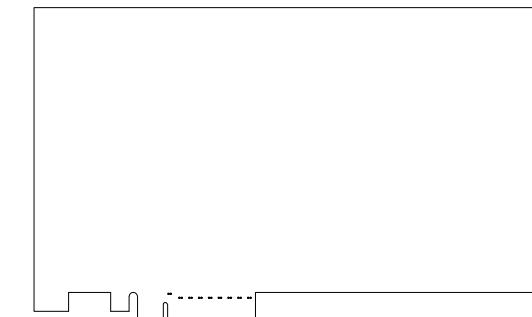
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BACKDRILL: TOP to 11 GND4 ALL UNITS ARE IN MILS					
FIGURE	FHS	TOLERANCE	PLATED	QTY	ADDITIONAL
.	10.0	+0.0/-10.0	PLATED	18	
TOTAL HOLES: 18					

NOTES:

- DRILL SIZES LISTED IN LEGEND ARE CONSIDERED FINISHED.
- PLEASE USE 15.7 MILS DRILL BIT TOOLING FOR 10 MILS FHS OVERDRILLING.
- LEGEND DOES NOT SPECIFY DEPTH INTO ADJACENT DIELECTRIC LAYER.
- 12_SIG3 IS MUST NOT CUT LAYER.

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE	XILINX		
DIMENSIONS ARE IN INCHES	Brian Forse	04-04-17	2100 LOGIC DR. SAN JOSE, CA 95124 HWCP - HARDWARE & CONFIGURATION PLATFORMS		
TOLERANCES ON;	Brian Forse				
2 PL DECIMALS +/- .010	Brian Forse	04-04-17	FABRICATION DRAWING		
3 PL DECIMALS +/- .005	Brian Forse	04-04-17	PCB, ROHS COMPLIANT		
ANGLES +	Steve Carey	04-04-17	HW-U1-KCU116		
FRACTIONS +			SIZE	FSCM NO	DWG NO
			D		1280924
			SCALE	NONE	
					SHEET
					1 . 0
					5 OF 5

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5. LPI SOLDER MASK TAIYO PSR4000 (ROHS COMPLIANT MATERIAL) OR EQUIVALENT WILL BE USED ON BOTH
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HARD GOLD ON PINGERS, 30-50 MICRO INCHES OF GOLD OVER 150-200 MICRO INCHES OF NICKEL MINIMUM.

9. SILKSCREEN USING WHITE - HAVEN PC421 (NON-CONDUCTIVE OR EQUIVALENT ROHS COMPLIANT MATERIAL)
BOTH SIDES DISTORTION OF SILKSCREEN IS ACCEPTABLE OVER TRACES. EPOXY INK ON SOLDER LANDS IS
NOT ACCEPTABLE.

10. VENDOR LOGO AND DATE CODE TO BE MARKED SOLDER SIDE IN SILKSCREEN. MAXIMUM HEIGHT 0.12 INCHES.

11. 100% ELECTRICAL TEST REQUIRED FOR CONTINUITY. BOARD SHALL HAVE A
UL-RATING OF 94V-0. UL SYMBOL AND RATING SHALL BE MARKED SOLDER SIDE IN SILKSCREEN.

12. REMOVE ALL UNUSED PADS FROM INTERNAL LAYERS.

13. 274X GERBER/CDB+ USED FOR FAB MUST BE VERIFIED AGAINST THE PROVIDED IPC356 NETLIST. COPPER
SLIVERS THAT ARE LESS THAN .030" IN WIDTH BETWEEN ANTI-EDGE ANTI-PAD AND THE SPLIT
PAD AND ANTI-PAD NO ANTI-PAD MUST REMAIN. MANUFACTURER (WHO PROVIDED NETLIST)
COMPARISON MUST BE PASSED WITH NO VIOLATION AFTER THE REMOVAL OF SLIVERS. ANY REQUIREMENT
FOR SLIVER REMOVAL ABOVE OR EQUAL TO THE 0.003" COPPER WIDTH MUST BE ADDRESSED AND APPROVED
IN WRITING BY SUPPLIER.

14. VIAS ARE SUPPOSED TO BE DIRECTLY CONNECTED TO RESPECTIVE PLANE.

15. ALL VIA IN PAD (10.0 AND 12.0 DRILLS) TO BE COMPLETELY FILLED.
PLANARIZED SMOOTH AND PLATED OVER ON SURFACE. USE SAME NON-CONDUCTIVE EPOXY OR
EQUIVALENT FILL MATERIALS. MINIMUM OF .0007 TO BE PLATED ON SURFACE.
VIA IN PAD MUST INCLUDE WRAP REQUIREMENTS PER IPC 6012B.

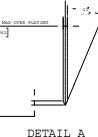
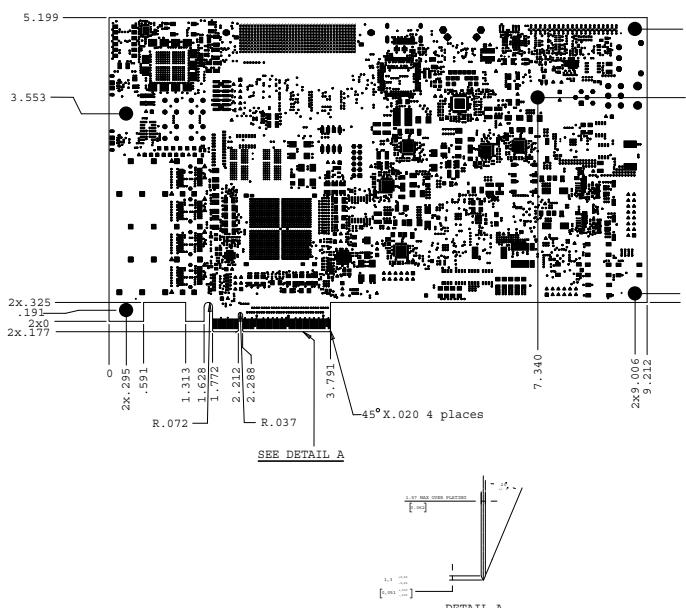
16. FOR IMPEDANCE CONTROL DETAILS REFER TO THE FILE HW-U1-KCU116_rev1.0_stackup.pdf

07. INTENTIONAL SHORT: HW-U1-KCU116_REV1.0_SHORTS.TXT

1-16	* SURFACE - AIR 0 MIL
	* DIELECTRIC - CONFORMAL COAT 0.8 MIL
L1:	TOP CONDUCTOR - 050Z_COPPER 1.6 MIL
	* DIELECTRIC - MEG6_PREG_1078HRC 3.4 MIL
L2:	02 GND1 PLANE - 050Z HVLP CU 0.6 MIL
	* DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
L3:	03 SIG1 CONDUCTOR - 050Z HVLP CU 0.6 MIL
	* DIELECTRIC - MEG6_PREG_1078(72) 3.4 MIL
L4:	04 GND2 PLANE - 050Z HVLP CU 0.6 MIL
	* DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
L5:	05 SIG2 CONDUCTOR - 050Z HVLP CU 0.6 MIL
	* DIELECTRIC - MEG6_PREG_1078(72) 3.4 MIL
L6:	06 GND3 PLANE - 050Z COPPER 0.6 MIL
	* DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
L7:	07_PWR1 PLANE - 10Z_COPPER 1.2 MIL
	* DIELECTRIC - MEG6_PREG_1078(72) 3.4 MIL
L8:	08_PWR2 PLANE - 10Z_COPPER 1.2 MIL
	* DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
L9:	09_PWR3 PLANE - 10Z_COPPER 1.2 MIL
	* DIELECTRIC - MEG6_PREG_1078(72) 3.4 MIL
L10:	10_PWR4 PLANE - 10Z_COPPER 1.2 MIL
	* DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
L11:	11_GND4 PLANE - 050Z_COPPER 0.6 MIL
	* DIELECTRIC - MEG6_PREG_1078(72) 3.4 MIL
L12:	12 SIG3 CONDUCTOR - 050Z HVLP CU 0.6 MIL
	* DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
L13:	13_GND5 PLANE - 050Z HVLP CU 0.6 MIL
	* DIELECTRIC - MEG6_PREG_1078(72) 3.4 MIL
L14:	14 SIG4 CONDUCTOR - 050Z HVLP CU 0.6 MIL
	* DIELECTRIC - MEG6_CORE_1=1078 2.9 MIL
L15:	15_GND6 PLANE - 050Z HVLP CU 0.6 MIL
	* DIELECTRIC - MEG6_PREG_1078HRC 3.4 MIL
L16:	BOTTOM CONDUCTOR - 050Z_COPPER 1.6 MIL
	* DIELECTRIC - CONFORMAL_COAT 0.8 MIL
	* SURFACE - AIR 0 MIL

DESIGN CROSS SECTION CHART

TOTAL THICKNESS 62.0 MILS +/- 5 MILS



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A	PROTOTYPE	11/30/16	
B	SFP FIXES	12/3/16	
C	SFP SWAPS PCIE SI FIX	02/13/17	
1.0	PRODUCTION RELEASE	04/04/17	

DRILL CHART: TOP to BOTTOM					
ALL LINES ARE IN MILS					
FIGURE	FHS	TOLERANCE	PLATED	QTY	ADDITIONAL
.	8.0	+0.0/-8.0	PLATED	530	
.	10.0	+0.0/-10.0	PLATED	3672	
.	12.0	+0.0/-12.0	PLATED	665	
■	32.0	+3.0/-3.0	PLATED	4	
■	36.0	+2.0/-4.0	PLATED	12	
▲	37.4	+2.0/-2.0	PLATED	20	PRESS FIT
▲	40.0	+3.0/-3.0	PLATED	117	
■	40.0	+4.0/-2.0	PLATED	4	
■	41.3	+2.0/-2.0	PLATED	14	PRESS FIT
●	46.0	+1.0/-3.0	PLATED	12	
●	48.0	+3.0/-3.0	PLATED	6	
◎	62.0	+3.0/-3.0	PLATED	2	
●	63.0	+3.0/-3.0	PLATED	16	
●	71.0	+3.0/-3.0	PLATED	6	
●	73.0	+3.0/-3.0	PLATED	5	
■	106.0	+3.0/-3.0	PLATED	2	
■	125.0	+3.0/-3.0	PLATED	7	
■	33.0	+2.0/-2.0	NON-PLATED	2	
■	40.0	+2.0/-2.0	NON-PLATED	2	
■	50.0	+2.0/-2.0	NON-PLATED	2	
●	61.0	+2.0/-2.0	NON-PLATED	8	
■	63.0	+2.0/-2.0	NON-PLATED	4	
◆	127.0	+2.0/-4.0	NON-PLATED	2	
■	33.0x26.0	+3.0/-3.0	PLATED	4	
■	60.0x32.0	+3.0/-3.0	PLATED	4	
■	67.0x35.0	+2.0/-2.0	PLATED	2	
■	106.0x35.0	+2.0/-2.0	PLATED	2	

TOTAL HOLES: 5126

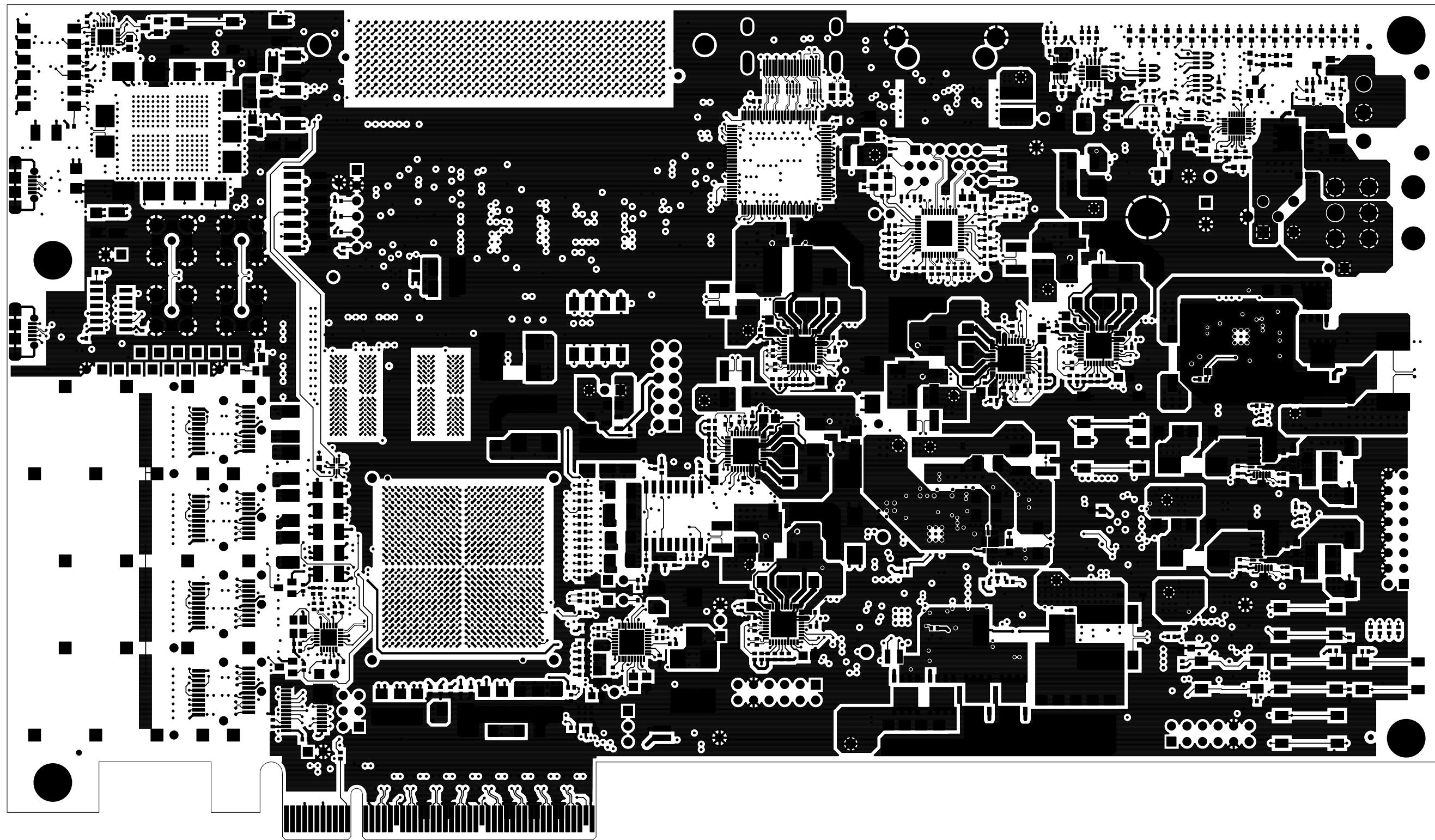
UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE
DIMENSIONS ARE IN INCHES	Brian Forsse	04-04-17
TOLERANCES ON;		
2 PL DECIMALS +/- .010		
3 PL DECIMALS +/- .005		
ANGLES +		
FRACTIONS +		
ISSUED	Steve Carey	04-04-17
FABRICATION DRAWING		
SIZE	FSMC NO	DWG NO
D		1280924
SCALE	NONE	REV
		1.0
		1 OF 5

XILINX

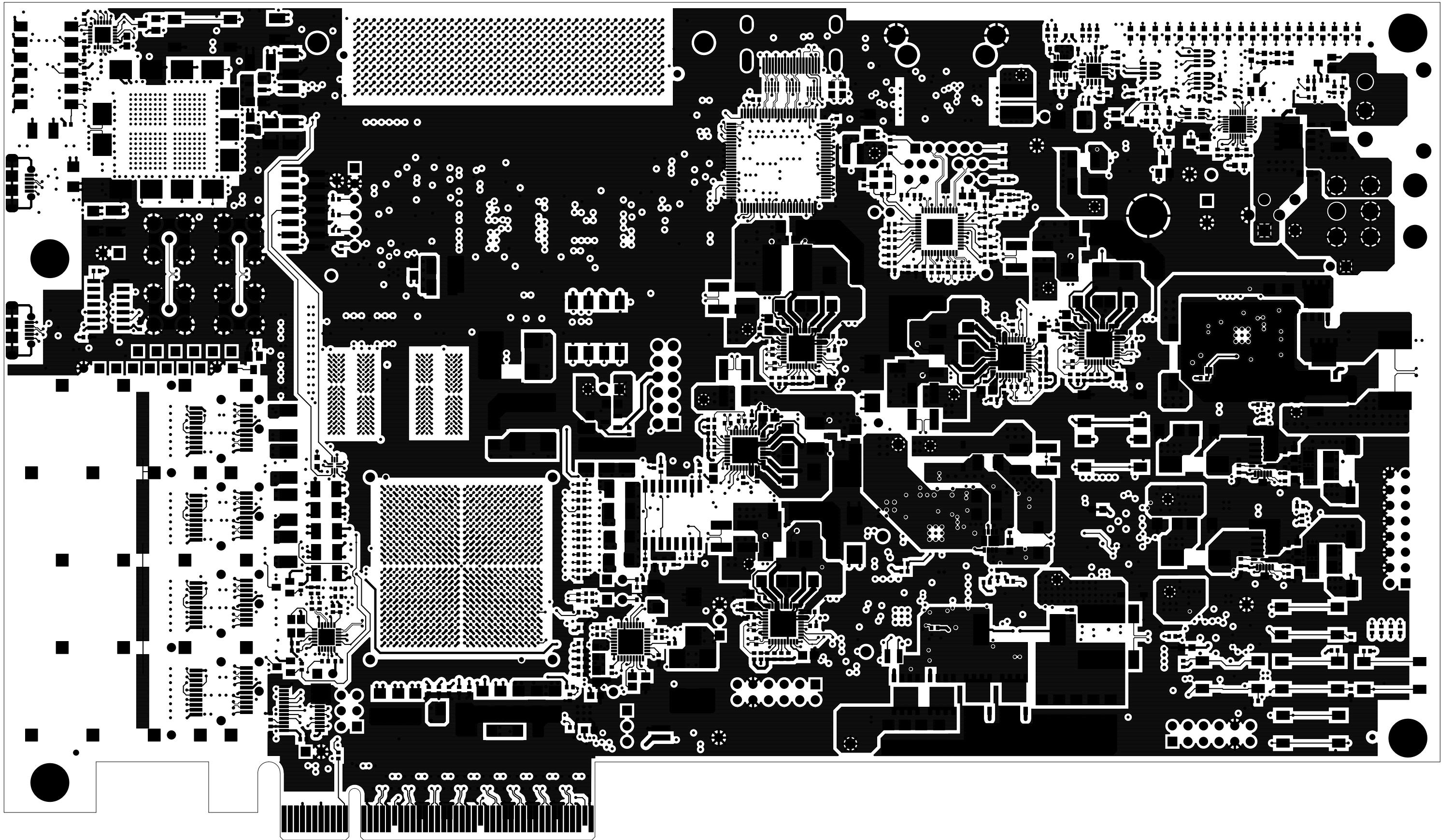
2100 LOGIC DR.
SAN JOSE, CA 95124
HWCP - HARDWARE & CONFIGURATION PLATFORMS

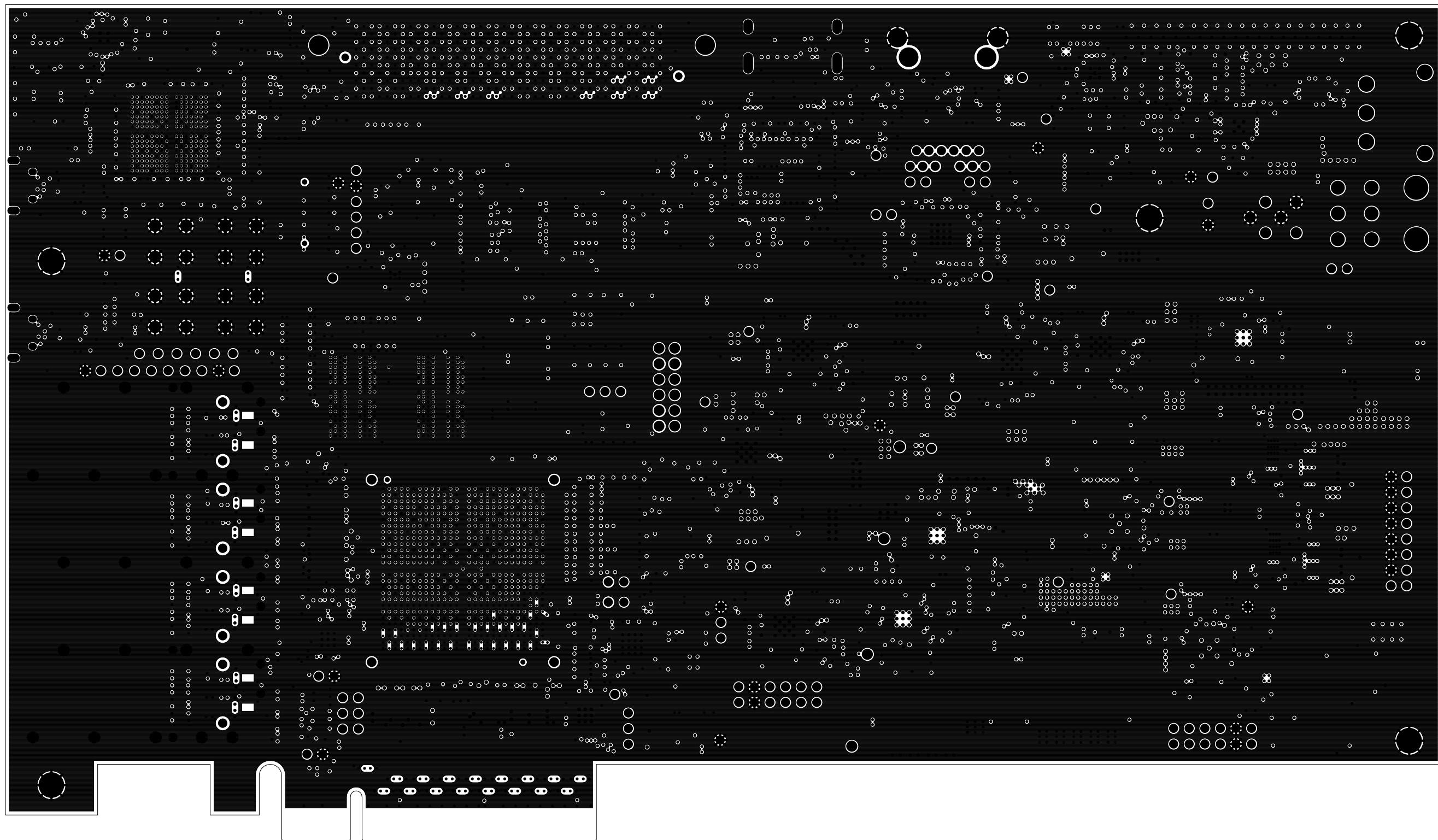
HW-U1-KCU116
PCB, ROHS COMPLIANT



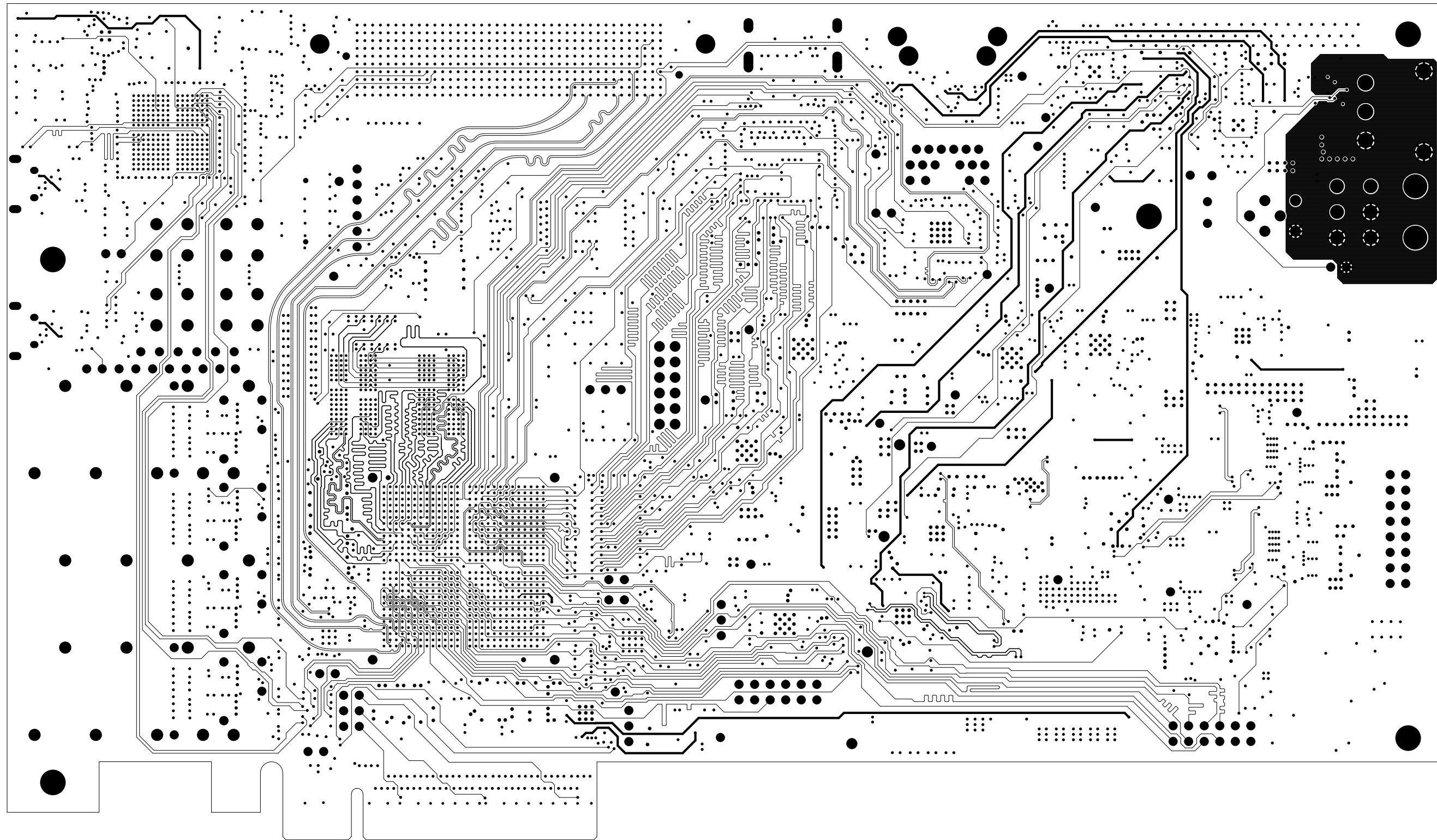


Layer: TOP	Sheet: 01 of: 22
Layout Engineer: SCAREY	Company Name: XILINX
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116
Whizz Job Number: 04-04-17	Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:	LATEST MECHANICAL REV OR DATE:

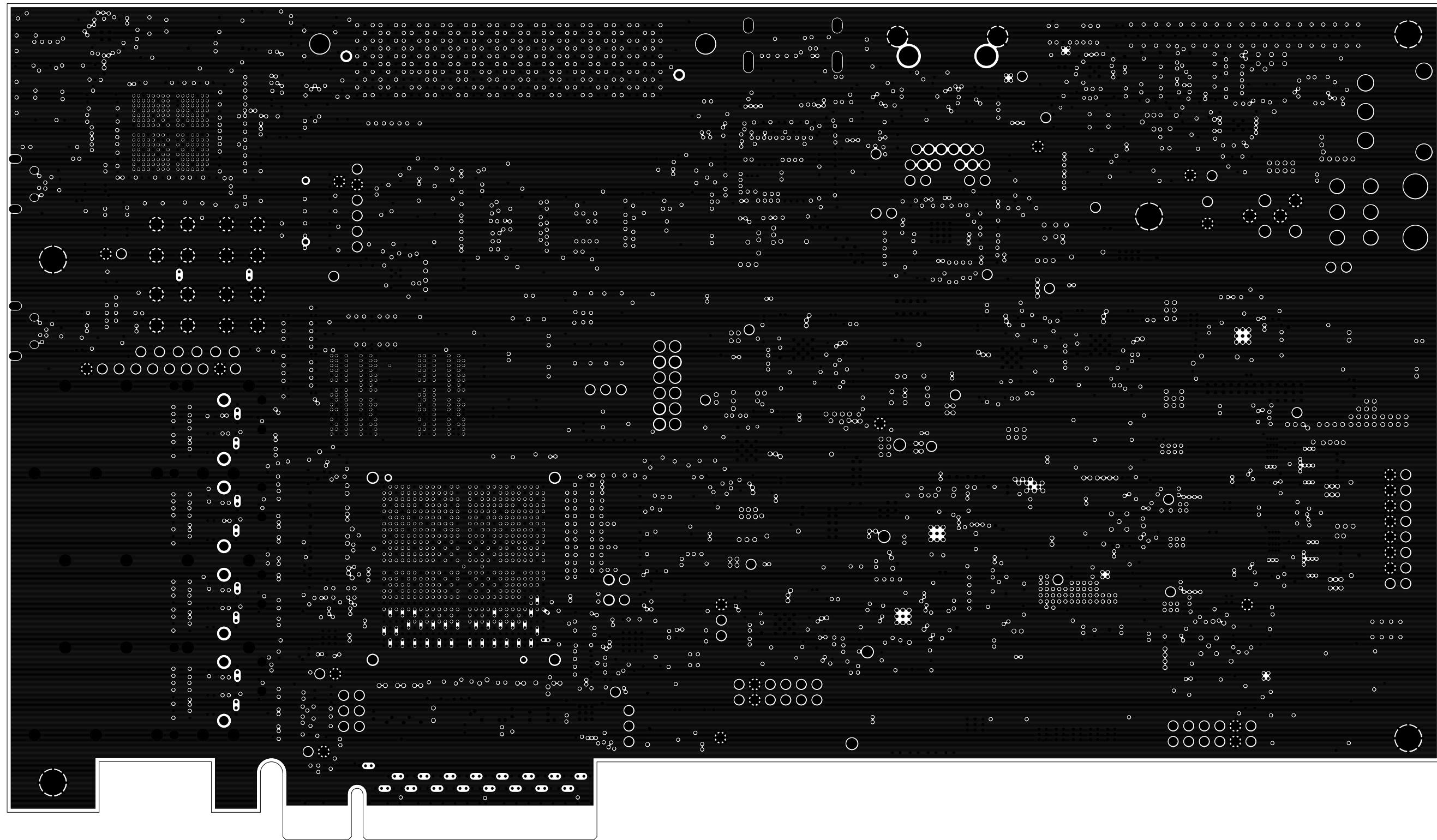




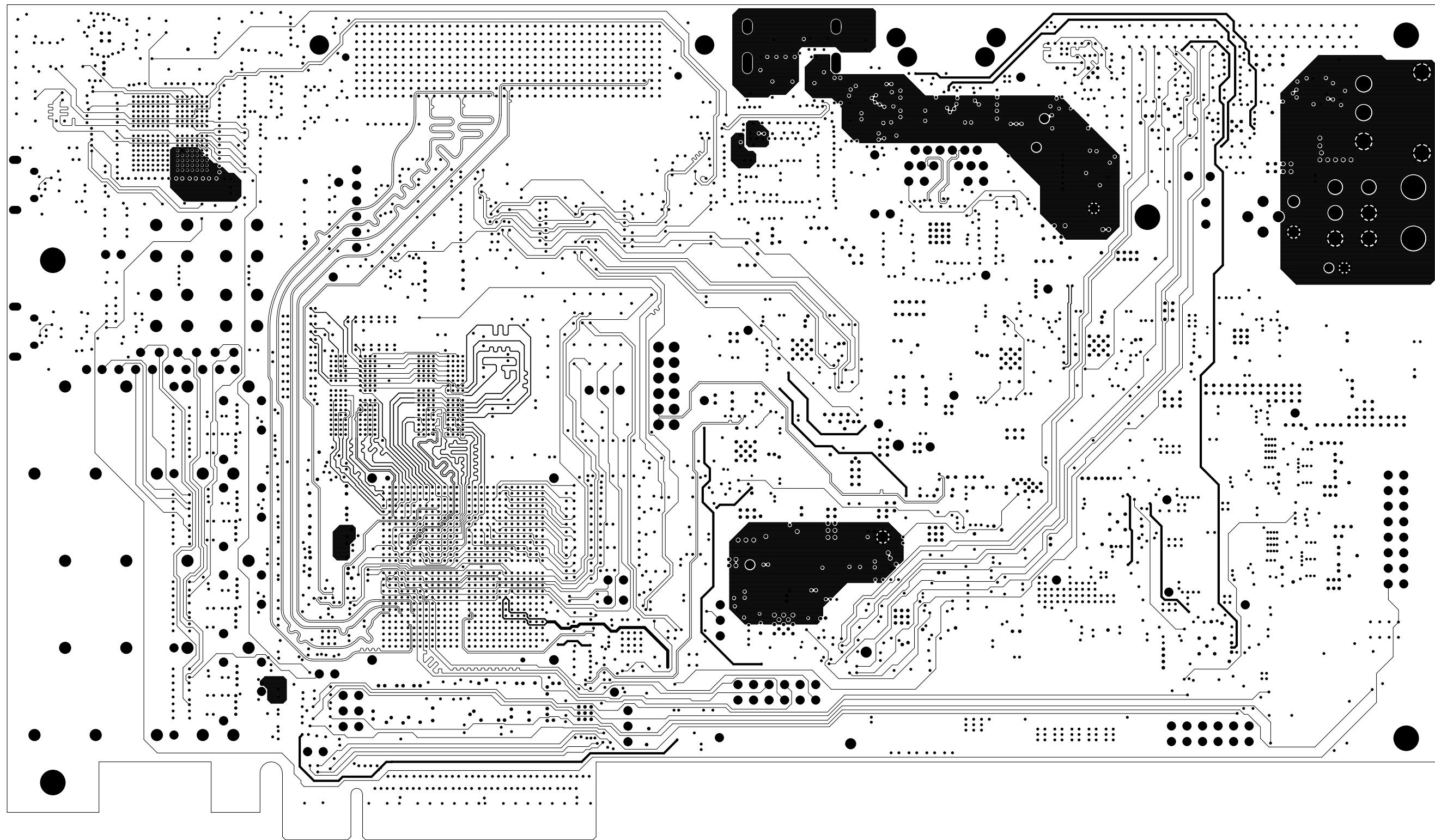
Layer: 02_GND1	Sheet: 02 of: 22	
Layout Engineer: SCAREY	Company Name: XILINX	
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116	
Whizz Job Number: 04-04-17	Date: 04-04-17	Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:



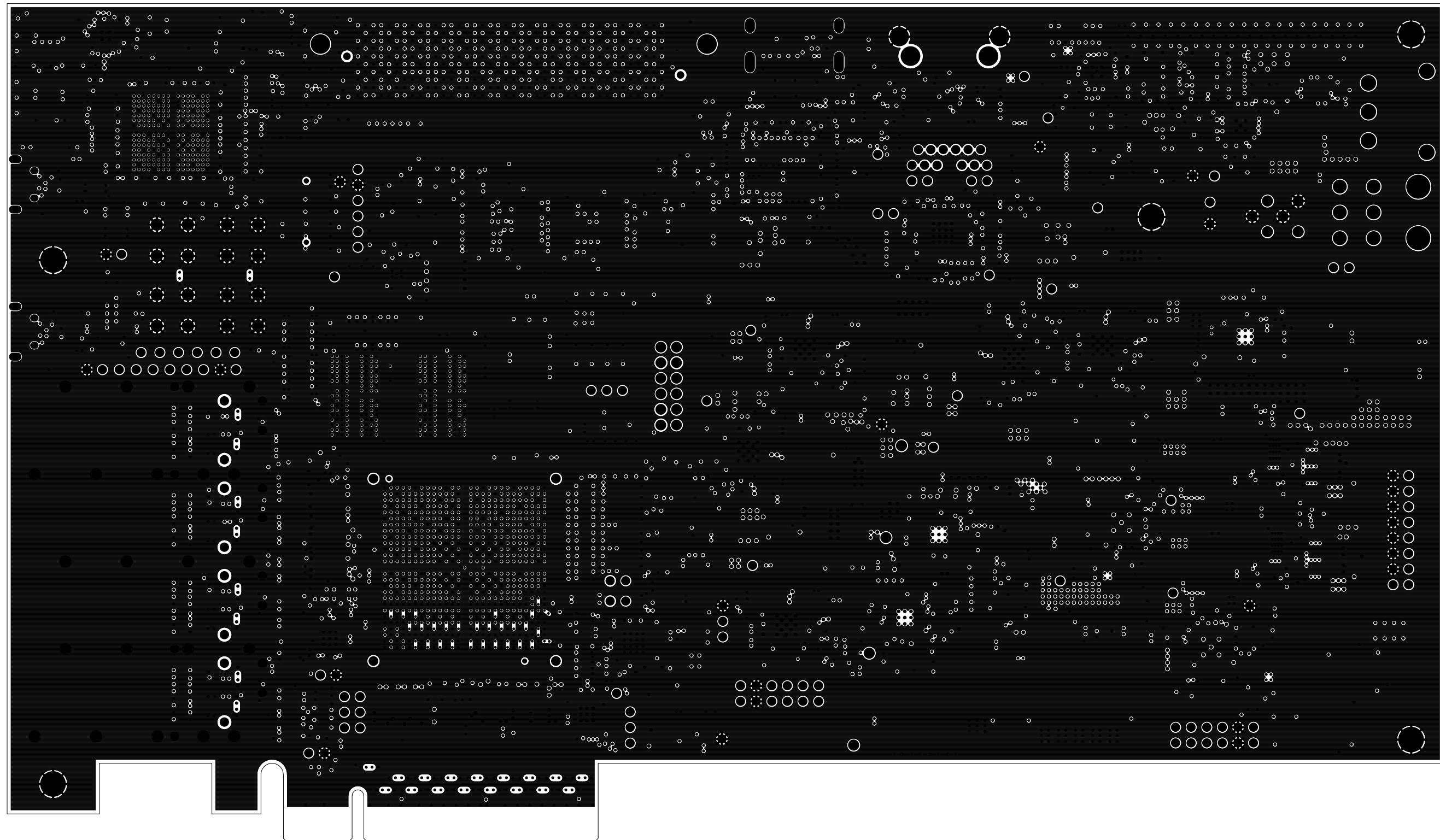
Layer: 03_SIG1	Sheet: 03 of: 22	
Layout Engineer: SCAREY	Company Name: XILINX	
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116	
Whizz Job Number: 04-04-17	Date: 04-04-17	Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:



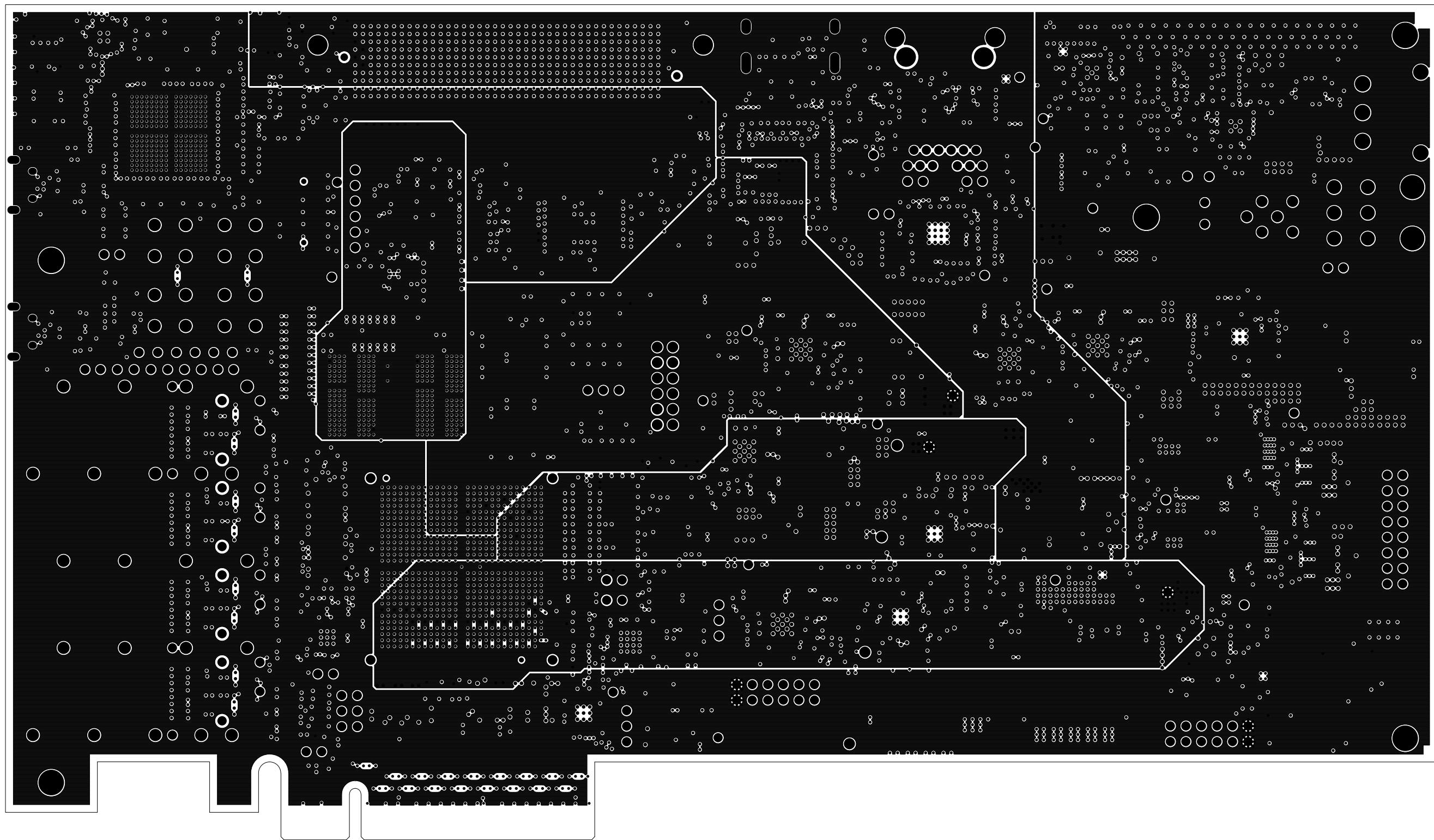
Layer: 04_GND2	Sheet: 04 of: 22	
Layout Engineer: SCAREY	Company Name: XILINX	
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116	
Whizz Job Number: 04-04-17	Date: 04-04-17	Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:



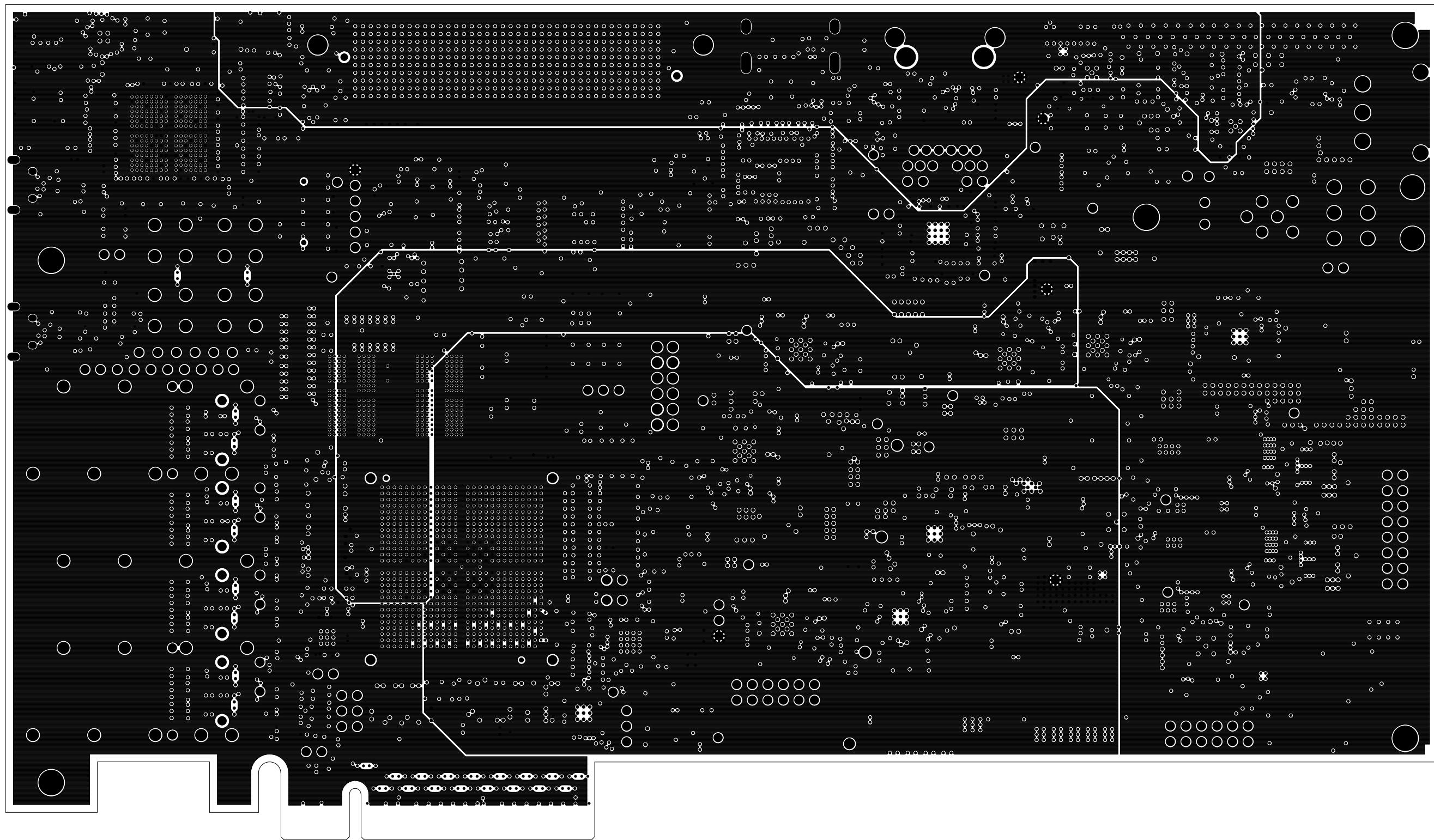
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Layout Engineer: SCAREY	Company Name: XILINX	
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116	
Whizz Job Number: 04-04-17	Date: 04-04-17	Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:



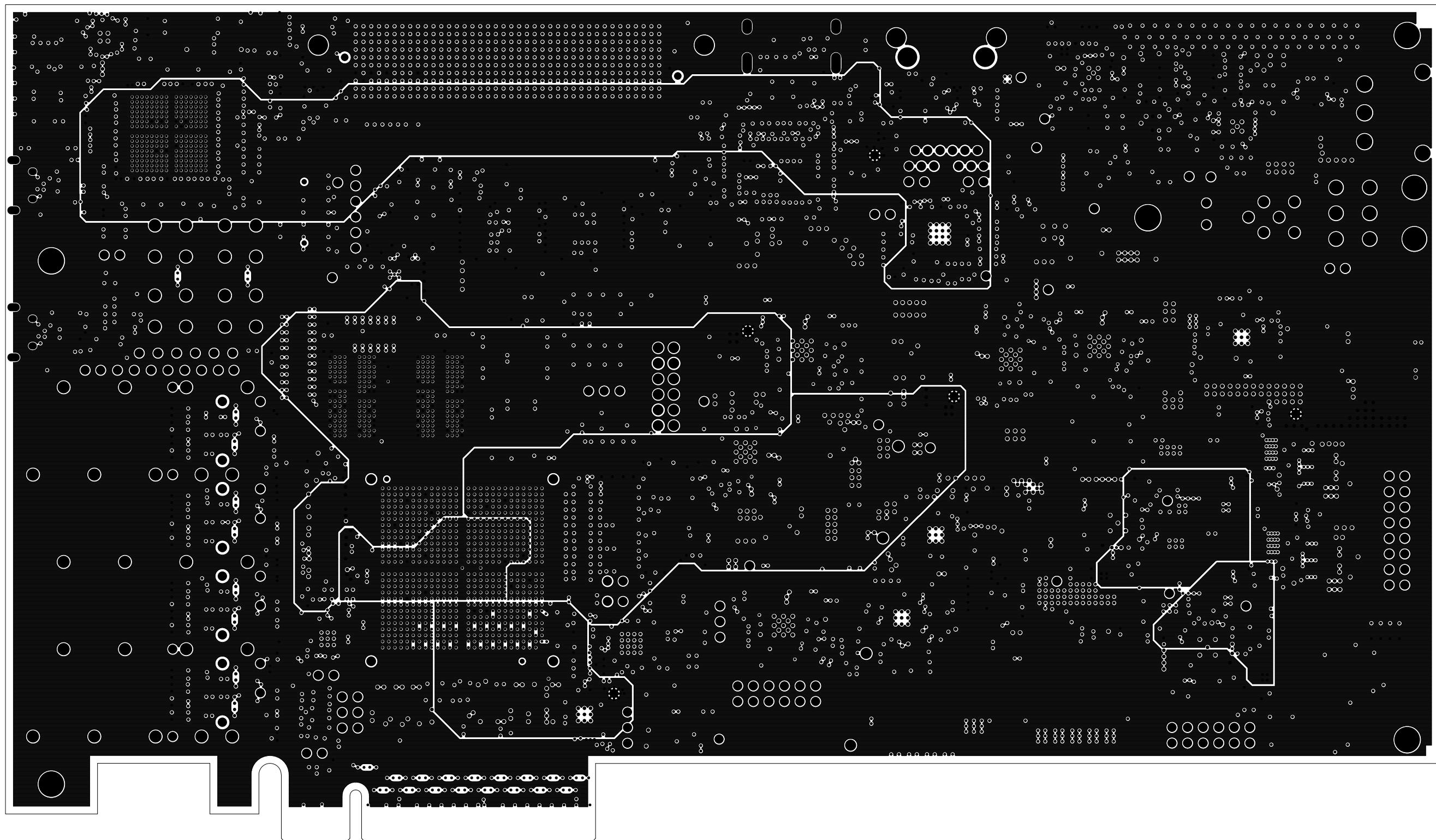
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Design Engineer: BFORSSE	Project Name: HW-U1-KCU116	
Whizz Job Number: 04-04-17	Date: 04-04-17	Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:



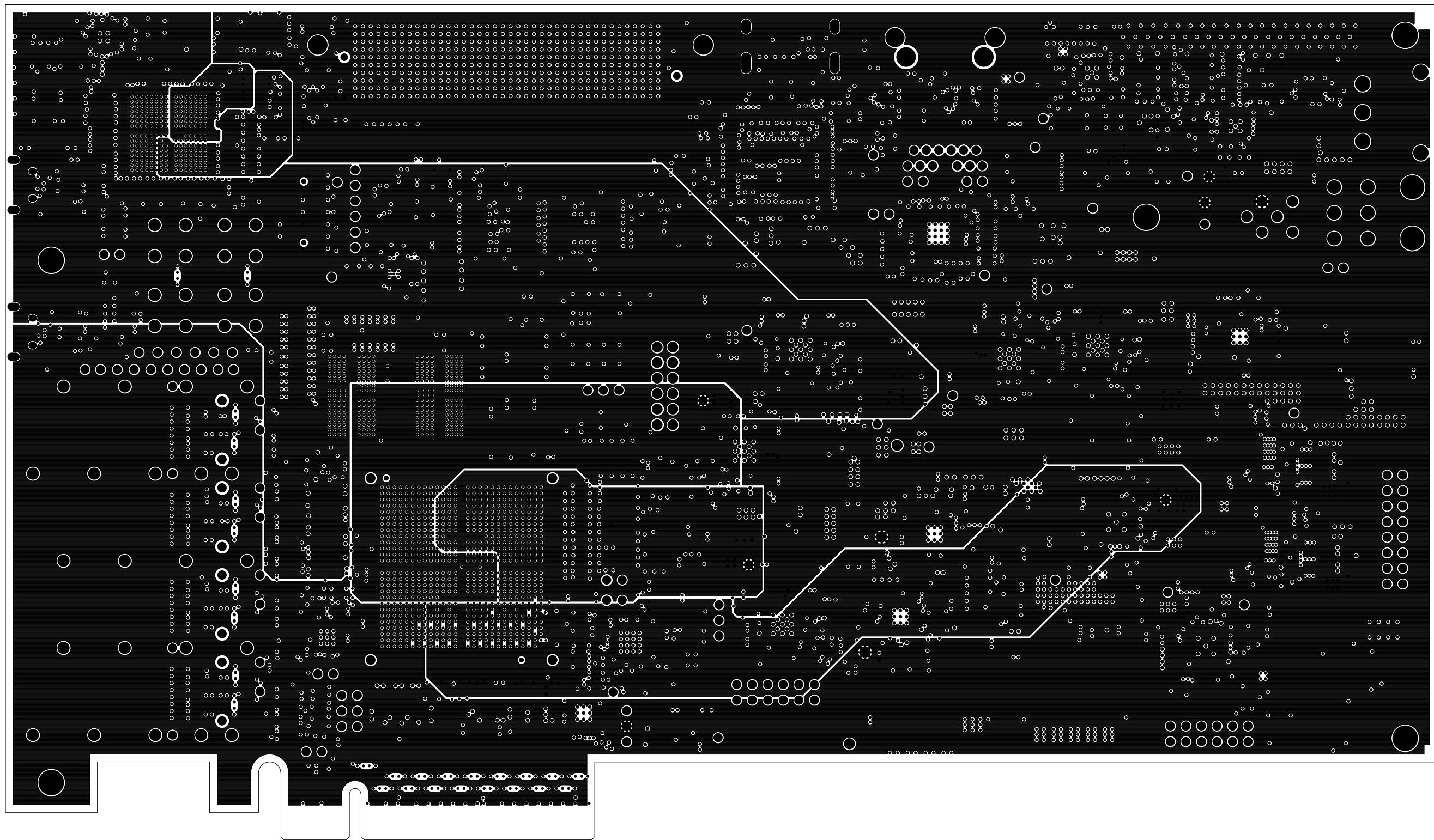
Layer: 07_PWR1	Sheet: 07 of: 22	
Layout Engineer: SCAREY	Company Name: XILINX	
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116	
Whizz Job Number: 04-04-17	Date: 04-04-17	Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:



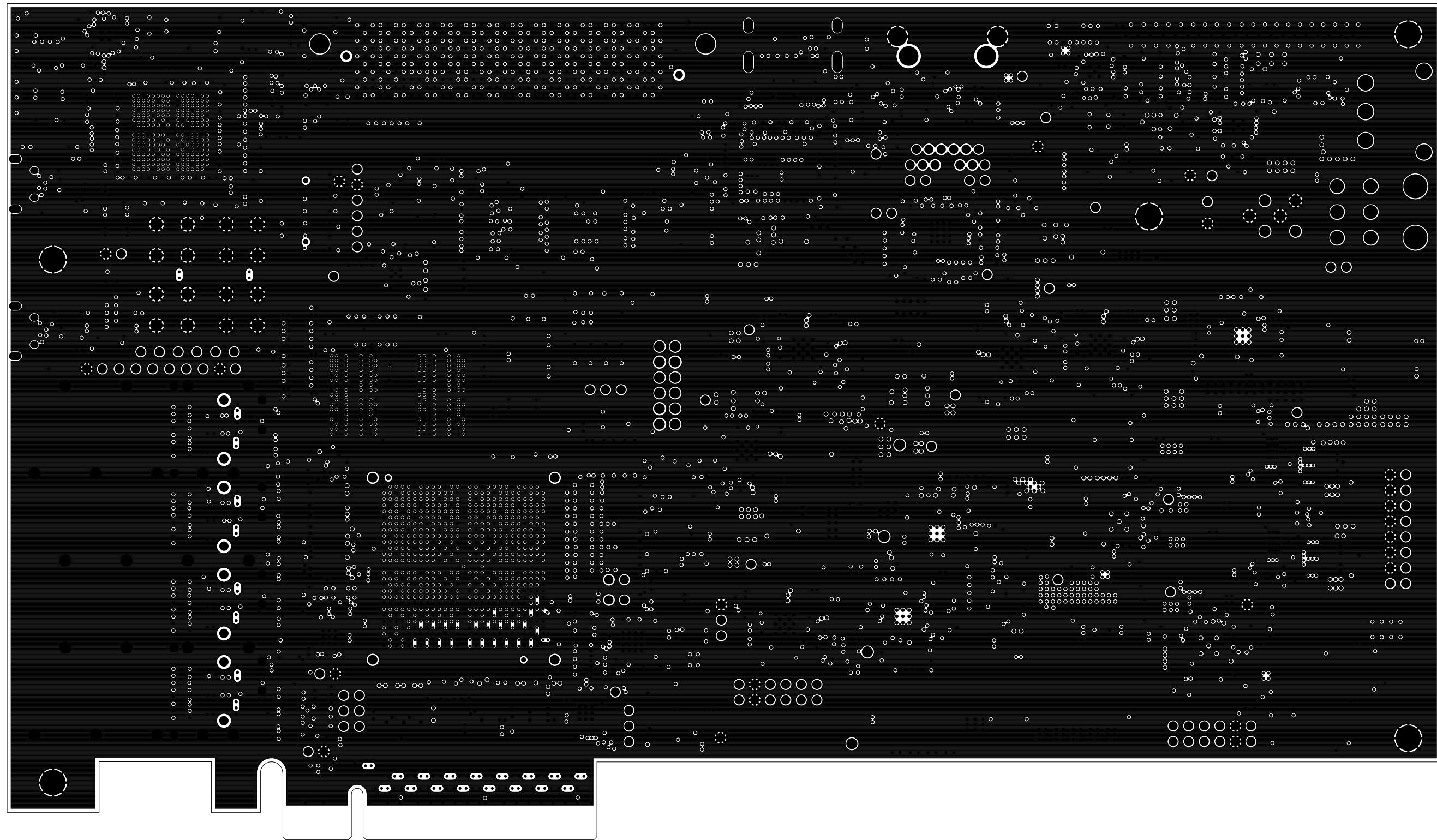
Layer: 08_PWR2	Sheet: 08 of: 22	
Layout Engineer: SCAREY	Company Name: XILINX	
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116	
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LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:



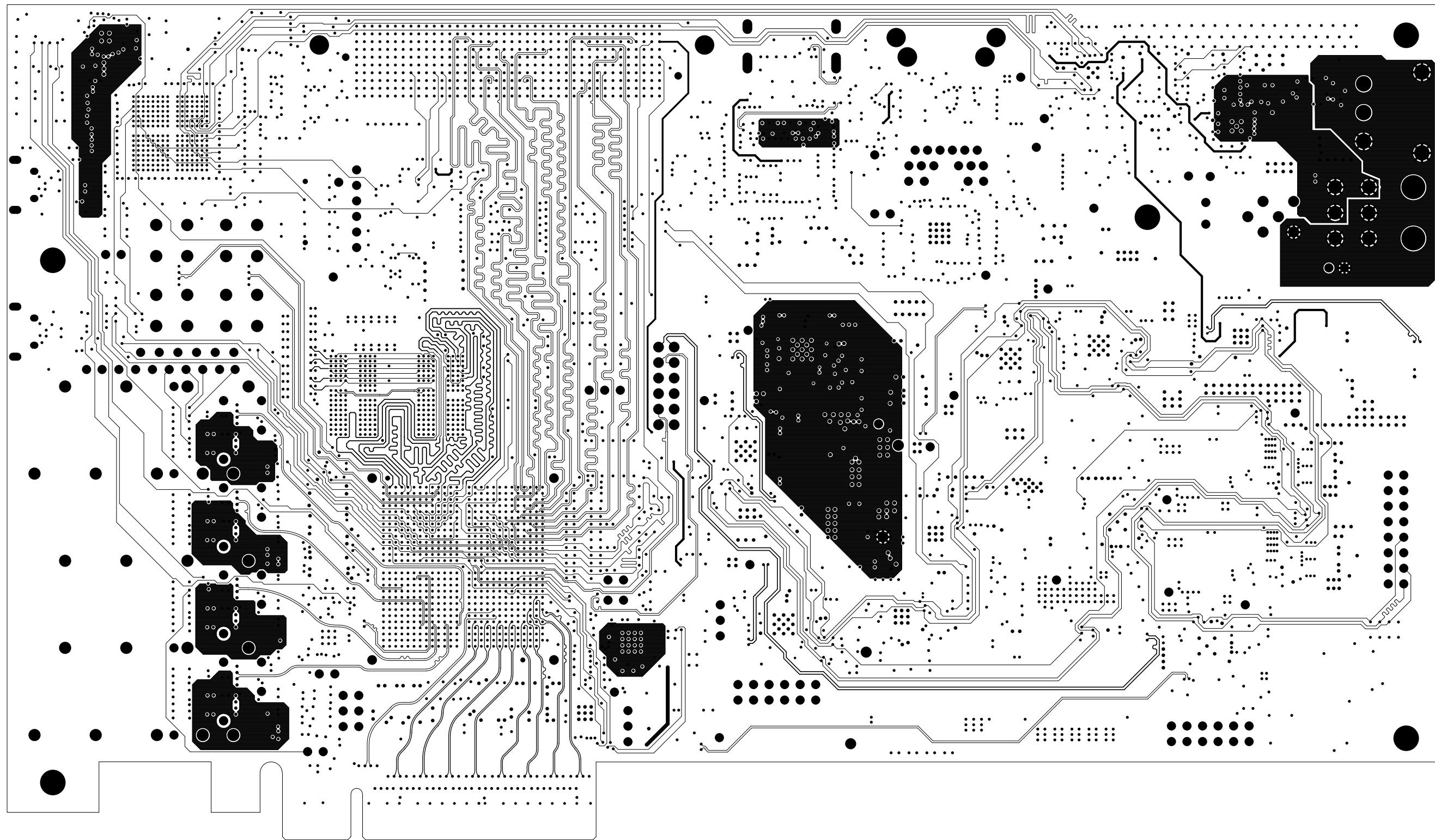
Layer: 09_PWR3	Sheet: 09 of: 22
Layout Engineer: SCAREY	Company Name: XILINX
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116
Whizz Job Number: 04-04-17	Date: Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:	
LATEST MECHANICAL REV OR DATE:	



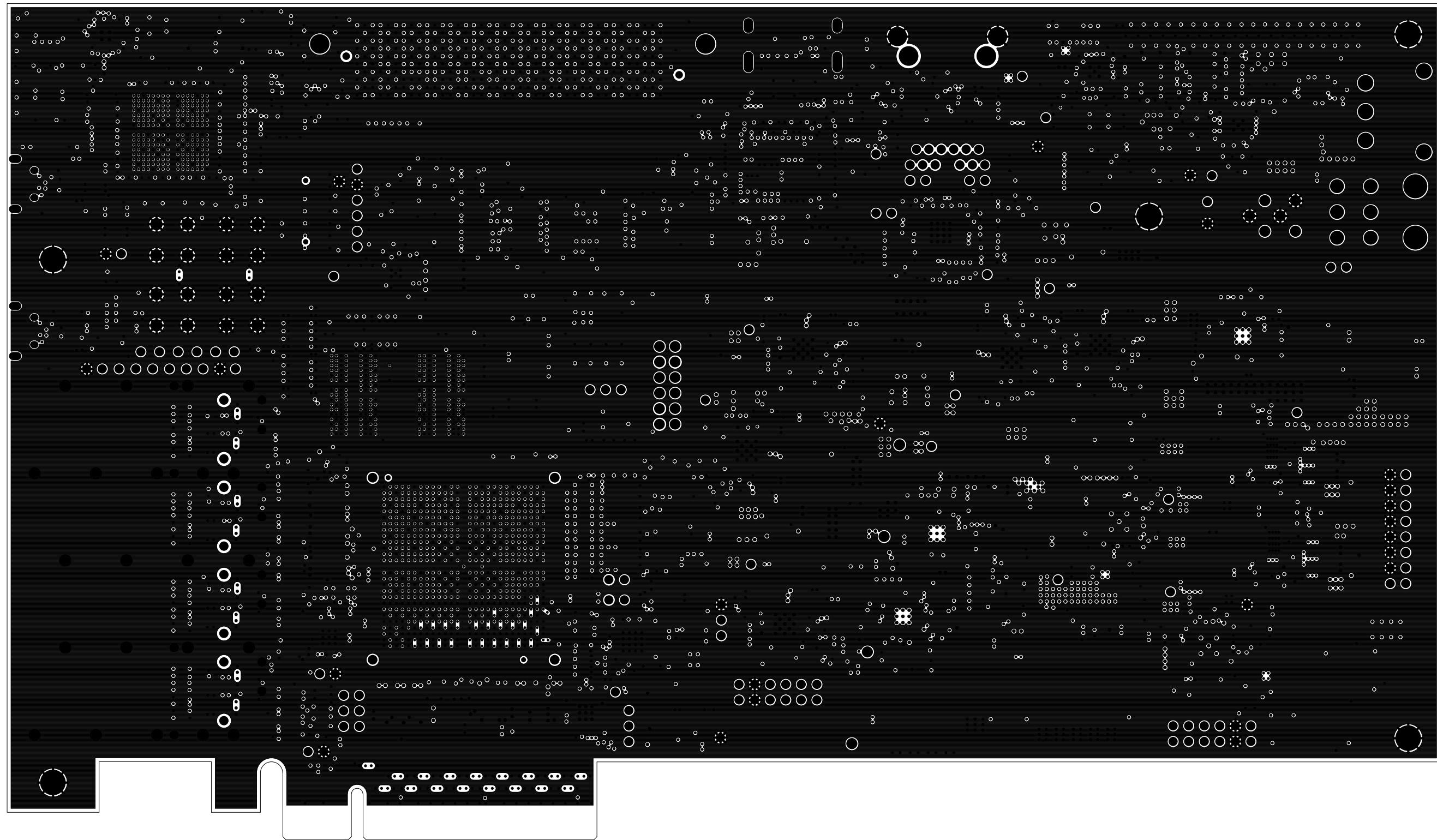
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Layout Engineer: SCAREY	Company Name: XILINX
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116
Whizz Job Number: 04-04-17	Date: 04-04-17 Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:	LATEST MECHANICAL REV OR DATE:



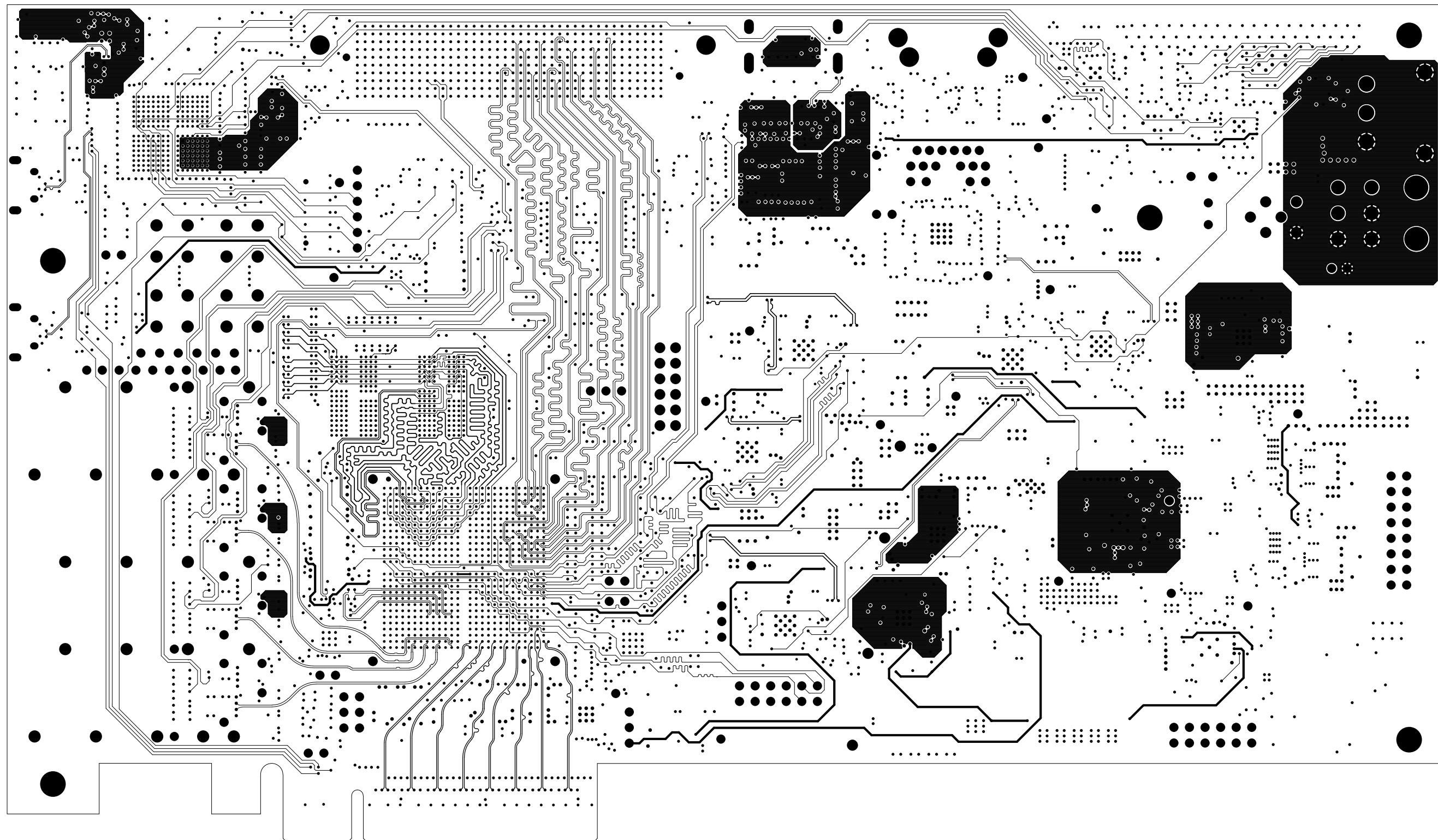
Layer: 11_GND4		Sheet: 11 of: 22	
Layout Engineer:	SCAREY	Company Name:	XILINX
Design Engineer:	BFORSSE	Project Name:	HW-U1-KCU116
Whizz Job Number:	Date: 04-04-17	Project Number:	1280924 REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:	



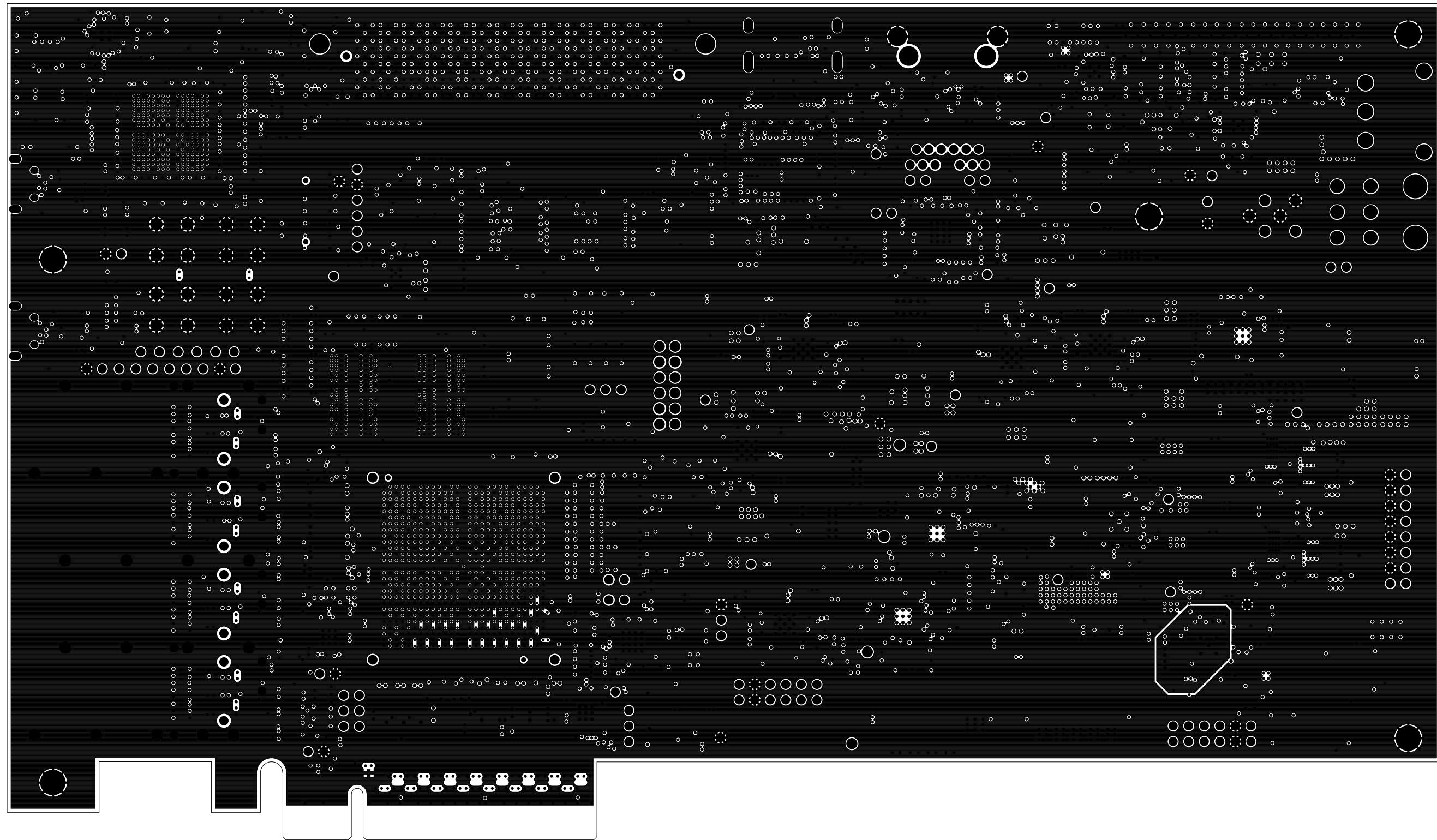
Layer: 12_SIG3	Sheet: 12 of: 22	
Layout Engineer: SCAREY	Company Name: XILINX	
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116	
Whizz Job Number: 04-04-17	Date: 04-04-17	Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:



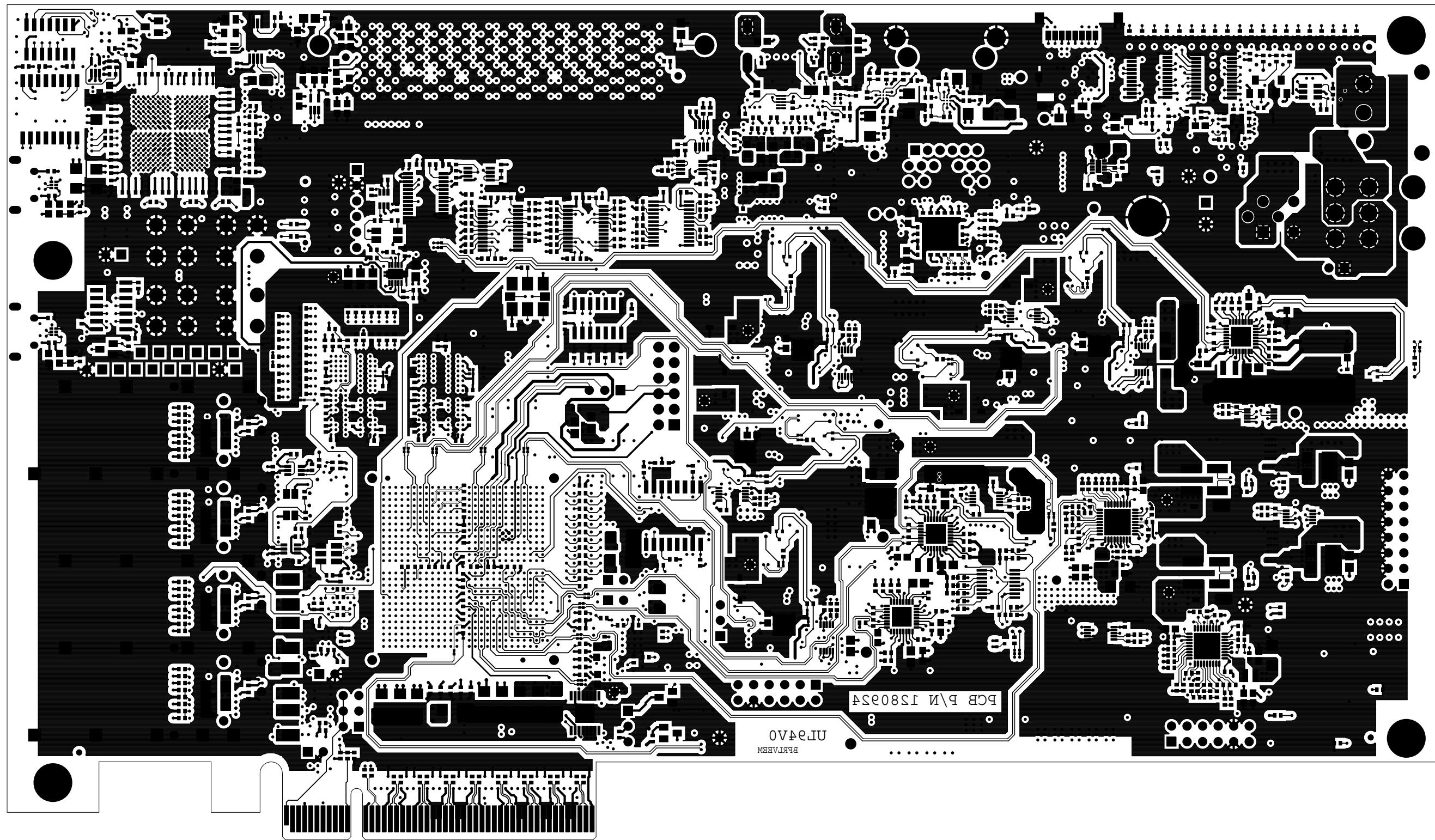
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Layout Engineer: SCAREY	Company Name: XILINX
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116
Whizz Job Number: 04-04-17	Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:	LATEST MECHANICAL REV OR DATE:



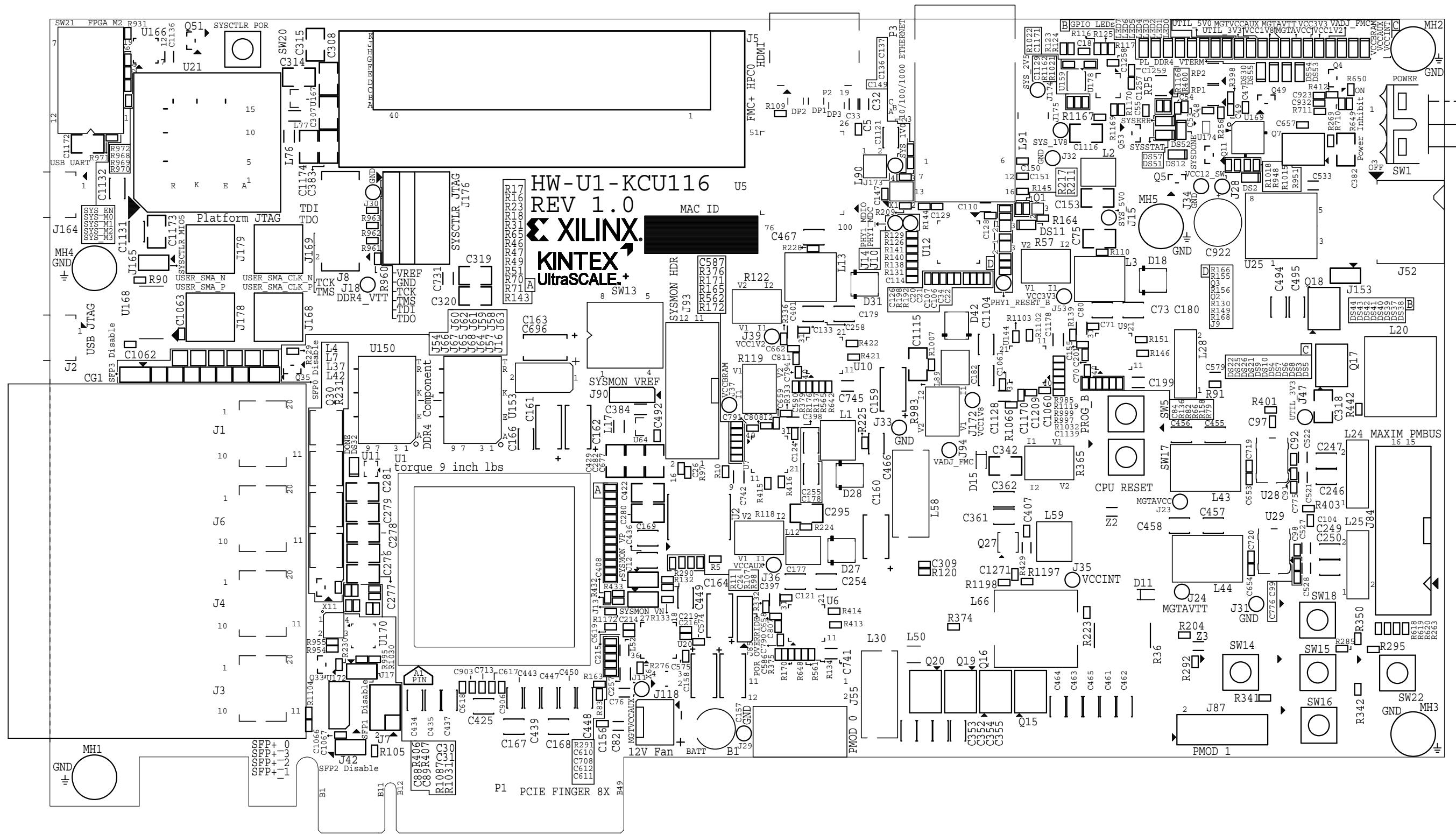
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Layout Engineer: SCAREY	Company Name: XILINX	
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116	
Whizz Job Number: 04-04-17	Date: 04-04-17	Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:



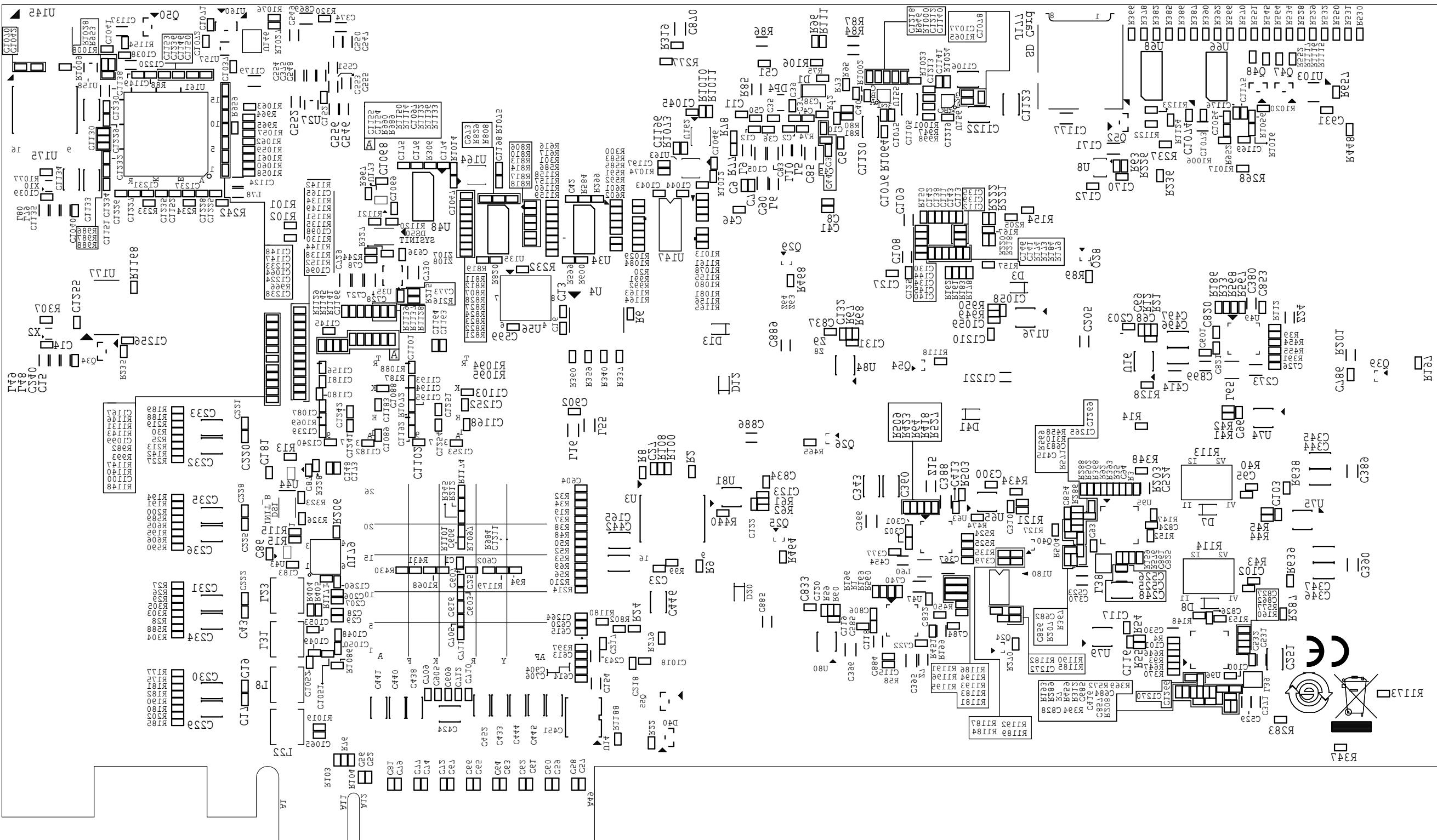
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Design Engineer:	BFORSSE	Project Name:	HW-U1-KCU116
Whizz Job Number:	Date: 04-04-17	Project Number:	1280924 REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:	



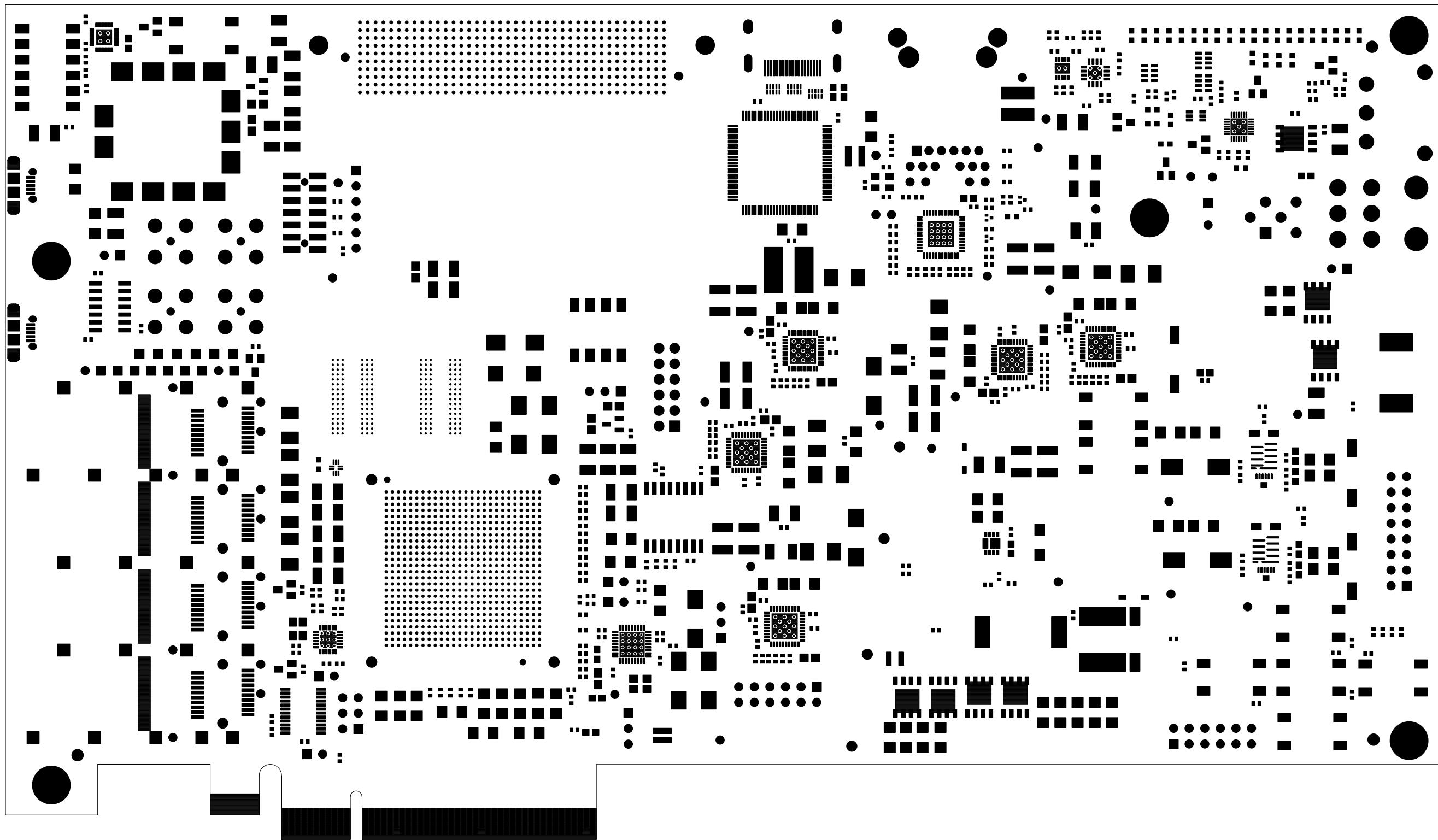
Layer: BOTTOM		Sheet: 16 of: 22
Layout Engineer:	SCAREY	Company Name: XILINX
Design Engineer:	BFORSSE	Project Name: HW-U1-KCU116
Whizz Job Number:	Date: 04-04-17	Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:



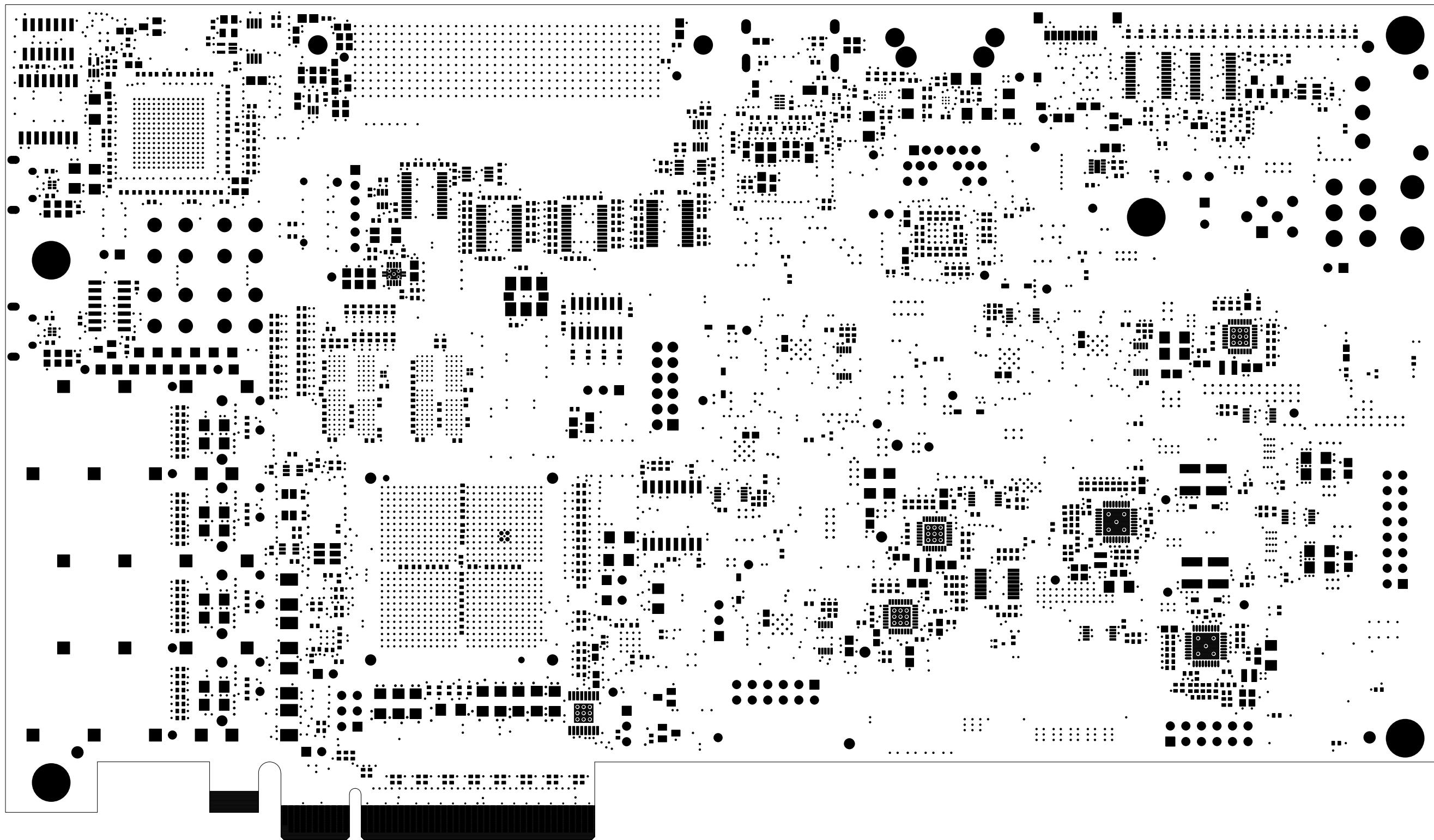
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Layout Engineer: SCAREY	Company Name:	XILINX
Design Engineer: BFORSSE	Project Name:	HW-U1-KCU116
Whizz Job Number:	Date: 04-04-17	Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:	LATEST MECHANICAL REV OR DATE:	



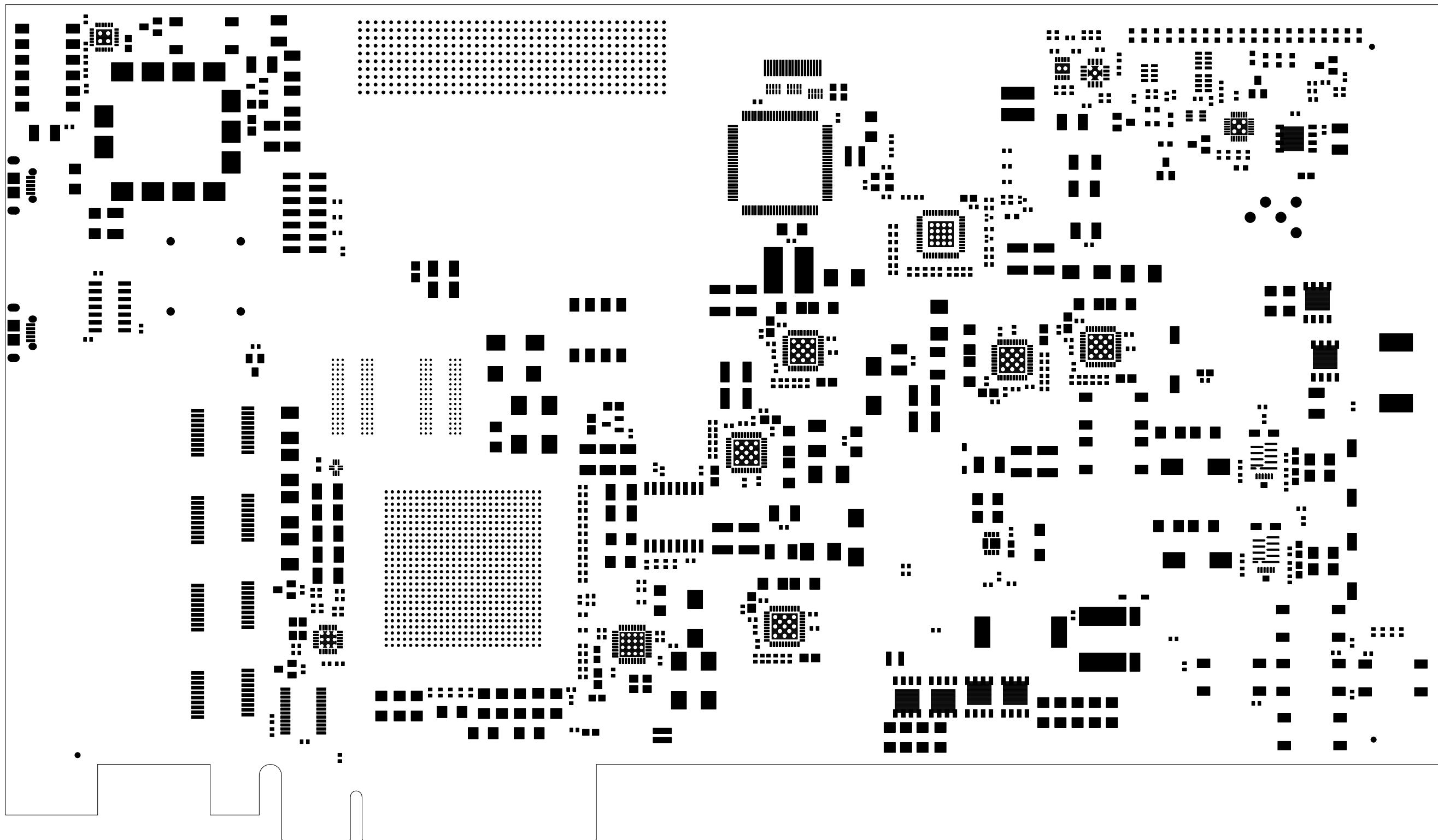
Layer: 18_SILK_BOT	Sheet: 18	of: 22
Layout Engineer: SCAREY	Company Name: XILINX	
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116	
Whizz Job Number: 04-04-17	Project Number: 1280924	REV. 1.0
LATEST NETLIST REV OR DATE:	LATEST MECHANICAL REV OR DATE:	



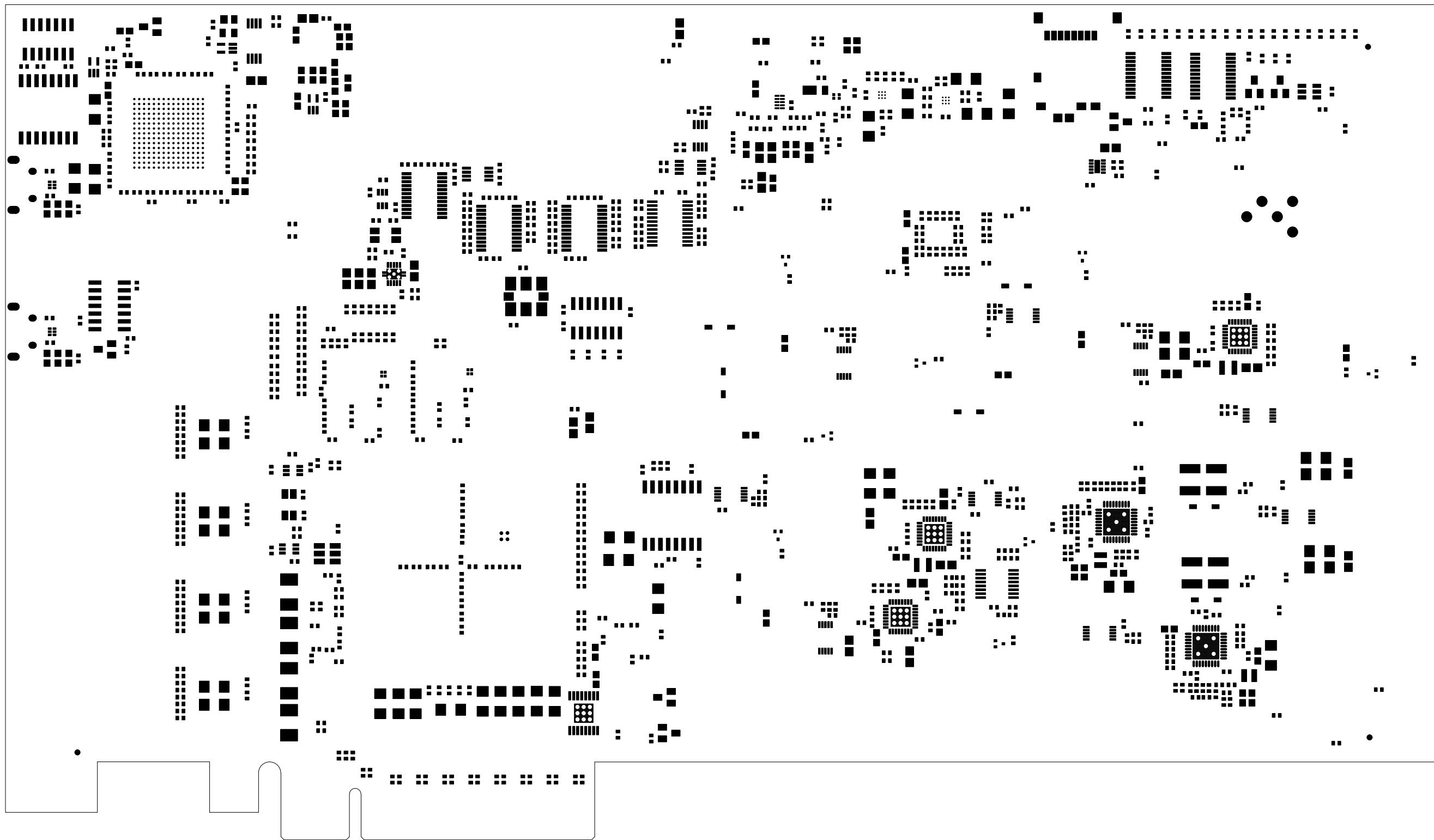
Layer: 19_SMASK_TOP	Sheet: 19 of: 22		
Layout Engineer: SCAREY	Company Name: XILINX		
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116		
Whizz Job Number: 04-04-17	Date: 04-04-17	Project Number: 1280924	REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:	



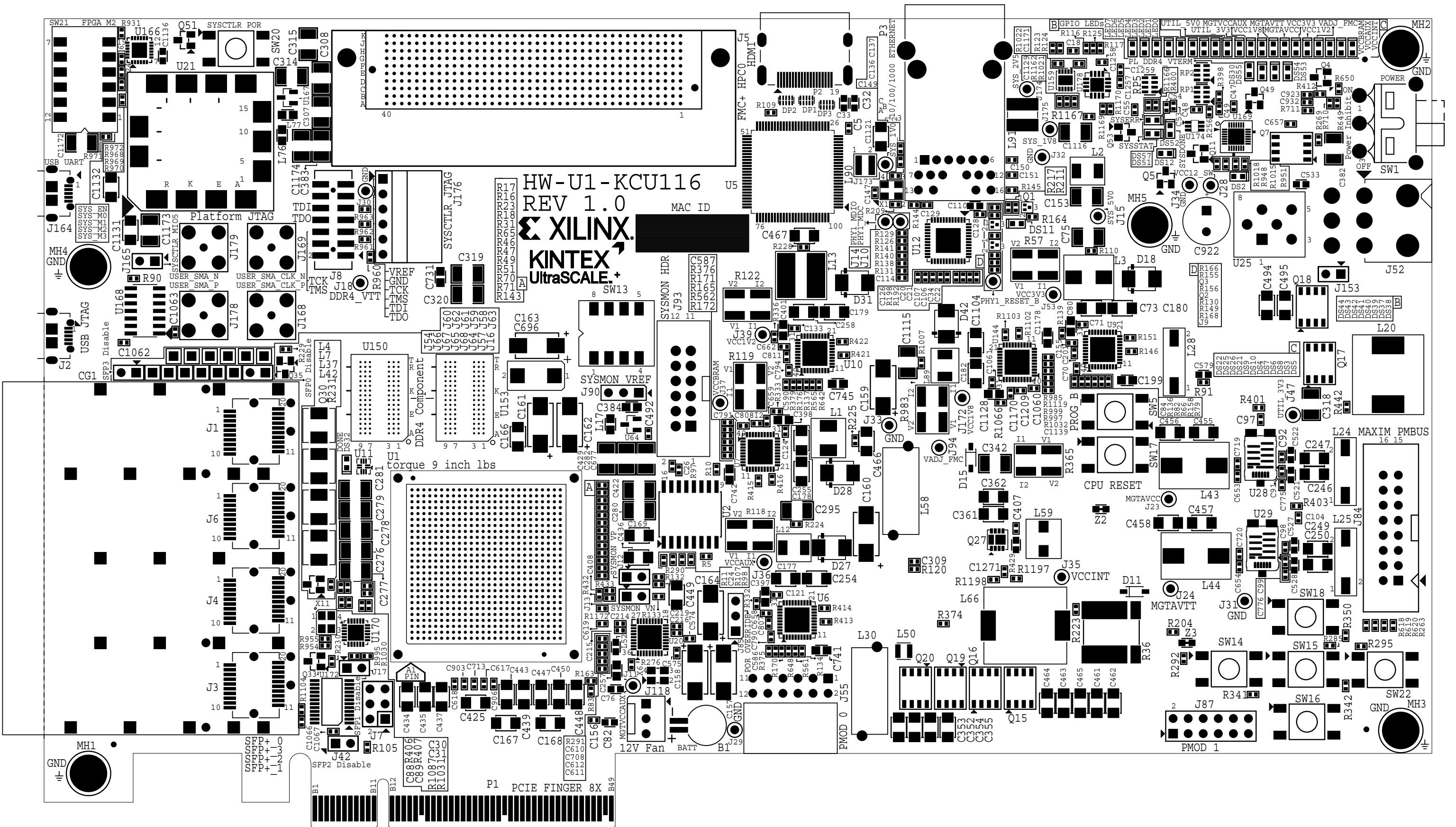
Layer: 20_SMASK_BOT	Sheet: 20 of: 22	
Layout Engineer: SCAREY	Company Name: XILINX	
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116	
Whizz Job Number: 04-04-17	Project Number: 1280924	REV. 1.0
LATEST NETLIST REV OR DATE:	LATEST MECHANICAL REV OR DATE:	

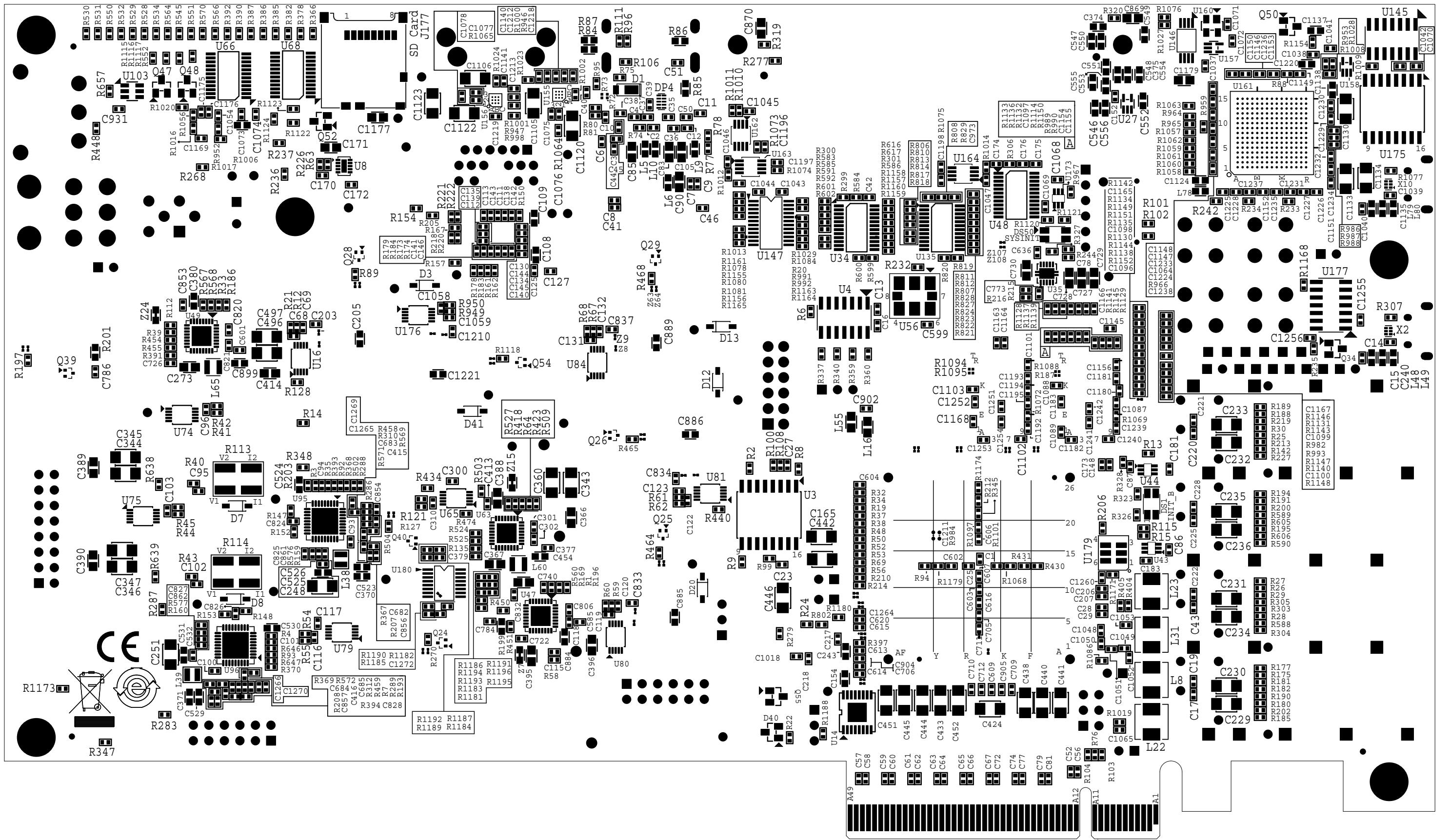


Layer: 21_PMASK_TOP	Sheet: 21 of: 22		
Layout Engineer: SCAREY	Company Name: XILINX		
Design Engineer: BFORSSE	Project Name: HW-U1-KCU116		
Whizz Job Number: 04-04-17	Date: 04-04-17	Project Number: 1280924	REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:	



Layer: 22_PMASK_BOT	Sheet:	22 of: 22
Layout Engineer: SCAREY	Company Name:	XILINX
Design Engineer: BFORSSE	Project Name:	HW-U1-KCU116
Whizz Job Number: 04-04-17	Date:	Project Number: 1280924 REV. 1.0
LATEST NETLIST REV OR DATE:		LATEST MECHANICAL REV OR DATE:





NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ASSEMBLE TO MEET INSPECTION CRITERIA OF IPC-A-610, CLASS 2, CURRENT REVISION.
2. BAG AND TAG (OR MARK CONTAINER) WITH PART NUMBER.
3. REFERENCE SCHEMATIC (OR AVL) FOR BILL OF MATERIALS.
4. ASSEMBLY SHOULD BE "ROHS" AND "LEAD FREE" COMPLIANT.
5. CG1 IS PRESSFIT CONNECTOR.
6. FAB IS BOUND TO USE "SAC305" SOLDER PASTE FOR COMPONENT ASSEMBLY.
7. (a). VERIFY THAT THE SOLDER PASTE IS NOT APPLIED TO THE BGA PADS ON THE TOPSIDE.
- (b). VERIFY THAT SOLDER PASTE IS NOT APPLIED TO THE UN-POPULATED RESISTORS AND CAPACITORS UNDERNEATH U1.
8. SERIAL NUMBER INSTRUCTIONS:-
" FOLLOW THE XILINX SERIAL NUMBER CONVENTION. FOR EXAMPLE KCU105 REV A IS NUMBERED 1280723A001 TO 1280723A020, REV B SHOULD START AT 1280723B001 AND END AT 1280723B075"
FOR REV C IT SHOULD START AT 1280723C001
9. DATASHEET SHOULD BE FOLLOWED FOR ALL HSMF-C155 DEVICES.
10. MAXIMUM PASTE MASK STENCIL THICKNESS IN THE AREA OF MAXIM POWER SUPPLIES (EG HPQFN_19_A DEVICES) MUST BE 4MILS MAX.

1 2
3 4

REVISIONS		
REV	DESCRIPTION	DATE APPROVED
A	PROTOTYPE	11/30/16
B	SFP FIXES	12/3/16
C	SFP SWAPS PCIE SI FIX	02/13/17
1.0	PRODUCTION RELEASE	04/04/17

