



# VC707 GTX IBERT Design Creation

April 2015

XTP210

# Revision History

Date	Version	Description
04/30/14	12.0	Regenerated for 2015.1.
11/24/14	11.0	Regenerated for 2014.4.
10/08/14	10.0	Regenerated for 2014.3.
06/09/14	9.0	Regenerated for 2014.2.
04/16/14	8.0	Regenerated for 2014.1.
12/18/13	7.0	Regenerated for 2013.4.
10/23/13	6.0	Regenerated for 2013.3.
06/19/13	5.0	Regenerated for 2013.2.
04/03/13	4.0	Regenerated for 2013.1.
12/18/12	3.0	Regenerated for 2012.4.
10/23/12	2.0	Regenerated for 2012.3.
08/20/12	1.0	Initial version for 2012.2.

© Copyright 2015 Xilinx, Inc. All Rights Reserved.

XILINX, the Xilinx logo, the Brand Window and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

**NOTICE OF DISCLAIMER:** The information disclosed to you hereunder (the “Information”) is provided “AS-IS” with no warranty of any kind, express or implied. Xilinx does not assume any liability arising from your use of the Information. You are responsible for obtaining any rights you may require for your use of this Information. Xilinx reserves the right to make changes, at any time, to the Information without notice and at its sole discretion. Xilinx assumes no obligation to correct any errors contained in the Information or to advise you of any corrections or updates. Xilinx expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the Information. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE INFORMATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS.

# VC707 IBERT Overview

- Xilinx VC707 Board
- Software Requirements
- Setup for the VC707 IBERT Designs
- Testing IBERT Bank 113
  - Create IBERT Design for Bank 113
    - Testing Bank 113 with Optional User Provided Hardware
- Create IBERT Design for Banks 114, 115
  - Testing Banks 114 and 115 with Optional User Provided Hardware
- References

# VC707 IBERT Overview

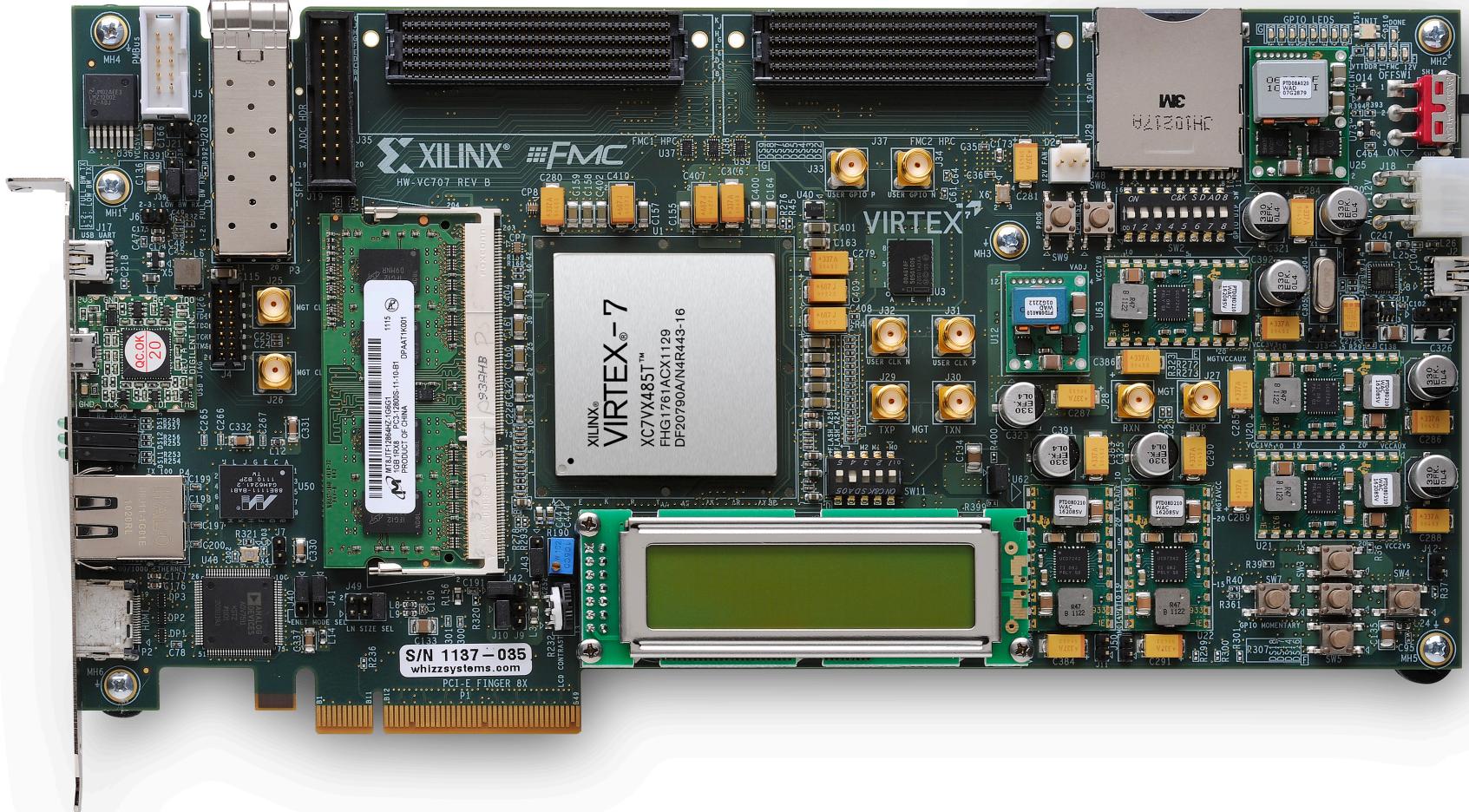
## ► Description

- The LogiCORE Integrated Bit Error Ratio (IBERT) core is used to create a pattern generation and verification design to exercise the Virtex-7 GTX transceivers. A graphical user interface is provided through the Vivado Hardware Manager.

## ► Reference Design IP

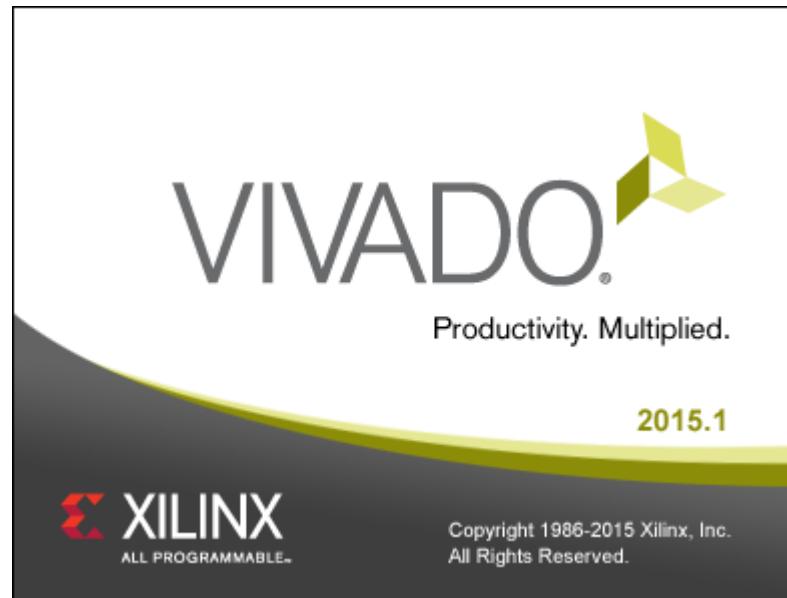
- LogiCORE IBERT Example Designs

# Xilinx VC707 Board



# Vivado Software Requirements

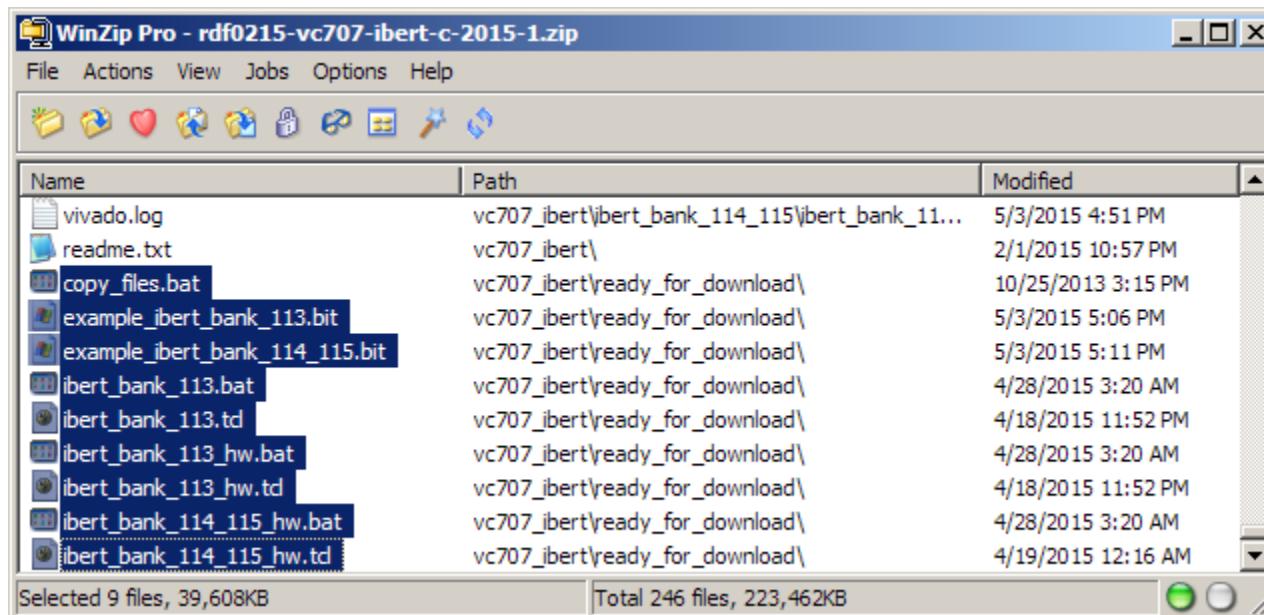
- Xilinx Vivado Design Suite 2015.1, Design Edition



# **Setup for the VC707 IBERT Designs**

# Setup for the VC707 IBERT Designs

- Open the VC707 GTX IBERT Design Files (2015.1 C) ZIP file, and extract these files to your C:\ drive:
  - vc707\_ibert\ready\_for\_download\\*
  - Available through <http://www.xilinx.com/vc707>

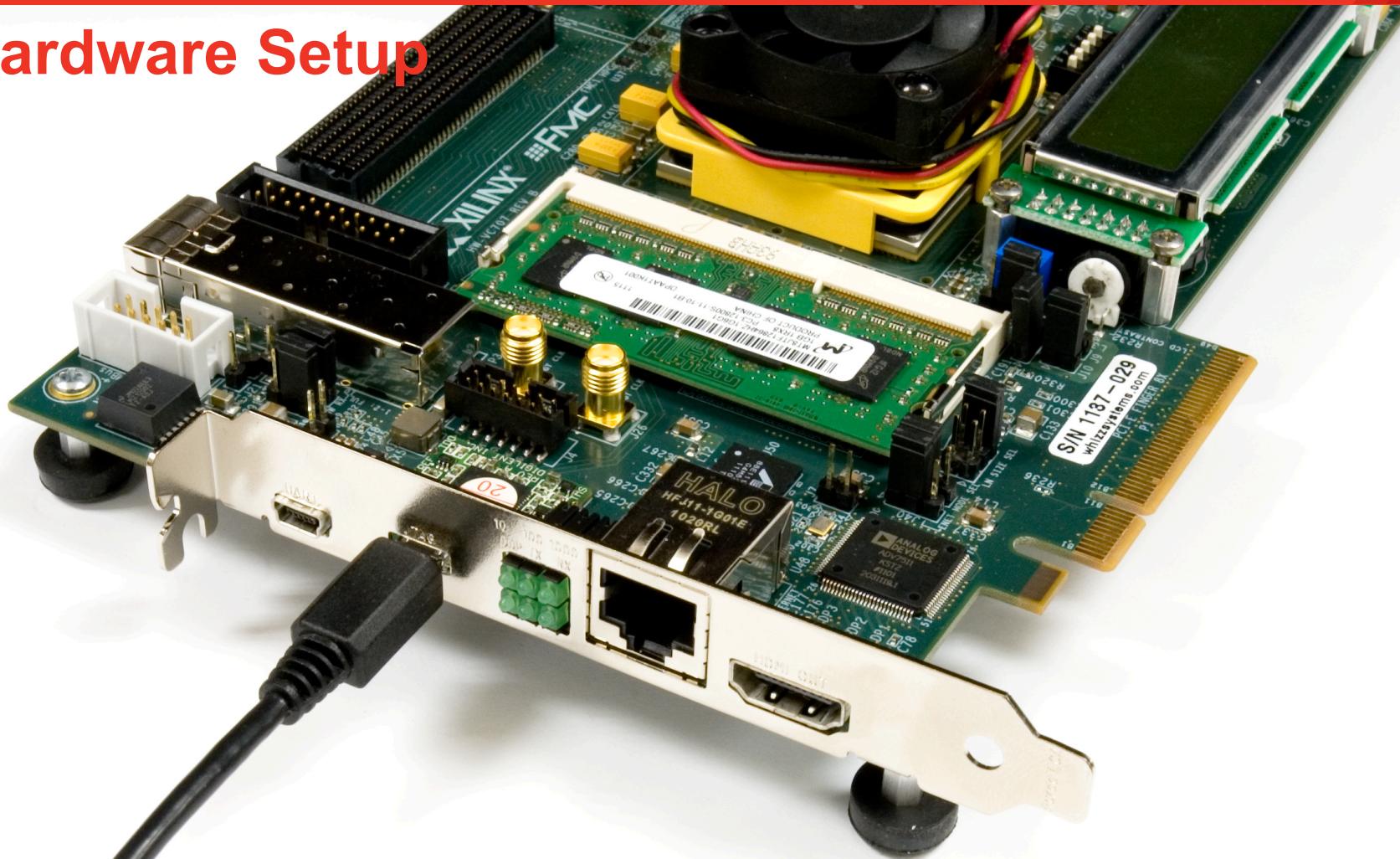


# Hardware Setup

- Set SW11 to 00101 (1 = on, Position 1 → Position 5, left to right)
  - This enables JTAG configuration



# Hardware Setup



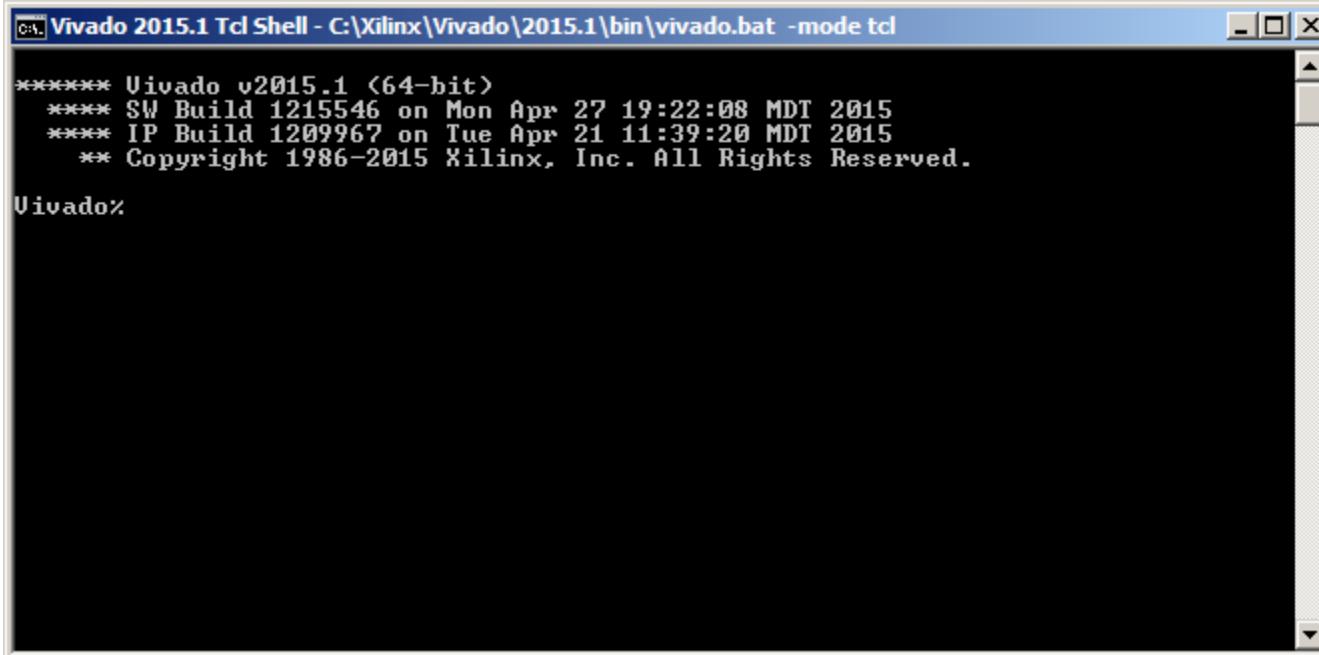
- **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the VC707 board**
  - Connect this cable to your PC
  - Power on the VC707 board

**Testing IBERT Bank 113**

# Testing IBERT Bank 113

## ► Open a Vivado Tcl Shell:

**Start → All Programs → Xilinx Design Tools → Vivado 2015.1 →  
Vivado 2015.1 Tcl Shell**



The screenshot shows a Windows command-line interface window titled "Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl". The window displays the following startup information:

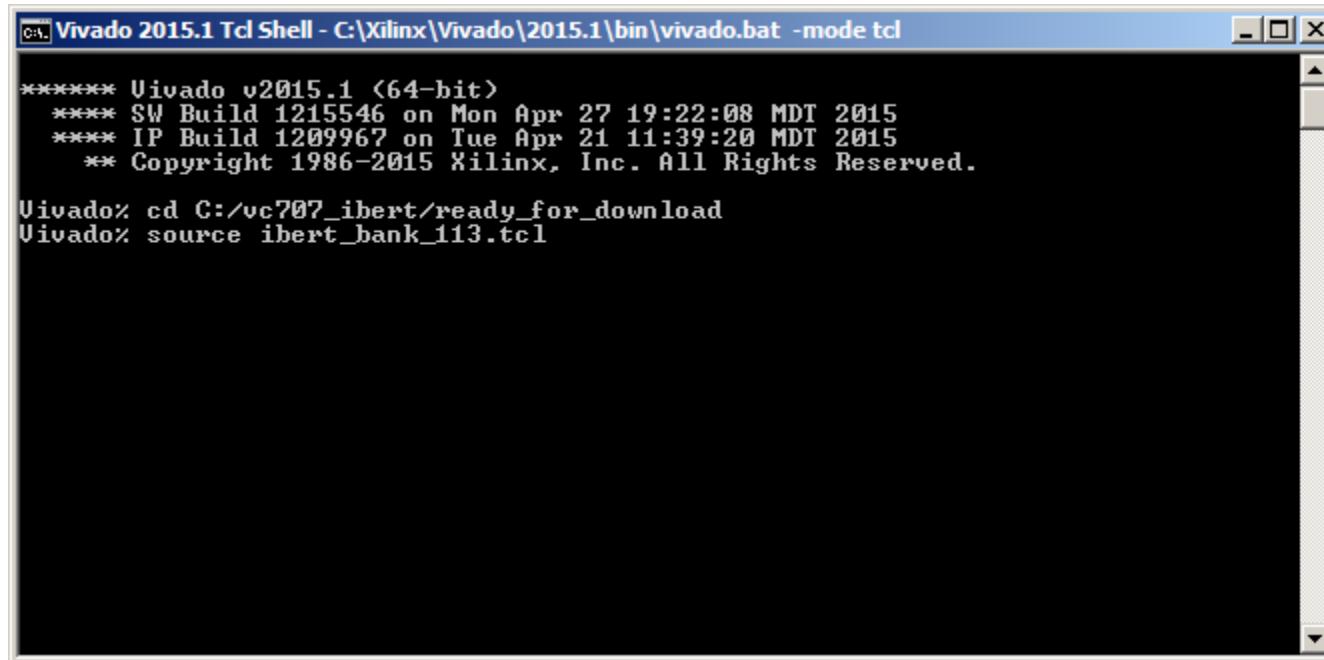
```
***** Vivado v2015.1 (64-bit)
***** SW Build 1215546 on Mon Apr 27 19:22:08 MDT 2015
***** IP Build 1209967 on Tue Apr 21 11:39:20 MDT 2015
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.
```

The prompt "Vivado%" is visible at the bottom of the window.

# Testing IBERT Bank 113

- In the Vivado Tcl Shell type:

```
cd C:/vc707_ibert/ready_for_download  
source ibert_bank_113.tcl
```

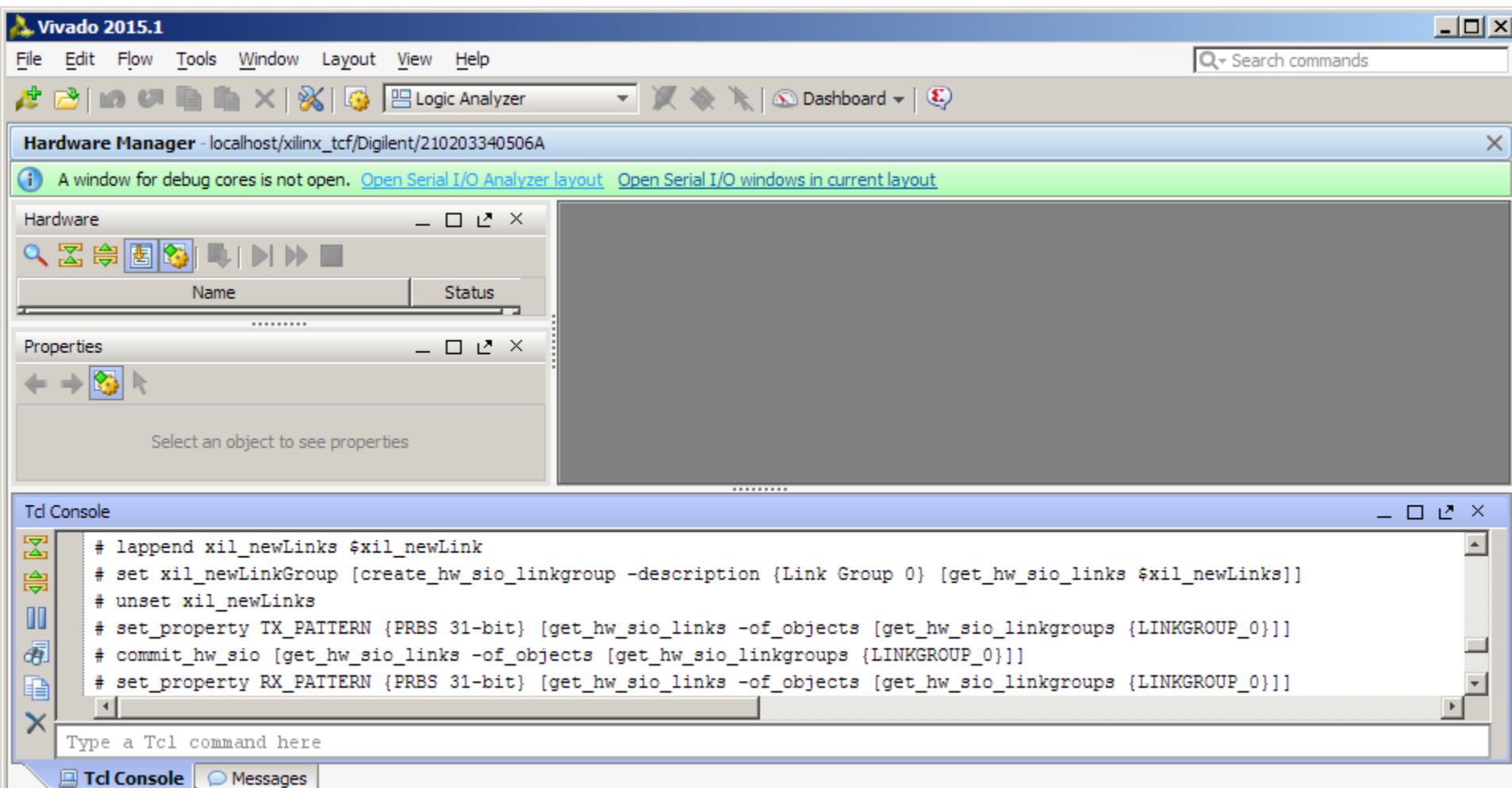


The screenshot shows a terminal window titled "Vivado 2015.1 Tcl Shell - C:\Xilinx\Vivado\2015.1\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2015.1 (64-bit)  
***** SW Build 1215546 on Mon Apr 27 19:22:08 MDT 2015  
***** IP Build 1209967 on Tue Apr 21 11:39:20 MDT 2015  
** Copyright 1986-2015 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/vc707_ibert/ready_for_download  
Vivado> source ibert_bank_113.tcl
```

# Testing IBERT Bank 113

► If needed, click on Open Serial I/O Analyzer layout



# Testing IBERT Bank 113

► The Status column shows the line rate is 10.000 Gbps for all GTXs

The screenshot shows the Vivado 2015.1 interface with the "Hardware Manager" window open. The window title is "Hardware Manager - localhost/xilinx\_tcf/Digilent/210203340506A". The main area displays "Serial I/O Links" for three links: Link 0, Link 1, and Link 2. All three links are operating at 10.000 Gbps, as indicated by the green background color in the "Status" column. The "TX" and "RX" columns show the respective MGT\_X1Y0, MGT\_X1Y1, and MGT\_X1Y2 ports for each link. The "Status" column also shows the number of bits processed (e.g., 7.592E11, 7.594E11, 7.597E11). The "Errors" column shows values like 0E0, 1.317E-12, and 1.316E-12. The "BERT" column shows BER values. The "BERT Reset" column contains "Reset" buttons. The "TX Pattern" and "RX Pattern" columns show PRBS 31-bit patterns. The "TX Pre-Cursor" and "TX P" columns are partially visible.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX P
Ungrouped Links (0)											
Link Group 0 (3)											
Link 0	MGT_X1Y0/TX	MGT_X1Y0/RX	10.000 Gbps	7.592E11	0E0	1.317E-12	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 d
Link 1	MGT_X1Y1/TX	MGT_X1Y1/RX	10.000 Gbps	7.594E11	0E0	1.317E-12	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 d
Link 2	MGT_X1Y2/TX	MGT_X1Y2/RX	10.000 Gbps	7.597E11	0E0	1.316E-12	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.68 d

# Testing IBERT Bank 113

- Scroll to the right; Loopback Mode is set to Near-End PCS
- Close Vivado GUI after finished viewing

	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode
1	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (11...)	<input checked="" type="checkbox"/>	Inject	R...	R...			Near-End PCS
2	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (11...)	<input checked="" type="checkbox"/>	Inject	R...	R...	Locked	Locked	Near-End PCS
3	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (11...)	<input checked="" type="checkbox"/>	Inject	R...	R...	Locked	Locked	Near-End PCS
4	PRBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (11...)	<input checked="" type="checkbox"/>	Inject	R...	R...	Locked	Locked	Near-End PCS

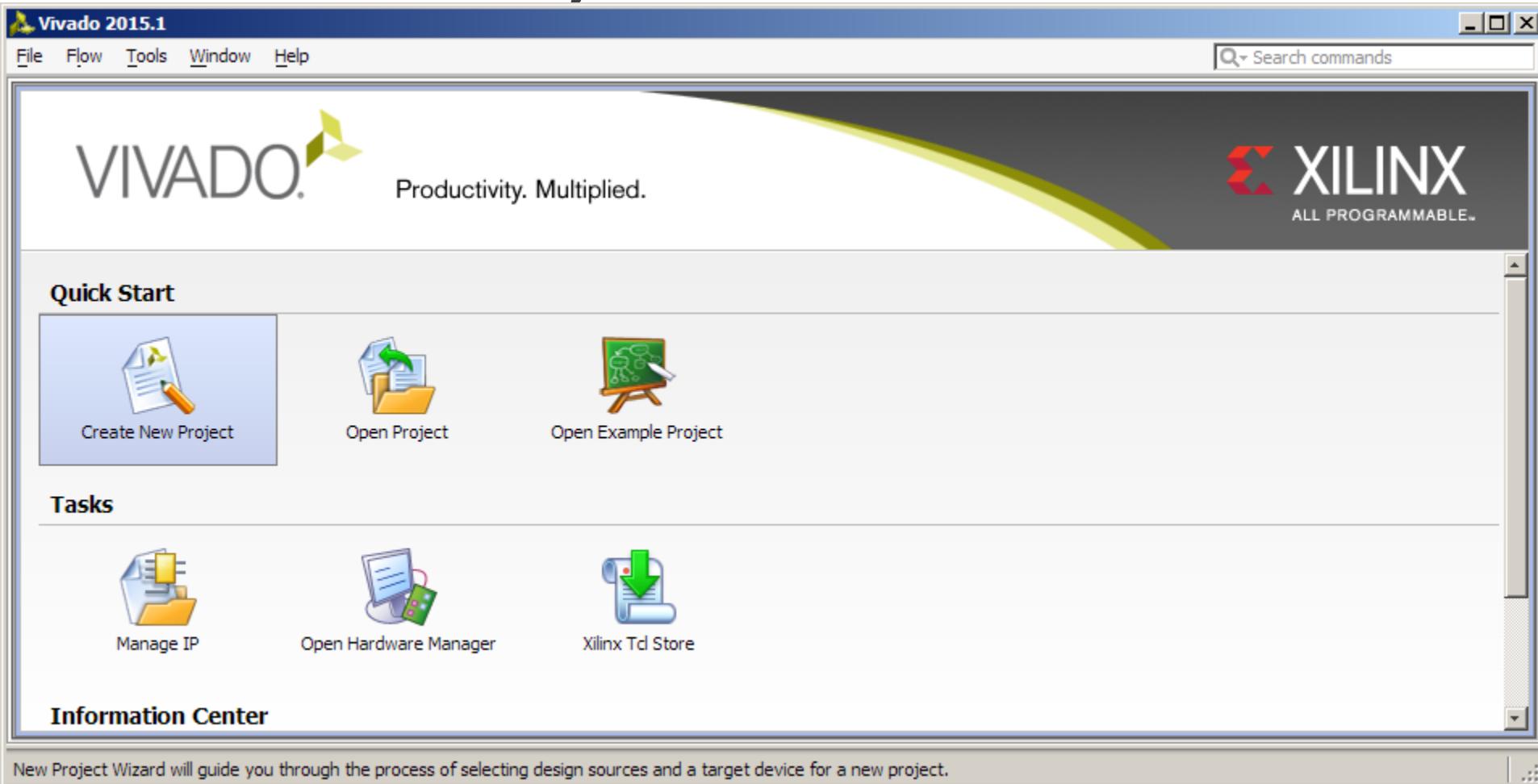
# Create IBERT Design for Bank 113

# Create IBERT Design for Bank 113

## ► Open Vivado

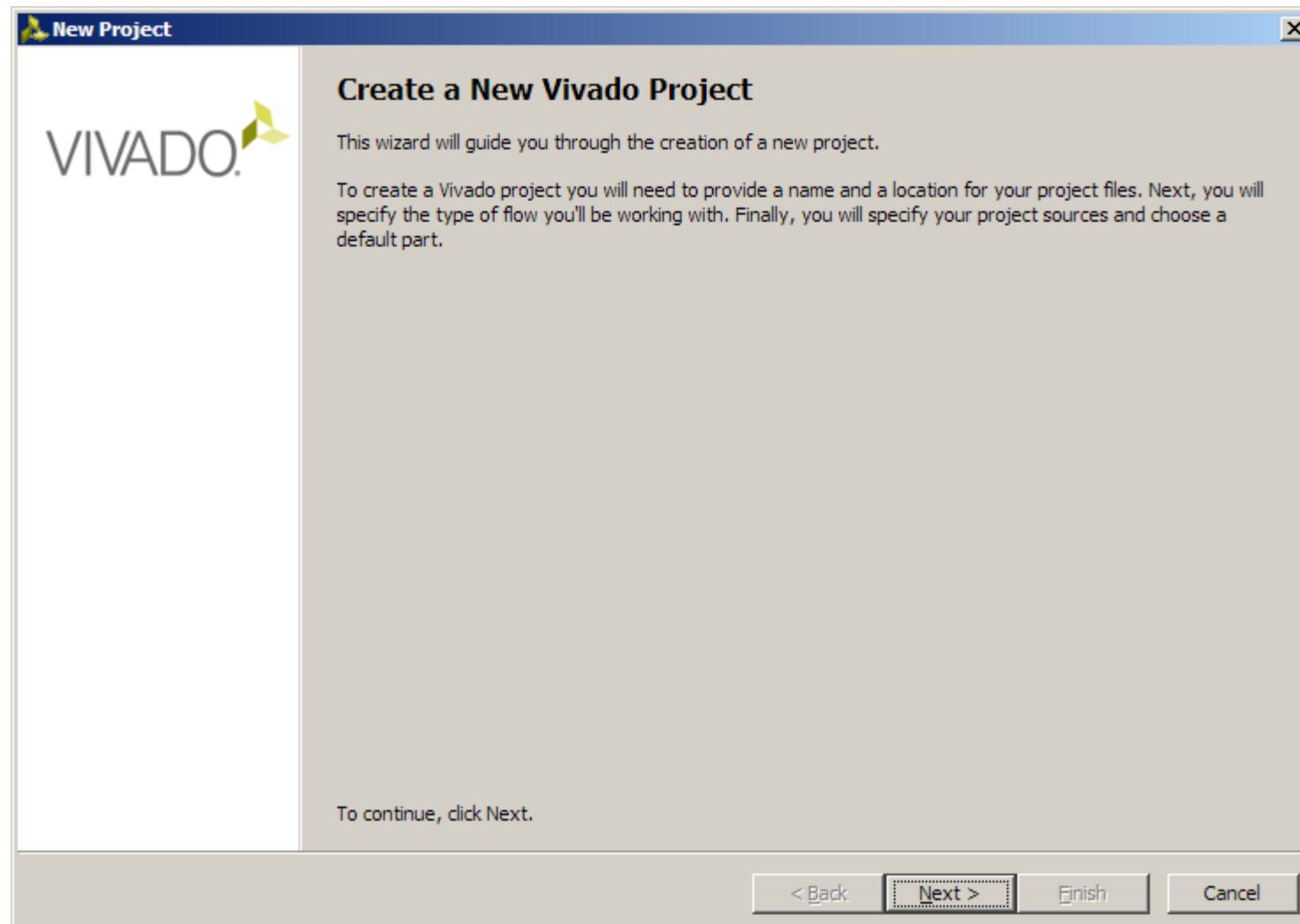
Start → All Programs → Xilinx Design Tools → Vivado 2015.1 → Vivado

## ► Select Create New Project



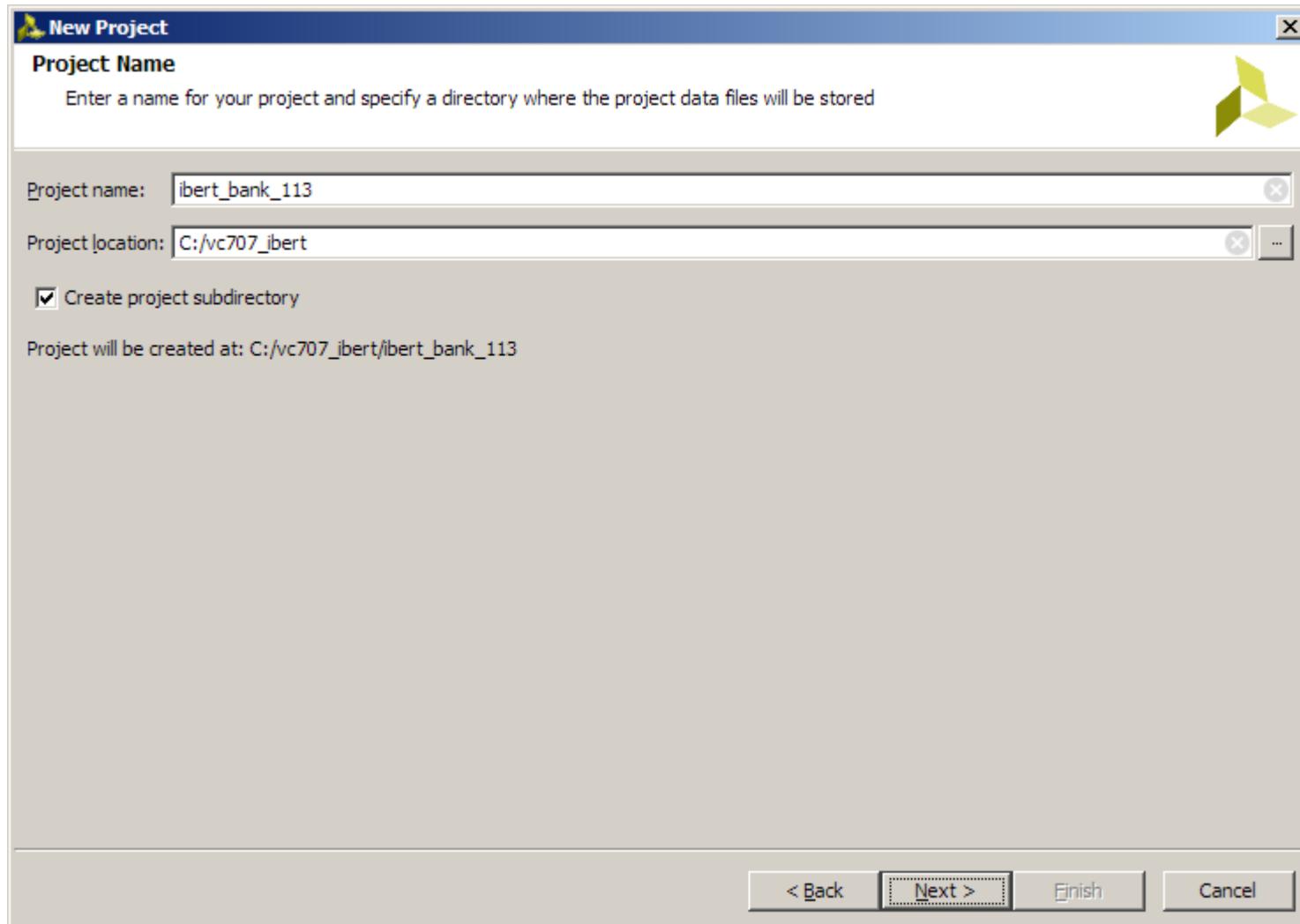
# Create IBERT Design for Bank 113

► Click Next



# Create IBERT Design for Bank 113

- Set the Project name and location to `ibert_bank_113` and `C:/vc707_ibert`; check Create project subdirectory



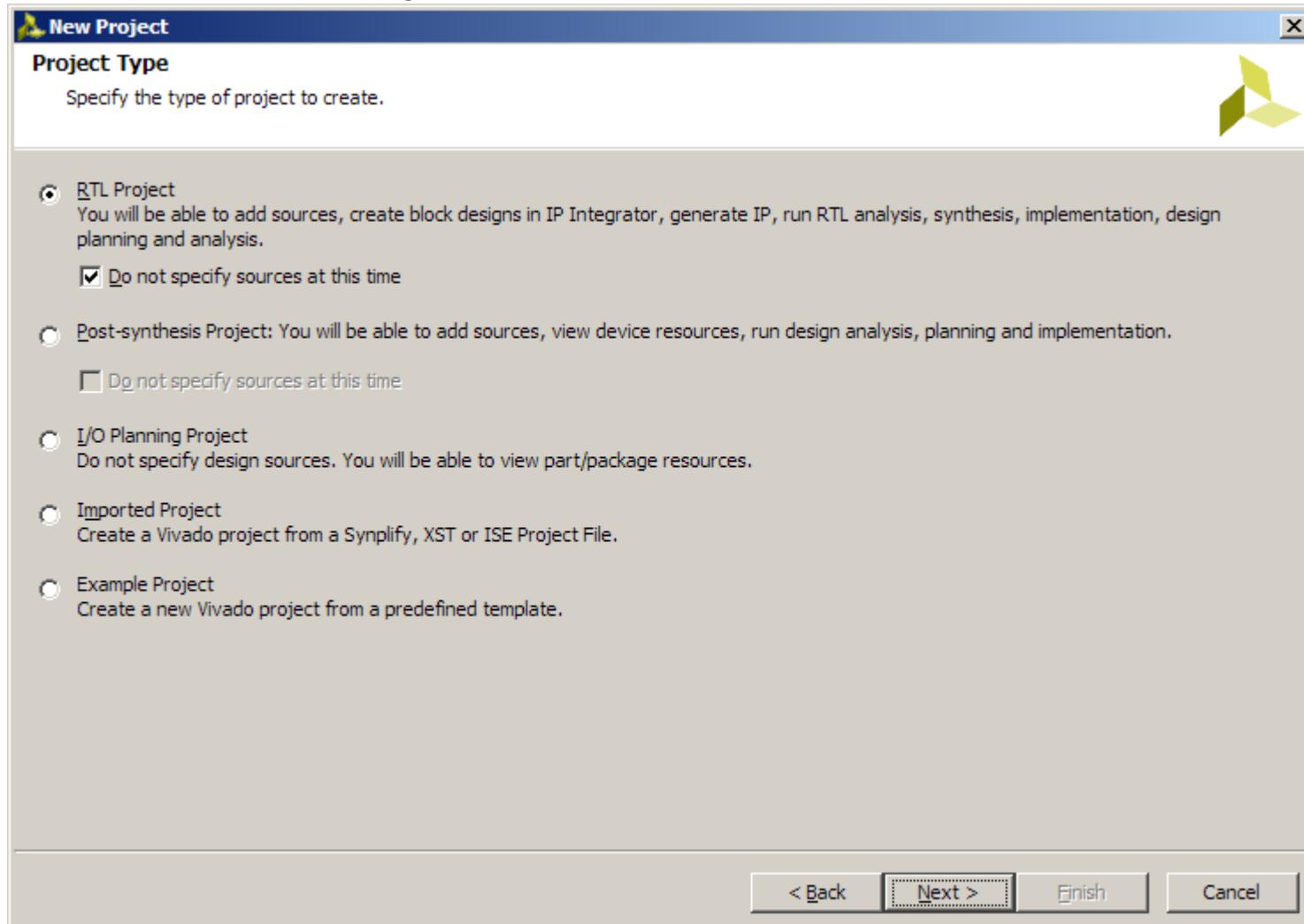
Note: Vivado generally requires forward slashes in paths

 XILINX  ALL PROGRAMMABLE™

# Create IBERT Design for Bank 113

## ► Select RTL Project

- Select **Do not specify sources at this time**



# Create IBERT Design for Bank 113

## ► Select the VC707 Board

The screenshot shows the 'New Project' dialog with the title 'Default Part'. It prompts the user to choose a default Xilinx part or board for their project, stating that this can be changed later. The interface includes a 'Select' dropdown set to 'Boards', a 'Parts' icon, and a 'Boards' icon. Below are filter options for 'Vendor' (All), 'Display Name' (All), and 'Board Rev' (Latest), along with a 'Reset All Filters' button. A search bar with a magnifying glass icon is also present. The main area displays a table of evaluation boards:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Avail IOBs
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484	1.3	200
Artix-7 AC701 Evaluation Platform	xilinx.com	1.1	xc7a200tfgb676-2	676	1.2	400
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	xc7k325tffg900-2	900	1.2	500
Kintex-Ultrascale KCU105 Evaluation Platform	xilinx.com	1.0	xcu040-ffva1156-2-e	1,156	1.0	520
<b>Virtex-7 VC707 Evaluation Platform</b>	xilinx.com	<b>1.1</b>	<b>xc7vx485tffg1761-2</b>	<b>1,761</b>	<b>1.2</b>	<b>700</b>
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2	1,761	1.6	850
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.2	200
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	1.1	xc7z045tffg900-2	900	1.2	362

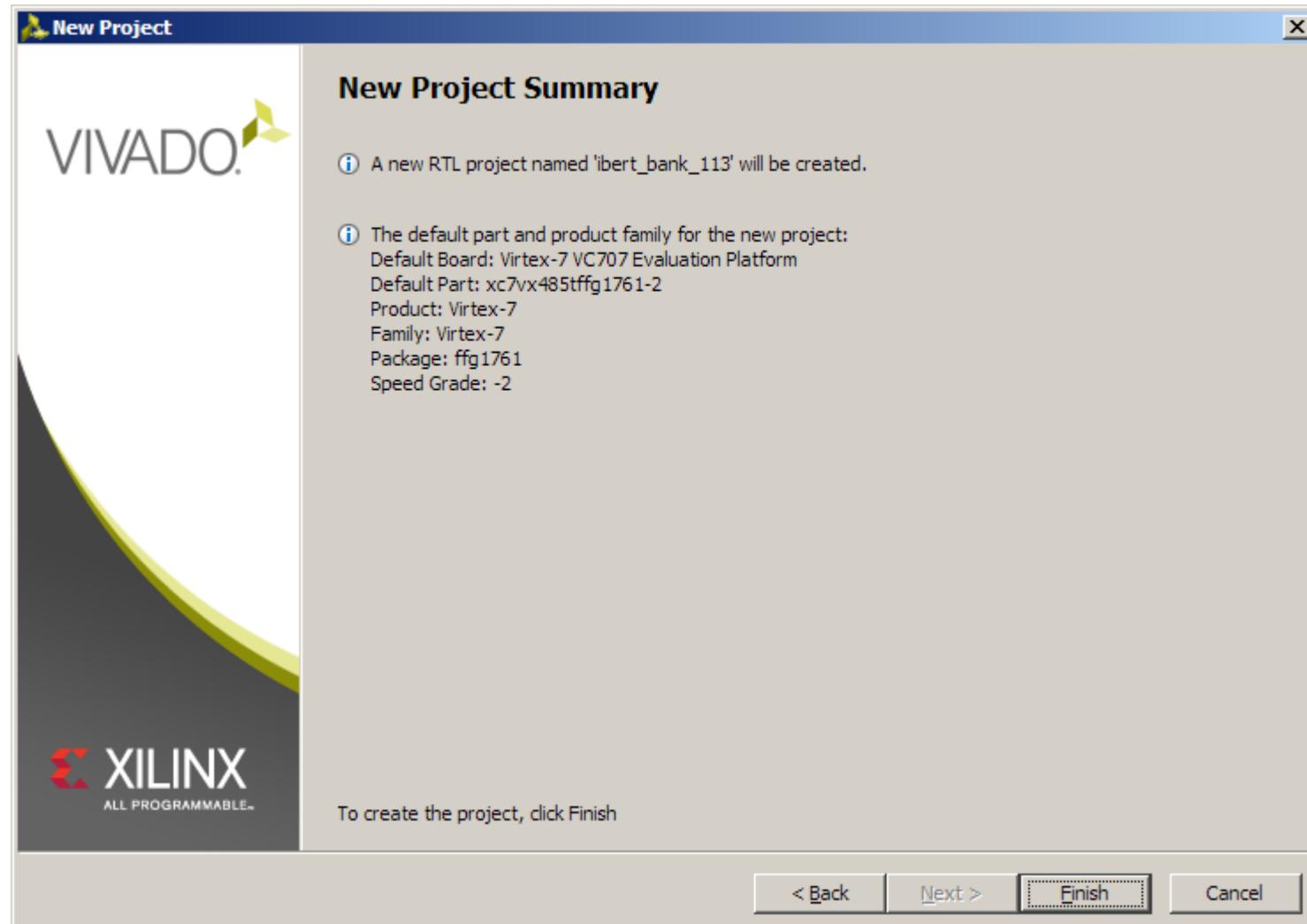
At the bottom are navigation buttons: '< Back', 'Next >', 'Finish', and 'Cancel'.

Note: Presentation applies to the VC707

XILINX ALL PROGRAMMABLE™

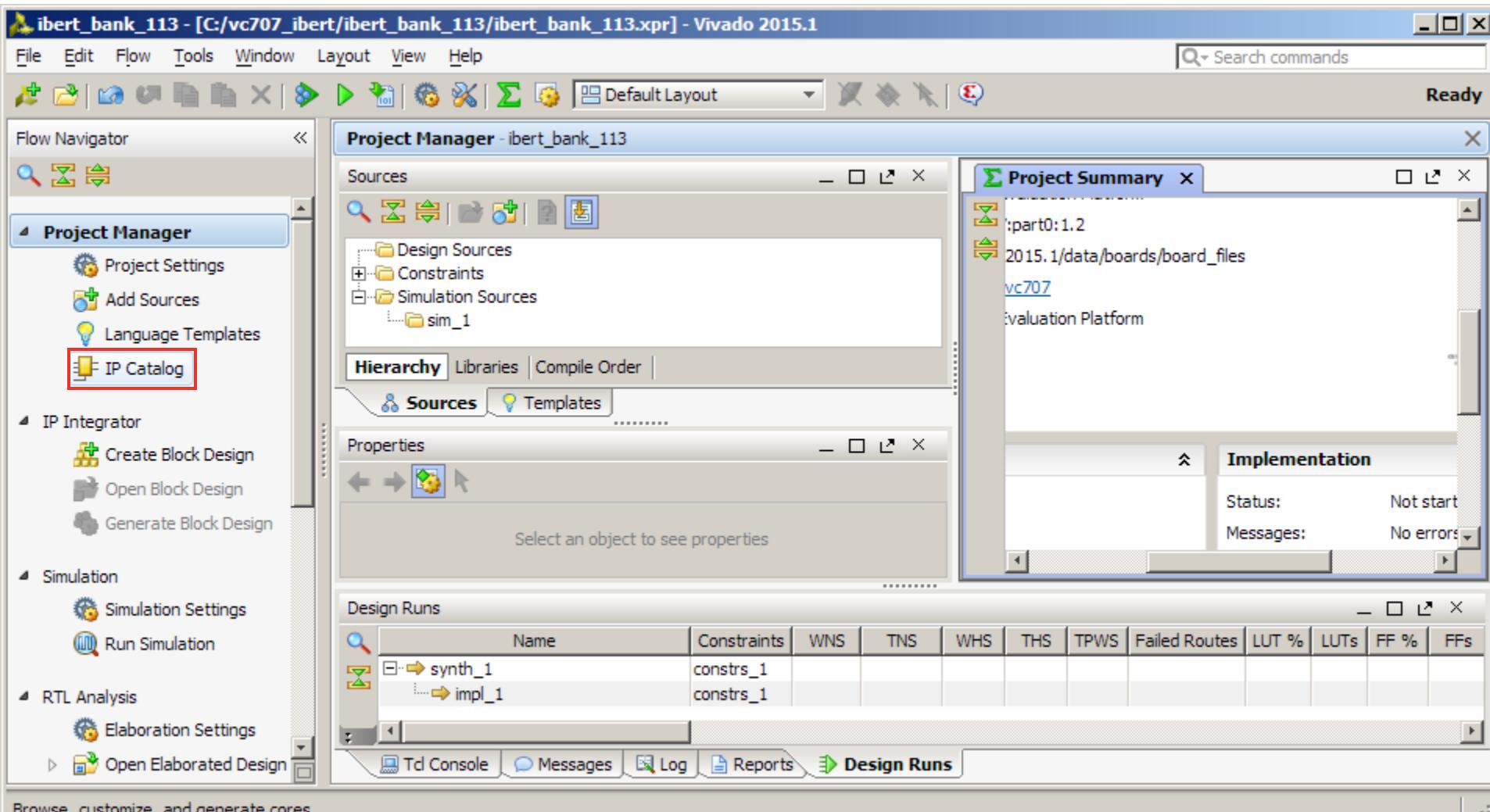
# Create IBERT Design for Bank 113

► Click Finish



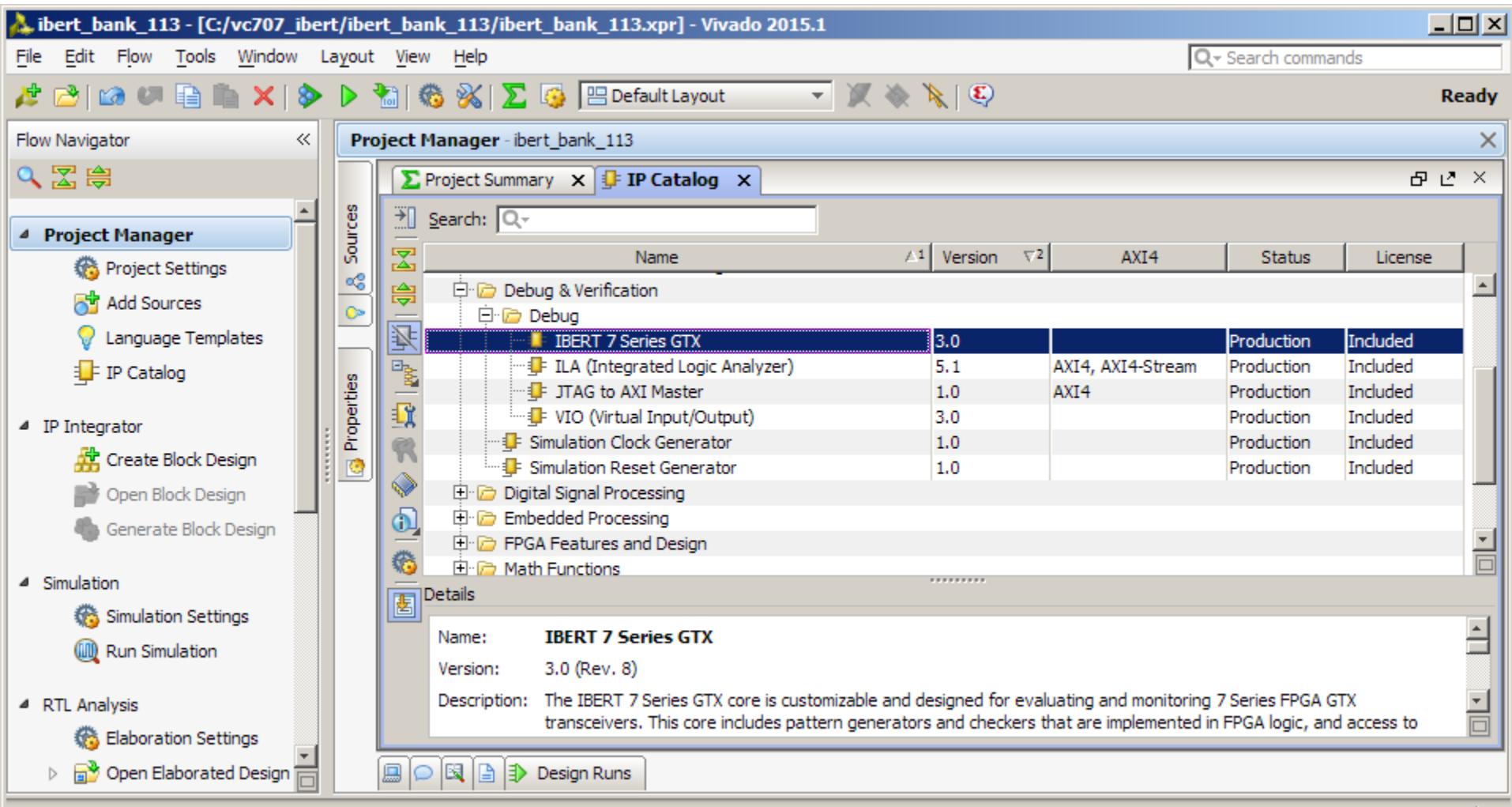
# Create IBERT Design for Bank 113

► Click on IP Catalog



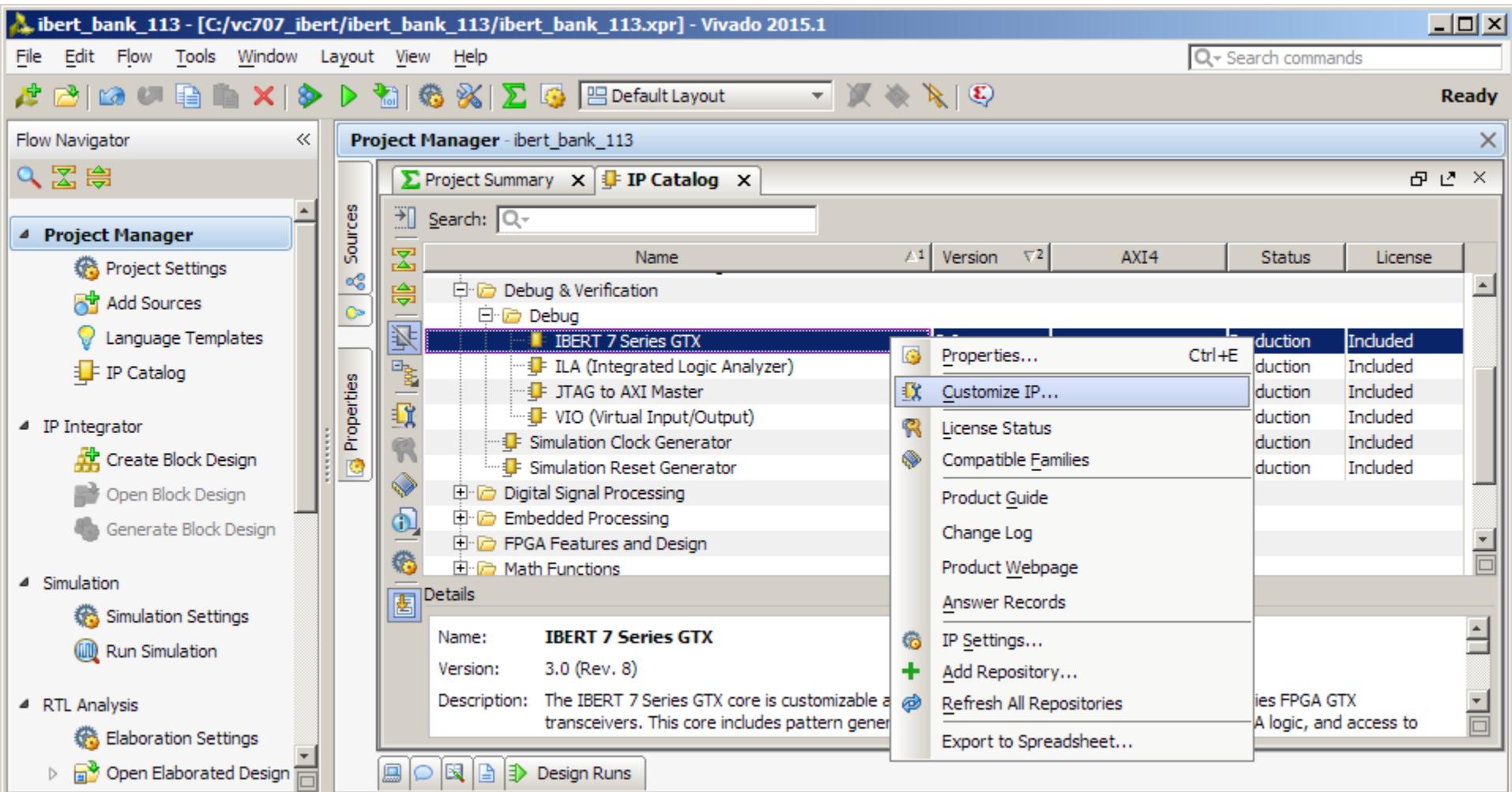
# Create IBERT Design for Bank 113

► Select IBERT 7 Series GTX, v3.0 under Debug & Verification



# Create IBERT Design for Bank 113

► Right click on IBERT 7 Series GTX and select Customize IP...



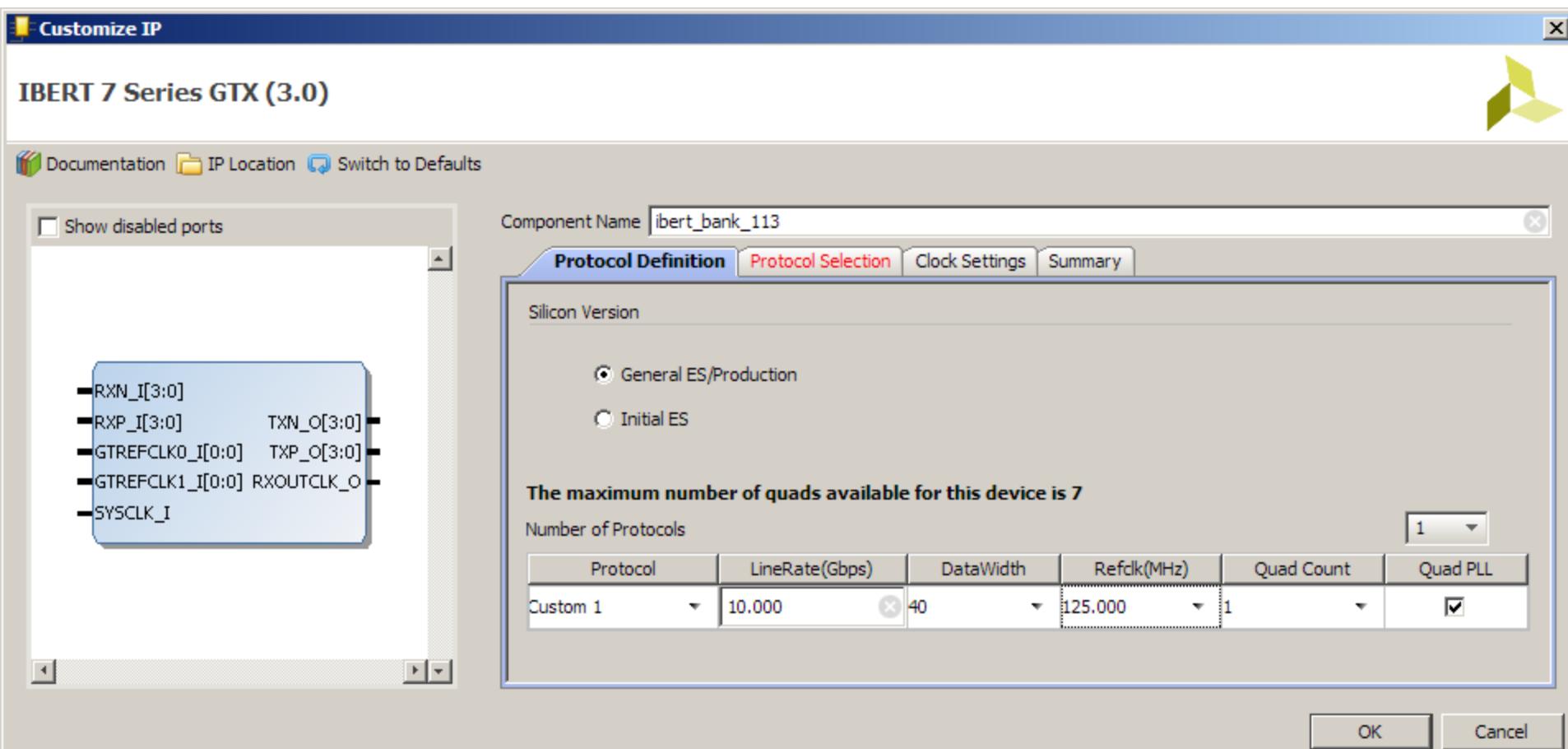
Customize the selected core

Note: Presentation applies to the VC707

XILINX ➤ ALL PROGRAMMABLE

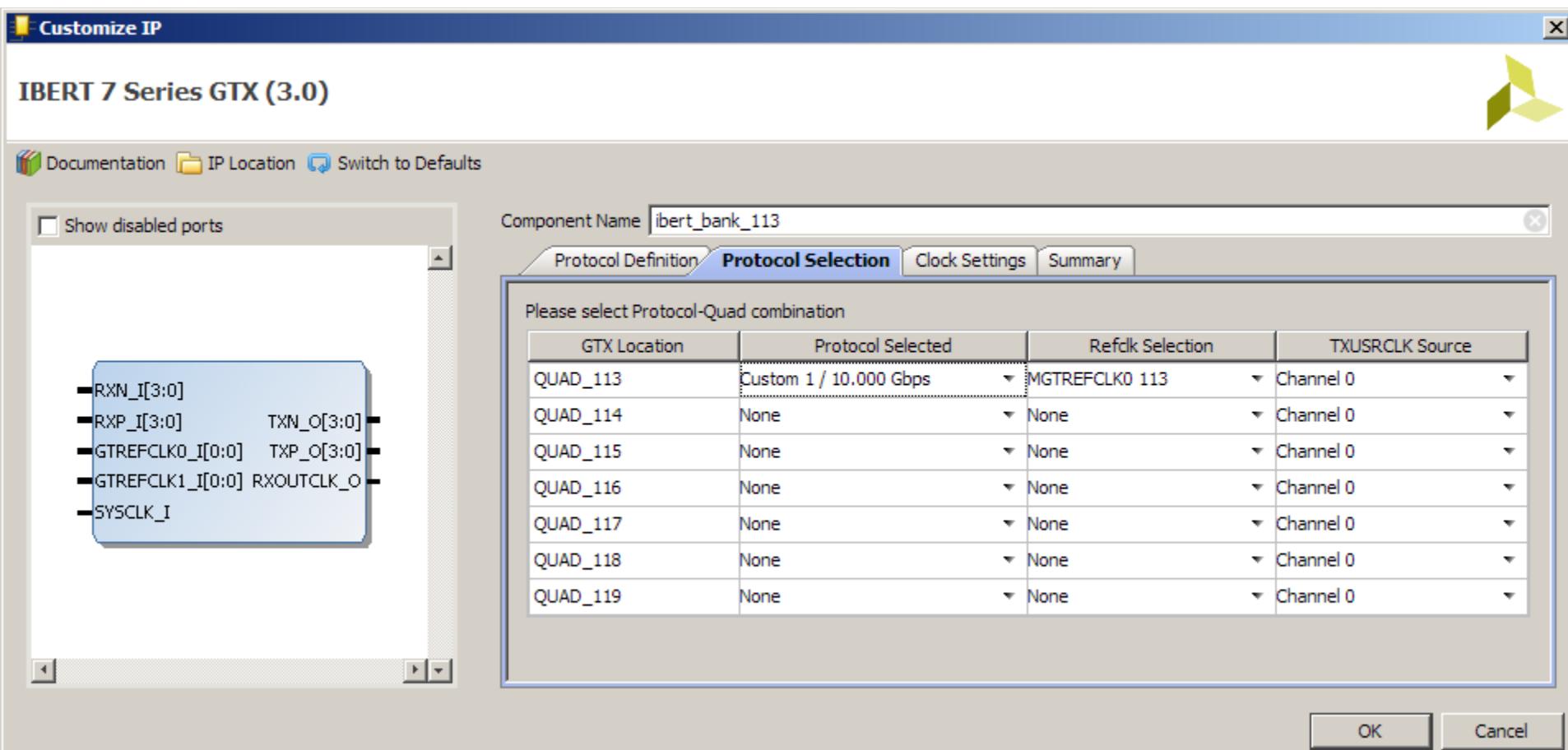
# Create IBERT Design for Bank 113

- Set the Component name: **ibert\_bank\_113**
- Under the Protocol Definition tab
  - Silicon Version: **General ES / Production**
  - Protocol: LineRate: **10.000**, DataWidth: **40** Refclk: **125.000** Quad Count: **1**



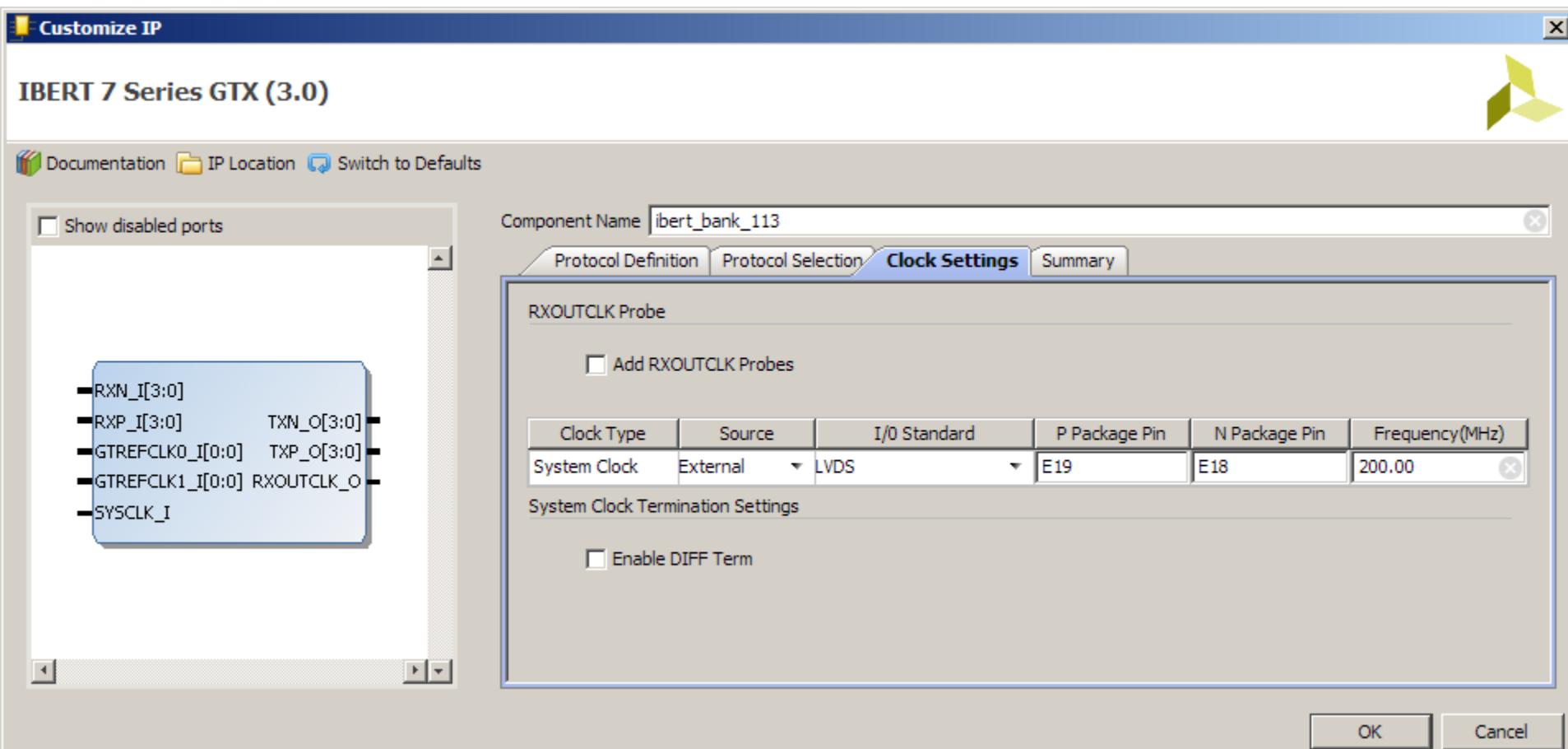
# Create IBERT Design for Bank 113

- Under the Protocol Selection tab
- Set QUAD\_113 to
  - Custom 1 / 10.000 Gbps, and MGTRREFCLK0 113



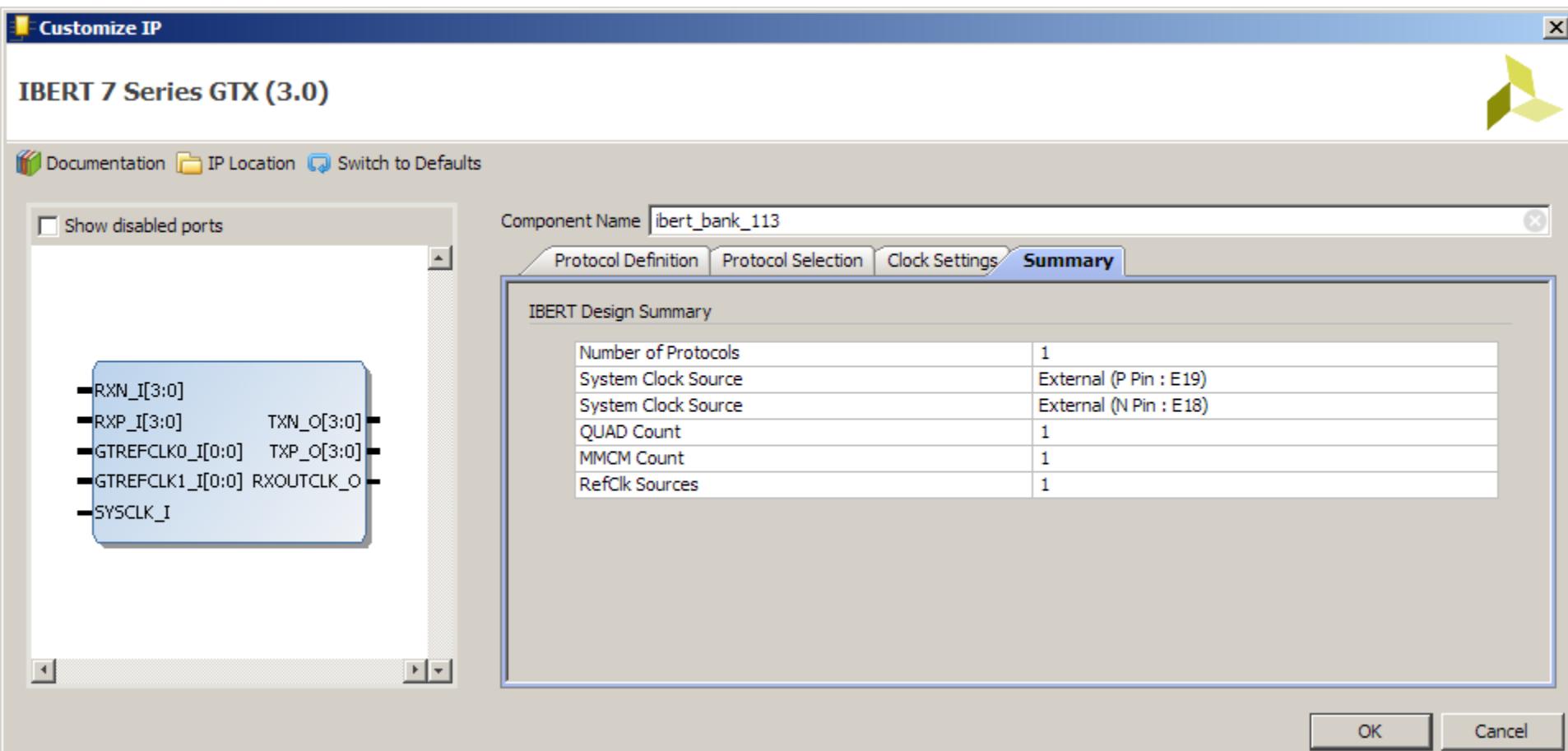
# Create IBERT Design for Bank 113

- Under the Clock Settings tab, set the System Clock:
  - LVDS, P Pin Location: **E19**, N Pin Location: **E18**



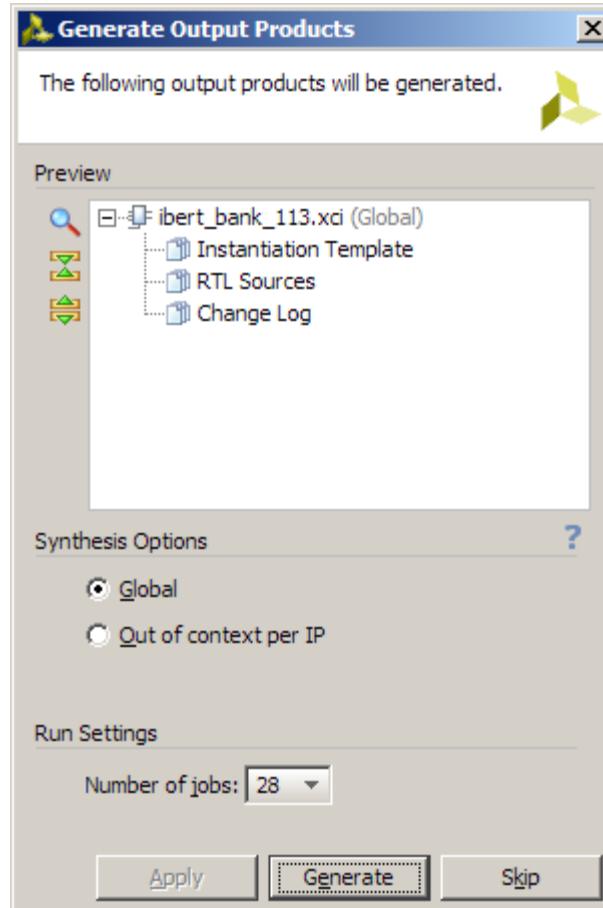
# Create IBERT Design for Bank 113

► Review the summary and click OK



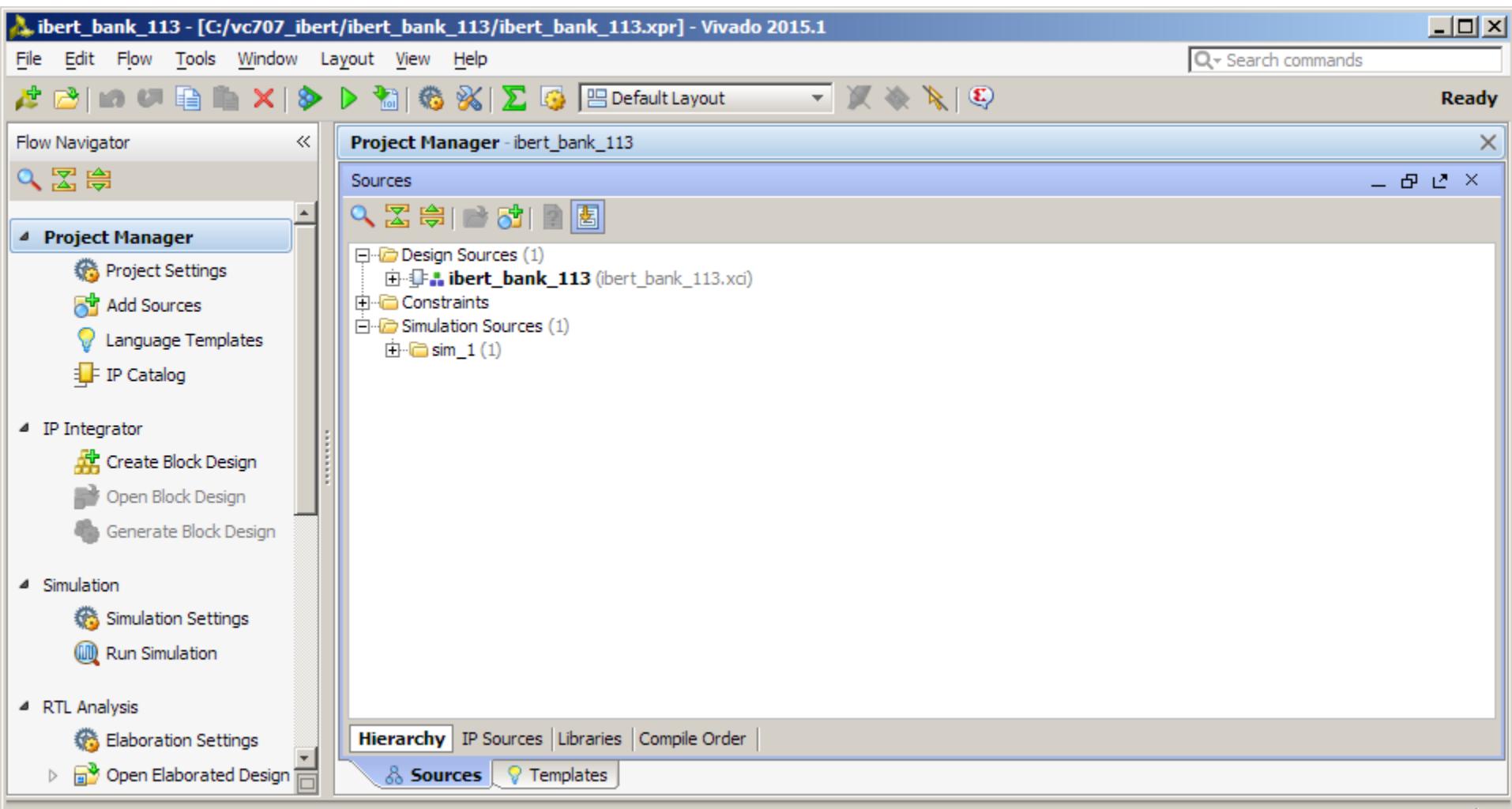
# Create IBERT Design for Bank 113

► Click Generate



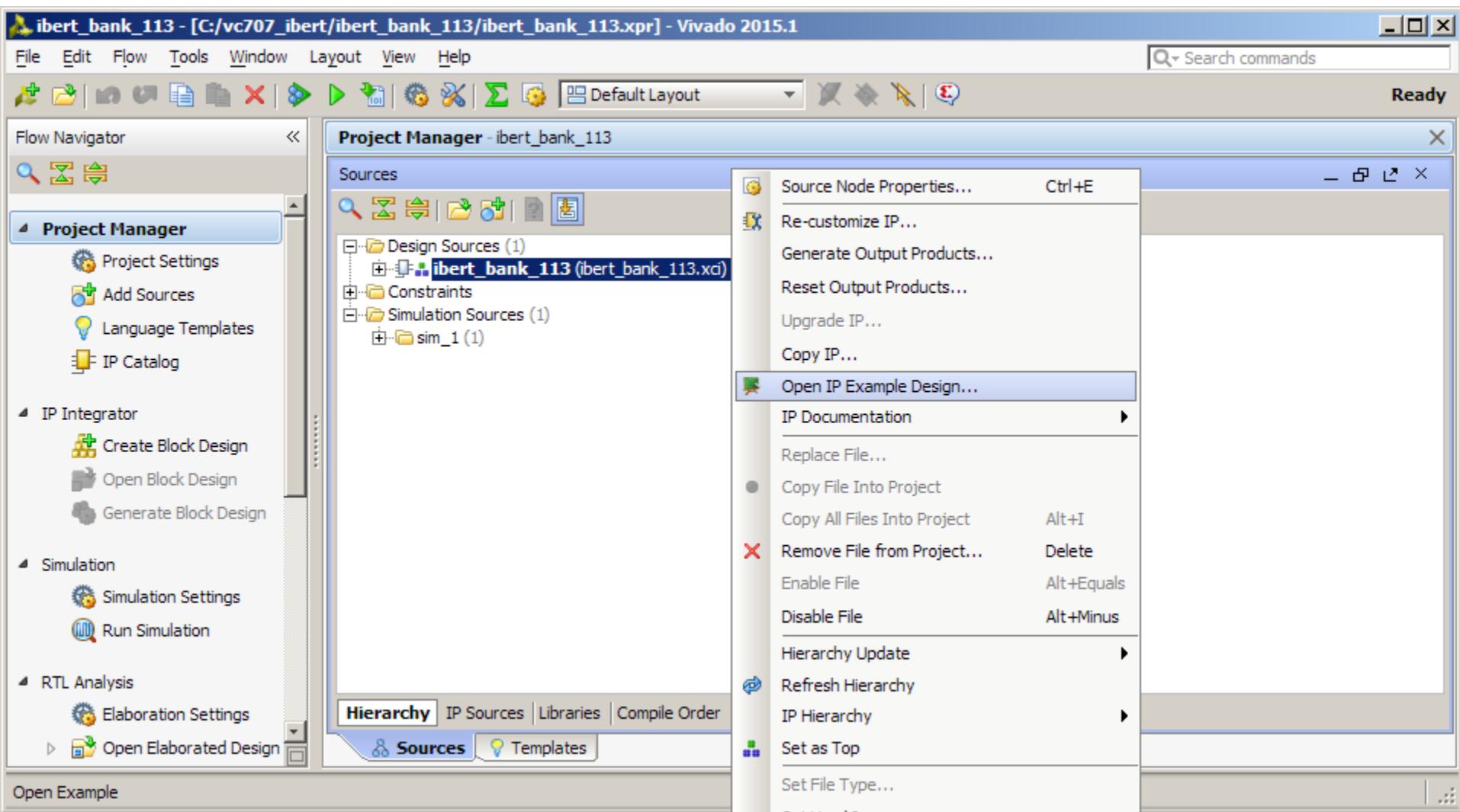
# Create IBERT Design for Bank 113

► Bank 113 IBERT design appears in Design Sources



# Compile Example Design

► Right click on ibert\_bank\_113 and select Open IP Example Design...

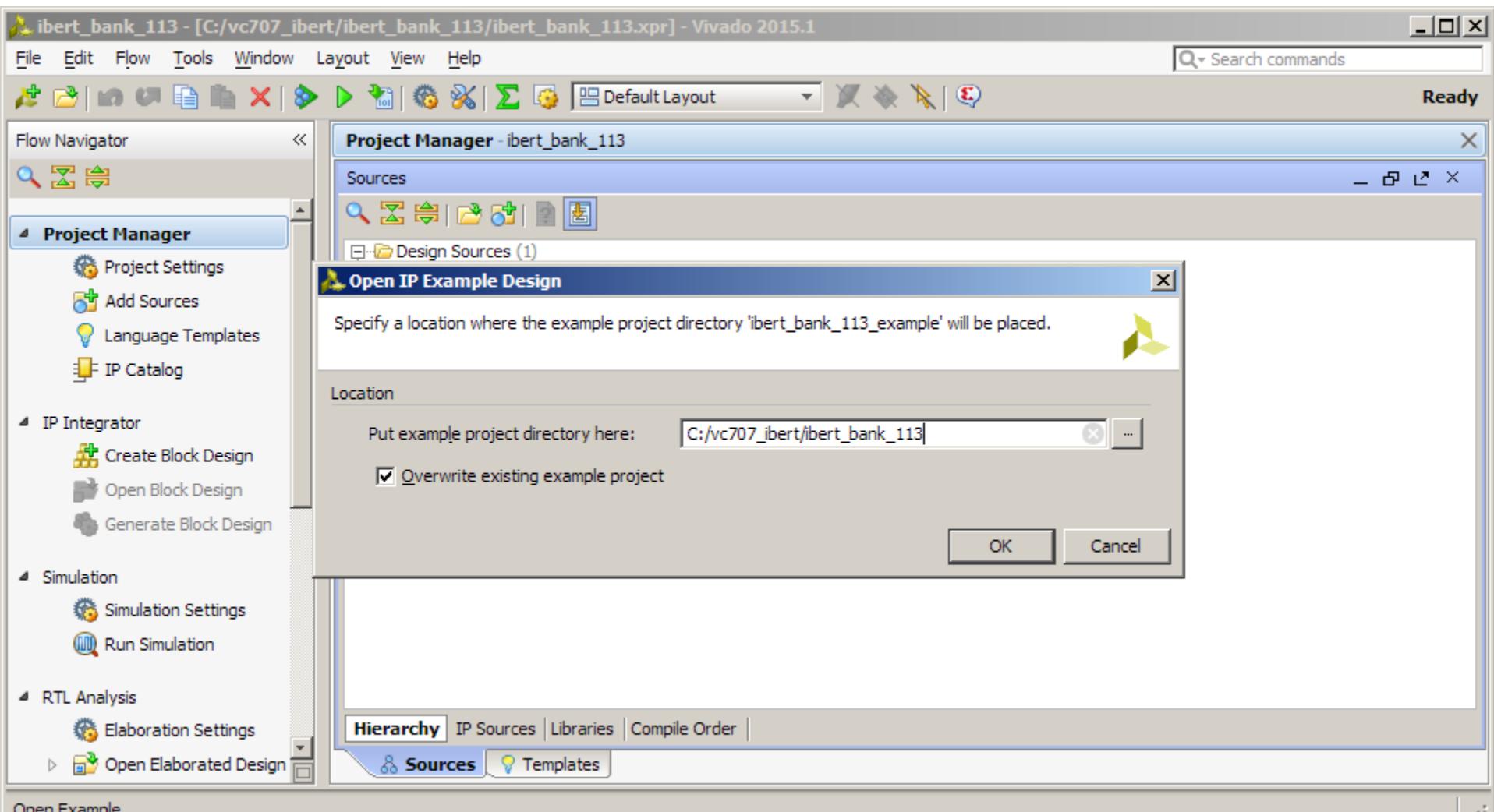


Note: Presentation applies to the VC707

XILINX ➤ ALL PROGRAMMABLE™

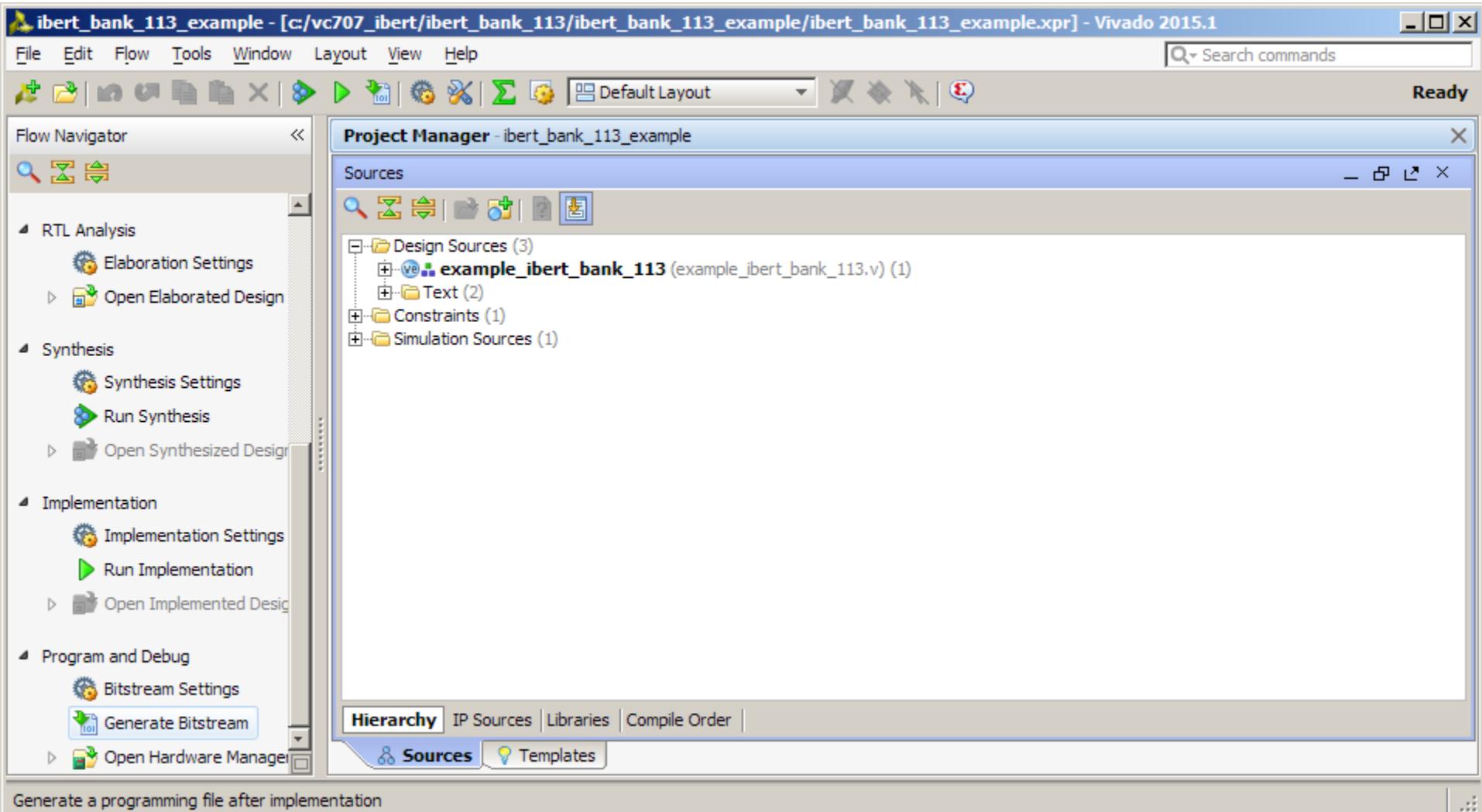
# Compile Example Design

► Set the location to C:/vc707\_ibert/ibert\_bank\_113 and click OK



# Compile Example Design

- A new project is created
- Click Generate Bitstream

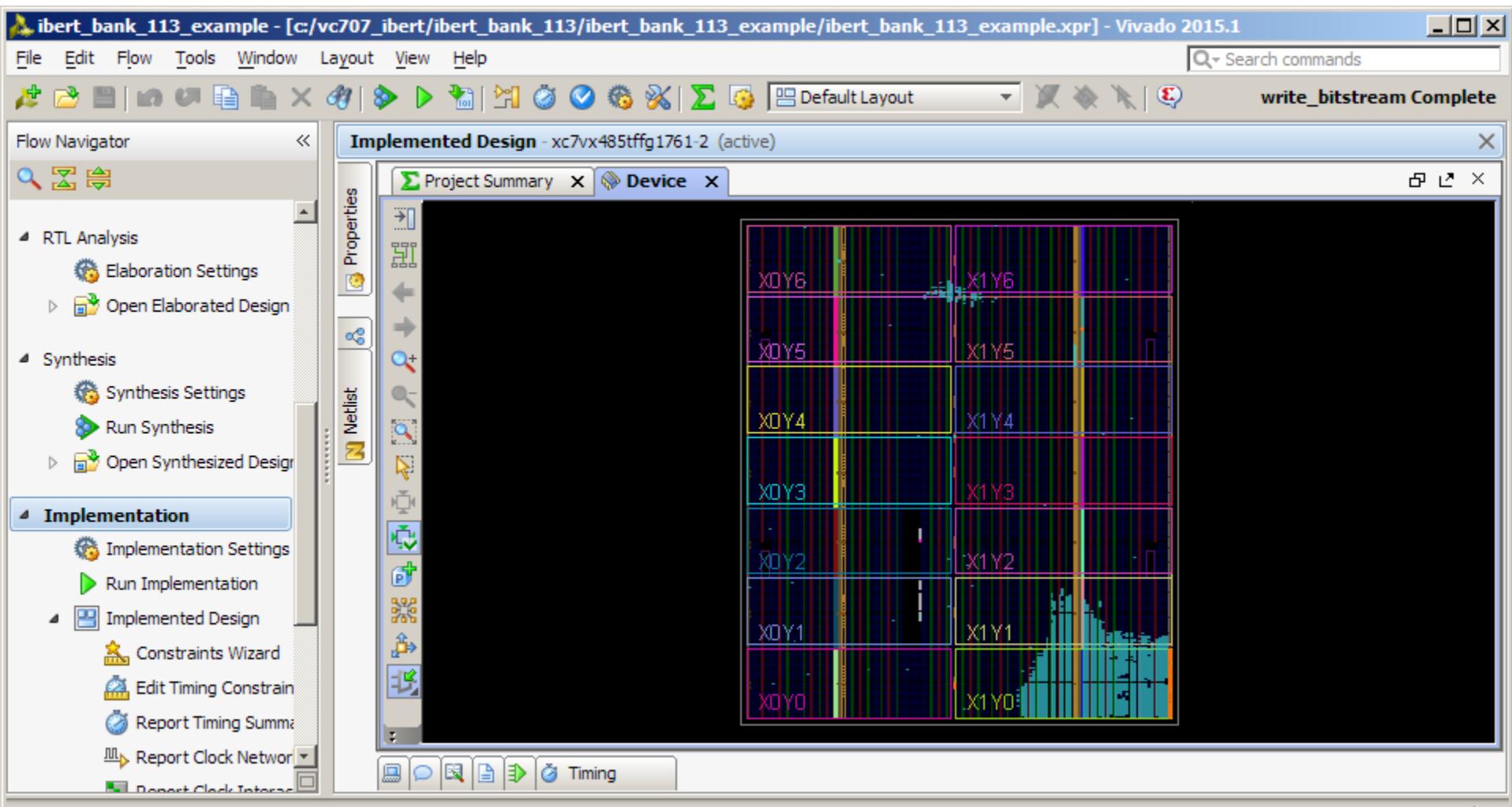


Note: The original project window can be closed

XILINX ➤ ALL PROGRAMMABLE™

# Compile Example Design

► Open and view the Implemented Design



# **Testing Bank 113 with Optional User Provided Hardware**

# Optional Testing with User Provided Hardware

## ► SMA Cables

- [www.rosenbergerna.com](http://www.rosenbergerna.com)
- Part number:  
72D-32S1-32S1-00610A



## ► SMA Quick connects

- RADIALL
- Part number: R125791501
- Available [here](#) or [here](#)



# Optional Testing with User Provided Hardware

## ► Connect Optical Loopback Adapter

- [www.molex.com](http://www.molex.com)
- SFP Loopback Adapter,  
5.0 db Attenuation
- Part # [74765-0904](#)

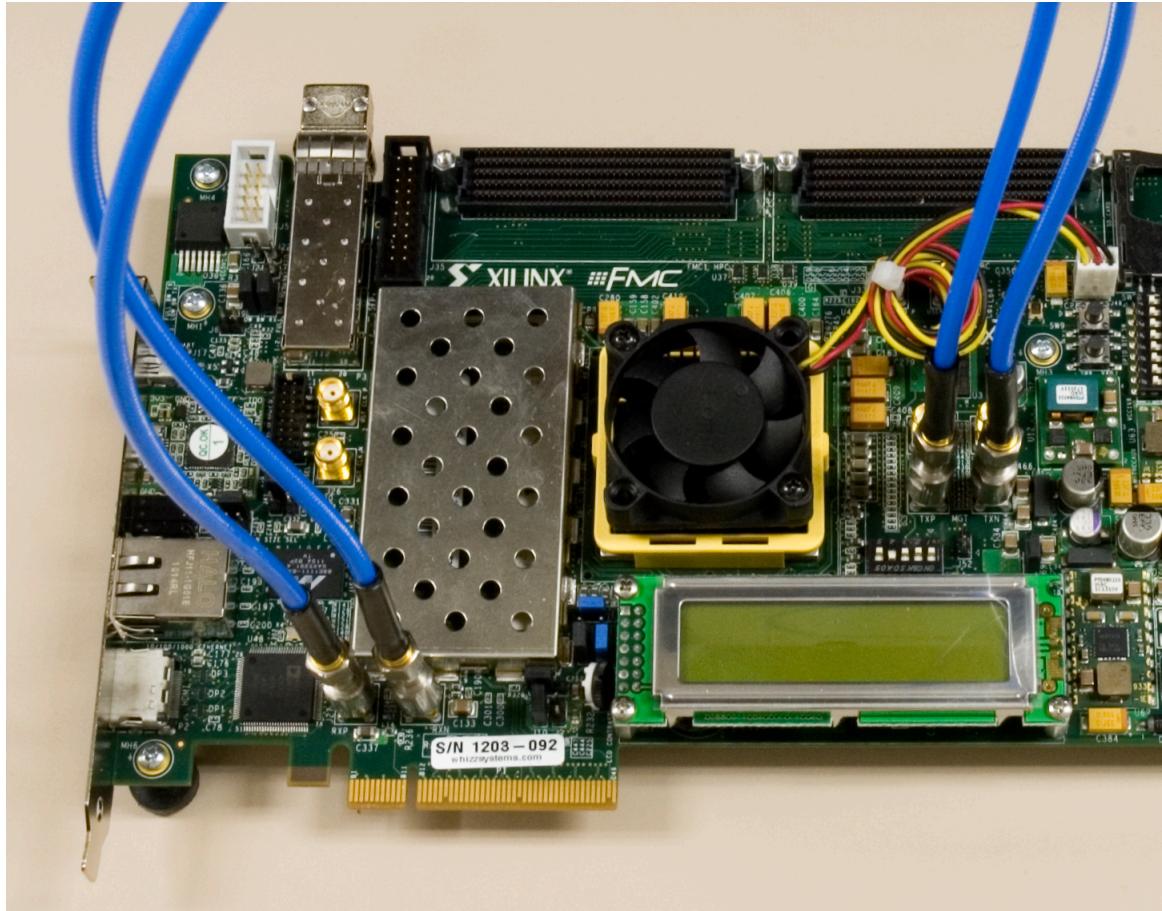


# Optional Testing with User Provided Hardware

## ► Testing Bank 113

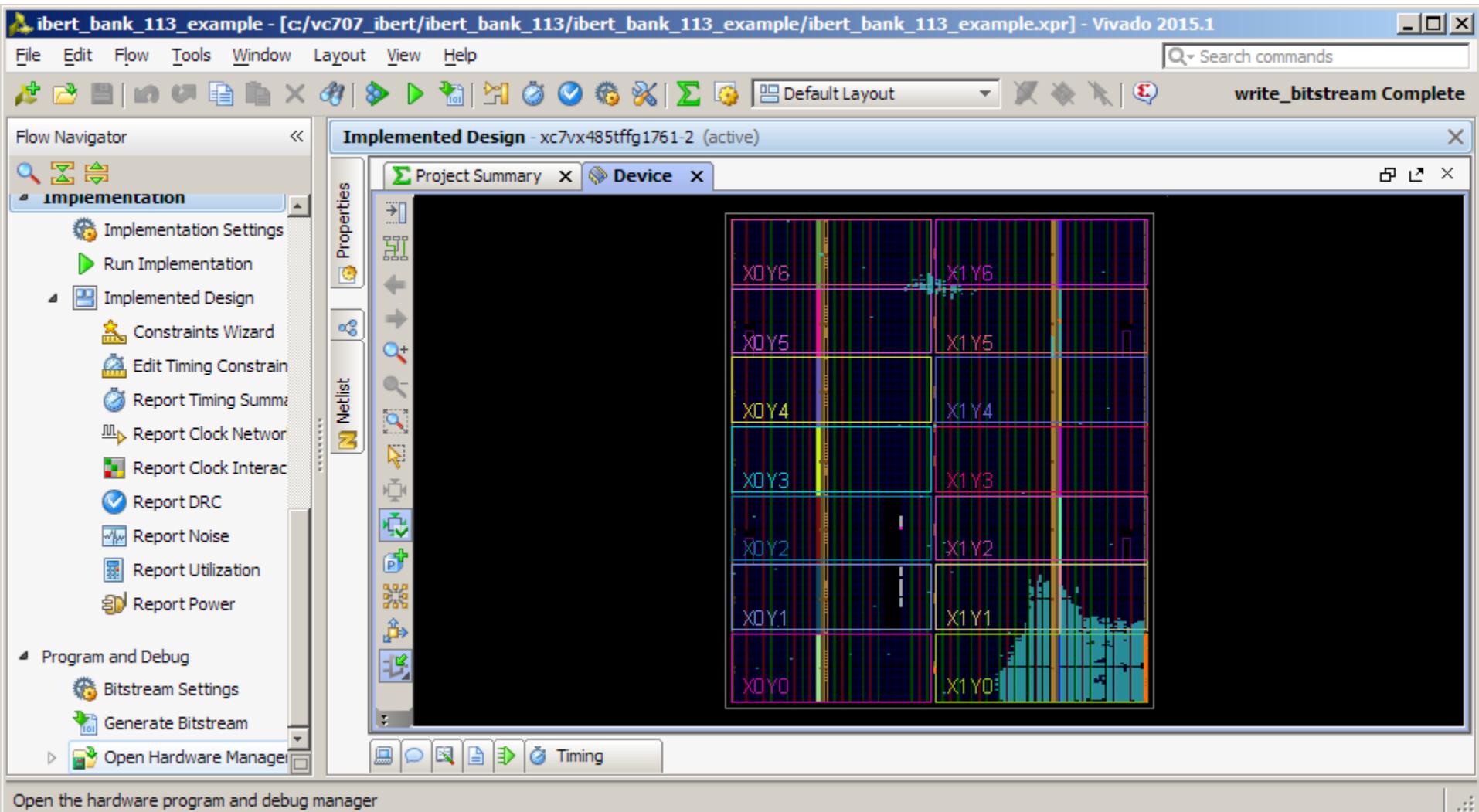
- Insert SFP Loopback adapter
- Connect SMA cables:
  - J30 to J28
  - J29 to J27

## ► Power on the VC707 board



# Run IBERT Example Design

► Click Open Hardware Manager



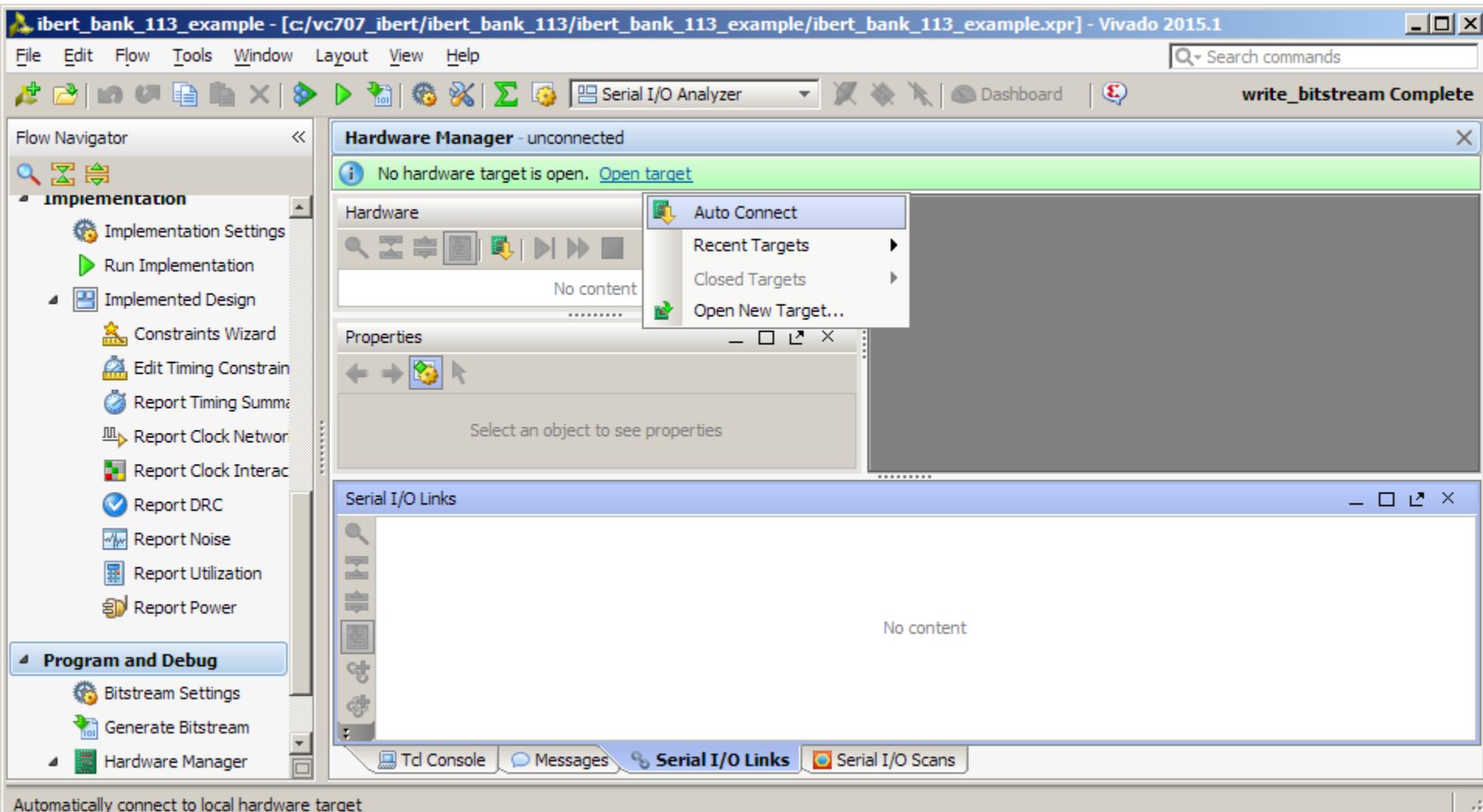
Open the hardware program and debug manager

Note: Presentation applies to the VC707

XILINX ➤ ALL PROGRAMMABLE™

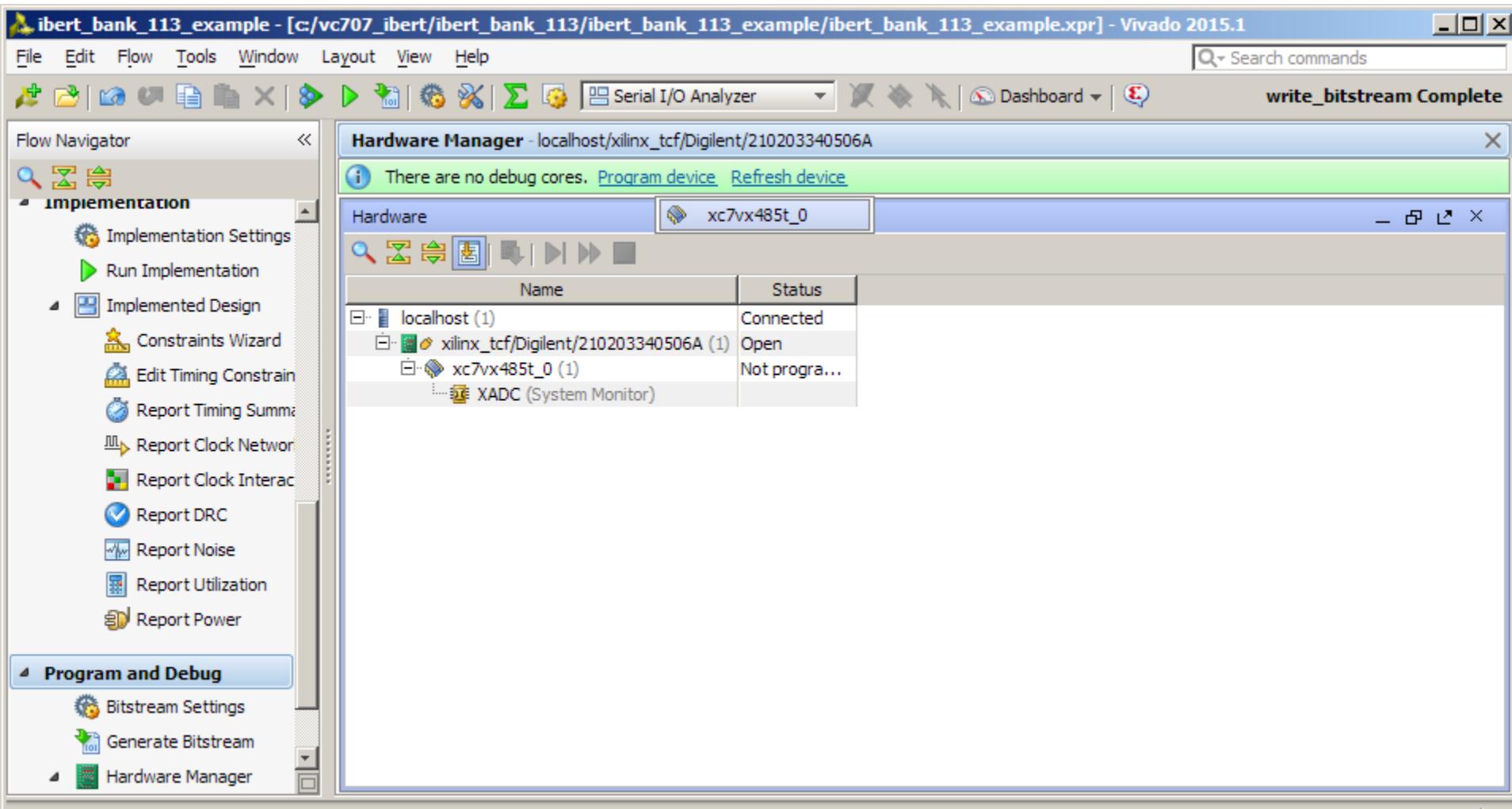
# Run IBERT Example Design

► Click Open target and select Auto Connect



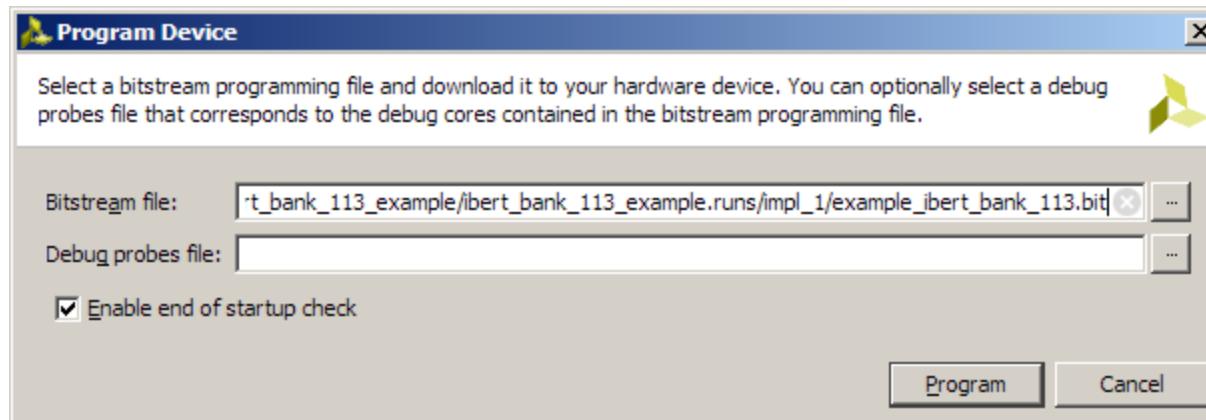
# Run IBERT Example Design

► Select Program device → xc7vx485t\_0



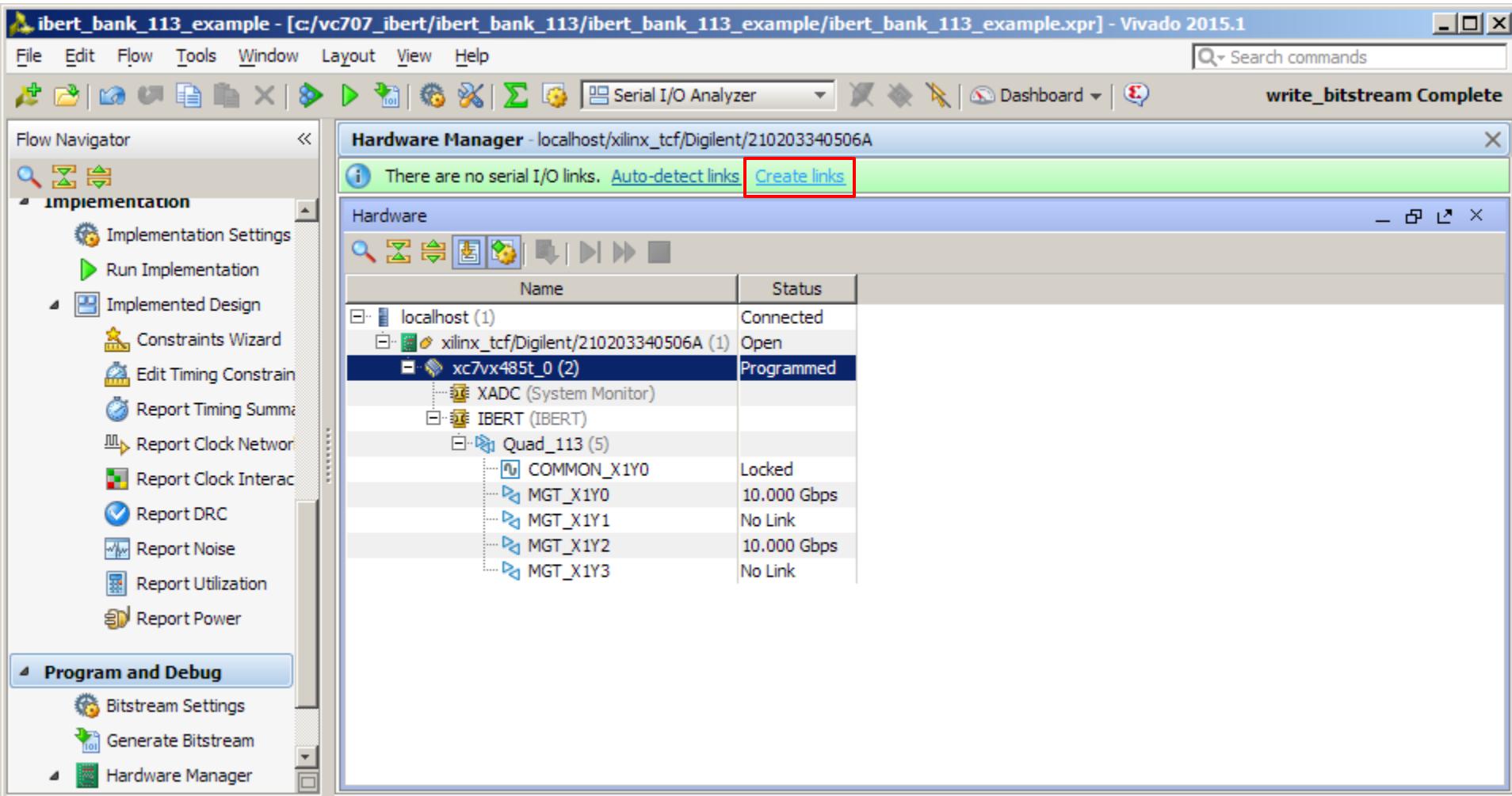
# Run IBERT Example Design

- The newly created bitstream is default
- Click Program



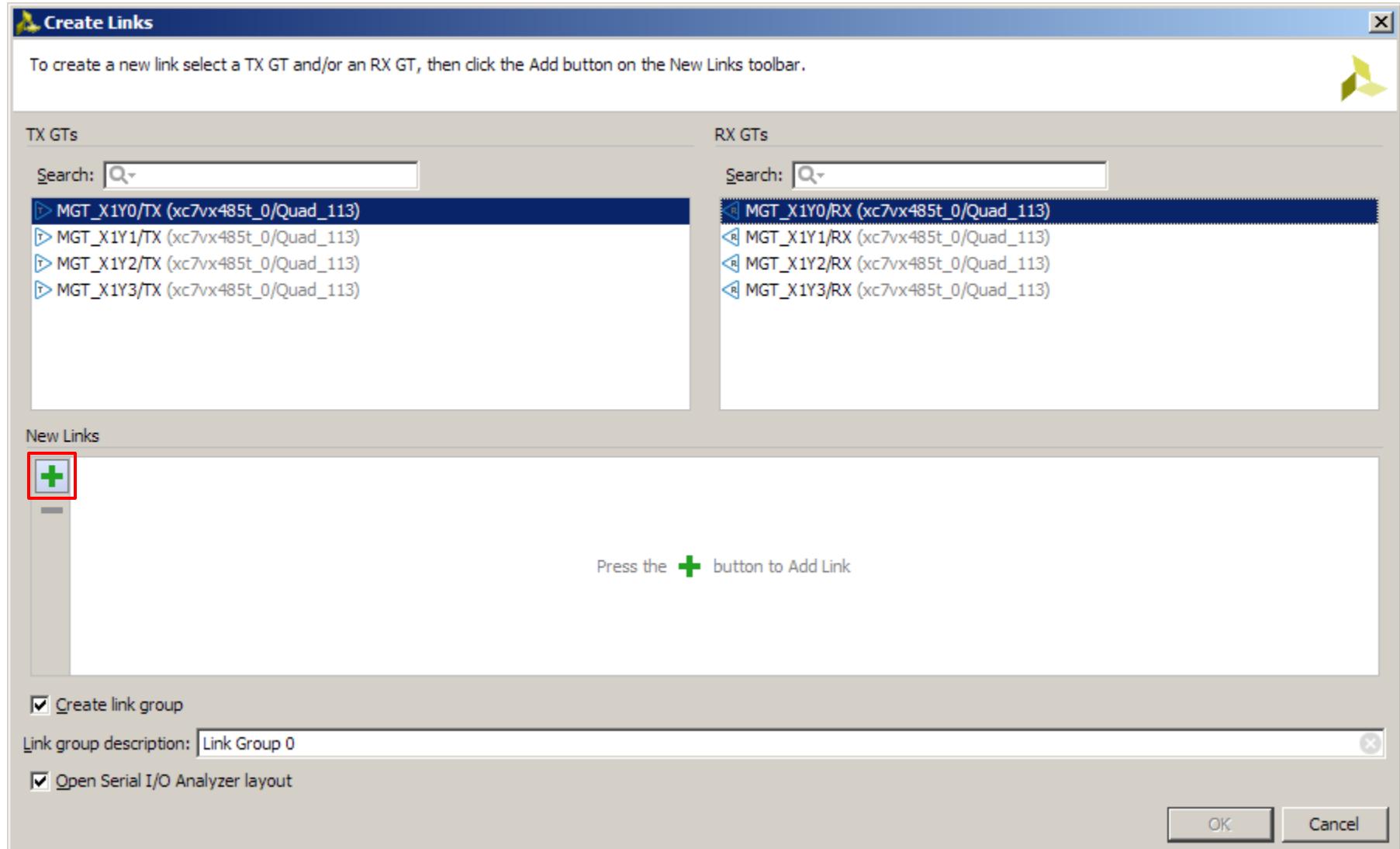
# Run IBERT Example Design

- Quad\_113 shows Locked
- Click Create links



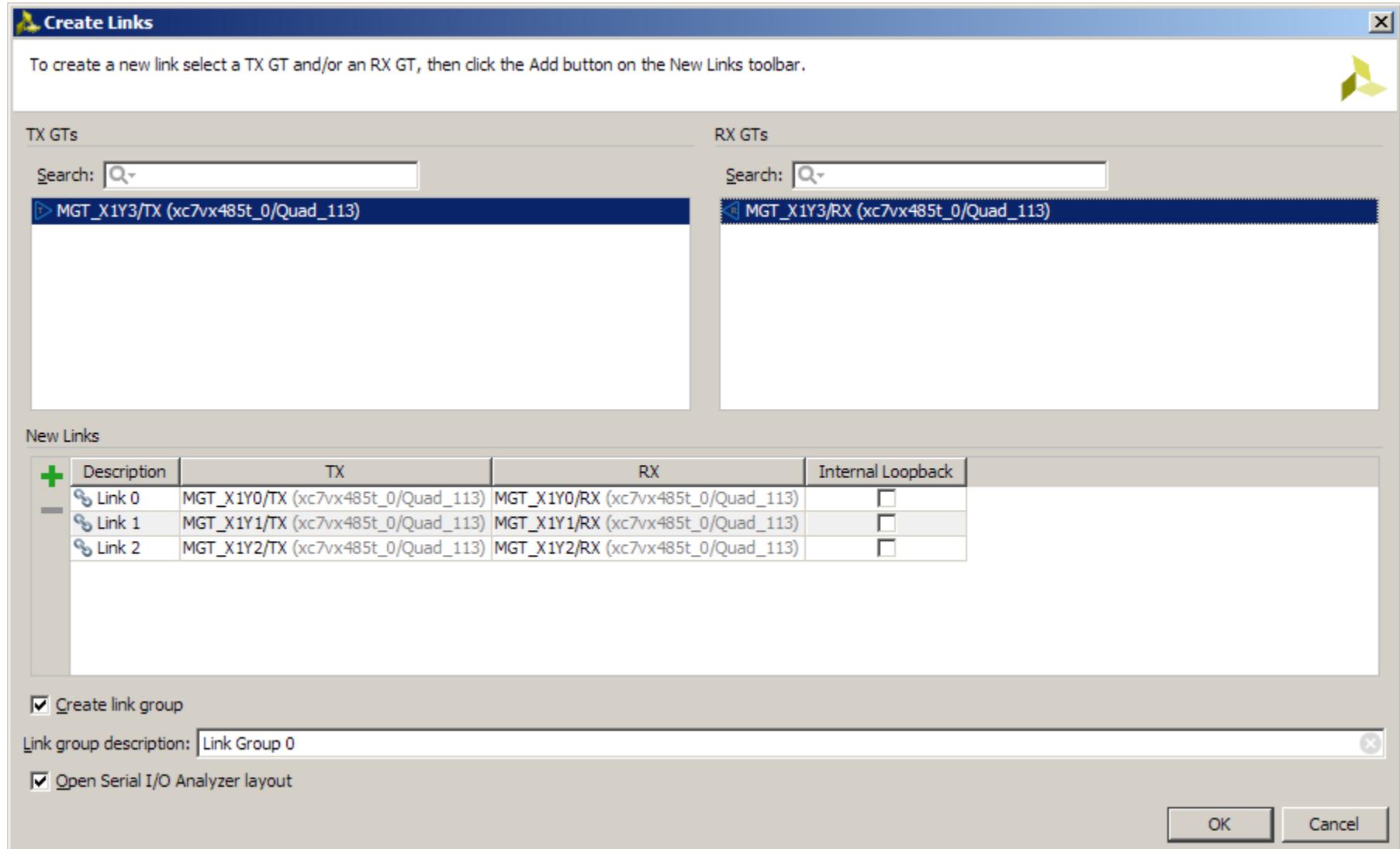
# Run IBERT Example Design

► Click on the Add Link button until the first three MGT pairs are “linked”



# Run IBERT Example Design

► Leave the last link alone, then click OK



# Run IBERT Example Design

► The IBERT data appears as seen below

The screenshot shows the Vivado 2015.1 Hardware Manager window titled "ibert\_bank\_113\_example - [c:/vc707\_ibert/ibert\_bank\_113/ibert\_bank\_113\_example/ibert\_bank\_113\_example.xpr] - Vivado 2015.1". The main area displays the "Serial I/O Links" table. The table has columns: Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and a final column partially visible. The table data is as follows:

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	
Ungrouped Links (0)											
Link Group 0 (3)											
Link 0	MGT_X1Y0/TX	MGT_X1Y0/RX	10.000 Gbps	3.176E12	6.297E11	1.983E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.6
Link 1	MGT_X1Y1/TX	MGT_X1Y1/RX	No Link	3.176E12	1.631E12	5.134E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.6
Link 2	MGT_X1Y2/TX	MGT_X1Y2/RX	10.000 Gbps	3.176E12	0E0	3.149E-13	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.6

# Run IBERT Example Design

- ▶ Set the TX and RX Pattern to PRBS 31-bit

The screenshot shows the Vivado 2015.1 Hardware Manager interface for the "ibert\_bank\_113\_example" project. The main window displays the "Serial I/O Links" table. The table has columns for Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and TX Post-Cursor. There are three link groups: "Link Group 0 (3)" containing "Link 0", "Link 1", and "Link 2". "Link 0" and "Link 2" have "MGT\_X1Y0/TX" and "MGT\_X1Y0/RX" assignments respectively, while "Link 1" has "MGT\_X1Y1/TX" and "MGT\_X1Y1/RX". "Link 0" and "Link 2" are connected to "10.000 Gbps" and "3.361E12" bits respectively, while "Link 1" is "No Link" and has "3.362E12" bits. "Link 0" has "6.297E11" errors, "1.874E-1" BER, and a "Reset" button. "Link 1" has "1.726E12" errors, "5.134E-1" BER, and a "Reset" button. "Link 2" has "0E0" errors, "2.975E-13" BER, and a "Reset" button. The TX Pattern for "Link 0" is currently set to "PRBS 7-bit", but a dropdown menu shows options: "PRBS 31-bit", "Fast Clk", and "Slow Clk". The RX Pattern for "Link 0" is "PRBS 7-bit". The TX Pre-Cursor for "Link 0" is "1.67 dB (00111)" and the TX Post-Cursor is "0.6". The RX Pre-Cursor for "Link 0" is "1.67 dB (00111)" and the RX Post-Cursor is "0.6". The TX Pre-Cursor for "Link 1" is "1.67 dB (00111)" and the TX Post-Cursor is "0.6". The RX Pre-Cursor for "Link 1" is "1.67 dB (00111)" and the RX Post-Cursor is "0.6". The TX Pre-Cursor for "Link 2" is "1.67 dB (00111)" and the TX Post-Cursor is "0.6". The RX Pre-Cursor for "Link 2" is "1.67 dB (00111)" and the RX Post-Cursor is "0.6".

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	RX Pre-Cursor
Ungrouped Links (0)											
Link Group 0 (3)								Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111) 0.6
Link 0	MGT_X1Y0/TX	MGT_X1Y0/RX	10.000 Gbps	3.361E12	6.297E11	1.874E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111) 0.6	
Link 1	MGT_X1Y1/TX	MGT_X1Y1/RX	No Link	3.362E12	1.726E12	5.134E-1	Reset	PRBS 15-bit	PRBS 7-bit	1.67 dB (00111) 0.6	
Link 2	MGT_X1Y2/TX	MGT_X1Y2/RX	10.000 Gbps	3.362E12	0E0	2.975E-13	Reset	PRBS 23-bit	PRBS 7-bit	1.67 dB (00111) 0.6	
								PRBS 31-bit			
								Fast Clk			
								Slow Clk			

Link Group: Link Group 0

Note: Presentation applies to the VC707

XILINX ➤ ALL PROGRAMMABLE™

# Run IBERT Example Design

- Now all three links are set to a RX Pattern of PRBS 31-bit
- Scroll to the right to view the Loopback Mode

The screenshot shows the Vivado 2015.1 Hardware Manager interface with the title bar "ibert\_bank\_113\_example - [c:/vc707\_ibert/ibert\_bank\_113/ibert\_bank\_113\_example/ibert\_bank\_113\_example.xpr] - Vivado 2015.1". The main window displays the "Hardware Manager - localhost/xilinx\_tcf/Digilent/210203340506A" tab. The "Serial I/O Links" table lists three links under "Link Group 0": Link 0 (MGT\_X1Y0/TX to MGT\_X1Y0/RX), Link 1 (MGT\_X1Y1/TX to MGT\_X1Y1/RX), and Link 2 (MGT\_X1Y2/TX to MGT\_X1Y2/RX). The RX Pattern for all three links is set to "PRBS 31-bit".

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	1
Ungrouped Links (0)											
Link Group 0 (3)											
Link 0	MGT_X1Y0/TX	MGT_X1Y0/RX	10.000 Gbps	3.597E12	6.399E11	1.779E-1	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.6
Link 1	MGT_X1Y1/TX	MGT_X1Y1/RX	No Link	3.597E12	1.846E12	5.131E-1	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.6
Link 2	MGT_X1Y2/TX	MGT_X1Y2/RX	10.000 Gbps	3.597E12	1.019E10	2.832E-3	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.6

# Run IBERT Example Design

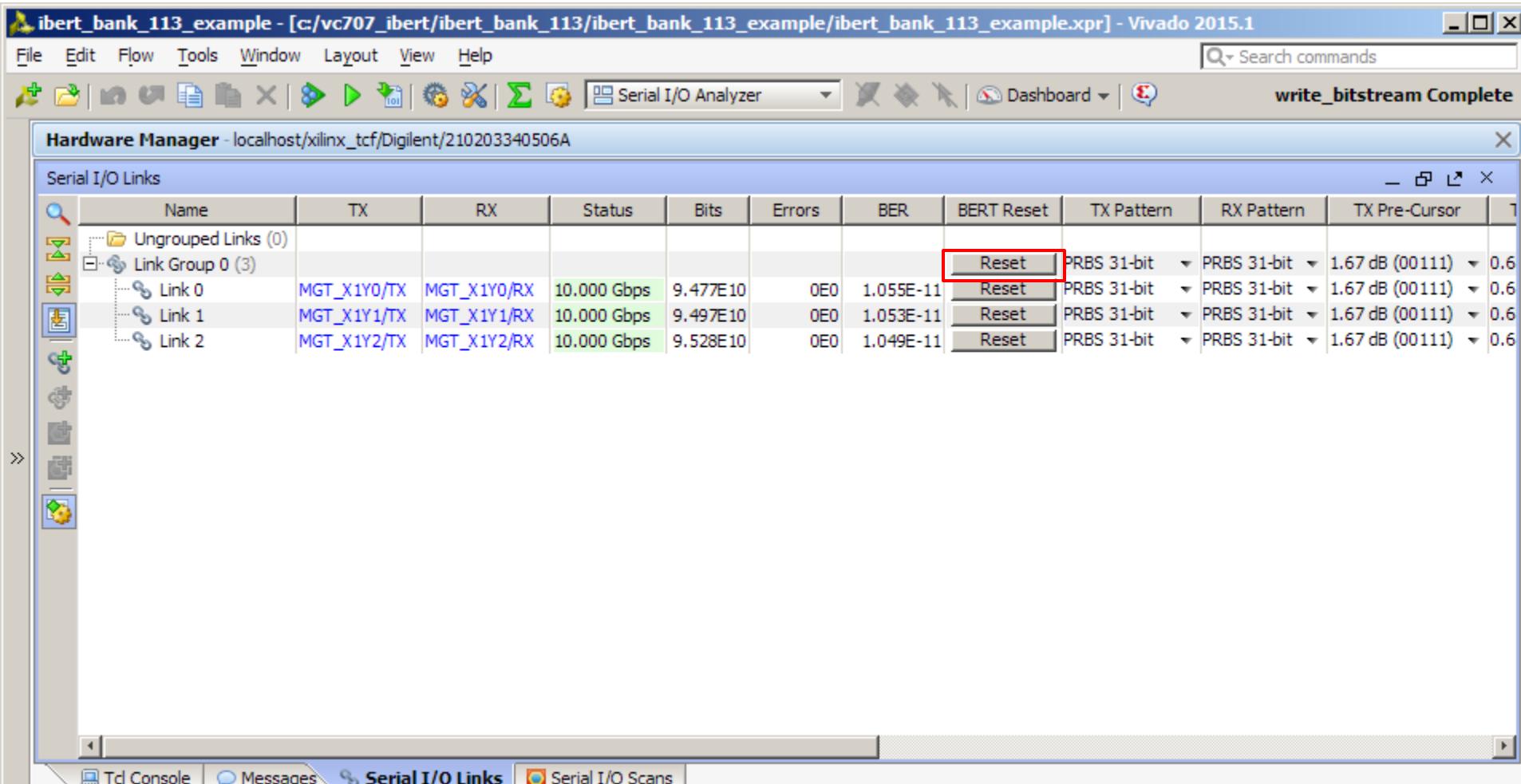
- Set the second link to Near-End PCS

The screenshot shows the Vivado 2015.1 Hardware Manager interface with the title bar "ibert\_bank\_113\_example - [c:/vc707\_ibert/ibert\_bank\_113/ibert\_bank\_113\_example/ibert\_bank\_113\_example.xpr] - Vivado 2015.1". The menu bar includes File, Edit, Flow, Tools, Window, Layout, View, and Help. The toolbar contains icons for New, Open, Save, Close, Run, Stop, and Dashboard. The main window displays the "Hardware Manager - localhost/xilinx\_tcf/Digilent/210203340506A" tab, specifically the "Serial I/O Links" section. The table lists four serial I/O links, each with settings for RX Pattern, TX Pre-Cursor, TX Post-Cursor, TX Diff Swing, DFE Enabled, Inject Error, TX Reset, RX Reset, RX PLL Status, TX PLL Status, and Loopback Mode. The second link's "Loopback Mode" is set to "Near-End PCS" and is highlighted with a red box.

RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode
RBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (11...)	<input checked="" type="checkbox"/>	Inject	R...	R...			Multiple
RBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (11...)	<input checked="" type="checkbox"/>	Inject	R...	R...	Locked	Locked	None
RBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (11...)	<input checked="" type="checkbox"/>	Inject	R...	R...	Locked	Locked	Near-End PCS
RBS 31-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (11...)	<input checked="" type="checkbox"/>	Inject	R...	R...	Locked	Locked	None

# Run IBERT Example Design

- Click the BERT Reset button for Link Group 0 to reset all three links
- Close the Vivado GUI when done



# Run IBERT Example Design

- The Hardware Manager Tcl commands can be captured from the Tcl console; these can be used for scripting this test
- Review ready\_for\_download/ibert\_bank\_113\_hw.tcl for an example

The screenshot shows the Vivado 2015.1 interface with the title bar "ibert\_bank\_113\_example - [c:/vc707\_ibert/ibert\_bank\_113/ibert\_bank\_113\_example/ibert\_bank\_113\_example.xpr] - Vivado 2015.1". The menu bar includes File, Edit, Flow, Tools, Window, Layout, View, Help. The toolbar includes icons for New, Open, Save, Close, Run, Stop, and various analysis tools. The main window is titled "Hardware Manager - localhost/xilinx\_tcf/Digilent/210203340506A". A sub-tab "Tcl Console" is active, displaying the following captured Tcl script:

```
lappend xil_newLinks $xil_newLink
set xil_newLinkGroup [create_hw_sio_linkgroup -description {Link Group 0} [get_hw_sio_links $xil_newLinks]]
unset xil_newLinks
set_property TX_PATTERN {PRBS 31-bit} [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
set_property RX_PATTERN {PRBS 31-bit} [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
set_property LOOPBACK {Near-End PCS} [get_hw_sio_links {localhost/xilinx_tcf/Digilent/210203340506A/0_1/IBERT/Quad_113/MGT_X1Y1/TX->localhost/xilin
commit_hw_sio [get_hw_sio_links {localhost/xilinx_tcf/Digilent/210203340506A/0_1/IBERT/Quad_113/MGT_X1Y1/TX->localhost/xilin
set_property LOGIC.MGT_ERRCNT_RESET_CTRL 1 [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
set_property LOGIC.MGT_ERRCNT_RESET_CTRL 0 [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
```

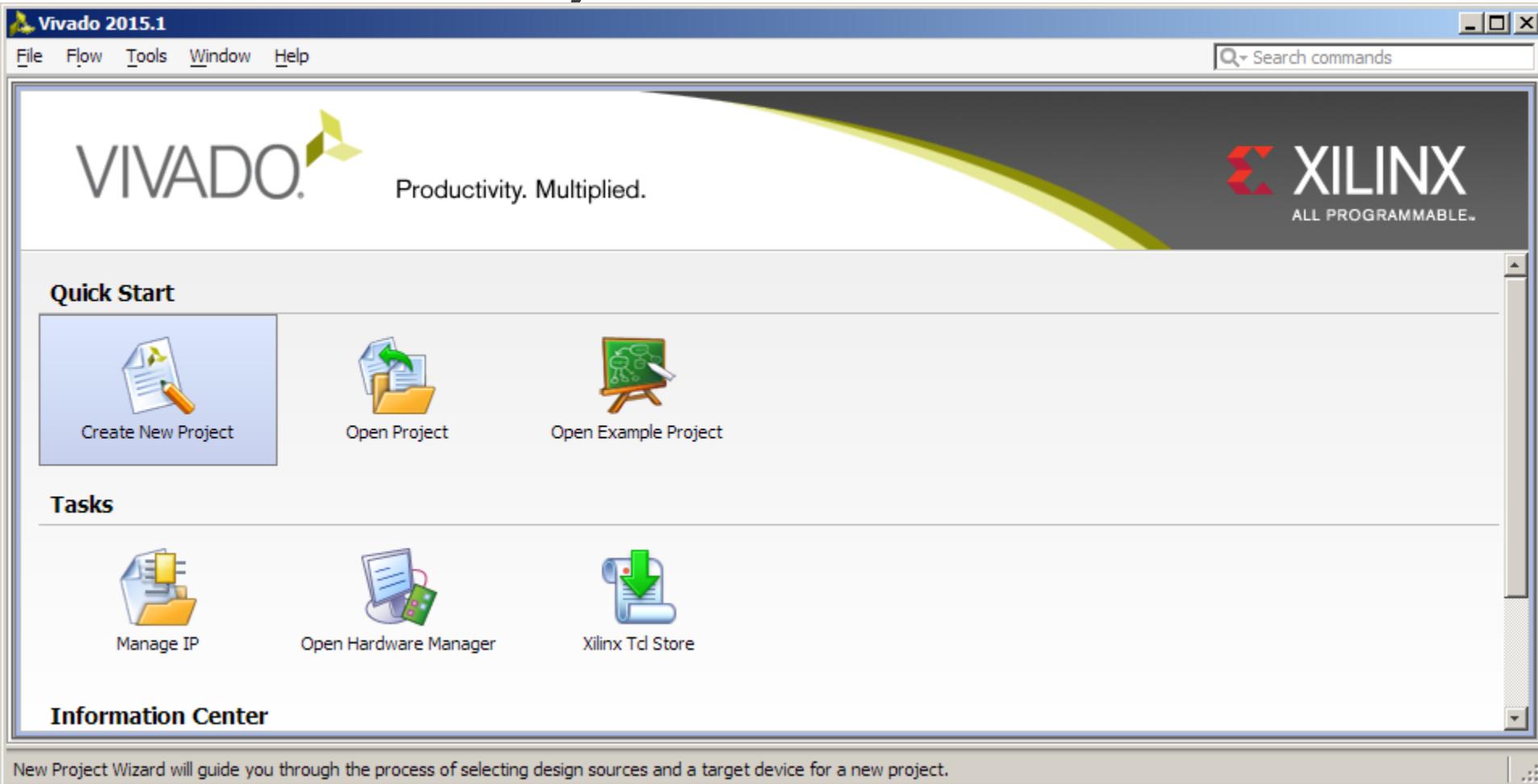
**Create IBERT Design for Banks 114, 115**

# Create IBERT Design for Banks 114, 115

## ► Open Vivado

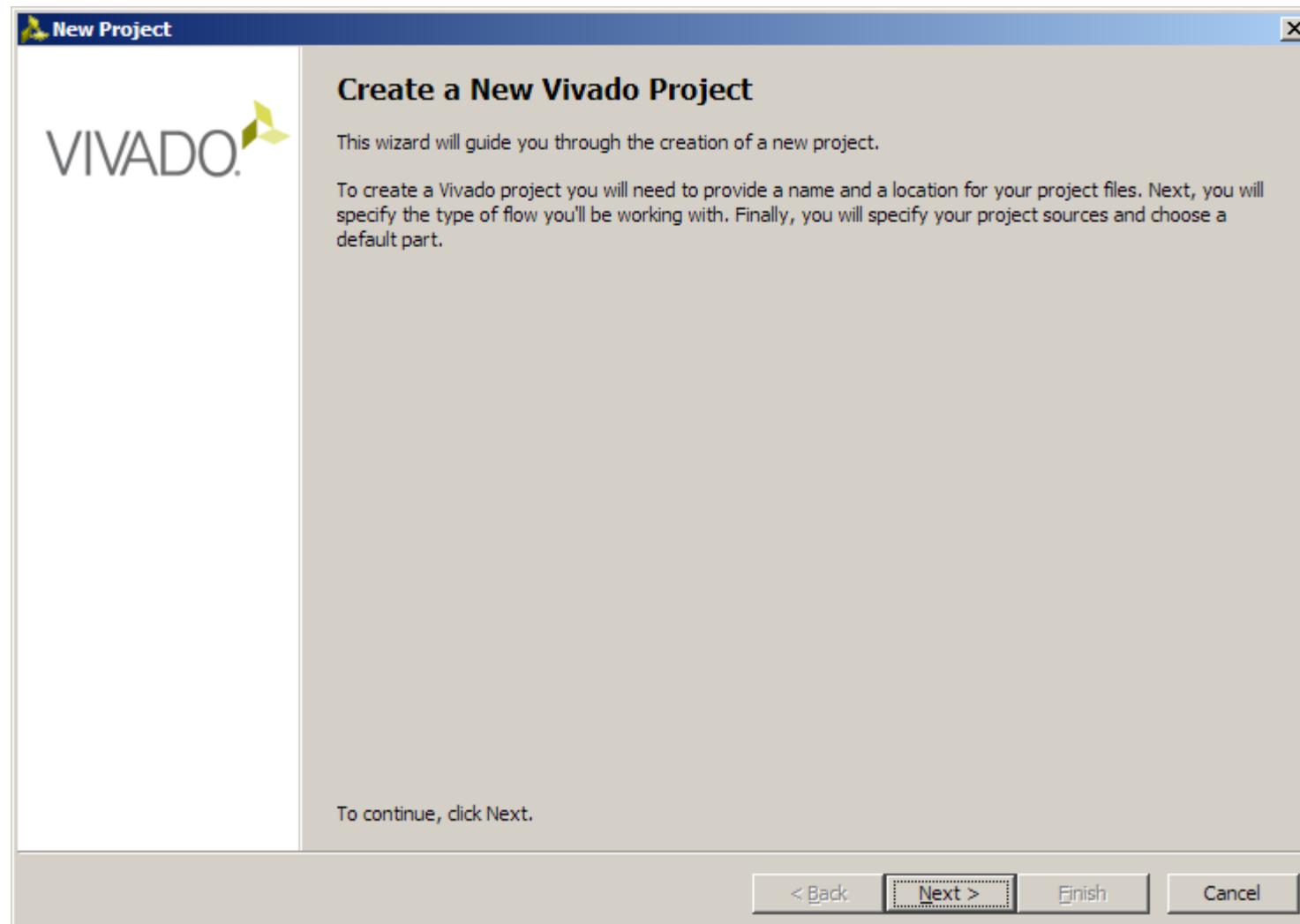
Start → All Programs → Xilinx Design Tools → Vivado 2015.1 → Vivado

## ► Select Create New Project



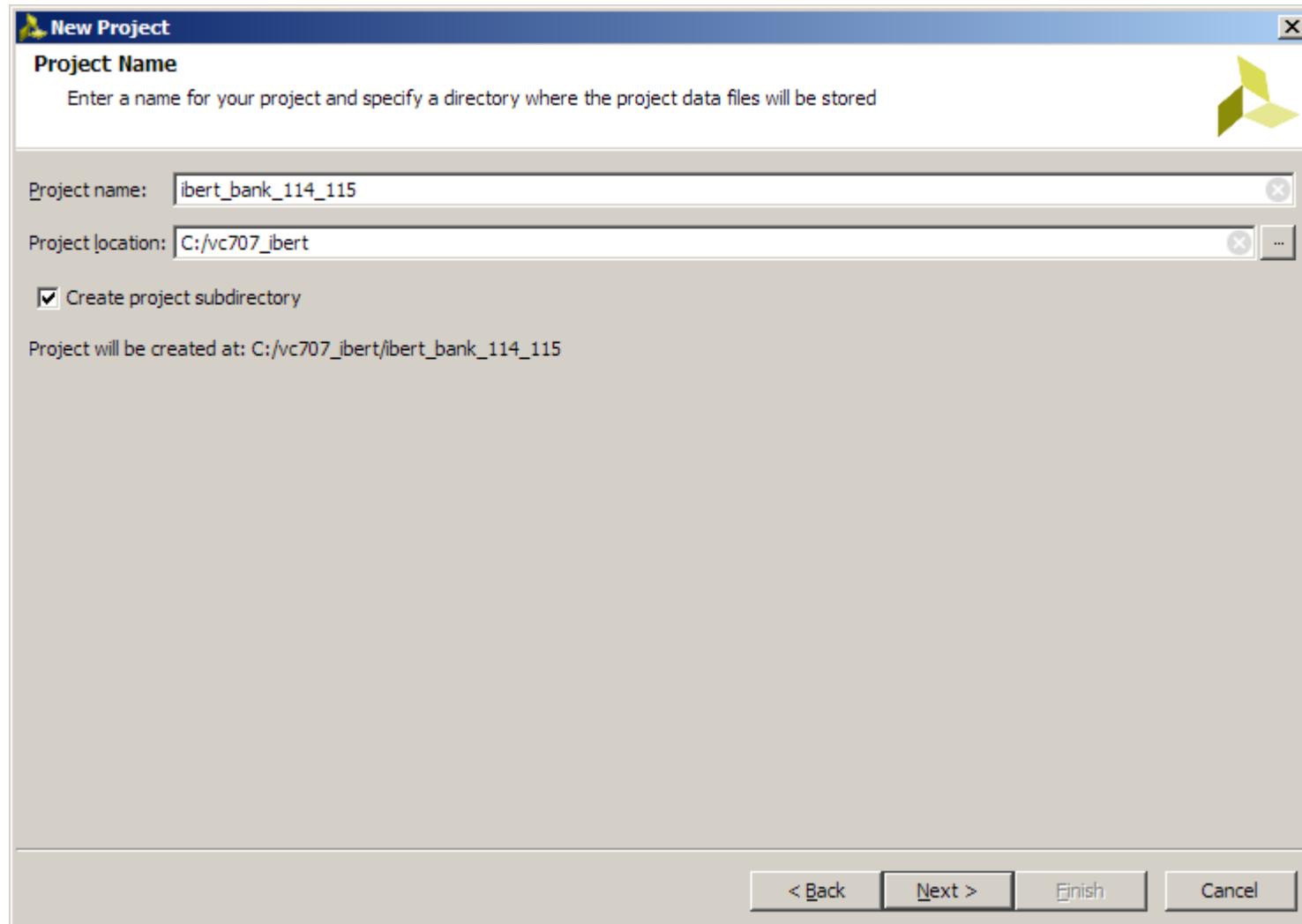
# Create IBERT Design for Banks 114, 115

► Click Next



# Create IBERT Design for Banks 114, 115

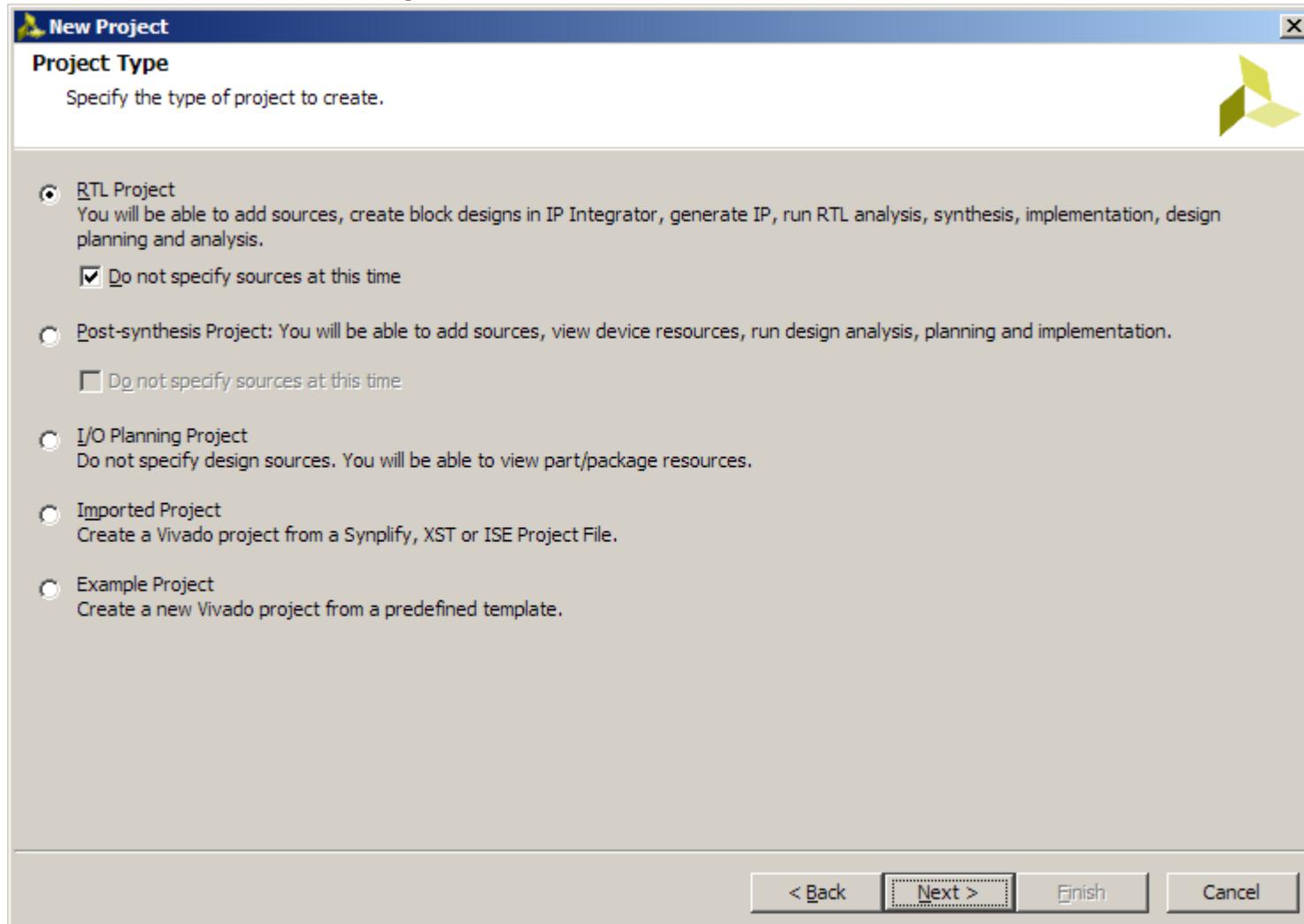
- Set the Project name and location to `ibert_bank_114_115` and `C:/vc707_ibert`; check Create project subdirectory



# Create IBERT Design for Banks 114, 115

## ► Select RTL Project

- Select **Do not specify sources at this time**



# Create IBERT Design for Banks 114, 115

## ► Select the VC707 Board

The screenshot shows the 'New Project' dialog box with the title 'Default Part'. It displays a list of Xilinx boards for selection. The 'Boards' tab is selected. The search bar contains the text 'VC707'. The table lists the following information for each board:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Avail IOBs
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484	1.3	200
Artix-7 AC701 Evaluation Platform	xilinx.com	1.1	xc7a200tfgb676-2	676	1.2	400
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	xc7k325tffg900-2	900	1.2	500
Kintex-Ultrascale KCU105 Evaluation Platform	xilinx.com	1.0	xcu040-ffva1156-2-e	1,156	1.0	520
<b>Virtex-7 VC707 Evaluation Platform</b>	<b>xilinx.com</b>	<b>1.1</b>	<b>xc7vx485tffg1761-2</b>	<b>1,761</b>	<b>1.2</b>	<b>700</b>
Virtex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2	1,761	1.6	850
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.2	200
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	1.1	xc7z045tffg900-2	900	1.2	362

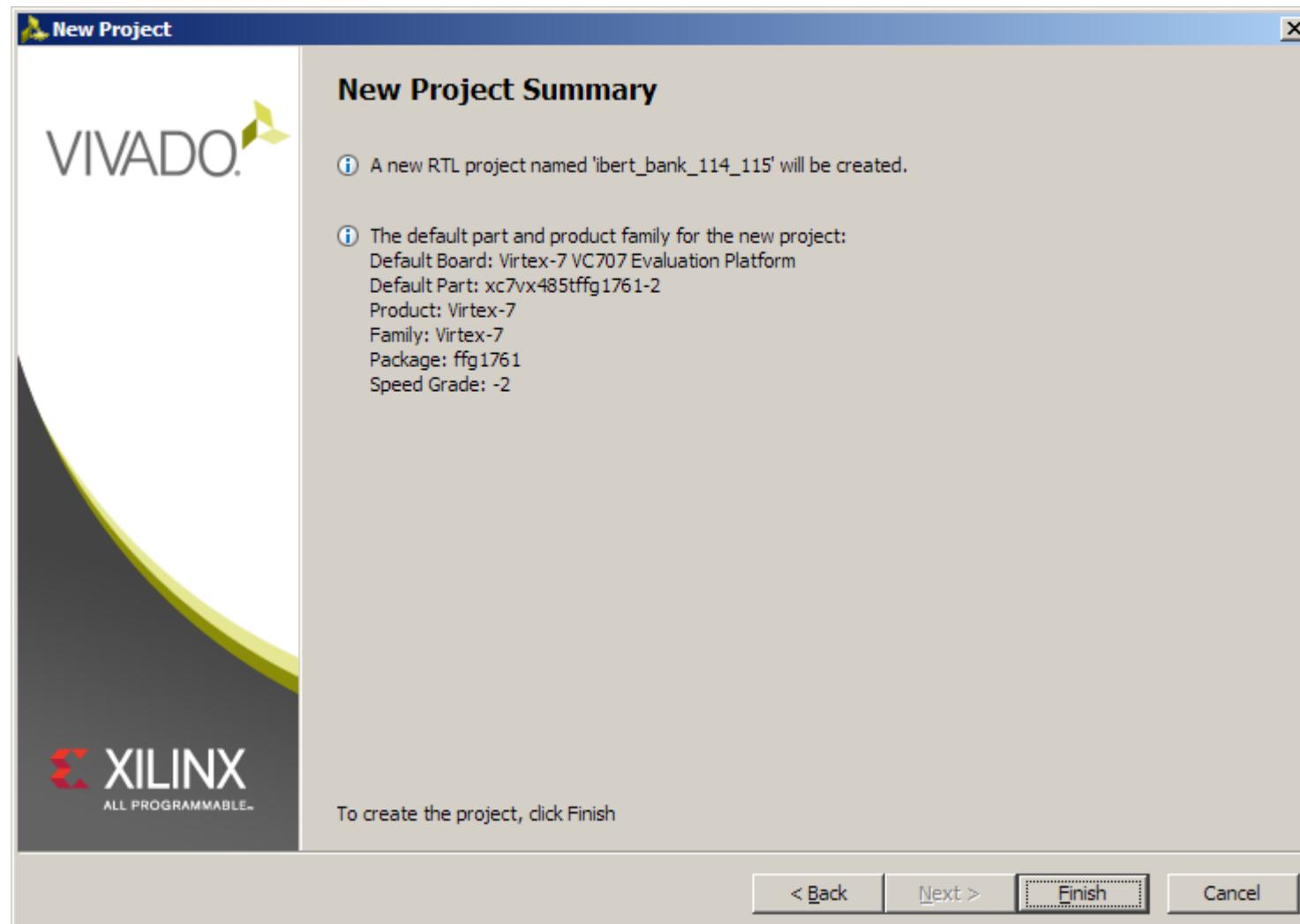
At the bottom of the dialog, there are buttons for '< Back', 'Next >', 'Finish', and 'Cancel'.

Note: Presentation applies to the VC707

XILINX ALL PROGRAMMABLE™

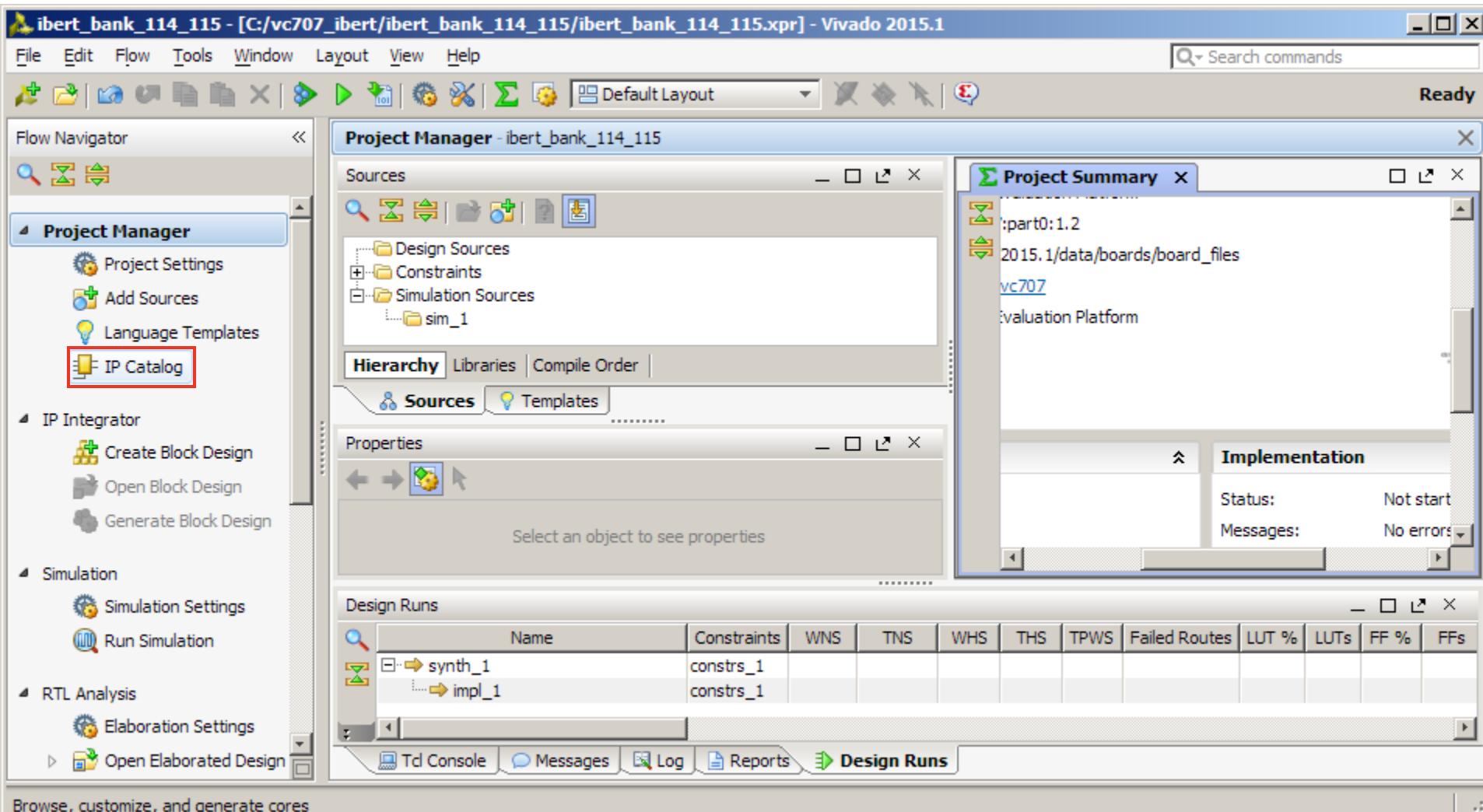
# Create IBERT Design for Banks 114, 115

► Click Finish



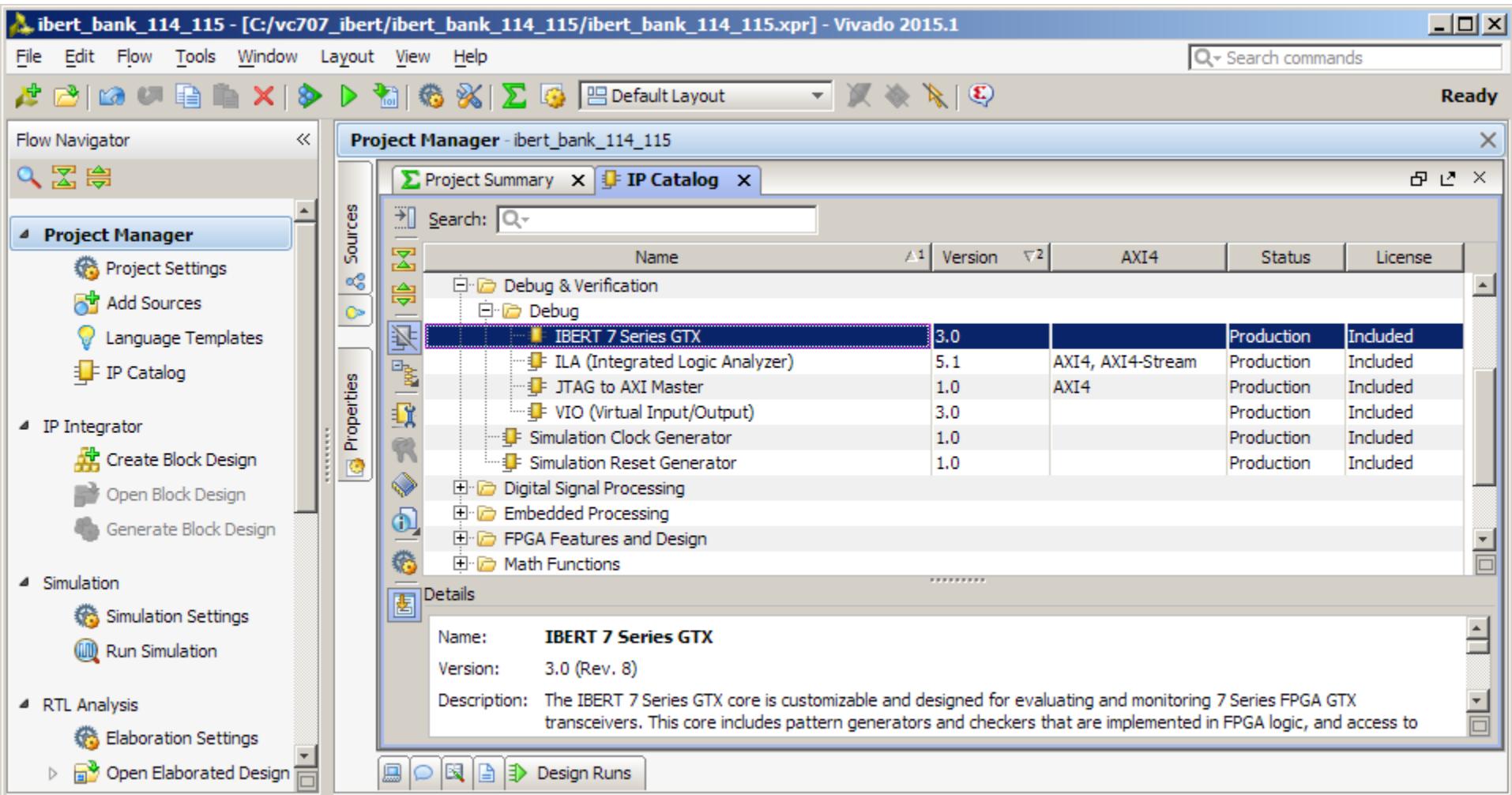
# Create IBERT Design for Banks 114, 115

► Click on IP Catalog



# Create IBERT Design for Banks 114, 115

► Select IBERT 7 Series GTX, v3.0 under Debug & Verification



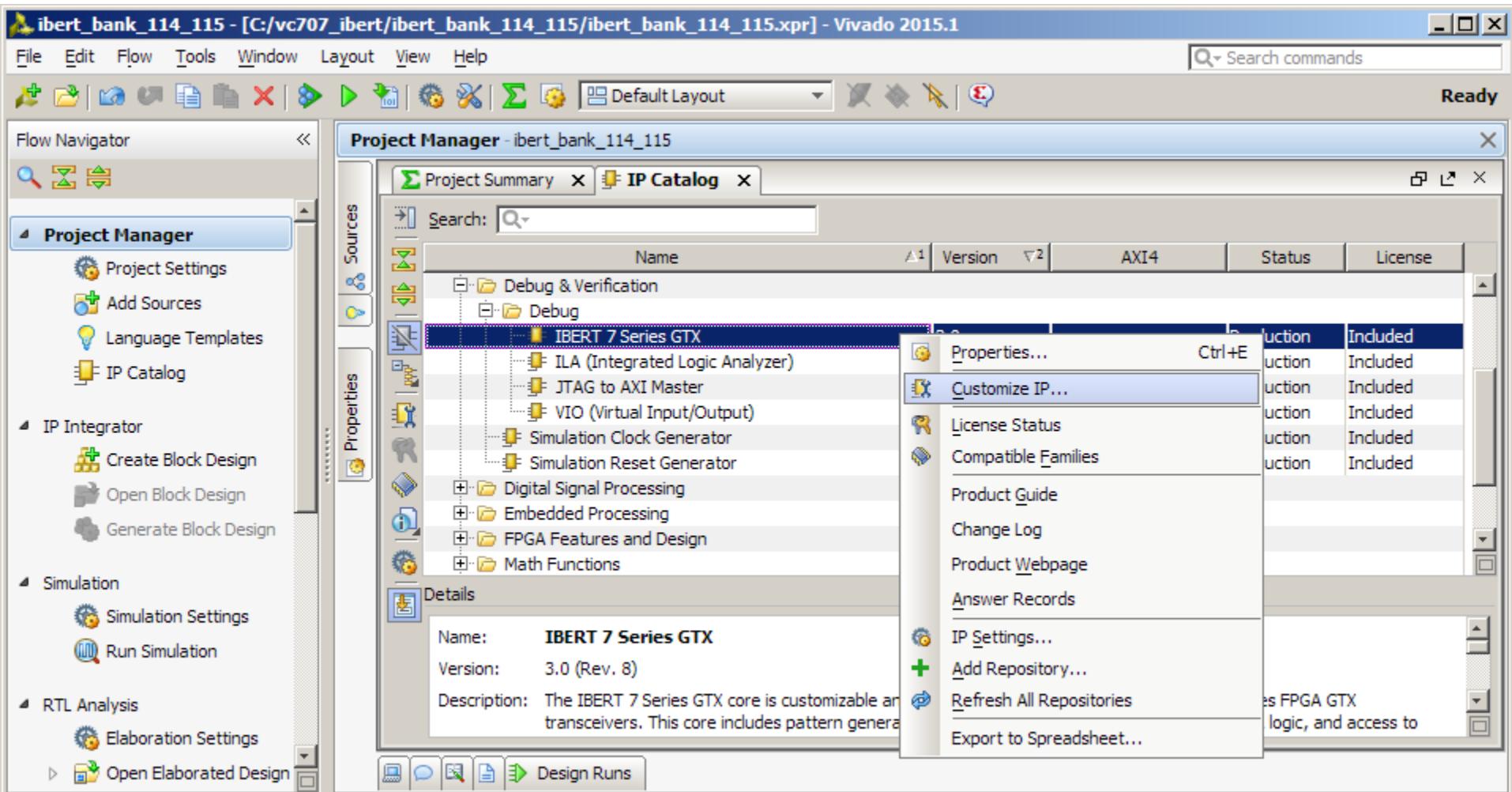
IP: IBERT 7 Series GTX

Note: Presentation applies to the VC707

XILINX ➤ ALL PROGRAMMABLE™

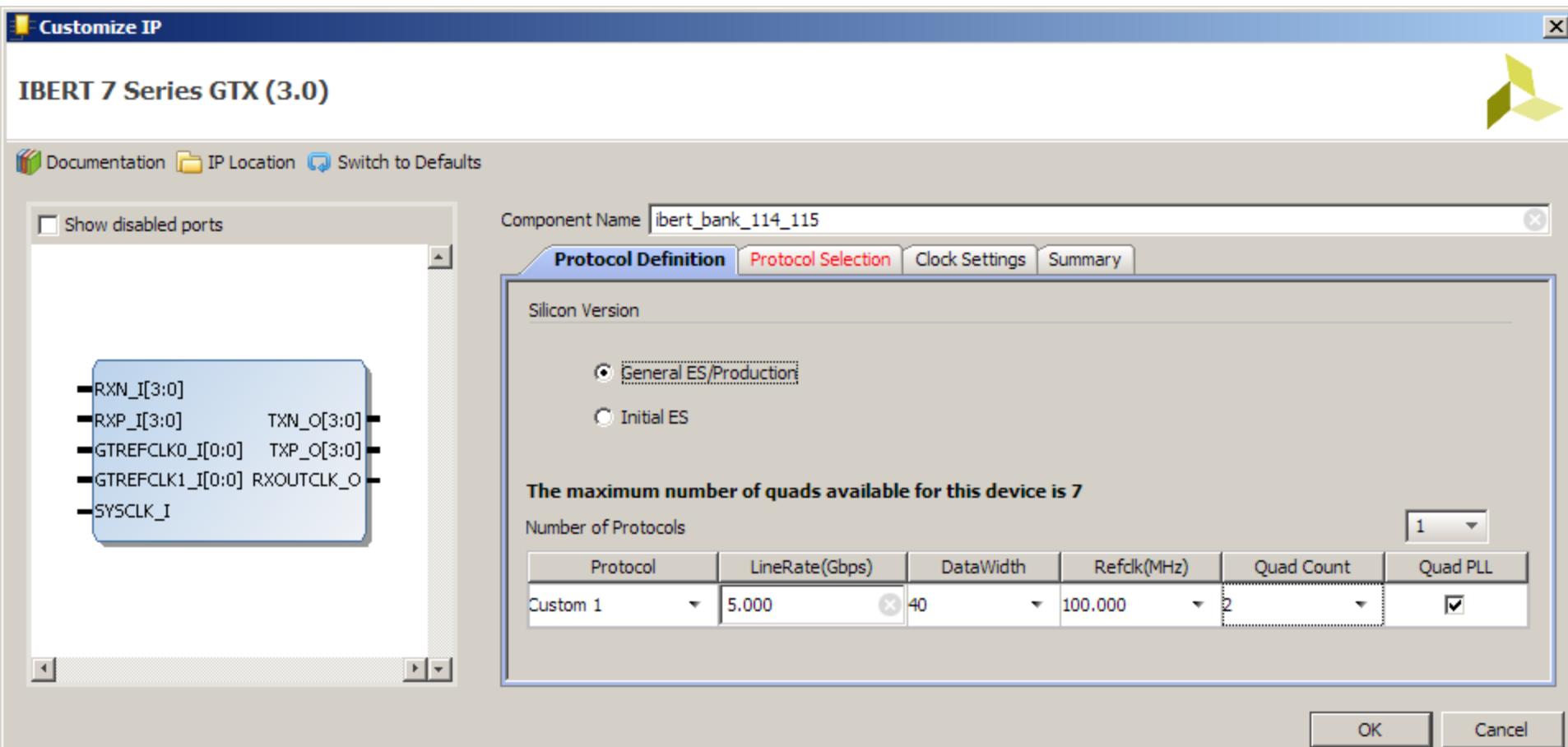
# Create IBERT Design for Banks 114, 115

► Right click on IBERT 7 Series GTX and select Customize IP...



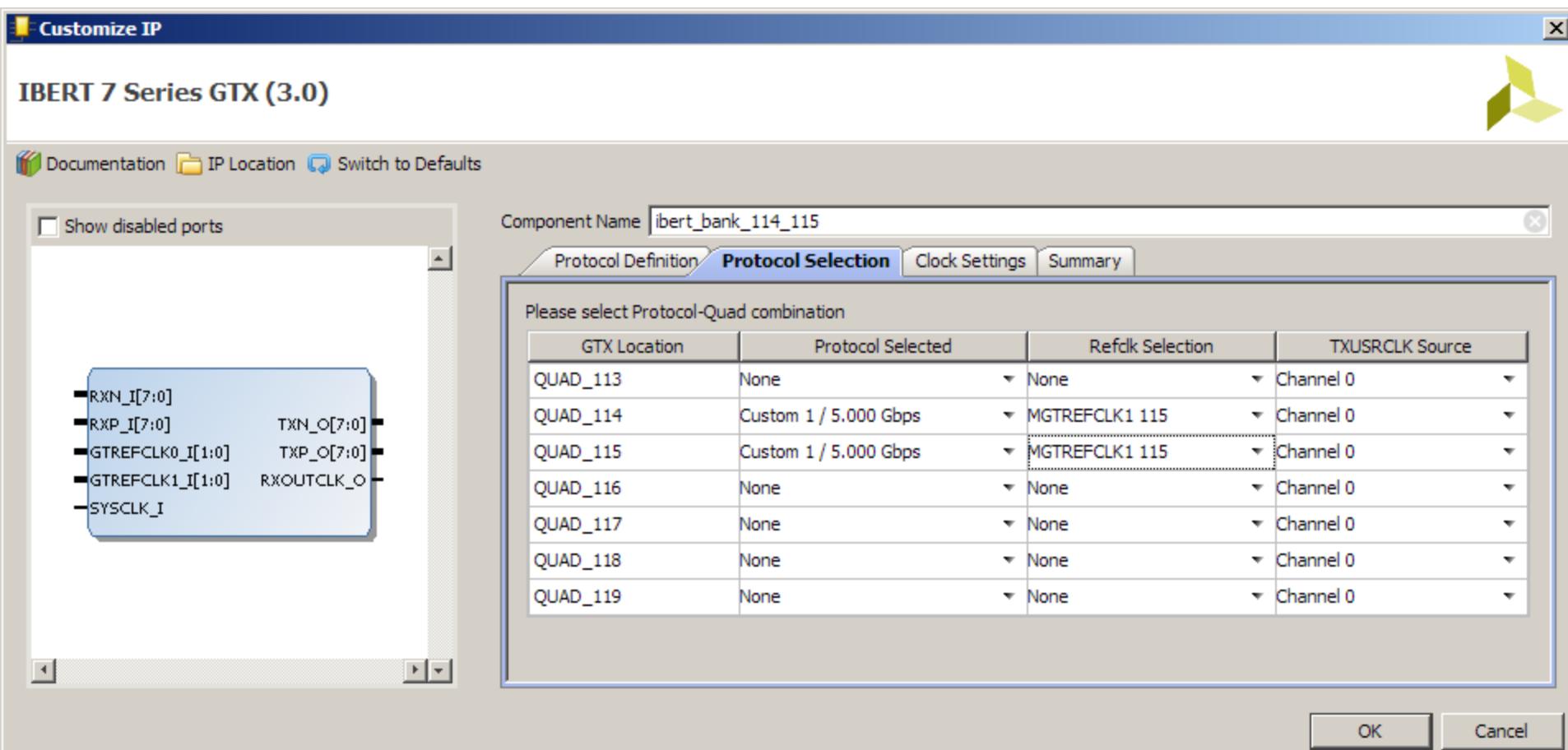
# Create IBERT Design for Banks 114, 115

- Set the Component name: **ibert\_bank\_114\_115**
- Under the Protocol Definition tab
  - Silicon Version: **General ES / Production**
  - Protocol: LineRate: **5.000**, DataWidth: **40** Refclk: **100.000** Quad Count: **2**



# Create IBERT Design for Banks 114, 115

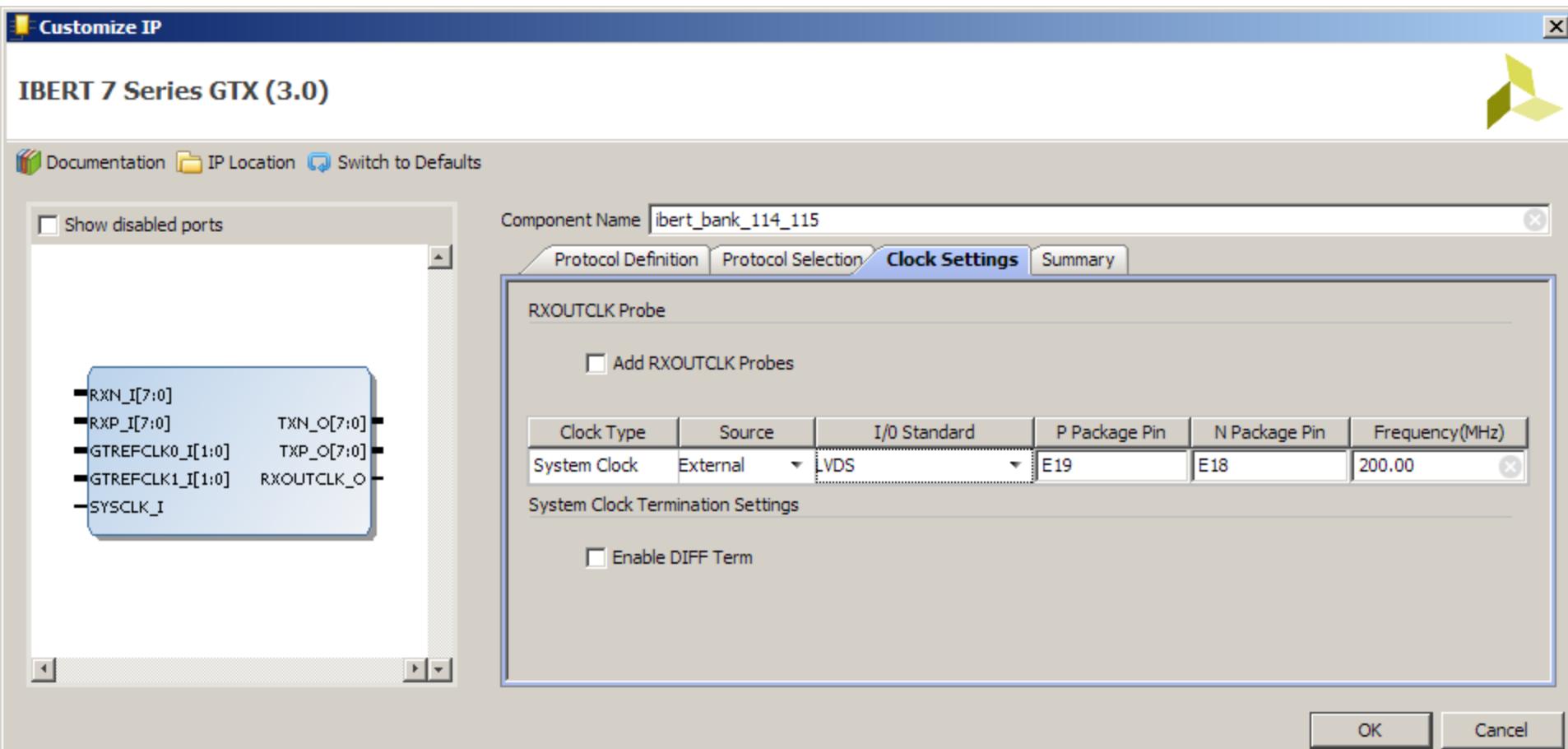
- Under the Protocol Selection tab
- Set QUAD\_114 and QUAD\_115 to
  - Custom 1 / 5.000 Gbps, and MGTREFCLK1 115



# Create IBERT Design for Banks 114, 115

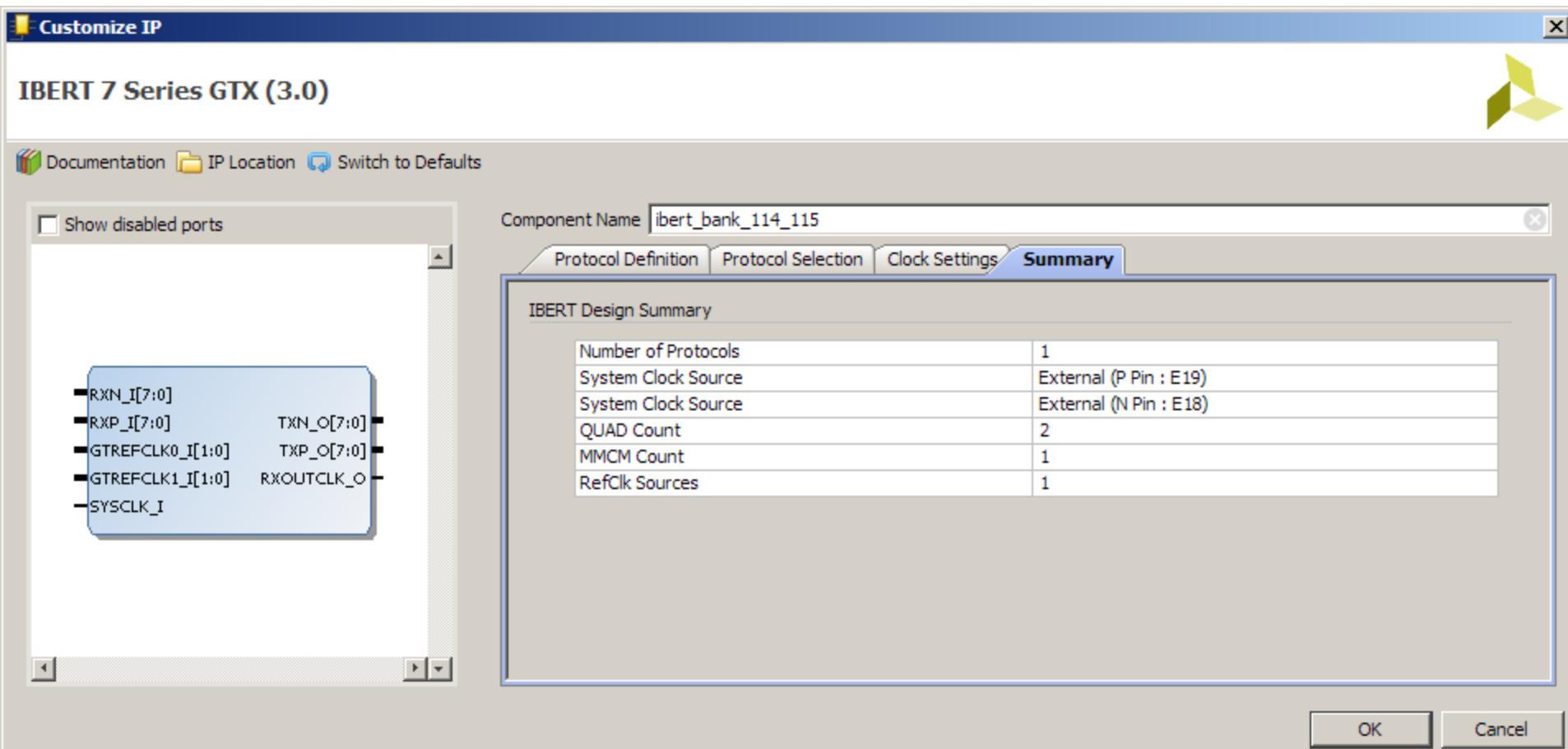
► Under the Clock Settings tab, set the System Clock:

- LVDS, P Pin Location: E19, N Pin Location: E18



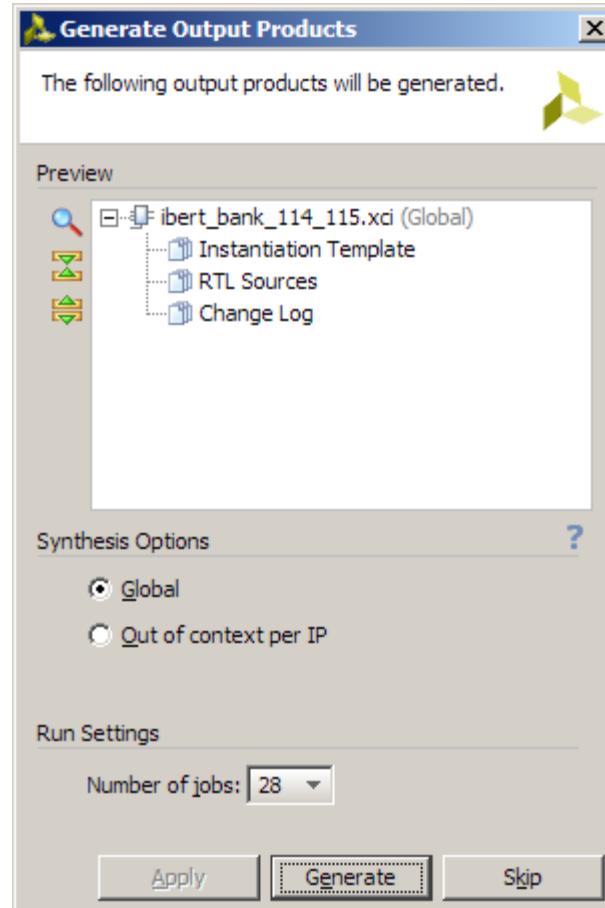
# Create IBERT Design for Banks 114, 115

► Review the summary and click OK



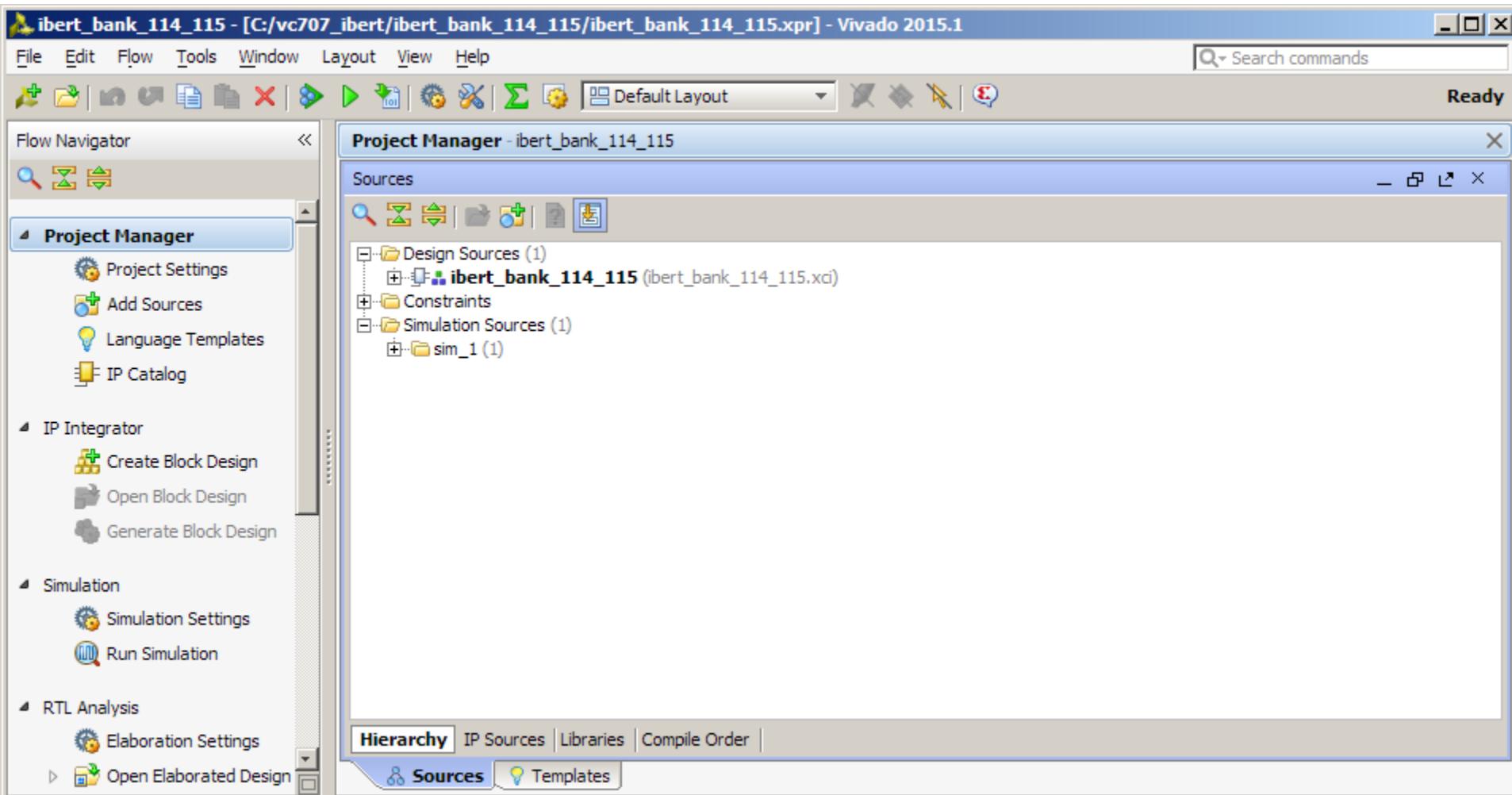
# Create IBERT Design for Banks 114, 115

► Click Generate



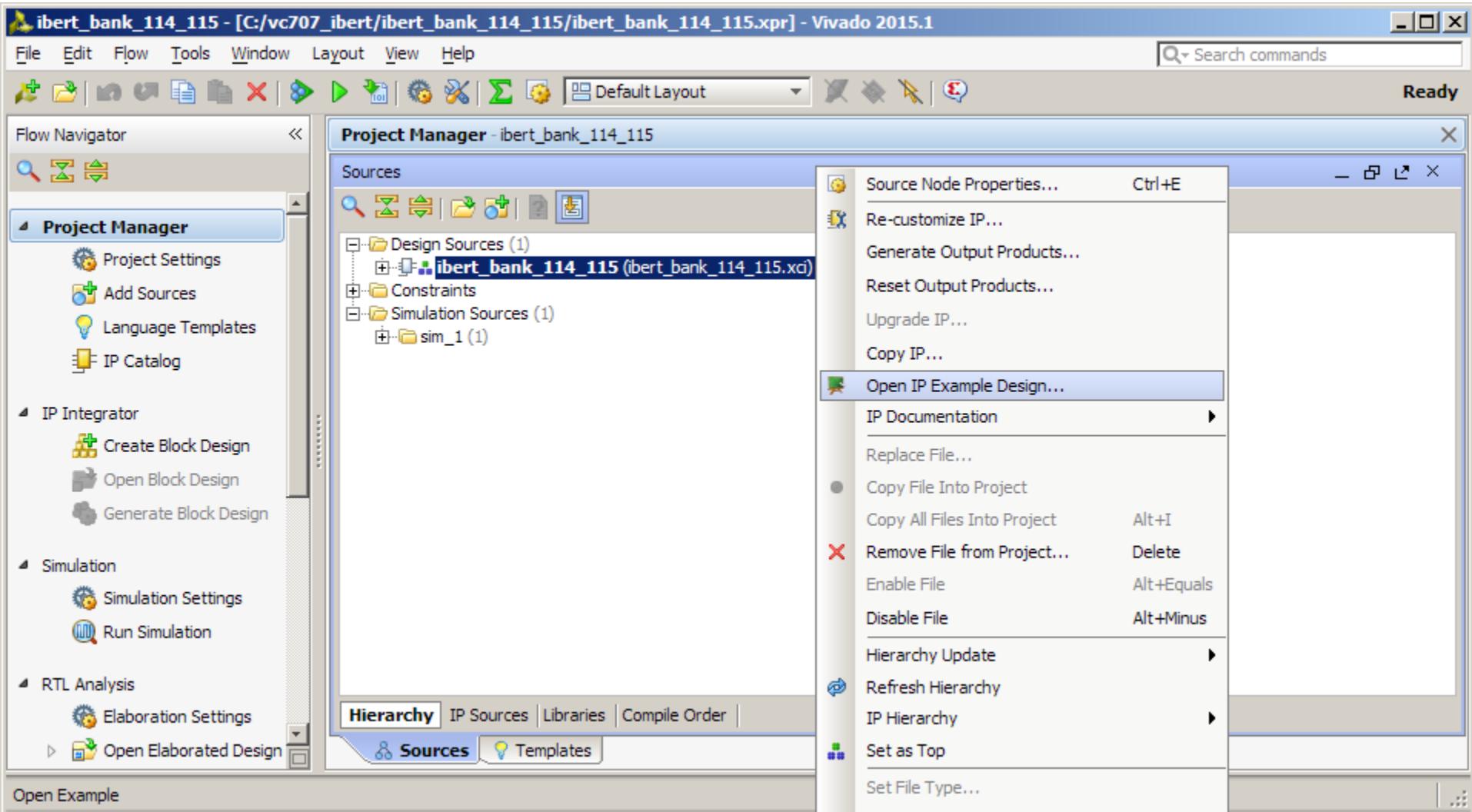
# Create IBERT Design for Banks 114, 115

► Bank 114 & 115 IBERT design appears in Design Sources



# Compile Example Design

► Right click on `ibert_bank_114_115` and select Open IP Example Design...

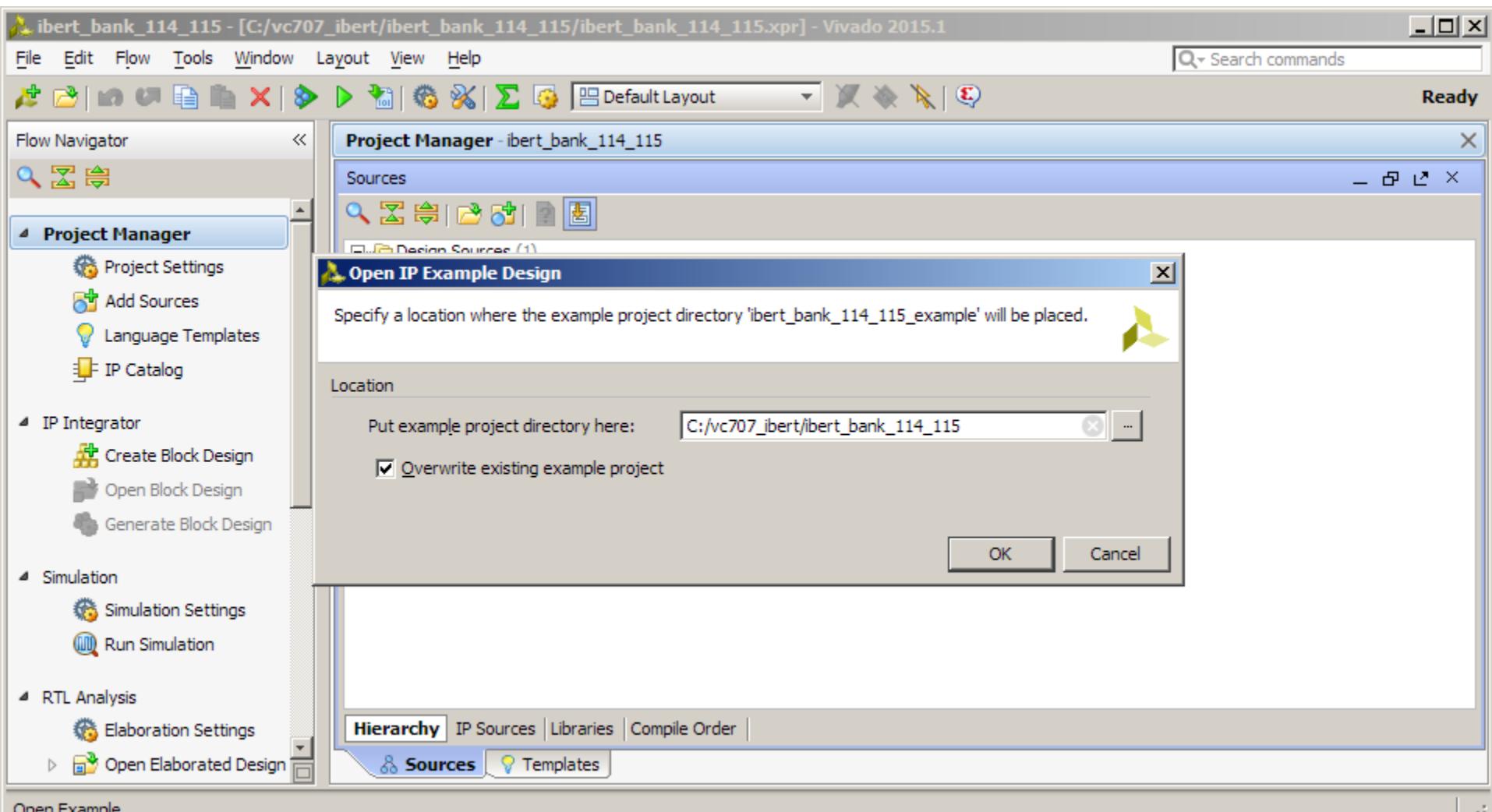


Note: Presentation applies to the VC707

XILINX ➤ ALL PROGRAMMABLE™

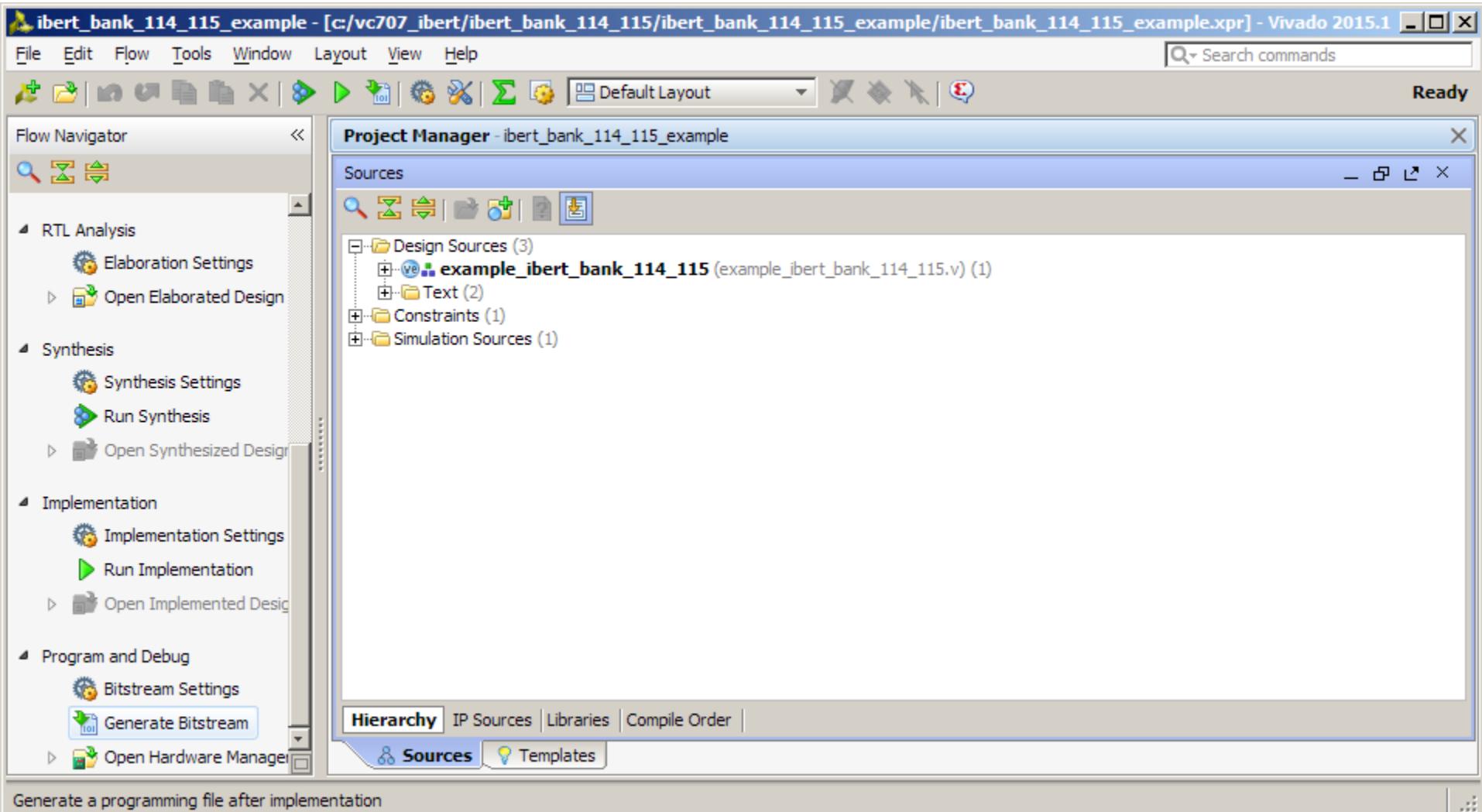
# Compile Example Design

► Set the location to C:/vc707\_ibert/ibert\_bank\_114\_115 and click OK



# Compile Example Design

- A new project is created
- Click Generate Bitstream

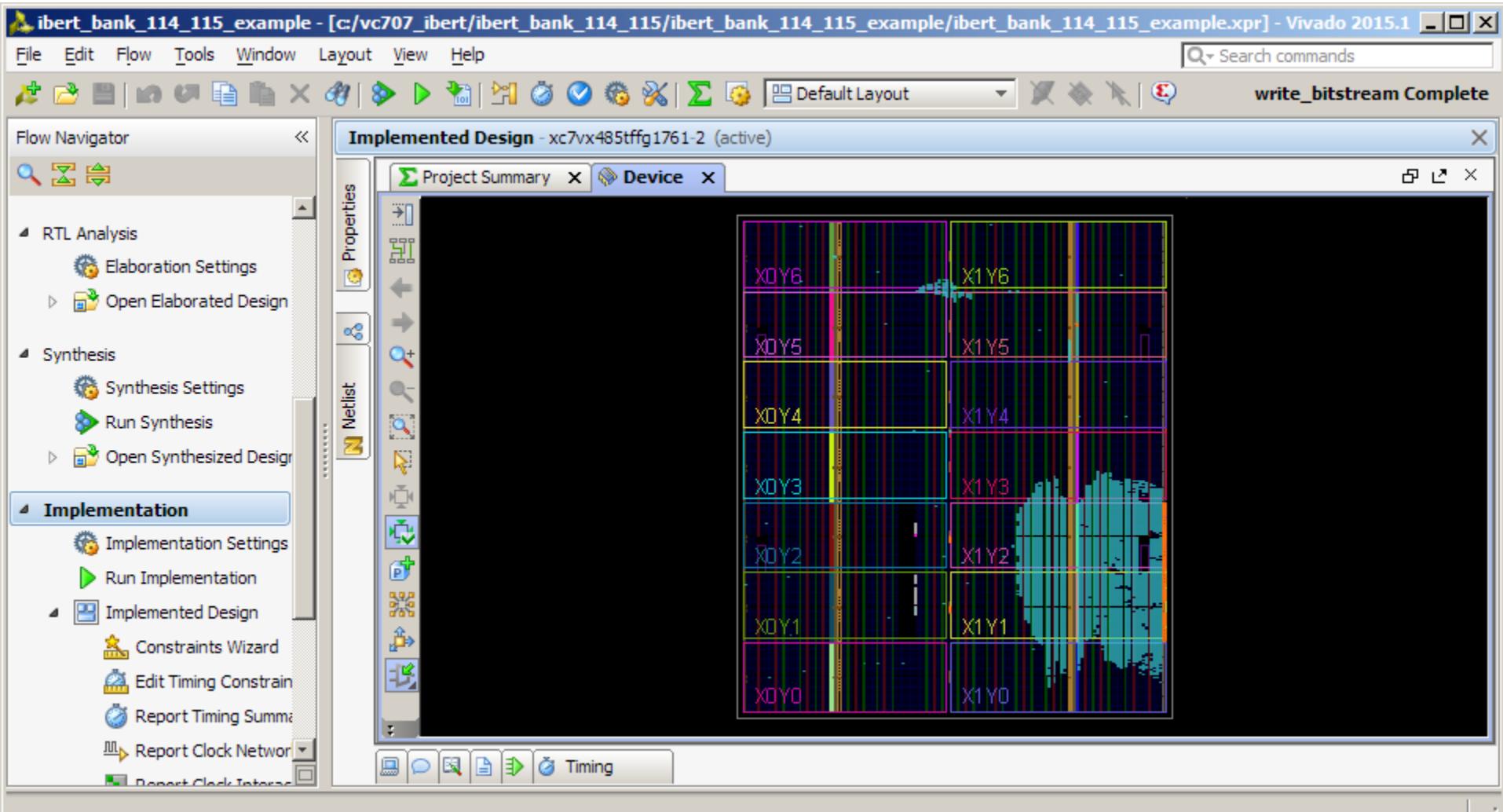


Note: The original project window can be closed

 XILINX ➤ ALL PROGRAMMABLE™

# Compile Example Design

► Open and view the Implemented Design



## **Testing Banks 114 and 115 with Optional User Provided Hardware**

# Optional Testing with User Provided Hardware

## ► SMA Cables

- [www.rosenbergerna.com](http://www.rosenbergerna.com)
- Part number:  
72D-32S1-32S1-00610A



## ► SMA Quick connects

- RADIALL
- Part number: R125791501
- Available [here](#) or [here](#)

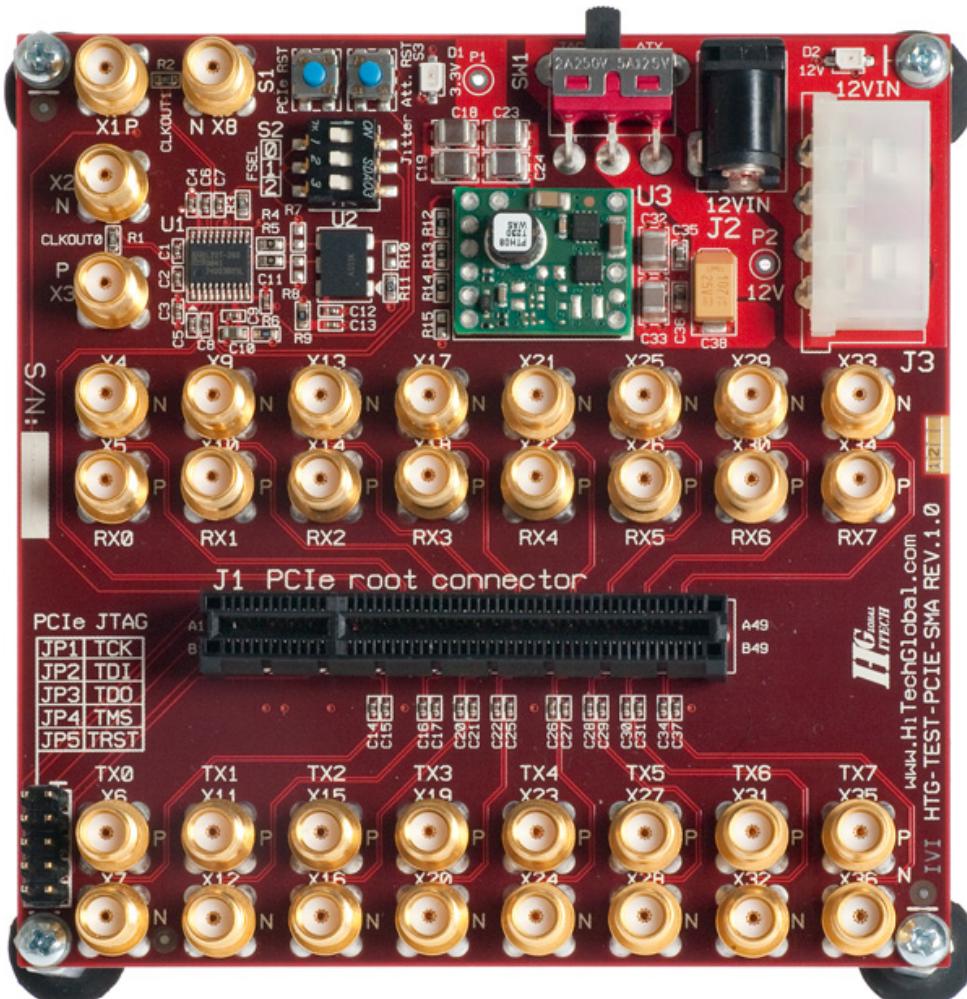


# Optional Testing with User Provided Hardware

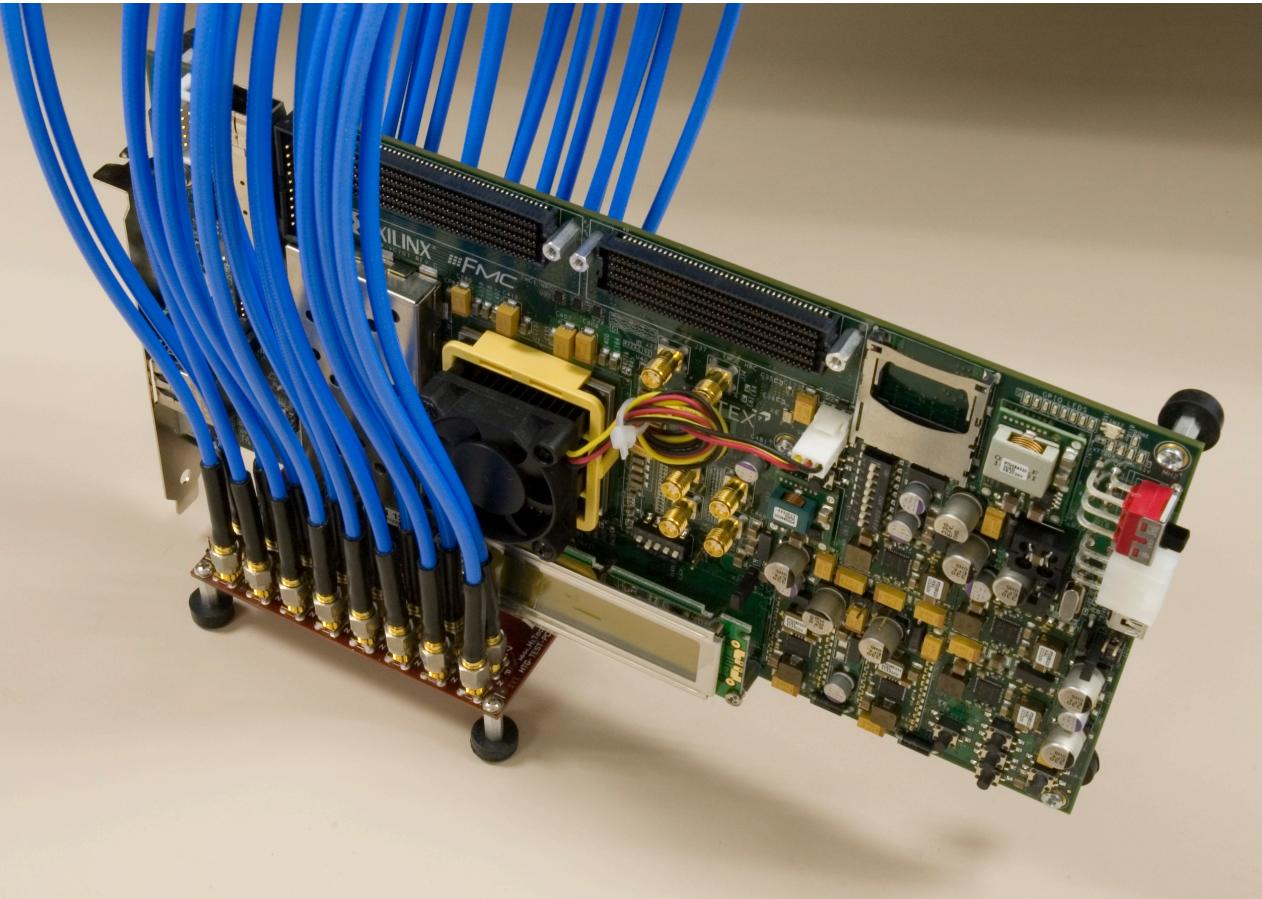
► For testing Banks 114 and 115:

## ► PCIe Testing Hardware:

- HiTechGlobal PCI Express Test & SerialIO Expansion Module
- [HTG-TEST-PCIE-SMA](#)
- 16 SMA cables required
- Requires power supply, either:
  - 4-pin Peripheral power connector from ATX power supply
- Or:
  - HiTechGlobal [PWR-12V-6A](#)



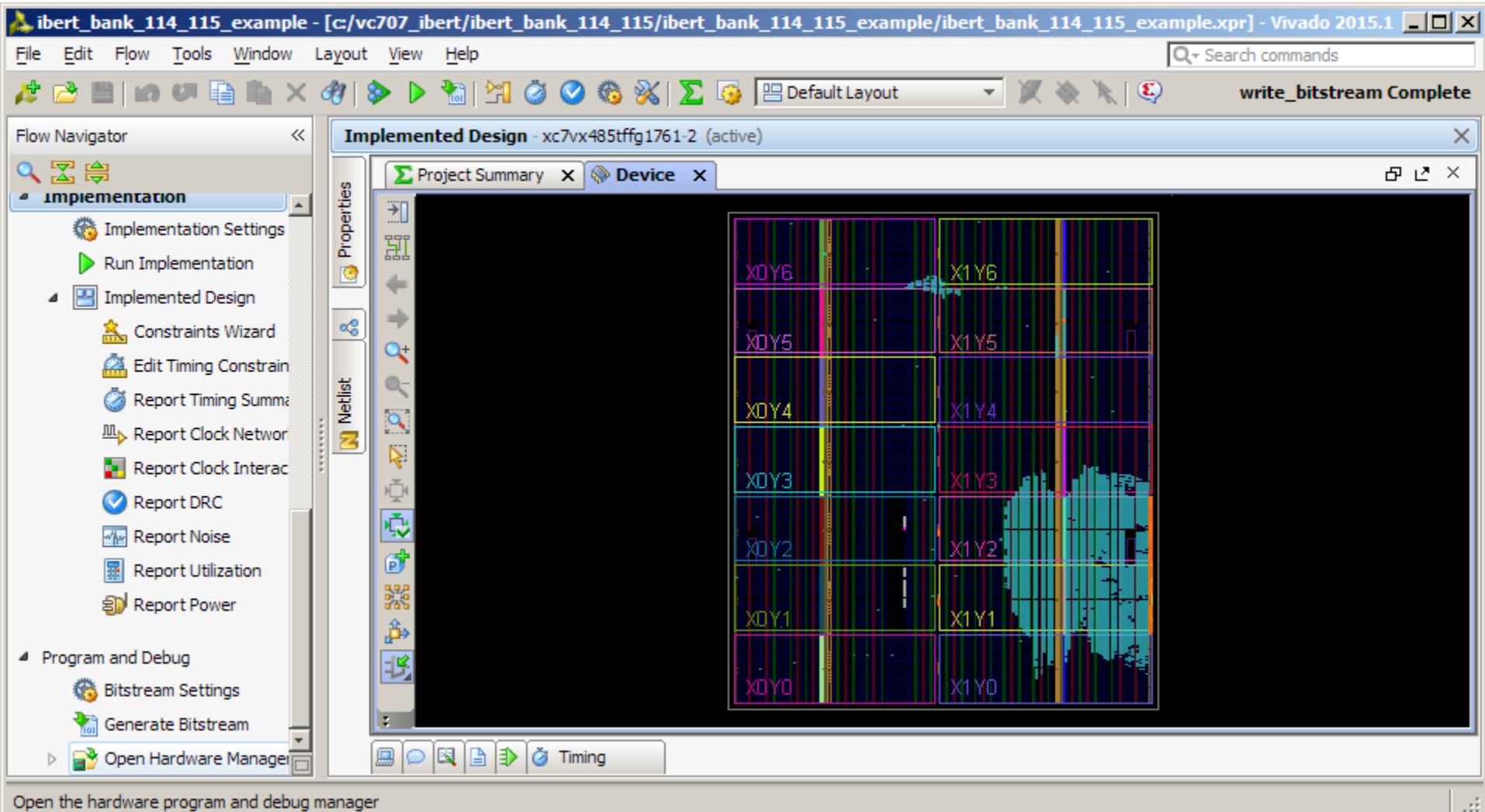
# Testing Banks 114 and 115 with Optional User Provided Hardware



- Connect SMA Cables:
  - TX0 P/N to RX0 P/N,  
TX1 P/N to RX1 P/N,  
etc.
- Insert VC707 into PCIe slot
- Connect the VC707 and HiTechGlobal power supplies
- Power up the VC707 and HiTechGlobal boards

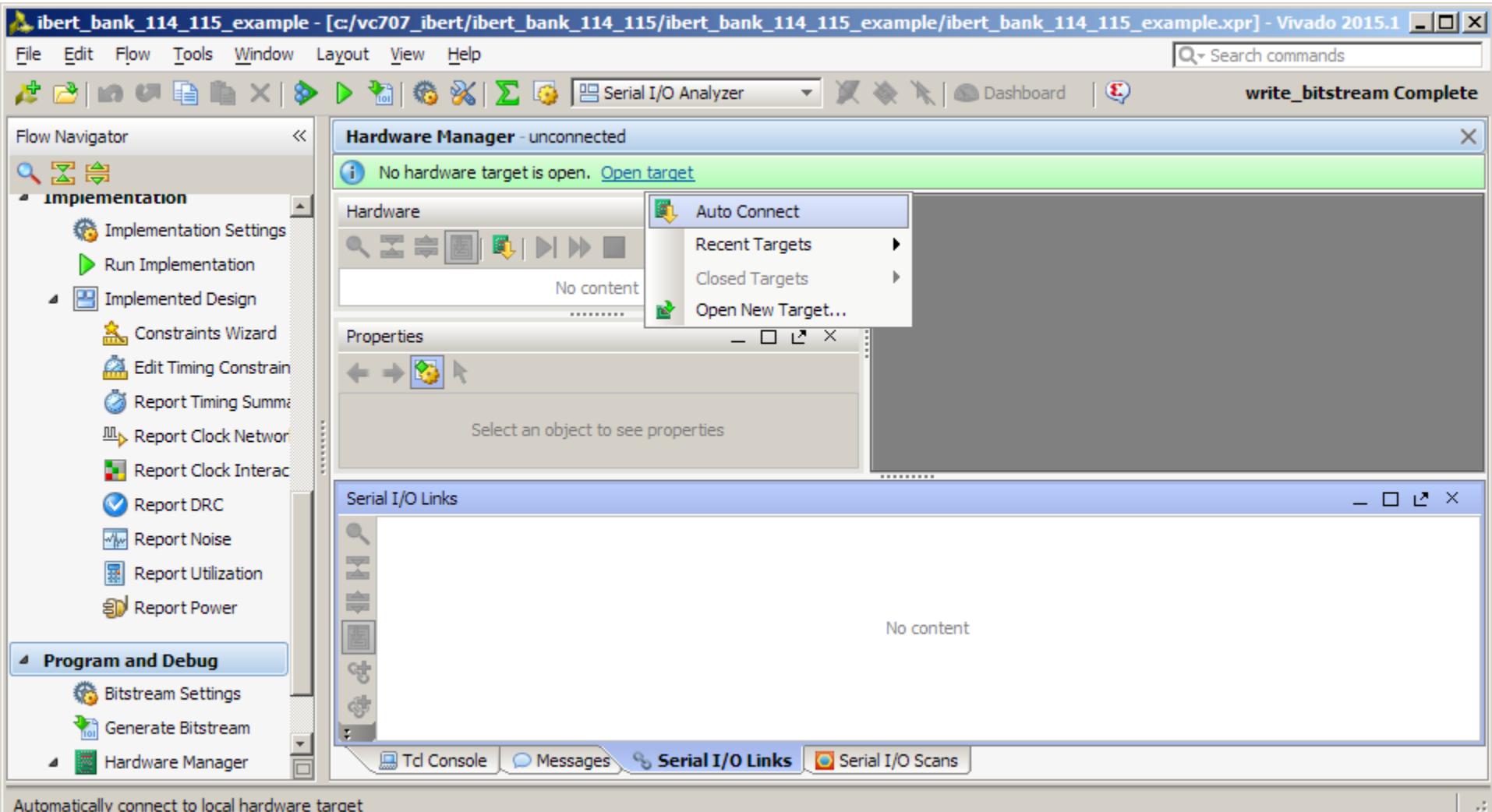
# Run IBERT Example Design

► Click Open Hardware Manager



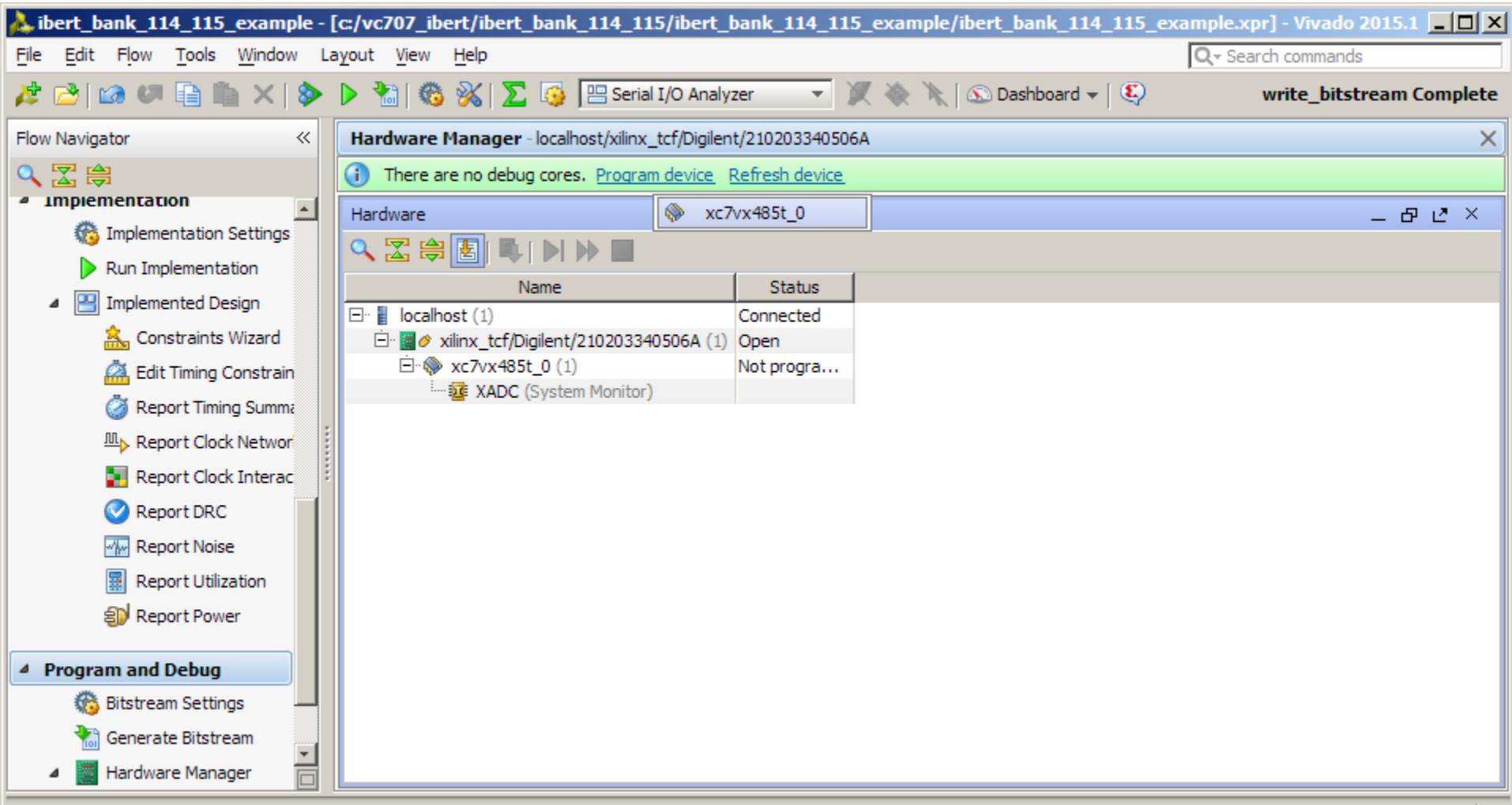
# Run IBERT Example Design

► Click Open target and select Auto Connect



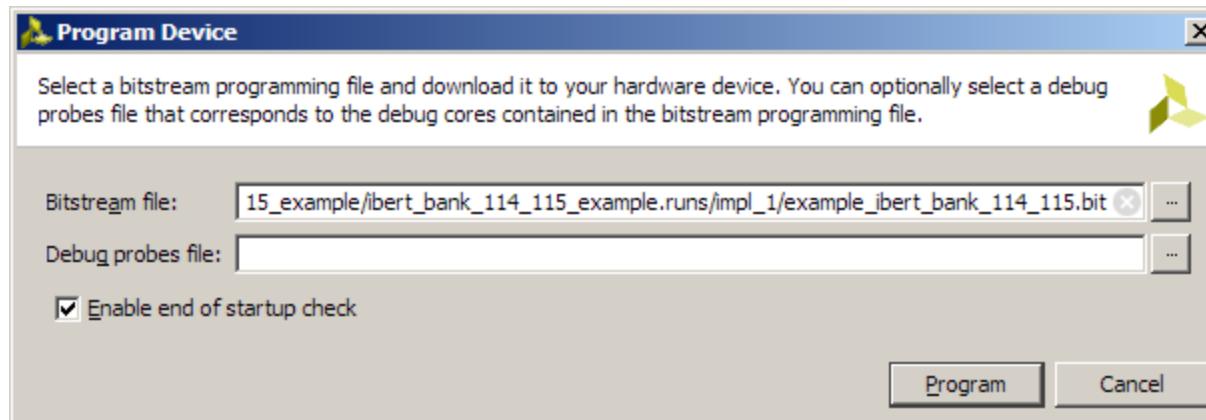
# Run IBERT Example Design

► Select Program device → xc7vx485t\_0



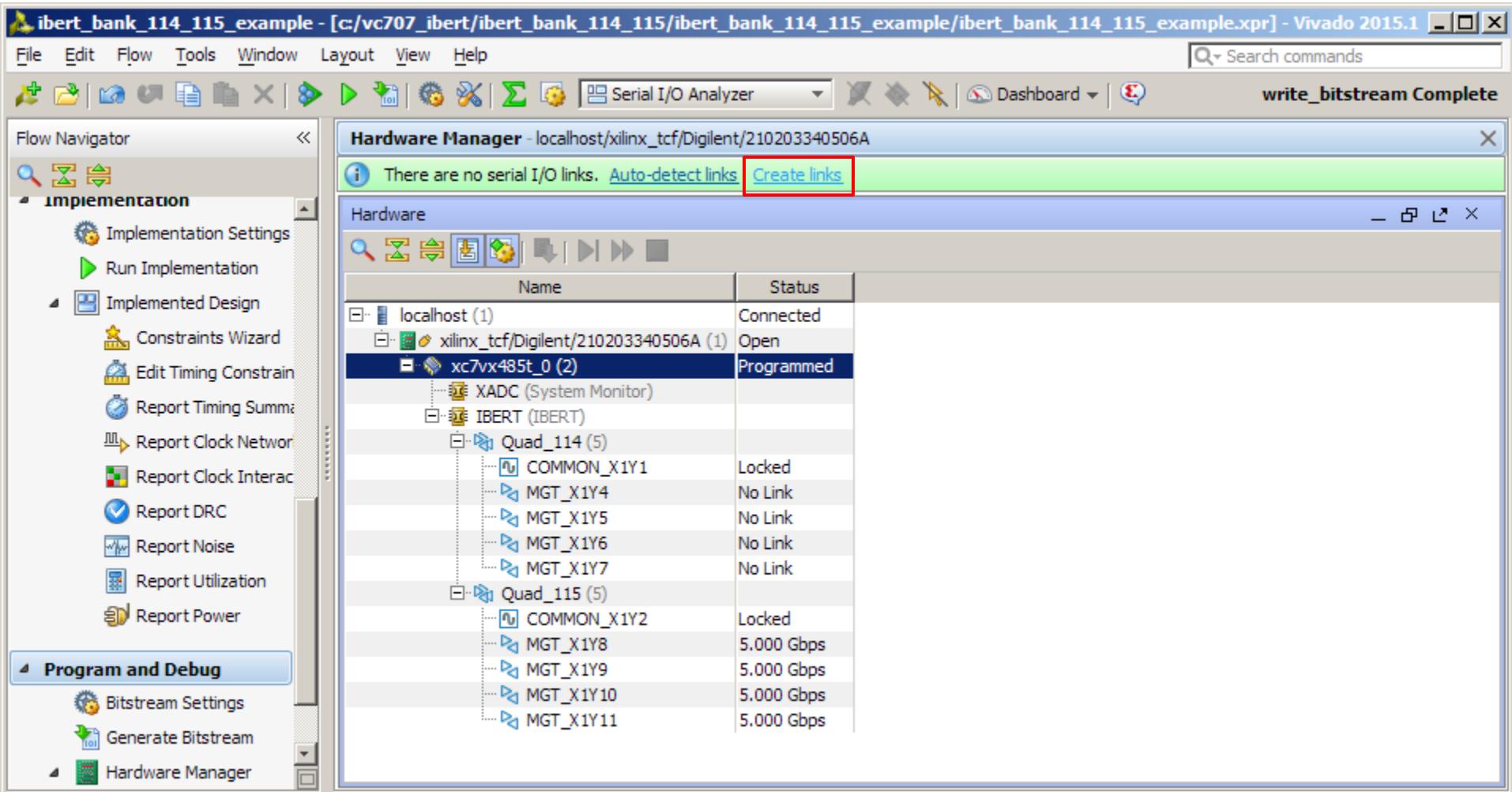
# Run IBERT Example Design

- The newly created bitstream is default
- Click Program



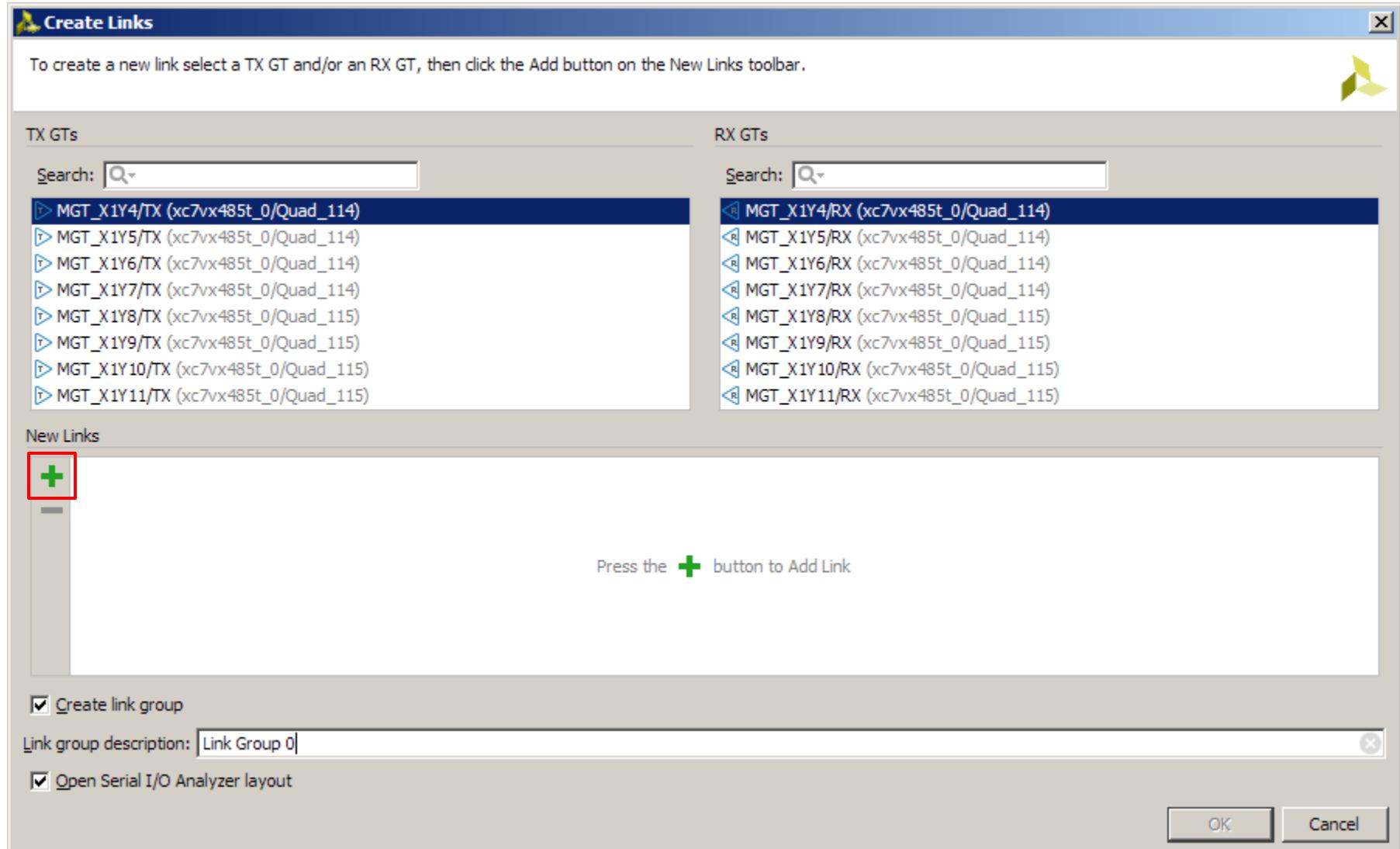
# Run IBERT Example Design

## ► Click Create links



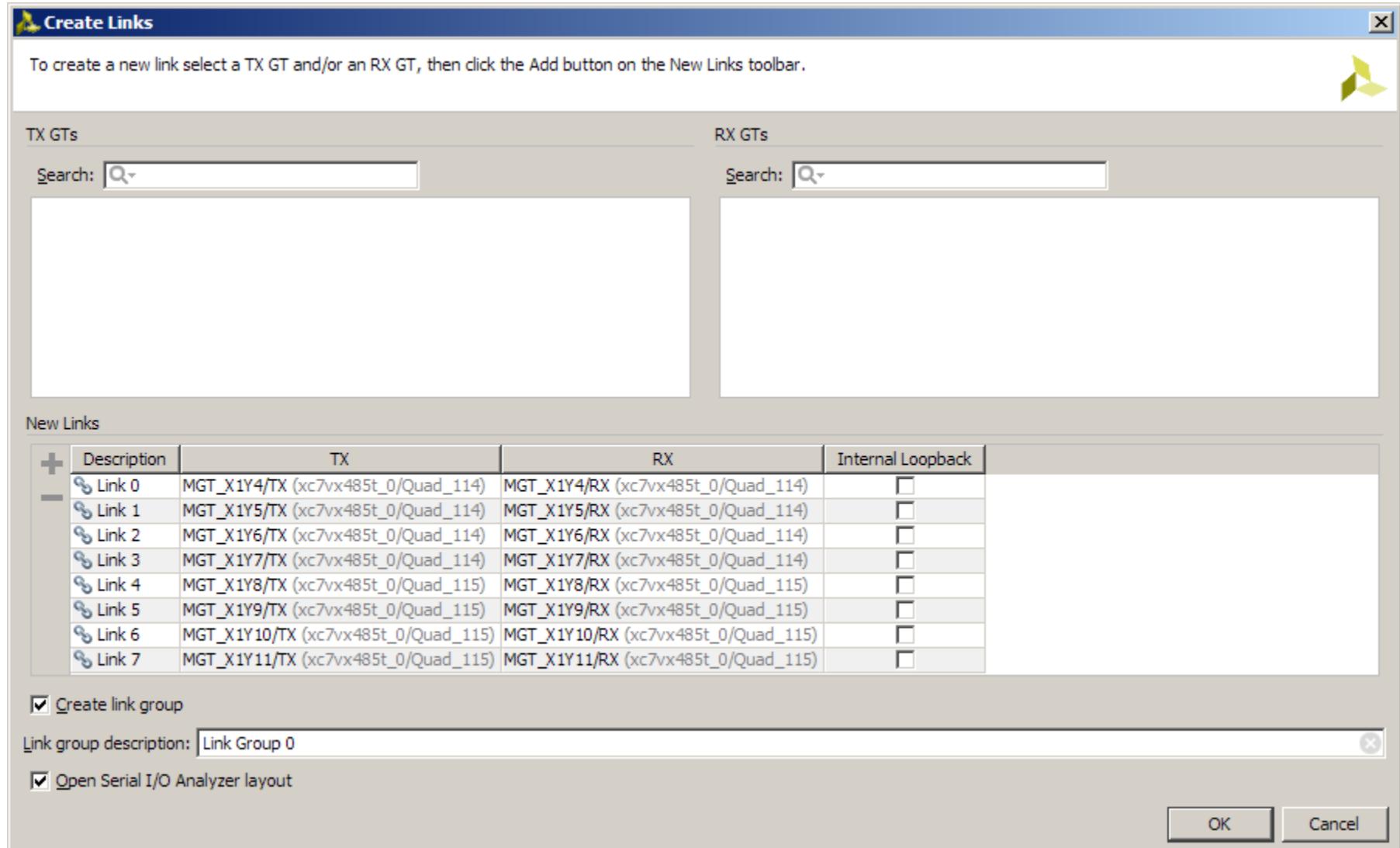
# Run IBERT Example Design

► Click on the Add Link button until all the MGT pairs are “linked”



# Run IBERT Example Design

► Click OK



# Run IBERT Example Design

► The IBERT data appears as seen below

The screenshot shows the Vivado 2015.1 Hardware Manager interface for the project "ibert\_bank\_114\_115\_example". The main window displays the "Serial I/O Links" configuration table. The table has columns for Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and a final column partially visible. The table lists 8 Link Groups under "Link Group 0", each containing 8 links (Link 0 to Link 7). All links are configured with MGT\_X1Y4/TX and MGT\_X1Y4/RX, operating at 5.000 Gbps. The "Status" column shows values like 1.938E11, 1.939E11, etc. The "Bits" column shows values like 1.938E11, 1.939E11, etc. The "Errors" column shows values like 0E0, 0E0, etc. The "BER" column shows values like 5.16E-12, 5.157E-12, etc. The "BERT Reset" column contains "Reset" buttons. The "TX Pattern" and "RX Pattern" columns show "PRBS 7-bit" dropdown menus. The "TX Pre-Cursor" column shows values like 1.67 dB (00111), 1.67 dB (00111), etc. The "Hardware Manager" title bar indicates the connection is to "localhost/xilinx\_tcf/Digilent/210203340506A". The bottom navigation bar includes tabs for Tcl Console, Messages, Serial I/O Links (which is selected), and Serial I/O Scans.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor
Ungrouped Links (0)										
Link Group 0 (8)										
Link 0	MGT_X1Y4/TX	MGT_X1Y4/RX	5.000 Gbps	1.938E11	0E0	5.16E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)
Link 1	MGT_X1Y5/TX	MGT_X1Y5/RX	5.000 Gbps	1.939E11	0E0	5.157E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)
Link 2	MGT_X1Y6/TX	MGT_X1Y6/RX	5.000 Gbps	1.941E11	0E0	5.153E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)
Link 3	MGT_X1Y7/TX	MGT_X1Y7/RX	5.000 Gbps	1.944E11	0E0	5.145E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)
Link 4	MGT_X1Y8/TX	MGT_X1Y8/RX	5.000 Gbps	1.945E11	0E0	5.14E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)
Link 5	MGT_X1Y9/TX	MGT_X1Y9/RX	5.000 Gbps	1.947E11	0E0	5.136E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)
Link 6	MGT_X1Y10/TX	MGT_X1Y10/RX	5.000 Gbps	1.949E11	0E0	5.131E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)
Link 7	MGT_X1Y11/TX	MGT_X1Y11/RX	5.000 Gbps	1.95E11	0E0	5.127E-12	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)

# Run IBERT Example Design

- ▶ Set the TX and RX Pattern to PRBS 31-bit

The screenshot shows the Vivado 2015.1 Hardware Manager interface for the "ibert\_bank\_114\_115\_example" project. The main window displays the "Serial I/O Links" configuration table. The table has columns for Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and TX Post-Cursor. The TX Pattern column for Link 0 is currently set to "PRBS 31-bit", which is highlighted with a blue selection bar. Other options in this column include "PRBS 7-bit", "PRBS 15-bit", "PRBS 23-bit", "Fast Clk", and "Slow Clk". The RX Pattern column for Link 0 is set to "PRBS 7-bit". The TX Pre-Cursor and TX Post-Cursor columns for Link 0 are both set to "0.6". The table also lists other links from Link 1 to Link 7, each with similar parameters. The "Hardware Manager" tab is selected at the bottom of the interface.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	
Ungrouped Links (0)												
Link Group 0 (8)								Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.6
Link 0	MGT_X1Y4/TX	MGT_X1Y4/RX	5.000 Gbps	2.729E11	0E0	3.665E-12	Reset	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.6
Link 1	MGT_X1Y5/TX	MGT_X1Y5/RX	5.000 Gbps	2.73E11	0E0	3.664E-12	Reset	PRBS 15-bit	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.6
Link 2	MGT_X1Y6/TX	MGT_X1Y6/RX	5.000 Gbps	2.731E11	0E0	3.661E-12	Reset	PRBS 23-bit	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.6
Link 3	MGT_X1Y7/TX	MGT_X1Y7/RX	5.000 Gbps	2.733E11	0E0	3.659E-12	Reset	PRBS 31-bit	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.6
Link 4	MGT_X1Y8/TX	MGT_X1Y8/RX	5.000 Gbps	2.734E11	0E0	3.657E-12	Reset	Fast Clk	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.6
Link 5	MGT_X1Y9/TX	MGT_X1Y9/RX	5.000 Gbps	2.736E11	0E0	3.655E-12	Reset	Slow Clk	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.6
Link 6	MGT_X1Y10/TX	MGT_X1Y10/RX	5.000 Gbps	2.739E11	0E0	3.651E-12	Reset	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.6
Link 7	MGT_X1Y11/TX	MGT_X1Y11/RX	5.000 Gbps	2.741E11	0E0	3.649E-12	Reset	PRBS 7-bit	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.6

Link Group: Link Group 0

Note: Presentation applies to the VC707

XILINX ➤ ALL PROGRAMMABLE™

# Run IBERT Example Design

► Now all eight links are set to a RX Pattern of PRBS 31-bit

The screenshot shows the Vivado 2015.1 Hardware Manager interface for the 'ibert\_bank\_114\_115\_example' project. The main window displays the 'Serial I/O Links' table. The table has columns for Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and TX Post-Cursor. A red box highlights the 'RX Pattern' column for all 8 links, which are all set to 'PRBS 31-bit'. The TX column shows various MGT\_X1Yx/TX and MGT\_X1Yx/RX pairs. The RX column shows various MGT\_X1Yx/RX pairs. The RX Pattern column for all 8 links is highlighted with a red border and shows 'PRBS 31-bit'.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor
Ungrouped Links (0)											
Link Group 0 (8)											
Link 0	MGT_X1Y4/TX	MGT_X1Y4/RX	5.000 Gbps	3.775E11	5.801E9	1.537E-2	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.6
Link 1	MGT_X1Y5/TX	MGT_X1Y5/RX	5.000 Gbps	3.777E11	5.801E9	1.536E-2	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.6
Link 2	MGT_X1Y6/TX	MGT_X1Y6/RX	5.000 Gbps	3.778E11	5.8E9	1.535E-2	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.6
Link 3	MGT_X1Y7/TX	MGT_X1Y7/RX	5.000 Gbps	3.78E11	5.801E9	1.535E-2	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.6
Link 4	MGT_X1Y8/TX	MGT_X1Y8/RX	5.000 Gbps	3.782E11	5.8E9	1.534E-2	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.6
Link 5	MGT_X1Y9/TX	MGT_X1Y9/RX	5.000 Gbps	3.783E11	5.807E9	1.535E-2	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.6
Link 6	MGT_X1Y10/TX	MGT_X1Y10/RX	5.000 Gbps	3.785E11	5.941E9	1.57E-2	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.6
Link 7	MGT_X1Y11/TX	MGT_X1Y11/RX	5.000 Gbps	3.787E11	5.942E9	1.569E-2	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)	0.6

# Run IBERT Example Design

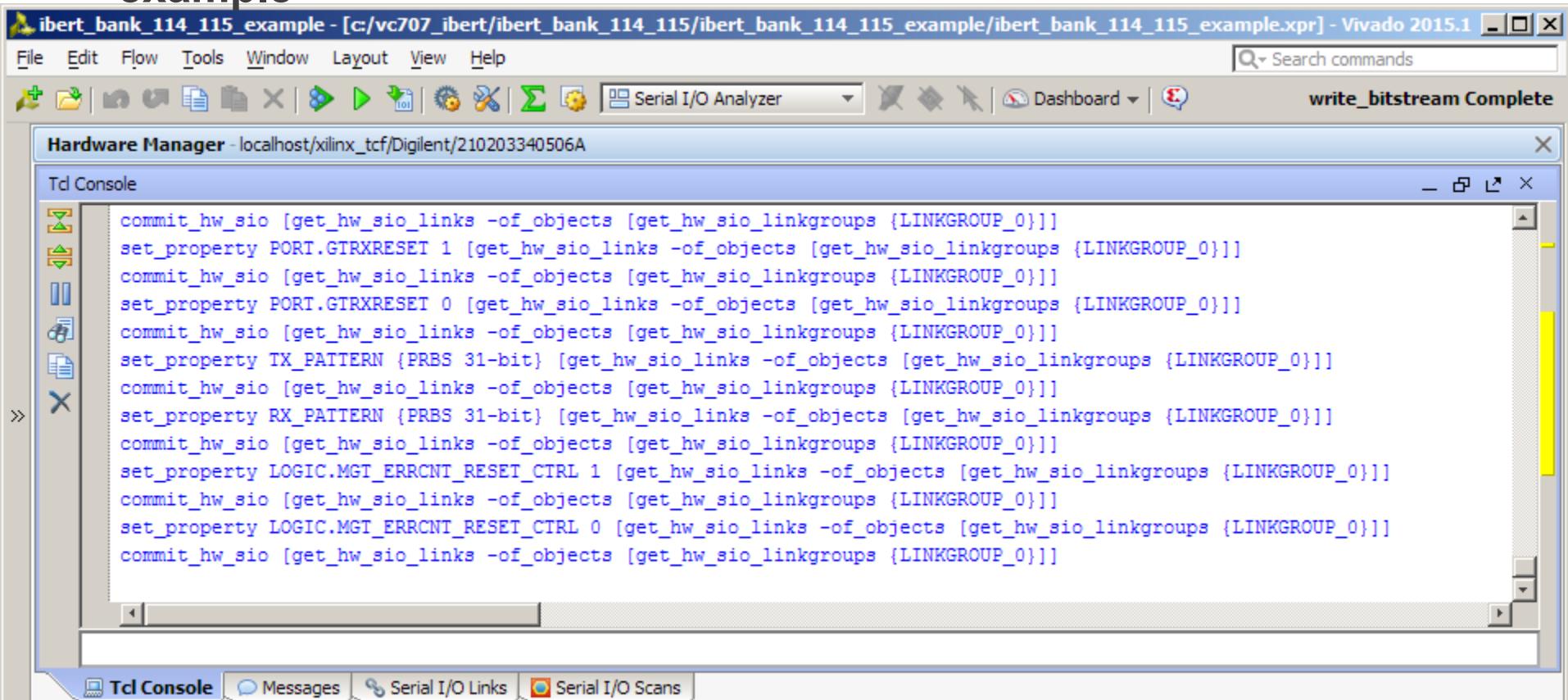
► Click the BERT Reset button for Link Group 0 to reset all eight links

The screenshot shows the Vivado 2015.1 Hardware Manager interface for the 'ibert\_bank\_114\_115\_example' project. The main window displays the 'Serial I/O Links' table. The table has columns for Name, TX, RX, Status, Bits, Errors, BER, BERT Reset, TX Pattern, RX Pattern, TX Pre-Cursor, and various dB and dBm values. A red box highlights the 'Reset' button for Link 0 under 'Link Group 0'. The table data is as follows:

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor
Ungrouped Links (0)										
Link Group 0 (8)										
Link 0	MGT_X1Y4/TX	MGT_X1Y4/RX	5.000 Gbps	2.363E10	0E0	4.232E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)
Link 1	MGT_X1Y5/TX	MGT_X1Y5/RX	5.000 Gbps	1.715E10	0E0	5.83E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)
Link 2	MGT_X1Y6/TX	MGT_X1Y6/RX	5.000 Gbps	1.756E10	0E0	5.694E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)
Link 3	MGT_X1Y7/TX	MGT_X1Y7/RX	5.000 Gbps	1.775E10	0E0	5.634E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)
Link 4	MGT_X1Y8/TX	MGT_X1Y8/RX	5.000 Gbps	1.79E10	0E0	5.586E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)
Link 5	MGT_X1Y9/TX	MGT_X1Y9/RX	5.000 Gbps	1.807E10	0E0	5.535E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)
Link 6	MGT_X1Y10/TX	MGT_X1Y10/RX	5.000 Gbps	1.827E10	0E0	5.472E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)
Link 7	MGT_X1Y11/TX	MGT_X1Y11/RX	5.000 Gbps	1.843E10	0E0	5.425E-11	Reset	PRBS 31-bit	PRBS 31-bit	1.67 dB (00111)

# Run IBERT Example Design

- The Hardware Manager Tcl commands can be captured from the Tcl console; these can be used for scripting this test
- Review `ready_for_download/ibert_bank_114_115_hw.tcl` for an example



The screenshot shows the Vivado 2015.1 interface with the title bar "ibert\_bank\_114\_115\_example - [c:/vc707\_ibert/ibert\_bank\_114\_115/ibert\_bank\_114\_115\_example/ibert\_bank\_114\_115\_example.xpr] - Vivado 2015.1". The menu bar includes File, Edit, Flow, Tools, Window, Layout, View, Help. The toolbar includes icons for New, Open, Save, Close, Run, Stop, and others. The main window is titled "Hardware Manager - localhost/xilinx\_tcf/Digilent/210203340506A". The "Tcl Console" tab is active, displaying the following Tcl script:

```
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
set_property PORT.GTRXRESET 1 [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
set_property PORT.GTRXRESET 0 [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
set_property TX_PATTERN {PRBS 31-bit} [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
set_property RX_PATTERN {PRBS 31-bit} [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
set_property LOGIC.MGT_ERRCNT_RESET_CTRL 1 [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
set_property LOGIC.MGT_ERRCNT_RESET_CTRL 0 [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]  
commit_hw_sio [get_hw_sio_links -of_objects [get_hw_sio_linkgroups {LINKGROUP_0}]]
```

## References

# References

## ► IBERT IP

- LogiCORE IP Integrated Bit Error Ratio Tester for 7 Series GTX – PG132
  - [http://www.xilinx.com/support/documentation/ip\\_documentation/ibert\\_7series\\_gtx/v3\\_0/pg132-ibert-7series-gtx.pdf](http://www.xilinx.com/support/documentation/ip_documentation/ibert_7series_gtx/v3_0/pg132-ibert-7series-gtx.pdf)

## ► Vivado Release Notes

- Vivado Design Suite User Guide - Release Notes – UG973
  - [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2015\\_1/ug973-vivado-release-notes-install-license.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_1/ug973-vivado-release-notes-install-license.pdf)
- Vivado Design Suite 2015.x - Vivado Known Issues
  - <http://www.xilinx.com/support/answers/63538.html>

## ► Vivado Programming and Debugging

- Vivado Design Suite Programming and Debugging User Guide – UG908
  - [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2015\\_1/ug908-vivado-programming-debugging.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx2015_1/ug908-vivado-programming-debugging.pdf)

# Documentation

# Documentation

## ➤ Virtex-7

- Virtex-7 FPGA Family
  - <http://www.xilinx.com/products/silicon-devices/fpga/virtex-7/index.htm>
- Design Advisory Master Answer Record for Virtex-7 FPGAs
  - <http://www.xilinx.com/support/answers/42944.htm>

## ➤ VC707 Documentation

- Virtex-7 FPGA VC707 Evaluation Kit
  - <http://www.xilinx.com/products/boards-and-kits/ek-v7-vc707-g.html>
- VC707 Getting Started Guide – UG848
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ vc707/ug848-VC707-getting-started-guide.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ vc707/ug848-VC707-getting-started-guide.pdf)
- VC707 User Guide – UG885
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/ vc707/ug885\\_VC707\\_Eval\\_Bd.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/ vc707/ug885_VC707_Eval_Bd.pdf)