VC707 IBERT Flow

Field Application Engineer
Adaptive and Embedded Computing Group (AECG)

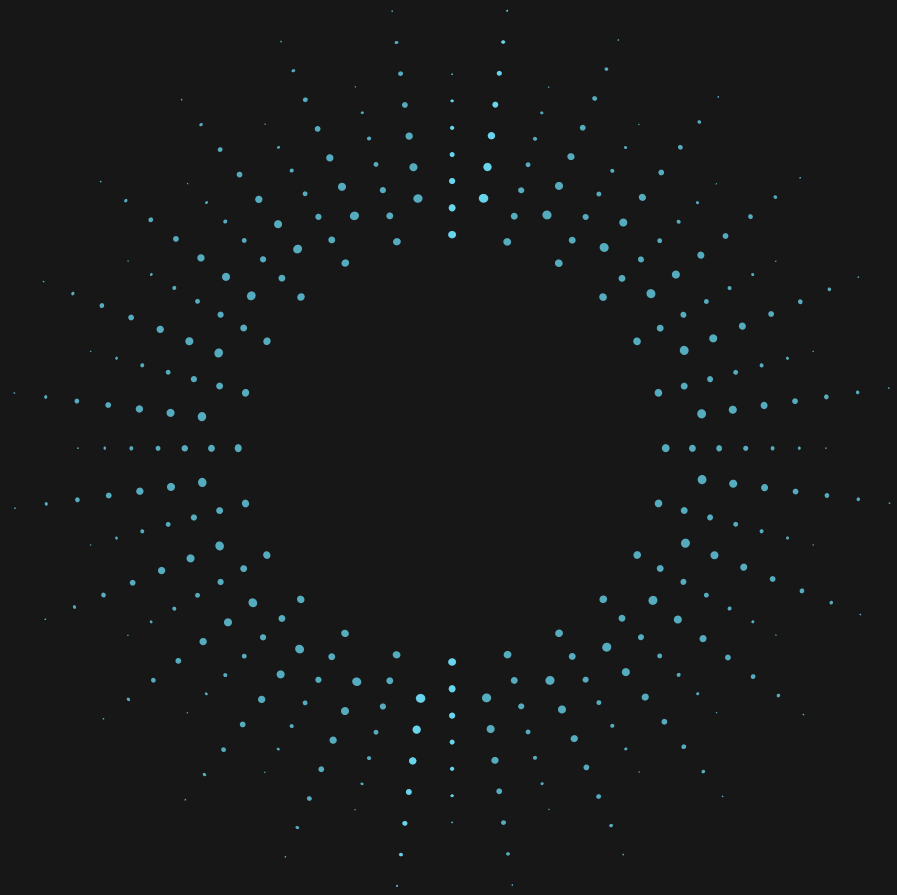
AMD
together we advance_

Revision History

Date	Version	Description
10/25/23	1.0	Initial version for flow introduction.

Vivado 2019.2 Part

version newer than 2019.2 will not support vc707 ibert debug core

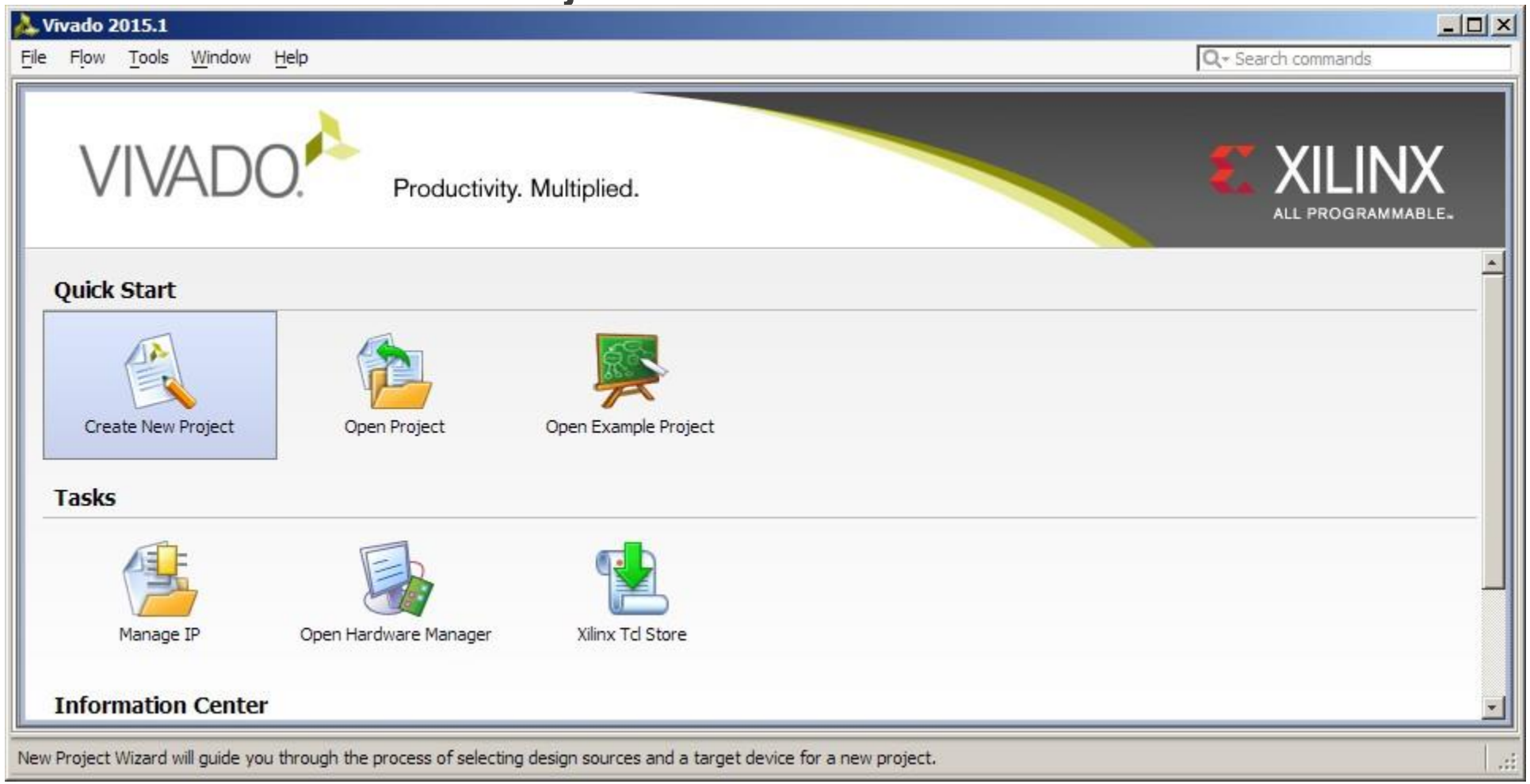


Create IBERT Design for Bank 113

- Open Vivado

  Start → All Programs → Xilinx Design Tools → Vivado 2015.1 → Vivado

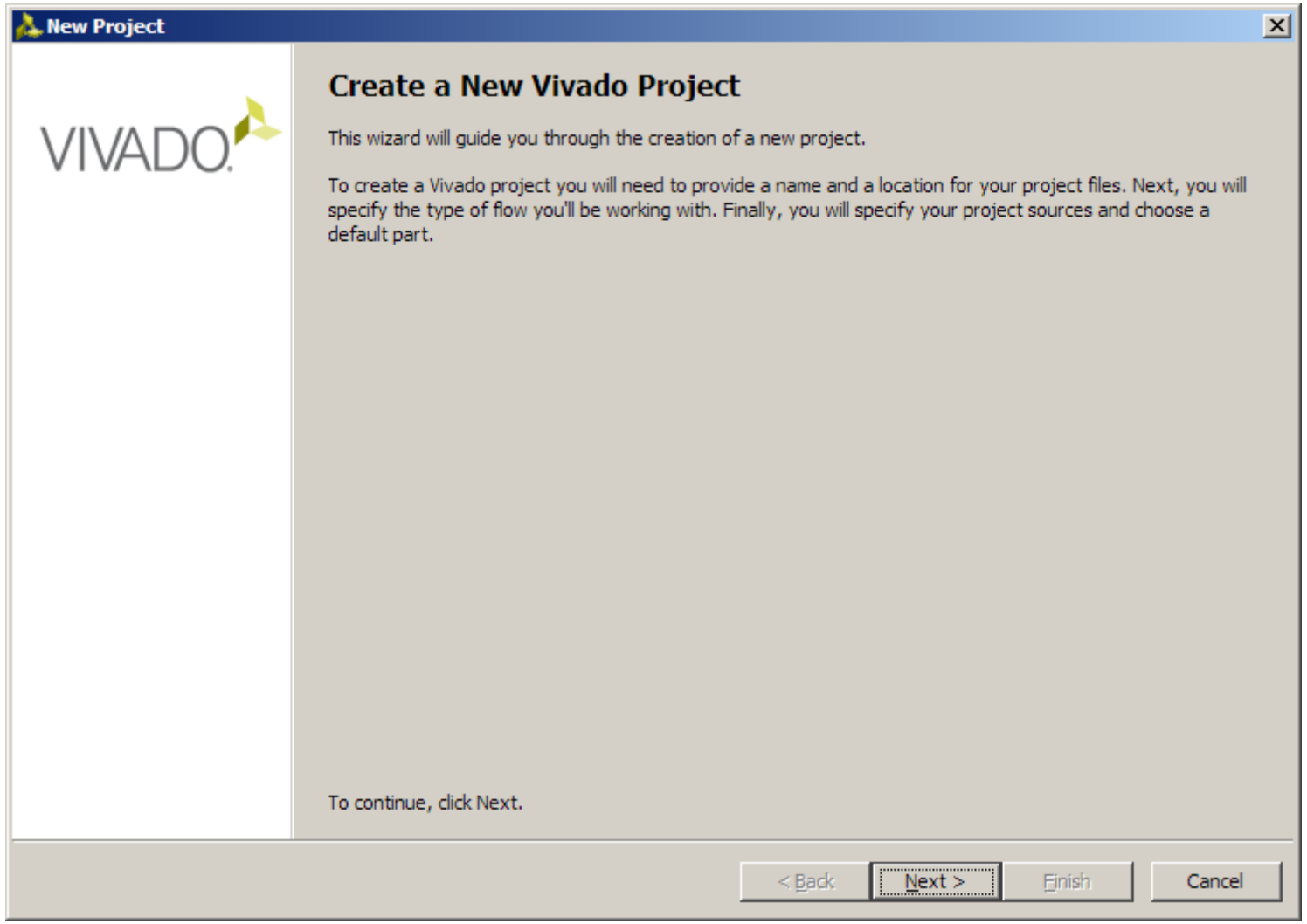
- Select Create New Project



Note: Presentation applies to the VC707

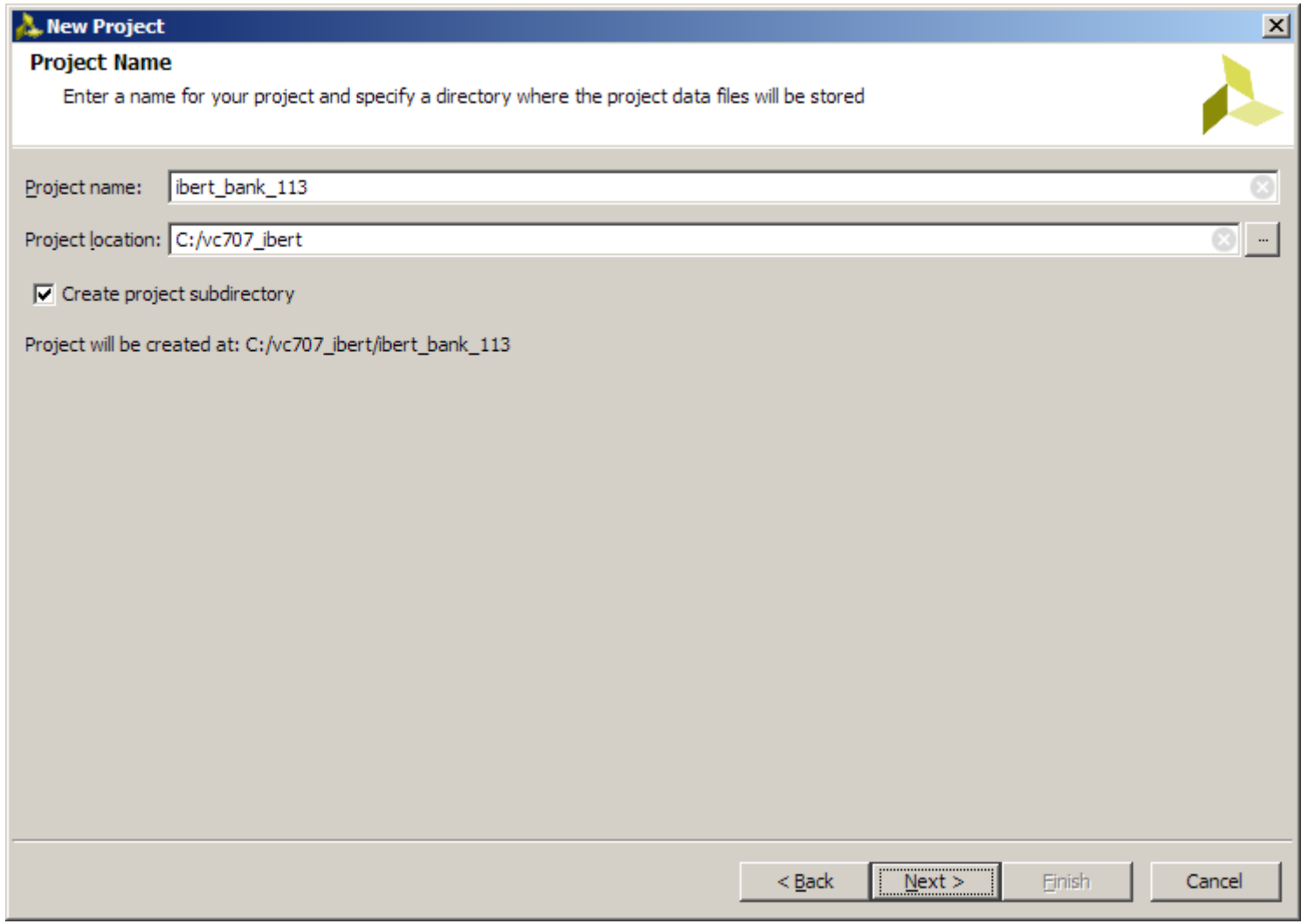
Create IBERT Design for Bank 113

- Click Next



Create IBERT Design for Bank 113

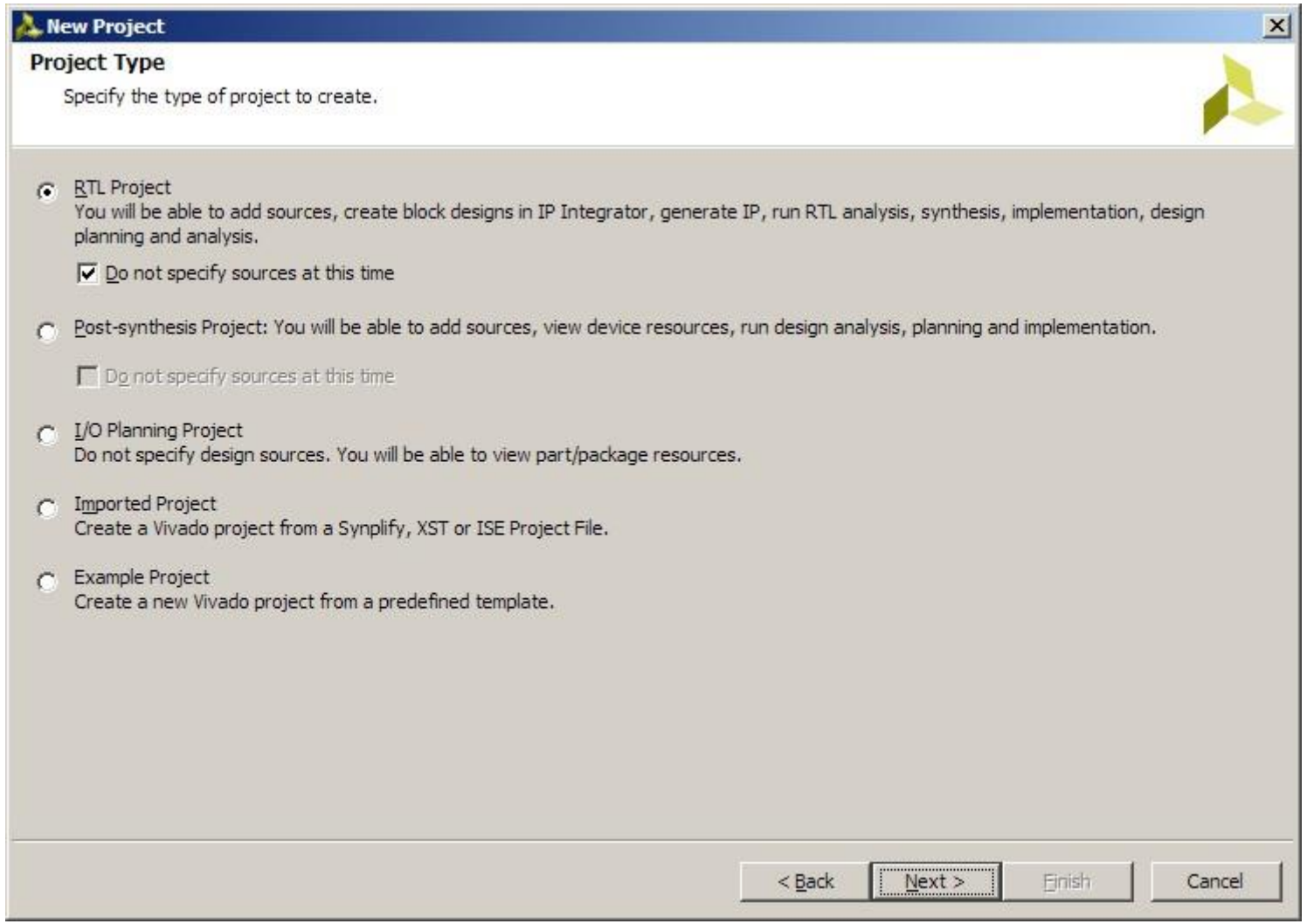
- Set the Project name and location to ibert_bank_113 and C:/vc707_ibert; check Create project subdirectory



Note: Vivado generally requires forward slashes in paths

Create IBERT Design for Bank 113

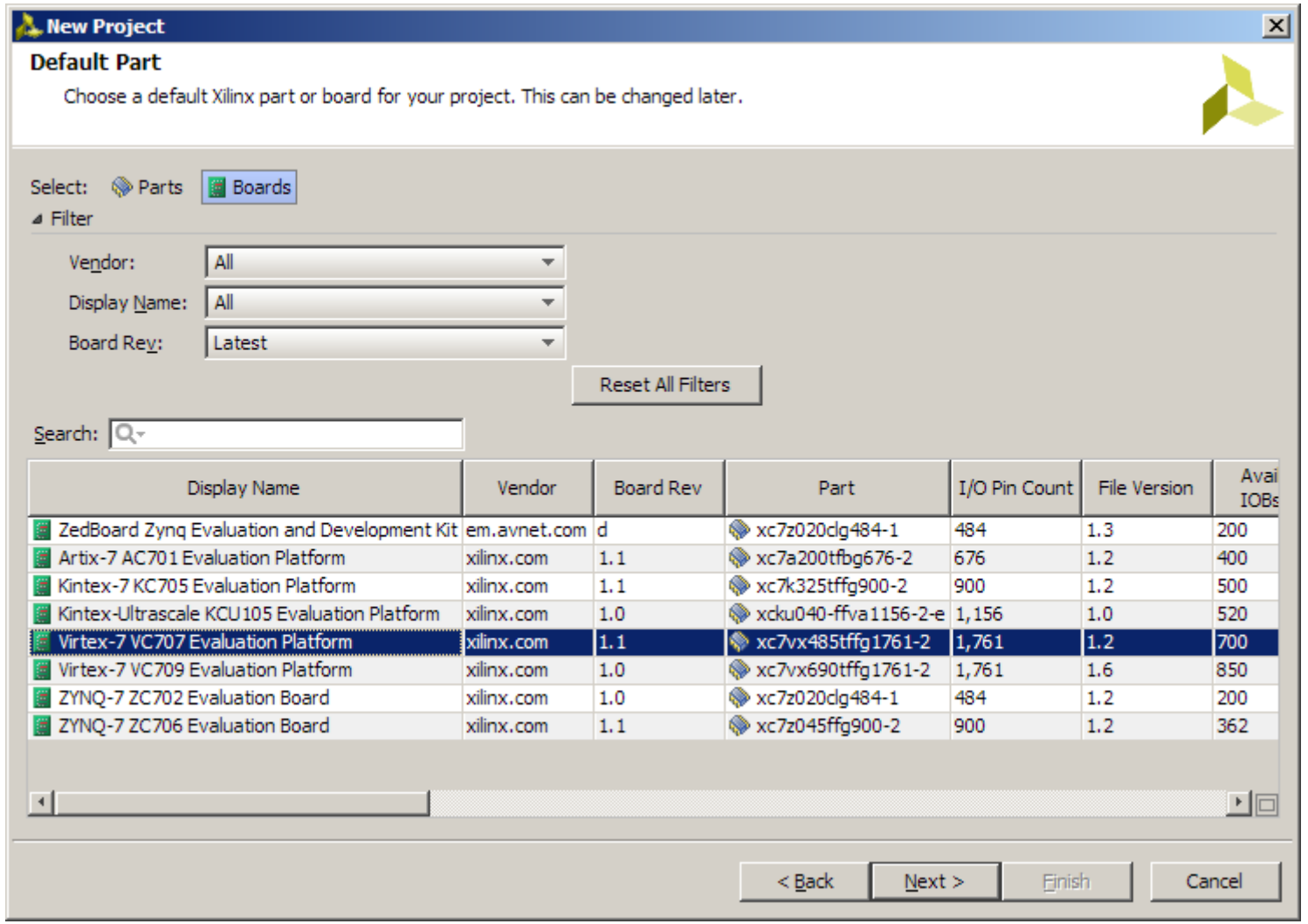
- **Select RTL Project**
  - Select **Do not specify sources at this time**



Note: Presentation applies to the VC707

Create IBERT Design for Bank 113

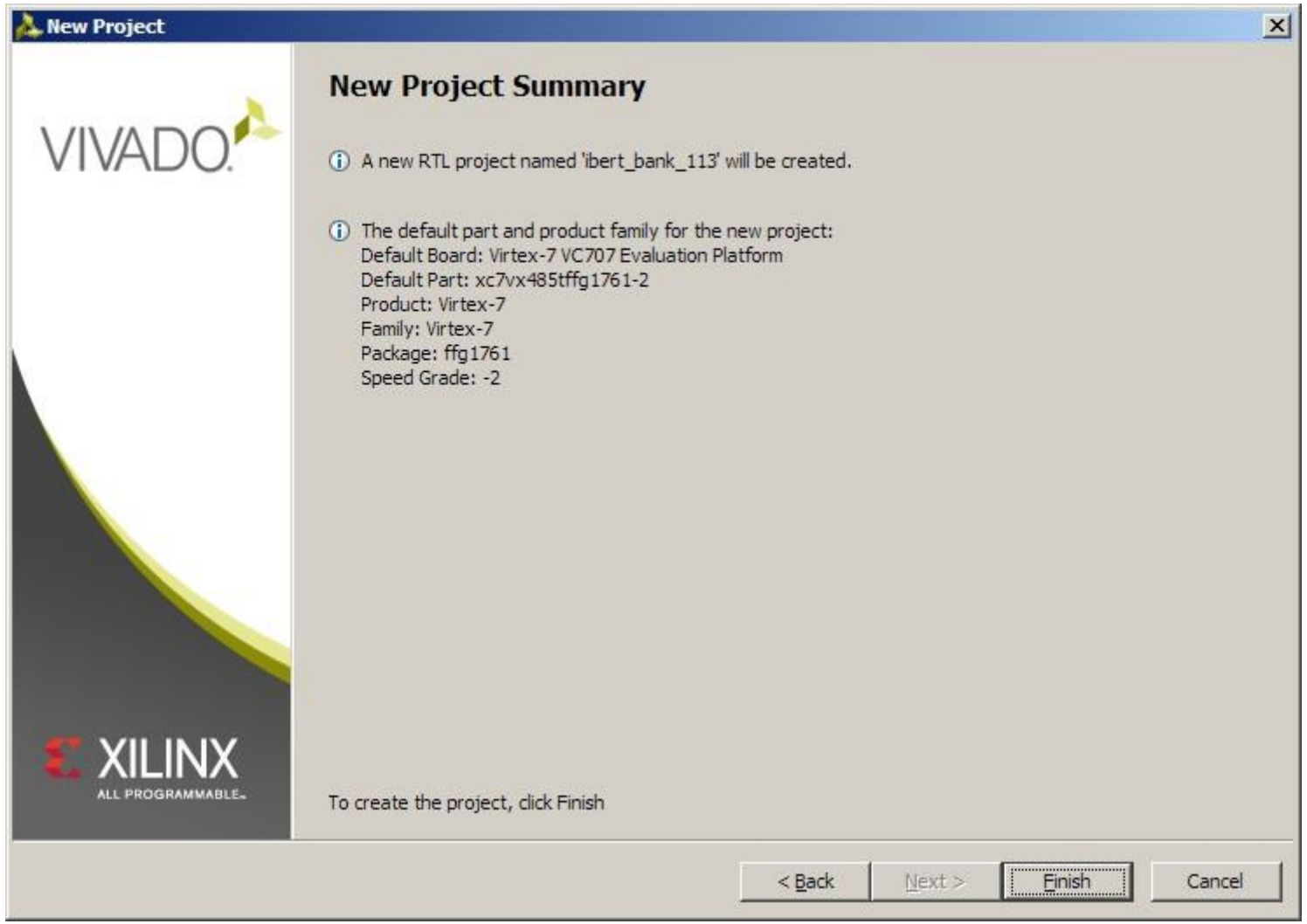
- Select the VC707 Board



Note: Presentation applies to the VC707

Create IBERT Design for Bank 113

- Click Finish



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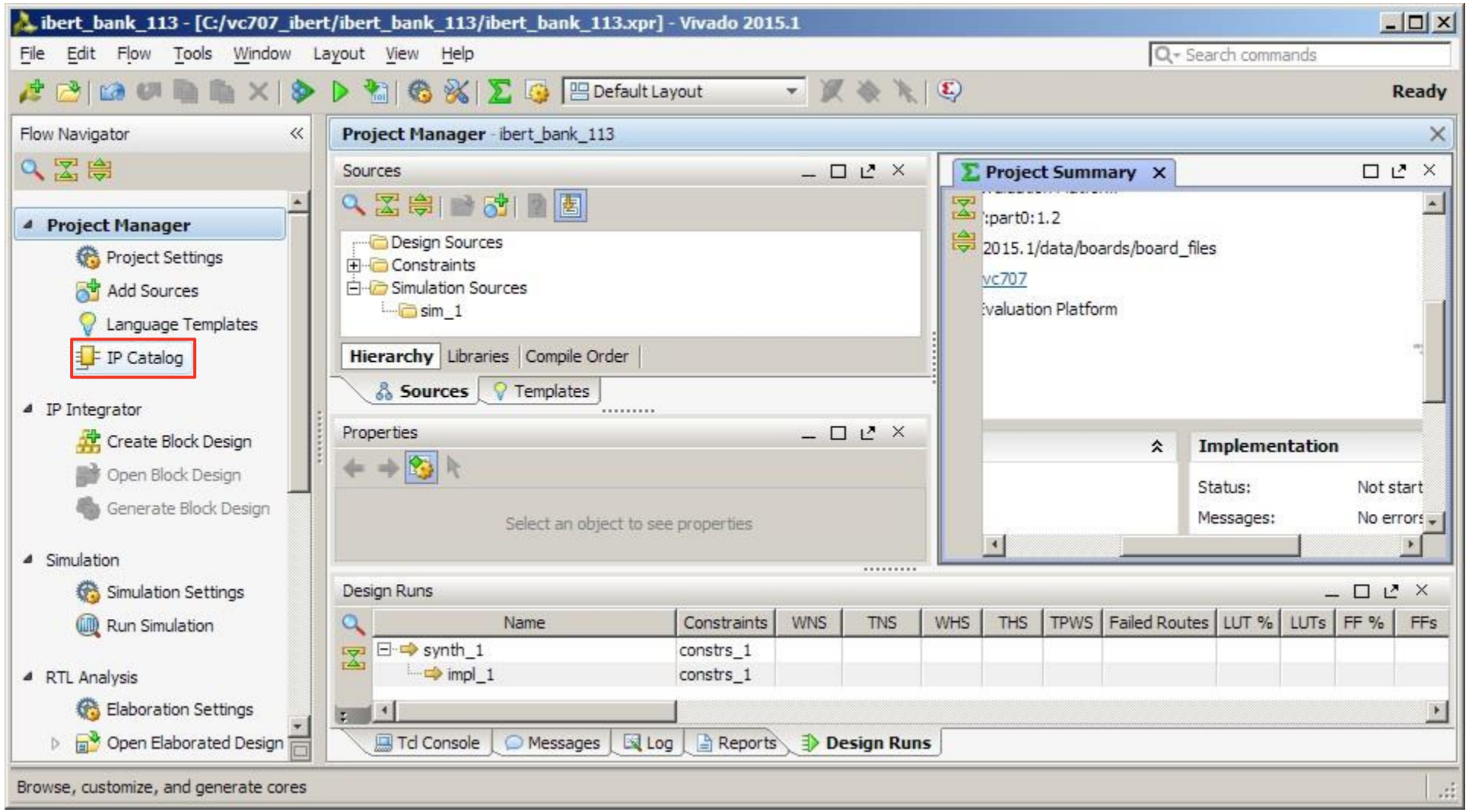
Create IBERT Design for Bank 113

- Click on IP Catalog



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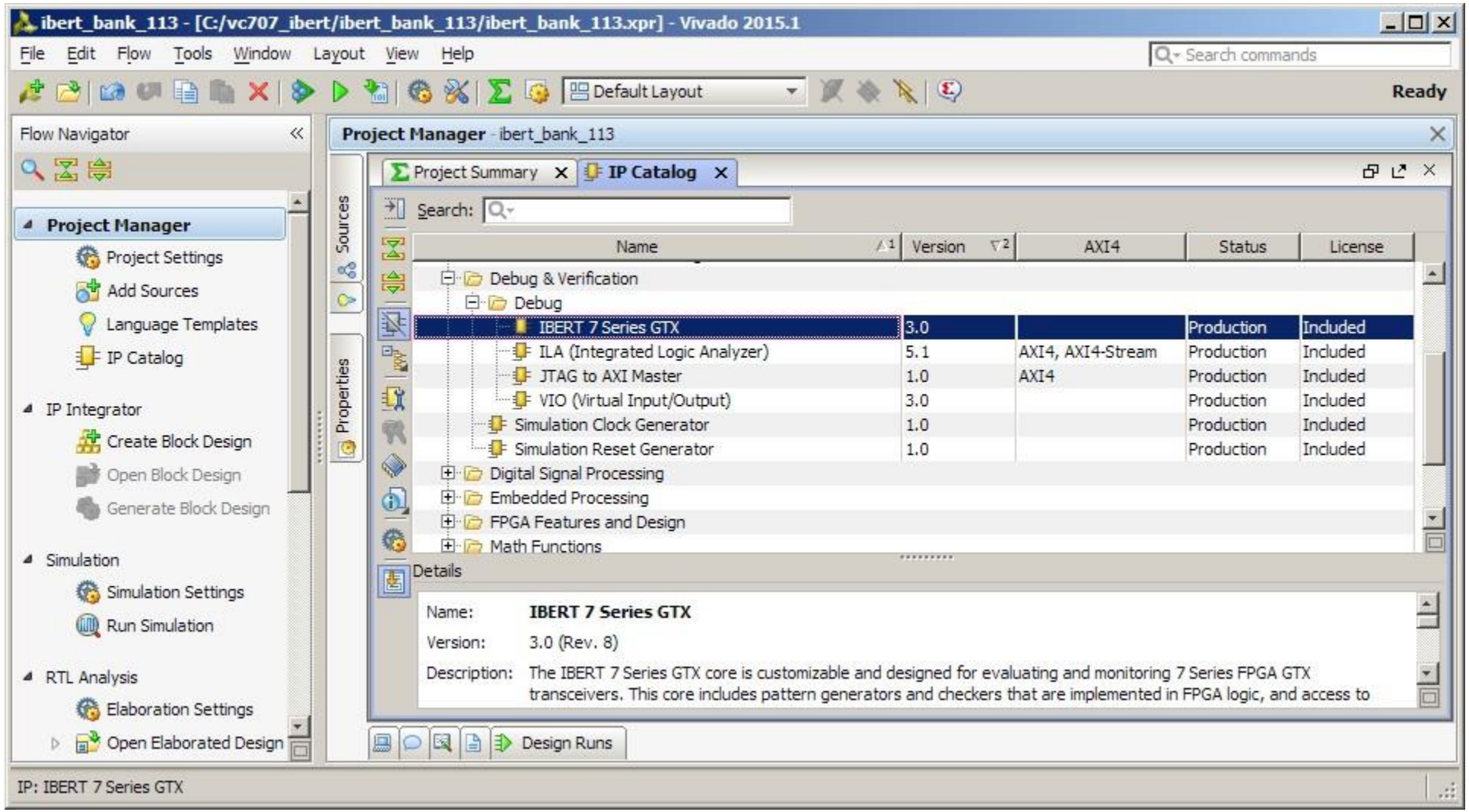
Create IBERT Design for Bank 113

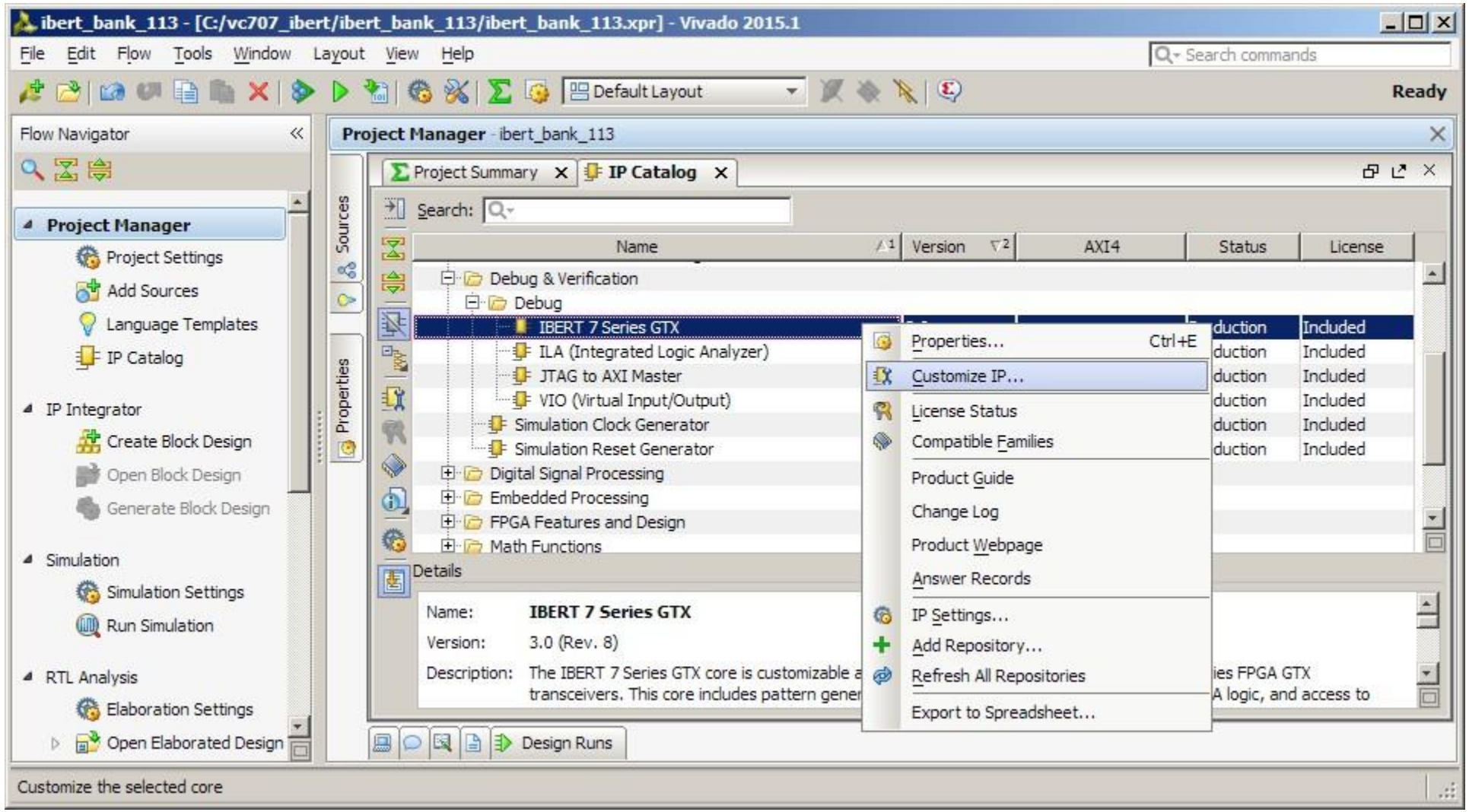
- Select IBERT 7 Series GTX, v3.0 under Debug & Verification



Note: Presentation applies to the VC707

Create IBERT Design for Bank 113

- Right click on IBERT 7 Series GTX and select Customize IP…



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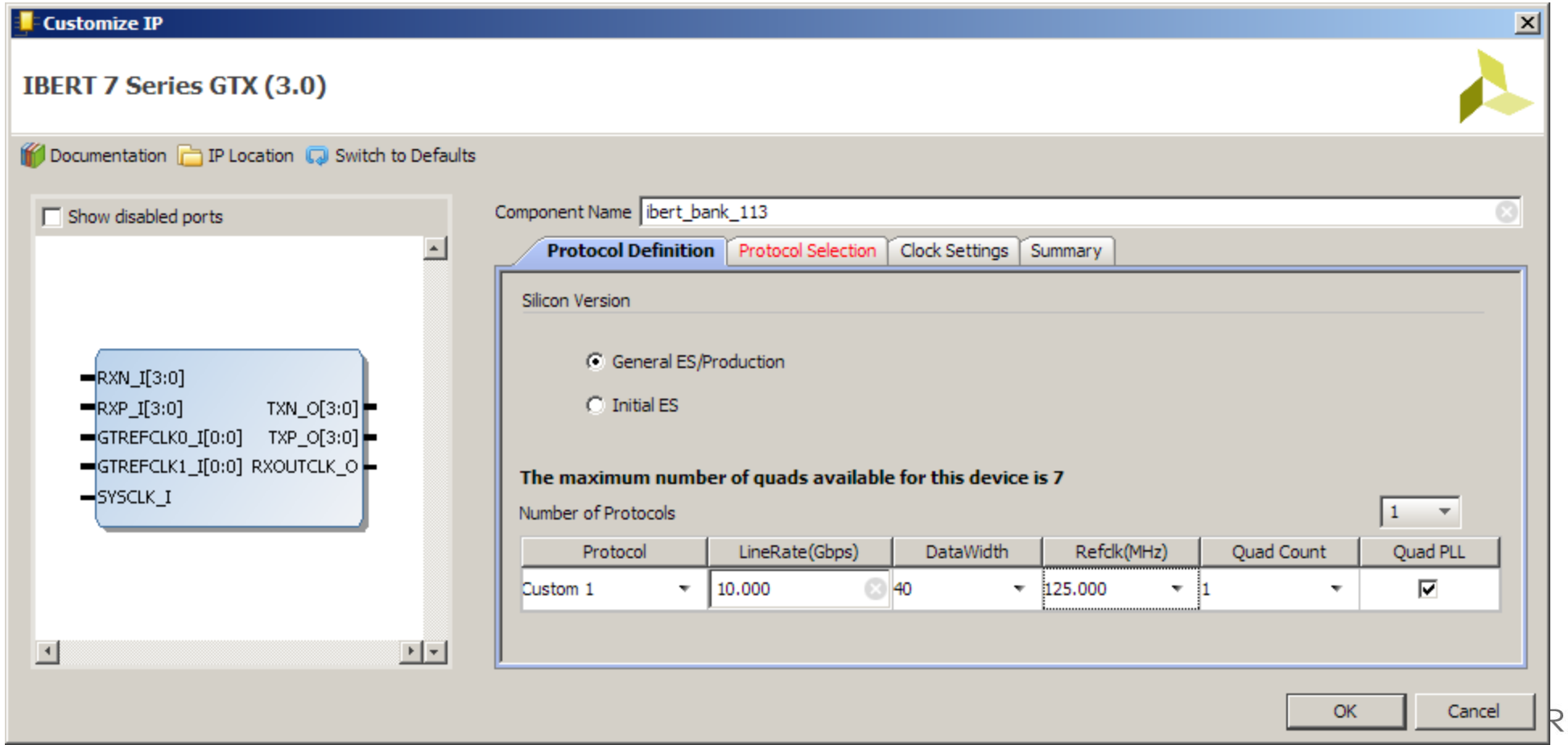
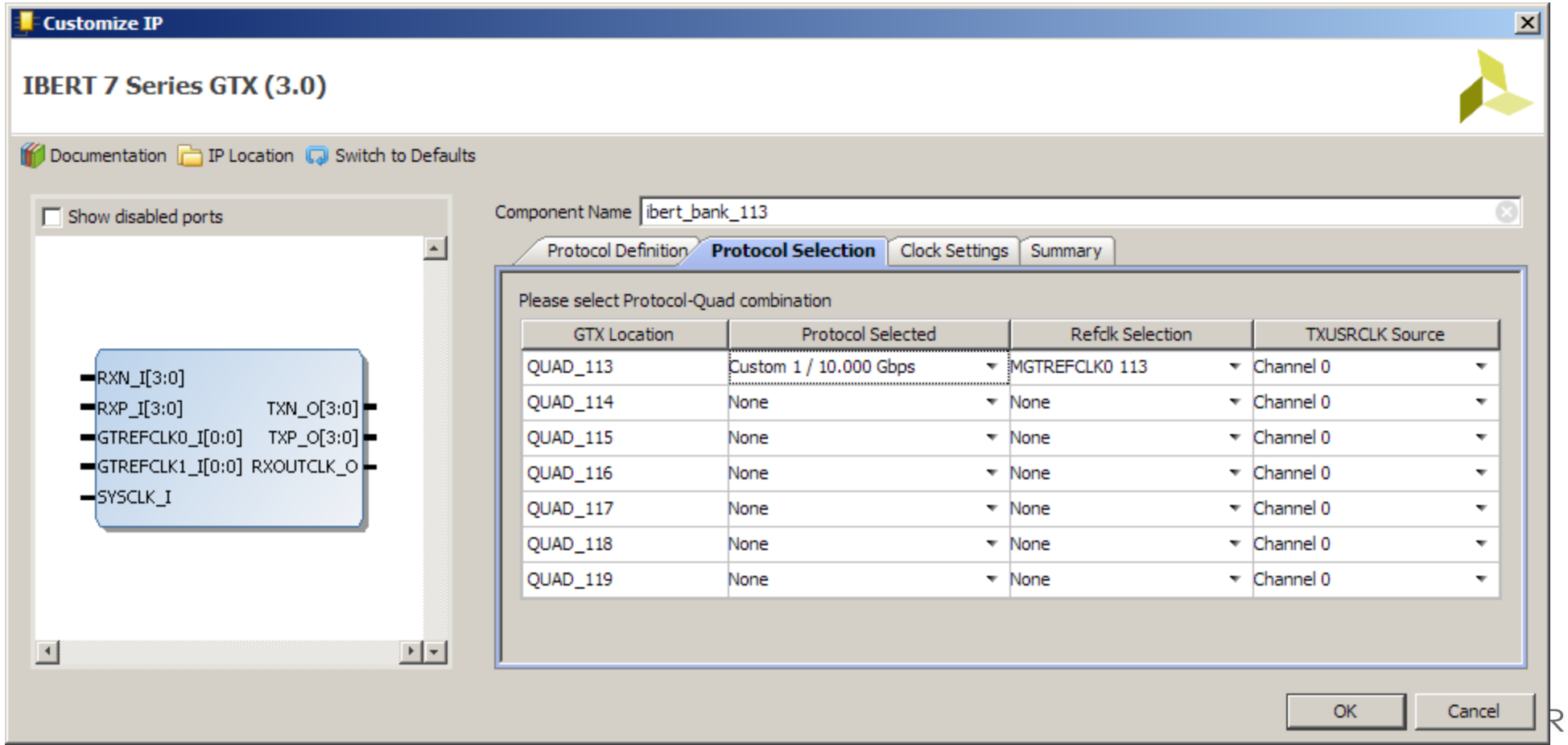
Create IBERT Design for Bank 113

- **Set the Component name: ibert_bank_113**
- **Under the Protocol Definition tab**
  - Silicon Version: **General ES / Production**
  - Protocol: LineRate: **10.000**, DataWidth: **40** Refclk: **125.000** Quad Count: **1**



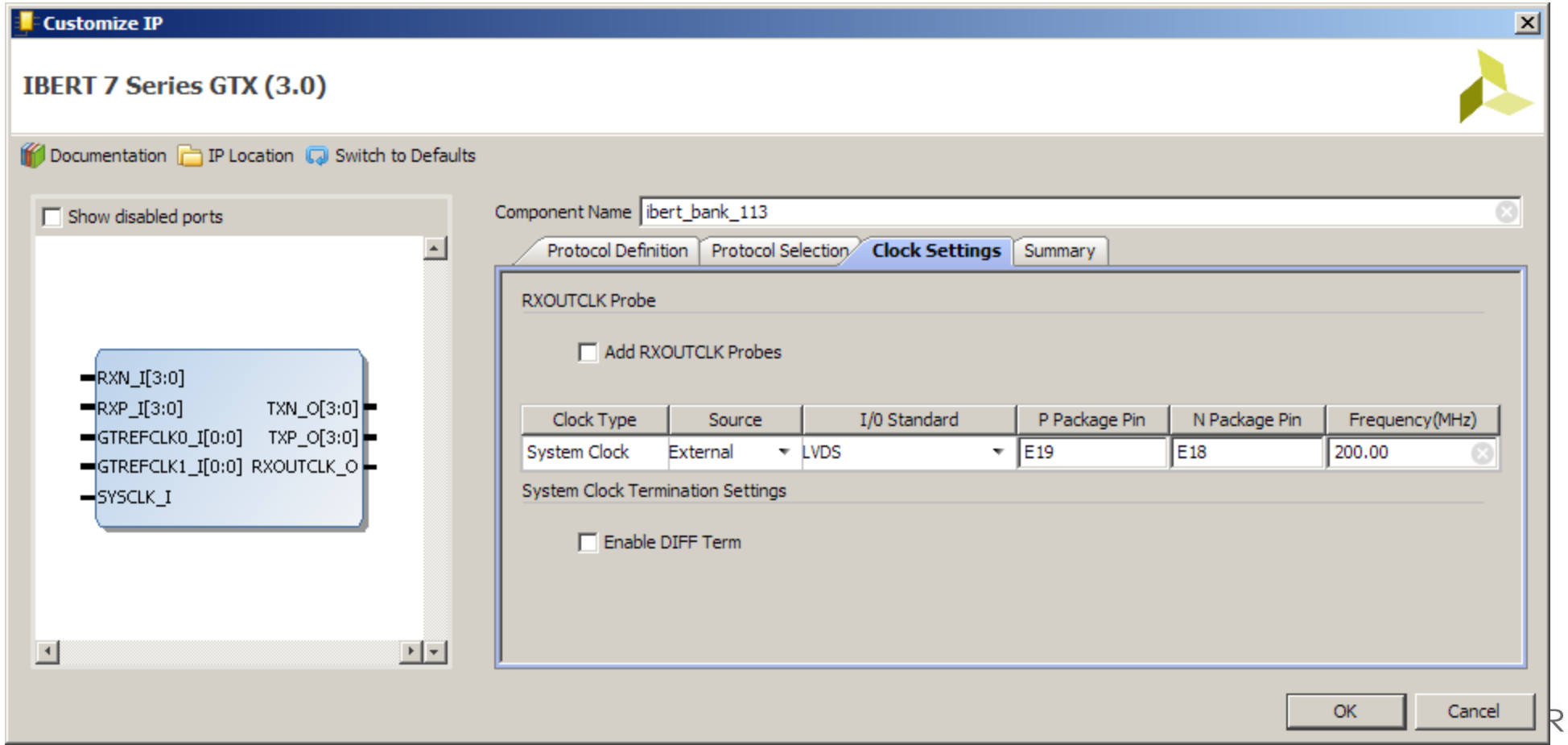
Create IBERT Design for Bank 113

- Under the Protocol Selection tab
- Set QUAD_113 to
  - **Custom 1 / 10.000 Gbps**, and **MGTREFCLK0 113**



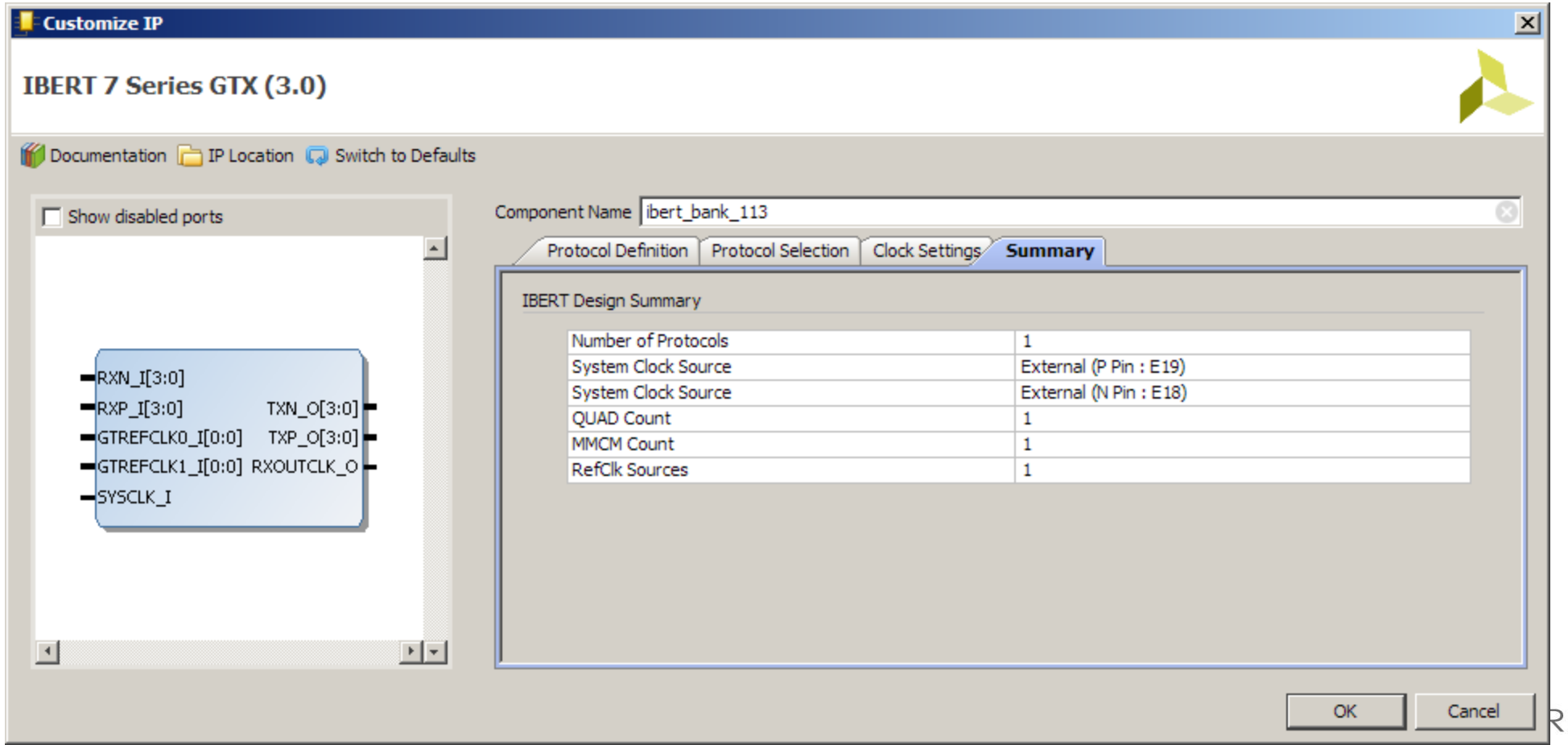
Create IBERT Design for Bank 113

- **Under the Clock Settings tab, set the System Clock:**
  - **LVDS**, P Pin Location: **E19**, N Pin Location: **E18**



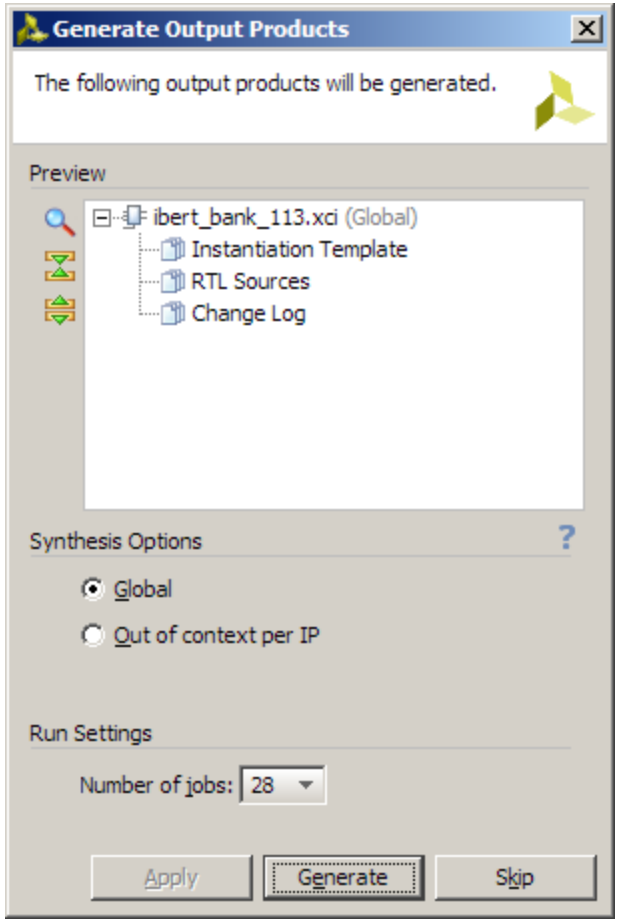
Create IBERT Design for Bank 113

- Review the summary and click OK



Create IBERT Design for Bank 113

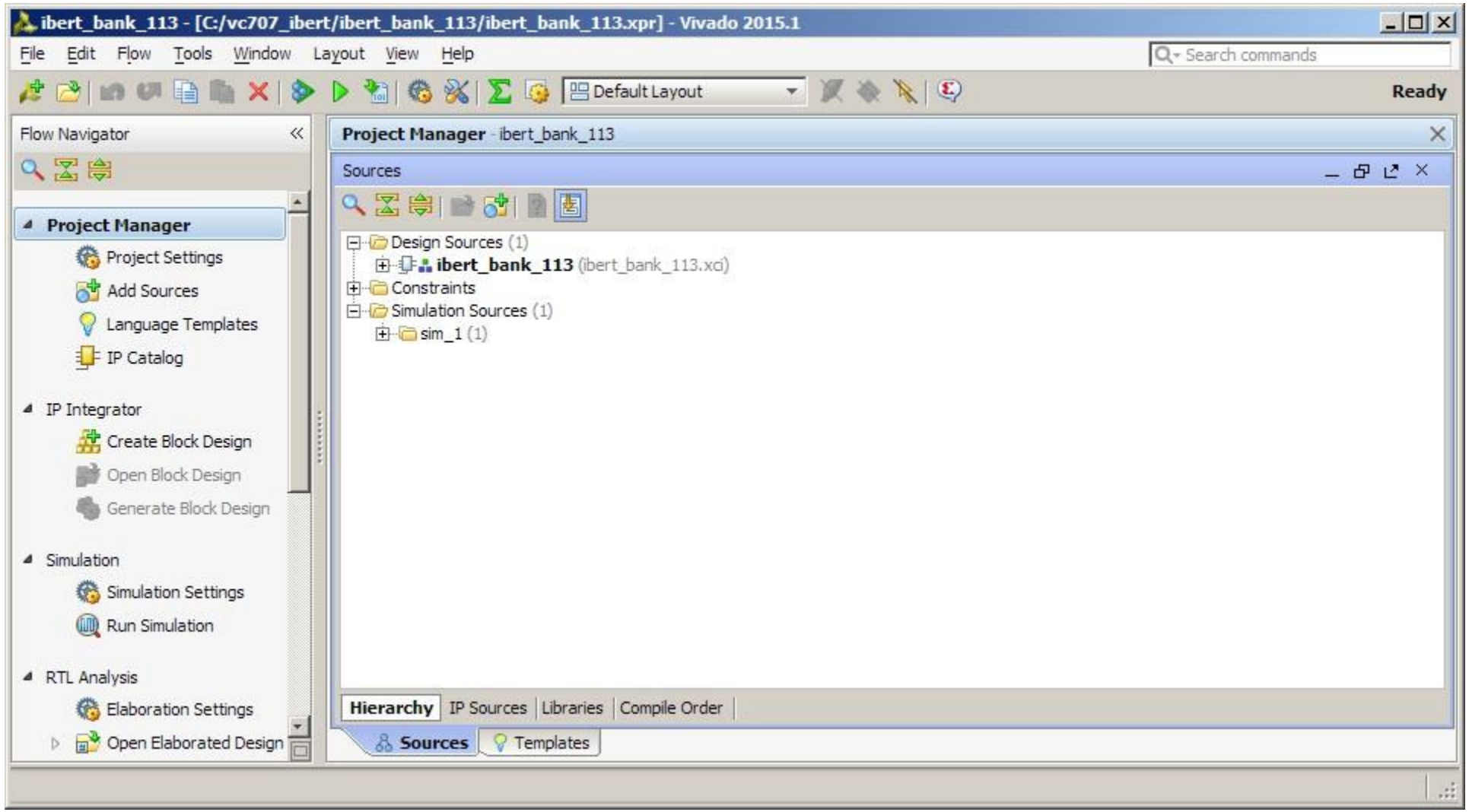
- Click Generate



Note: Presentation applies to the VC707

Create IBERT Design for Bank 113

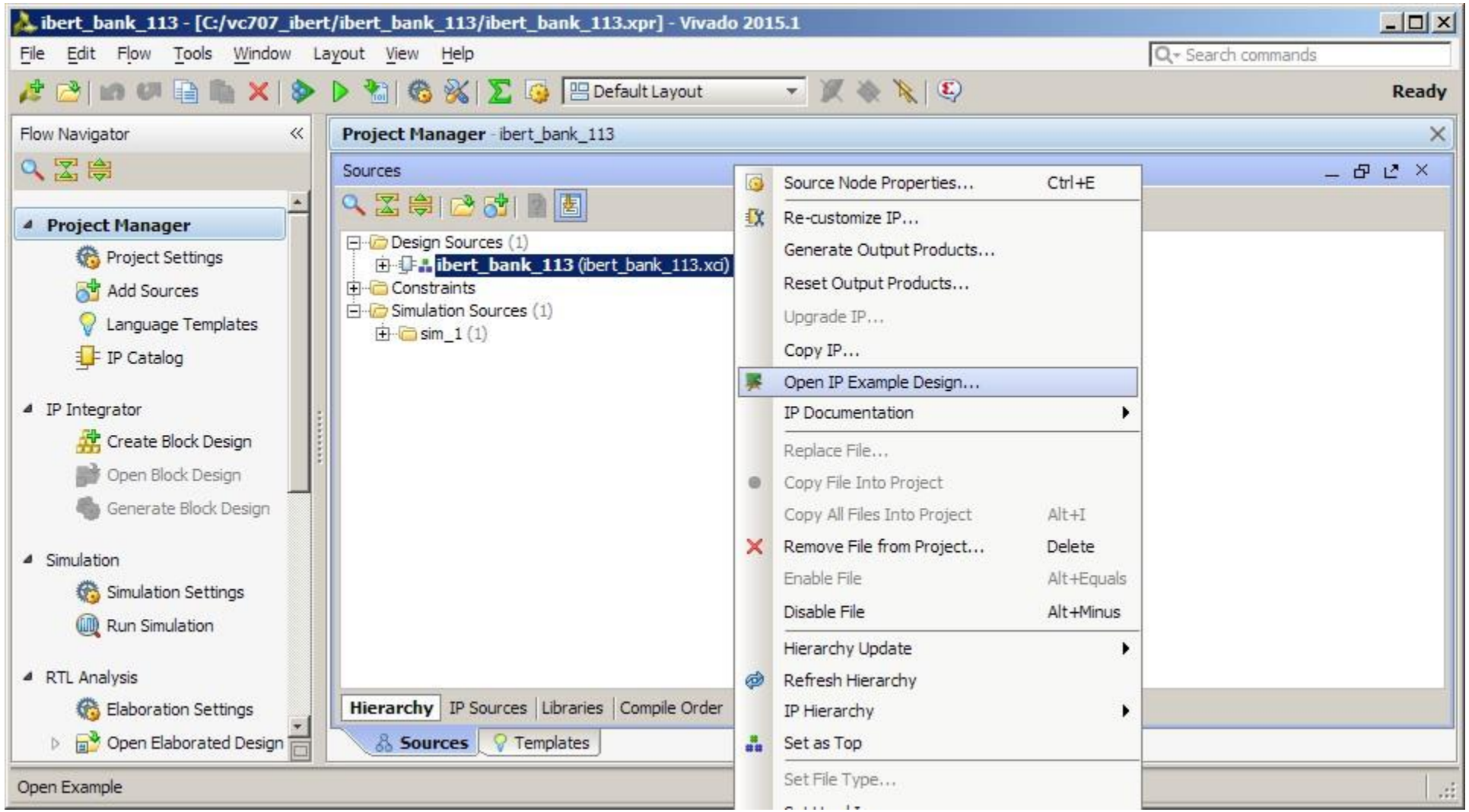
- Bank 113 IBERT design appears in Design Sources



Note: Presentation applies to the VC707

Compile Example Design

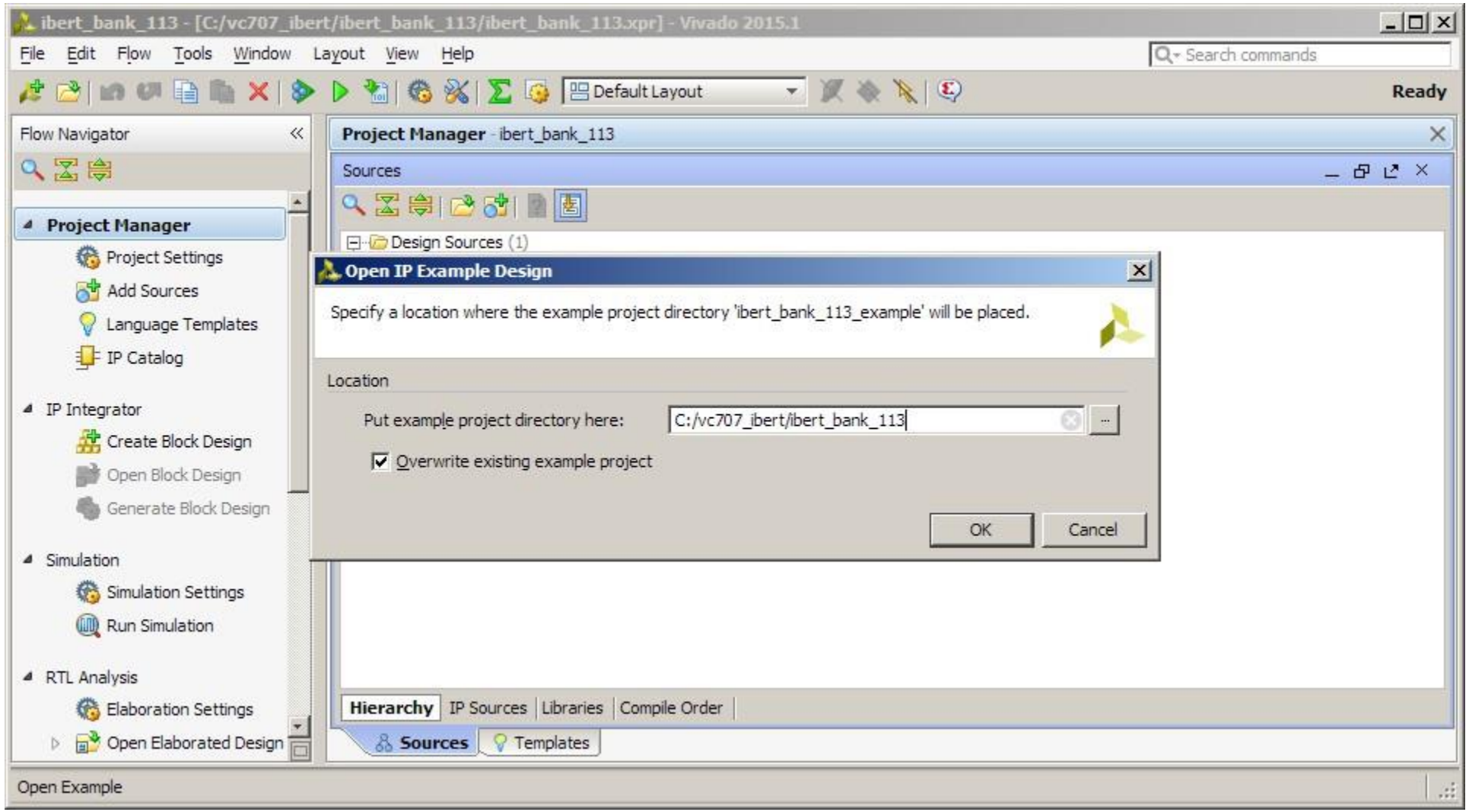
- Right click on ibert_bank_113 and select Open IP Example Design…



Note: Presentation applies to the VC707

Compile Example Design

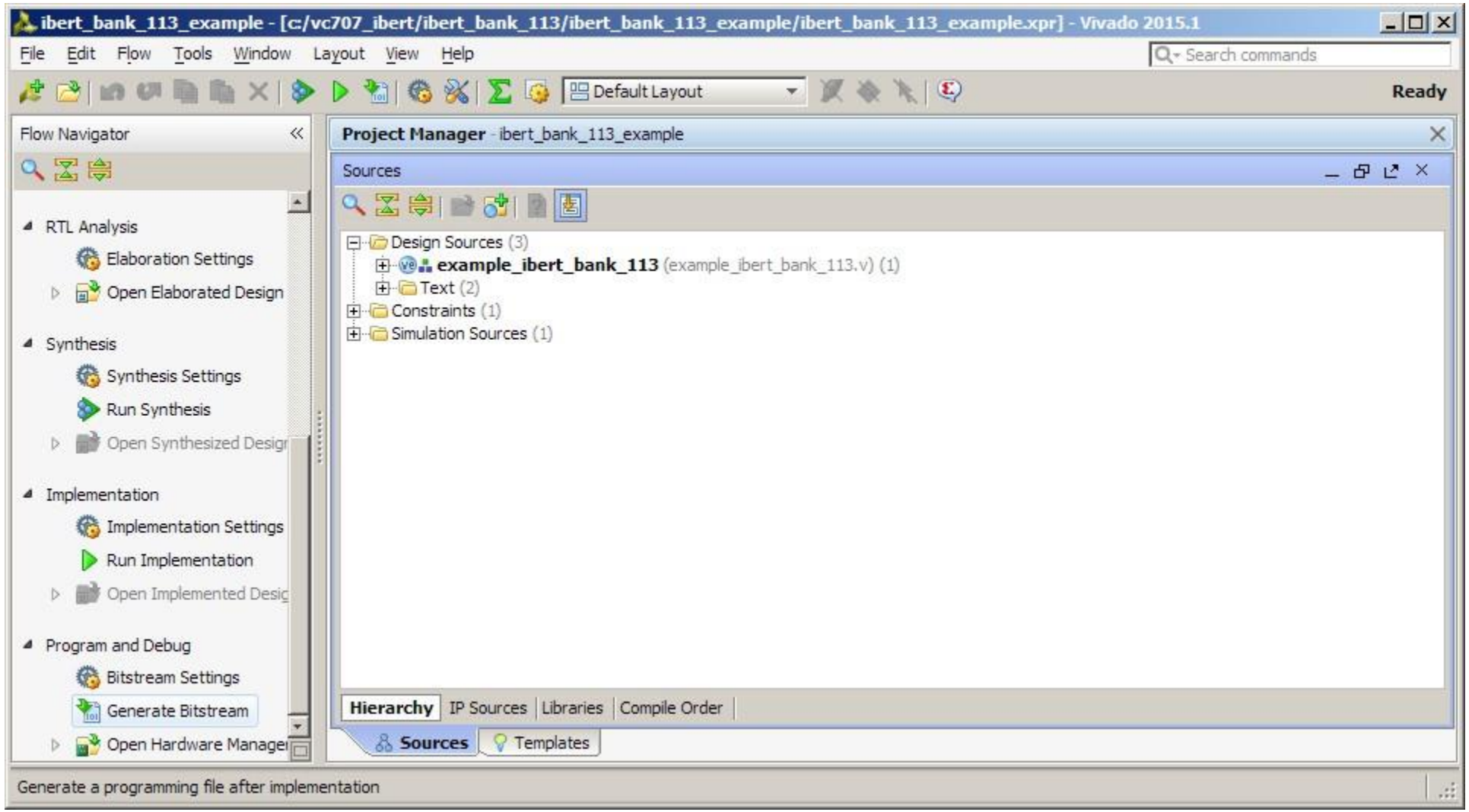
- Set the location to C:/vc707_ibert/ibert_bank_113 and click OK



Note: Presentation applies to the VC707

Compile Example Design

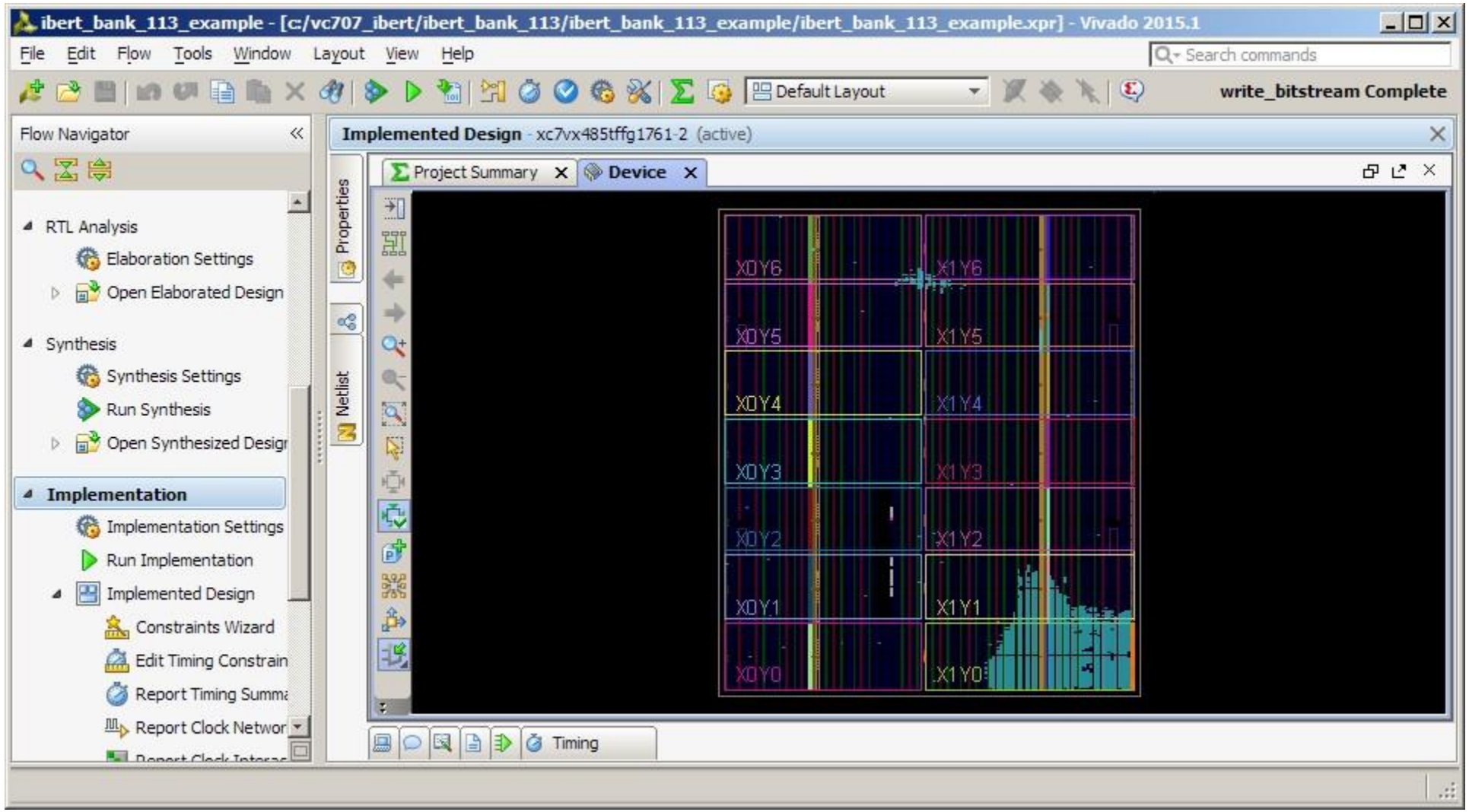
- A new project is created
- Click Generate Bitstream



Note: The original project window can be closed

Compile Example Design

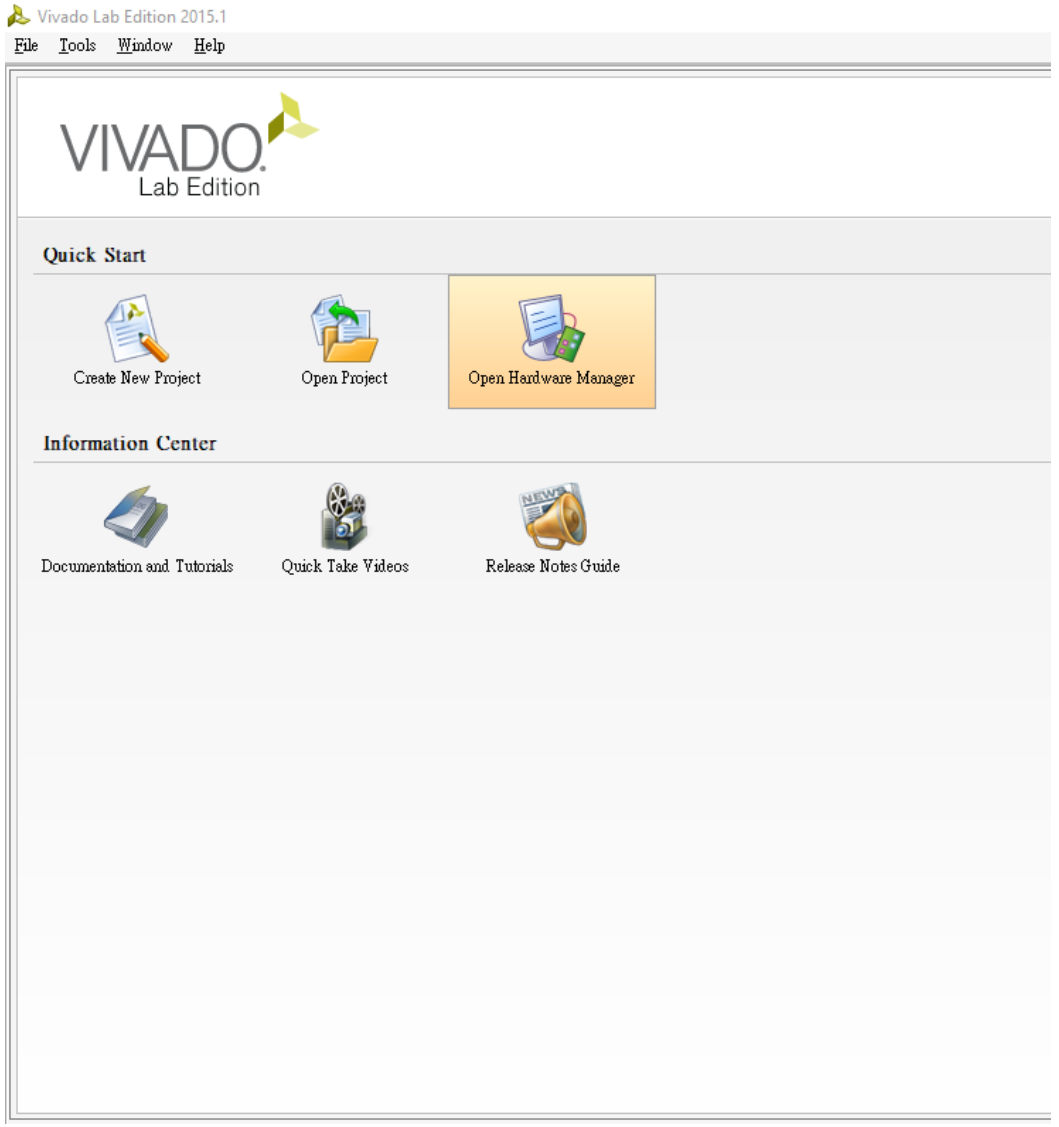
- Open and view the Implemented Design



Note: Presentation applies to the VC707

Open Hardware Manager(Vivado Lab 2015.1)

- Program the generated bitstream



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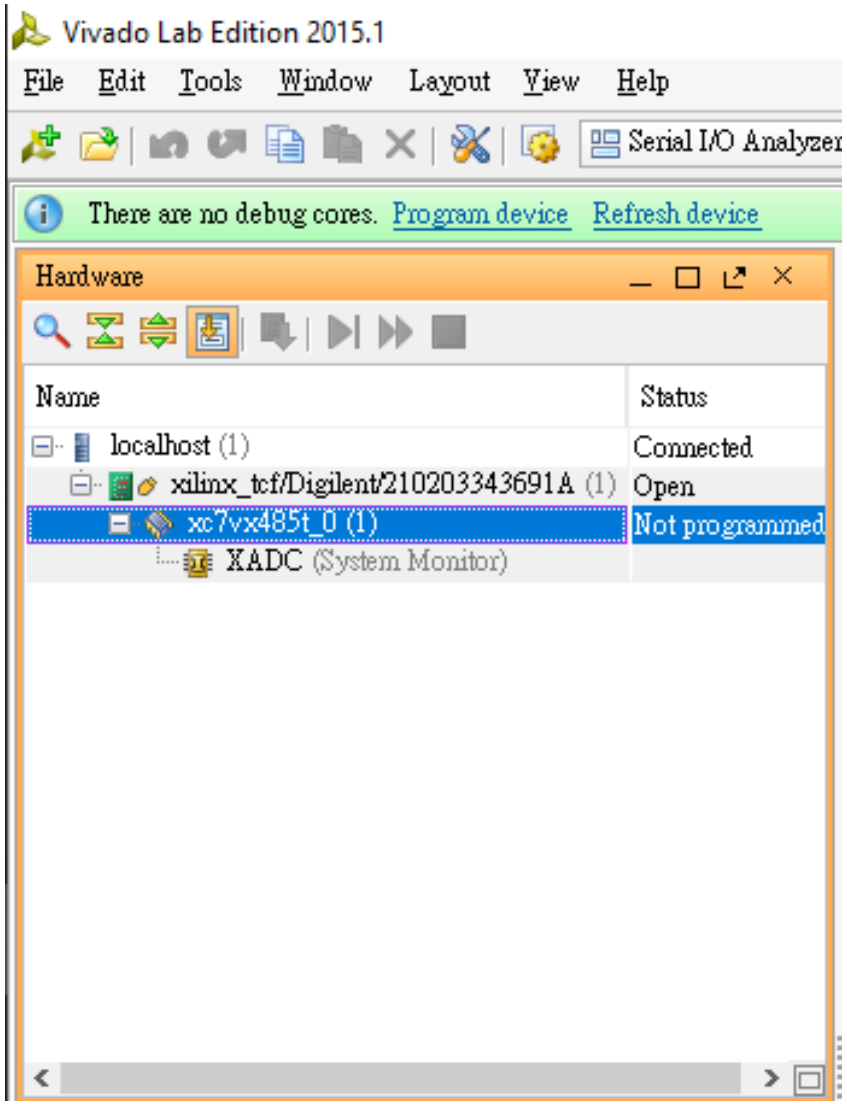
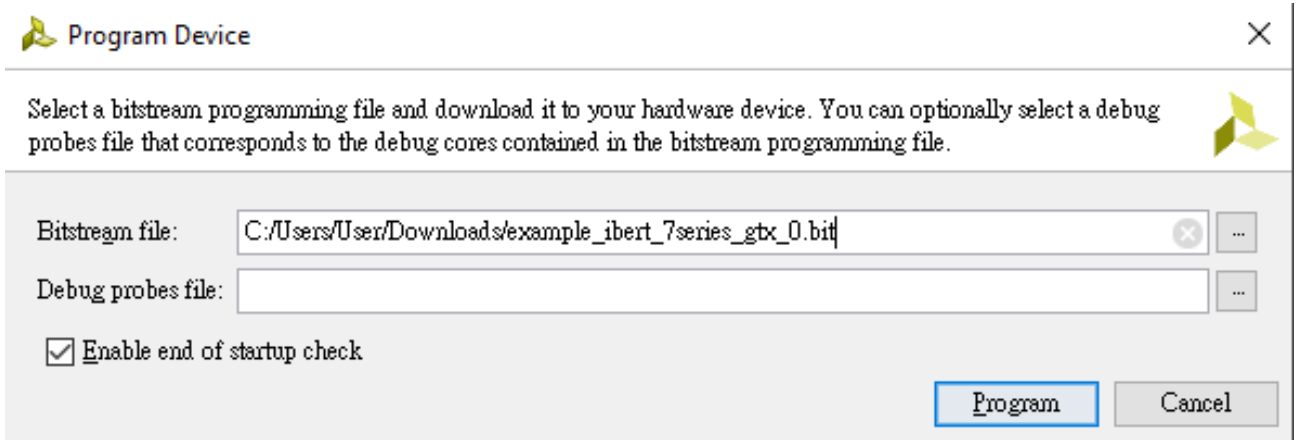
Open Hardware Manager(Vivado Lab 2015.1)

- Program the generated bitstream





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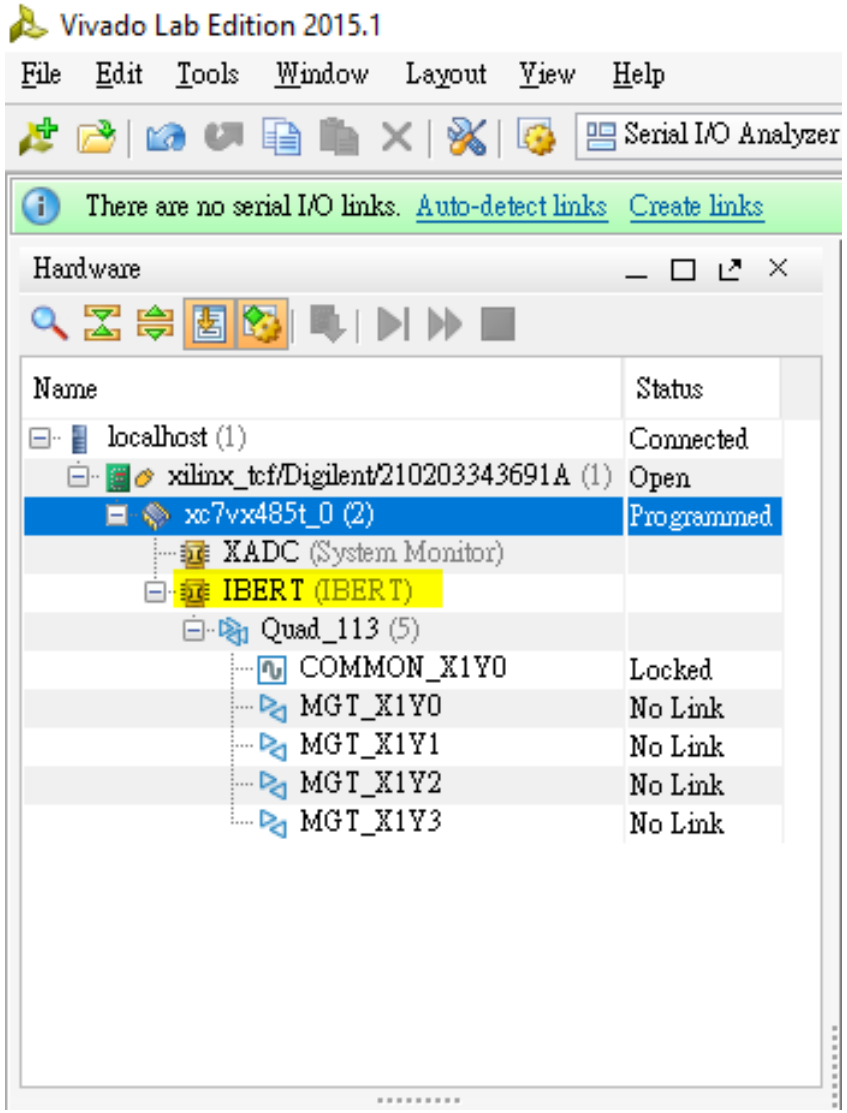

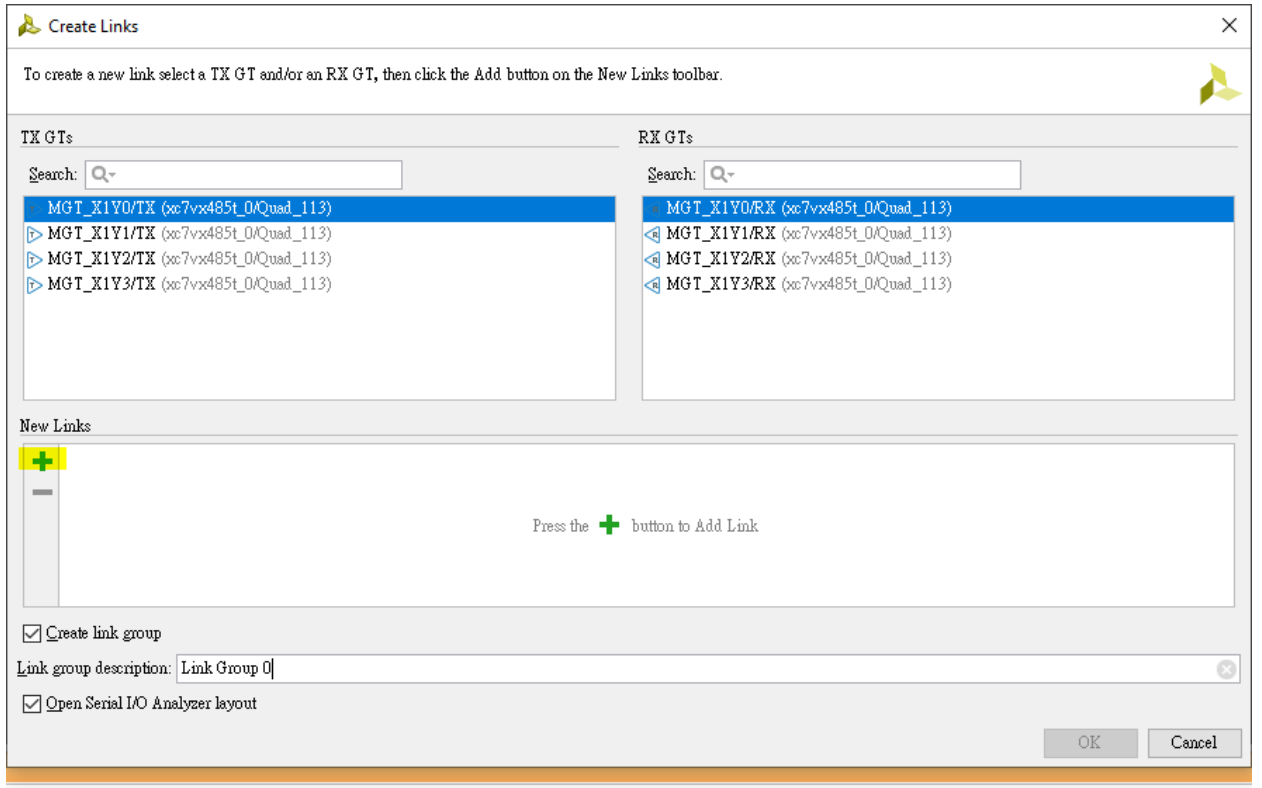

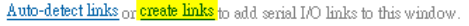

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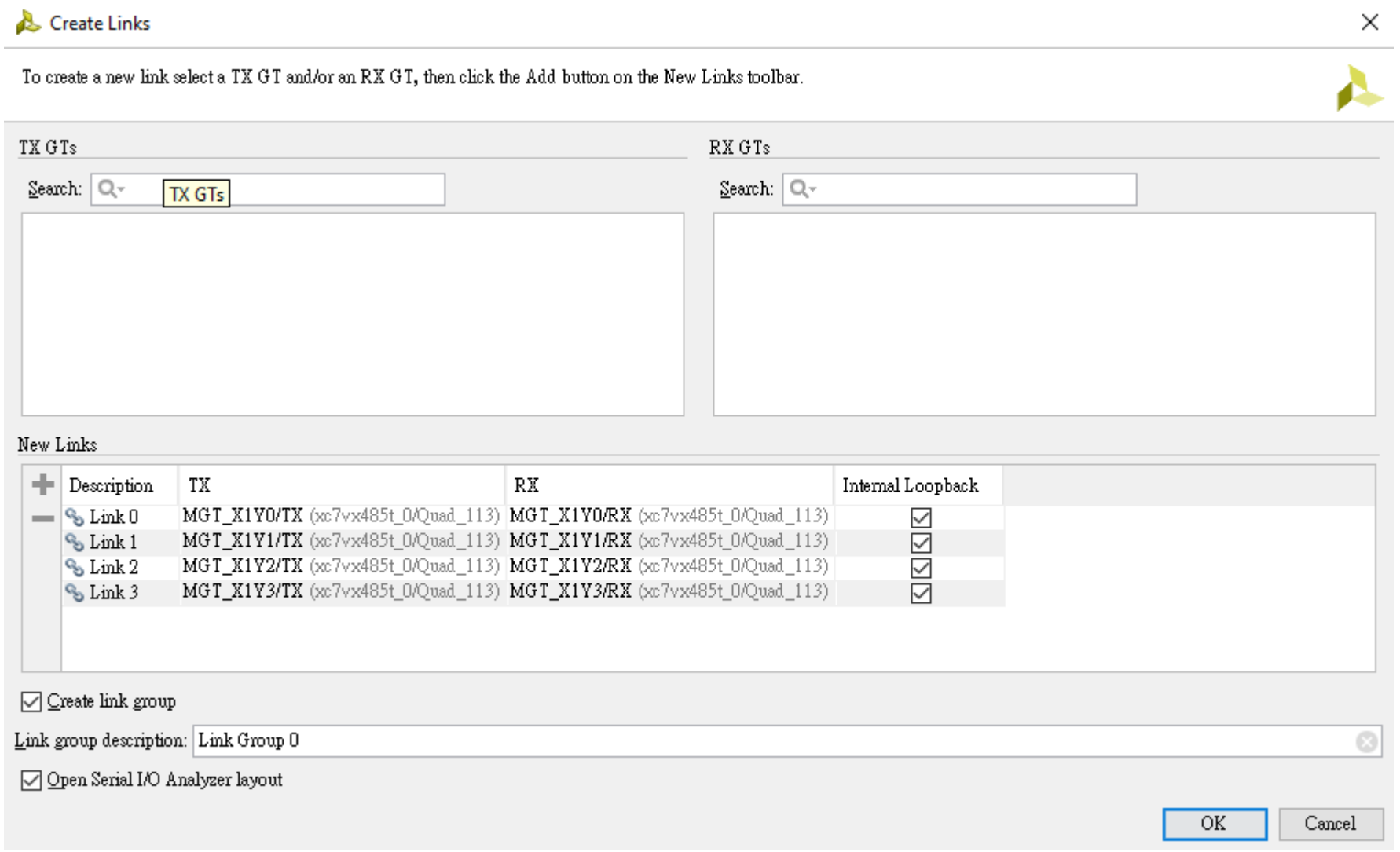
Open Hardware Manager(Vivado Lab 2015.1)

Program the generated bitstream



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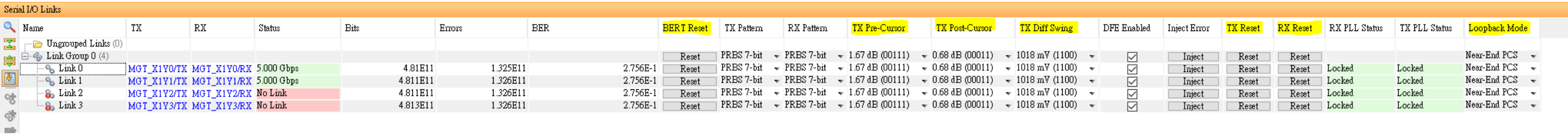
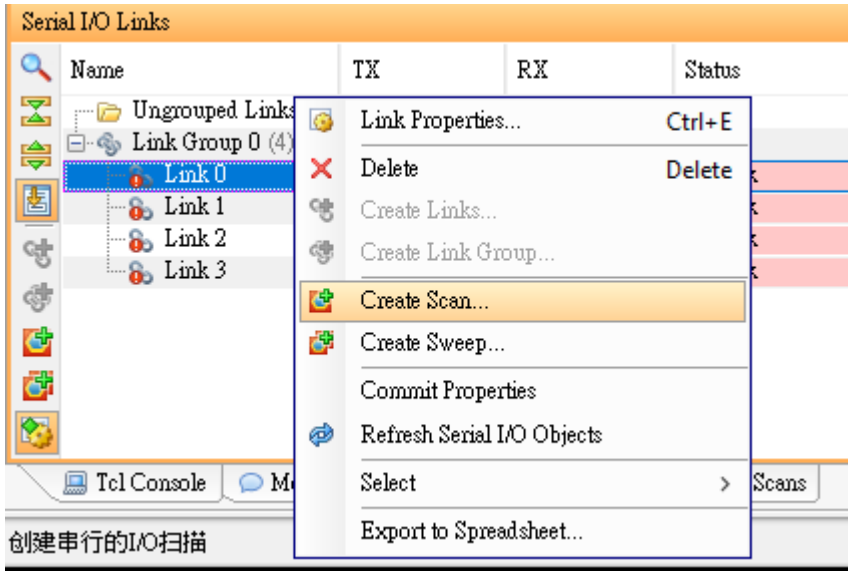
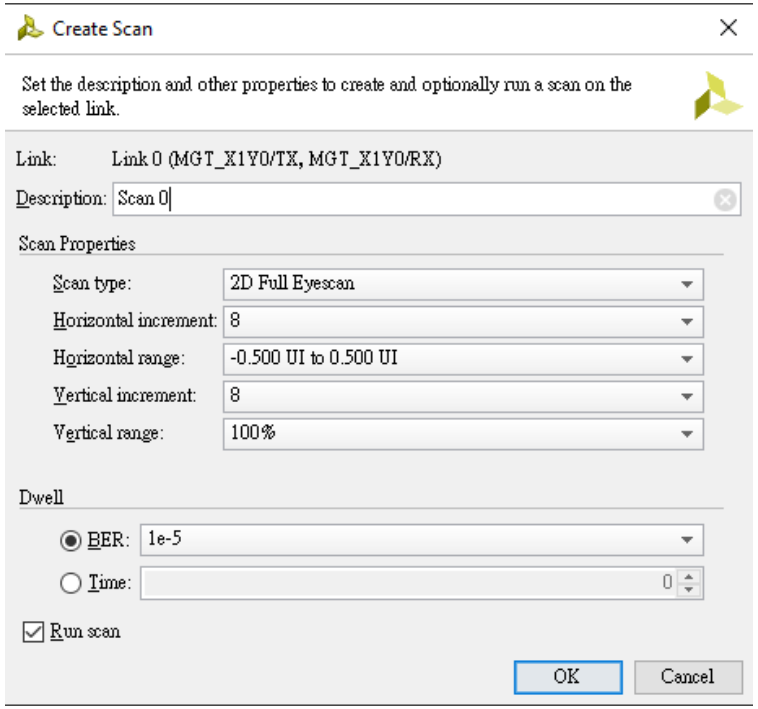
- Program the generated bitstream



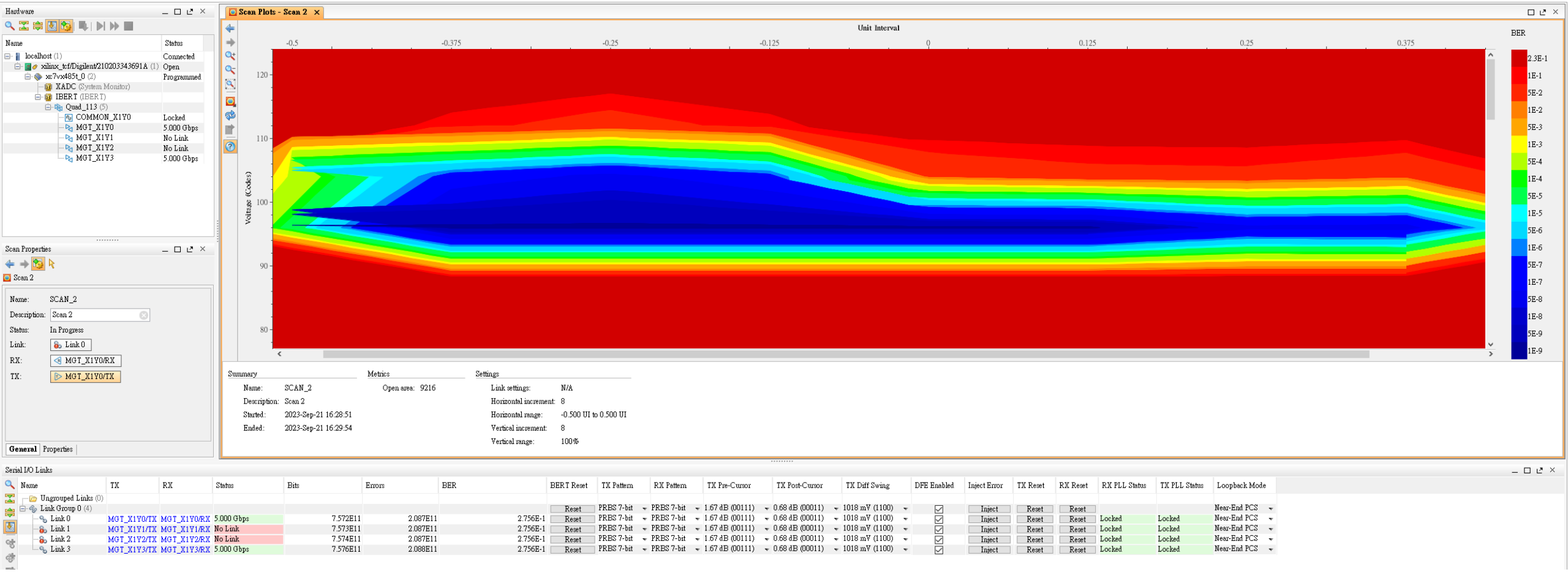




Note: Presentation applies to the VC707

Open Hardware Manager(Vivado Lab 2015.1)

Create Eye Scan



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AMD

APPENDIX A: Correct IBERT Flow Following Way

1. **Follow the board IBERT tutorial on Xilinx Website.**

XTP499 - ZCU104 IBERT Tutorial (v4.0)

Document Type: Example Designs

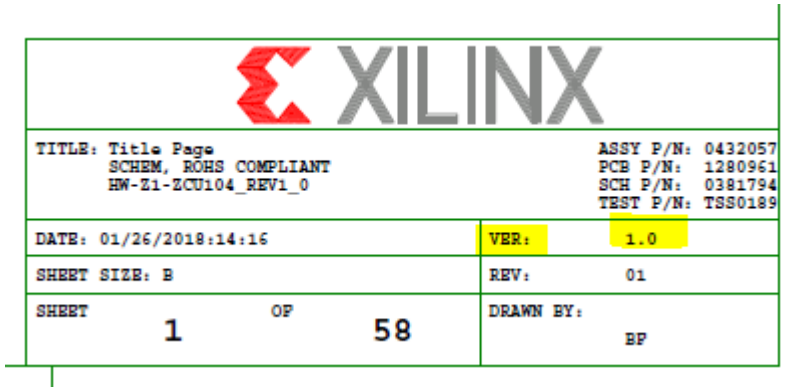
Creating an Using a GTH IBERT Design with the ZCU104 board

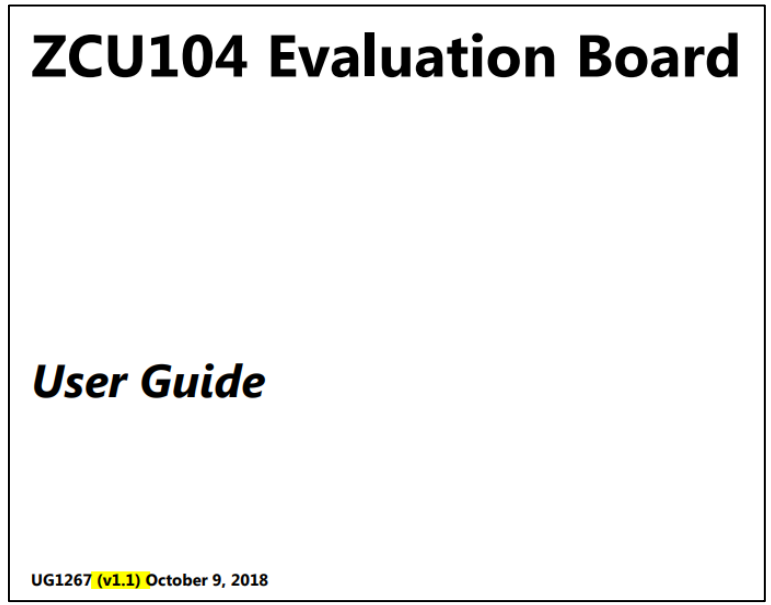
See All Versions

Design File(s):

rdf0453-zcu104-ibert-c-2018-3.zip

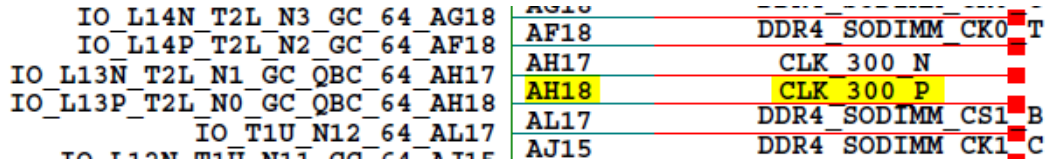
2. **Check the board schematic (notice the difference version cause difference pin assignment).**

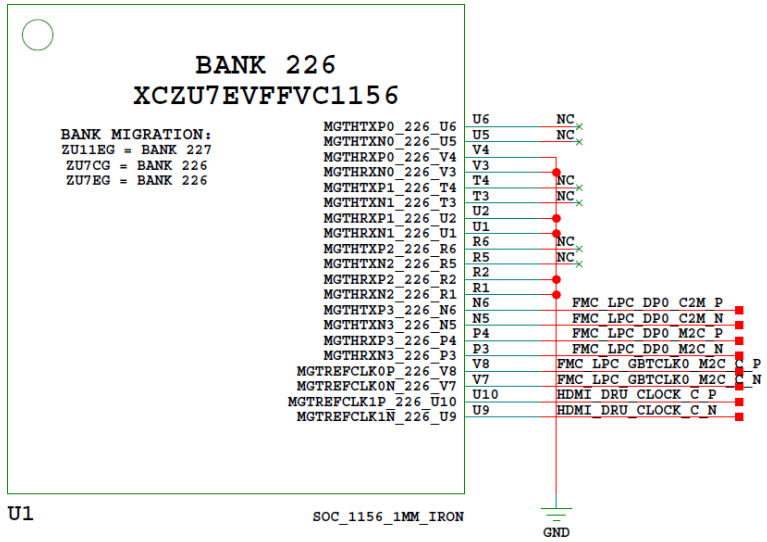




APPENDIX A: Correct IBERT Flow Following Way

3. Check the correct system clock and MGT Quad for testing.





4. Notice that additional FMC Card if needed for IBERT testing.

GTH Transceivers

[Figure 2-1, callout 1]

The Zynq UltraScale+ XCZU7EV MPSoC has 20 GTH gigabit transceivers (16.3 Gb/s capable) on the PL-side. The GTH transceivers in the XCZU7EV device are grouped into four channels referred to as Quads. The reference clock for a Quad can be sourced from the Quad above or the Quad below the GTH Quad of interest. There are five GTH Quads on the ZCU104 board with connectivity as listed here:

Quad 223:

- MGTREFCLK0 - Not connected
- MGTREFCLK1 - Not connected
- Four GTH transceivers not connected

Quad 224:

- MGTREFCLK0 - Not connected
- MGTREFCLK1 - Not connected
- Four GTH transceivers not connected

Quad 225:

- MGTREFCLK0 - Not connected
- MGTREFCLK1 - Not connected
- Four GTH transceivers not connected

Quad 226:

- MGTREFCLK0 - FMC_LPC_GBTCLK0_M2C_C_P/N
- MGTREFCLK1 - HDMI_DRU_CLOCK_C_P/N
- Contains one GTH transceiver allocated to FMC_LPC_DP0_C2M/M2C_P/N
- Four GTH transceivers not connected

Quad 227:

- MGTREFCLK0 - HDMI_8T49N241_OUT_C_P/N
- MGTREFCLK1 - HDMI_RX_CLK_C_P/N
- Contains three GTH transceivers allocated to HDMI_TX/RX[0:2]_P/N
- Contains one GTH transceiver allocated to FMC_LPC_DP0_C2M/M2C_P/N