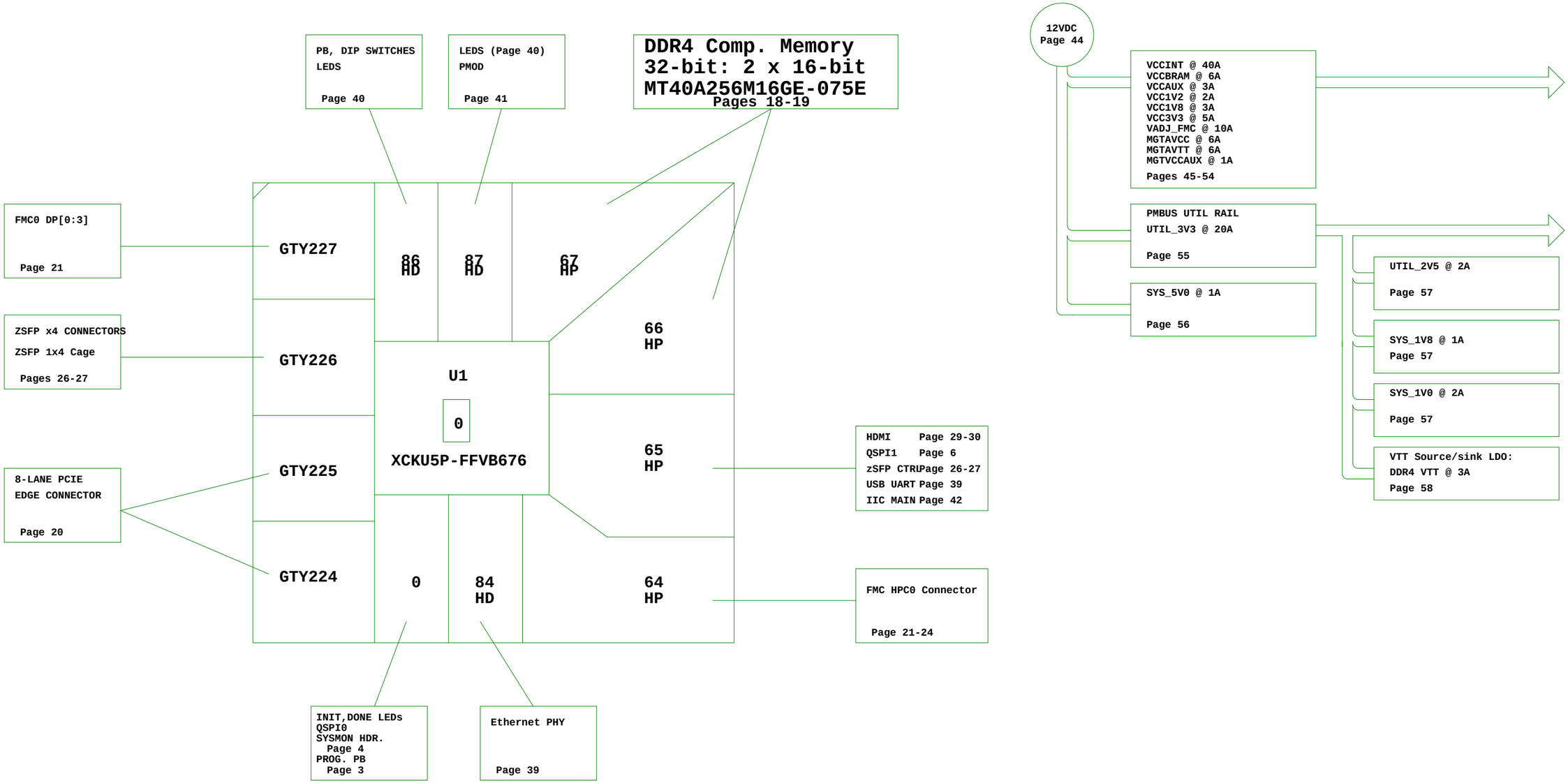
HW-U1-KCU116 Evaluation Board (XCKU5P-FFVB676)

Title Page

XILINX

TITLE: Title Page SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 1 OF 60	DRAWN BY: DN



JTAG CONN. Page 17	System Controller and SD Card Socket Page 31-35		
Blank Page Page 25	System Clock devices Fixed and Programmable Pages 36-37		
zSFP Clock Recovery Page 28	IIC EEPROM Page 38		

BANK#	PAGE#	BANK#	PAGE#
BANK 0	3	GTY224	10
BANK 64	5	GTY225	10
BANK 65	6	GTY226	11
BANK 66	7	GTY227	11
BANK 67	7	PWR BANKS	12-14
BANK 86	8	PWR DECOUPLING	15-16
BANK 84	9		
BANK 87	9		

MECHANICALS
Page 60

2 x IIC MUX
I/O EXPANDER
(IIC MAIN)
Page 42

PMBUS Hdr.
Level-Shifters
Page 43

Ironwood Socket P/N: C11090-D5616

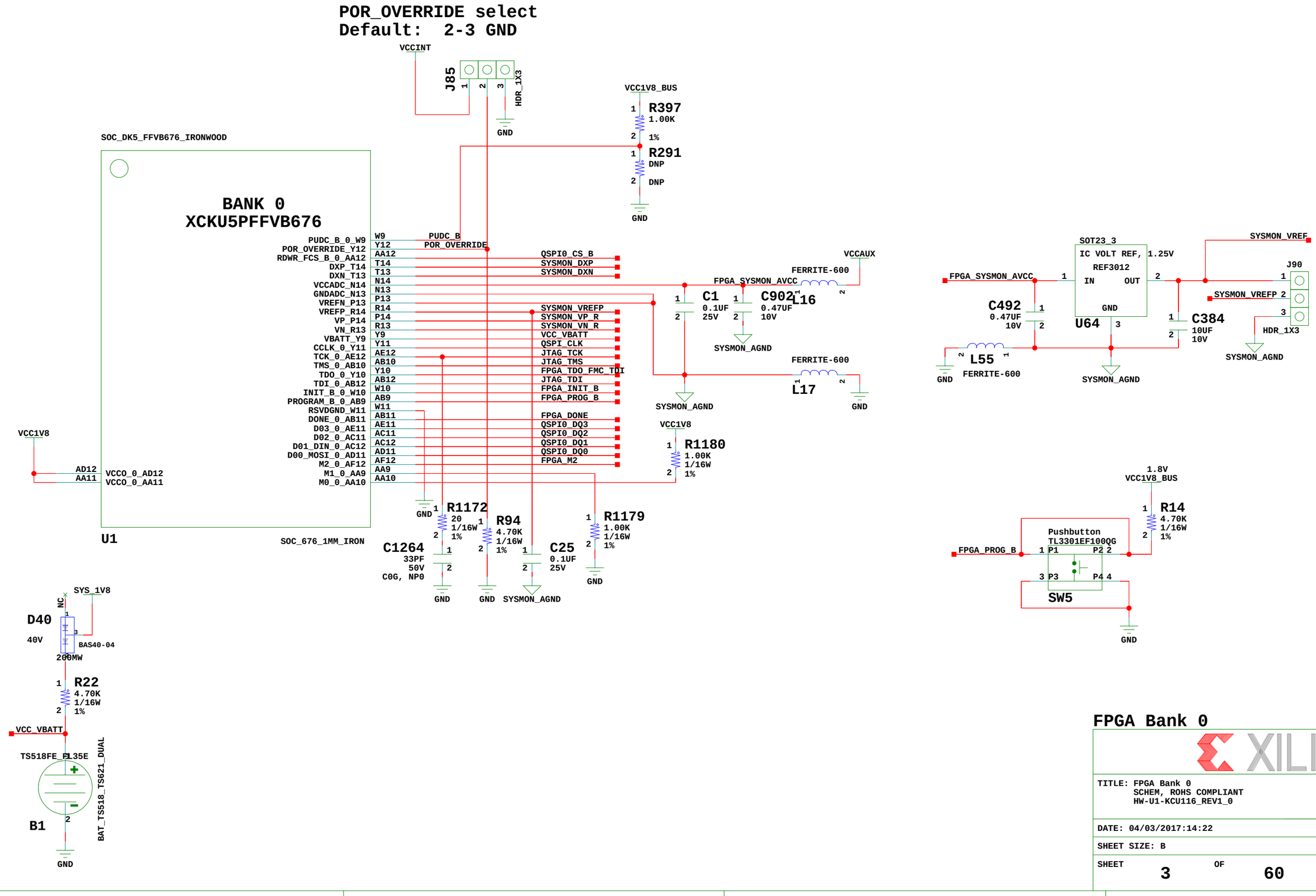
Block Diagram

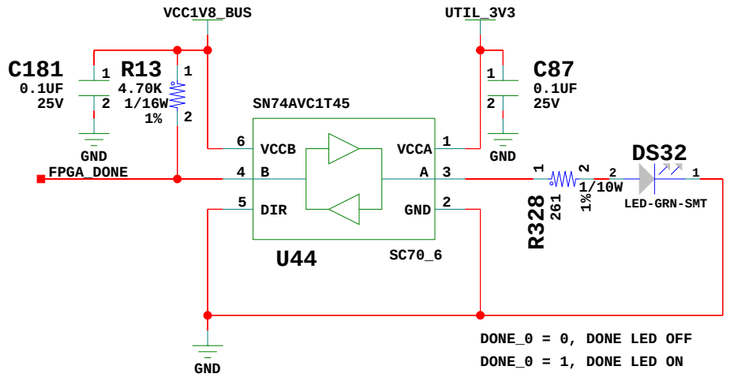
XILINX

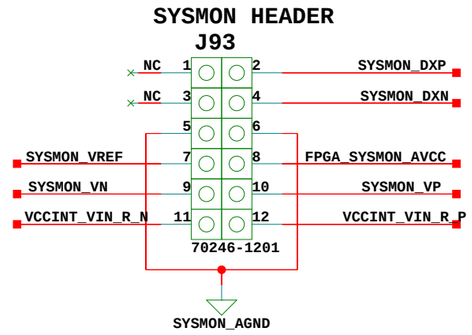
TITLE: Block Diagram
SCHEM, ROHS COMPLIANT
HW-U1-KCU116_REV1_0

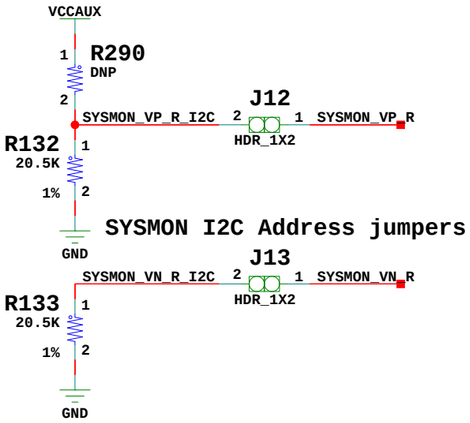
ASSY P/N: 0432019
PCB P/N: 1280924
SCH P/N: 0381757
TEST P/N: TSSXXXX

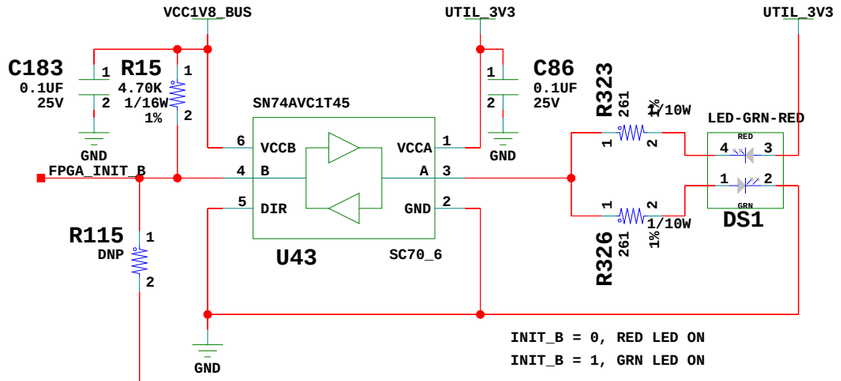
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 2 OF 60	DRAWN BY: DN

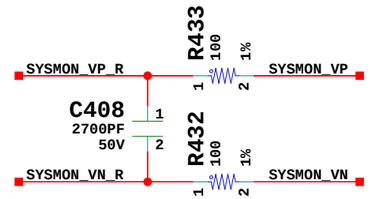

POR_OVERRIDE select
Default: 2-3 GND
VCCINT
J85
HDR_1X3
GND
VCC1V8_BUS
R397
1.00K
1%
R291
DNP
DNP
GND
SOC_DK5_FFVB676_IRONWOOD
BANK 0
XCKU5PFFVB676
PUDC_B_0_W9
POR_OVERRIDE_Y12
RDWR_FCS_B_0_AA12
DXP_T14
DXN_T13
VCCADC_N14
GNDADC_N13
VREFN_P13
VREFP_R14
VP_P14
VN_R13
VBATT_Y9
CCLK_0_Y11
TCK_0_AE12
TMS_0_AB10
TDO_0_Y10
TDI_0_AB12
INIT_B_0_W10
PROGRAM_B_0_AB9
RSVDGND_W11
DONE_0_AB11
D03_0_AE11
D02_0_AC11
D01_DIN_0_AC12
D00_MOSI_0_AD11
M2_0_AF12
M1_0_AA9
M0_0_AA10
W9 PUDC_B
Y12 POR_OVERRIDE
AA12 QSPI0_CS_B
T14 SYSMON_DXP
T13 SYSMON_DXN
N14
N13
P13
R14 SYSMON_VREFP
P14 SYSMON_VP_R
R13 SYSMON_VN_R
Y9 VCC_VBATT
Y11 QSPI_CLK
AE12 JTAG_TCK
AB10 JTAG_TMS
Y10 FPGA_TDO_FMC_TDI
AB12 JTAG_TDI
W10 FPGA_INIT_B
AB9 FPGA_PROG_B
W11
AB11 FPGA_DONE
AE11 QSPI0_DQ3
AC11 QSPI0_DQ2
AC12 QSPI0_DQ1
AD11 QSPI0_DQ0
AF12 FPGA_M2
AA9
AA10
VCCAUX
FERRITE-600
FPGA_SYSMON_AVCC
C1
0.1UF
25V
C902
0.47UF
10V
L16
SYSMON_AGND
FERRITE-600
L17
GND
SYSMON_AGND
VCC1V8
R1180
1.00K
1/16W
1%
VCC1V8
AD12
AA11
VCCO_0_AD12
VCCO_0_AA11
U1
SOC_676_1MM_IRON
R1172
20
1/16W
1%
R94
4.70K
1/16W
1%
R1179
1.00K
1/16W
1%
C1264
33PF
50V
C0G, NP0
C25
0.1UF
25V
GND
GND
SYSMON_AGND
GND
SOT23_3
IC VOLT REF, 1.25V
REF3012
IN
OUT
GND
U64
FPGA_SYSMON_AVCC
C492
0.47UF
10V
L55
FERRITE-600
GND
SYSMON_AGND
C384
10UF
10V
SYSMON_VREF
J90
SYSMON_VREFP 2
HDR_1X3
SYSMON_AGND
1.8V
VCC1V8_BUS
R14
4.70K
1/16W
1%
Pushbutton
TL3301EF100QG
FPGA_PROG_B
P1
P2
P3
P4
SW5
GND
SYS_1V8
NC
D40
40V
BAS40-04
200MW
R22
4.70K
1/16W
1%
VCC_VBATT
TS518FE_FL35E
B1
BAT_TS518_TS621_DUAL
GND
FPGA Bank 0
XILINX
TITLE: FPGA Bank 0
SCHEM, ROHS COMPLIANT
HW-U1-KCU116_REV1_0
ASSY P/N: 0432019
PCB P/N: 1280924
SCH P/N: 0381757
TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22
VER: 1.0
SHEET SIZE: B
REV: 01
SHEET 3 OF 60
DRAWN BY: DN

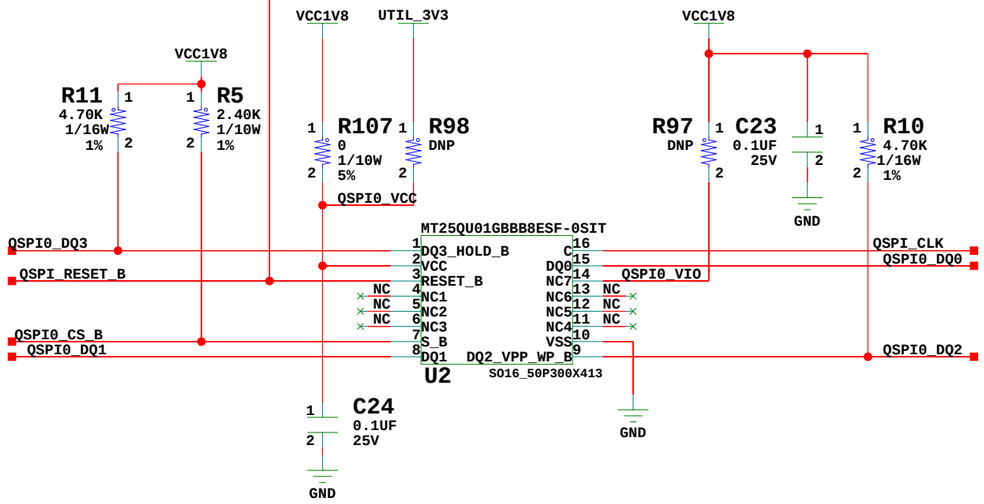












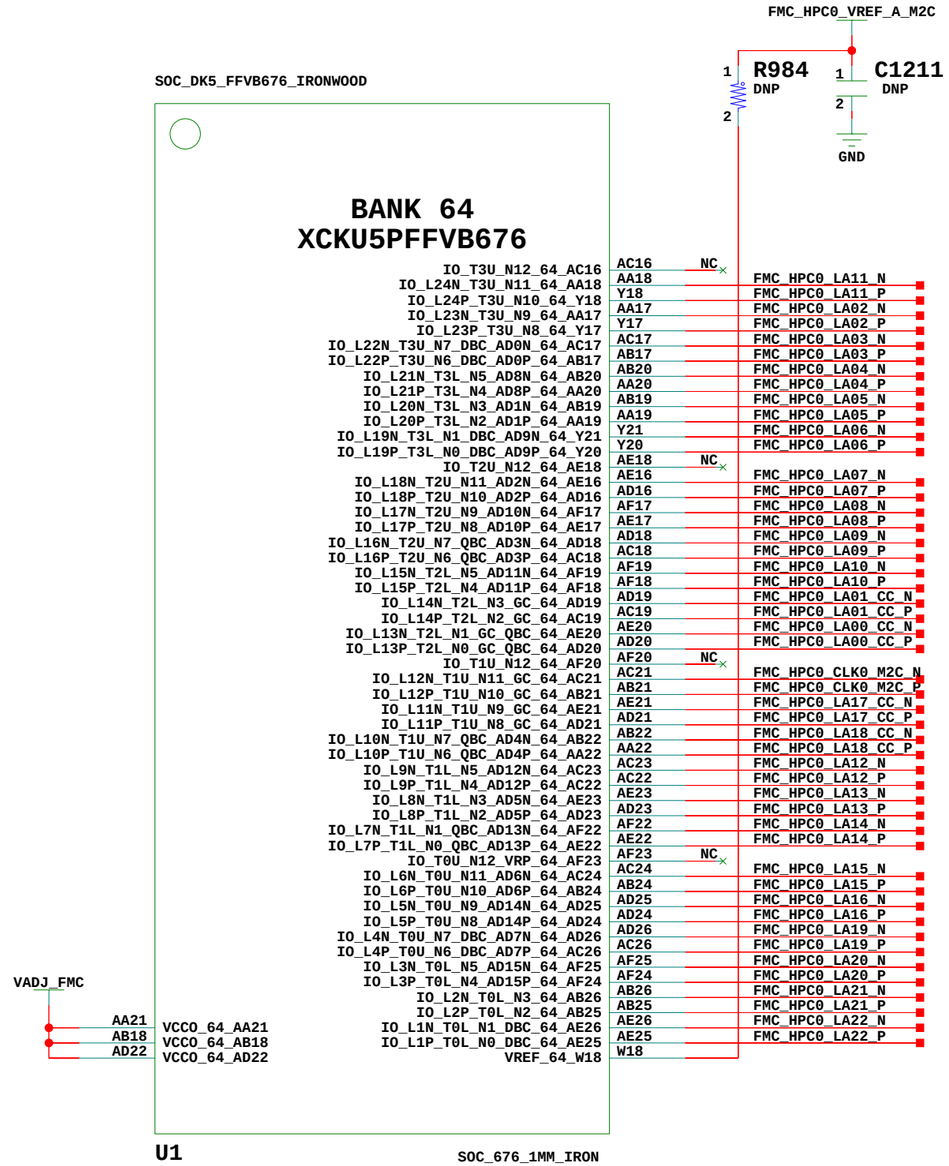
SYSMON Hdr INIT DONE LED QSPI0

XILINX

TITLE: SYSMON Hdr INIT DONE LED QSPI0 SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 4 OF 60	DRAWN BY: DN

Layout: Place resistor and capacitor for VREF

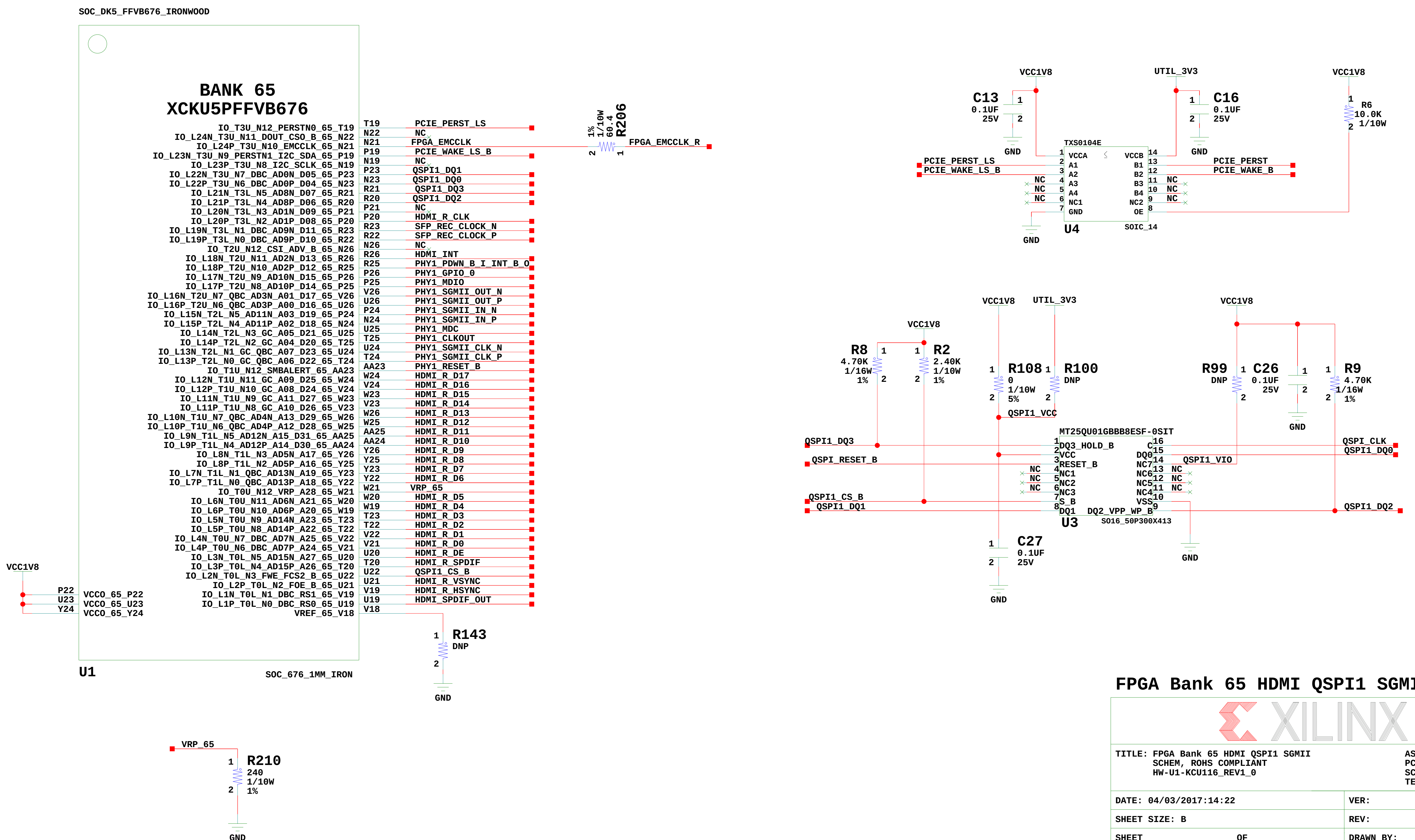
Underneath the FPGA via array
right next to the via



FPGA Banks 64 FMC

XILINX

TITLE: FPGA Banks 64 FMC SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 5 OF 60	DRAWN BY: DN



FPGA Bank 65 HDMI QSPI1 SGMII

XILINX

TITLE: FPGA Bank 65 HDMI QSPI1 SGMII SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 6 OF 60	DRAWN BY: DN

SOC_DK5_FFVB676_IRONWOOD

BANK 66
XCKU5PFFVB676

IO_T3U_N12_66_F22	F22	DDR4_A8
IO_L24N_T3U_N11_66_B26	B26	DDR4_A13
IO_L24P_T3U_N10_66_B25	B25	DDR4_A7
IO_L23N_T3U_N9_66_C26	C26	DDR4_A5
IO_L23P_T3U_N8_66_D26	D26	DDR4_A2
IO_L22N_T3U_N7_DBC_AD0N_66_C24	C24	DDR4_A9
IO_L22P_T3U_N6_DBC_AD0P_66_D23	D23	DDR4_A1
IO_L21N_T3L_N5_AD8N_66_D25	D25	DDR4_A0
IO_L21P_T3L_N4_AD8P_66_D24	D24	DDR4_A3
IO_L20N_T3L_N3_AD1N_66_E23	E23	DDR4_A12
IO_L20P_T3L_N2_AD1P_66_F23	F23	DDR4_A11
IO_L19N_T3L_N1_DBC_AD9N_66_E26	E26	DDR4_A4
IO_L19P_T3L_N0_DBC_AD9P_66_E25	E25	DDR4_A10
IO_T2U_N12_66_G22	G22	DDR4_A6
IO_L18N_T2U_N11_AD2N_66_H22	H22	DDR4_BA0
IO_L18P_T2U_N10_AD2P_66_H21	H21	DDR4_BA1
IO_L17N_T2U_N9_AD10N_66_G26	G26	DDR4_BG0
IO_L17P_T2U_N8_AD10P_66_H26	H26	DDR4_A14_WE_B
IO_L16N_T2U_N7_QBC_AD3N_66_F25	F25	DDR4_A15_CAS_B
IO_L16P_T2U_N6_QBC_AD3P_66_F24	F24	DDR4_A16_RAS_B
IO_L15N_T2L_N5_AD11N_66_J26	J26	DDR4_ACT_B
IO_L15P_T2L_N4_AD11P_66_J25	J25	DDR4_PAR
IO_L14N_T2L_N3_GC_66_H24	H24	DDR4_ODT
IO_L14P_T2L_N2_GC_66_H23	H23	DDR4_CS_B
IO_L13N_T2L_N1_GC_QBC_66_G25	G25	DDR4_CK_C
IO_L13P_T2L_N0_GC_QBC_66_G24	G24	DDR4_CK_T
IO_T1U_N12_66_M24	M24	DDR4_CKE
IO_L12N_T1U_N11_GC_66_J24	J24	USER_SMA_CLOCK_N
IO_L12P_T1U_N10_GC_66_J23	J23	USER_SMA_CLOCK_P
IO_L11N_T1U_N9_GC_66_K23	K23	SYSCLK_300_N
IO_L11P_T1U_N8_GC_66_K22	K22	SYSCLK_300_P
IO_L10N_T1U_N7_QBC_AD4N_66_L25	L25	DDR4_RESET_B
IO_L10P_T1U_N6_QBC_AD4P_66_L24	L24	DDR4_ALERT_B
IO_L9N_T1L_N5_AD12N_66_K26	K26	USER_SMA_N
IO_L9P_T1L_N4_AD12P_66_K25	K25	USER_SMA_P
IO_L8N_T1L_N3_AD5N_66_M26	M26	NC
IO_L8P_T1L_N2_AD5P_66_M25	M25	NC
IO_L7N_T1L_N1_QBC_AD13N_66_L23	L23	NC
IO_L7P_T1L_N0_QBC_AD13P_66_L22	L22	NC
IO_T0U_N12_VRP_66_M22	M22	VRP_66
IO_L6N_T0U_N11_AD6N_66_K20	K20	NC
IO_L6P_T0U_N10_AD6P_66_L20	L20	NC
IO_L5N_T0U_N9_AD14N_66_J21	J21	NC
IO_L5P_T0U_N8_AD14P_66_K21	K21	NC
IO_L4N_T0U_N7_DBC_AD7N_66_L19	L19	NC
IO_L4P_T0U_N6_DBC_AD7P_66_M19	M19	NC
IO_L3N_T0L_N5_AD15N_66_J20	J20	NC
IO_L3P_T0L_N4_AD15P_66_J19	J19	NC
IO_L2N_T0L_N3_66_M21	M21	NC
IO_L2P_T0L_N2_66_M20	M20	NC
IO_L1N_T0L_N1_DBC_66_K18	K18	NC
IO_L1P_T0L_N0_DBC_66_L18	L18	NC
VREF_66_J18	J18	

USER_SMA_CLOCK_P
R1174
100
1/10W
1%
USER_SMA_CLOCK_N

SYSCLK_300_P
R212
100
1/10W
1%
SYSCLK_300_N

VRP_66
R1097
1.00K
1/16W
1%
GND

VCC1V2
E24 VCCO_66_E24
H25 VCCO_66_H25
J22 VCCO_66_J22

U1
SOC_676_1MM_IRON

VRP_66
R345
240
1/10W
1%
GND

SOC_DK5_FFVB676_IRONWOOD

BANK 67
XCKU5PFFVB676

IO_T3U_N12_67_E22	E22	NC
IO_L24N_T3U_N11_67_B22	B22	DDR4_DQ5
IO_L24P_T3U_N10_67_C22	C22	DDR4_DQ0
IO_L23N_T3U_N9_67_A25	A25	DDR4_DQ7
IO_L23P_T3U_N8_67_A24	A24	DDR4_DQ3
IO_L22N_T3U_N7_DBC_AD0N_67_B21	B21	DDR4_DQS0_C
IO_L22P_T3U_N6_DBC_AD0P_67_C21	C21	DDR4_DQS0_T
IO_L21N_T3L_N5_AD8N_67_B24	B24	DDR4_DQ1
IO_L21P_T3L_N4_AD8P_67_C23	C23	DDR4_DQ2
IO_L20N_T3L_N3_AD1N_67_D21	D21	DDR4_DQ4
IO_L20P_T3L_N2_AD1P_67_E21	E21	DDR4_DQ6
IO_L19N_T3L_N1_DBC_AD9N_67_A23	A23	NC
IO_L19P_T3L_N0_DBC_AD9P_67_A22	A22	DDR4_DM0
IO_T2U_N12_67_B16	B16	NC
IO_L18N_T2U_N11_AD2N_67_A20	A20	DDR4_DQ10
IO_L18P_T2U_N10_AD2P_67_A19	A19	DDR4_DQ8
IO_L17N_T2U_N9_AD10N_67_A15	A15	DDR4_DQ13
IO_L17P_T2U_N8_AD10P_67_B15	B15	DDR4_DQ15
IO_L16N_T2U_N7_QBC_AD3N_67_A18	A18	DDR4_DQS1_C
IO_L16P_T2U_N6_QBC_AD3P_67_A17	A17	DDR4_DQS1_T
IO_L15N_T2L_N5_AD11N_67_B17	B17	DDR4_DQ11
IO_L15P_T2L_N4_AD11P_67_C17	C17	DDR4_DQ9
IO_L14N_T2L_N3_GC_67_B20	B20	DDR4_DQ12
IO_L14P_T2L_N2_GC_67_B19	B19	DDR4_DQ14
IO_L13N_T2L_N1_GC_QBC_67_C19	C19	NC
IO_L13P_T2L_N0_GC_QBC_67_C18	C18	DDR4_DM1
IO_T1U_N12_67_G19	G19	NC
IO_L12N_T1U_N11_GC_67_D20	D20	DDR4_DQ19
IO_L12P_T1U_N10_GC_67_D19	D19	DDR4_DQ21
IO_L11N_T1U_N9_GC_67_D18	D18	DDR4_DQ23
IO_L11P_T1U_N8_GC_67_E18	E18	DDR4_DQ20
IO_L10N_T1U_N7_QBC_AD4N_67_E20	E20	DDR4_DQS2_C
IO_L10P_T1U_N6_QBC_AD4P_67_F20	F20	DDR4_DQS2_T
IO_L9N_T1L_N5_AD12N_67_G21	G21	DDR4_DQ17
IO_L9P_T1L_N4_AD12P_67_G20	G20	DDR4_DQ22
IO_L8N_T1L_N3_AD5N_67_F19	F19	DDR4_DQ18
IO_L8P_T1L_N2_AD5P_67_F18	F18	DDR4_DQ16
IO_L7N_T1L_N1_QBC_AD13N_67_H19	H19	NC
IO_L7P_T1L_N0_QBC_AD13P_67_H18	H18	DDR4_DM2
IO_T0U_N12_VRP_67_F17	F17	VRP_67
IO_L6N_T0U_N11_AD6N_67_C16	C16	DDR4_DQ29
IO_L6P_T0U_N10_AD6P_67_D16	D16	DDR4_DQ25
IO_L5N_T0U_N9_AD14N_67_G16	G16	DDR4_DQ26
IO_L5P_T0U_N8_AD14P_67_H16	H16	DDR4_DQ30
IO_L4N_T0U_N7_DBC_AD7N_67_E17	E17	DDR4_DQS3_C
IO_L4P_T0U_N6_DBC_AD7P_67_E16	E16	DDR4_DQS3_T
IO_L3N_T0L_N5_AD15N_67_D15	D15	DDR4_DQ27
IO_L3P_T0L_N4_AD15P_67_E15	E15	DDR4_DQ28
IO_L2N_T0L_N3_67_G17	G17	DDR4_DQ31
IO_L2P_T0L_N2_67_H17	H17	DDR4_DQ24
IO_L1N_T0L_N1_DBC_67_F15	F15	NC
IO_L1P_T0L_N0_DBC_67_G15	G15	DDR4_DM3
VREF_67_J16	J16	

VCC1V2
C20 VCCO_67_C20
D17 VCCO_67_D17
G18 VCCO_67_G18

R1101
1.00K
1/16W
1%
GND

U1
SOC_676_1MM_IRON

VRP_67
R1068
240
1/10W
1%
GND

FPGA Banks 66 67 DDR4

XILINX

TITLE: FPGA Banks 66 67 DDR4 SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 7 OF 60	DRAWN BY: DN

SOC_DK5_FFVB676_IRONWOOD

BANK 86
XCKU5PFFVB676

IO_L12N_AD0N_86_B11	B11	GPIO_SW_E
IO_L12P_AD0P_86_C11	C11	GPIO_SW_S
IO_L11N_AD1N_86_A10	A10	GPIO_SW_N
IO_L11P_AD1P_86_B10	B10	GPIO_SW_W
IO_L10N_AD2N_86_A9	A9	GPIO_SW_C
IO_L10P_AD2P_86_B9	B9	CPU_RESET
IO_L9N_AD3N_86_C9	C9	GPIO_LED_0
IO_L9P_AD3P_86_D9	D9	GPIO_LED_1
IO_L8N_HDGC_AD4N_86_D10	D10	CLK_74_25_N
IO_L8P_HDGC_AD4P_86_D11	D11	CLK_74_25_P
IO_L7N_HDGC_AD5N_86_E10	E10	GPIO_LED_2
IO_L7P_HDGC_AD5P_86_E11	E11	GPIO_LED_3
IO_L6N_HDGC_AD6N_86_F9	F9	GPIO_LED_4
IO_L6P_HDGC_AD6P_86_F10	F10	GPIO_LED_5
IO_L5N_HDGC_AD7N_86_G9	G9	GPIO_LED_6
IO_L5P_HDGC_AD7P_86_G10	G10	GPIO_LED_7
IO_L4N_AD8N_86_G11	G11	GPIO_DIP_SW0
IO_L4P_AD8P_86_H11	H11	GPIO_DIP_SW1
IO_L3N_AD9N_86_H9	H9	GPIO_DIP_SW2
IO_L3P_AD9P_86_J9	J9	GPIO_DIP_SW3
IO_L2N_AD10N_86_J10	J10	NC
IO_L2P_AD10P_86_J11	J11	NC
IO_L1N_AD11N_86_K9	K9	NC
IO_L1P_AD11P_86_K10	K10	NC

VCC3V3

E9	VCCO_86_E9
H10	VCCO_86_H10

U1

SOC_676_1MM_IRON

CLK_74_25_P

1 **R430** 2

100
1/10W
1%

CLK_74_25_N

FPGA Banks 86 - GPIO and CLOCKS

XILINX

TITLE: FPGA Banks 86 - GPIO and CLOCKS
SCHEM, ROHS COMPLIANT
HW-U1-KCU116_REV1_0

ASSY P/N: 0432019
PCB P/N: 1280924
SCH P/N: 0381757
TEST P/N: TSSXXXX

DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 8 OF 60	DRAWN BY: DN

SOC_DK5_FFVB676_IRONWOOD

BANK 87
XCKU5PFFVB676

IO_L12N_AD8N_87_A14	A14	PMOD0_0
IO_L12P_AD8P_87_B14	B14	PMOD0_1
IO_L11N_AD9N_87_A12	A12	PMOD0_2
IO_L11P_AD9P_87_A13	A13	PMOD0_3
IO_L10N_AD10N_87_B12	B12	PMOD0_4
IO_L10P_AD10P_87_C12	C12	PMOD0_5
IO_L9N_AD11N_87_C13	C13	PMOD0_6
IO_L9P_AD11P_87_C14	C14	PMOD0_7
IO_L8N_HDGC_87_D13	D13	PMOD1_0
IO_L8P_HDGC_87_D14	D14	PMOD1_1
IO_L7N_HDGC_87_E12	E12	PMOD1_2
IO_L7P_HDGC_87_E13	E13	PMOD1_3
IO_L6N_HDGC_87_F13	F13	PMOD1_4
IO_L6P_HDGC_87_F14	F14	PMOD1_5
IO_L5N_HDGC_87_F12	F12	CLK_125_N
IO_L5P_HDGC_87_G12	G12	CLK_125_P
IO_L4N_AD12N_87_J14	J14	PMOD1_6
IO_L4P_AD12P_87_J15	J15	PMOD1_7
IO_L3N_AD13N_87_G14	G14	IIC_EXPANDER_GPIO
IO_L3P_AD13P_87_H14	H14	FMC_HPC0_PRSNT_M2C_B
IO_L2N_AD14N_87_H13	H13	FMC_HPC0_PG_M2C
IO_L2P_AD14P_87_J13	J13	VADJ_FMC_PGOOD
IO_L1N_AD15N_87_H12	H12	NC
IO_L1P_AD15P_87_J12	J12	NC

VCC3V3

E14	VCCO_87_E14
H15	VCCO_87_H15

CLK_125_P

1 **R431** 2
100
1/10W
1%

CLK_125_N

U1

SOC_676_1MM_IRON

SOC_DK5_FFVB676_IRONWOOD

BANK 84
XCKU5PFFVB676

IO_L12N_AD0N_84_W13	W13	USB_UART_RX_FPGA_TX_LS
IO_L12P_AD0P_84_W12	W12	USB_UART_TX_FPGA_RX_LS
IO_L11N_AD1N_84_AA13	AA13	USB_UART_RTS_O_B_LS
IO_L11P_AD1P_84_Y13	Y13	USB_UART_CTS_I_B_LS
IO_L10N_AD2N_84_W15	W15	SYSCTLR_GPIO_5
IO_L10P_AD2P_84_W14	W14	SYSCTLR_GPIO_6
IO_L9N_AD3N_84_Y16	Y16	SYSCTLR_GPIO_7
IO_L9P_AD3P_84_W16	W16	SFP_SI5328_INT_ALM
IO_L8N_HDGC_AD4N_84_AB14	AB14	SFP0_TX_DISABLE_B
IO_L8P_HDGC_AD4P_84_AA14	AA14	SFP1_TX_DISABLE_B
IO_L7N_HDGC_AD5N_84_AA15	AA15	SFP2_TX_DISABLE_B
IO_L7P_HDGC_AD5P_84_Y15	Y15	SFP3_TX_DISABLE_B
IO_L6N_HDGC_AD6N_84_AB16	AB16	NC
IO_L6P_HDGC_AD6P_84_AB15	AB15	NC
IO_L5N_HDGC_AD7N_84_AC14	AC14	NC
IO_L5P_HDGC_AD7P_84_AC13	AC13	NC
IO_L4N_AD8N_84_AD14	AD14	NC
IO_L4P_AD8P_84_AD13	AD13	NC
IO_L3N_AD9N_84_AE15	AE15	IIC_SDA_HDMI
IO_L3P_AD9P_84_AD15	AD15	IIC_SCL_HDMI
IO_L2N_AD10N_84_AF13	AF13	IIC_MAIN_SDA_LS
IO_L2P_AD10P_84_AE13	AE13	IIC_MAIN_SCL_LS
IO_L1N_AD11N_84_AF15	AF15	NC
IO_L1P_AD11P_84_AF14	AF14	NC

VCC3V3

AC15	VCCO_84_AC15
Y14	VCCO_84_Y14

U1

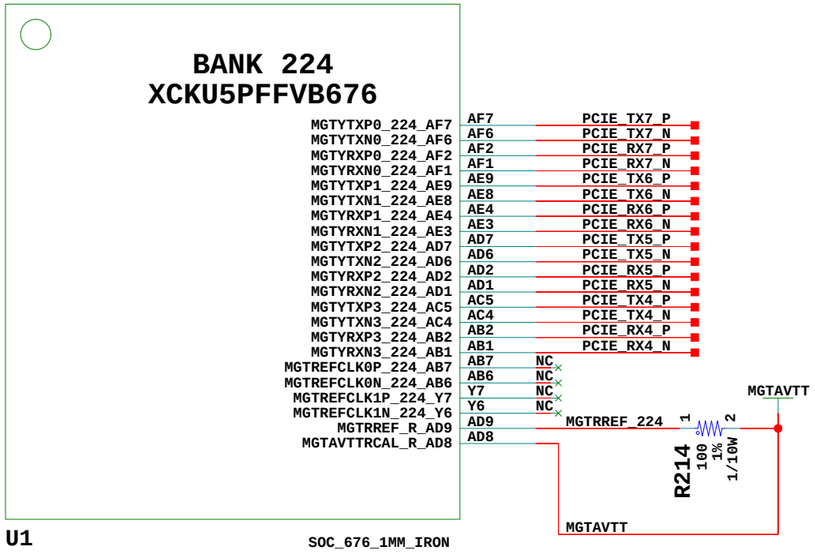
SOC_676_1MM_IRON

FPGA Banks 87 PMOD 84 UART ZSFP SMA

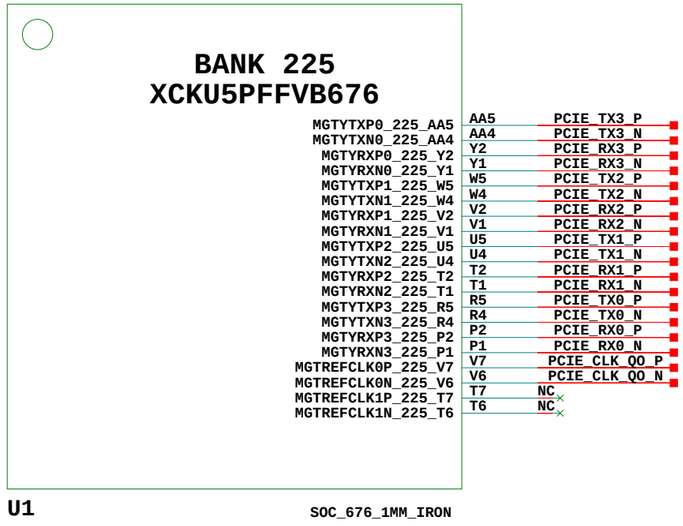
XILINX

TITLE: FPGA Banks 87 PMOD 84 UART ZSFP SMA SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 9 OF 60	DRAWN BY: DN

SOC_DK5_FFVB676_IRONWOOD



SOC_DK5_FFVB676_IRONWOOD



FPGA GTY224 GTY225 PCIE

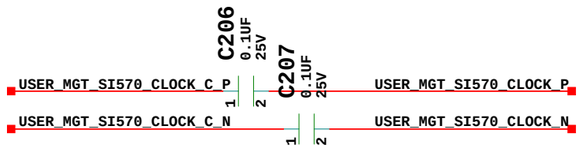
XILINX

TITLE: FPGA GTY224 GTY225 PCIE SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/04/2017:14:52	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 10 OF 60	DRAWN BY: DN

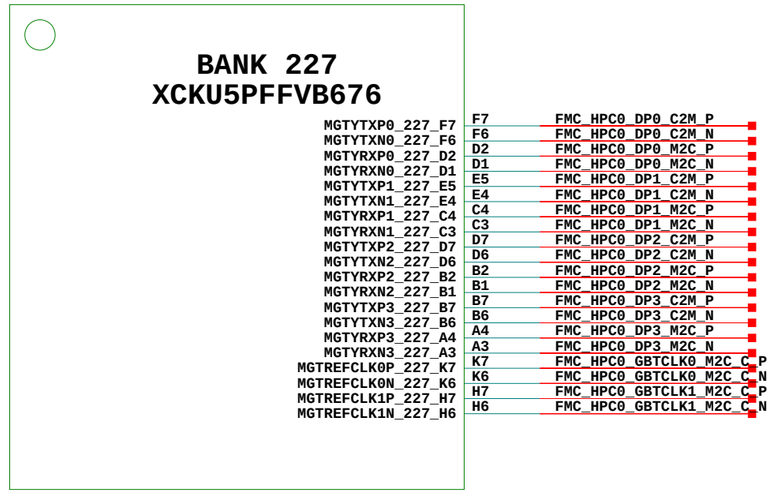
SOC_DK5_FFVB676_IRONWOOD

U1

SOC_676_1MM_IRON

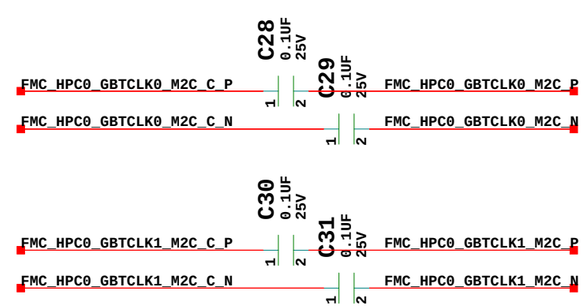


SOC_DK5_FFVB676_IRONWOOD



U1

SOC_676_1MM_IRON



FPGA GTY226 - ZSFP GTY227 - FMC DP

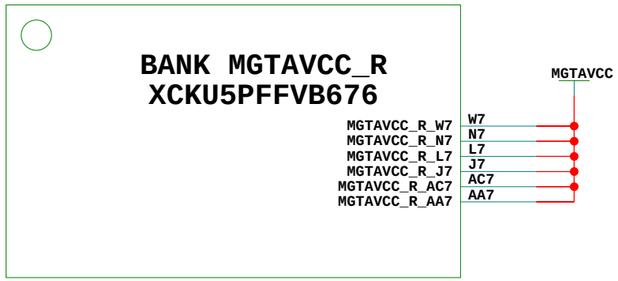
XILINX

TITLE: FPGA GTY226 - ZSFP GTY227 - FMC DP
SCHEM, ROHS COMPLIANT
HW-U1-KCU116_REV1_0

ASSY P/N: 0432019
PCB P/N: 1280924
SCH P/N: 0381757
TEST P/N: TSSXXXX

DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 11 OF 60	DRAWN BY: DN

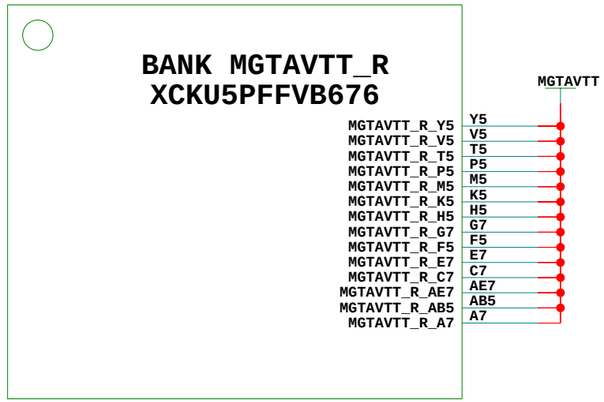
SOC_DK5_FFVB676_IRONWOOD



U1

SOC_676_1MM_IRON

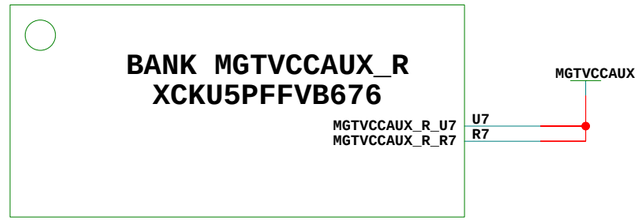
SOC_DK5_FFVB676_IRONWOOD



U1

SOC_676_1MM_IRON

SOC_DK5_FFVB676_IRONWOOD



U1

SOC_676_1MM_IRON

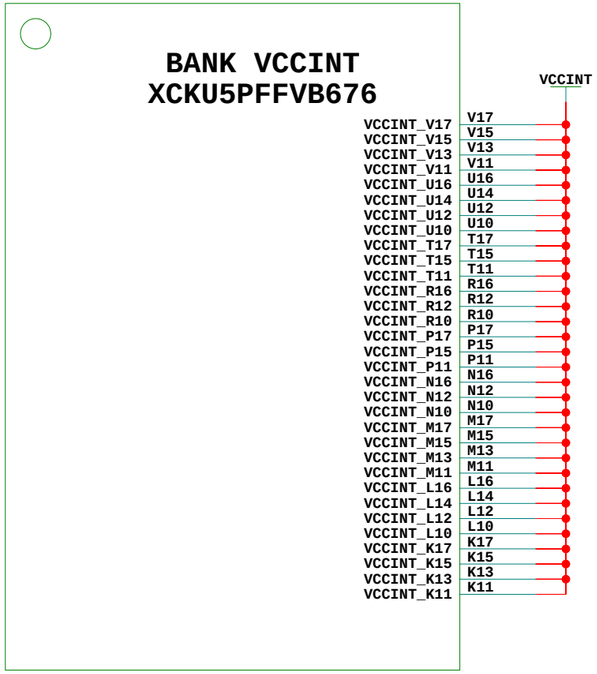
FPGA Power 1

XILINX

TITLE: FPGA Power 1 SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 12 OF 60	DRAWN BY: DN

SOC_DK5_FFVB676_IRONWOOD

BANK VCCINT
XCKU5PFFVB676

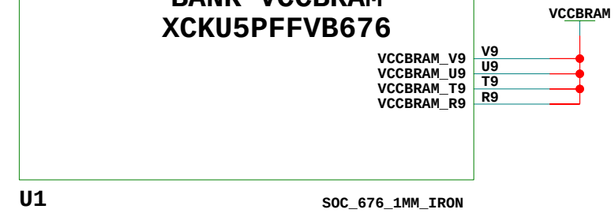


U1

SOC_676_1MM_IRON

SOC_DK5_FFVB676_IRONWOOD

BANK VCCBRAM
XCKU5PFFVB676

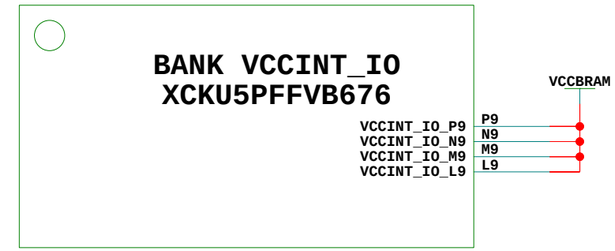


U1

SOC_676_1MM_IRON

SOC_DK5_FFVB676_IRONWOOD

BANK VCCINT_IO
XCKU5PFFVB676



U1

SOC_676_1MM_IRON

SOC_DK5_FFVB676_IRONWOOD

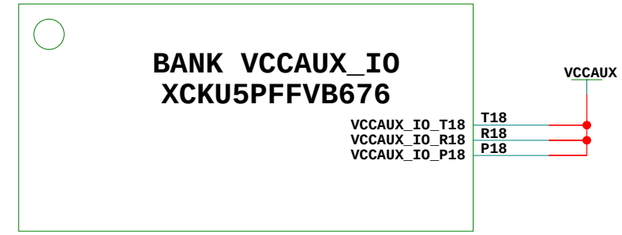
BANK VCCAUX
XCKU5PFFVB676

U1

SOC_676_1MM_IRON

SOC_DK5_FFVB676_IRONWOOD

BANK VCCAUX_IO
XCKU5PFFVB676



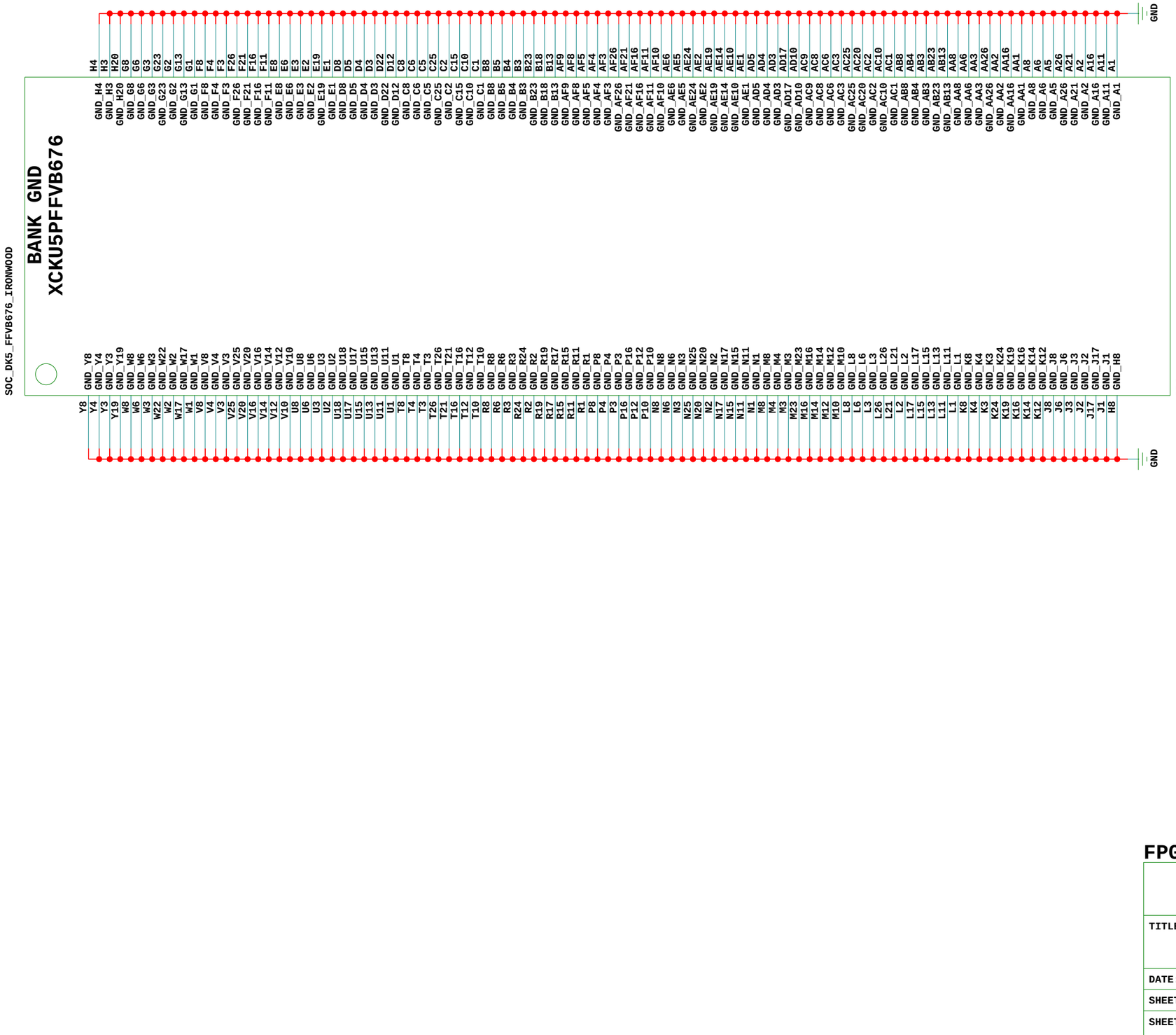
U1

SOC_676_1MM_IRON

FPGA Power 2

XILINX

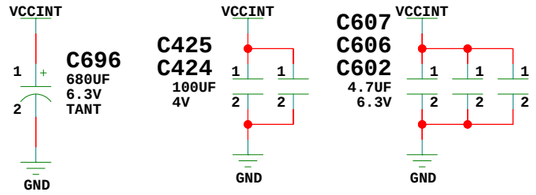
TITLE: FPGA Power 2 SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 13 OF 60	DRAWN BY: DN



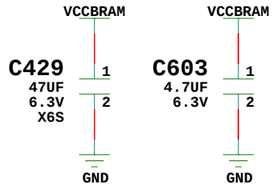
FPGA GND

TITLE: FPGA GND SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 14 OF 60	DRAWN BY: DN

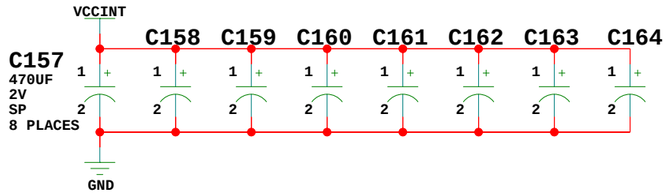
VCCINT (UG583 v1.8)



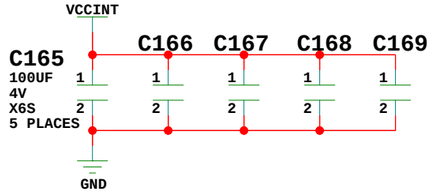
VCCBRAM/VCCINT_IO (UG583 v1.8)



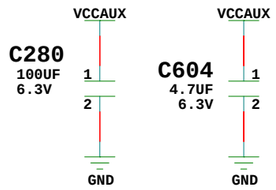
VCCINT (Maxim xlsx)



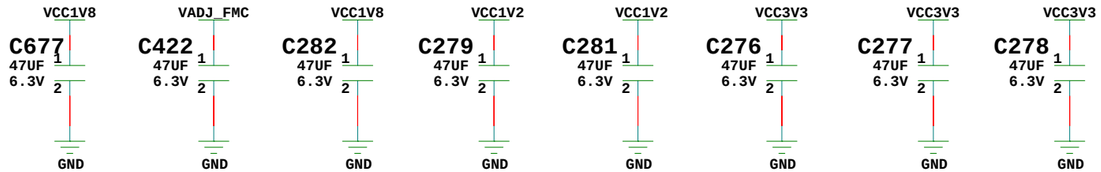
VCCINT (Maxim xlsx)



VCCAUX/VCCAUX_IO (UG583 v1.8)



VCCO BANKS 0 64 65 66 67 84 86 87 (UG583 v1.8)



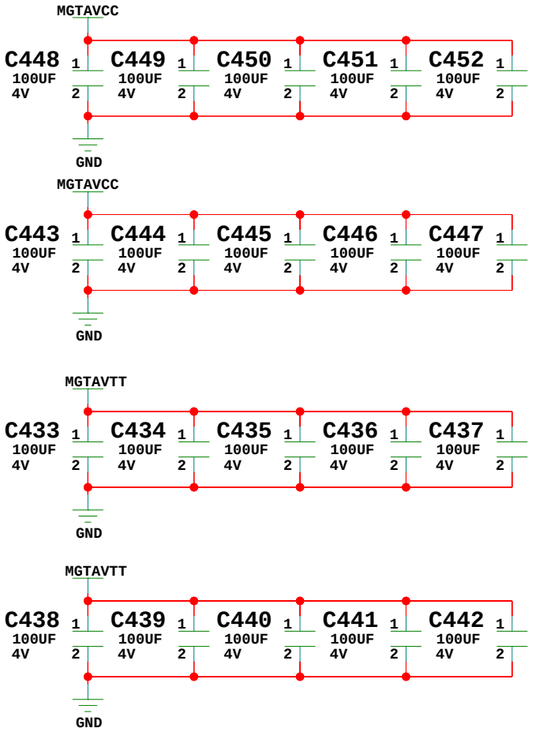
FPGA Decoupling 1

XILINX

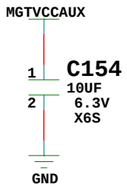
TITLE: FPGA Decoupling 1 SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 15 OF 60	DRAWN BY: DN

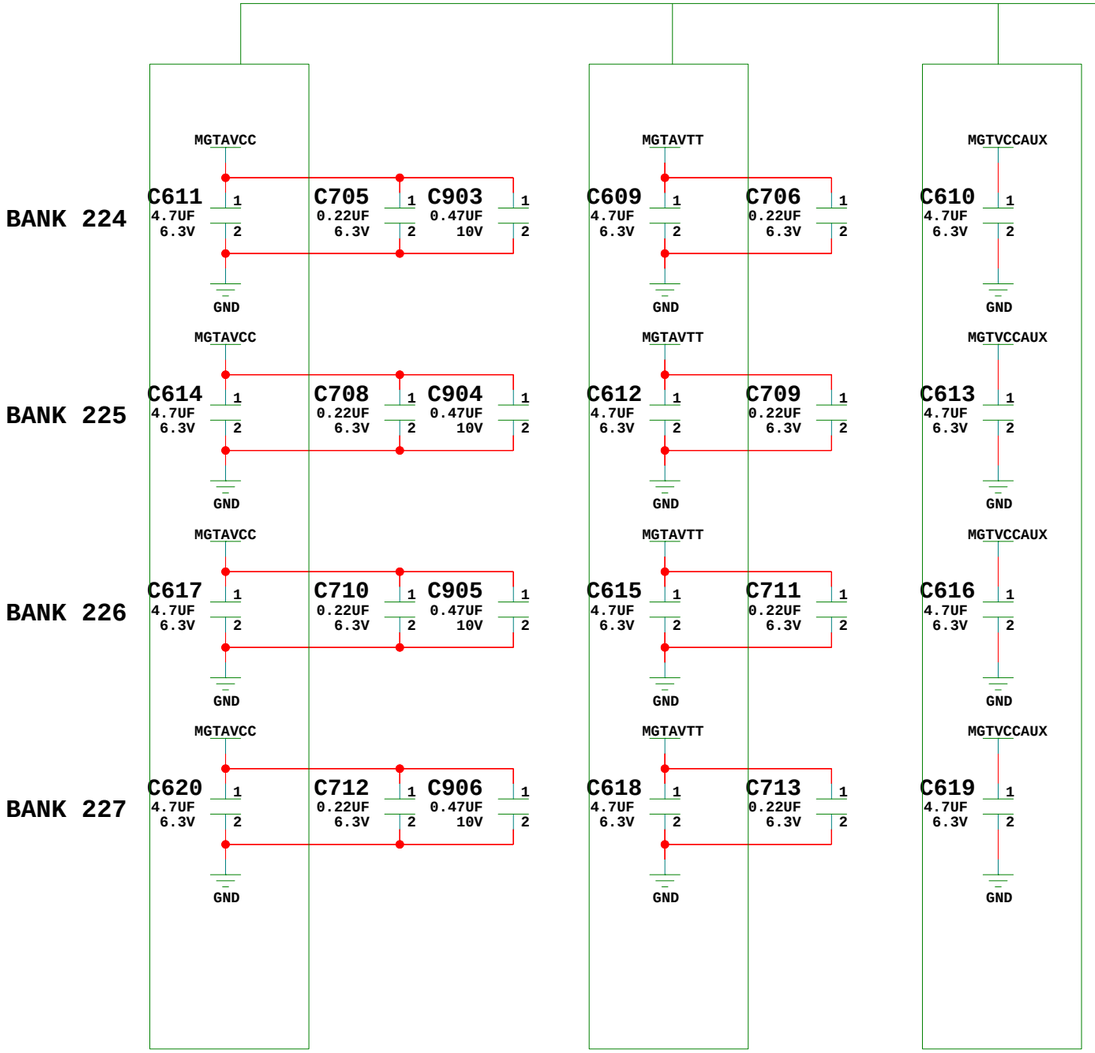
(UG578 v1.1)

Decoupling Source: E-mail from Maxim 7/9/2015



MGTVCCAUX (Maxim xlsx)

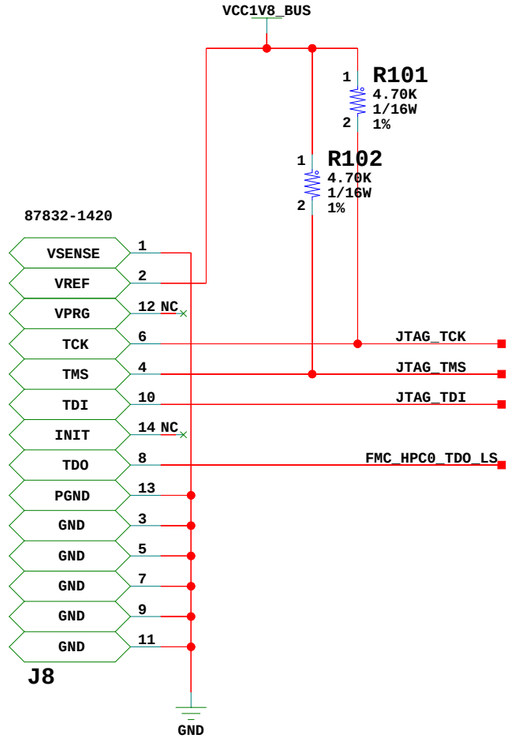


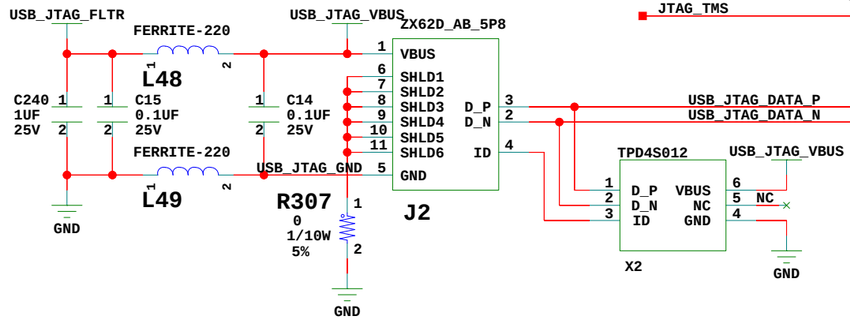


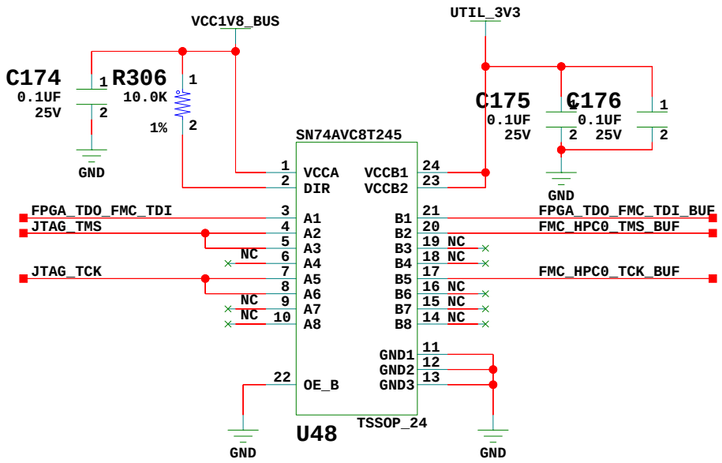
FPGA Decoupling 2

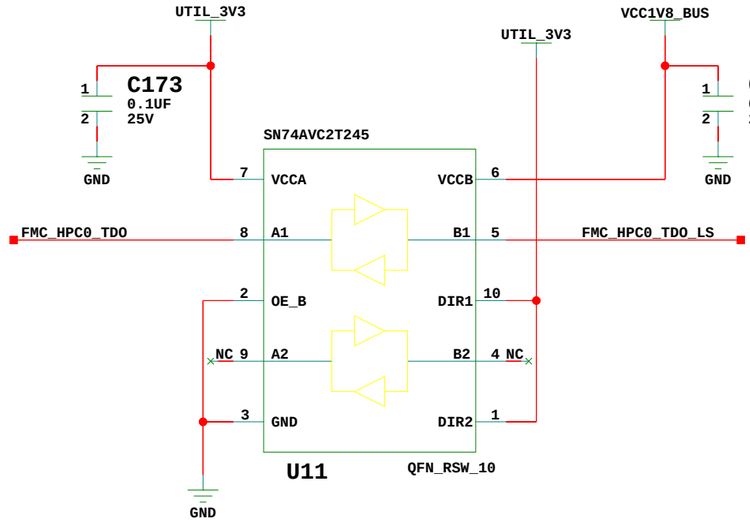
XILINX

TITLE: FPGA Decoupling 2 SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 16 OF 60	DRAWN BY: DN





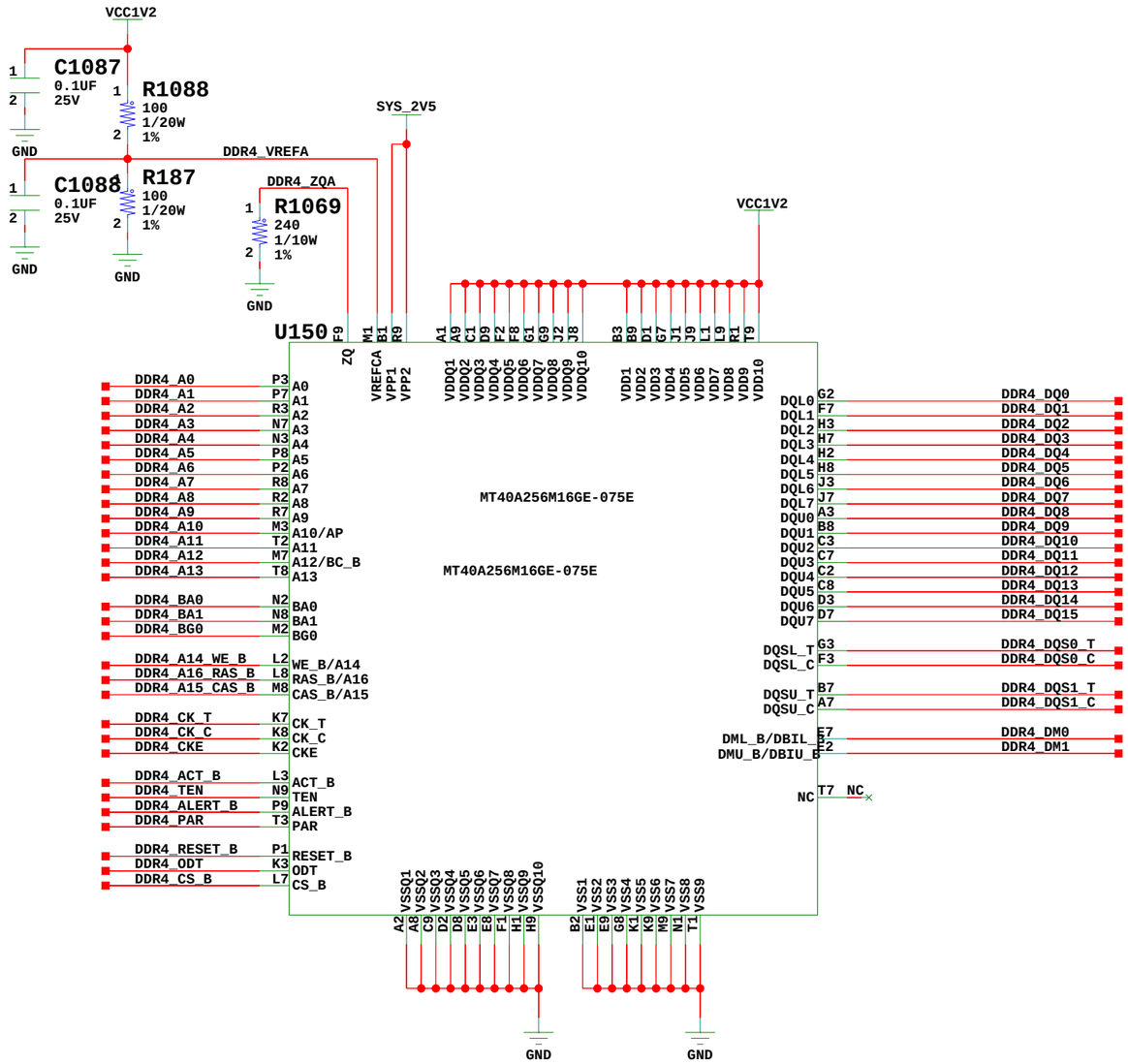


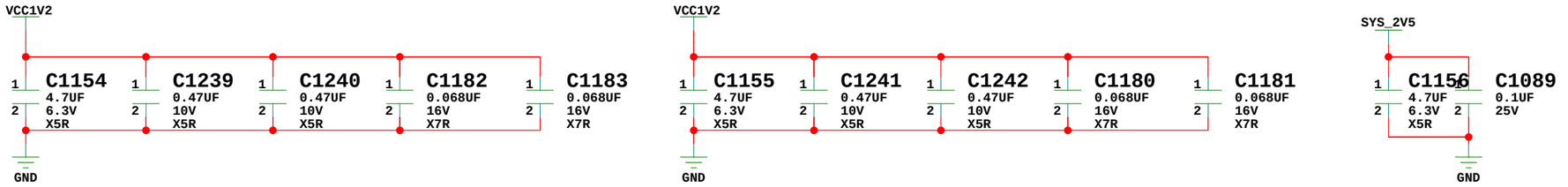


JTAG Headers

XILINX

TITLE: JTAG Headers SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 17 OF 60	DRAWN BY: DN

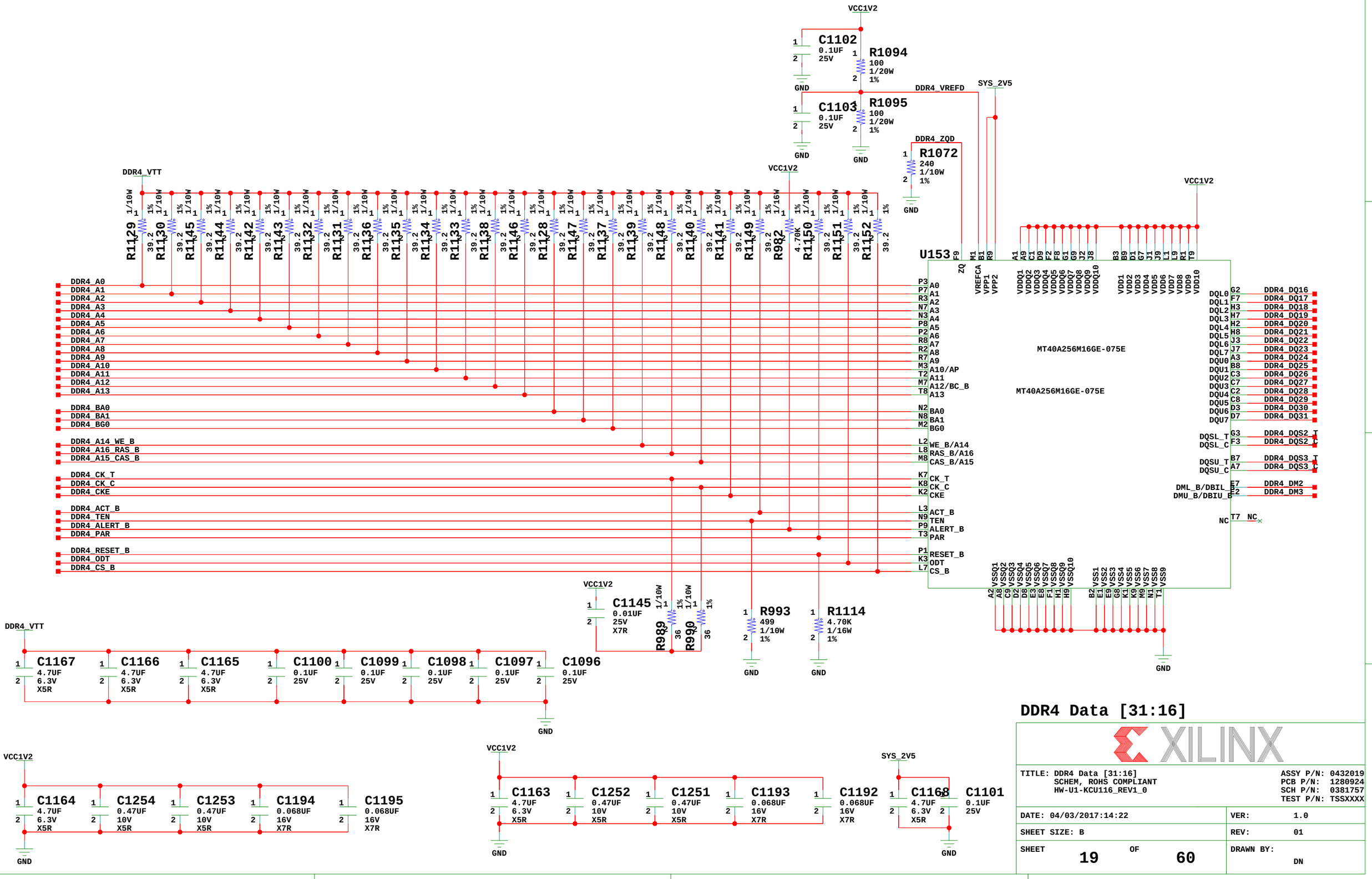




DDR4 Data [15-0]

XILINX

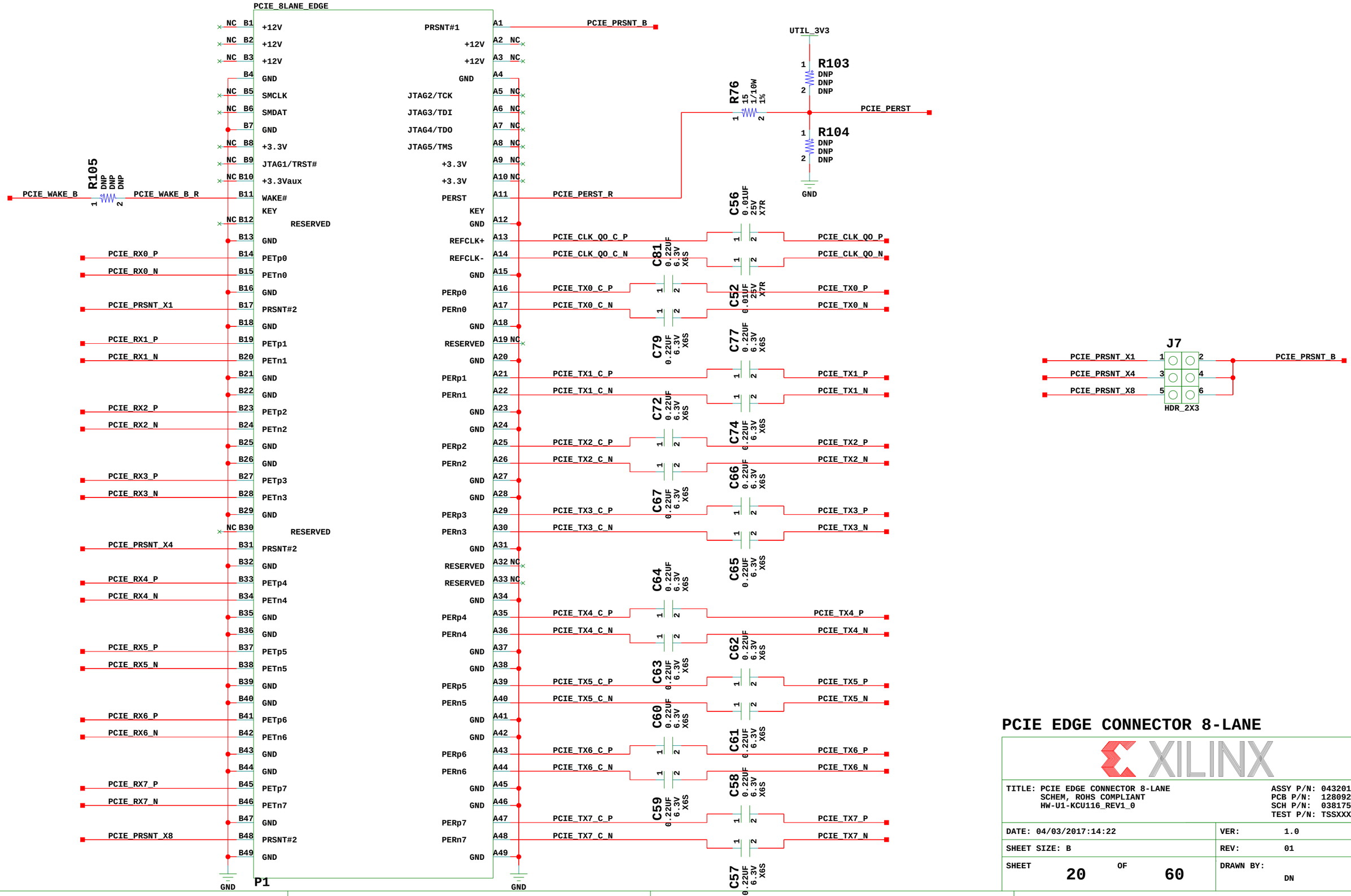
TITLE: DDR4 Data [15-0] SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 18 OF 60	DRAWN BY: DN



DDR4 Data [31:16]

XILINX

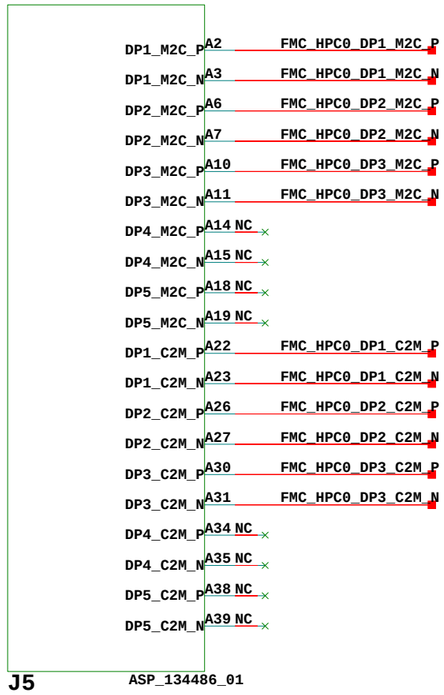
TITLE: DDR4 Data [31:16] SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 19 OF 60	DRAWN BY: DN

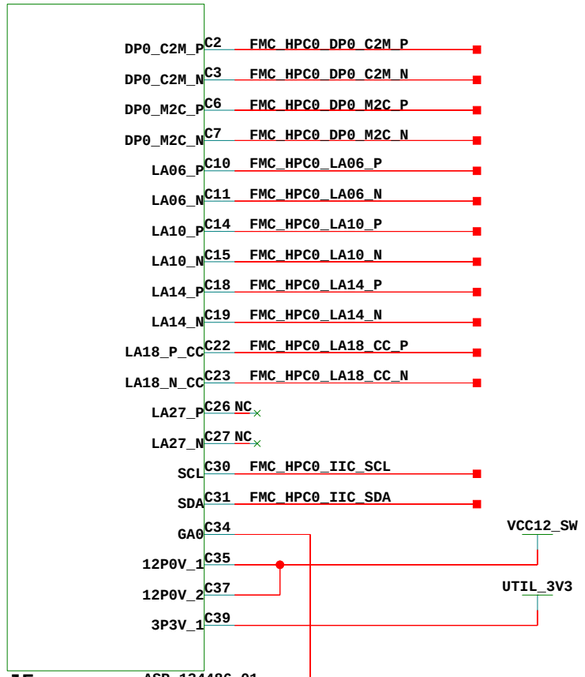


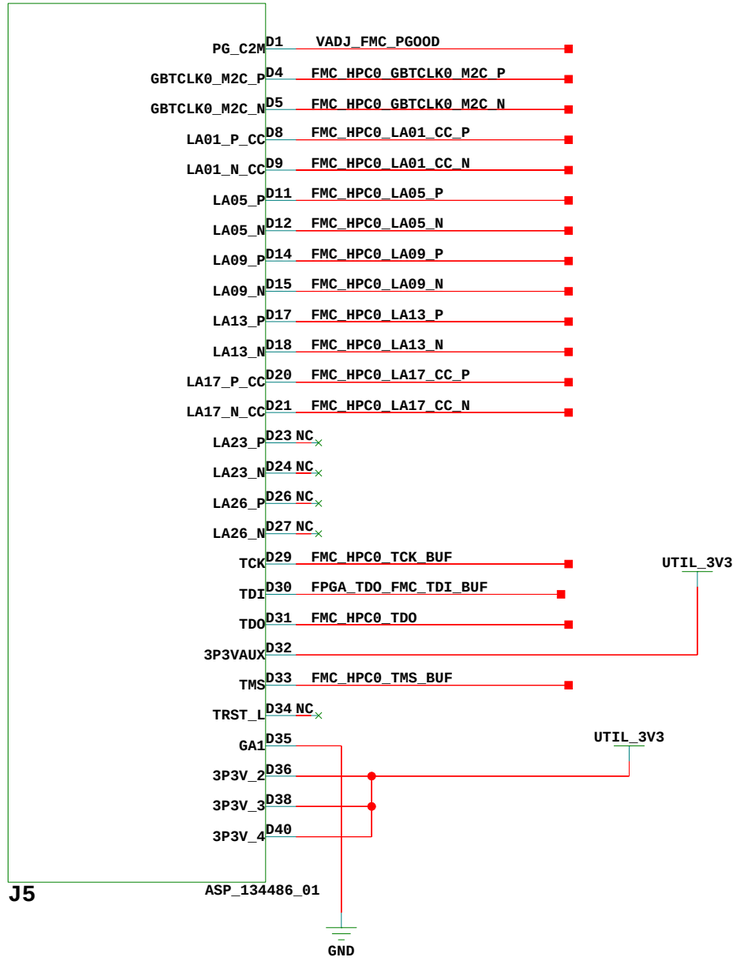
PCIE EDGE CONNECTOR 8-LANE

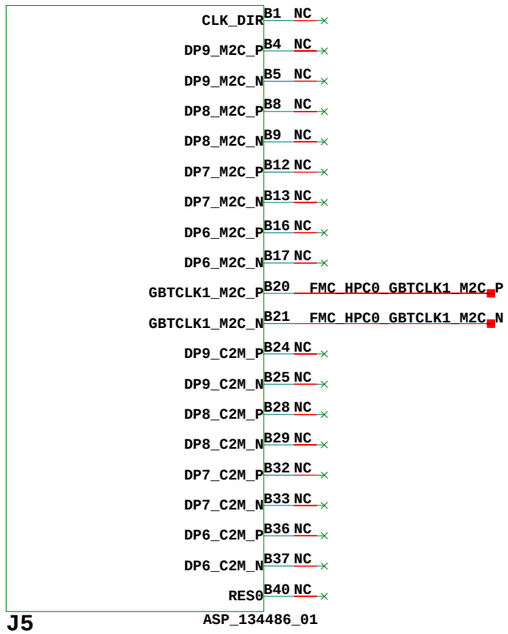
XILINX

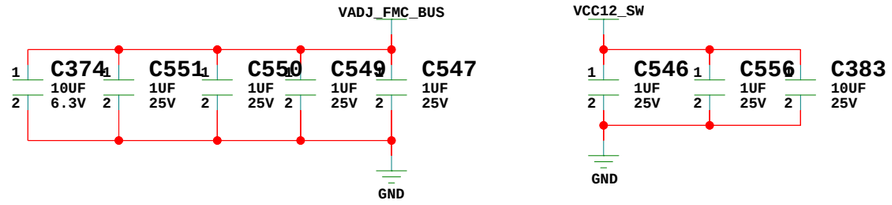
TITLE: PCIE EDGE CONNECTOR 8-LANE SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 20 OF 60	DRAWN BY: DN

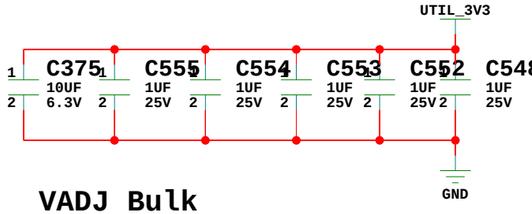




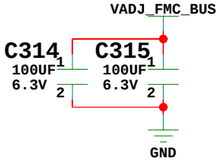




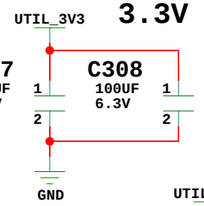


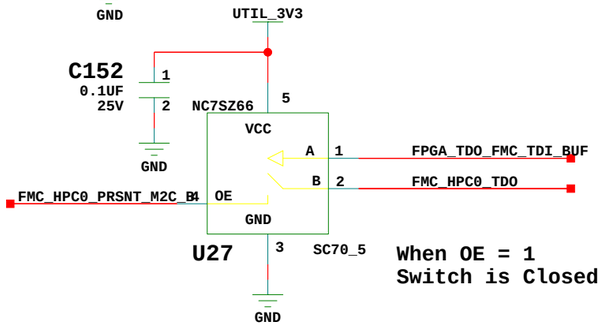


VADJ Bulk



3.3V Bulk

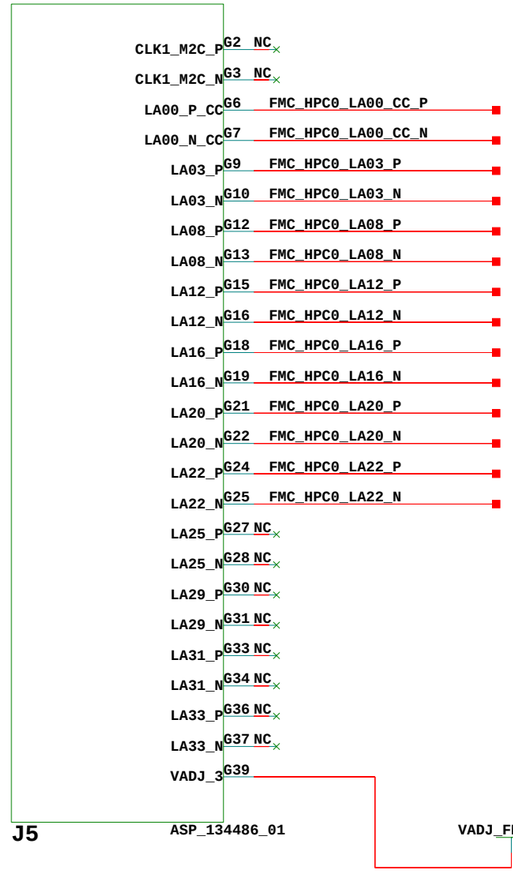




ANSI/VITA 57.1 - Revised 2010
FMC+ HPC0 Header Rows A B C D

XILINX

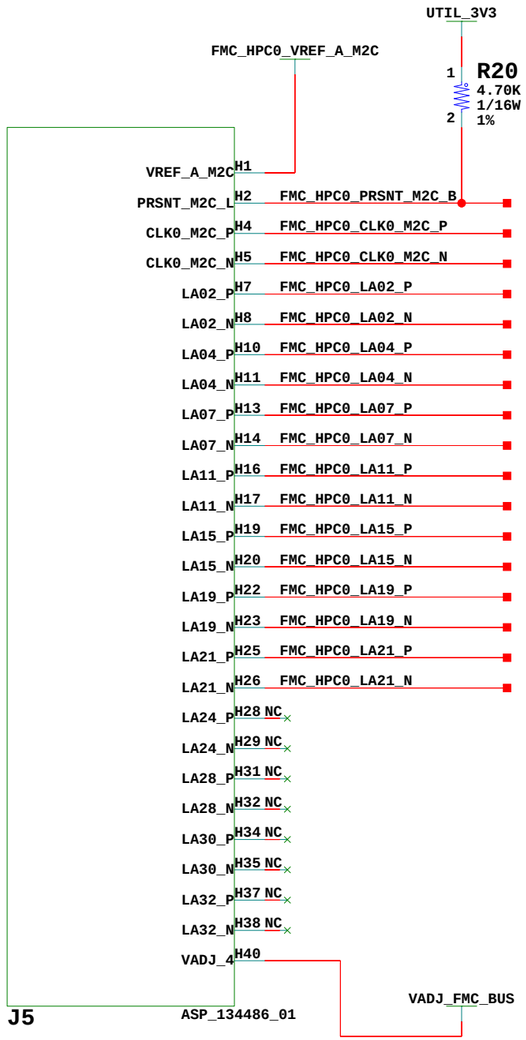
TITLE: FMC+ HPC0 Header Rows A B C D SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 21 OF 60	DRAWN BY: DN

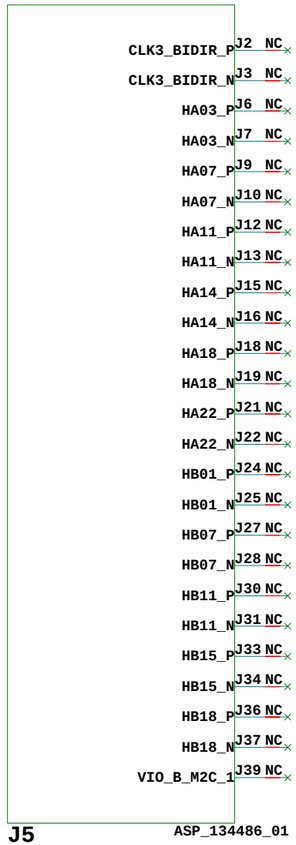


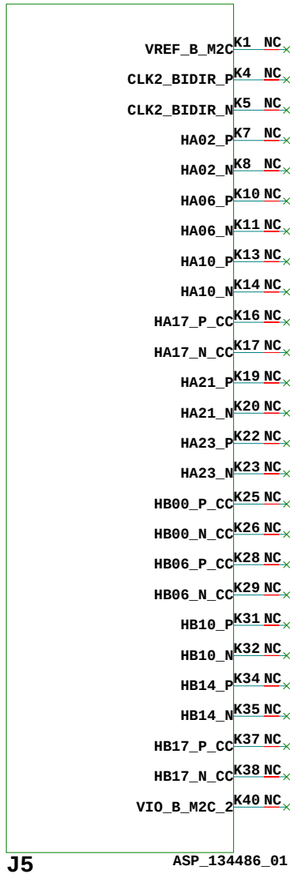
ANSI/VITA 57.1 - Revised 2010
FMC+ HPC0 Header Rows E F G

XILINX

TITLE: FMC+ HPC0 Header Rows E F G SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 22 OF 60	DRAWN BY: DN



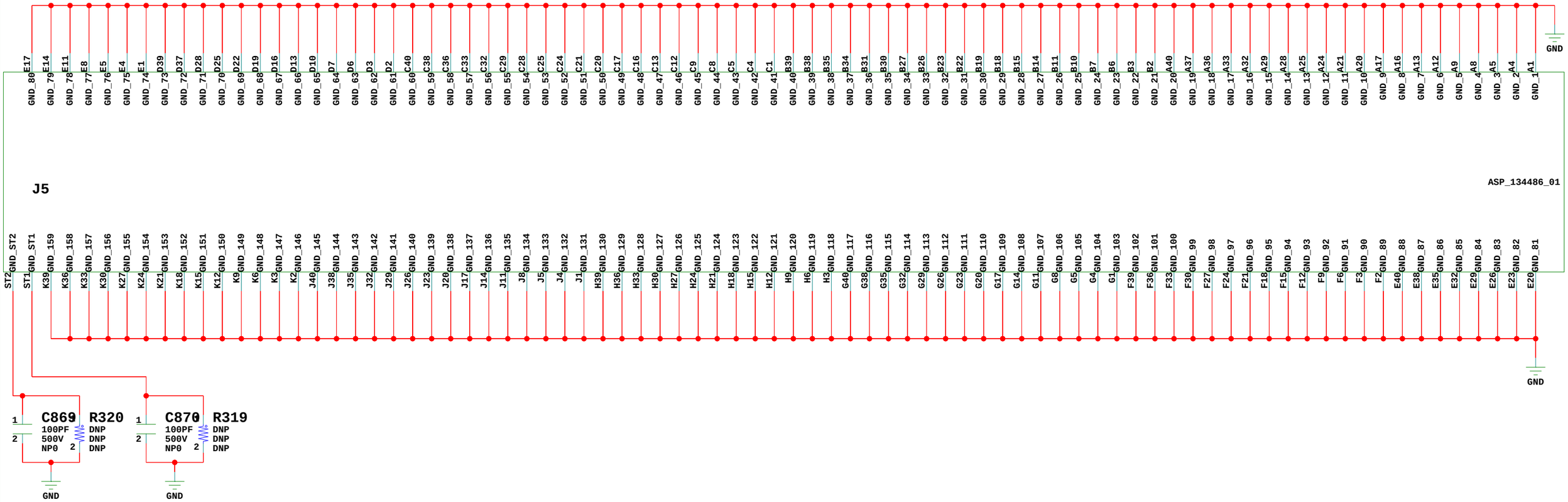




ANSI/VITA 57.1 - Revised 2010
FMC+ HPC0 Header Rows H J K

XILINX

TITLE: FMC+ HPC0 Header Rows H J K SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 23 OF 60	DRAWN BY: DN



ANSI/VITA 57.1 - Revised 2010
FMC+ HPC0 Header_GND

XILINX

TITLE: FMC+ HPC0 Header_GND SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 24 OF 60	DRAWN BY: DN

D C B A

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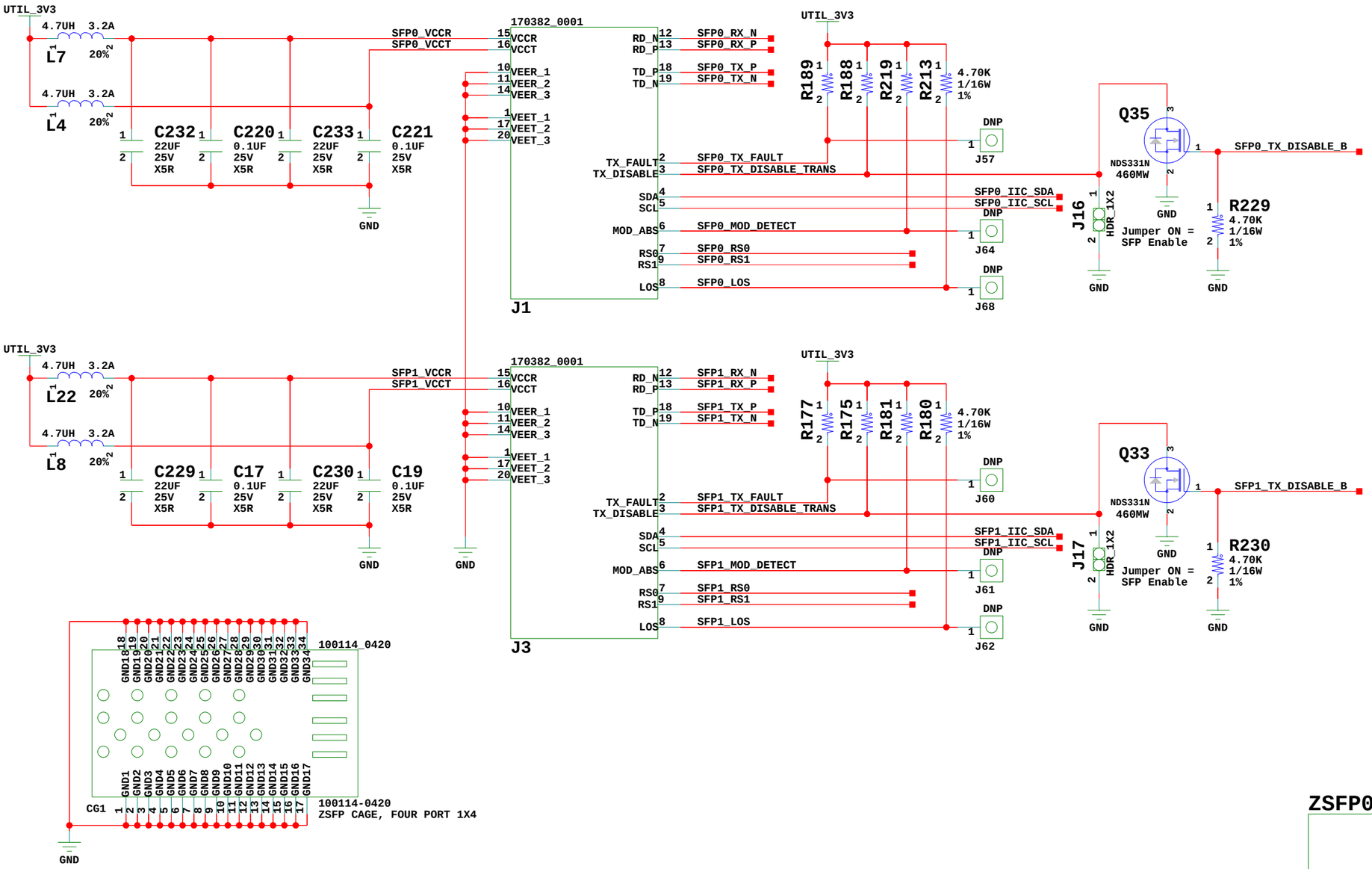
Blank

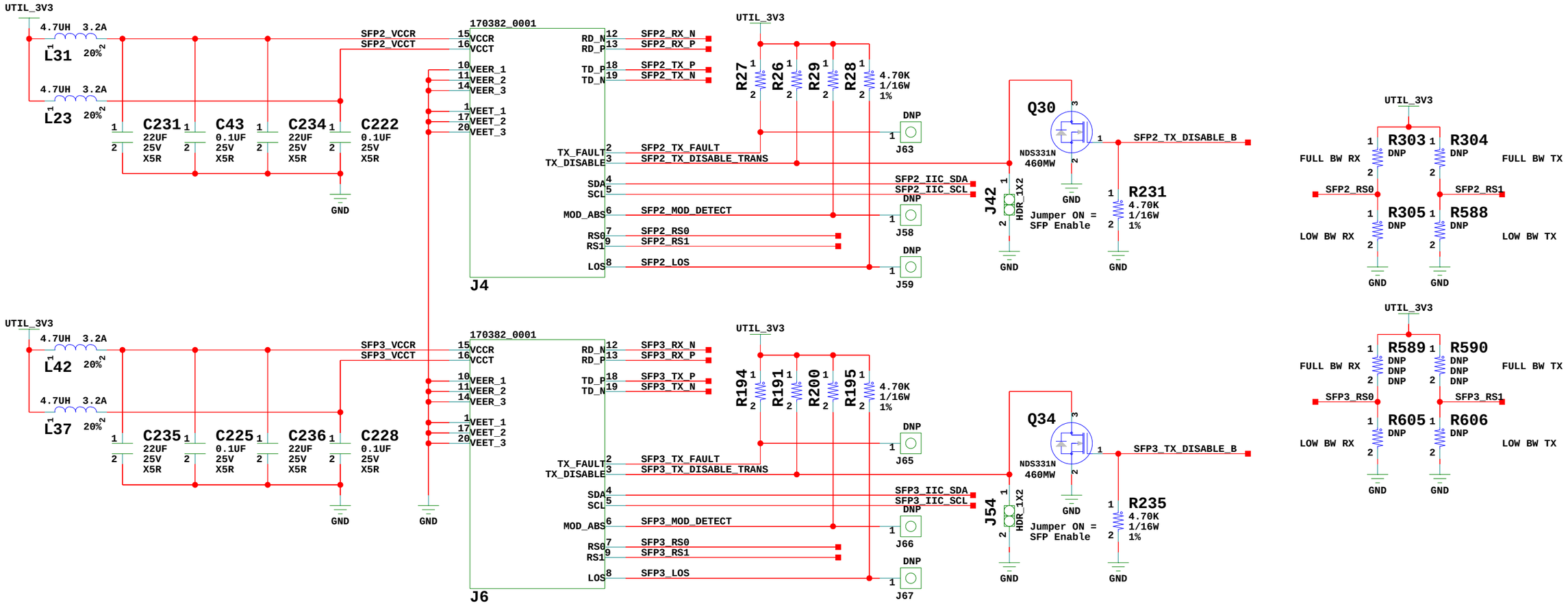
XILINX

TITLE: Blank SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 25 OF 60	DRAWN BY: DN



ZSFP0 and ZSFP1

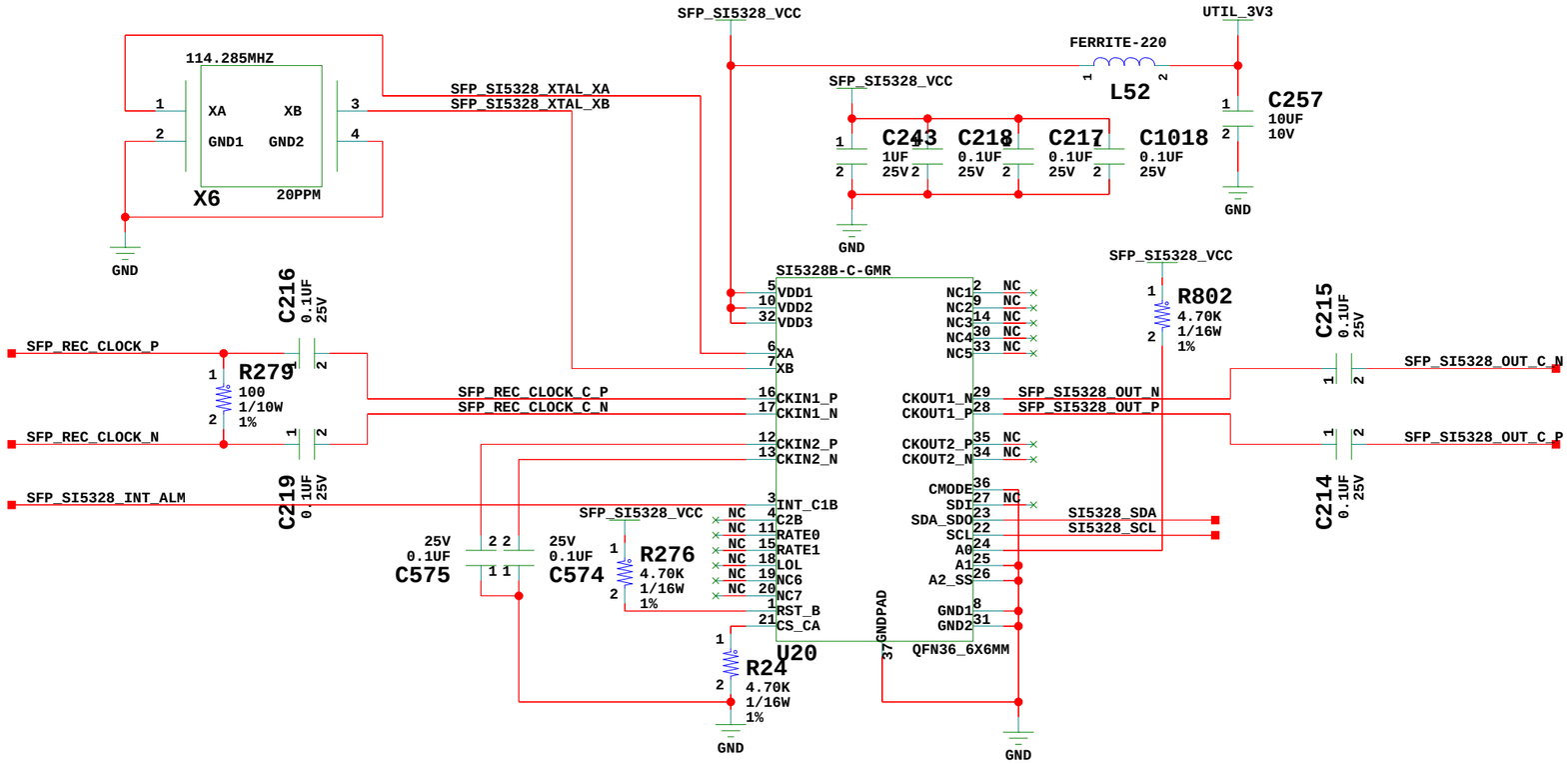
TITLE: ZSFP0 and ZSFP1 SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 26 OF 60	DRAWN BY: DN



ZSFP2 and ZSPF3

XILINX

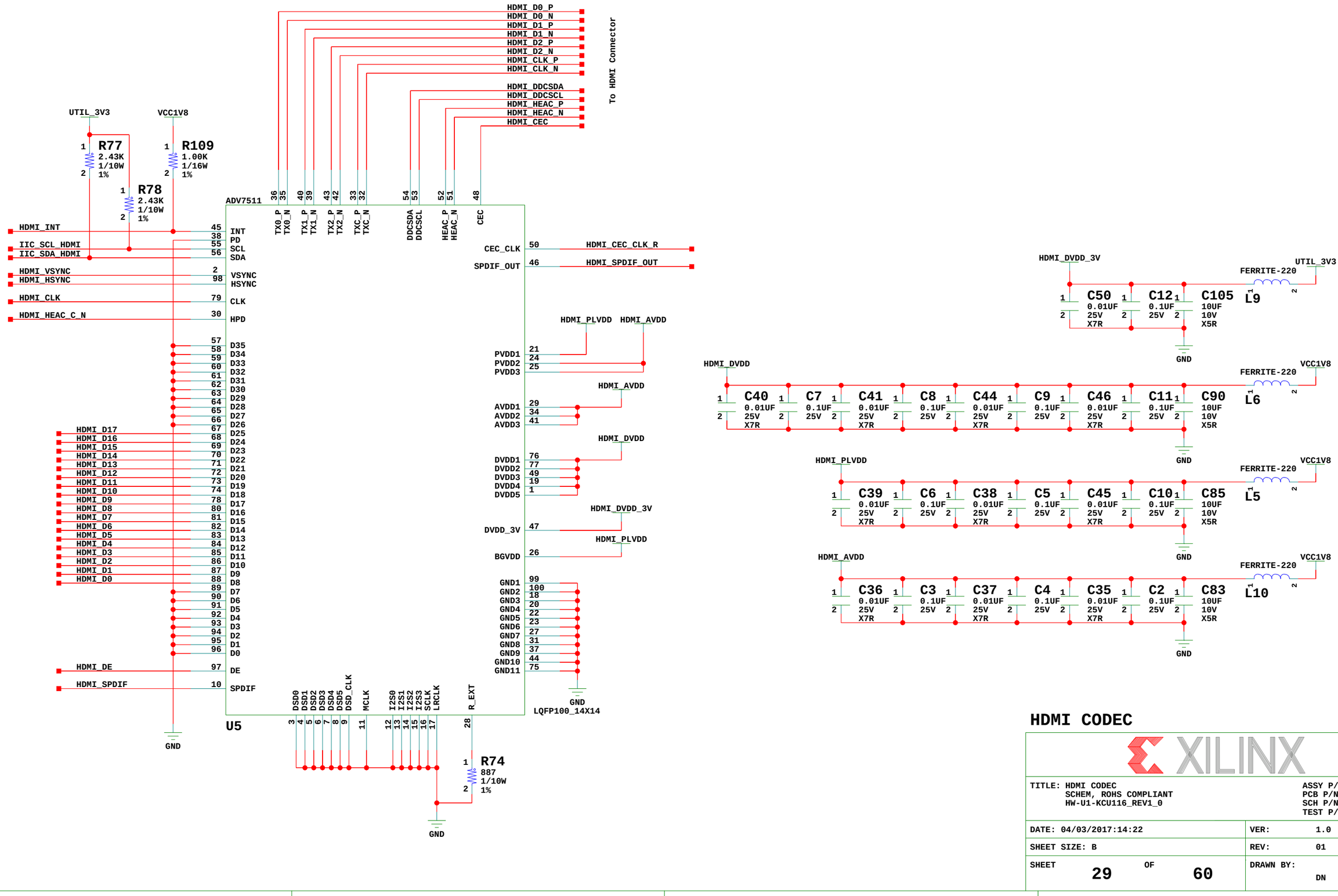
TITLE: ZSFP2 and ZSPF3 SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 27 OF 60	DRAWN BY: DN



SFP Clock Recovery

XILINX

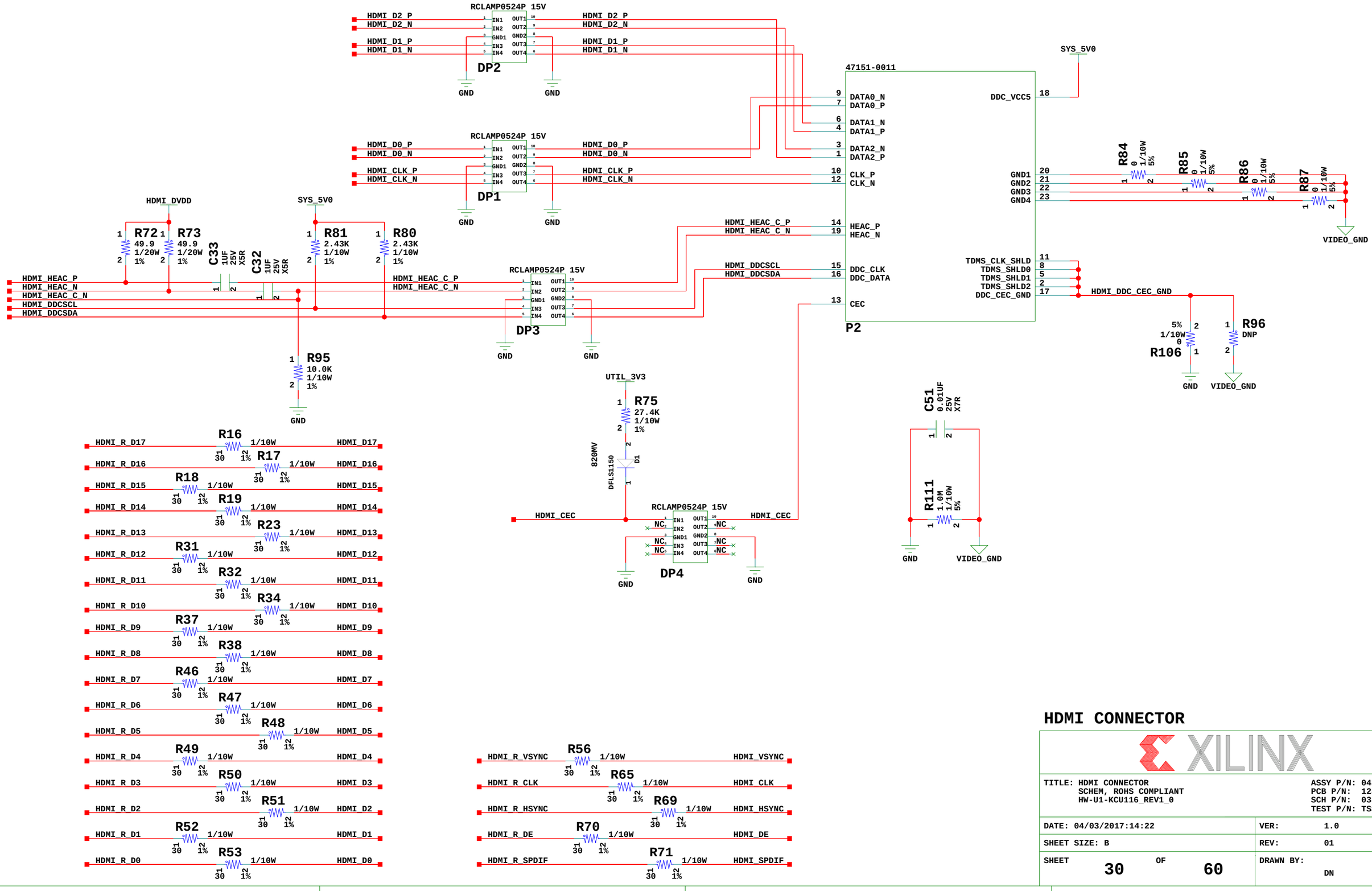
TITLE: SFP Clock Recovery SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 02
SHEET 28 OF 60	DRAWN BY: DN



HDMI CODEC

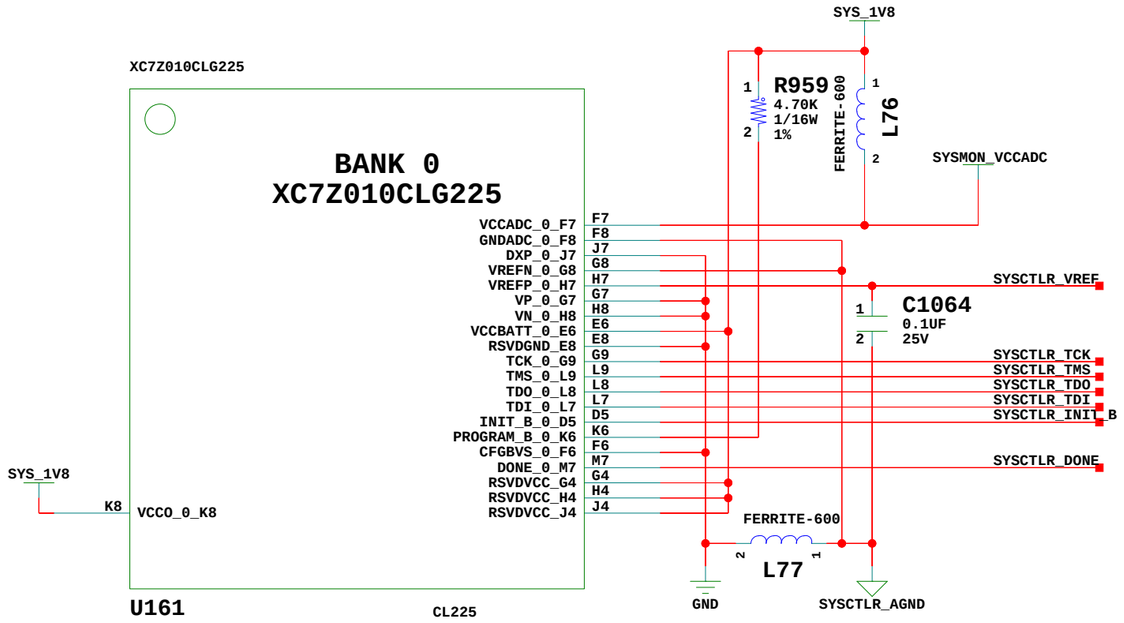
XILINX

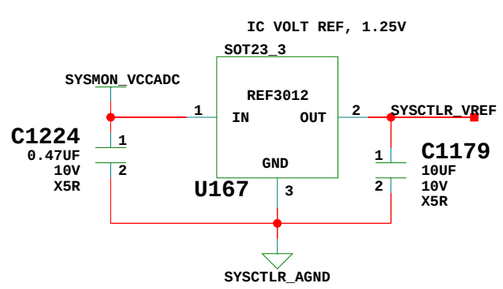
TITLE: HDMI CODEC SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 29 OF 60	DRAWN BY: DN

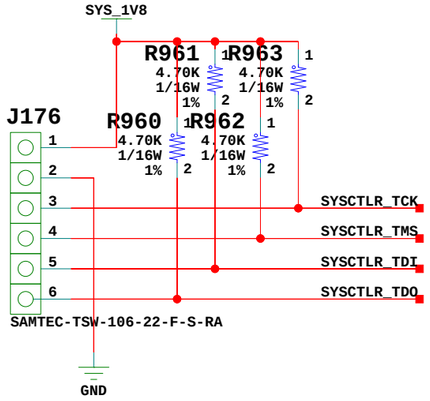


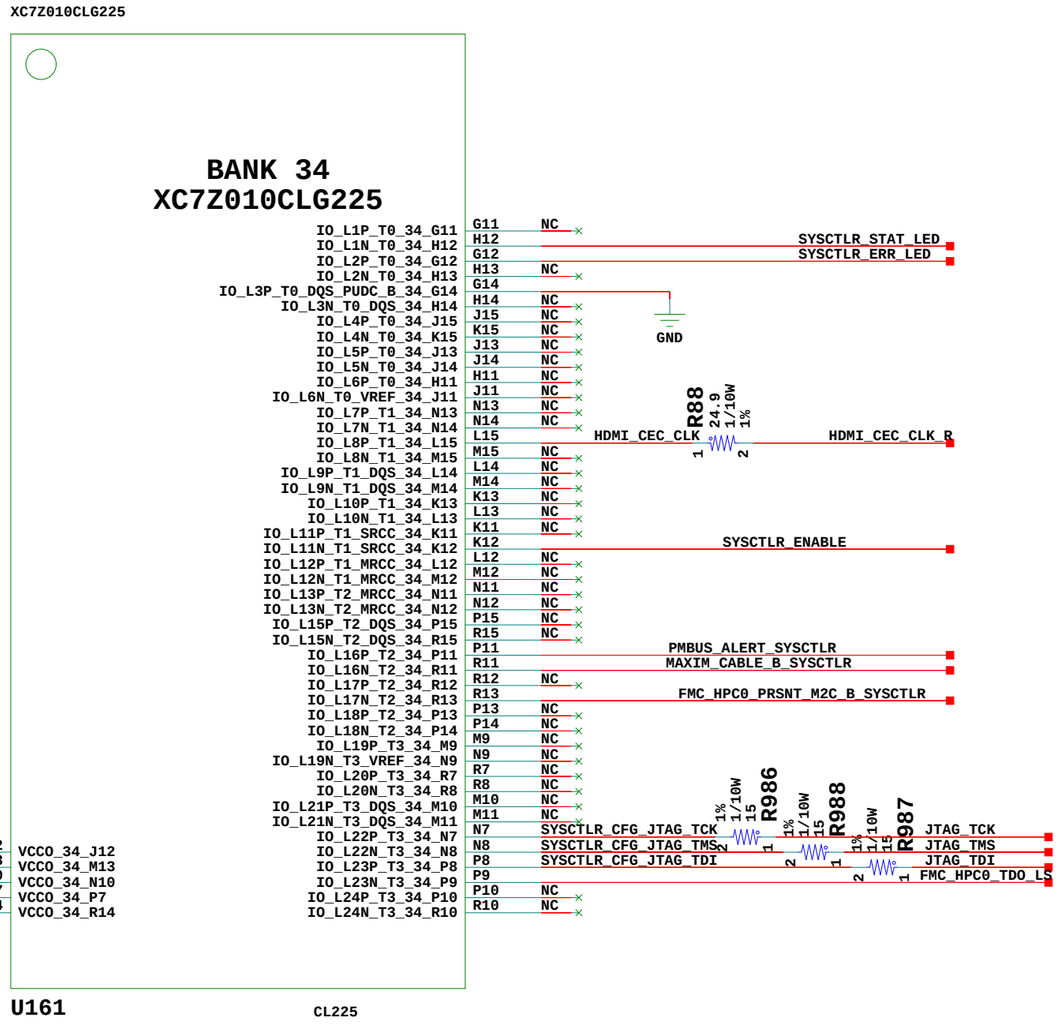
HDMI CONNECTOR

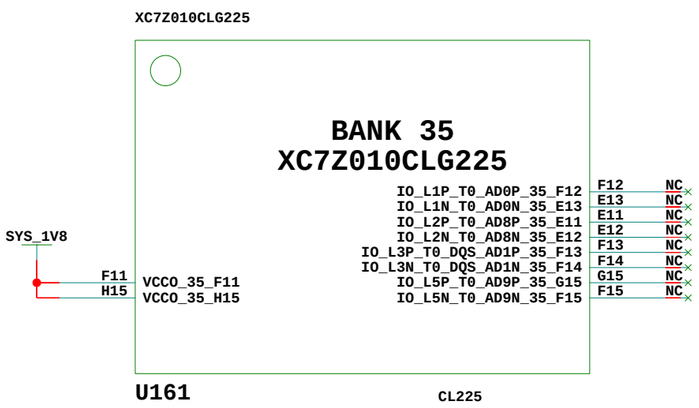
TITLE: HDMI CONNECTOR SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 30 OF 60	DRAWN BY: DN

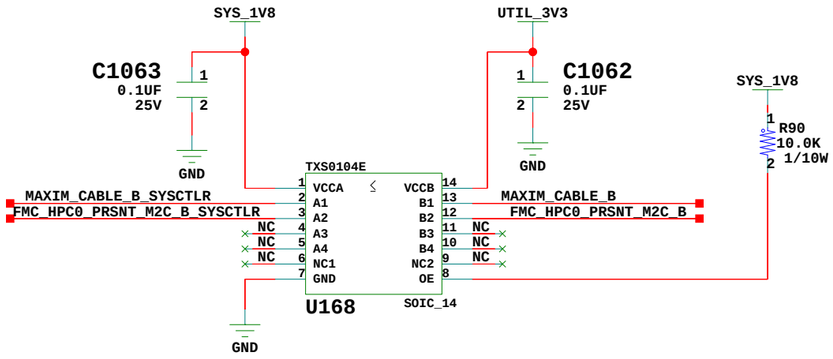








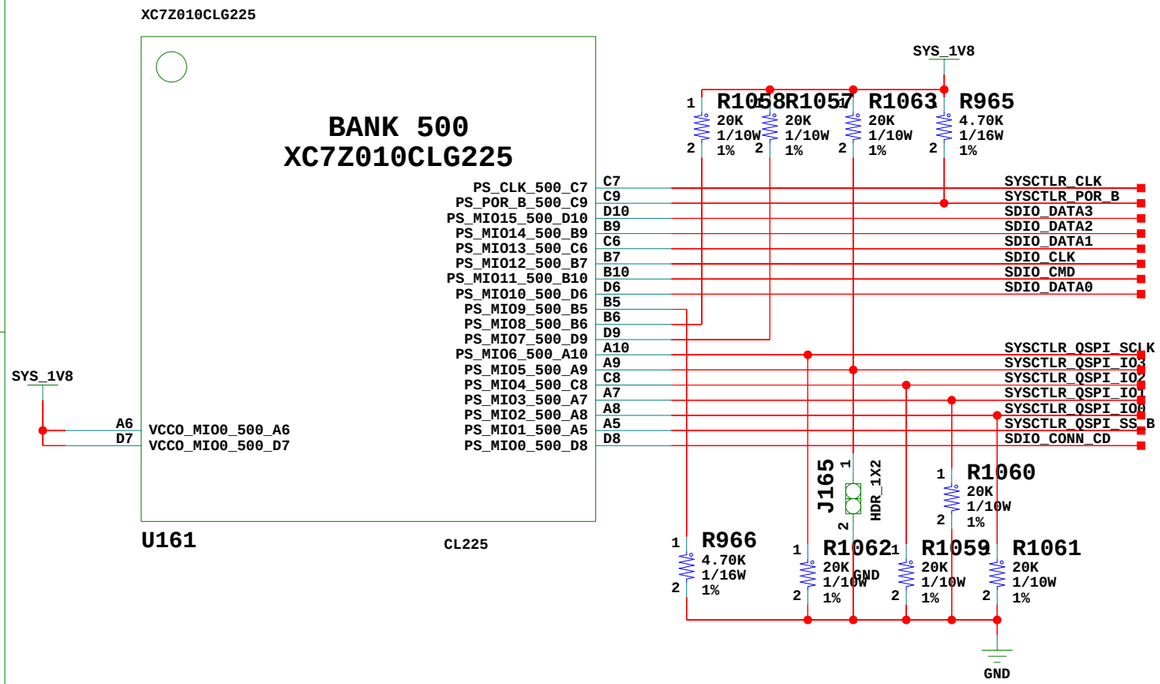


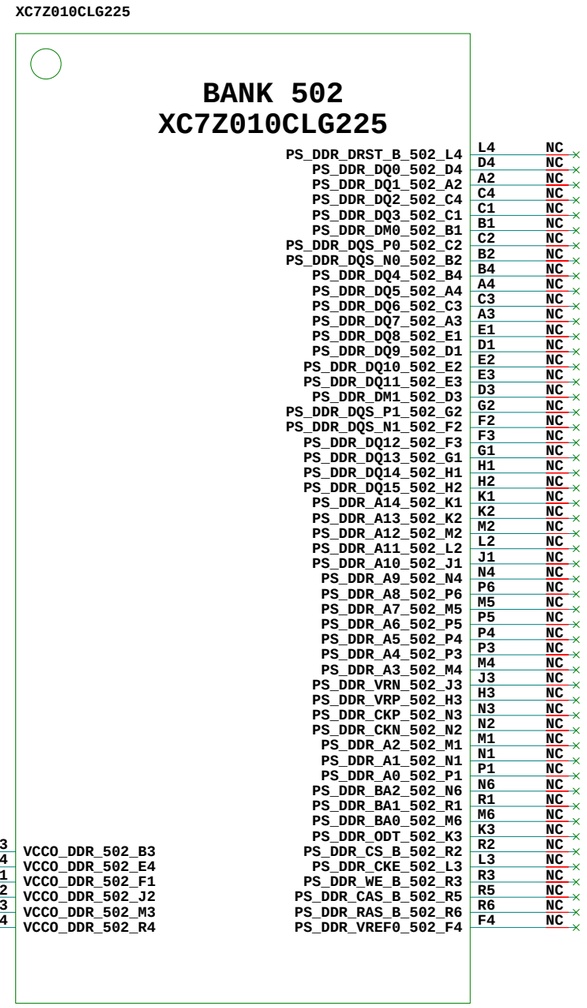


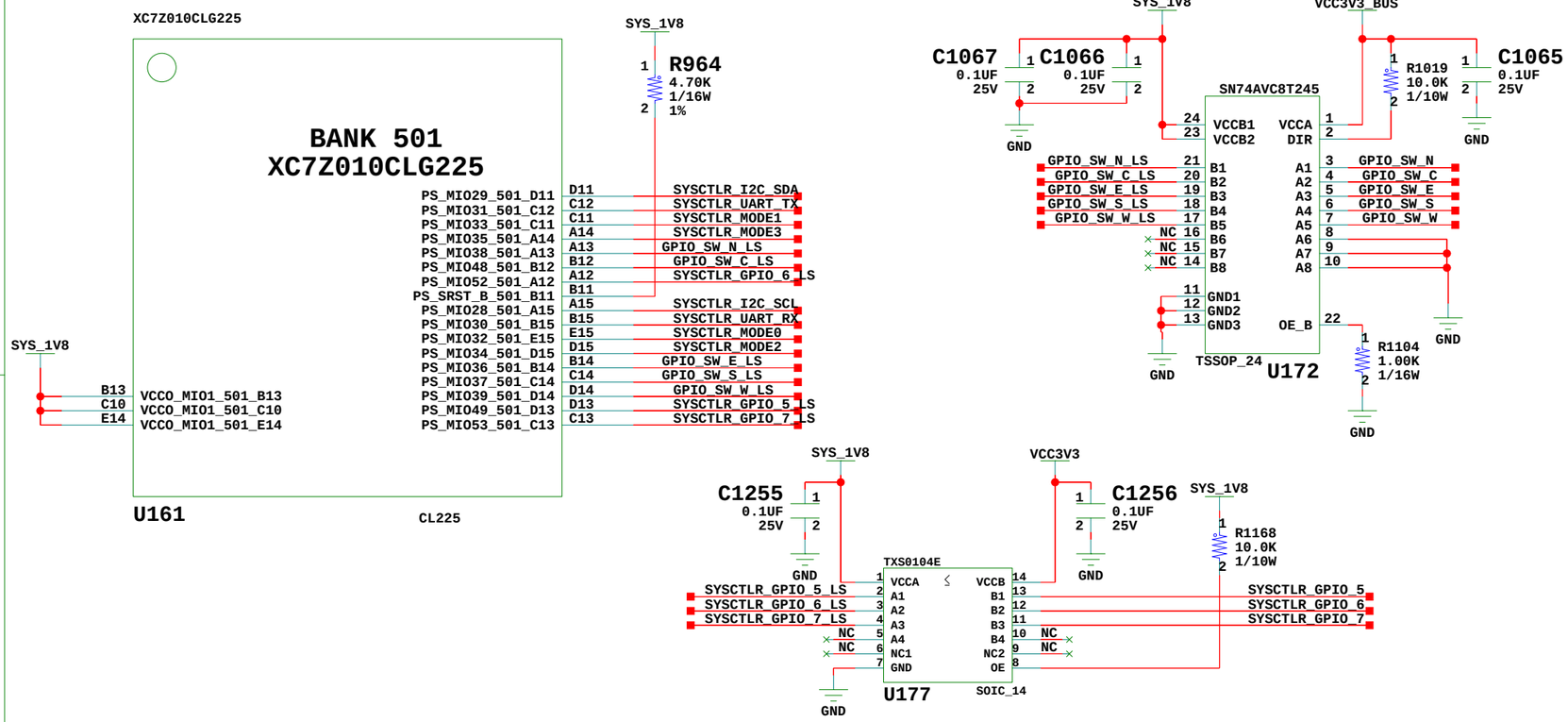
System Controller 1

XILINX

TITLE: System Controller 1 SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 31 OF 60	DRAWN BY: DN







System Controller 2

XILINX

TITLE: System Controller 2 SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 32 OF 60	DRAWN BY: DN

XC7Z010CLG225

BANK VCCPINT
XC7Z010CLG225

VCCPINT_K5 K5
VCCPINT_H5 H5
VCCPINT_G6 G6

SYS_1V0

U161 CL225

XC7Z010CLG225

BANK VCCINT
XC7Z010CLG225

VCCINT_L10 L10
VCCINT_J10 J10
VCCINT_G10 G10
VCCINT_F9 F9
VCCINT_E10 E10

SYS_1V0

U161 CL225

XC7Z010CLG225

BANK GND
XC7Z010CLG225

GND_R9 R9
GND_P2 P2
GND_P12 P12
GND_N5 N5
GND_N15 N15
GND_M8 M8
GND_L5 L5
GND_L11 L11
GND_L1 L1
GND_K7 K7
GND_K4 K4
GND_K14 K14
GND_K10 K10
GND_J9 J9
GND_J5 J5
GND_H6 H6
GND_H10 H10
GND_G5 G5
GND_G3 G3
GND_G13 G13
GND_F10 F10
GND_E9 E9
GND_E7 E7
GND_E5 E5
GND_D2 D2
GND_D12 D12
GND_C5 C5
GND_C15 C15
GND_B8 B8
GND_A11 A11
GND_A1 A1

GND

U161 CL225

XC7Z010CLG225

BANK VCCPAUX
XC7Z010CLG225

VCCPAUX_L6 L6
VCCPAUX_J6 J6

SYS_1V8

U161 CL225

XC7Z010CLG225

BANK VCCAUX
XC7Z010CLG225

VCCAUX_K9 K9
VCCAUX_J8 J8
VCCAUX_H9 H9

SYS_1V8

U161 CL225

XC7Z010CLG225

BANK VCCPLL
XC7Z010CLG225

VCCPLL_F5 F5

SYS_1V8
VCCPLL
FERRITE-120
L78 3A

C1225 0.47UF 10V X5R
C1124 10UF 4V X5R

GND

U161 CL225

VCCINT/VCCBRAM

SYS_1V0

C1130 100UF 4V X6S
C1146 4.7UF 6.3V X5R
C1227 0.47UF 10V X5R
C1226 0.47UF 10V X5R

GND

Bank 0

SYS_1V8

C1172 47UF 6.3V X6S

GND

VCCAUX

SYS_1V8

C1174 47UF 6.3V X6S
C1147 4.7UF 6.3V X5R
C1228 0.47UF 10V X5R

GND

Bank 34

SYS_1V8

C1173 47UF 6.3V X6S
C1148 4.7UF 6.3V X5R
C1149 4.7UF 6.3V X5R
C1229 0.47UF 10V X5R
C1230 0.47UF 10V X5R
C1231 0.47UF 10V X5R
C1232 0.47UF 10V X5R

GND

VCCPINT

SYS_1V0

C1131 100UF 4V X6S
C1151 4.7UF 6.3V X5R
C1234 0.47UF 10V X5R
C1235 0.47UF 10V X5R
C1236 0.47UF 10V X5R

GND

VCCPAUX

SYS_1V8

C1132 100UF 4V X6S
C1150 4.7UF 6.3V X5R
C1233 0.47UF 10V X5R

GND

VCCO_MIO0

SYS_1V8

C1133 100UF 4V X6S
C1152 4.7UF 6.3V X5R
C1237 0.47UF 10V X5R

GND

VCCO_MIO1

SYS_1V8

C1134 100UF 4V X6S
C1153 4.7UF 6.3V X5R
C1238 0.47UF 10V X5R

GND

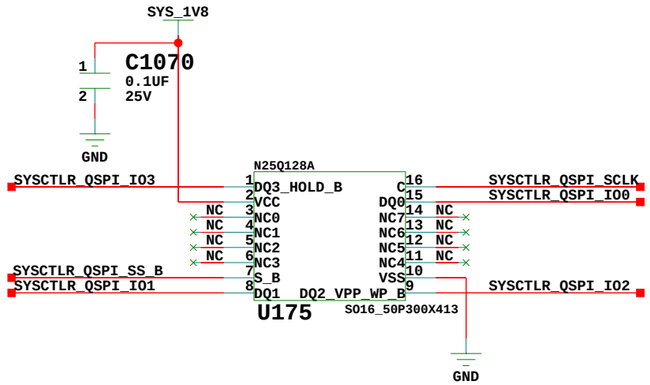
System Controller 3

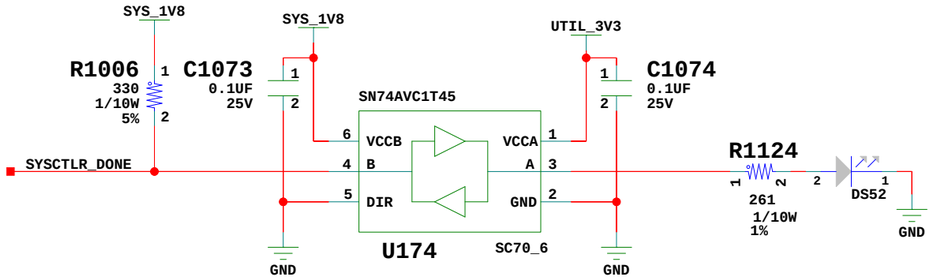
XILINX

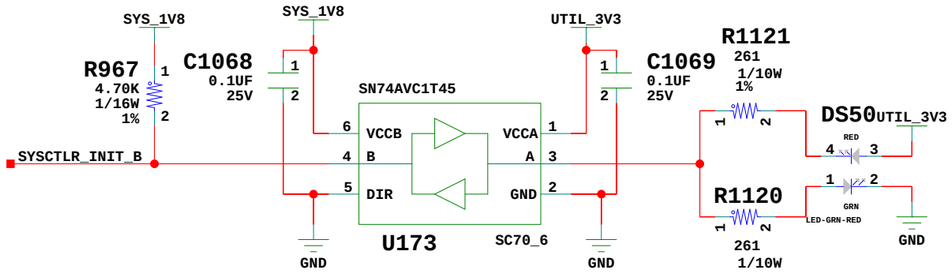
TITLE: System Controller 3
SCHEM, ROHS COMPLIANT
HW-U1-KCU116_REV1_0

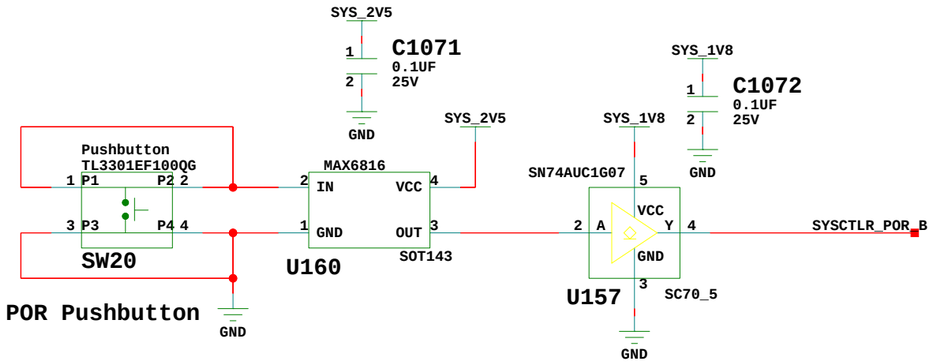
ASSY P/N: 0432019
PCB P/N: 1280924
SCH P/N: 0381757
TEST P/N: TSSXXXX

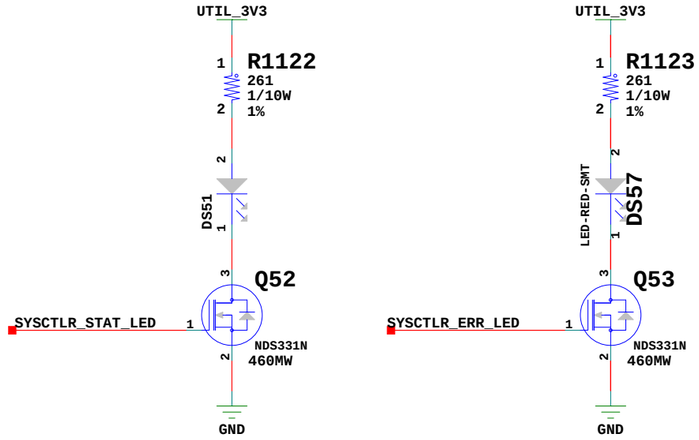
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 33 OF 60	DRAWN BY: DN

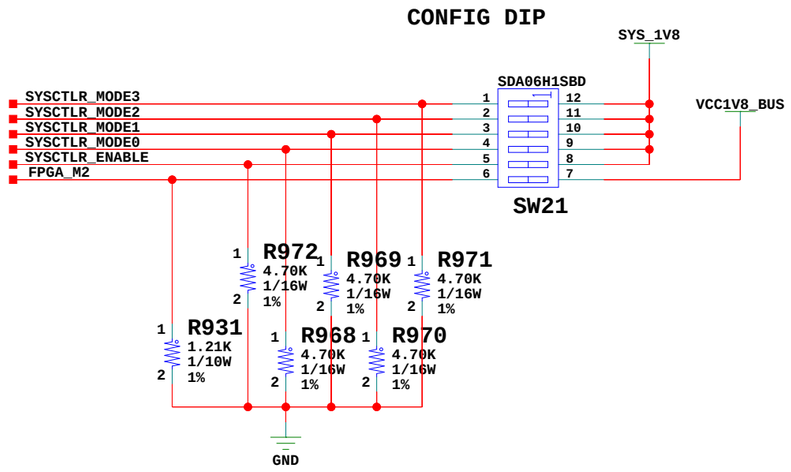








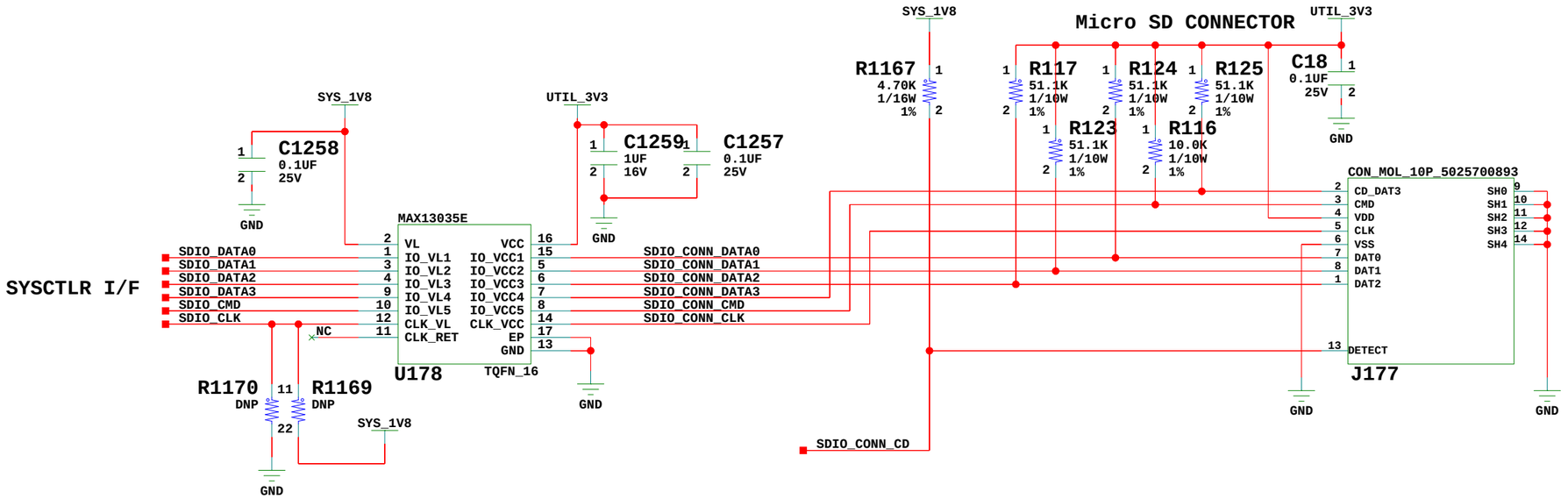




System Controller 4 - Config DIP

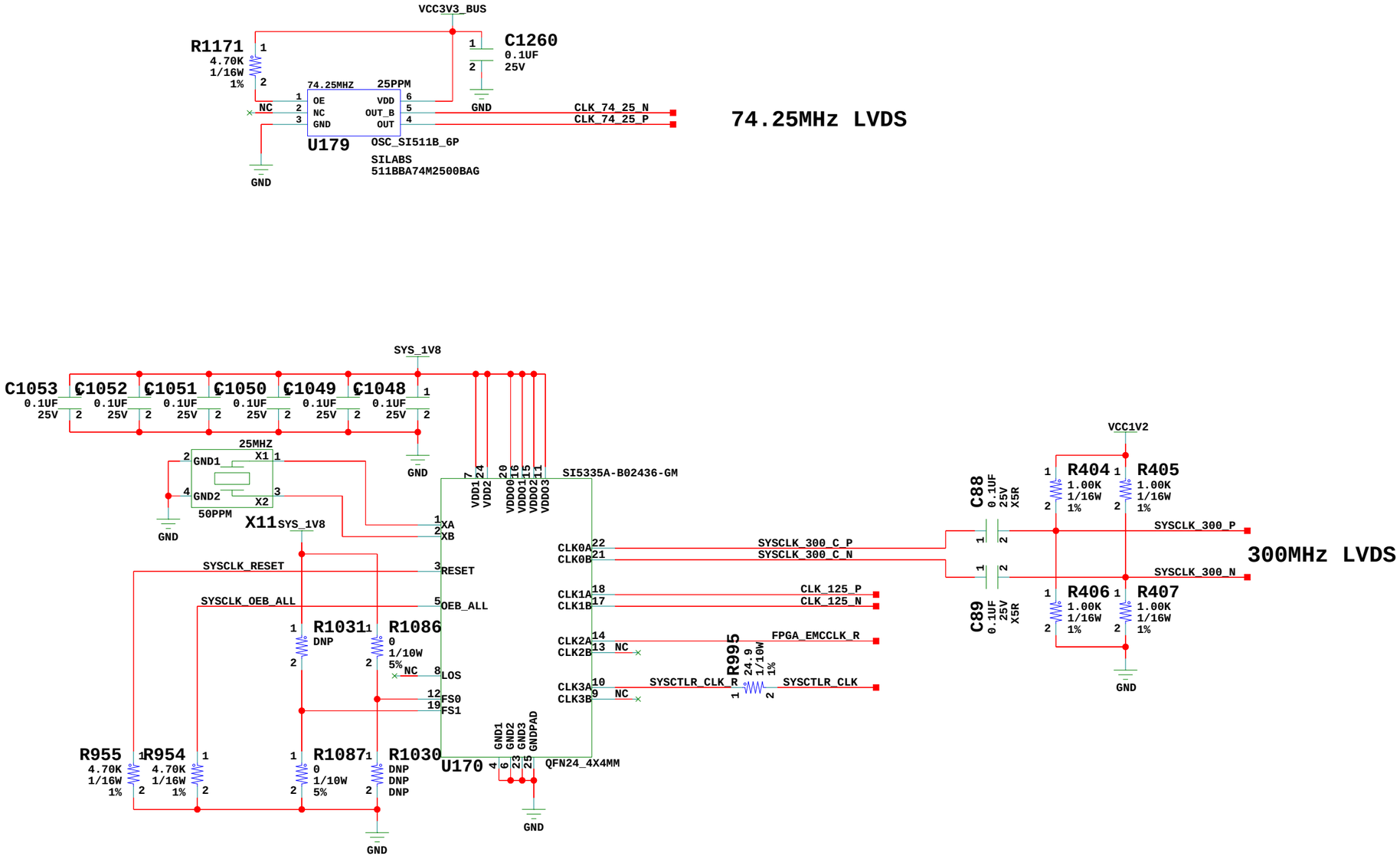
XILINX

TITLE: System Controller 4 - Config DIP SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 34 OF 60	DRAWN BY: DN



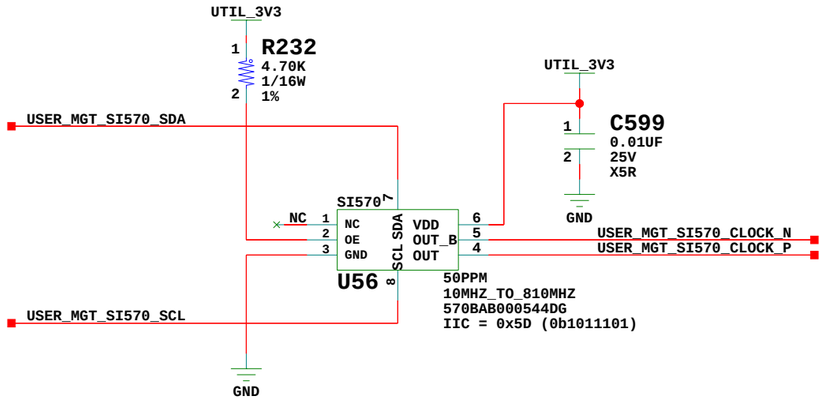
Micro SD Card Connector

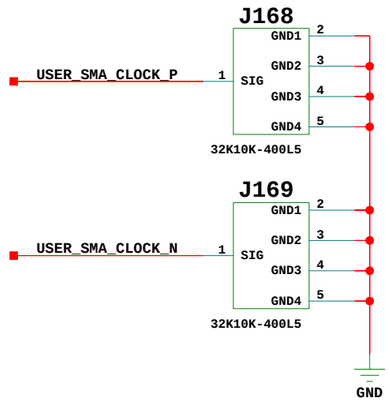
TITLE: Micro SD Card Connector SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 35 OF 60	DRAWN BY: DN

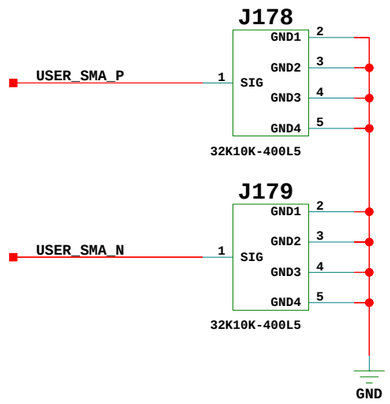


Fixed Clocks

TITLE: Fixed Clocks SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 36 OF 60	DRAWN BY: DN

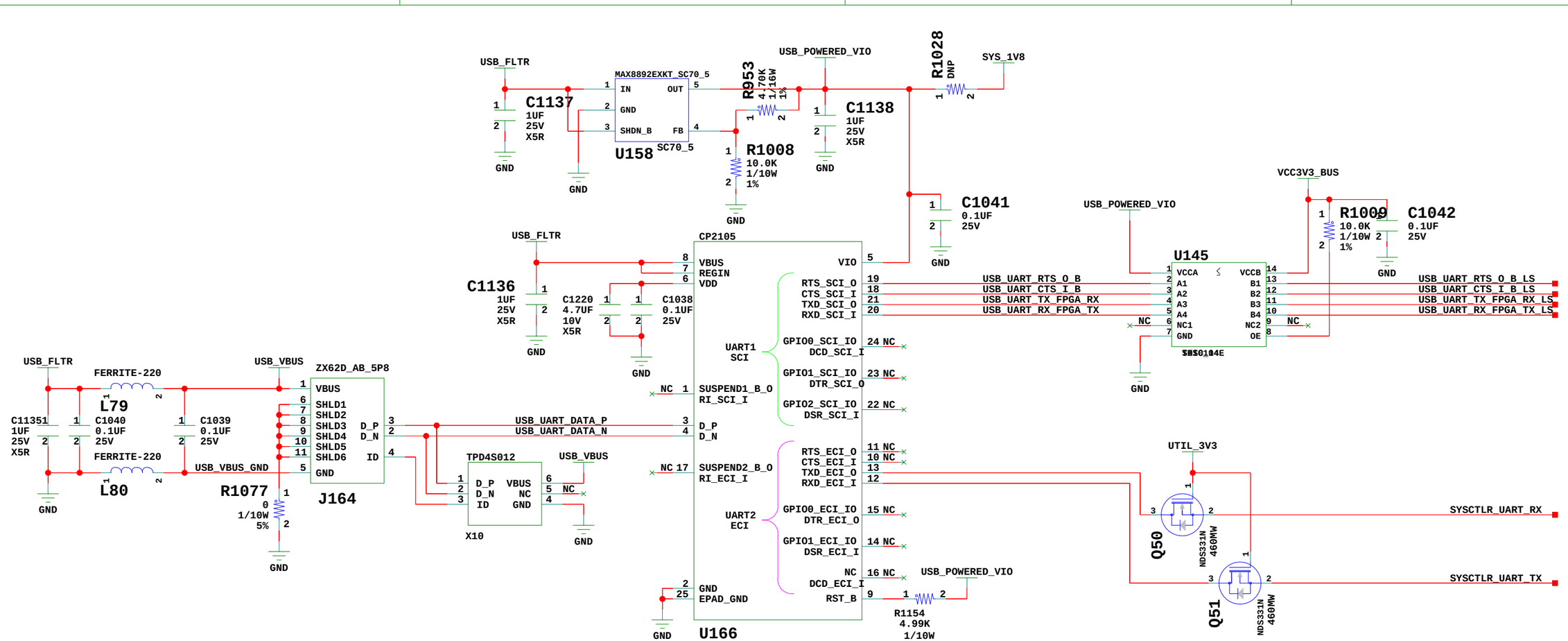


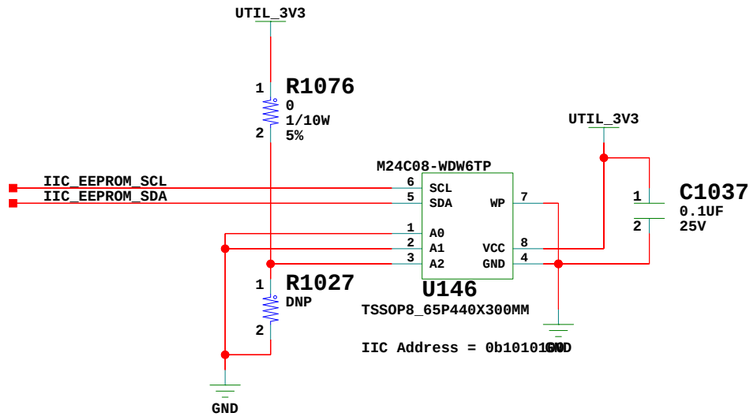




MGT Programmable Clock - SMAs

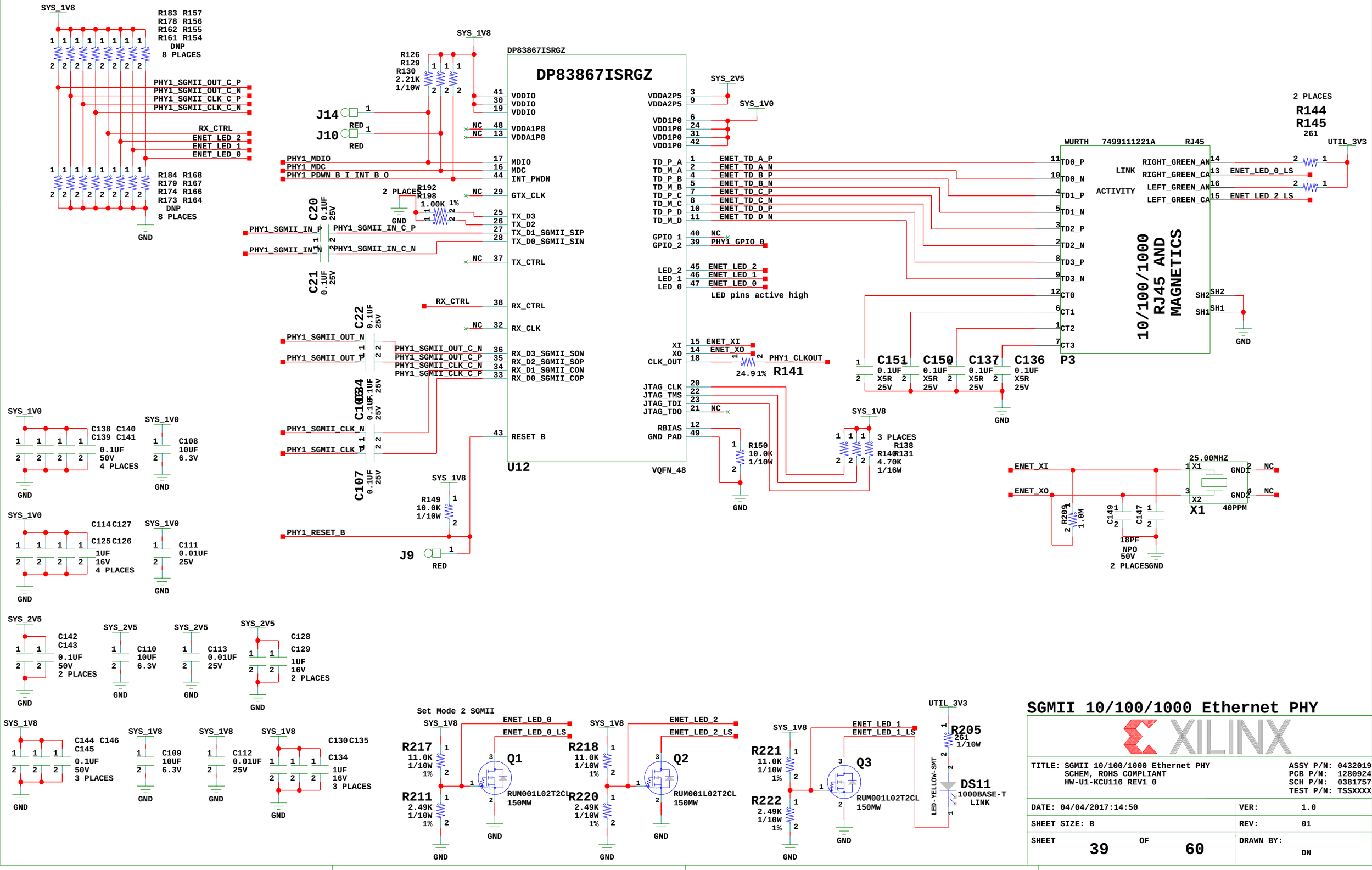
TITLE: MGT Programmable Clock - SMAs SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 37 OF 60	DRAWN BY: DN





Dual USB UART - EEPROM

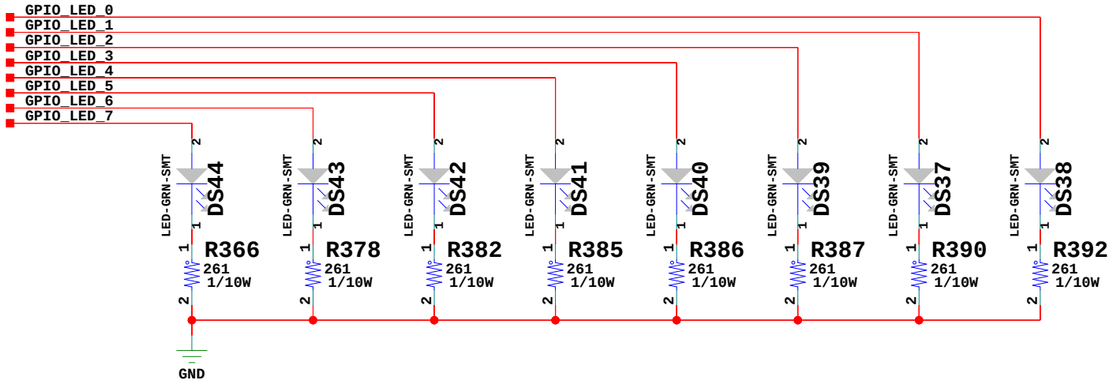
TITLE: Dual USB UART - EEPROM SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 38 OF 60	DRAWN BY: DN

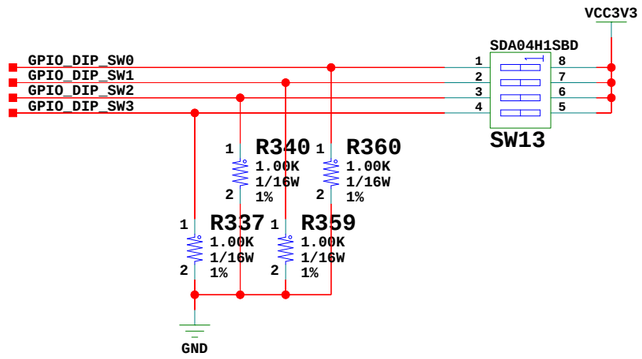


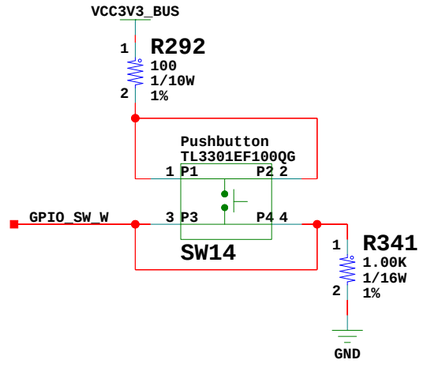
SGMII 10/100/1000 Ethernet PHY

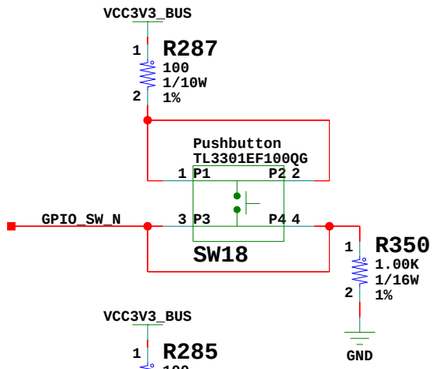
TITLE: SGMII 10/100/1000 Ethernet PHY SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/04/2017:14:50	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 39 OF 60	DRAWN BY: DN

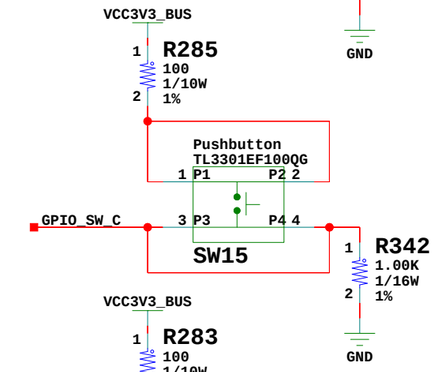
LEDs near top right edge

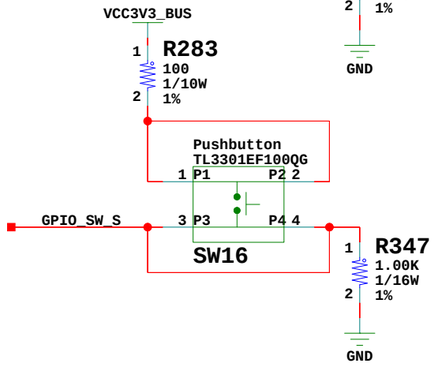


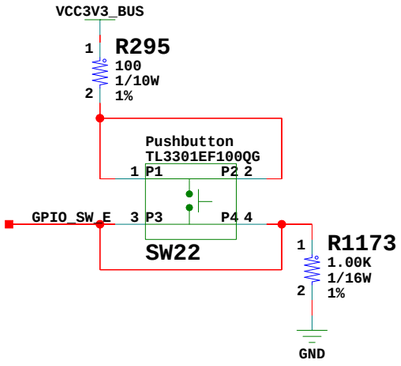


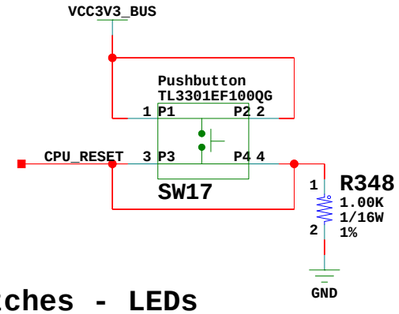










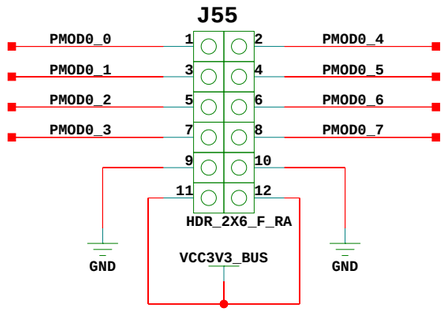


Buttons - Switches - LEDs

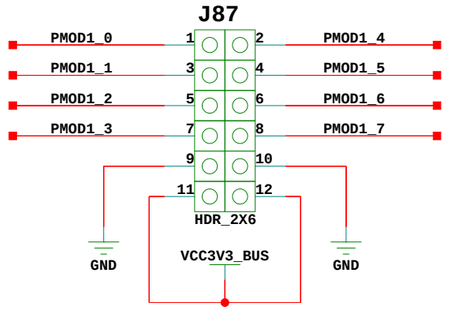
XILINX

TITLE: Buttons - Switches - LEDs SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 40 OF 60	DRAWN BY: DN

RT-ANGLE RECEPTACLE



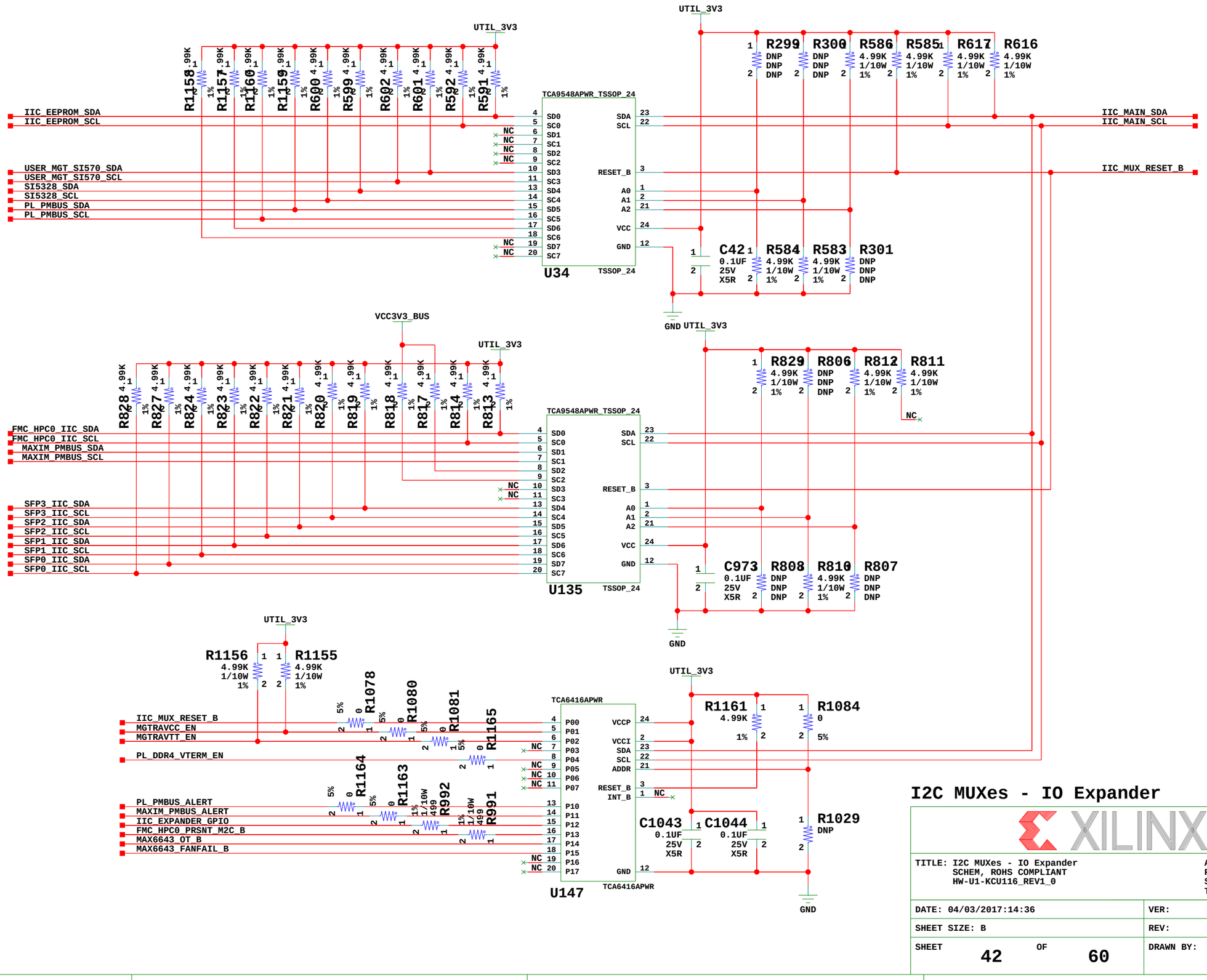
VERTICAL MALE PIN HEADER



PMODs

XILINX

TITLE: PMODs SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 41 OF 60	DRAWN BY: DN

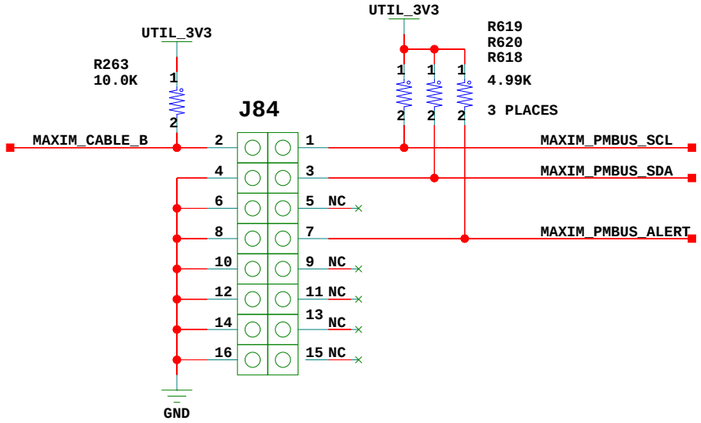


I2C MUXes - IO Expander

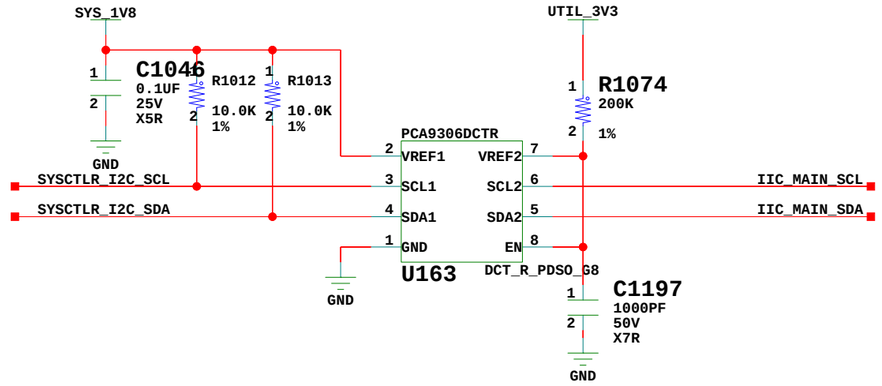
XILINX

TITLE: I2C MUXes - IO Expander SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:36	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 42 OF 60	DRAWN BY: DN

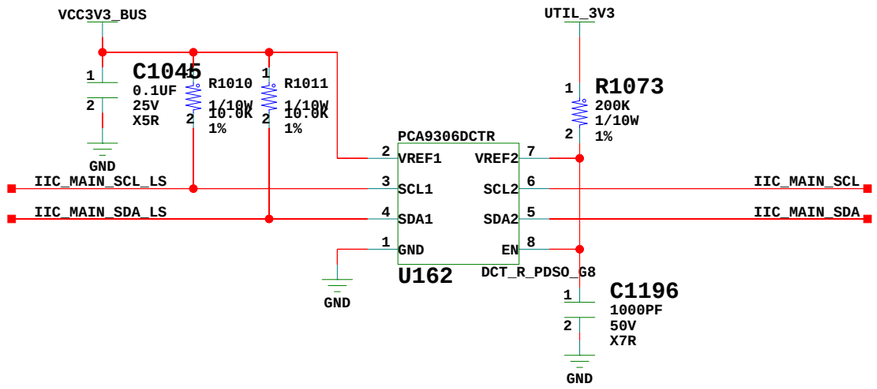
MAXIM PMBUS PROGRAMMING CABLE



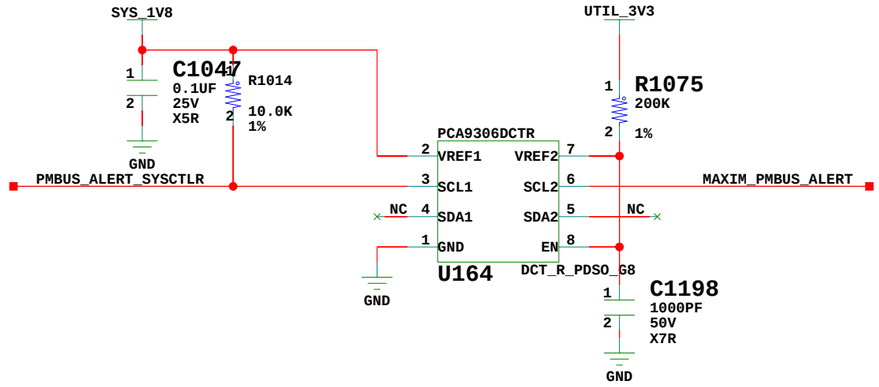
SYSCTLR I2C Level Shifter



I2C MAIN Level Shifter



SYSCTLR I2C Level Shifter



PMBUS Header - I2C Level Shifters

TITLE: PMBUS Header - I2C Level Shifters SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 43 OF 60	DRAWN BY: DN

6-PIN MINI-FIT AC ADAPTER (BRICK)

J52
12V 1
12V 4
COM 2
12V 5
COM 3
COM 6
INPUT_GND

VCC12_P
R448 2.00K 1/16W
C382 10UF 25V X5R
Q7 SI7157DP
R269 10.0K 1/10W
C657 1UF 16V
C533 1UF 25V X5R
U25 50MOHM
INPUT_GND
GND
DNP J28
VCC12_SW
C922 330UF 16V ELEC
DS2 LED-GRN-SMT MASTER POWER
R268 2.00K 1/16W 1%
GND

R412 1.00K 1/16W
SW1 ON OFF SH1 SH2
MASTER_SW_12V
Q4 BSS138 360MW
INPUT_GND

UTIL_3V3
R657 10.0K 1/10W
R650 3.32K 1/10W 1%
MAX16052
EN VCC OUT CDELAY GND IN
VCC12_P
C923 0.1UF 25V X5R
R711 4.99K 1/10W 1%
REG_EN
C931 0.01UF 25V X5R
R649 1.50K 1/10W 1%
R710 1.00K 1/16W 1%
J153 HDR_1X2
U103
C932 DNP DNP DNP
INPUT_GND

SYS_2V5 SYS_1V8 SYS_1V0 UTIL_3V3
MAX16050
R1018 R1015 R1016 R1017 10.0K 1/10W
DISC1 DISC2 DISC3 DISC4 NC
VCC12_P
C1054 0.1UF 25V X5R
EN SET1 SET2 SET3 SET4 SEQ3 SEQ2 SEQ1 SHDN_B EN_HOLD_B ABP EPAD GND
OUT1 OUT2 OUT3 OUT4 CP_OUT REM OV_OUT_B FAULT_B RESET_B TIMEOUT DELAY
SYS_1V0_POR_B
SYS_1V8_POR_B
SYS_2V5_POR_B
SYSCTLR_POR_B
R948 3.32K 1/10W 1%
R951 5.9K 1/10W
R1056 20K 1/10W
R952 4.32K 1/10W
C1169 1UF 16V
C1175 C1176 DNP DNP 2 PLACES
U169 TQFN_28_EP
GND

DNP J29
DNP J30
DNP J31
DNP J32
DNP J33
DNP J34
GND

GND Test points

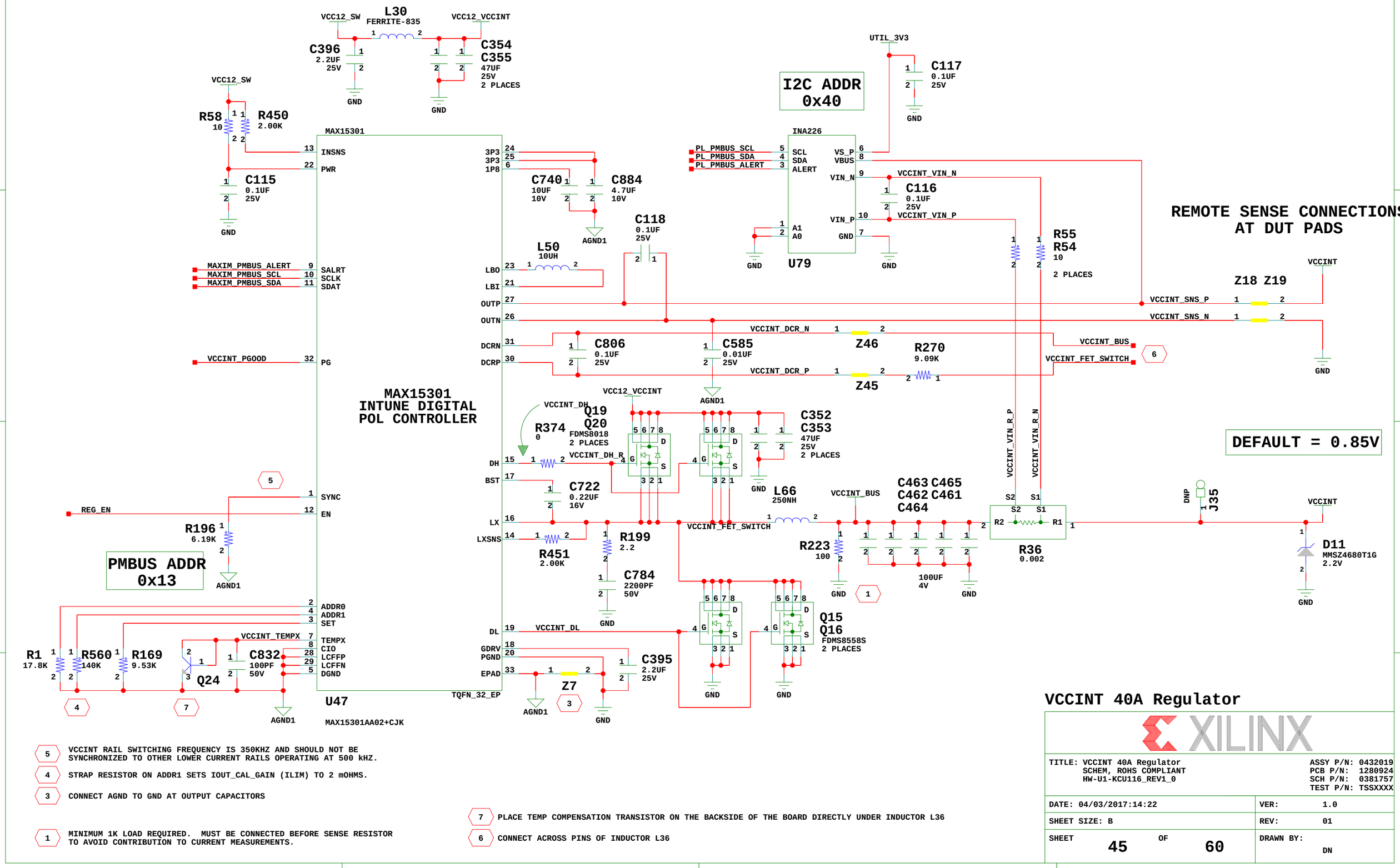
2 Maxim Regulator Inhibit Jumper

1 DELAY TIME AND RESET TIMEOUT PERIOD SET TO 11mS

12V Power Connectors Switch

XILINX

TITLE: 12V Power Connectors Switch SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 44 OF 60	DRAWN BY: DN



5 VCCINT RAIL SWITCHING FREQUENCY IS 350KHZ AND SHOULD NOT BE SYNCHRONIZED TO OTHER LOWER CURRENT RAILS OPERATING AT 500 kHZ.

4 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS.

3 CONNECT AGND TO GND AT OUTPUT CAPACITORS

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

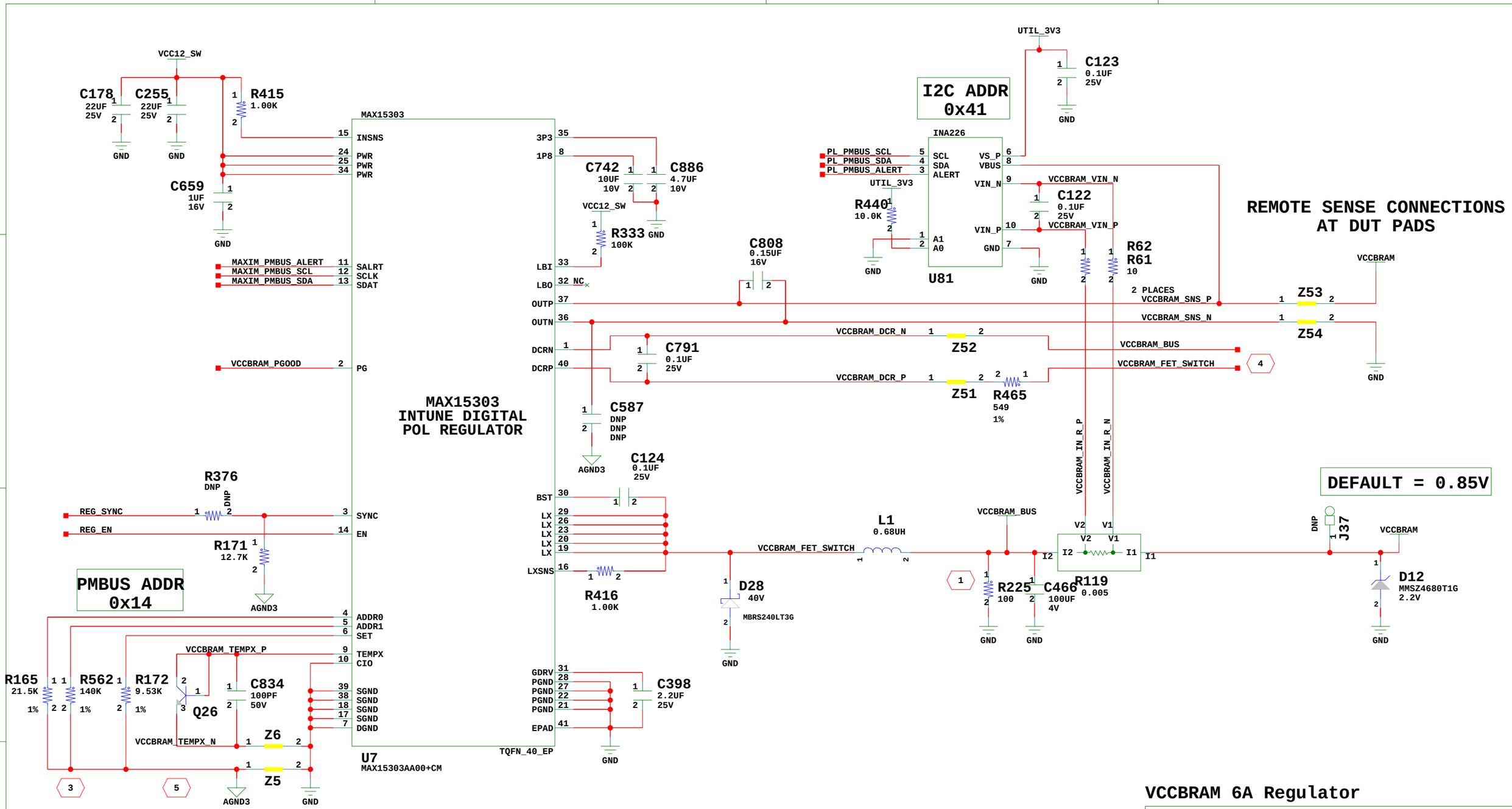
7 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER INDUCTOR L36

6 CONNECT ACROSS PINS OF INDUCTOR L36

VCCINT 40A Regulator

XILINX

TITLE: VCCINT 40A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 45 OF 60	DRAWN BY: DN



5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

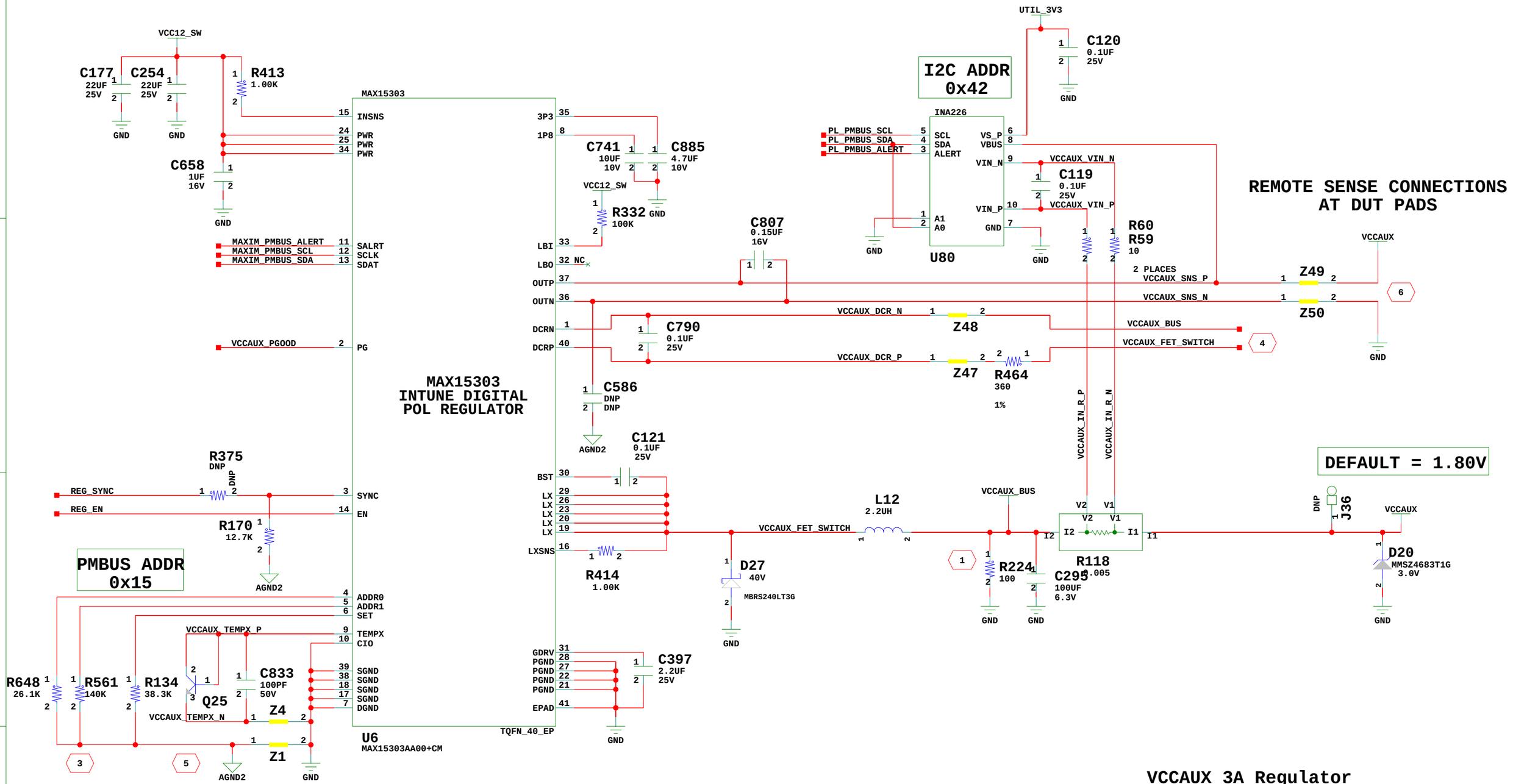
2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

VCCBRAM 6A Regulator

XILINX

TITLE: VCCBRAM 6A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 46 OF 60	DRAWN BY: DN

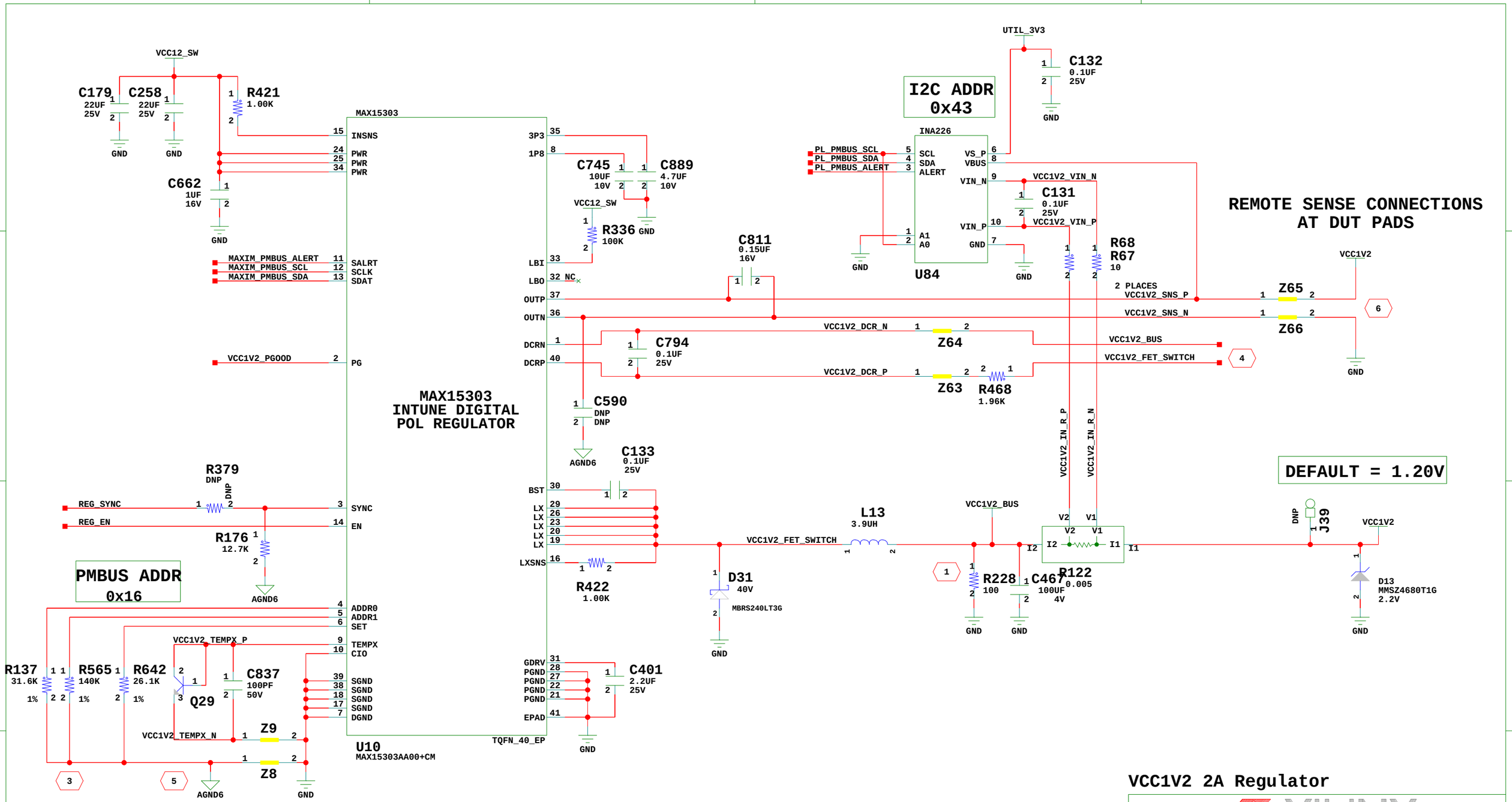


6. TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE VCCAUX PLANE.
5. PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR
4. CONNECT ACROSS PINS OF OUTPUT INDUCTOR
3. STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.
2. HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.
1. MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

VCCAUX 3A Regulator

XILINX

TITLE: VCCAUX 3A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 47 OF 60	DRAWN BY: DN



6 TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE VCC1V2 PLANE.

5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

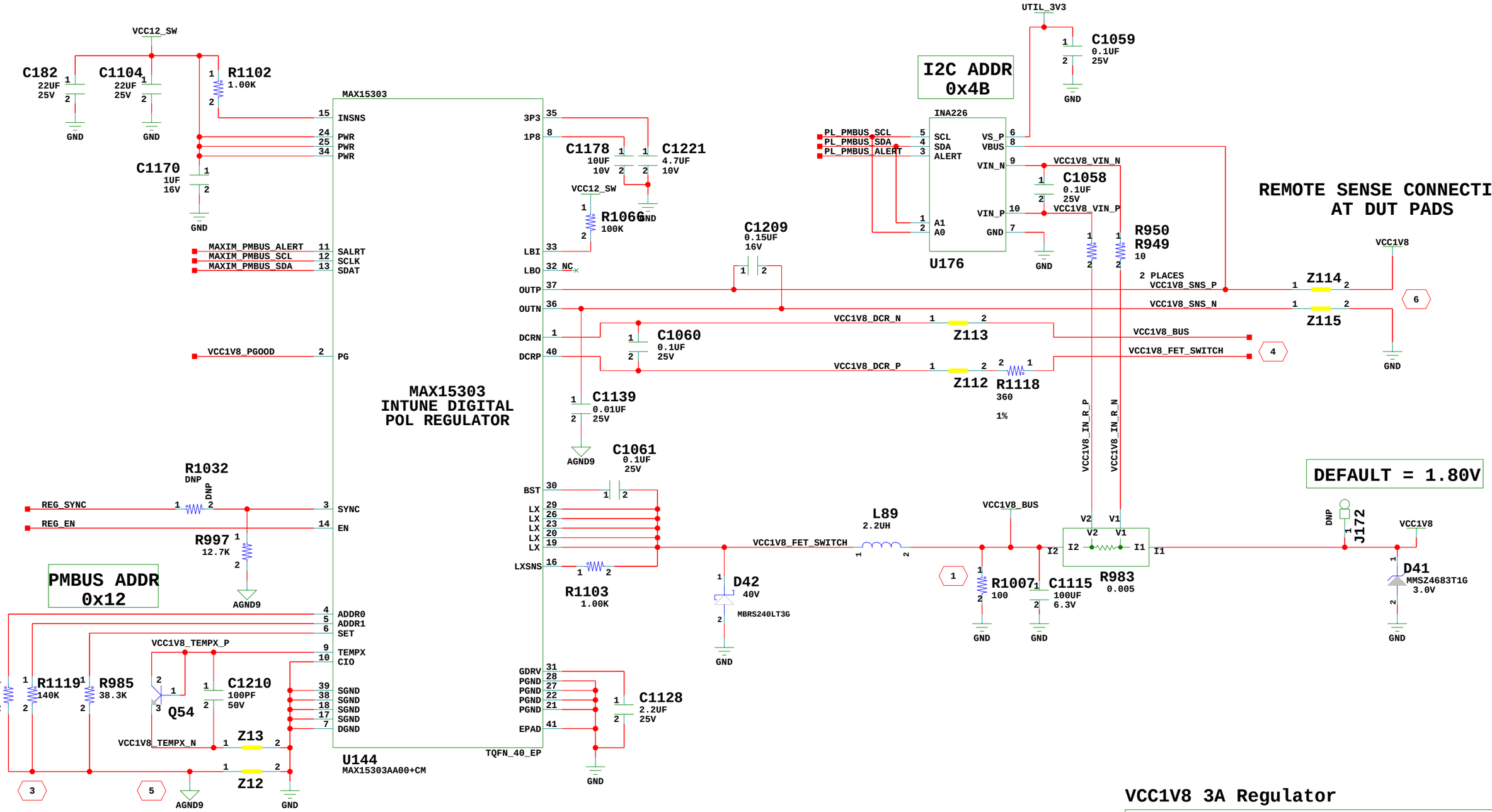
2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

VCC1V2 2A Regulator

XILINX

TITLE: VCC1V2 2A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 48 OF 60	DRAWN BY: DN



6 TWO VOLTAGE SENSE POINTS ARE REQUIRED DUE TO THE SHAPE AND SIZE OF THE VCC1V8 PLANE.

5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

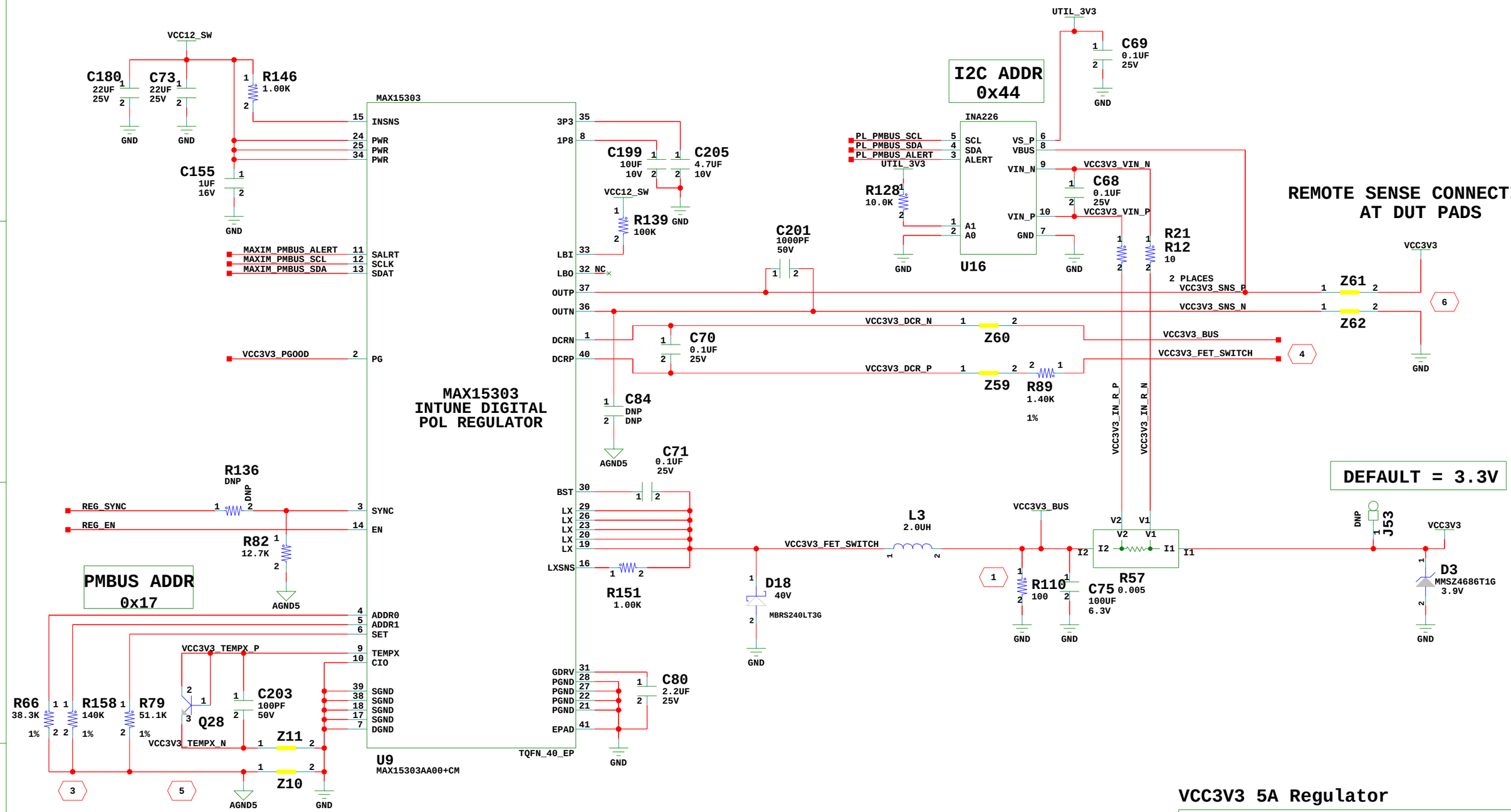
2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

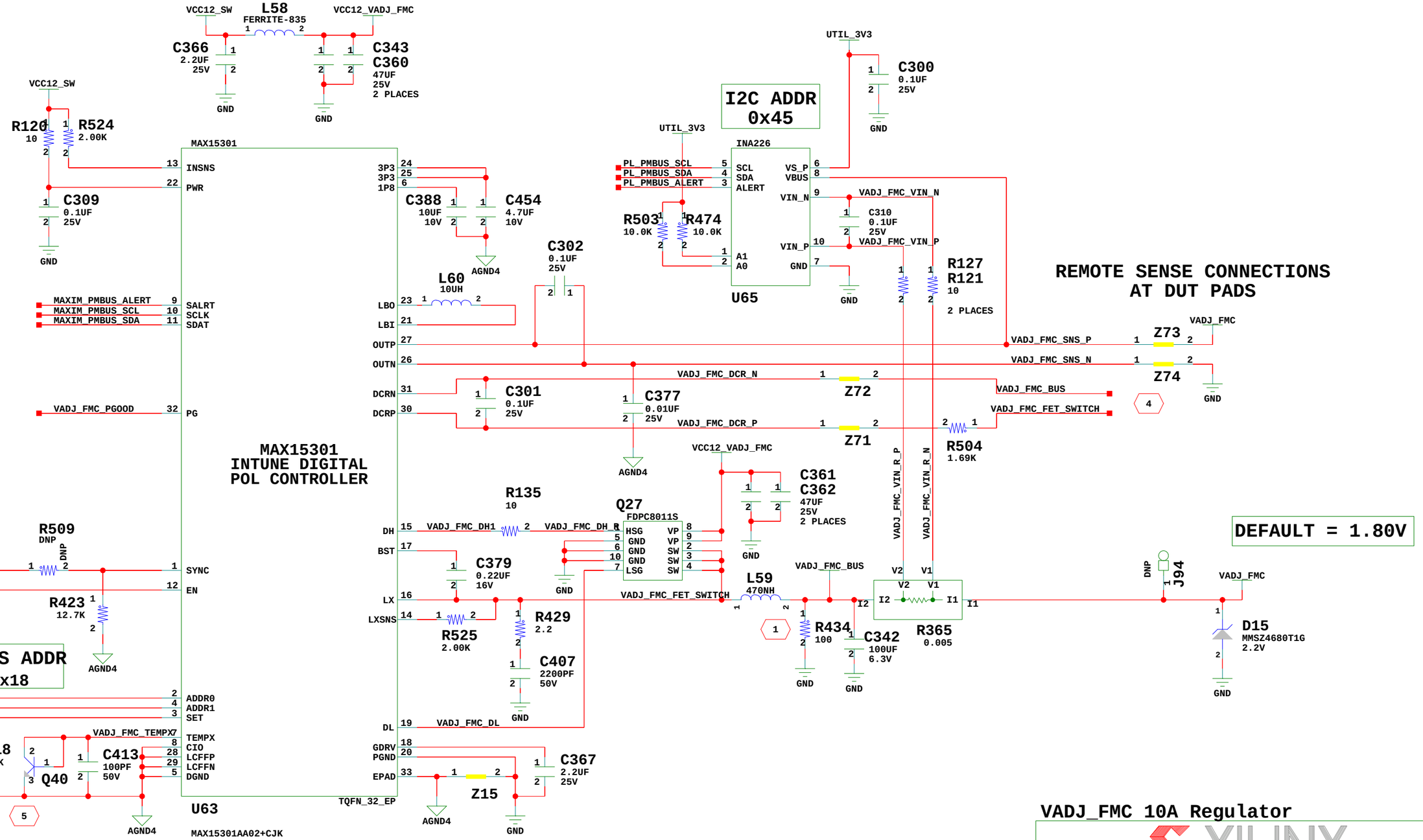
VCC1V8 3A Regulator

XILINX

TITLE: VCC1V8 3A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/04/2017:14:52	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 49 OF 60	DRAWN BY: DN



TITLE: VCC3V3 5A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 50 OF 60	DRAWN BY: DN



5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER INDUCTOR L3

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

3 STRAP RESISTOR ON ADDR1 SETS IOUT_CAL_GAIN (ILIM) TO 2 mOHMS. THIS PARAMETER MUST BE OVERRIDDEN TO 5 mOHMS (MATCHING THE CURRENT SENSE RESISTOR) WHEN THE CONTROLLER IS CONFIGURED.

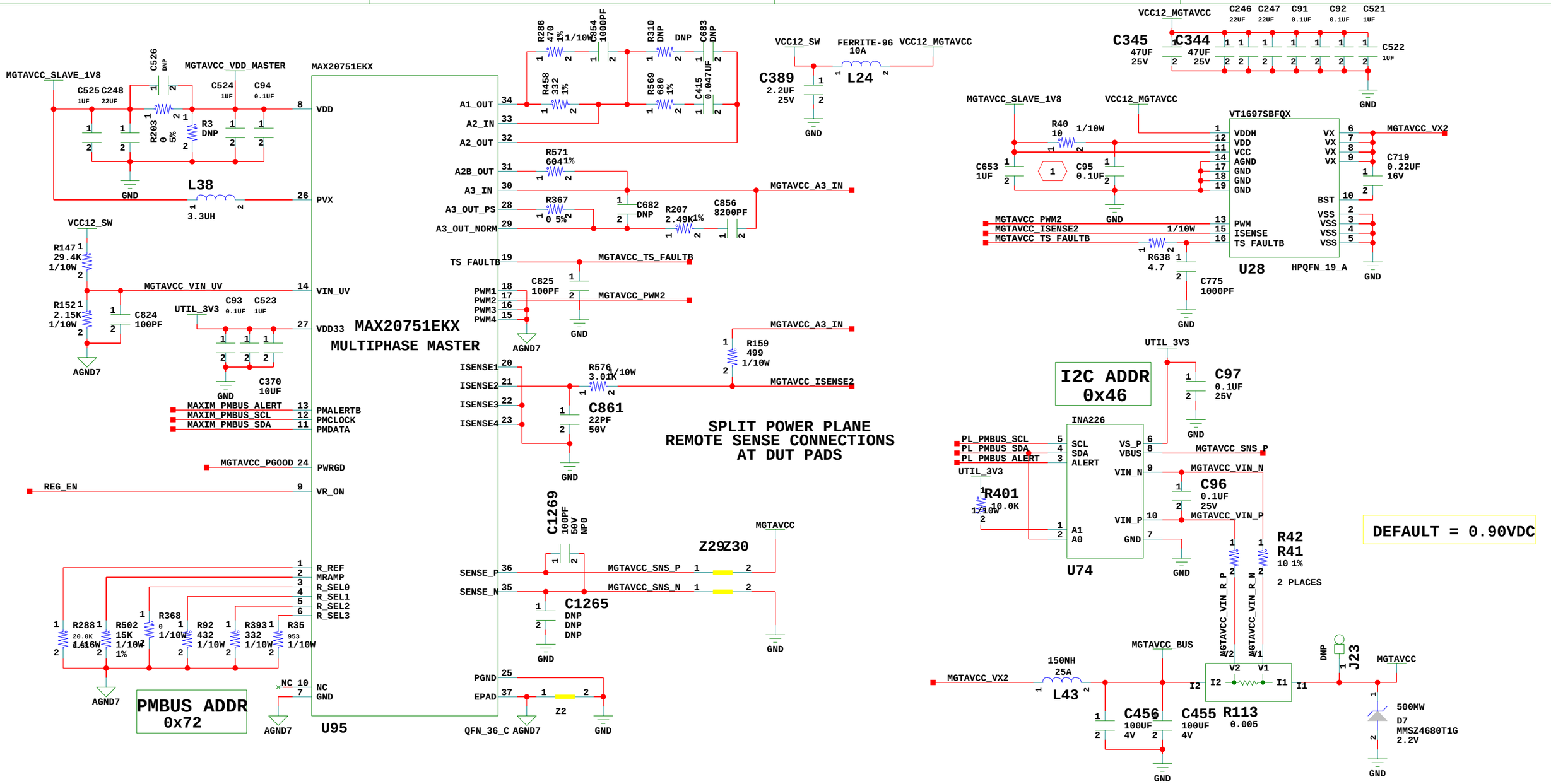
2 HEADER IS FOR SCOPE ATTACHMENT TO OBSERVE STEP LOAD RESPONSE.

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

VADJ_FMC 10A Regulator

XILINX

TITLE: VADJ_FMC 10A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 51 OF 60	DRAWN BY: DN



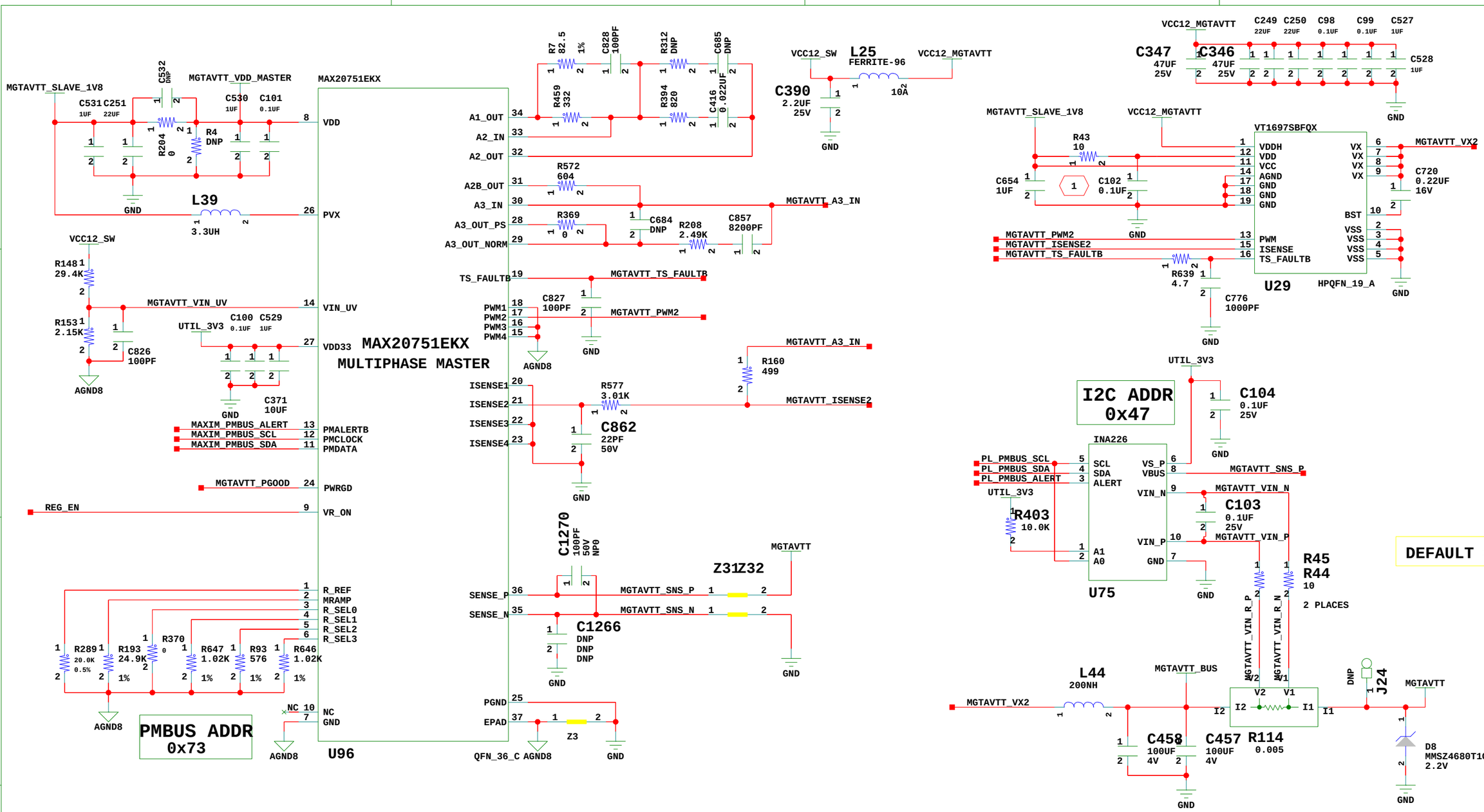
NOTES

1. Capacitors should be placed as close as possible to Pin12 and 14

MGTAVCC 6A Regulator

XILINX

TITLE: MGTAVCC 6A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 52 OF 60	DRAWN BY: DN



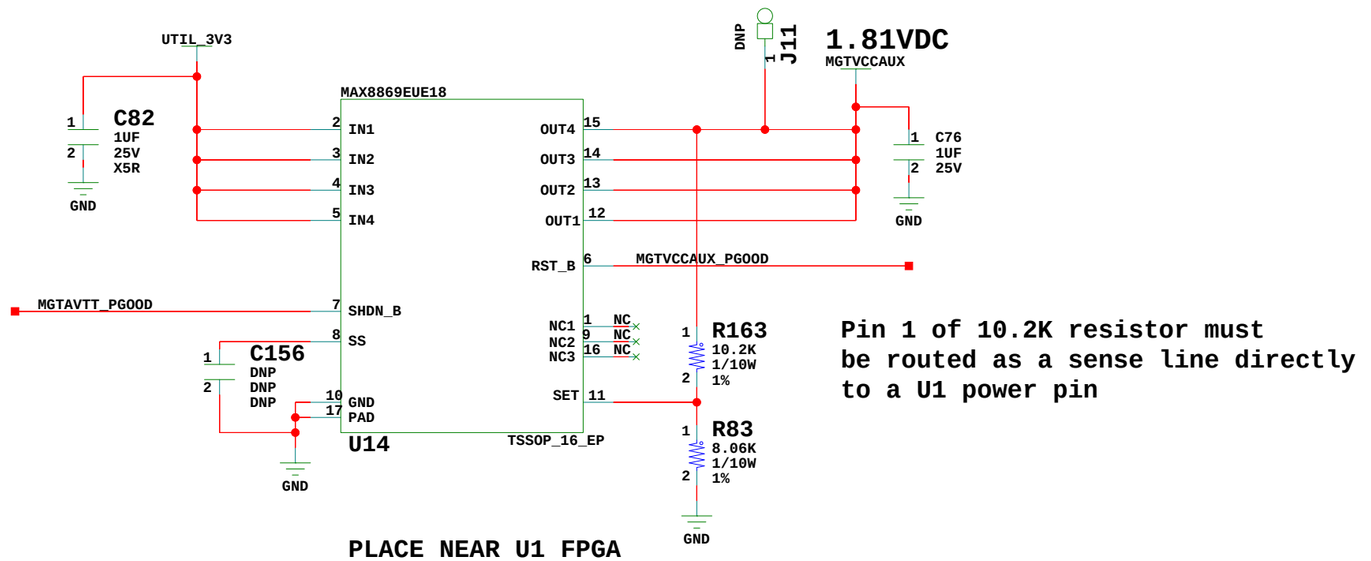
NOTES

1. Capacitors should be placed as close as possible to Pin12 and 14

MGTAVTT 6A Regulator

XILINX

TITLE: MGTAVTT 6A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:15:24	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 53 OF 60	DRAWN BY: DN



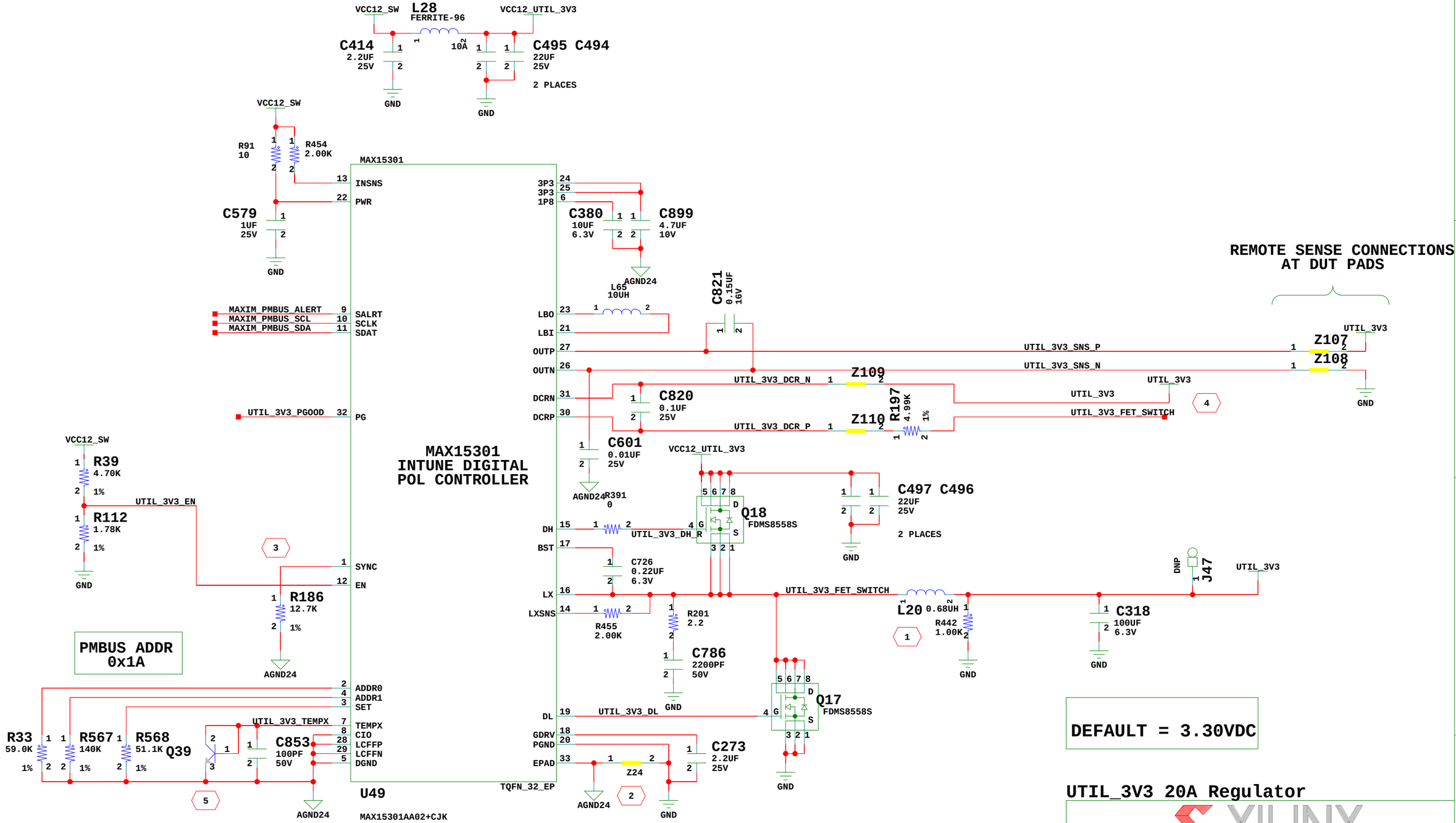
Pin 1 of 10.2K resistor must be routed as a sense line directly to a U1 power pin

PLACE NEAR U1 FPGA

MGTVCCAUX 1A Regulator

XILINX

TITLE: MGTVCCAUX 1A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 54 OF 60	DRAWN BY: DN



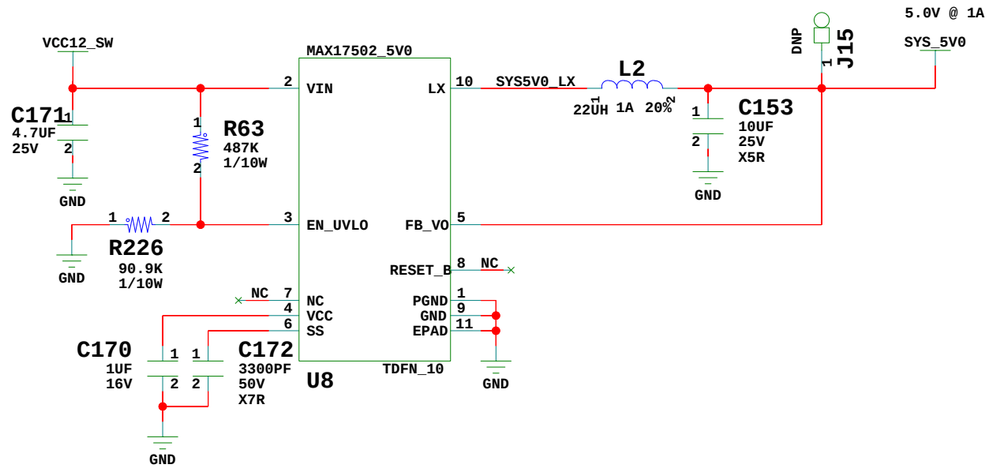
3 UTIL_3V3 RAIL SWITCHING FREQUENCY IS 400kHz AND SHOULD NOT BE SYNCHRONIZED TO OTHER LOWER CURRENT RAILS OPERATING AT 600 kHZ.

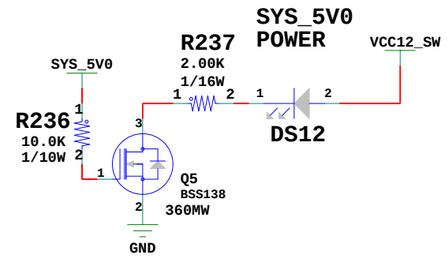
2 CONNECT AGND TO GND AT OUTPUT CAPACITORS

1 MINIMUM 1K LOAD REQUIRED. MUST BE CONNECTED BEFORE SENSE RESISTOR TO AVOID CONTRIBUTION TO CURRENT MEASUREMENTS.

5 PLACE TEMP COMPENSATION TRANSISTOR ON THE BACKSIDE OF THE BOARD DIRECTLY UNDER OUTPUT INDUCTOR

4 CONNECT ACROSS PINS OF OUTPUT INDUCTOR

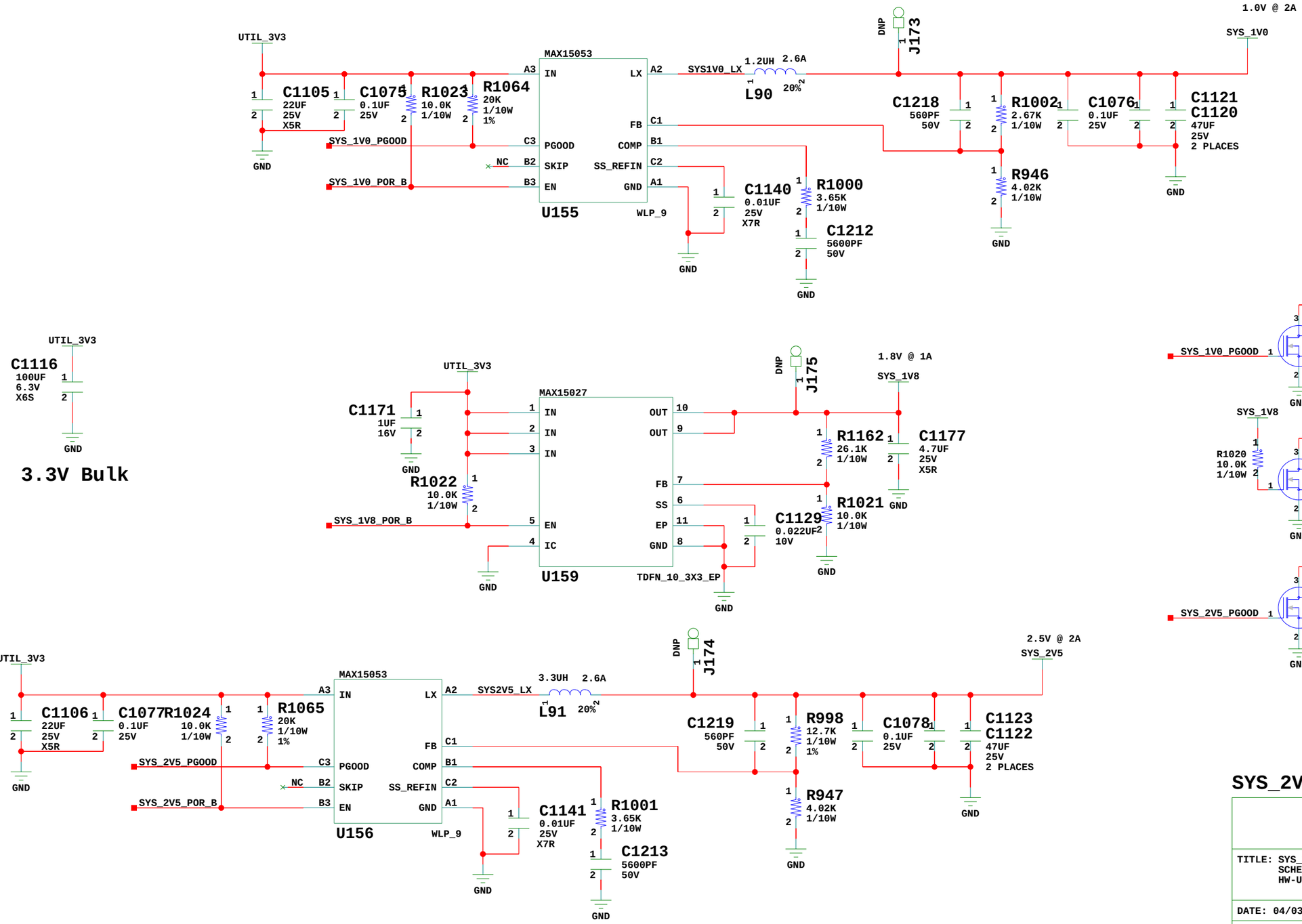




SYS_5V0 1A Regulator

XILINX

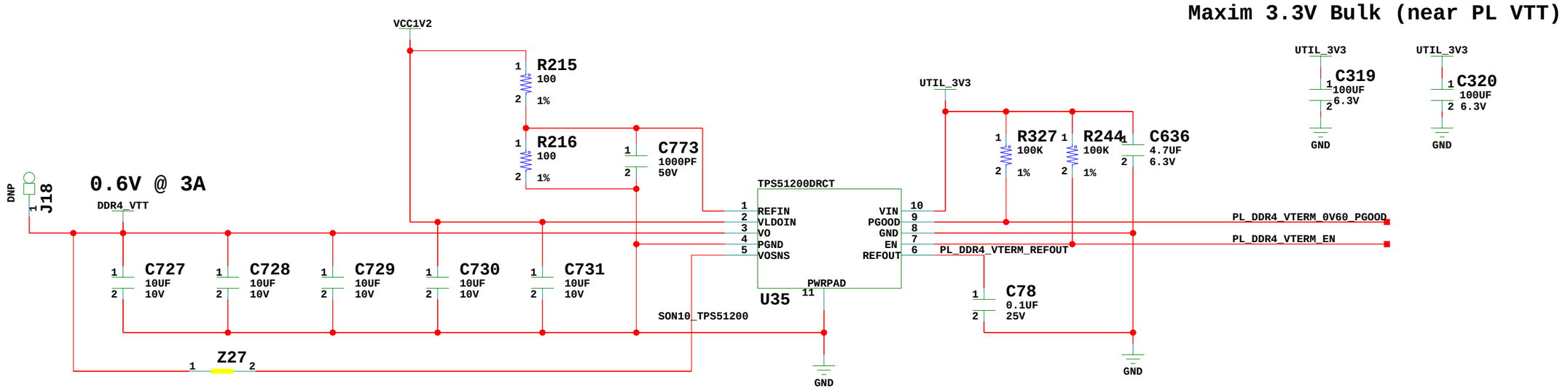
TITLE: SYS_5V0 1A Regulator SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 56 OF 60	DRAWN BY: DN



SYS_2V5 SYS_1V8 SYS_1V0 Regulators

XILINX

TITLE: SYS_2V5 SYS_1V8 SYS_1V0 Regulators SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 57 OF 60	DRAWN BY: DN

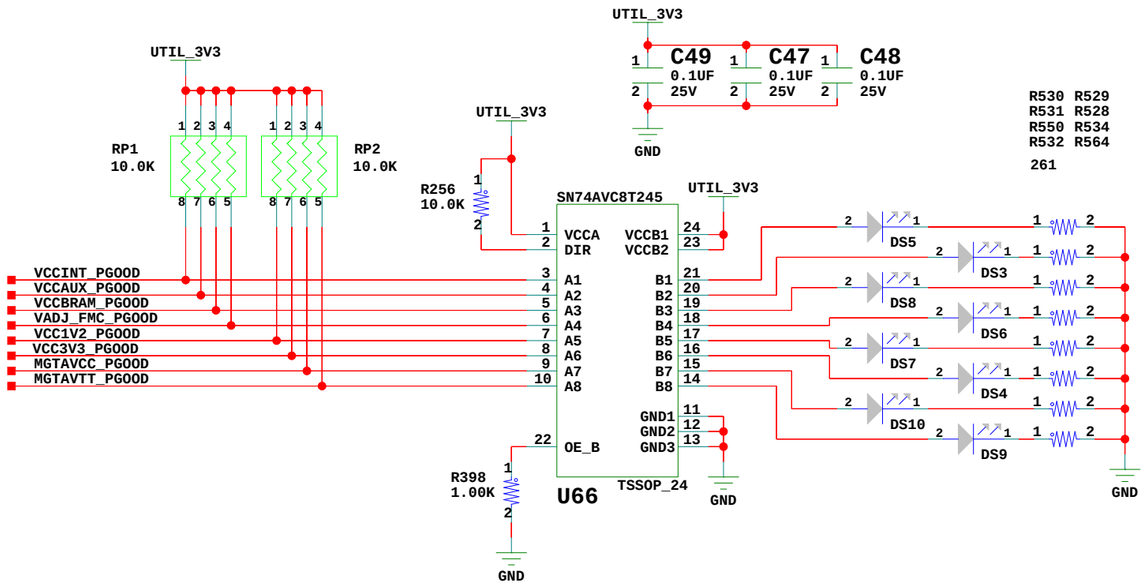


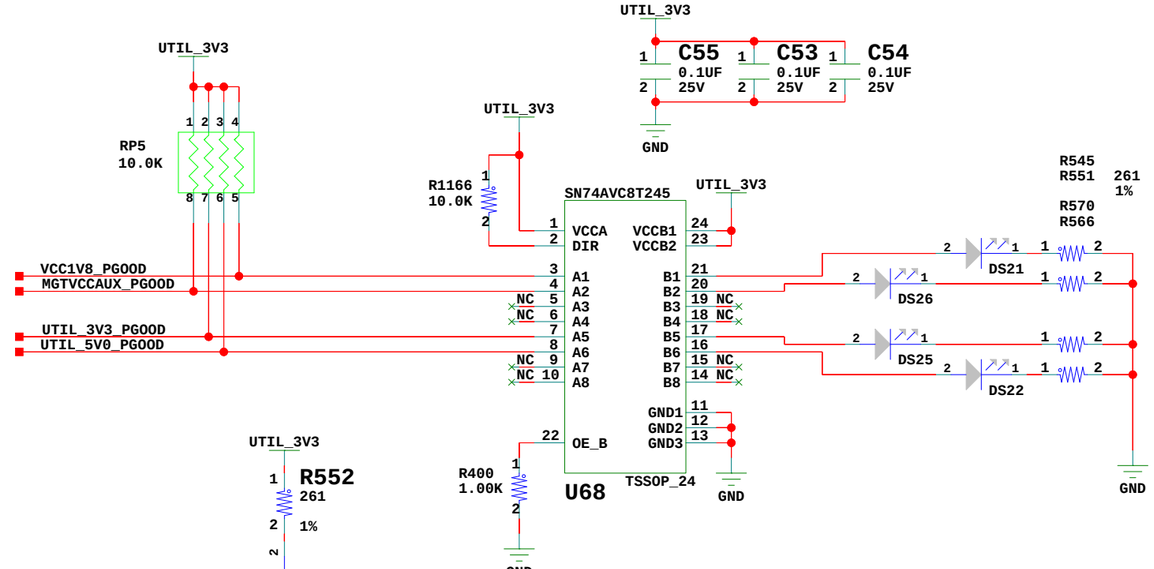
Place sense near DDR4 components

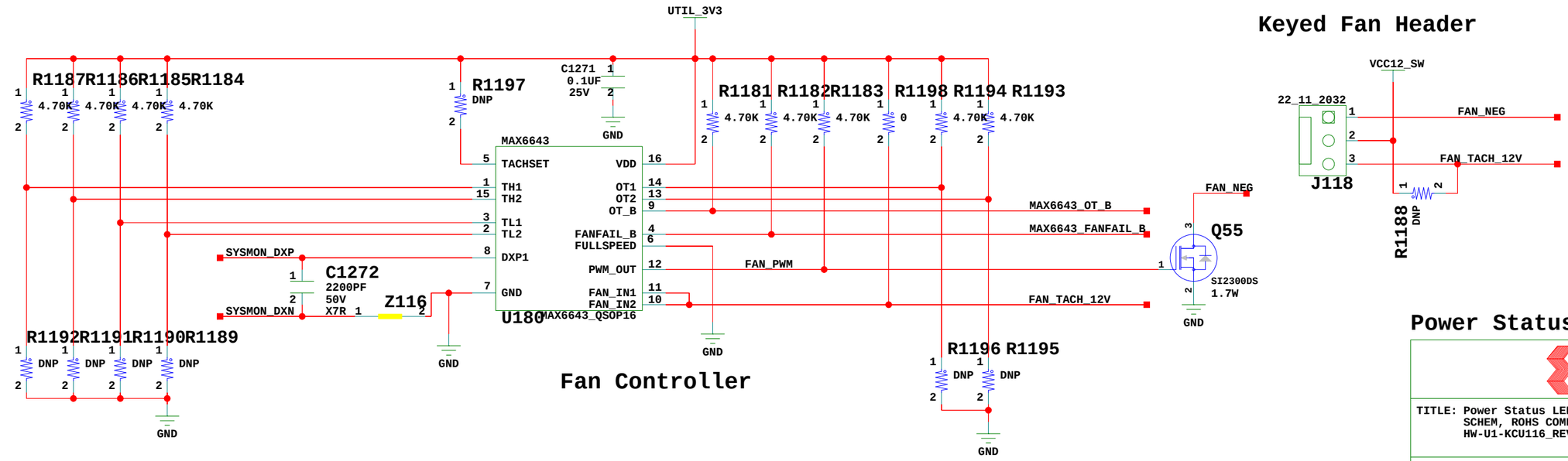
DDR4 Termination Supply

XILINX

TITLE: DDR4 Termination Supply SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 58 OF 60	DRAWN BY: DN







Fan Controller

Power Status LEDs - Fan Ctrl

XILINX

TITLE: Power Status LEDs - Fan Ctrl SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:15:22	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 59 OF 60	DRAWN BY: DN

MS01
STANDOFF_0P625

MW1
WASHER_FLAT_4

MRB1
RUBBER_BUMPER

MS1
MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MS2
MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MH_125_250
MH1
GND

MS02
STANDOFF_0P625

MW2
WASHER_FLAT_4

MRB2
RUBBER_BUMPER

MS3
MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MS4
MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MH_125_250
MH2
GND

HS1
12V Fan / Heatsink
RADIAN XLX042_A1

MS03
STANDOFF_0P625

MW3
WASHER_FLAT_4

MRB3
RUBBER_BUMPER

MS5
MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MS6
MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MH_125_250
MH3
GND

CBL1
NEMA 5-15P
IEC320-C13
110V 3 Prong
PC_POWER_CABLE
Power Cord

MS04
STANDOFF_0P625

MW4
WASHER_FLAT_4

MRB4
RUBBER_BUMPER

MS7
MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 3/16"

MS8
MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 3/16"

MH_125_250
MH4
GND

PB1
12v Power Brick
PWR_BRICK_12V

MS05
STANDOFF_0P625

MW5
WASHER_FLAT_4

MRB5
RUBBER_BUMPER

MS9
MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 0.25"

MS10
MACHINE_SCREW_4-40
#4-40 MACHINE SCREW 3/16"

MH_125_250
MH5
GND

CBL2
USB A
USB Micro-B
USB Micro-B Cable
USB_MICRO_CABLE

PL1
KCU116_PCIE_PLATE

MJB1 MJB2 MJB3 MJB4 MJB5 MJB6 MJB7 MJB8
JUMPER_BLOCK_2-PIN

MJB9 MJB10 MJB11 MJB12 MJB13 MJB14
JUMPER_BLOCK_2-PIN

Mechanical Components

XILINX

TITLE: Mechanical Components SCHEM, ROHS COMPLIANT HW-U1-KCU116_REV1_0	ASSY P/N: 0432019 PCB P/N: 1280924 SCH P/N: 0381757 TEST P/N: TSSXXXX
DATE: 04/03/2017:14:33	VER: 1.0
SHEET SIZE: B	REV: 01
SHEET 60 OF 60	DRAWN BY: DN