VC707 EVALUATION PLATFORM HW-V7-VC707 (XC7VX485T-FF1761)

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Title:	DISCLAIMER SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N:	0431663
		PCB P/N:	1280586
		SCH P/N:	0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
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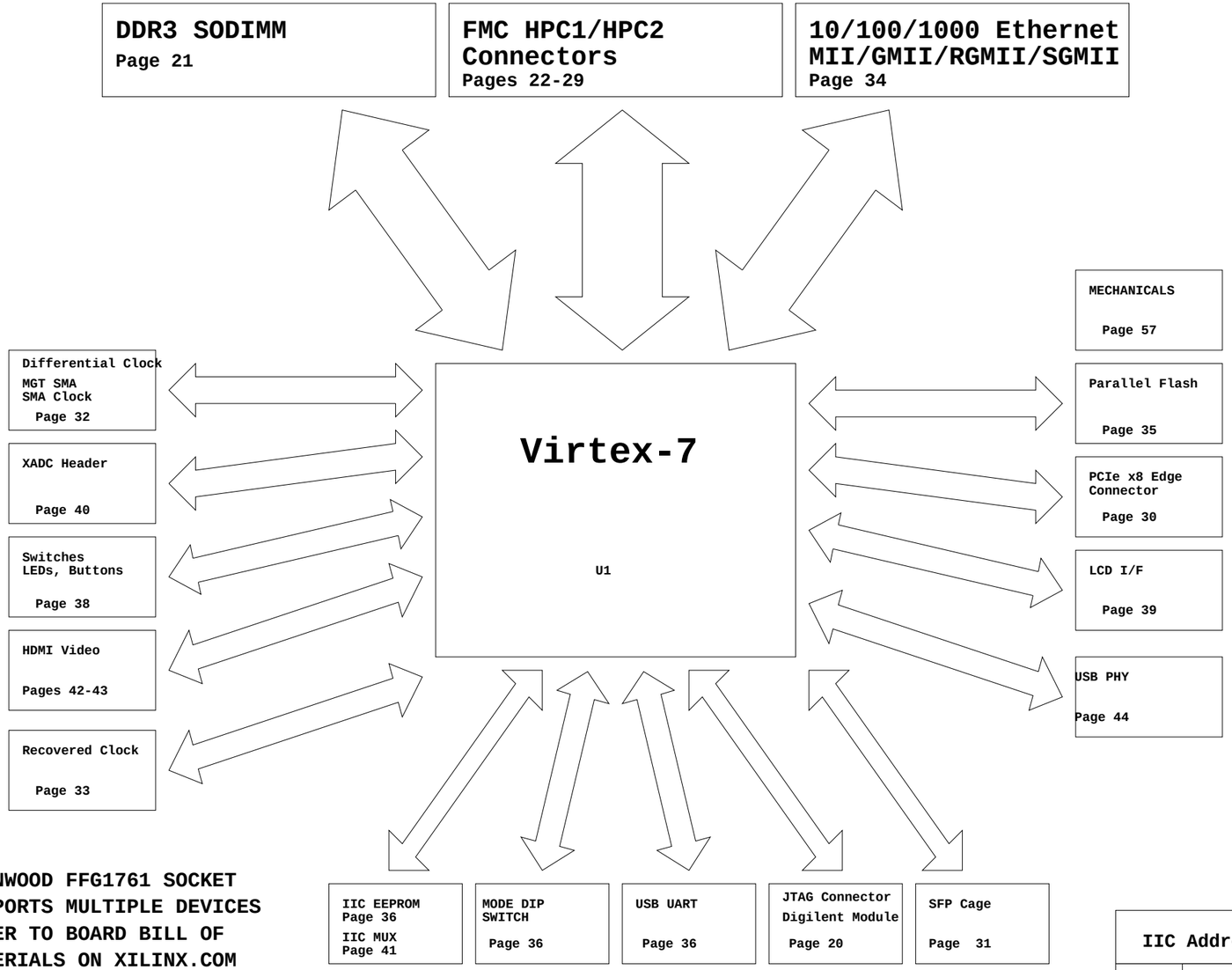
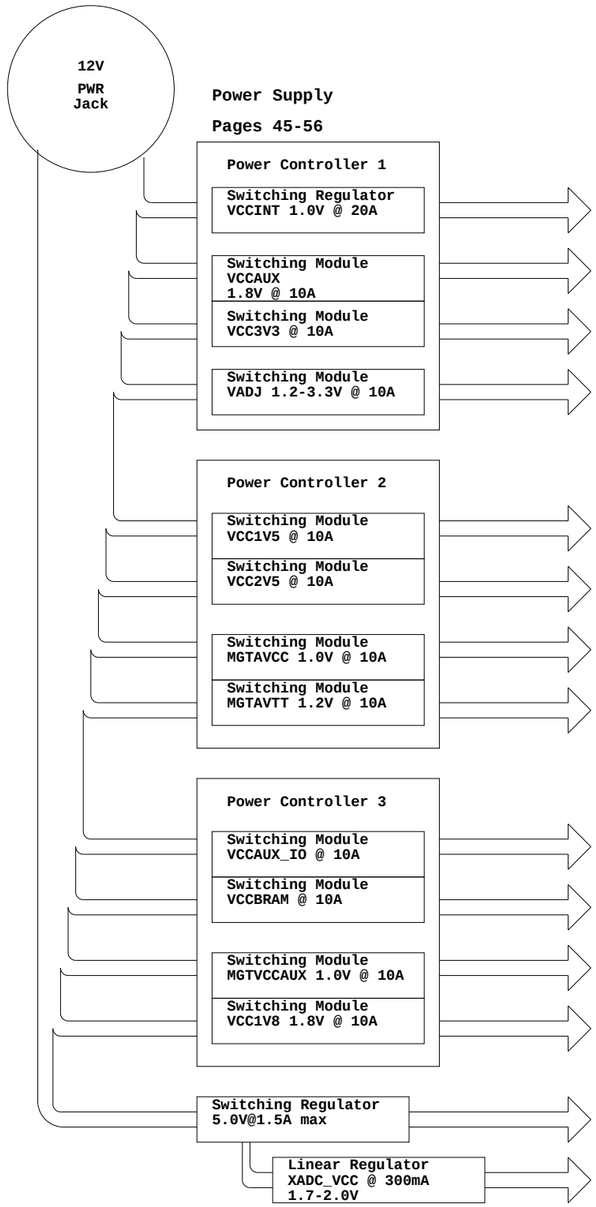
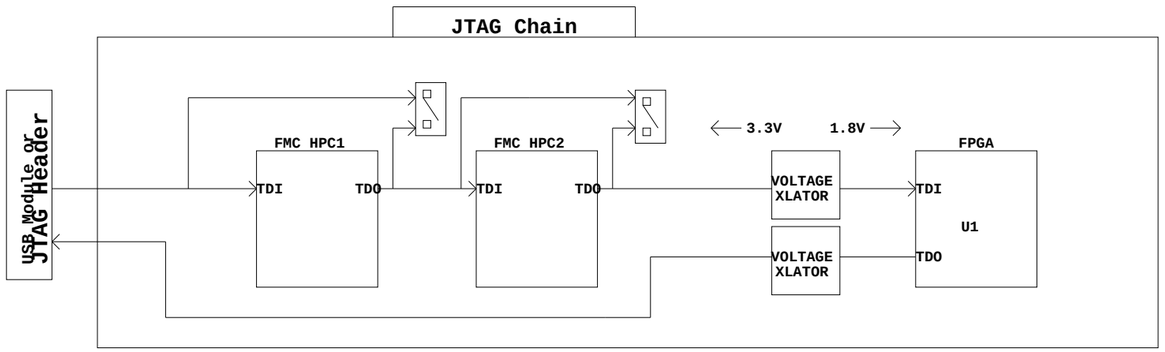


IRONWOOD FFG1761 SOCKET SUPPORTS MULTIPLE DEVICES REFER TO BOARD BILL OF MATERIALS ON XILINX.COM TO CONFIRM FPGA PROVIDED





IIC Addressing

0b1110000	PCA9548
0b1010100	SI570
0bxxxxx00	FMC HPC 1
0bxxxxx00	FMC HPC 2
0b1010100	IIC EEPROM
0b1010000	SFP+
0b0111001	ADV7512
0b1010000 0b0011000	DDR3 SODIMM
0b1010000	SI5326

XILINX

Title:	VC707 Block Diagram SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418
Date:	2-3-2012_10:13	Ver: 1.0
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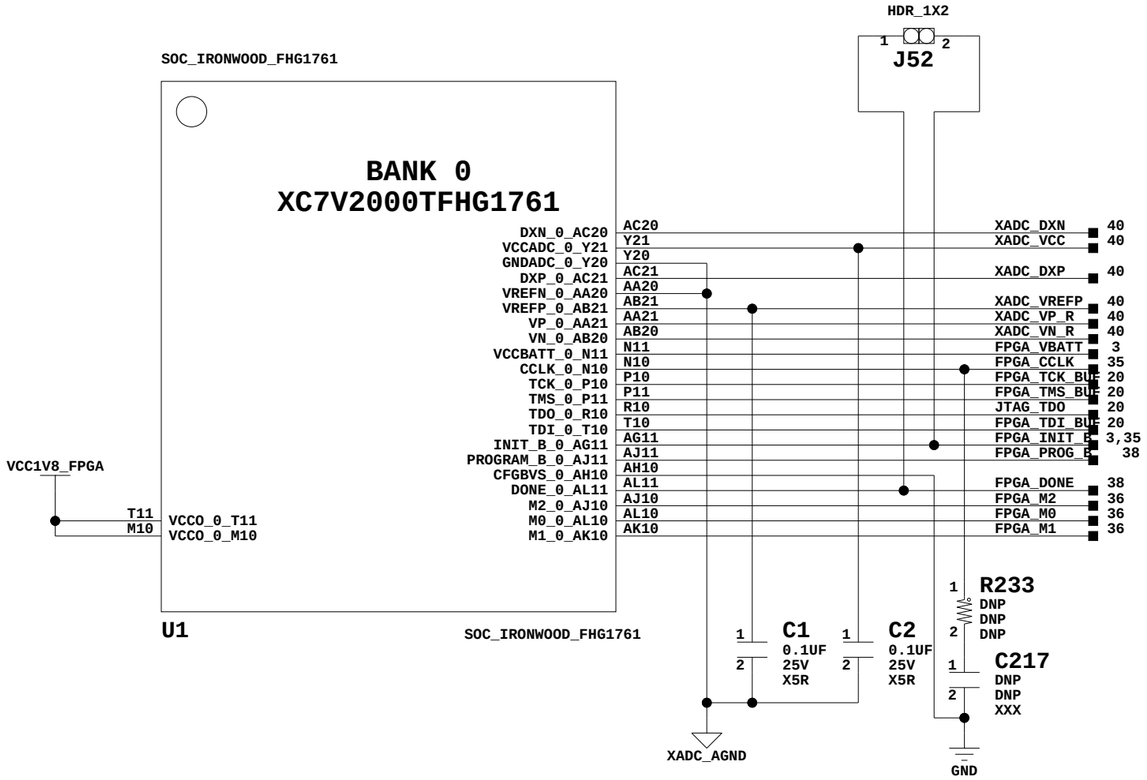

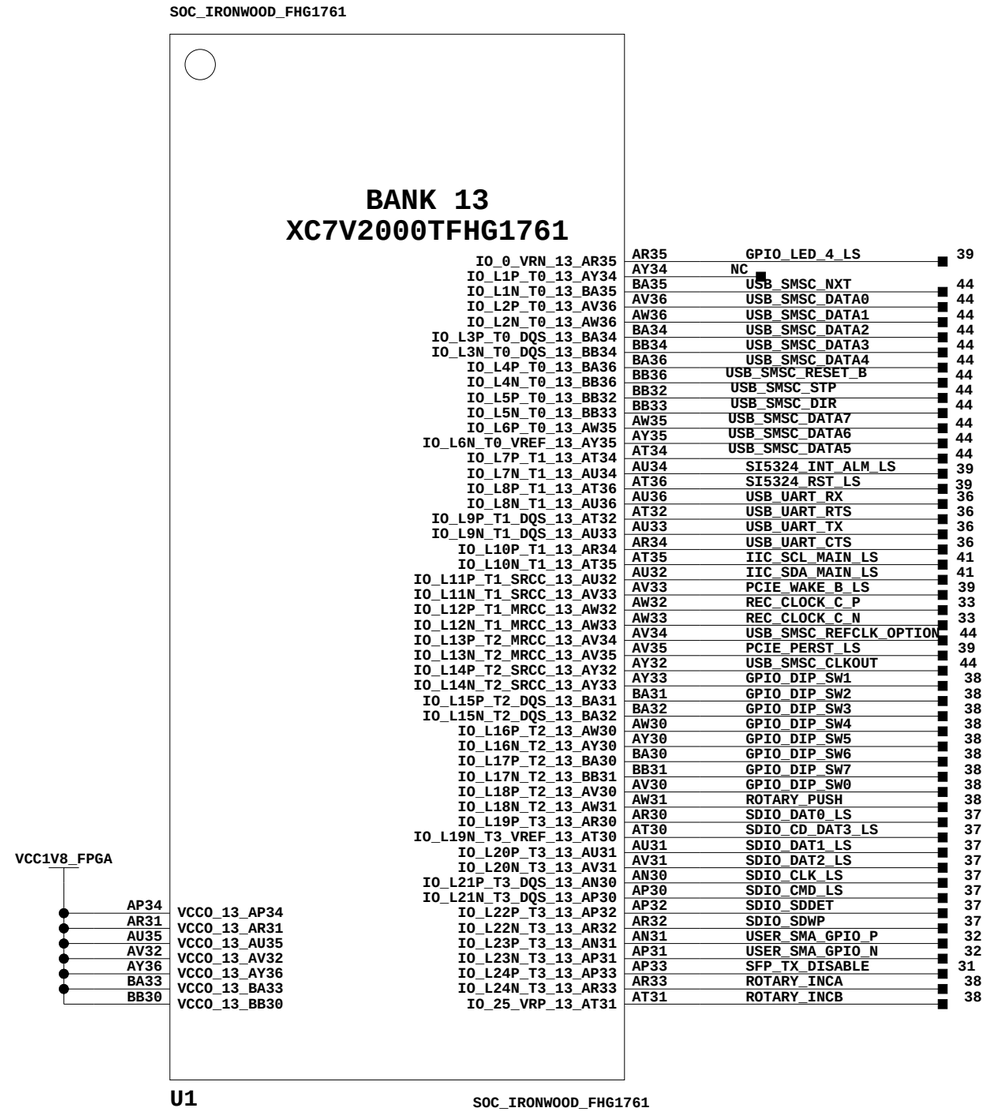

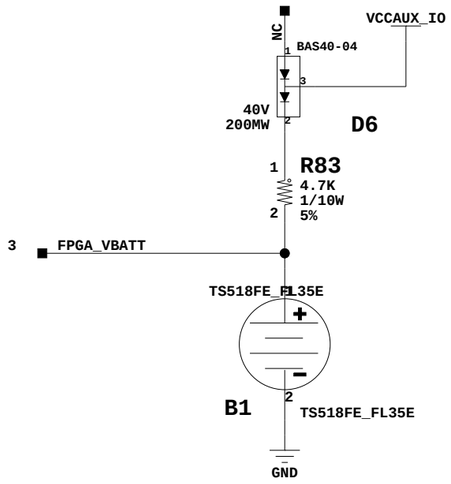

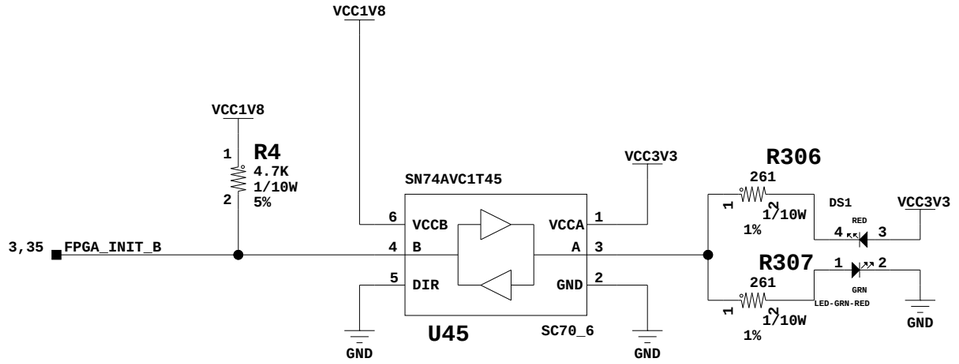

FPGA Banks 0,13

Title:	FPGA Banks 0,13 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
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SOC_IRONWOOD_FHG1761

BANK 14
XC7V2000TFHG1761

IO_0_VRN_14_AH35	AH35	FMC_VADJ_ON_B_LS	39
IO_L1P_T0_D00_MOSI_14_AM36	AM36	FLASH_D0	35
IO_L1N_T0_D01_DIN_14_AN36	AN36	FLASH_D1	35
IO_L2P_T0_D02_14_AJ36	AJ36	FLASH_D2	35
IO_L2N_T0_D03_14_AJ37	AJ37	FLASH_D3	35
IO_L3P_T0_DQS_PUDC_B_14_AP36	AP36		
IO_L3N_T0_DQS_EMCCLK_14_AP37	AP37	FPGA_EMCCLK	20
IO_L4P_T0_D04_14_AK37	AK37	FLASH_D4	35
IO_L4N_T0_D05_14_AL37	AL37	FLASH_D5	35
IO_L5P_T0_D06_14_AN35	AN35	FLASH_D6	35
IO_L5N_T0_D07_14_AP35	AP35	FLASH_D7	35
IO_L6P_T0_FCS_B_14_AL36	AL36	FLASH_CE_B	35
IO_L6N_T0_D08_VREF_14_AM37	AM37	FLASH_D8	35
IO_L7P_T1_D09_14_AG33	AG33	FLASH_D9	35
IO_L7N_T1_D10_14_AH33	AH33	FLASH_D10	35
IO_L8P_T1_D11_14_AK35	AK35	FLASH_D11	35
IO_L8N_T1_D12_14_AL35	AL35	FLASH_D12	35
IO_L9P_T1_DQS_14_AH31	AH31	PHY_MDC_LS	39
IO_L9N_T1_DQS_D13_14_AJ31	AJ31	FLASH_D13	35
IO_L10P_T1_D14_14_AH34	AH34	FLASH_D14	35
IO_L10N_T1_D15_14_AJ35	AJ35	FLASH_D15	35
IO_L11P_T1_SRCC_14_AJ33	AJ33	PHY_RESET_LS	39
IO_L11N_T1_SRCC_14_AK33	AK33	PHY_MDIO_LS	39
IO_L12P_T1_MRCC_14_AK34	AK34	USER_CLOCK_P	32
IO_L12N_T1_MRCC_14_AL34	AL34	USER_CLOCK_N	32
IO_L13P_T2_MRCC_14_AJ32	AJ32	USER_SMA_CLOCK_P	32
IO_L13N_T2_MRCC_14_AK32	AK32	USER_SMA_CLOCK_N	32
IO_L14P_T2_SRCC_14_AL31	AL31	PHY_INT_LS	39
IO_L14N_T2_SRCC_14_AL32	AL32	FMC_C2M_PG_LS	39
IO_L15P_T2_DQS_RDWR_B_14_AM34	AM34	FLASH_WAIT	35
IO_L15N_T2_DQSDOUT_CSOB_14_AN34	AN34	FMC1_HPC_PG_M2C_LS	39
IO_L16P_T2_CSI_B_14_AM31	AM31	FMC1_HPC_PRSNT_M2C_B_LS	39
IO_L16N_T2_A15_D31_14_AM32	AM32	FLASH_A15	35
IO_L17P_T2_A14_D30_14_AM33	AM33	FLASH_A14	35
IO_L17N_T2_A13_D29_14_AN33	AN33	FLASH_A13	35
IO_L18P_T2_A12_D28_14_AL29	AL29	FLASH_A12	35
IO_L18N_T2_A11_D27_14_AL30	AL30	FLASH_A11	35
IO_L19P_T3_A10_D26_14_AH29	AH29	FLASH_A10	35
IO_L19N_T3A09D25_VREF_14_AH30	AH30	FLASH_A9	35
IO_L20P_T3_A08_D24_14_AJ30	AJ30	FLASH_A8	35
IO_L20N_T3_A07_D23_14_AK30	AK30	FLASH_A7	35
IO_L21P_T3_DQS_14_AF29	AF29	FMC2_HPC_PG_M2C_LS	39
IO_L21N_T3_DQS_A06_D22_14_AG29	AG29	FLASH_A6	35
IO_L22P_T3_A05_D21_14_AK28	AK28	FLASH_A5	35
IO_L22N_T3_A04_D20_14_AK29	AK29	FLASH_A4	35
IO_L23P_T3_A03_D19_14_AF30	AF30	FLASH_A3	35
IO_L23N_T3_A02_D18_14_AG31	AG31	FLASH_A2	35
IO_L24P_T3_A01_D17_14_AH28	AH28	FLASH_A1	35
IO_L24N_T3_A00_D16_14_AJ28	AJ28	FLASH_A0	35
IO_25_VRP_14_AG32	AG32	FMC2_HPC_PRSNT_M2C_B_LS	39

VCC1V8_FPGA

AF28	VCCO_14_AF28
AH32	VCCO_14_AH32
AJ29	VCCO_14_AJ29
AK36	VCCO_14_AK36
AL33	VCCO_14_AL33
AM30	VCCO_14_AM30
AN37	VCCO_14_AN37

R276 1.00K 1/16W 1% (1 — 2) — 1 — GND

U1 SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

BANK 15
XC7V2000TFHG1761

IO_0_VRN_15_AM38	AM38	VRN_15	4
IO_L1P_T0_AD0P_15_AN38	AN38	XADC_VAUX0P_R	40
IO_L1N_T0_AD0N_15_AP38	AP38	XADC_VAUX0N_R	40
IO_L2P_T0_AD8P_15_AM41	AM41	XADC_VAUX8P_R	40
IO_L2N_T0_AD8N_15_AM42	AM42	XADC_VAUX8N_R	40
IO_L3P_T0_DQS_AD1P_15_AR38	AR38	LCD_DB5_LS	39
IO_L3N_T0_DQS_AD1N_15_AR39	AR39	LCD_DB6_LS	39
IO_L4P_T0_15_AN40	AN40	LCD_DB7_LS	39
IO_L4N_T0_15_AN41	AN41	LCD_RS_LS	39
IO_L5P_T0_AD9P_15_AR37	AR37	GPIO_LED_2_LS	39
IO_L5N_T0_AD9N_15_AT37	AT37	GPIO_LED_3_LS	39
IO_L6P_T0_15_AM39	AM39	GPIO_LED_0_LS	39
IO_L6N_T0_VREF_15_AN39	AN39	GPIO_LED_1_LS	39
IO_L7P_T1_AD2P_15_AP40	AP40	GPIO_SW_S	38
IO_L7N_T1_AD2N_15_AR40	AR40	GPIO_SW_N	38
IO_L8P_T1_AD10P_15_AP41	AP41	GPIO_LED_5_LS	39
IO_L8N_T1_AD10N_15_AP42	AP42	GPIO_LED_6_LS	39
IO_L9P_T1_DQS_AD3P_15_AT39	AT39	NC	
IO_L9N_T1_DQS_AD3N_15_AT40	AT40	LCD_E_LS	39
IO_L10P_T1_AD11P_15_AR42	AR42	LCD_RW_LS	39
IO_L10N_T1_AD11N_15_AT42	AT42	LCD_DB4_LS	39
IO_L11P_T1_SRCC_15_AU39	AU39	GPIO_LED_7_LS	39
IO_L11N_T1_SRCC_15_AV39	AV39	GPIO_SW_C	38
IO_L12P_T1_MRCC_15_AU38	AU38	GPIO_SW_E	38
IO_L12N_T1_MRCC_15_AV38	AV38	PMBUS_ALERT_LS	45
IO_L13P_T2_MRCC_15_AV40	AV40	CPU_RESET	38
IO_L13N_T2_MRCC_15_AW40	AW40	GPIO_SW_W	38
IO_L14P_T2_SRCC_15_AY39	AY39	PMBUS_DATA_LS	45
IO_L14N_T2_SRCC_15_AY40	AY40	NC	
IO_L15P_T2_DQS_15_AW37	AW37	PMBUS_CLK_LS	45
IO_L15N_T2_DQS_ADV_B_15_AY37	AY37	FLASH_ADV_B	35
IO_L16P_T2_A28_15_BA37	BA37	SM_FAN_PWM	45
IO_L16N_T2_A27_15_BB37	BB37	SM_FAN_TACH	45
IO_L17P_T2_A26_15_AW38	AW38	NC	
IO_L17N_T2_A25_15_AY38	AY38	NC	
IO_L18P_T2_A24_15_BB38	BB38	SFP_LOS_LS	39
IO_L18N_T2_A23_15_BB39	BB39	FLASH_A23	35
IO_L19P_T3_A22_15_BA39	BA39	FLASH_A22	35
IO_L19N_T3_A21_VREF_15_BA40	BA40	FLASH_A21	35
IO_L20P_T3_A20_15_AT41	AT41	FLASH_A20	35
IO_L20N_T3_A19_15_AU42	AU42	FLASH_A19	35
IO_L21P_T3_DQS_15_AY42	AY42	IIC_MUX_RESET_B_LS	39
IO_L21N_T3_DQS_A18_15_BA42	BA42	FLASH_A18	35
IO_L22P_T3_A17_15_AU41	AU41	FLASH_A17	35
IO_L22N_T3_A16_15_AV41	AV41	FLASH_A16	35
IO_L23P_T3_FOE_B_15_BA41	BA41	FLASH_OE_B	35
IO_L23N_T3_FWE_B_15_BB41	BB41	FLASH_FWE_B	35
IO_L24P_T3_RS1_15_AW41	AW41	FLASH_A25	35,36
IO_L24N_T3_RS0_15_AW42	AW42	FLASH_A24	35,36
IO_25_VRP_15_AU37	AU37	VRP_15	4

VCC1V8_FPGA

AM40	VCCO_15_AM40
AR41	VCCO_15_AR41
AT38	VCCO_15_AT38
AV42	VCCO_15_AV42
AW39	VCCO_15_AW39
BB40	VCCO_15_BB40

U1 SOC_IRONWOOD_FHG1761

VCC1V8_FPGA

R419 100 1/10W 1% (1 — 2) — 4 — VRN_15

R420 100 1/10W 1% (1 — 2) — 4 — VRP_15 — GND

FPGA Banks 14, 15

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Title:	FPGA Banks 14, 15 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N:	0431663
		PCB P/N:	1280586
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SOC_IRONWOOD_FHG1761

BANK 16
XC7V2000TFHG1761

IO_0_VRN_16_Y34	Y34	NC	
IO_L1P_T0_16_AF35	AF35	FMC2_HPC_HA14_P	28
IO_L1N_T0_16_AF36	AF36	FMC2_HPC_HA14_N	28
IO_L2P_T0_16_AE37	AE37	FMC2_HPC_HA15_P	27
IO_L2N_T0_16_AF37	AF37	FMC2_HPC_HA15_N	27
IO_L3P_T0_DQS_16_AF34	AF34	FMC2_HPC_HA12_P	27
IO_L3N_T0_DQS_16_AG34	AG34	FMC2_HPC_HA12_N	27
IO_L4P_T0_16_AD36	AD36	FMC2_HPC_HA20_P	27
IO_L4N_T0_16_AD37	AD37	FMC2_HPC_HA20_N	27
IO_L5P_T0_16_AC35	AC35	FMC2_HPC_HA19_P	27
IO_L5N_T0_16_AC36	AC36	FMC2_HPC_HA19_N	27
IO_L6P_T0_16_AG36	AG36	FMC2_HPC_HA16_P	27
IO_L6N_T0_VREF_16_AH36	AH36	FMC2_HPC_HA16_N	27
IO_L7P_T1_16_Y37	Y37	FMC2_HPC_HA23_P	28
IO_L7N_T1_16_AA37	AA37	FMC2_HPC_HA23_N	28
IO_L8P_T1_16_Y35	Y35	FMC2_HPC_HA22_P	28
IO_L8N_T1_16_AA36	AA36	FMC2_HPC_HA22_N	28
IO_L9P_T1_DQS_16_AB36	AB36	FMC2_HPC_HA18_P	28
IO_L9N_T1_DQS_16_AB37	AB37	FMC2_HPC_HA18_N	28
IO_L10P_T1_16_AA34	AA34	FMC2_HPC_HA21_P	28
IO_L10N_T1_16_AA35	AA35	FMC2_HPC_HA21_N	28
IO_L11P_T1_SRCC_16_AB31	AB31	FMC2_HPC_HA06_P	28
IO_L11N_T1_SRCC_16_AB32	AB32	FMC2_HPC_HA06_N	28
IO_L12P_T1_MRCC_16_AB33	AB33	FMC2_HPC_HA00_CC_P	27
IO_L12N_T1_MRCC_16_AC33	AC33	FMC2_HPC_HA00_CC_N	27
IO_L13P_T2_MRCC_16_AD32	AD32	FMC2_HPC_HA01_CC_P	27
IO_L13N_T2_MRCC_16_AD33	AD33	FMC2_HPC_HA01_CC_N	27
IO_L14P_T2_SRCC_16_AC34	AC34	FMC2_HPC_HA17_CC_P	28
IO_L14N_T2_SRCC_16_AD35	AD35	FMC2_HPC_HA17_CC_N	28
IO_L15P_T2_DQS_16_AE32	AE32	FMC2_HPC_HA13_P	27
IO_L15N_T2_DQS_16_AE33	AE33	FMC2_HPC_HA13_N	27
IO_L16P_T2_16_AF31	AF31	FMC2_HPC_HA10_P	28
IO_L16N_T2_16_AF32	AF32	FMC2_HPC_HA10_N	28
IO_L17P_T2_16_AE34	AE34	FMC2_HPC_HA11_P	28
IO_L17N_T2_16_AE35	AE35	FMC2_HPC_HA11_N	28
IO_L18P_T2_16_AE29	AE29	FMC2_HPC_HA09_P	27
IO_L18N_T2_16_AE30	AE30	FMC2_HPC_HA09_N	27
IO_L19P_T3_16_Y32	Y32	FMC2_HPC_HA05_P	27
IO_L19N_T3_VREF_16_Y33	Y33	FMC2_HPC_HA05_N	27
IO_L20P_T3_16_AC31	AC31	FMC2_HPC_HA07_P	28
IO_L20N_T3_16_AD31	AD31	FMC2_HPC_HA07_N	28
IO_L21P_T3_DQS_16_AA31	AA31	FMC2_HPC_HA08_P	27
IO_L21N_T3_DQS_16_AA32	AA32	FMC2_HPC_HA08_N	27
IO_L22P_T3_16_AC30	AC30	FMC2_HPC_HA02_P	28
IO_L22N_T3_16_AD30	AD30	FMC2_HPC_HA02_N	28
IO_L23P_T3_16_AA29	AA29	FMC2_HPC_HA03_P	28
IO_L23N_T3_16_AA30	AA30	FMC2_HPC_HA03_N	28
IO_L24P_T3_16_AB29	AB29	FMC2_HPC_HA04_P	27
IO_L24N_T3_16_AC29	AC29	FMC2_HPC_HA04_N	27
IO_25_VRP_16_AB34	AB34	NC	

VADJ_FPGA

AA33	VCCO_16_AA33
AB30	VCCO_16_AB30
AD34	VCCO_16_AD34
AE31	VCCO_16_AE31
AG35	VCCO_16_AG35
Y36	VCCO_16_Y36

U1

SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

BANK 17
XC7V2000TFHG1761

IO_0_VRN_17_Y38	Y38	NC	
IO_L1P_T0_17_AB41	AB41	FMC2_HPC_LA10_P	26
IO_L1N_T0_17_AB42	AB42	FMC2_HPC_LA10_N	26
IO_L2P_T0_17_W40	W40	FMC2_HPC_LA13_P	26
IO_L2N_T0_17_Y40	Y40	FMC2_HPC_LA13_N	26
IO_L3P_T0_DQS_17_Y39	Y39	FMC2_HPC_LA12_P	27
IO_L3N_T0_DQS_17_AA39	AA39	FMC2_HPC_LA12_N	27
IO_L4P_T0_17_Y42	Y42	FMC2_HPC_LA11_P	28
IO_L4N_T0_17_AA42	AA42	FMC2_HPC_LA11_N	28
IO_L5P_T0_17_AB38	AB38	FMC2_HPC_LA14_P	26
IO_L5N_T0_17_AB39	AB39	FMC2_HPC_LA14_N	26
IO_L6P_T0_17_AA40	AA40	NC	
IO_L6N_T0_VREF_17_AA41	AA41	NC	
IO_L7P_T1_17_AC38	AC38	FMC2_HPC_LA15_P	28
IO_L7N_T1_17_AC39	AC39	FMC2_HPC_LA15_N	28
IO_L8P_T1_17_AD42	AD42	FMC2_HPC_LA08_P	27
IO_L8N_T1_17_AE42	AE42	FMC2_HPC_LA08_N	27
IO_L9P_T1_DQS_17_AD38	AD38	FMC2_HPC_LA06_P	26
IO_L9N_T1_DQS_17_AE38	AE38	FMC2_HPC_LA06_N	26
IO_L10P_T1_17_AC40	AC40	FMC2_HPC_LA07_P	28
IO_L10N_T1_17_AC41	AC41	FMC2_HPC_LA07_N	28
IO_L11P_T1_SRCC_17_AE39	AE39	NC	
IO_L11N_T1_SRCC_17_AE40	AE40	NC	
IO_L12P_T1_MRCC_17_AD40	AD40	FMC2_HPC_LA00_CC_P	27
IO_L12N_T1_MRCC_17_AD41	AD41	FMC2_HPC_LA00_CC_N	27
IO_L13P_T2_MRCC_17_AF39	AF39	FMC2_HPC_CLK0_M2C_P	28
IO_L13N_T2_MRCC_17_AF40	AF40	FMC2_HPC_CLK0_M2C_N	28
IO_L14P_T2_SRCC_17_AF41	AF41	FMC2_HPC_LA01_CC_P	26
IO_L14N_T2_SRCC_17_AG41	AG41	FMC2_HPC_LA01_CC_N	26
IO_L15P_T2_DQS_17_AG39	AG39	NC	
IO_L15N_T2_DQS_17_AH39	AH39	NC	
IO_L16P_T2_17_AF42	AF42	FMC2_HPC_LA05_P	26
IO_L16N_T2_17_AG42	AG42	FMC2_HPC_LA05_N	26
IO_L17P_T2_17_AG38	AG38	NC	
IO_L17N_T2_17_AH38	AH38	NC	
IO_L18P_T2_17_AJ38	AJ38	FMC2_HPC_LA09_P	26
IO_L18N_T2_17_AK38	AK38	FMC2_HPC_LA09_N	26
IO_L19P_T3_17_AK40	AK40	NC	
IO_L19N_T3_VREF_17_AL40	AL40	NC	
IO_L20P_T3_17_AH40	AH40	NC	
IO_L20N_T3_17_AH41	AH41	NC	
IO_L21P_T3_DQS_17_AL41	AL41	FMC2_HPC_LA04_P	28
IO_L21N_T3_DQS_17_AL42	AL42	FMC2_HPC_LA04_N	28
IO_L22P_T3_17_AJ40	AJ40	FMC2_HPC_LA16_P	27
IO_L22N_T3_17_AJ41	AJ41	FMC2_HPC_LA16_N	27
IO_L23P_T3_17_AK39	AK39	FMC2_HPC_LA02_P	28
IO_L23N_T3_17_AL39	AL39	FMC2_HPC_LA02_N	28
IO_L24P_T3_17_AJ42	AJ42	FMC2_HPC_LA03_P	27
IO_L24N_T3_17_AK42	AK42	FMC2_HPC_LA03_N	27
IO_25_VRP_17_AG37	AG37	NC	

VADJ_FPGA

AB40	VCCO_17_AB40
AC37	VCCO_17_AC37
AE41	VCCO_17_AE41
AF38	VCCO_17_AF38
AH42	VCCO_17_AH42
AJ39	VCCO_17_AJ39

U1

SOC_IRONWOOD_FHG1761

FPGA Banks 16, 17

XILINX

Title:	FPGA Banks 16, 17 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	5 of 57	Drawn By	BF

SOC_IRONWOOD_FHG1761

BANK 18
XC7V2000TFHG1761

IO_0_VRN_18_N35	N35	NC	
IO_L1P_T0_18_T34	T34	NC	
IO_L1N_T0_18_R35	R35	NC	
IO_L2P_T0_18_N33	N33	FMC2_HPC_LA26_P	26
IO_L2N_T0_18_N34	N34	FMC2_HPC_LA26_N	26
IO_L3P_T0_DQS_18_R33	R33	FMC2_HPC_LA25_P	27
IO_L3N_T0_DQS_18_R34	R34	FMC2_HPC_LA25_N	27
IO_L4P_T0_18_P35	P35	FMC2_HPC_LA21_P	28
IO_L4N_T0_18_P36	P36	FMC2_HPC_LA21_N	28
IO_L5P_T0_18_T32	T32	FMC2_HPC_LA30_P	28
IO_L5N_T0_18_R32	R32	FMC2_HPC_LA30_N	28
IO_L6P_T0_18_P32	P32	FMC2_HPC_LA27_P	26
IO_L6N_T0_VREF_18_P33	P33	FMC2_HPC_LA27_N	26
IO_L7P_T1_18_T36	T36	FMC2_HPC_LA33_P	27
IO_L7N_T1_18_R37	R37	FMC2_HPC_LA33_N	27
IO_L8P_T1_18_P37	P37	FMC2_HPC_LA32_P	28
IO_L8N_T1_18_P38	P38	FMC2_HPC_LA32_N	28
IO_L9P_T1_DQS_18_U34	U34	FMC2_HPC_LA24_P	28
IO_L9N_T1_DQS_18_T35	T35	FMC2_HPC_LA24_N	28
IO_L10P_T1_18_R38	R38	FMC2_HPC_LA23_P	26
IO_L10N_T1_18_R39	R39	FMC2_HPC_LA23_N	26
IO_L11P_T1_SRCC_18_U37	U37	FMC2_HPC_LA17_CC_P	26
IO_L11N_T1_SRCC_18_U38	U38	FMC2_HPC_LA17_CC_N	26
IO_L12P_T1_MRCC_18_U39	U39	FMC2_HPC_CLK1_M2C_P	27
IO_L12N_T1_MRCC_18_T39	T39	FMC2_HPC_CLK1_M2C_N	27
IO_L13P_T2_MRCC_18_U36	U36	FMC2_HPC_LA18_CC_P	26
IO_L13N_T2_MRCC_18_T37	T37	FMC2_HPC_LA18_CC_N	26
IO_L14P_T2_SRCC_18_V35	V35	FMC2_HPC_LA28_P	28
IO_L14N_T2_SRCC_18_V36	V36	FMC2_HPC_LA28_N	28
IO_L15P_T2_DQS_18_V33	V33	FMC2_HPC_LA20_P	27
IO_L15N_T2_DQS_18_V34	V34	FMC2_HPC_LA20_N	27
IO_L16P_T2_18_W36	W36	FMC2_HPC_LA29_P	27
IO_L16N_T2_18_W37	W37	FMC2_HPC_LA29_N	27
IO_L17P_T2_18_U32	U32	FMC2_HPC_LA19_P	28
IO_L17N_T2_18_U33	U33	FMC2_HPC_LA19_N	28
IO_L18P_T2_18_W32	W32	FMC2_HPC_LA22_P	27
IO_L18N_T2_18_W33	W33	FMC2_HPC_LA22_N	27
IO_L19P_T3_18_V39	V39	FMC2_HPC_LA31_P	27
IO_L19N_T3_VREF_18_V40	V40	FMC2_HPC_LA31_N	27
IO_L20P_T3_18_T40	T40	NC	
IO_L20N_T3_18_T41	T41	NC	
IO_L21P_T3_DQS_18_W41	W41	NC	
IO_L21N_T3_DQS_18_W42	W42	NC	
IO_L22P_T3_18_U41	U41	NC	
IO_L22N_T3_18_T42	T42	NC	
IO_L23P_T3_18_W38	W38	NC	
IO_L23N_T3_18_V38	V38	NC	
IO_L24P_T3_18_V41	V41	NC	
IO_L24N_T3_18_U42	U42	NC	
IO_25_VRP_18_W35	W35	NC	

VADJ_FPGA

P34	VCCO_18_P34	
T38	VCCO_18_T38	
U35	VCCO_18_U35	
V32	VCCO_18_V32	
V42	VCCO_18_V42	
W39	VCCO_18_W39	

U1

SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

BANK 19
XC7V2000TFHG1761

IO_0_VRN_19_L36	L36	VRN_19	6
IO_L1P_T0_19_E40	E40	NC	
IO_L1N_T0_19_D40	D40	NC	
IO_L2P_T0_19_A40	A40	NC	
IO_L2N_T0_19_A41	A41	NC	
IO_L3P_T0_DQS_19_D41	D41	NC	
IO_L3N_T0_DQS_19_D42	D42	NC	
IO_L4P_T0_19_B41	B41	NC	
IO_L4N_T0_19_B42	B42	NC	
IO_L5P_T0_19_F42	F42	NC	
IO_L5N_T0_19_E42	E42	NC	
IO_L6P_T0_19_C40	C40	NC	
IO_L6N_T0_VREF_19_C41	C41	NC	
IO_L7P_T1_19_H40	H40	FMC1_HPC_LA04_P	24
IO_L7N_T1_19_H41	H41	FMC1_HPC_LA04_N	24
IO_L8P_T1_19_H39	H39	FMC1_HPC_LA13_P	22
IO_L8N_T1_19_G39	G39	FMC1_HPC_LA13_N	22
IO_L9P_T1_DQS_19_G41	G41	FMC1_HPC_LA07_P	24
IO_L9N_T1_DQS_19_G42	G42	FMC1_HPC_LA07_N	24
IO_L10P_T1_19_F40	F40	FMC1_HPC_LA11_P	24
IO_L10N_T1_19_F41	F41	FMC1_HPC_LA11_N	24
IO_L11P_T1_SRCC_19_J40	J40	FMC1_HPC_LA01_CC_P	22
IO_L11N_T1_SRCC_19_J41	J41	FMC1_HPC_LA01_CC_N	22
IO_L12P_T1_MRCC_19_K39	K39	FMC1_HPC_LA00_CC_P	23
IO_L12N_T1_MRCC_19_K40	K40	FMC1_HPC_LA00_CC_N	23
IO_L13P_T2_MRCC_19_L39	L39	FMC1_HPC_CLK0_M2C_P	24
IO_L13N_T2_MRCC_19_L40	L40	FMC1_HPC_CLK0_M2C_N	24
IO_L14P_T2_SRCC_19_M41	M41	FMC1_HPC_LA05_P	22
IO_L14N_T2_SRCC_19_L41	L41	FMC1_HPC_LA05_N	22
IO_L15P_T2_DQS_19_K42	K42	FMC1_HPC_LA06_P	22
IO_L15N_T2_DQS_19_J42	J42	FMC1_HPC_LA06_N	22
IO_L16P_T2_19_M42	M42	FMC1_HPC_LA03_P	23
IO_L16N_T2_19_L42	L42	FMC1_HPC_LA03_N	23
IO_L17P_T2_19_K37	K37	FMC1_HPC_LA16_P	23
IO_L17N_T2_19_K38	K38	FMC1_HPC_LA16_N	23
IO_L18P_T2_19_M36	M36	FMC1_HPC_LA15_P	24
IO_L18N_T2_19_L37	L37	FMC1_HPC_LA15_N	24
IO_L19P_T3_19_P41	P41	FMC1_HPC_LA02_P	24
IO_L19N_T3_VREF_19_N41	N41	FMC1_HPC_LA02_N	24
IO_L20P_T3_19_M37	M37	FMC1_HPC_LA08_P	23
IO_L20N_T3_19_M38	M38	FMC1_HPC_LA08_N	23
IO_L21P_T3_DQS_19_R42	R42	FMC1_HPC_LA09_P	22
IO_L21N_T3_DQS_19_P42	P42	FMC1_HPC_LA09_N	22
IO_L22P_T3_19_N38	N38	FMC1_HPC_LA10_P	22
IO_L22N_T3_19_M39	M39	FMC1_HPC_LA10_N	22
IO_L23P_T3_19_R40	R40	FMC1_HPC_LA12_P	23
IO_L23N_T3_19_P40	P40	FMC1_HPC_LA12_N	23
IO_L24P_T3_19_N39	N39	FMC1_HPC_LA14_P	22
IO_L24N_T3_19_N40	N40	FMC1_HPC_LA14_N	22
IO_25_VRP_19_N36	N36	VRP_19	6

VADJ_FPGA

B40	VCCO_19_B40	
E41	VCCO_19_E41	
H42	VCCO_19_H42	
J39	VCCO_19_J39	
M40	VCCO_19_M40	
N37	VCCO_19_N37	
R41	VCCO_19_R41	

U1

SOC_IRONWOOD_FHG1761

VCC1V8_FPGA

1 R450 2
100
1/10W
1%

6 VRN_19

6 VRP_19

1 R449 2
100
1/10W
1%

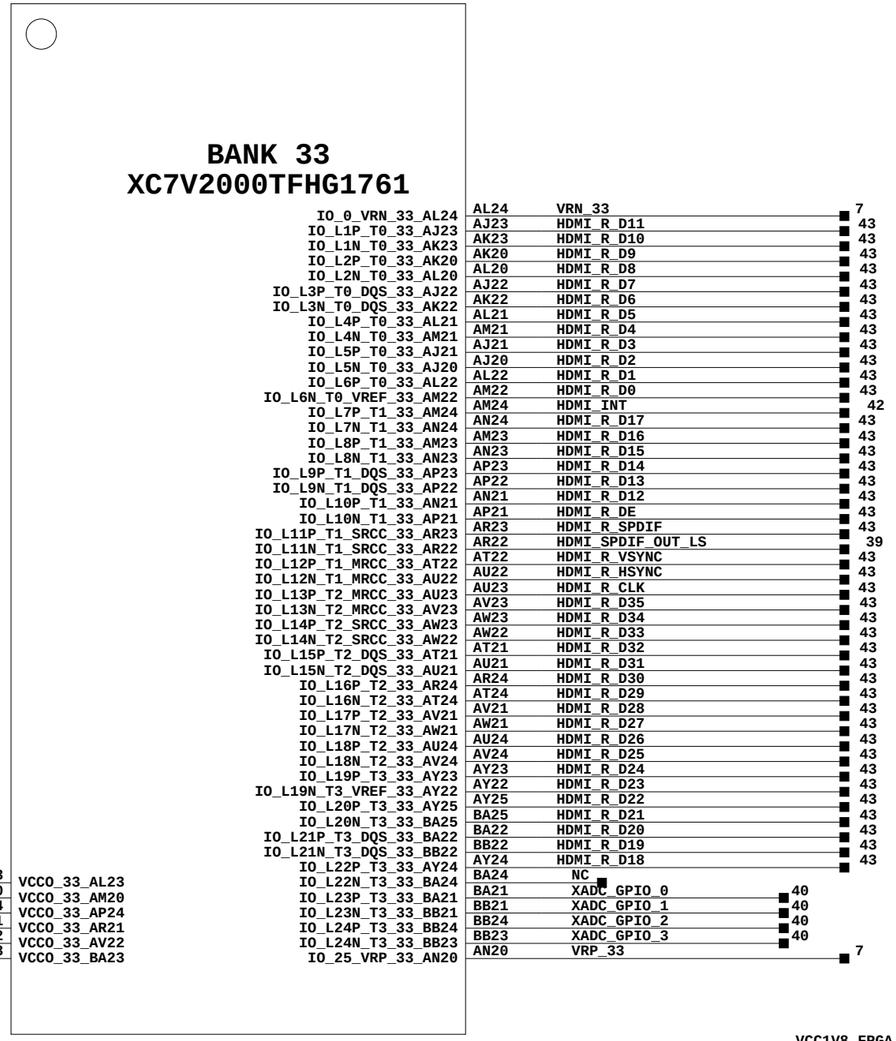
GND

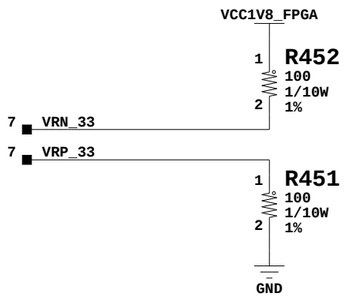
FPGA Banks 18, 19

XILINX

Title:	FPGA Banks 18, 19 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	6 of 57	Drawn By	BF

SOC_IRONWOOD_FHG1761





FPGA Bank 33

XILINX

Title:	FPGA Bank 33 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	7 of 57	Drawn By	BF

SOC_IRONWOOD_FHG1761

BANK 34
XC7V2000TFHG1761

IO_0_VRN_34_R29	R29	VRN_34	8
IO_L1P_T0_34_K35	K35	NC	
IO_L1N_T0_34_J35	J35	NC	
IO_L2P_T0_34_J32	J32	NC	
IO_L2N_T0_34_J33	J33	NC	
IO_L3P_T0_DQS_34_K33	K33	NC	
IO_L3N_T0_DQS_34_K34	K34	NC	
IO_L4P_T0_34_L34	L34	NC	
IO_L4N_T0_34_L35	L35	NC	
IO_L5P_T0_34_M33	M33	NC	
IO_L5N_T0_34_M34	M34	NC	
IO_L6P_T0_34_H34	H34	NC	
IO_L6N_T0_VREF_34_H35	H35	NC	
IO_L7P_T1_34_K29	K29	FMC1_HPC_LA25_P	23
IO_L7N_T1_34_K30	K30	FMC1_HPC_LA25_N	23
IO_L8P_T1_34_J30	J30	FMC1_HPC_LA26_P	22
IO_L8N_T1_34_H30	H30	FMC1_HPC_LA26_N	22
IO_L9P_T1_DQS_34_L29	L29	FMC1_HPC_LA28_P	24
IO_L9N_T1_DQS_34_L30	L30	FMC1_HPC_LA28_N	24
IO_L10P_T1_34_J31	J31	FMC1_HPC_LA27_P	22
IO_L10N_T1_34_H31	H31	FMC1_HPC_LA27_N	22
IO_L11P_T1_SRCC_34_M32	M32	FMC1_HPC_LA18_CC_P	22
IO_L11N_T1_SRCC_34_L32	L32	FMC1_HPC_LA18_CC_N	22
IO_L12P_T1_MRCC_34_L31	L31	FMC1_HPC_LA17_CC_P	22
IO_L12N_T1_MRCC_34_K32	K32	FMC1_HPC_LA17_CC_N	22
IO_L13P_T2_MRCC_34_N30	N30	FMC1_HPC_CLK1_M2C_P	23
IO_L13N_T2_MRCC_34_M31	M31	FMC1_HPC_CLK1_M2C_N	23
IO_L14P_T2_SRCC_34_P30	P30	FMC1_HPC_LA23_P	22
IO_L14N_T2_SRCC_34_N31	N31	FMC1_HPC_LA23_N	22
IO_L15P_T2_DQS_34_M28	M28	FMC1_HPC_LA31_P	23
IO_L15N_T2_DQS_34_M29	M29	FMC1_HPC_LA31_N	23
IO_L16P_T2_34_R28	R28	FMC1_HPC_LA22_P	23
IO_L16N_T2_34_P28	P28	FMC1_HPC_LA22_N	23
IO_L17P_T2_34_N28	N28	FMC1_HPC_LA21_P	24
IO_L17N_T2_34_N29	N29	FMC1_HPC_LA21_N	24
IO_L18P_T2_34_R30	R30	FMC1_HPC_LA24_P	24
IO_L18N_T2_34_P31	P31	FMC1_HPC_LA24_N	24
IO_L19P_T3_34_U31	U31	FMC1_HPC_LA33_P	23
IO_L19N_T3_VREF_34_T31	T31	FMC1_HPC_LA33_N	23
IO_L20P_T3_34_V30	V30	FMC1_HPC_LA30_P	24
IO_L20N_T3_34_V31	V31	FMC1_HPC_LA30_N	24
IO_L21P_T3_DQS_34_T29	T29	FMC1_HPC_LA29_P	23
IO_L21N_T3_DQS_34_T30	T30	FMC1_HPC_LA29_N	23
IO_L22P_T3_34_W30	W30	FMC1_HPC_LA19_P	24
IO_L22N_T3_34_W31	W31	FMC1_HPC_LA19_N	24
IO_L23P_T3_34_V29	V29	FMC1_HPC_LA32_P	24
IO_L23N_T3_34_U29	U29	FMC1_HPC_LA32_N	24
IO_L24P_T3_34_Y29	Y29	FMC1_HPC_LA20_P	23
IO_L24N_T3_34_Y30	Y30	FMC1_HPC_LA20_N	23
IO_25_VRP_34_U28	U28	VRP_34	8

VADJ_FPGA

H32	VCCO_34_H32	
L33	VCCO_34_L33	
M30	VCCO_34_M30	
R31	VCCO_34_R31	
T28	VCCO_34_T28	
W29	VCCO_34_W29	

U1

SOC_IRONWOOD_FHG1761

VCC1V8_FPGA

R454
1
2
100
1/10W
1%

8 VRN_34

8 VRP_34

R453
1
2
100
1/10W
1%

GND

SOC_IRONWOOD_FHG1761

BANK 35
XC7V2000TFHG1761

IO_0_VRN_35_G31	G31	NC	
IO_L1P_T0_35_B36	B36	FMC1_HPC_HA13_P	23
IO_L1N_T0_35_A37	A37	FMC1_HPC_HA13_N	23
IO_L2P_T0_AD4P_35_B34	B34	FMC1_HPC_HA20_P	23
IO_L2N_T0_AD4N_35_A34	A34	FMC1_HPC_HA20_N	23
IO_L3P_T0_DQS_AD12P_35_B39	B39	FMC1_HPC_HA16_P	23
IO_L3N_T0_DQS_AD12N_35_A39	A39	FMC1_HPC_HA16_N	23
IO_L4P_T0_AD5P_35_A35	A35	FMC1_HPC_HA23_P	24
IO_L4N_T0_AD5N_35_A36	A36	FMC1_HPC_HA23_N	24
IO_L5P_T0_AD13P_35_C38	C38	FMC1_HPC_HA07_P	24
IO_L5N_T0_AD13N_35_C39	C39	FMC1_HPC_HA07_N	24
IO_L6P_T0_35_B37	B37	FMC1_HPC_HA12_P	23
IO_L6N_T0_VREF_35_B38	B38	FMC1_HPC_HA12_N	23
IO_L7P_T1_AD6P_35_E32	E32	FMC1_HPC_HA09_P	23
IO_L7N_T1_AD6N_35_D32	D32	FMC1_HPC_HA09_N	23
IO_L8P_T1_AD14P_35_B32	B32	FMC1_HPC_HA19_P	23
IO_L8N_T1_AD14N_35_B33	B33	FMC1_HPC_HA19_N	23
IO_L9P_T1_DQS_AD7P_35_E33	E33	FMC1_HPC_HA02_P	24
IO_L9N_T1_DQS_AD7N_35_D33	D33	FMC1_HPC_HA02_N	24
IO_L10P_T1_AD15P_35_C33	C33	FMC1_HPC_HA15_P	23
IO_L10N_T1_AD15N_35_C34	C34	FMC1_HPC_HA15_N	23
IO_L11P_T1_SRCC_35_D35	D35	FMC1_HPC_HA01_CC_P	23
IO_L11N_T1_SRCC_35_D36	D36	FMC1_HPC_HA01_CC_N	23
IO_L12P_T1_MRCC_35_C35	C35	FMC1_HPC_HA17_CC_P	24
IO_L12N_T1_MRCC_35_C36	C36	FMC1_HPC_HA17_CC_N	24
IO_L13P_T2_MRCC_35_E34	E34	FMC1_HPC_HA00_CC_P	23
IO_L13N_T2_MRCC_35_E35	E35	FMC1_HPC_HA00_CC_N	23
IO_L14P_T2_SRCC_35_D37	D37	FMC1_HPC_HA21_P	24
IO_L14N_T2_SRCC_35_D38	D38	FMC1_HPC_HA21_N	24
IO_L15P_T2_DQS_35_G32	G32	FMC1_HPC_HA05_P	23
IO_L15N_T2_DQS_35_F32	F32	FMC1_HPC_HA05_N	23
IO_L16P_T2_35_F36	F36	FMC1_HPC_HA22_P	24
IO_L16N_T2_35_F37	F37	FMC1_HPC_HA22_N	24
IO_L17P_T2_35_F34	F34	FMC1_HPC_HA04_P	23
IO_L17N_T2_35_F35	F35	FMC1_HPC_HA04_N	23
IO_L18P_T2_35_H33	H33	FMC1_HPC_HA03_P	24
IO_L18N_T2_35_G33	G33	FMC1_HPC_HA03_N	24
IO_L19P_T3_35_E37	E37	FMC1_HPC_HA14_P	24
IO_L19N_T3_VREF_35_E38	E38	FMC1_HPC_HA14_N	24
IO_L20P_T3_35_G36	G36	FMC1_HPC_HA06_P	24
IO_L20N_T3_35_G37	G37	FMC1_HPC_HA06_N	24
IO_L21P_T3_DQS_35_F39	F39	FMC1_HPC_HA18_P	24
IO_L21N_T3_DQS_35_E39	E39	FMC1_HPC_HA18_N	24
IO_L22P_T3_35_J37	J37	FMC1_HPC_HA11_P	24
IO_L22N_T3_35_J38	J38	FMC1_HPC_HA11_N	24
IO_L23P_T3_35_H38	H38	FMC1_HPC_HA10_P	24
IO_L23N_T3_35_G38	G38	FMC1_HPC_HA10_N	24
IO_L24P_T3_35_J36	J36	FMC1_HPC_HA08_P	23
IO_L24N_T3_35_H36	H36	FMC1_HPC_HA08_N	23
IO_25_VRP_35_G34	G34	NC	

VADJ_FPGA

A33	VCCO_35_A33	
C37	VCCO_35_C37	
D34	VCCO_35_D34	
E31	VCCO_35_E31	
F38	VCCO_35_F38	
G35	VCCO_35_G35	
K36	VCCO_35_K36	

U1

SOC_IRONWOOD_FHG1761

FPGA Banks 34, 35

XILINX

Title:	FPGA Banks 34, 35 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N:	0431663
		PCB P/N:	1280586
		SCH P/N:	0381418
Date:	2-3-2012_10:13	Ver:	1.0
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BANK 36
XC7V2000TFHG1761

IO_0_VRN_36_M23	M23	NC	
IO_L1P_T0_36_H24	H24	FMC1_HPC_HB04_P	23
IO_L1N_T0_36_G24	G24	FMC1_HPC_HB04_N	23
IO_L2P_T0_36_J21	J21	FMC1_HPC_HB14_P	24
IO_L2N_T0_36_H21	H21	FMC1_HPC_HB14_N	24
IO_L3P_T0_DQS_36_H25	H25	FMC1_HPC_HB08_P	23
IO_L3N_T0_DQS_36_H26	H26	FMC1_HPC_HB08_N	23
IO_L4P_T0_36_G21	G21	FMC1_HPC_HB18_P	24
IO_L4N_T0_36_G22	G22	FMC1_HPC_HB18_N	24
IO_L5P_T0_36_G26	G26	FMC1_HPC_HB07_P	24
IO_L5N_T0_36_G27	G27	FMC1_HPC_HB07_N	24
IO_L6P_T0_36_H23	H23	FMC1_HPC_HB09_P	23
IO_L6N_T0_VREF_36_G23	G23	FMC1_HPC_HB09_N	23
IO_L7P_T1_36_G28	G28	FMC1_HPC_HB03_P	23
IO_L7N_T1_36_G29	G29	FMC1_HPC_HB03_N	23
IO_L8P_T1_36_K28	K28	FMC1_HPC_HB02_P	23
IO_L8N_T1_36_J28	J28	FMC1_HPC_HB02_N	23
IO_L9P_T1_DQS_36_H28	H28	FMC1_HPC_HB01_P	24
IO_L9N_T1_DQS_36_H29	H29	FMC1_HPC_HB01_N	24
IO_L10P_T1_36_K27	K27	FMC1_HPC_HB05_P	23
IO_L10N_T1_36_J27	J27	FMC1_HPC_HB05_N	23
IO_L11P_T1_SRCC_36_K24	K24	FMC1_HPC_HB12_P	23
IO_L11N_T1_SRCC_36_K25	K25	FMC1_HPC_HB12_N	23
IO_L12P_T1_MRCC_36_J25	J25	FMC1_HPC_HB00_CC_P	24
IO_L12N_T1_MRCC_36_J26	J26	FMC1_HPC_HB00_CC_N	24
IO_L13P_T2_MRCC_36_M24	M24	FMC1_HPC_HB17_CC_P	24
IO_L13N_T2_MRCC_36_L24	L24	FMC1_HPC_HB17_CC_N	24
IO_L14P_T2_SRCC_36_K23	K23	FMC1_HPC_HB06_CC_P	24
IO_L14N_T2_SRCC_36_J23	J23	FMC1_HPC_HB06_CC_N	24
IO_L15P_T2_DQS_36_M22	M22	FMC1_HPC_HB10_P	24
IO_L15N_T2_DQS_36_L22	L22	FMC1_HPC_HB10_N	24
IO_L16P_T2_36_L25	L25	FMC1_HPC_HB19_P	23
IO_L16N_T2_36_L26	L26	FMC1_HPC_HB19_N	23
IO_L17P_T2_36_K22	K22	FMC1_HPC_HB11_P	24
IO_L17N_T2_36_J22	J22	FMC1_HPC_HB11_N	24
IO_L18P_T2_36_M21	M21	FMC1_HPC_HB15_P	24
IO_L18N_T2_36_L21	L21	FMC1_HPC_HB15_N	24
IO_L19P_T3_36_P21	P21	FMC1_HPC_HB20_P	23
IO_L19N_T3_VREF_36_N21	N21	FMC1_HPC_HB20_N	23
IO_L20P_T3_36_P25	P25	FMC1_HPC_HB13_P	23
IO_L20N_T3_36_P26	P26	FMC1_HPC_HB13_N	23
IO_L21P_T3_DQS_36_P22	P22	FMC1_HPC_HB21_P	23
IO_L21N_T3_DQS_36_P23	P23	FMC1_HPC_HB21_N	23
IO_L22P_T3_36_N25	N25	FMC1_HPC_HB16_P	23
IO_L22N_T3_36_N26	N26	FMC1_HPC_HB16_N	23
IO_L23P_T3_36_N23	N23	NC	
IO_L23N_T3_36_N24	N24	NC	
IO_L24P_T3_36_M27	M27	NC	
IO_L24N_T3_36_L27	L27	NC	
IO_25_VRP_36_M26	M26	NC	

FMC1_VIO_B_M2C

G25	VCCO_36_G25	
H22	VCCO_36_H22	
J29	VCCO_36_J29	
K26	VCCO_36_K26	
L23	VCCO_36_L23	
N27	VCCO_36_N27	
P24	VCCO_36_P24	

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SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

BANK 37
XC7V2000TFHG1761

IO_0_VRN_37_F21	F21	VRN_37	9
IO_L1P_T0_37_A24	A24	DDR3_D32	21
IO_L1N_T0_37_A25	A25	DDR3_D38	21
IO_L2P_T0_37_B22	B22	DDR3_D37	21
IO_L2N_T0_37_A22	A22	DDR3_D36	21
IO_L3P_T0_DQS_37_A26	A26	DDR3_DQS4_P	21
IO_L3N_T0_DQS_37_A27	A27	DDR3_DQS4_N	21
IO_L4P_T0_37_C23	C23	DDR3_DM4	21
IO_L4N_T0_37_B23	B23	DDR3_D33	21
IO_L5P_T0_37_B26	B26	DDR3_D35	21
IO_L5N_T0_37_B27	B27	DDR3_D34	21
IO_L6P_T0_37_C24	C24	DDR3_D39	21
IO_L6N_T0_VREF_37_B24	B24		
IO_L7P_T1_37_E23	E23	DDR3_D44	21
IO_L7N_T1_37_E24	E24	DDR3_D40	21
IO_L8P_T1_37_F22	F22	DDR3_D46	21
IO_L8N_T1_37_E22	E22	DDR3_D47	21
IO_L9P_T1_DQS_37_F25	F25	DDR3_DQS5_P	21
IO_L9N_T1_DQS_37_E25	E25	DDR3_DQS5_N	21
IO_L10P_T1_37_D22	D22	DDR3_D45	21
IO_L10N_T1_37_D23	D23	DDR3_D41	21
IO_L11P_T1_SRCC_37_D25	D25	DDR3_DM5	21
IO_L11N_T1_SRCC_37_D26	D26	DDR3_D42	21
IO_L12P_T1_MRCC_37_C25	C25	DDR3_D43	21
IO_L12N_T1_MRCC_37_C26	C26	NC	
IO_L13P_T2_MRCC_37_D27	D27	DDR3_D49	21
IO_L13N_T2_MRCC_37_D28	D28	DDR3_D52	21
IO_L14P_T2_SRCC_37_C28	C28	DDR3_D51	21
IO_L14N_T2_SRCC_37_C29	C29	DDR3_RESET_B	21
IO_L15P_T2_DQS_37_B28	B28	DDR3_DQS6_P	21
IO_L15N_T2_DQS_37_B29	B29	DDR3_DQS6_N	21
IO_L16P_T2_37_A31	A31	DDR3_D54	21
IO_L16N_T2_37_A32	A32	DDR3_D55	21
IO_L17P_T2_37_A29	A29	DDR3_D50	21
IO_L17N_T2_37_A30	A30	DDR3_D48	21
IO_L18P_T2_37_C31	C31	DDR3_DM6	21
IO_L18N_T2_37_B31	B31	DDR3_D53	21
IO_L19P_T3_37_E30	E30	DDR3_D56	21
IO_L19N_T3_VREF_37_D31	D31		
IO_L20P_T3_37_D30	D30	DDR3_D63	21
IO_L20N_T3_37_C30	C30	DDR3_D60	21
IO_L21P_T3_DQS_37_E27	E27	DDR3_DQS7_P	21
IO_L21N_T3_DQS_37_E28	E28	DDR3_DQS7_N	21
IO_L22P_T3_37_F29	F29	DDR3_D57	21
IO_L22N_T3_37_E29	E29	DDR3_D61	21
IO_L23P_T3_37_F26	F26	DDR3_D62	21
IO_L23N_T3_37_F27	F27	DDR3_D59	21
IO_L24P_T3_37_F30	F30	DDR3_D58	21
IO_L24N_T3_37_F31	F31	DDR3_DM7	21
IO_25_VRP_37_F24	F24	VRP_37	9

VCC1V5_FPGA

A23	VCCO_37_A23	
B30	VCCO_37_B30	
C27	VCCO_37_C27	
D24	VCCO_37_D24	
E21	VCCO_37_E21	
F28	VCCO_37_F28	

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SOC_IRONWOOD_FHG1761

VTTVREF

C461 0.1UF 25V X5R (1, 2)

C490 0.1UF 25V X5R (1, 2)

GND

VCC1V5_FPGA

R160 80.6 1/10W 1% (1, 2)

9 VRN_37

9 VRP_37

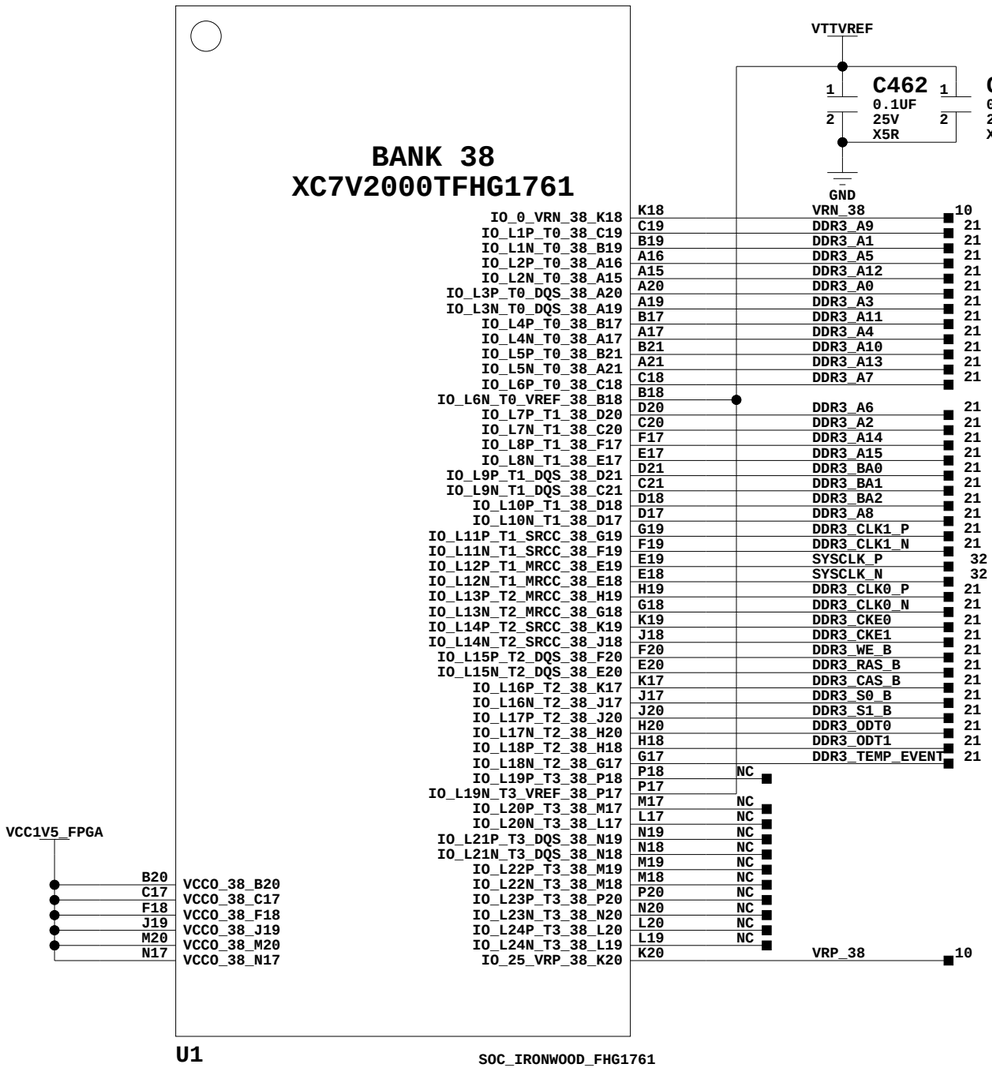
R159 80.6 1/10W 1% (1, 2)

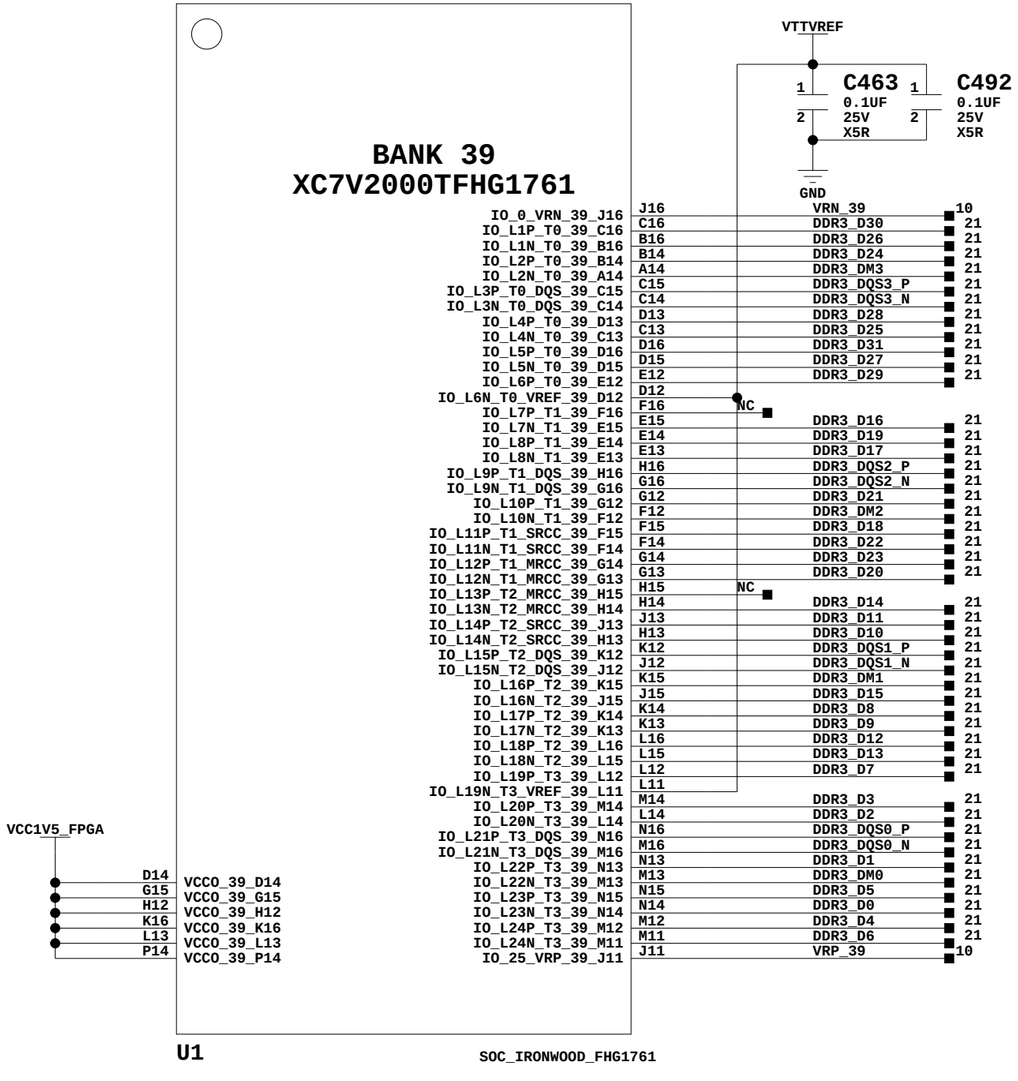
GND

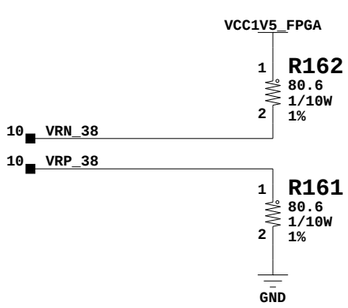
FPGA Banks 36, 37

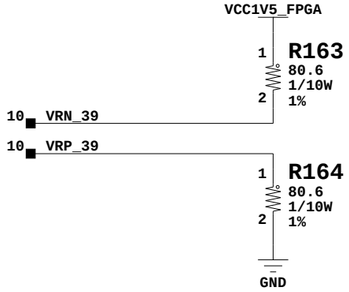
XILINX

Title:	FPGA Banks 36, 37 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N:	0431663
		PCB P/N:	1280586
		SCH P/N:	0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	9 of 57	Drawn By	BF









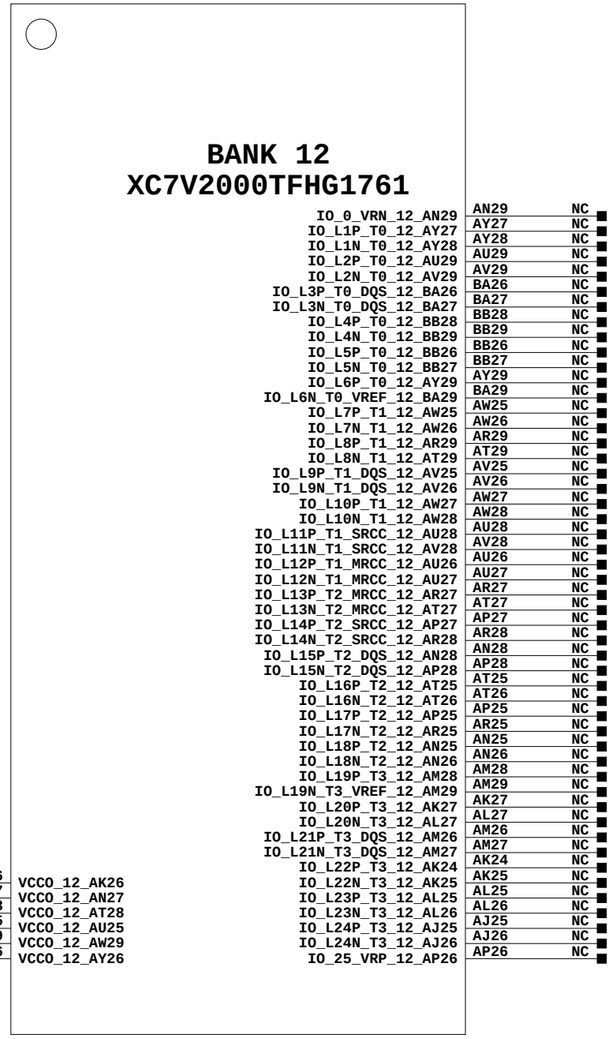
FPGA Banks 38, 39

XILINX

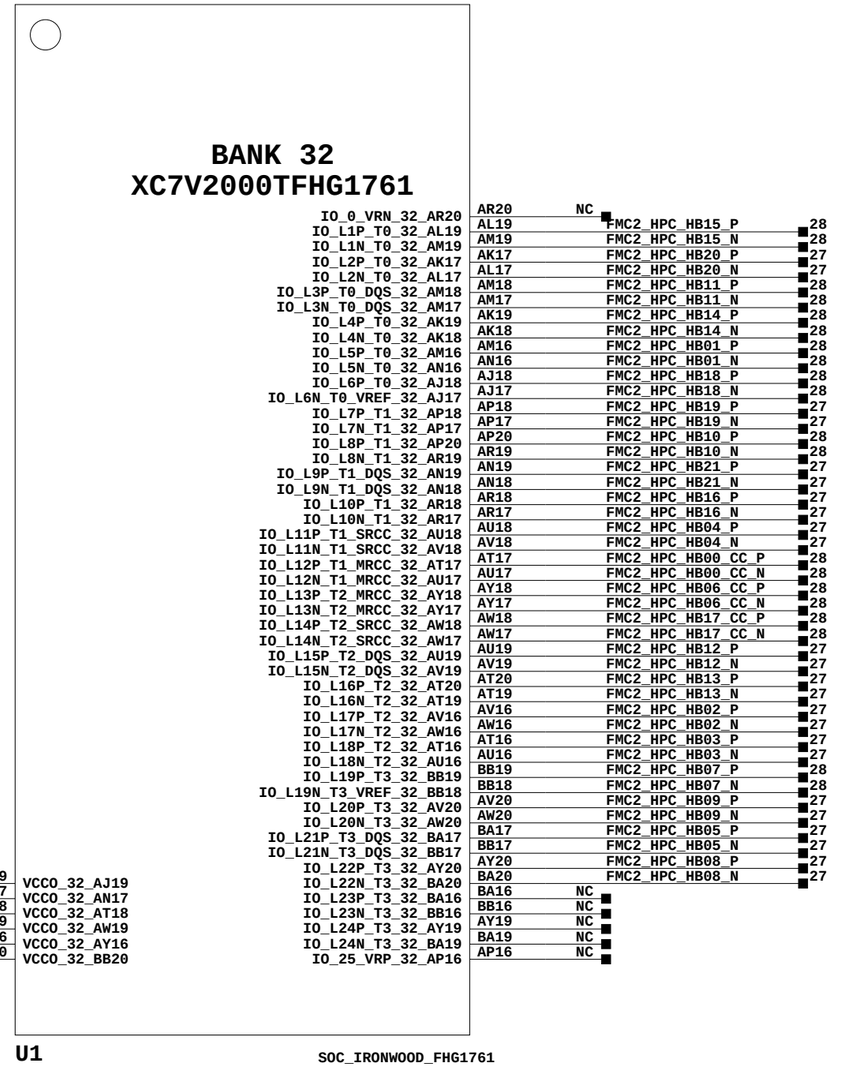
Title:	FPGA Banks 38, 39 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	10 of 57	Drawn By	BF

NOT USED ON 7VX485FFG1761
USED ON 7V585FFG1761

SOC_IRONWOOD_FHG1761



SOC_IRONWOOD_FHG1761



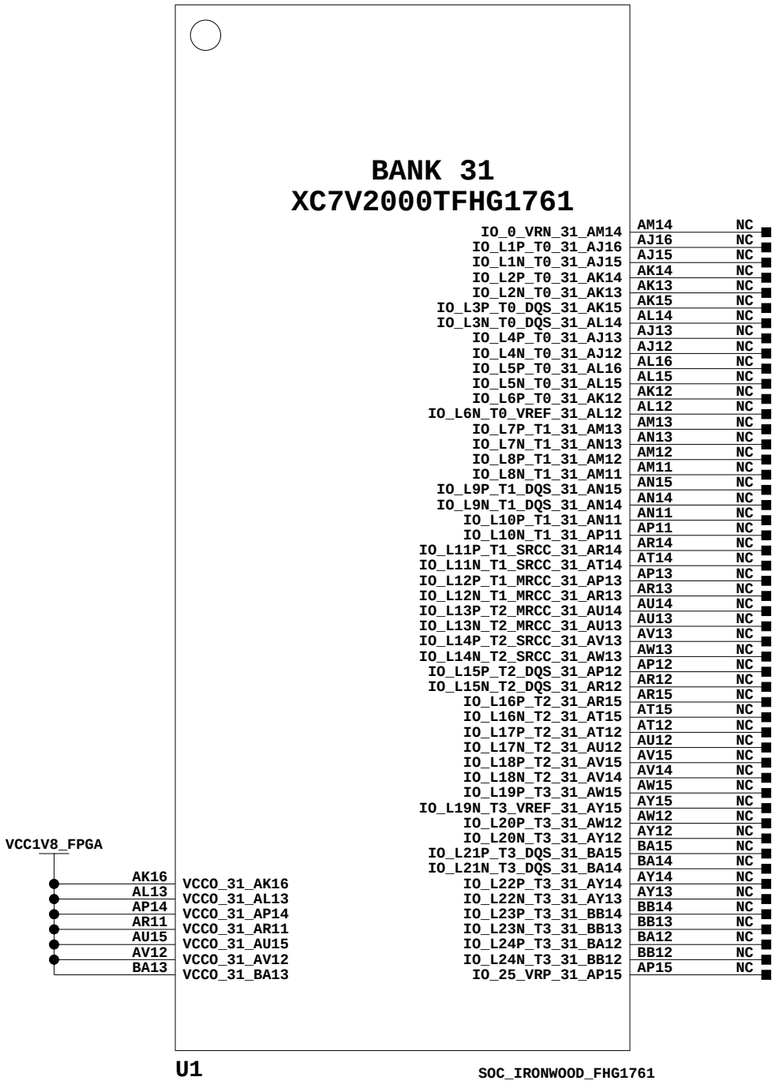
FPGA Banks 12, 32

XILINX

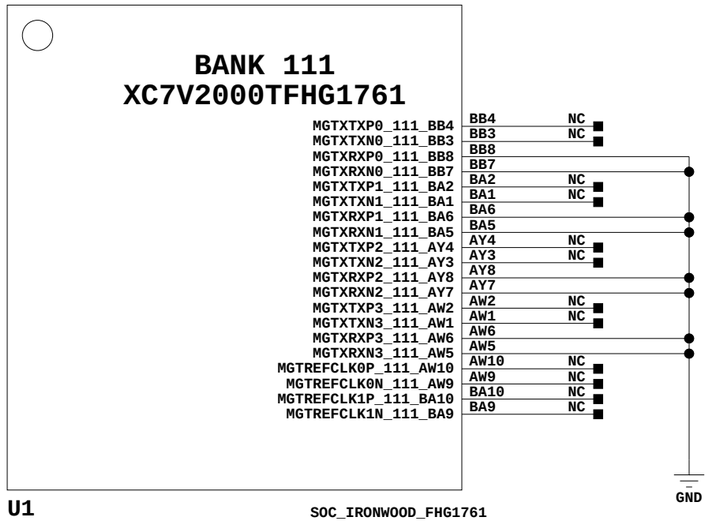
Title:	FPGA Banks 12, 32 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	11 of 57	Drawn By	BF

NOT USED ON 7VX485FFG1761
USED ON 7V585FFG1761

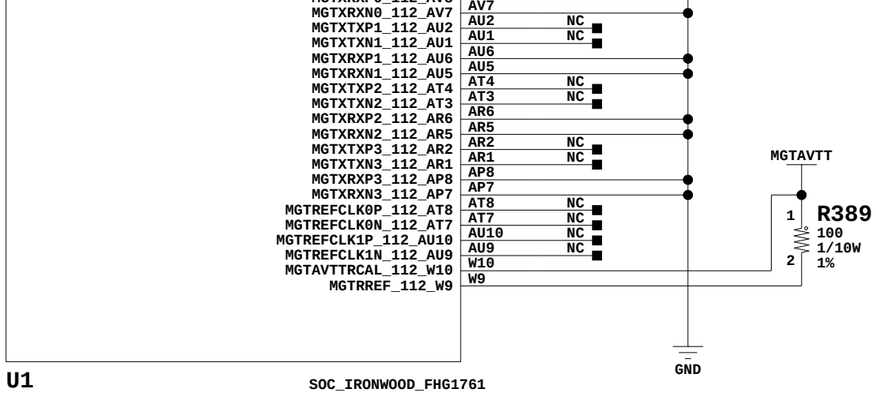
SOC_IRONWOOD_FHG1761



SOC_IRONWOOD_FHG1761



SOC_IRONWOOD_FHG1761



FPGA Bank 31, GT Banks 111, 112

XILINX

Title:	FPGA Bank 31, GT Banks 111, 112 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
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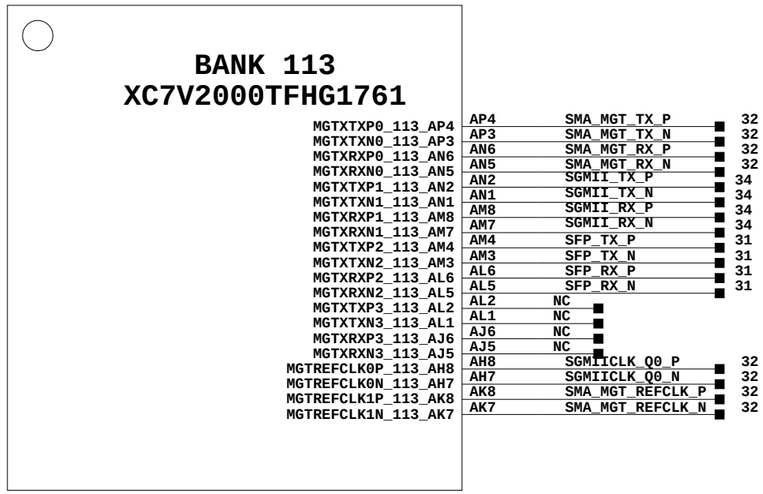

AP4	SMA_MGT_TX_P		32
AP3	SMA_MGT_TX_N		32
AN6	SMA_MGT_RX_P		32
AN5	SMA_MGT_RX_N		32
AN2	SGMII_TX_P		34
AN1	SGMII_TX_N		34
AM8	SGMII_RX_P		34
AM7	SGMII_RX_N		34
AM4	SFP_TX_P		31
AM3	SFP_TX_N		31
AL6	SFP_RX_P		31
AL5	SFP_RX_N		31
AL2	NC		
AL1	NC		
AJ6	NC		
AJ5	NC		
AH8	SGMIICLK_Q0_P		32
AH7	SGMIICLK_Q0_N		32
AK8	SMA_MGT_REFCLK_P		32
AK7	SMA_MGT_REFCLK_N		32

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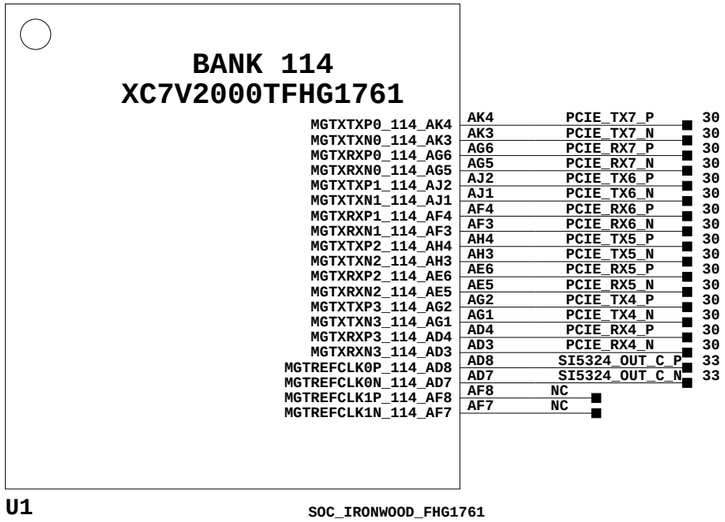
SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761



AK4	PCIE_TX7_P		30
AK3	PCIE_TX7_N		30
AG6	PCIE_RX7_P		30
AG5	PCIE_RX7_N		30
AJ2	PCIE_TX6_P		30
AJ1	PCIE_TX6_N		30
AF4	PCIE_RX6_P		30
AF3	PCIE_RX6_N		30
AH4	PCIE_TX5_P		30
AH3	PCIE_TX5_N		30
AE6	PCIE_RX5_P		30
AE5	PCIE_RX5_N		30
AG2	PCIE_TX4_P		30
AG1	PCIE_TX4_N		30
AD4	PCIE_RX4_P		30
AD3	PCIE_RX4_N		30
AD8	SI5324_OUT_C_P		33
AD7	SI5324_OUT_C_N		33
AF8	NC		
AF7	NC		

U1

SOC_IRONWOOD_FHG1761

FPGA GT Banks 113, 114

XILINX

Title:	FPGA GT Banks 113, 114 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
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SOC_IRONWOOD_FHG1761

BANK 115
XC7V2000TFHG1761

MGTXTXP0_115_AE2	AE2	PCIE_TX3_P	30
MGTXTXN0_115_AE1	AE1	PCIE_TX3_N	30
MGTXRXP0_115_AC6	AC6	PCIE_RX3_P	30
MGTXRXN0_115_AC5	AC5	PCIE_RX3_N	30
MGTXTXP1_115_AC2	AC2	PCIE_TX2_P	30
MGTXTXN1_115_AC1	AC1	PCIE_TX2_N	30
MGTXRXP1_115_AB4	AB4	PCIE_RX2_P	30
MGTXRXN1_115_AB3	AB3	PCIE_RX2_N	30
MGTXTXP2_115_AA2	AA2	PCIE_TX1_P	30
MGTXTXN2_115_AA1	AA1	PCIE_TX1_N	30
MGTXRXP2_115_AA6	AA6	PCIE_RX1_P	30
MGTXRXN2_115_AA5	AA5	PCIE_RX1_N	30
MGTXTXP3_115_W2	W2	PCIE_TX0_P	30
MGTXTXN3_115_W1	W1	PCIE_TX0_N	30
MGTXRXP3_115_Y4	Y4	PCIE_RX0_P	30
MGTXRXN3_115_Y3	Y3	PCIE_RX0_N	30
MGTREFCLK0P_115_Y8	Y8	NC	
MGTREFCLK0N_115_Y7	Y7	NC	
MGTREFCLK1P_115_AB8	AB8	PCIE_CLK_QO_P	30
MGTREFCLK1N_115_AB7	AB7	PCIE_CLK_QO_N	30
MGTAVTTRCAL_115_A12	A12		
MGTRREF_115_B11	B11		

MGTAVTT

R165
100
1/10W
1%

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SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

BANK 116
XC7V2000TFHG1761

MGTXTXP0_116_U2	U2	FMC2_HPC_DP4_C2M_P	26
MGTXTXN0_116_U1	U1	FMC2_HPC_DP4_C2M_N	26
MGTXRXP0_116_W6	W6	FMC2_HPC_DP4_M2C_P	26
MGTXRXN0_116_W5	W5	FMC2_HPC_DP4_M2C_N	26
MGTXTXP1_116_T4	T4	FMC2_HPC_DP5_C2M_P	26
MGTXTXN1_116_T3	T3	FMC2_HPC_DP5_C2M_N	26
MGTXRXP1_116_V4	V4	FMC2_HPC_DP5_M2C_P	26
MGTXRXN1_116_V3	V3	FMC2_HPC_DP5_M2C_N	26
MGTXTXP2_116_R2	R2	FMC2_HPC_DP6_C2M_P	26
MGTXTXN2_116_R1	R1	FMC2_HPC_DP6_C2M_N	26
MGTXRXP2_116_U6	U6	FMC2_HPC_DP6_M2C_P	26
MGTXRXN2_116_U5	U5	FMC2_HPC_DP6_M2C_N	26
MGTXTXP3_116_P4	P4	FMC2_HPC_DP7_C2M_P	26
MGTXTXN3_116_P3	P3	FMC2_HPC_DP7_C2M_N	26
MGTXRXP3_116_R6	R6	FMC2_HPC_DP7_M2C_P	26
MGTXRXN3_116_R5	R5	FMC2_HPC_DP7_M2C_N	26
MGTREFCLK0P_116_T8	T8	FMC2_HPC_GBTCLK1_M2C_C_P	14
MGTREFCLK0N_116_T7	T7	FMC2_HPC_GBTCLK1_M2C_C_N	14
MGTREFCLK1P_116_V8	V8	NC	
MGTREFCLK1N_116_V7	V7	NC	

U1

SOC_IRONWOOD_FHG1761

C395
0.1UF
25V
X5R

C396
0.1UF
25V
X5R

26	FMC2_HPC_GBTCLK1_M2C_P	FMC2_HPC_GBTCLK1_M2C_C_P	14
26	FMC2_HPC_GBTCLK1_M2C_N	FMC2_HPC_GBTCLK1_M2C_C_N	14

FPGA GT Banks 115, 116

XILINX

Title:	FPGA GT Banks 115, 116 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
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Sheet	14 of 57	Drawn By	BF

SOC_IRONWOOD_FHG1761

BANK 118
XC7V2000TFHG1761

MGTXTXP0_118_J2	J2	FMC1_HPC_DP4_C2M_P	22
MGTXTXN0_118_J1	J1	FMC1_HPC_DP4_C2M_N	22
MGTXRXP0_118_H8	H8	FMC1_HPC_DP4_M2C_P	22
MGTXRXN0_118_H7	H7	FMC1_HPC_DP4_M2C_N	22
MGTXTXP1_118_H4	H4	FMC1_HPC_DP5_C2M_P	22
MGTXTXN1_118_H3	H3	FMC1_HPC_DP5_C2M_N	22
MGTXRXP1_118_G6	G6	FMC1_HPC_DP5_M2C_P	22
MGTXRXN1_118_G5	G5	FMC1_HPC_DP5_M2C_N	22
MGTXTXP2_118_G2	G2	FMC1_HPC_DP6_C2M_P	22
MGTXTXN2_118_G1	G1	FMC1_HPC_DP6_C2M_N	22
MGTXRXP2_118_F8	F8	FMC1_HPC_DP6_M2C_P	22
MGTXRXN2_118_F7	F7	FMC1_HPC_DP6_M2C_N	22
MGTXTXP3_118_F4	F4	FMC1_HPC_DP7_C2M_P	22
MGTXTXN3_118_F3	F3	FMC1_HPC_DP7_C2M_N	22
MGTXRXP3_118_E6	E6	FMC1_HPC_DP7_M2C_P	22
MGTXRXN3_118_E5	E5	FMC1_HPC_DP7_M2C_N	22
MGTREFCLK0P_118_E10	E10	FMC1_HPC_GBTCLK1_M2C_C_P	15
MGTREFCLK0N_118_E9	E9	FMC1_HPC_GBTCLK1_M2C_C_N	15
MGTREFCLK1P_118_G10	G10	NC	
MGTREFCLK1N_118_G9	G9	NC	
MGTAVTTRCAL_118_AC10	AC10		
MGTRREF_118_AC9	AC9		

MGTAVTT

R390 100 1/10W 1%

U1

SOC_IRONWOOD_FHG1761

22 FMC1_HPC_GBTCLK1_M2C_P — C393 0.1UF 25V X5R — FMC1_HPC_GBTCLK1_M2C_C_P 15

22 FMC1_HPC_GBTCLK1_M2C_N — C394 0.1UF 25V X5R — FMC1_HPC_GBTCLK1_M2C_C_N 15

SOC_IRONWOOD_FHG1761

BANK 117
XC7V2000TFHG1761

MGTXTXP0_117_N2	N2	FMC2_HPC_DP0_C2M_P	26
MGTXTXN0_117_N1	N1	FMC2_HPC_DP0_C2M_N	26
MGTXRXP0_117_P8	P8	FMC2_HPC_DP0_M2C_P	26
MGTXRXN0_117_P7	P7	FMC2_HPC_DP0_M2C_N	26
MGTXTXP1_117_M4	M4	FMC2_HPC_DP1_C2M_P	26
MGTXTXN1_117_M3	M3	FMC2_HPC_DP1_C2M_N	26
MGTXRXP1_117_N6	N6	FMC2_HPC_DP1_M2C_P	26
MGTXRXN1_117_N5	N5	FMC2_HPC_DP1_M2C_N	26
MGTXTXP2_117_L2	L2	FMC2_HPC_DP2_C2M_P	26
MGTXTXN2_117_L1	L1	FMC2_HPC_DP2_C2M_N	26
MGTXRXP2_117_L6	L6	FMC2_HPC_DP2_M2C_P	26
MGTXRXN2_117_L5	L5	FMC2_HPC_DP2_M2C_N	26
MGTXTXP3_117_K4	K4	FMC2_HPC_DP3_C2M_P	26
MGTXTXN3_117_K3	K3	FMC2_HPC_DP3_C2M_N	26
MGTXRXP3_117_J6	J6	FMC2_HPC_DP3_M2C_P	26
MGTXRXN3_117_J5	J5	FMC2_HPC_DP3_M2C_N	26
MGTREFCLK0P_117_K8	K8	FMC2_HPC_GBTCLK0_M2C_C_P	15
MGTREFCLK0N_117_K7	K7	FMC2_HPC_GBTCLK0_M2C_C_N	15
MGTREFCLK1P_117_M8	M8	NC	
MGTREFCLK1N_117_M7	M7	NC	

U1

SOC_IRONWOOD_FHG1761

26 FMC2_HPC_GBTCLK0_M2C_P — C3 0.1UF 25V X5R — C4 0.1UF 25V X5R — FMC2_HPC_GBTCLK0_M2C_C_P 15

26 FMC2_HPC_GBTCLK0_M2C_N — FMC2_HPC_GBTCLK0_M2C_C_N 15

SOC_IRONWOOD_FHG1761

BANK 119
XC7V2000TFHG1761

MGTXTXP0_119_E2	E2	FMC1_HPC_DP0_C2M_P	22
MGTXTXN0_119_E1	E1	FMC1_HPC_DP0_C2M_N	22
MGTXRXP0_119_D8	D8	FMC1_HPC_DP0_M2C_P	22
MGTXRXN0_119_D7	D7	FMC1_HPC_DP0_M2C_N	22
MGTXTXP1_119_D4	D4	FMC1_HPC_DP1_C2M_P	22
MGTXTXN1_119_D3	D3	FMC1_HPC_DP1_C2M_N	22
MGTXRXP1_119_C6	C6	FMC1_HPC_DP1_M2C_P	22
MGTXRXN1_119_C5	C5	FMC1_HPC_DP1_M2C_N	22
MGTXTXP2_119_C2	C2	FMC1_HPC_DP2_C2M_P	22
MGTXTXN2_119_C1	C1	FMC1_HPC_DP2_C2M_N	22
MGTXRXP2_119_B8	B8	FMC1_HPC_DP2_M2C_P	22
MGTXRXN2_119_B7	B7	FMC1_HPC_DP2_M2C_N	22
MGTXTXP3_119_B4	B4	FMC1_HPC_DP3_C2M_P	22
MGTXTXN3_119_B3	B3	FMC1_HPC_DP3_C2M_N	22
MGTXRXP3_119_A6	A6	FMC1_HPC_DP3_M2C_P	22
MGTXRXN3_119_A5	A5	FMC1_HPC_DP3_M2C_N	22
MGTREFCLK0P_119_A10	A10	FMC1_HPC_GBTCLK0_M2C_C_P	15
MGTREFCLK0N_119_A9	A9	FMC1_HPC_GBTCLK0_M2C_C_N	15
MGTREFCLK1P_119_C10	C10	NC	
MGTREFCLK1N_119_C9	C9	NC	

U1

SOC_IRONWOOD_FHG1761

22 FMC1_HPC_GBTCLK0_M2C_P — C6 0.1UF 25V X5R — C5 0.1UF 25V X5R — FMC1_HPC_GBTCLK0_M2C_C_P 15

22 FMC1_HPC_GBTCLK0_M2C_N — FMC1_HPC_GBTCLK0_M2C_C_N 15

FPGA GT Banks 117, 118, 119

XILINX

Title:	FPGA GT Banks 117, 118, 119 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
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SOC_IRONWOOD_FHG1761

BANK VCCINT
XC7V2000TFHG1761

VCCINT_FPGA

VCCINT_Y27	Y27
VCCINT_Y23	Y23
VCCINT_Y19	Y19
VCCINT_Y15	Y15
VCCINT_Y13	Y13
VCCINT_Y11	Y11
VCCINT_W28	W28
VCCINT_W24	W24
VCCINT_W20	W20
VCCINT_W16	W16
VCCINT_W14	W14
VCCINT_W12	W12
VCCINT_V27	V27
VCCINT_V23	V23
VCCINT_V21	V21
VCCINT_V19	V19
VCCINT_V15	V15
VCCINT_V13	V13
VCCINT_V11	V11
VCCINT_U24	U24
VCCINT_U20	U20
VCCINT_U16	U16
VCCINT_U14	U14
VCCINT_U12	U12
VCCINT_T27	T27
VCCINT_T23	T23
VCCINT_T21	T21
VCCINT_T15	T15
VCCINT_T13	T13
VCCINT_R24	R24
VCCINT_R20	R20
VCCINT_R16	R16
VCCINT_R14	R14
VCCINT_R12	R12
VCCINT_P27	P27
VCCINT_P15	P15
VCCINT_P13	P13
VCCINT_AH27	AH27
VCCINT_AH23	AH23
VCCINT_AH19	AH19
VCCINT_AH15	AH15
VCCINT_AH13	AH13
VCCINT_AH11	AH11
VCCINT_AG28	AG28
VCCINT_AG24	AG24
VCCINT_AG20	AG20
VCCINT_AG16	AG16
VCCINT_AG14	AG14
VCCINT_AG12	AG12
VCCINT_AF27	AF27
VCCINT_AF23	AF23
VCCINT_AF21	AF21
VCCINT_AF15	AF15
VCCINT_AF13	AF13
VCCINT_AF11	AF11
VCCINT_AE28	AE28
VCCINT_AE24	AE24
VCCINT_AE20	AE20
VCCINT_AE16	AE16
VCCINT_AE14	AE14
VCCINT_AE12	AE12
VCCINT_AE10	AE10
VCCINT_AD27	AD27
VCCINT_AD23	AD23
VCCINT_AD21	AD21
VCCINT_AD19	AD19
VCCINT_AD15	AD15
VCCINT_AD13	AD13
VCCINT_AD11	AD11
VCCINT_AC28	AC28
VCCINT_AC24	AC24
VCCINT_AC16	AC16
VCCINT_AC14	AC14
VCCINT_AC12	AC12
VCCINT_AB27	AB27
VCCINT_AB23	AB23
VCCINT_AB19	AB19
VCCINT_AB15	AB15
VCCINT_AB13	AB13
VCCINT_AB11	AB11
VCCINT_AA28	AA28
VCCINT_AA24	AA24
VCCINT_AA16	AA16
VCCINT_AA14	AA14
VCCINT_AA12	AA12
VCCINT_AA10	AA10

U1 SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

BANK VCCAUX
XC7V2000TFHG1761

VCCAUX

VCCAUX_Y17	Y17
VCCAUX_W26	W26
VCCAUX_V17	V17
VCCAUX_U26	U26
VCCAUX_T17	T17
VCCAUX_AG26	AG26
VCCAUX_AF17	AF17
VCCAUX_AE26	AE26
VCCAUX_AD17	AD17
VCCAUX_AC26	AC26
VCCAUX_AB17	AB17
VCCAUX_AA26	AA26

U1 SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

BANK VCCAUX_IO_G0
XC7V2000TFHG1761

VCCAUX_IO

VCCAUX_IO_G0_AF25	AF25
VCCAUX_IO_G0_AH25	AH25

U1 SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

BANK VCCAUX_IO_G1
XC7V2000TFHG1761

VCCAUX_IO

VCCAUX_IO_G1_Y25	Y25
VCCAUX_IO_G1_AB25	AB25
VCCAUX_IO_G1_AD25	AD25

U1 SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

BANK VCCAUX_IO_G2
XC7V2000TFHG1761

VCCAUX_IO

VCCAUX_IO_G2_R26	R26
VCCAUX_IO_G2_T25	T25
VCCAUX_IO_G2_V25	V25

U1 SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

BANK VCCAUX_IO_G3
XC7V2000TFHG1761

VCCAUX_IO

VCCAUX_IO_G3_AE18	AE18
VCCAUX_IO_G3_AF19	AF19
VCCAUX_IO_G3_AG18	AG18

U1 SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

BANK VCCAUX_IO_G4
XC7V2000TFHG1761

VCCAUX_IO

VCCAUX_IO_G4_W18	W18
VCCAUX_IO_G4_AA18	AA18
VCCAUX_IO_G4_AC18	AC18

U1 SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

BANK VCCAUX_IO_G5
XC7V2000TFHG1761

VCCAUX_IO

VCCAUX_IO_G5_R18	R18
VCCAUX_IO_G5_T19	T19
VCCAUX_IO_G5_U18	U18

U1 SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

BANK VCCBRAM
XC7V2000TFHG1761

VCCBRAM

VCCBRAM_W22	W22
VCCBRAM_U22	U22
VCCBRAM_R22	R22
VCCBRAM_AH21	AH21
VCCBRAM_AG22	AG22
VCCBRAM_AE22	AE22
VCCBRAM_AC22	AC22
VCCBRAM_AA22	AA22

U1 SOC_IRONWOOD_FHG1761

FPGA Power Pins

XILINX

Title:	FPGA Power Pins SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
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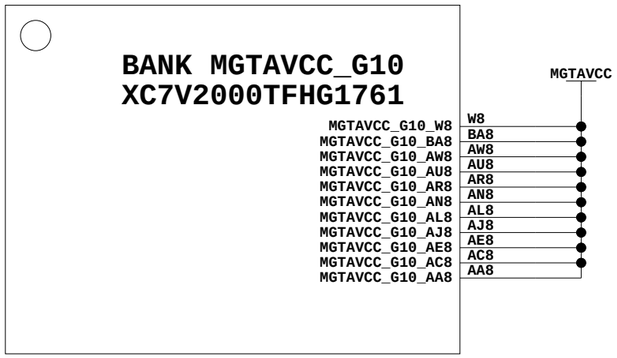
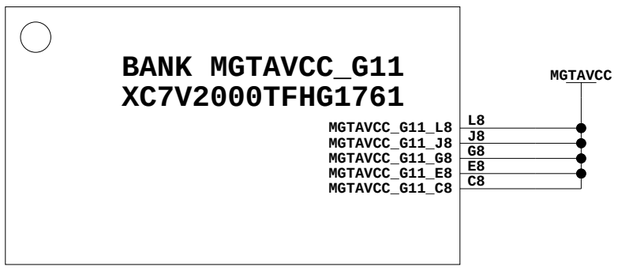
SOC_IRONWOOD_FHG1761



U1

SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761



U1

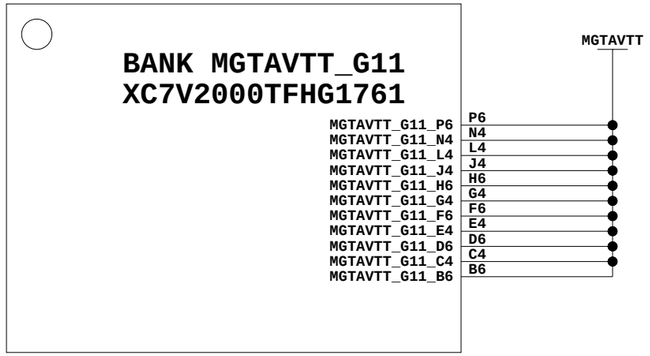
SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

U1

SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761



U1

SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

U1

SOC_IRONWOOD_FHG1761

SOC_IRONWOOD_FHG1761

U1

SOC_IRONWOOD_FHG1761

FPGA Power Pins

Title:	FPGA Power Pins SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM		ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
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FPGA GND

XILINX

Title:	FPGA GND SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
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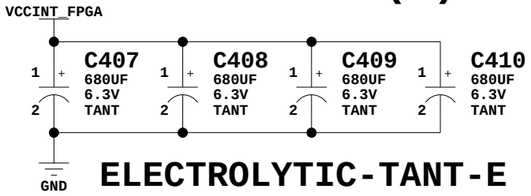
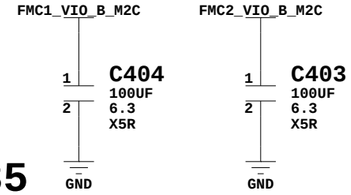
BYPASS CAPACITORS

VCCINT 680uF (4)

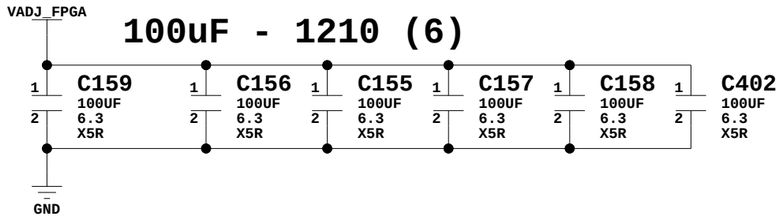


ELECTROLYTIC-TANT-E

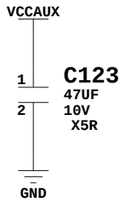
Banks 32, 36 FMC_VIO_B VCCO
100uF - 1210 (2)



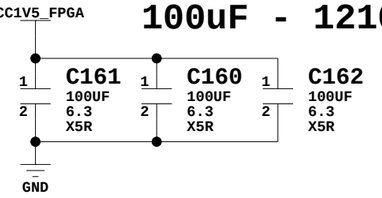
Banks 16, 17, 18, 19, 34, 35 VADJ VCCO
100uF - 1210 (6)



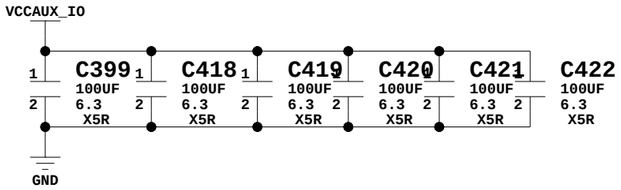
VCCAUX
47uF - 1210 (1)



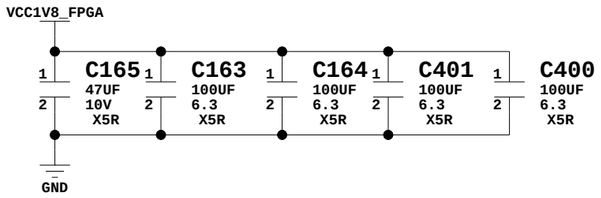
Banks 37, 38, 39 1.5V VCCO
100uF - 1210 (3)



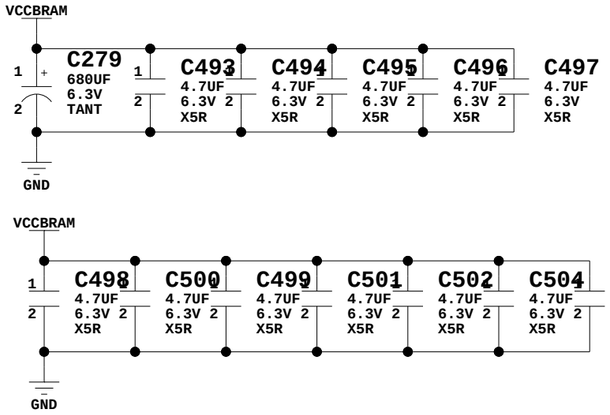
VCCAUX_IO 100uF - 1210 (6)

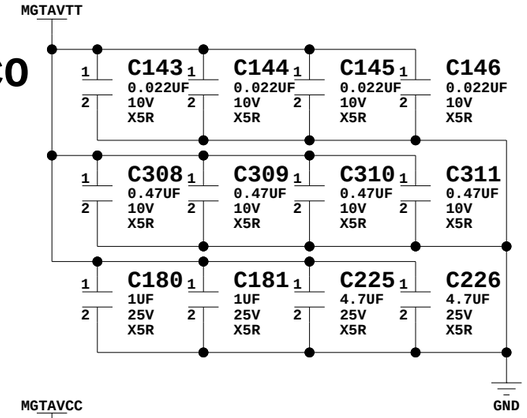


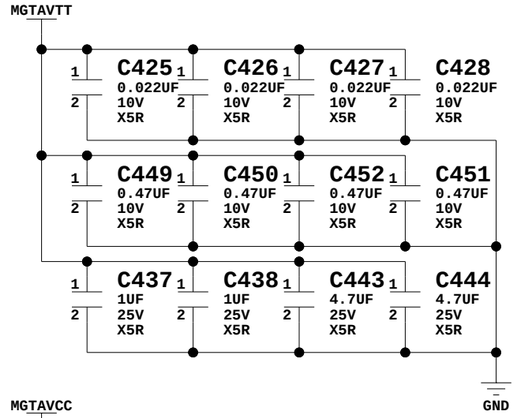
Bank 0, 13, 14, 15, 33 1.8V VCCO
100uF - 1210 (1)

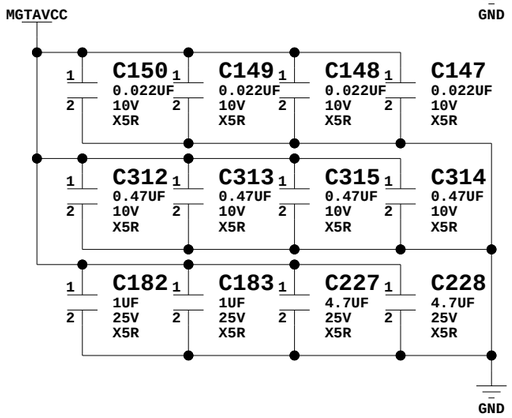


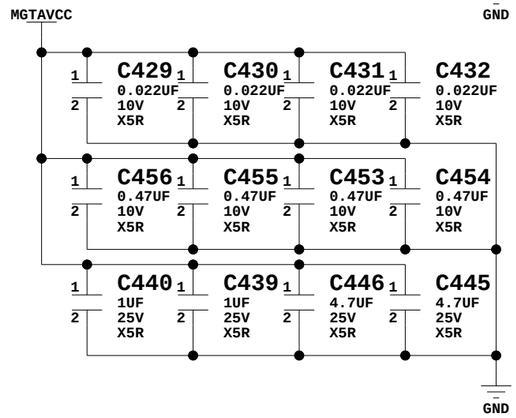
VCCBRAM
330uF (2), 4.7uf (12)

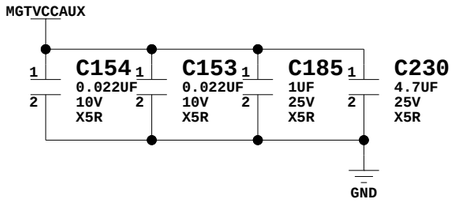


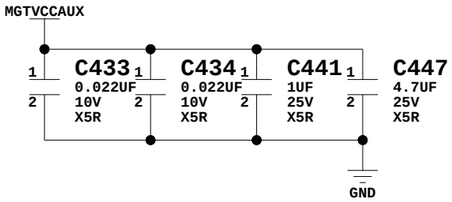








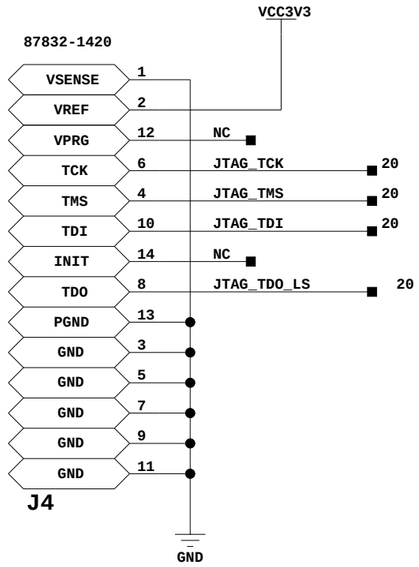


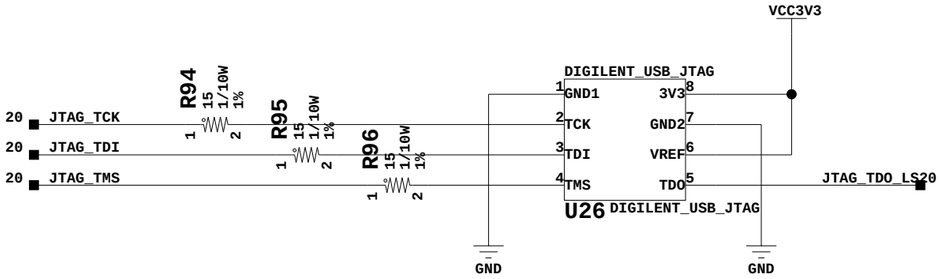


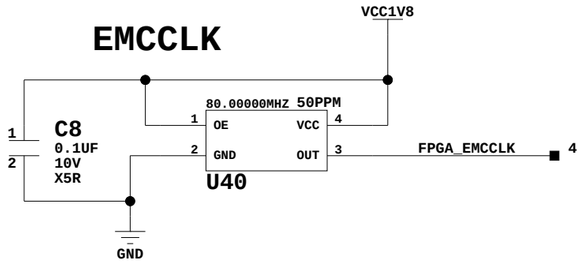
FPGA Bypass Capacitors

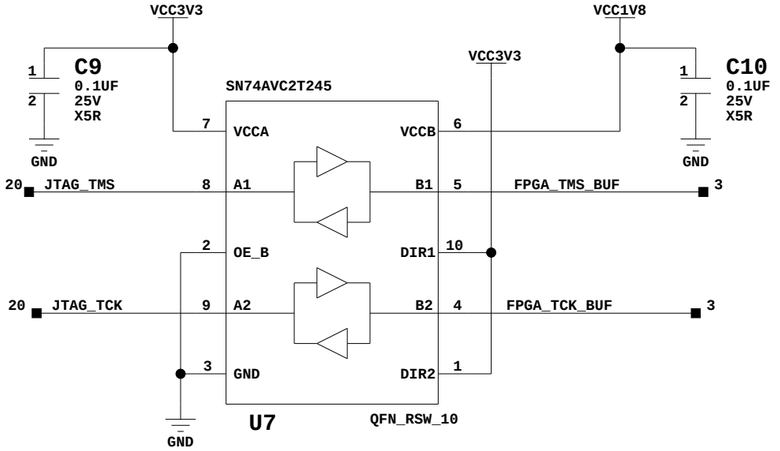
XILINX

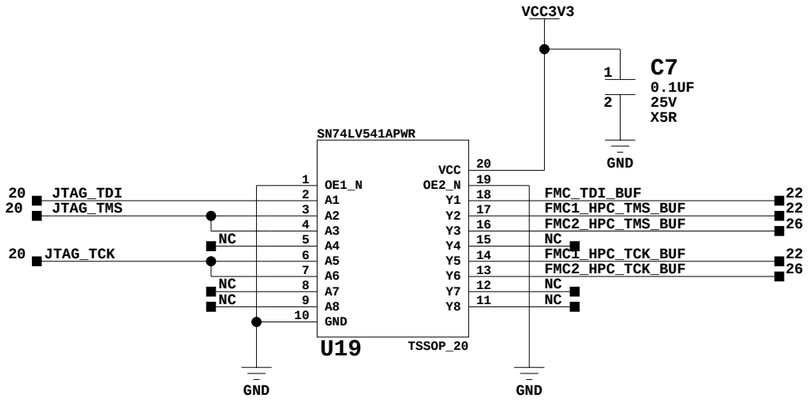
Title:	FPGA Bypass Capacitors SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	19 of 57	Drawn By	BF

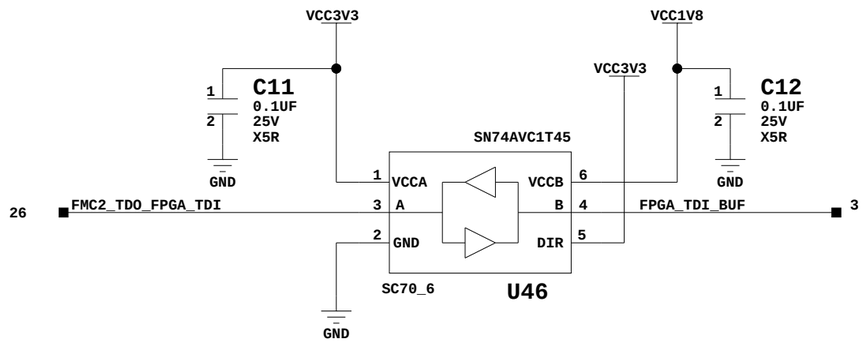


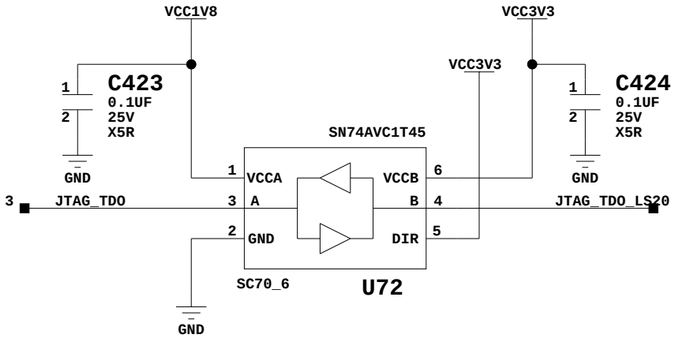








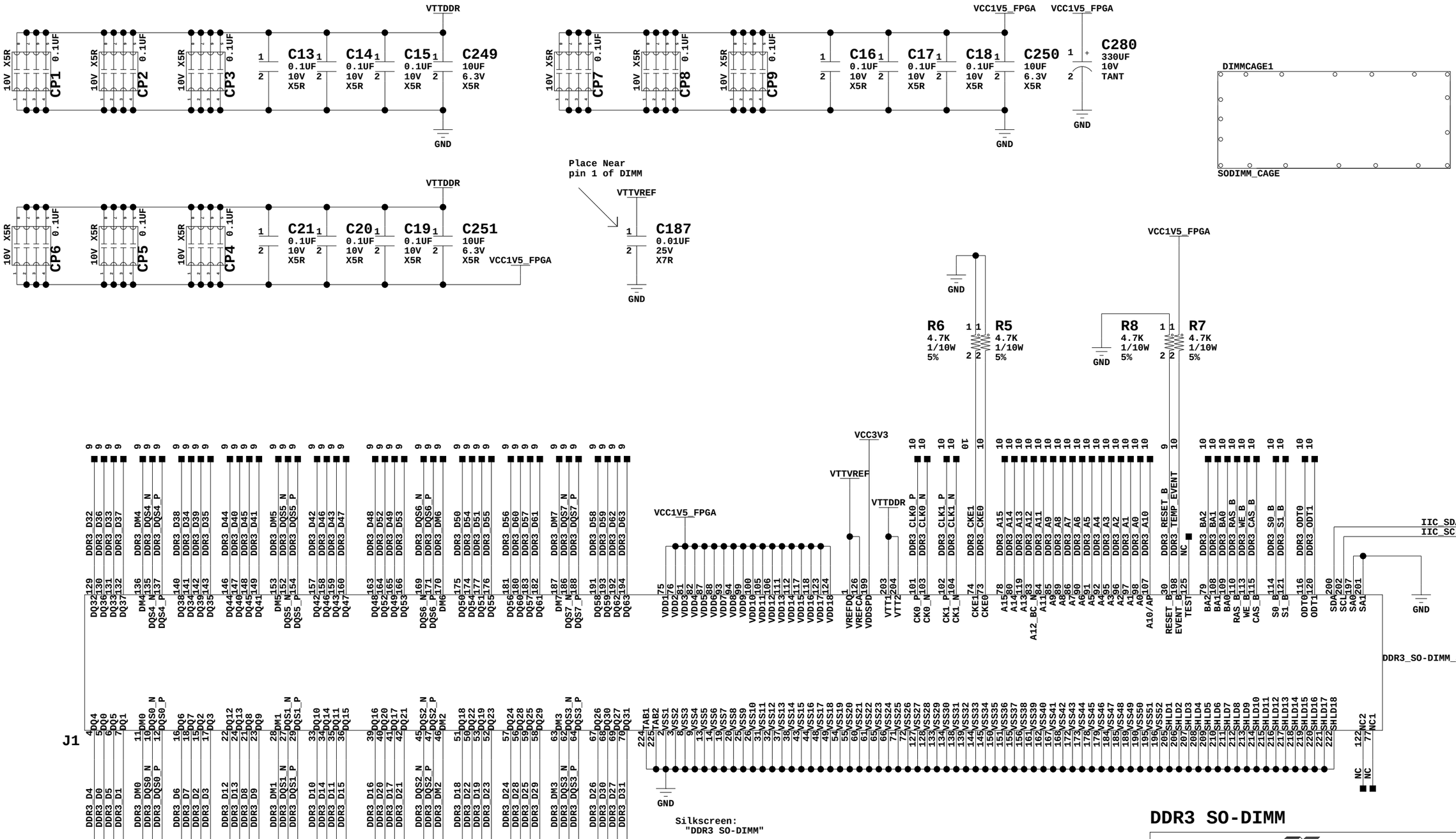




JTAG Buffer, USB JTAG Module, JTAG Hdr

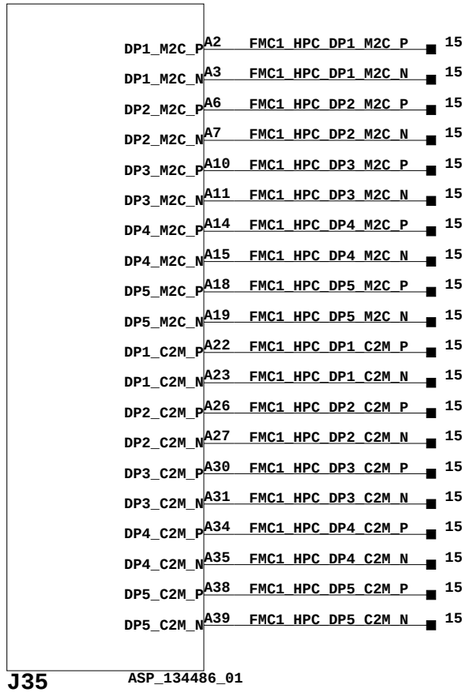
XILINX

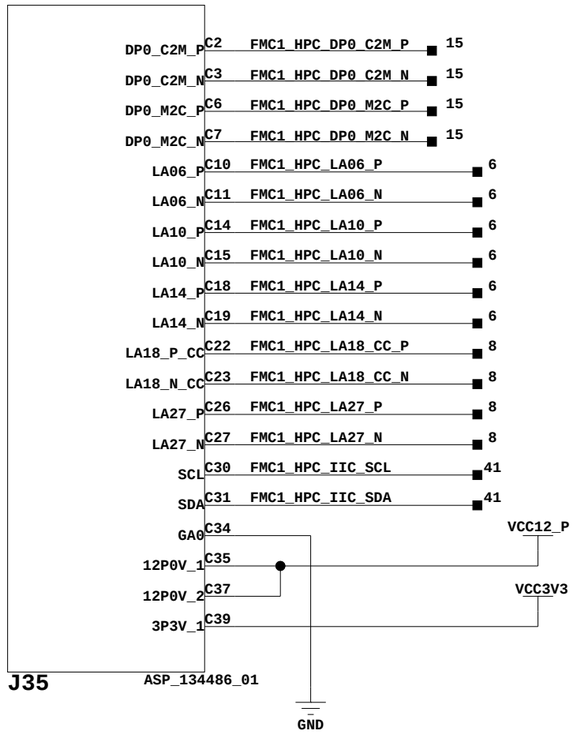
Title:	JTAG Buffer, USB JTAG Module, JTAG Hdr SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	20 of 57	Drawn By	BF

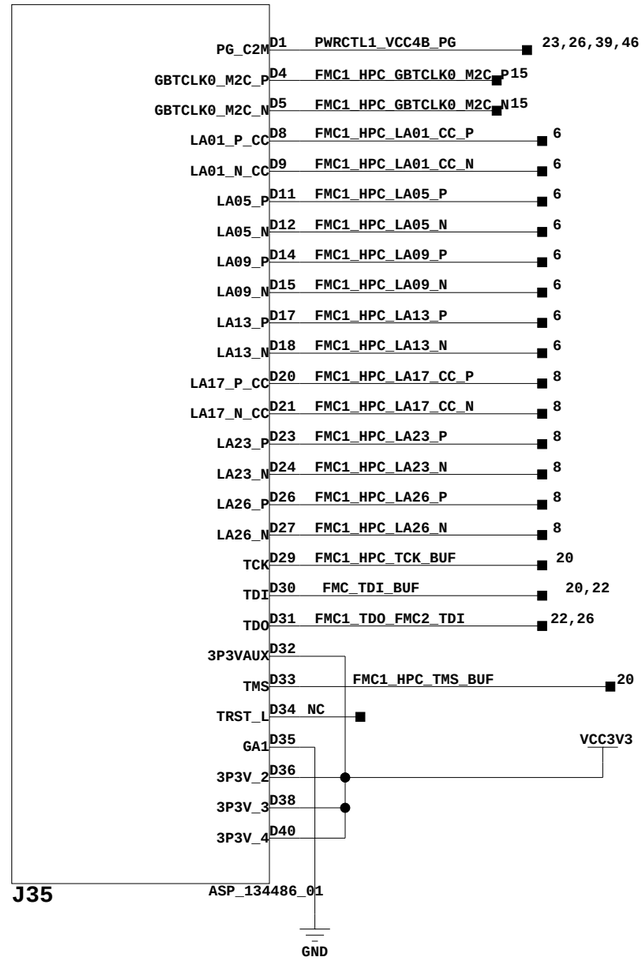


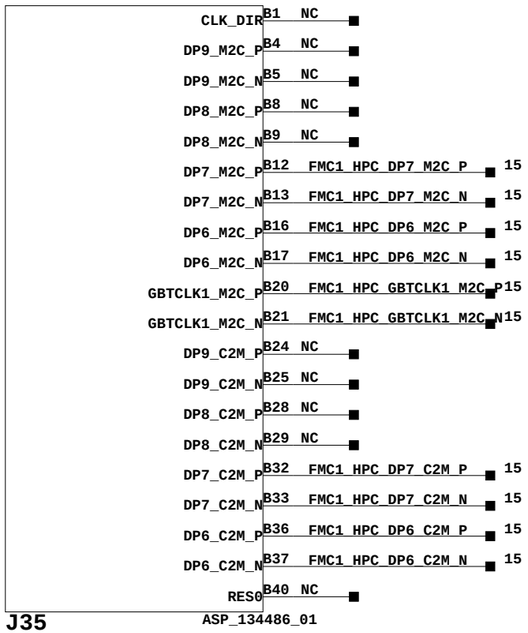
DDR3 SO-DIMM

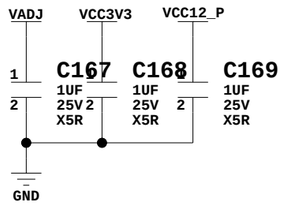
Title:	DDR3 SO-DIMM SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N:	0431663
		PCB P/N:	1280586
		SCH P/N:	0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	21 of 57	Drawn By	BF

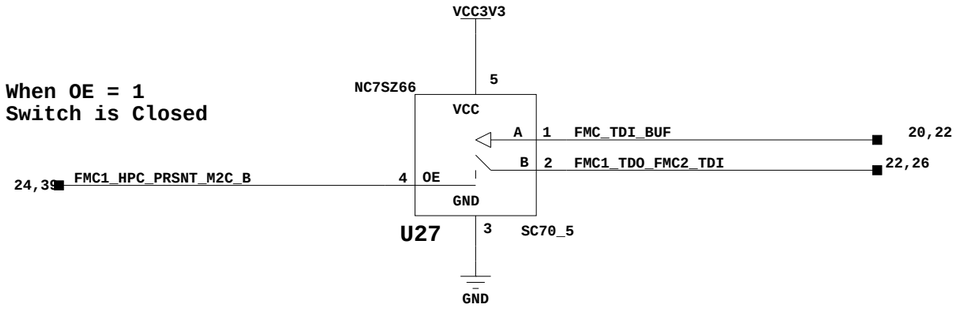








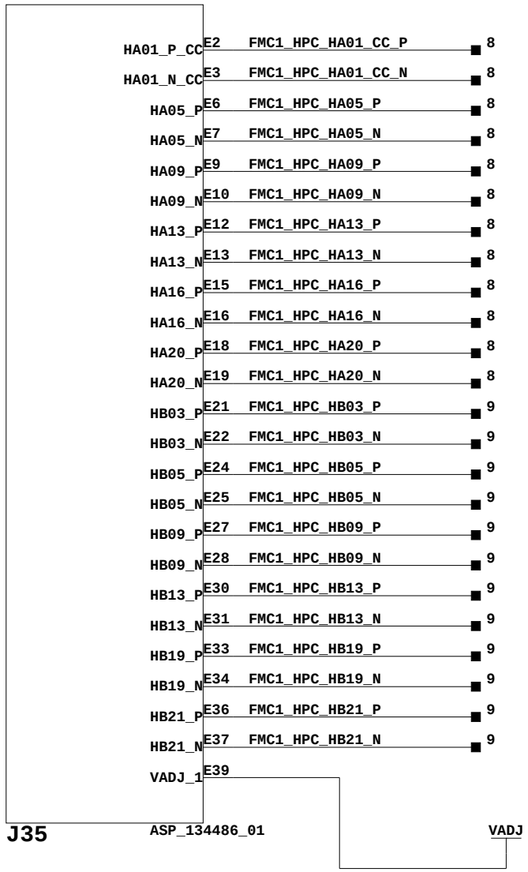


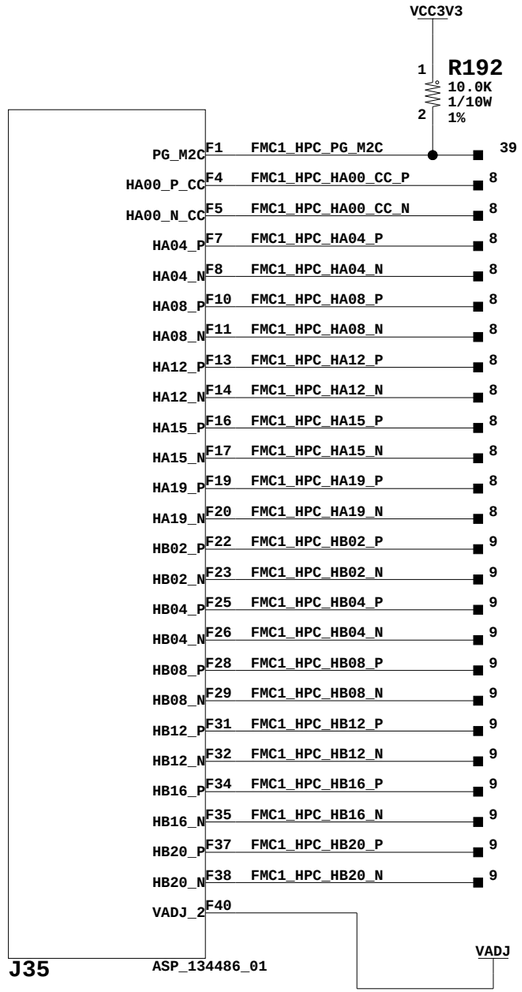


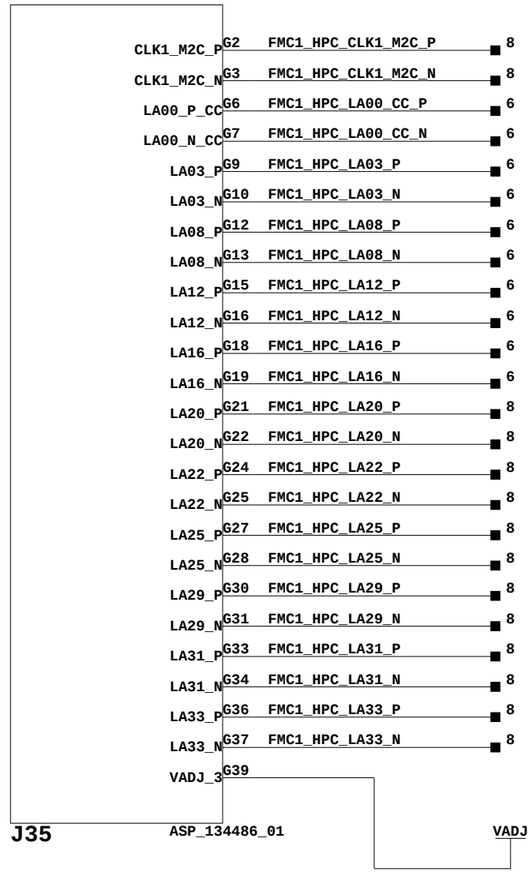
ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows A, B, C, D

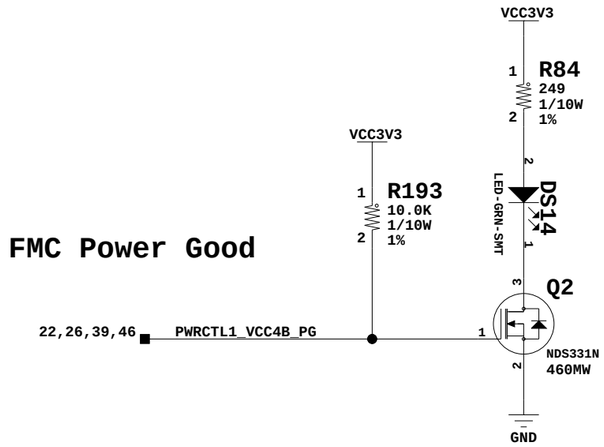
XILINX

Title:	FMC 1 HPC Header, Rows A, B, C, D SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	22 of 57	Drawn By	BF





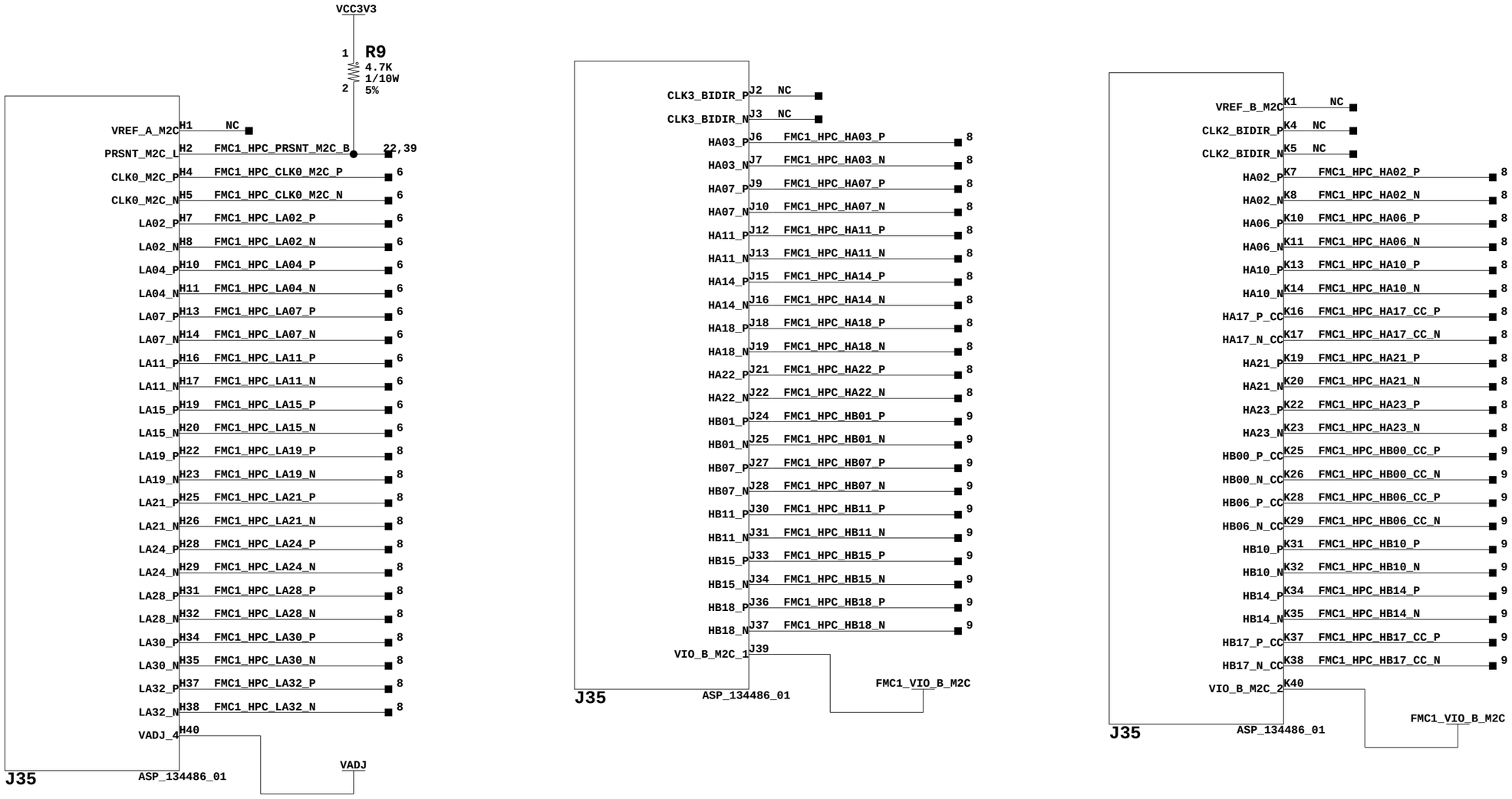




ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows E, F, G

XILINX

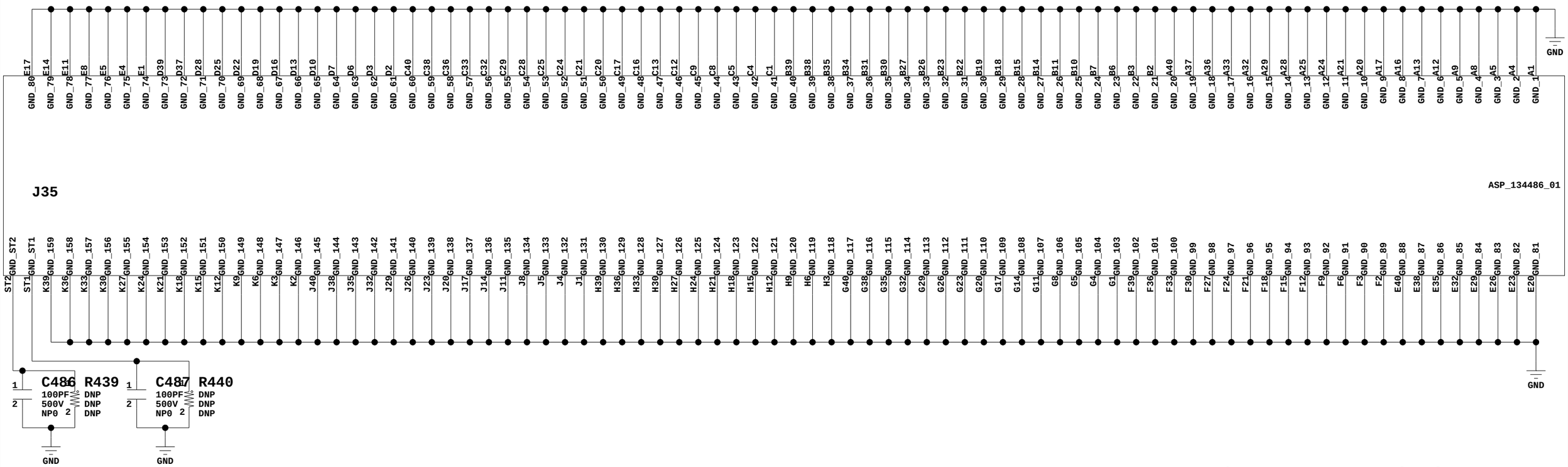
Title:	FMC 1 HPC Header, Rows E, F, G SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	23 of 57	Drawn By	BF



ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, Rows H, J, K

XILINX

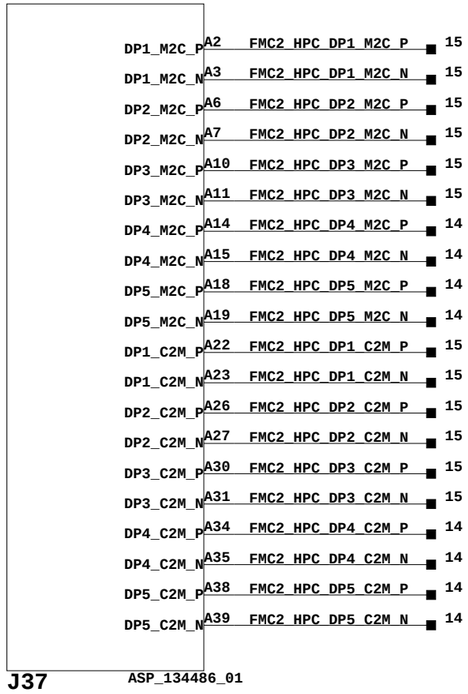
Title:	FMC 1 HPC Header, Rows H, J, K SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	24 of 57	Drawn By	BF

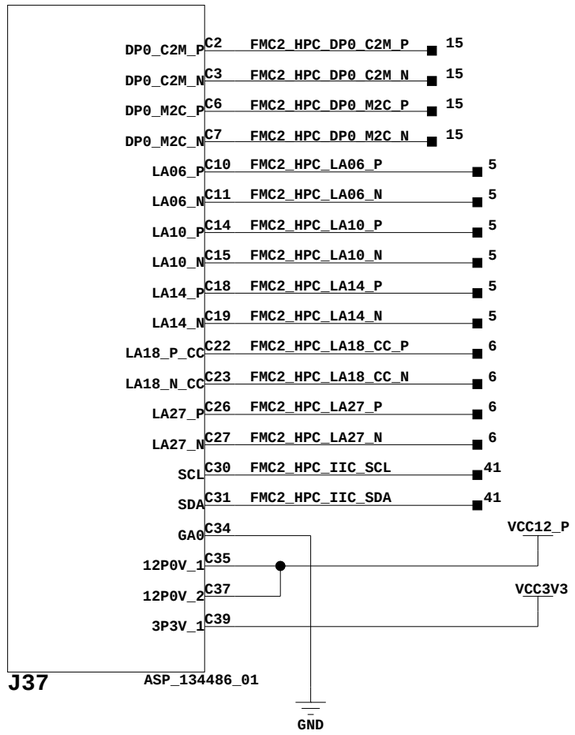


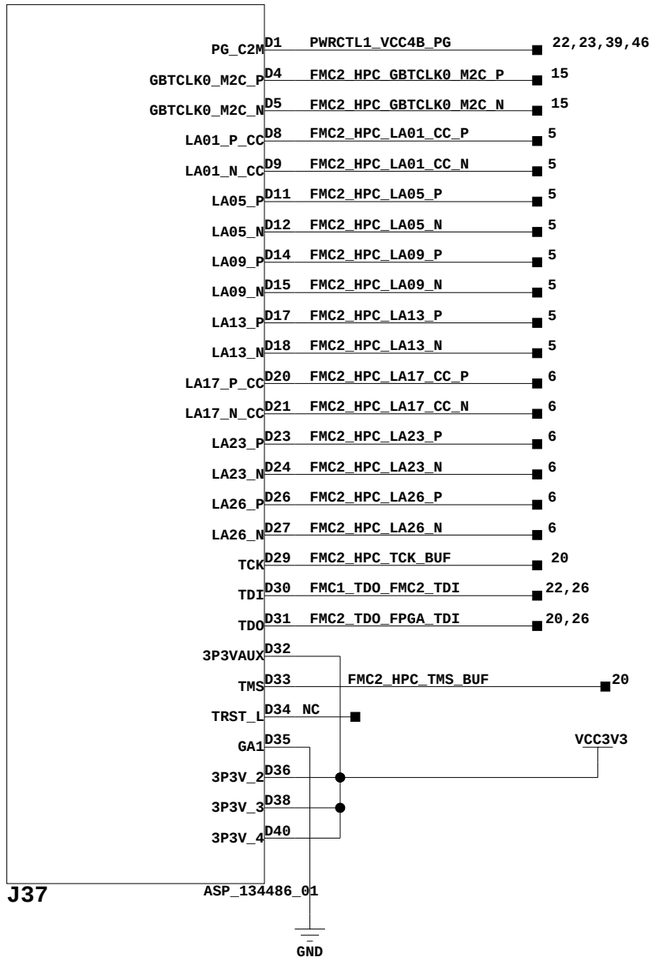
ANSI/VITA 57.1 - Revised 2010
FMC 1 HPC Header, GND

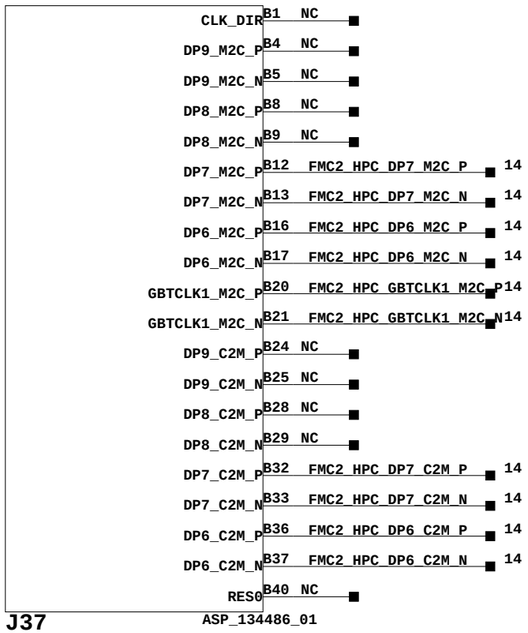
XILINX

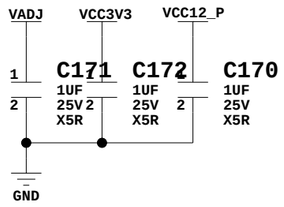
Title:	FMC 1 HPC Header, GND SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	25 of 57	Drawn By	BF

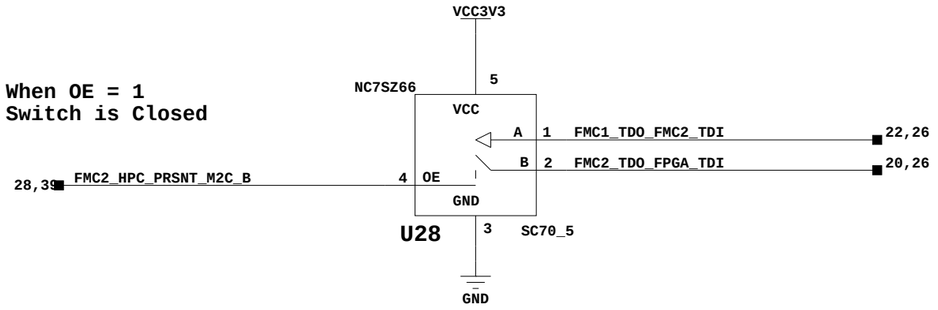








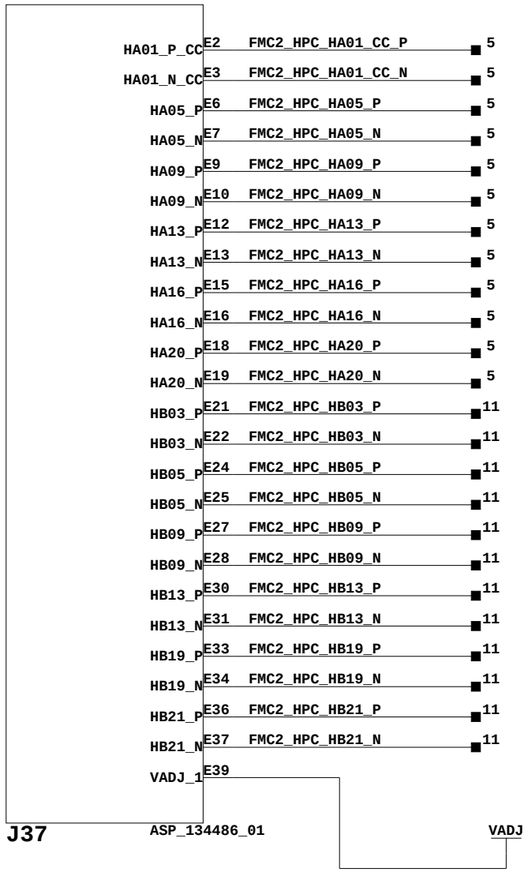


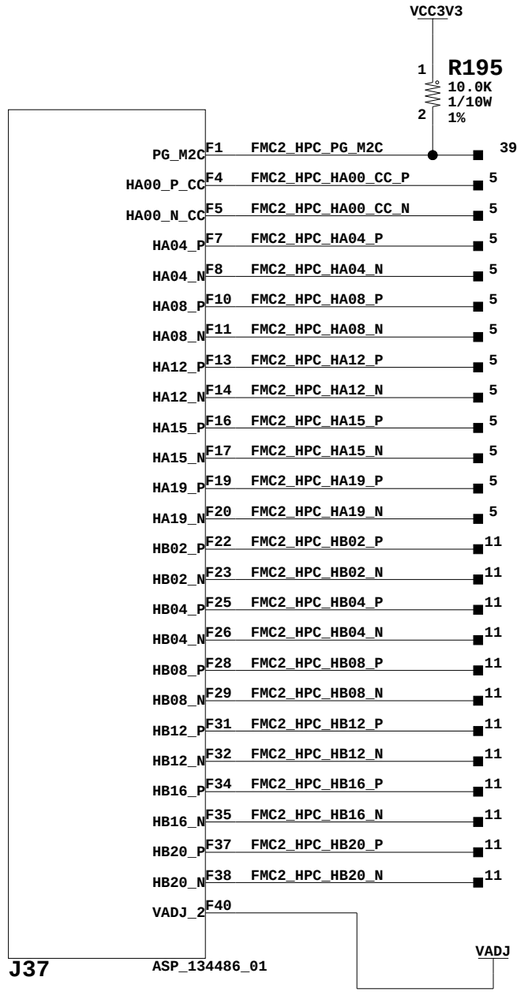


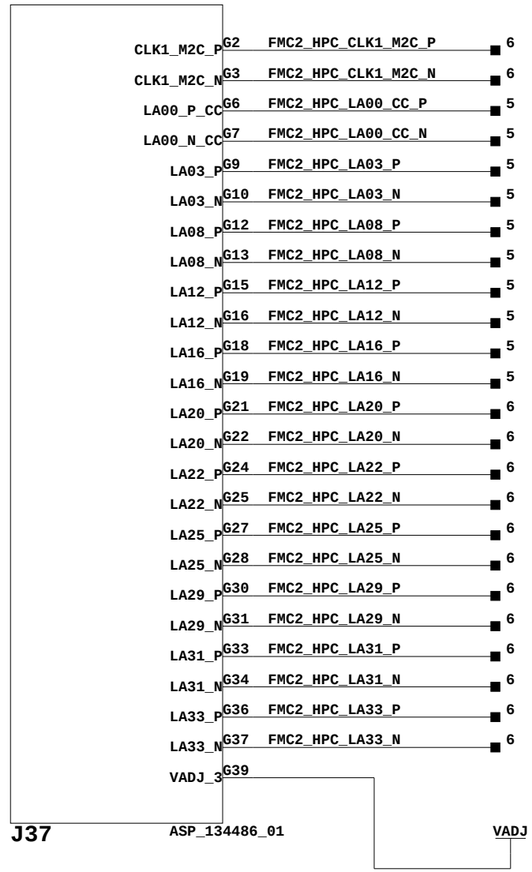
ANSI/VITA 57.1 - Revised 2010
FMC 2 HPC Header, Rows A, B, C, D

XILINX

Title:	FMC 2 HPC Header, Rows A, B, C, D SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N:	0431663
		PCB P/N:	1280586
		SCH P/N:	0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	26 of 57	Drawn By	BF



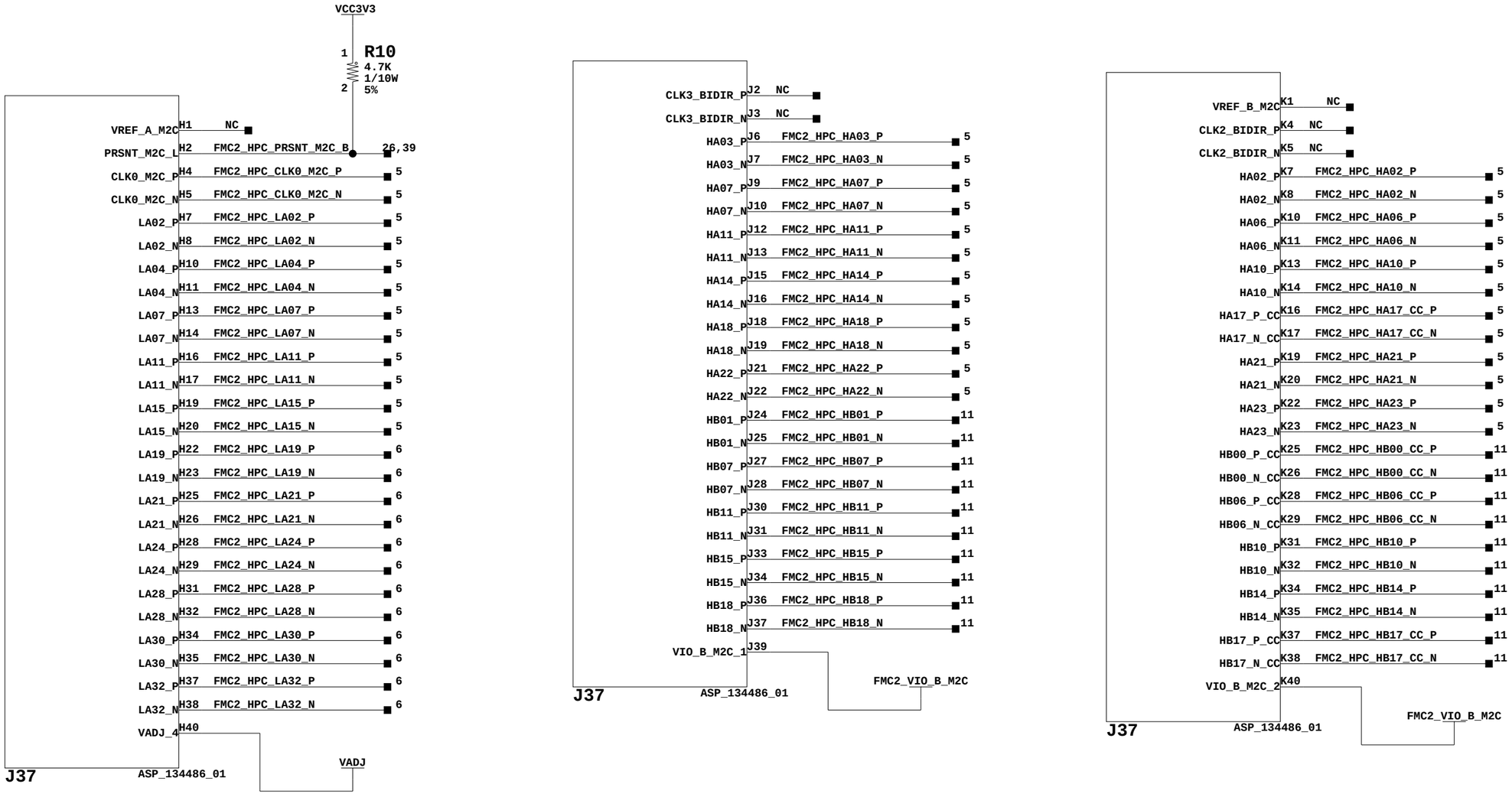




ANSI/VITA 57.1 - Revised 2010
FMC 2 HPC Header, Rows E, F, G

XILINX

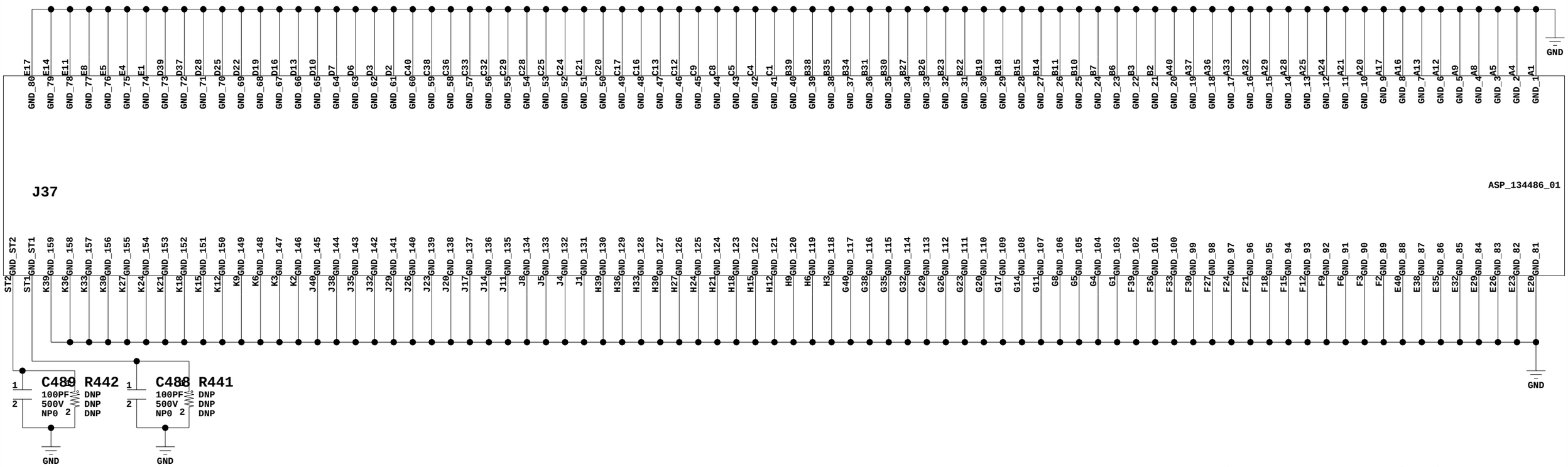
Title:	FMC 2 HPC Header, Rows E, F, G SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	27 of 57	Drawn By	BF



ANSI/VITA 57.1 - Revised 2010
FMC 2 HPC Header, Rows H, J, K

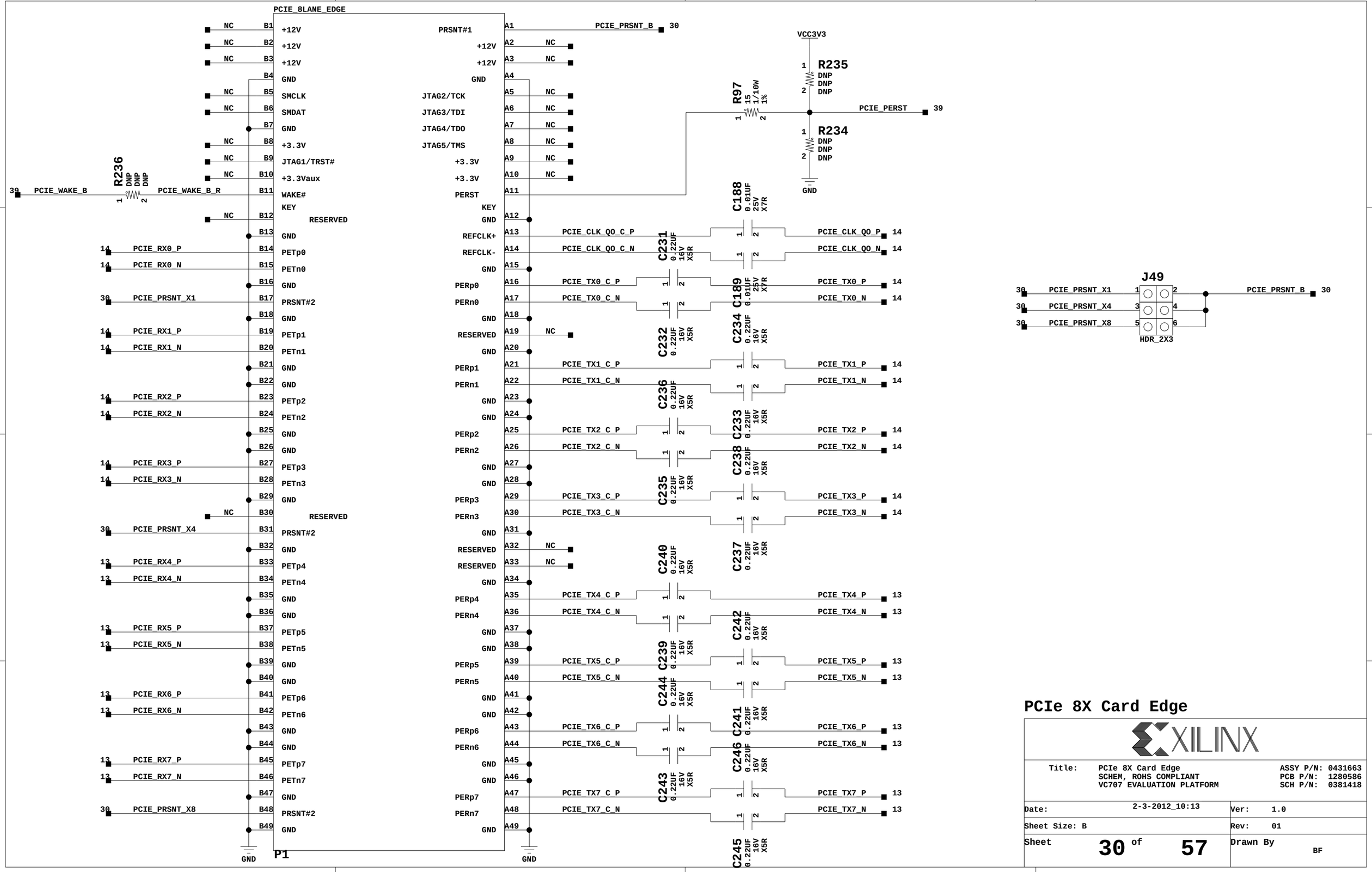
XILINX

Title:	FMC 2 HPC Header, Rows H, J, K SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	28 of 57	Drawn By	BF



ANSI/VITA 57.1 - Revised 2010
FMC 2 HPC Header, GND

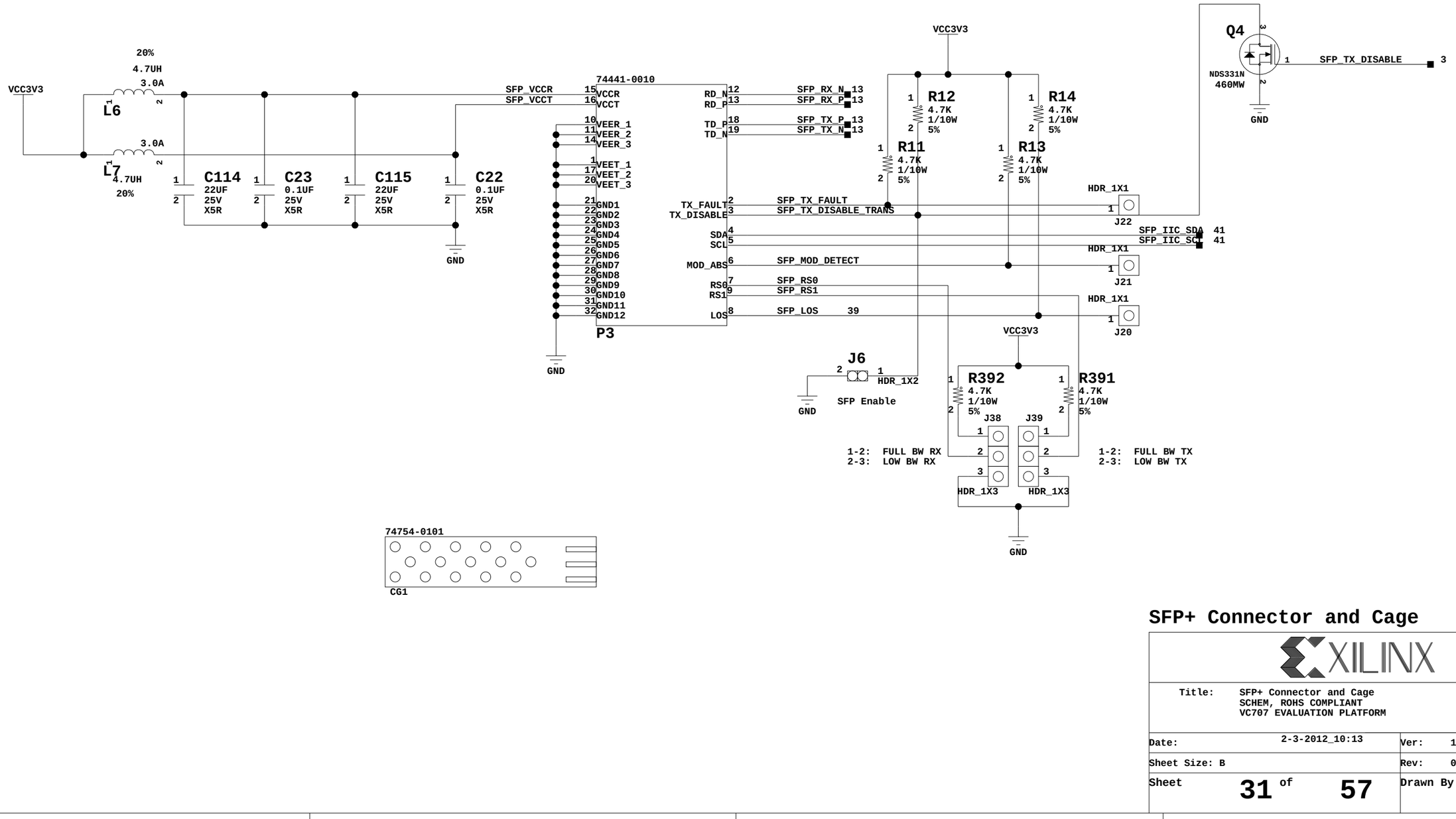
Title:	FMC 2 HPC Header, GND SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	29 of 57	Drawn By	BF



PCIe 8X Card Edge

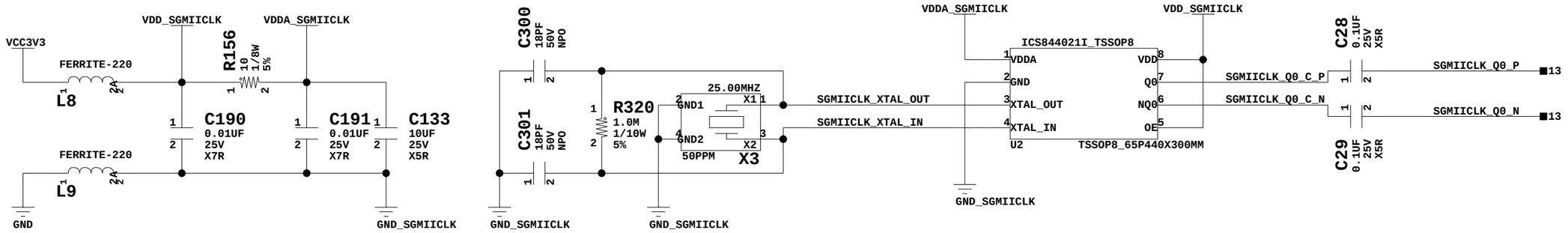
XILINX

Title:	PCIe 8X Card Edge SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	30 of 57	Drawn By	BF



SFP+ Connector and Cage

Title:	SFP+ Connector and Cage SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	31 of 57	Drawn By	BF



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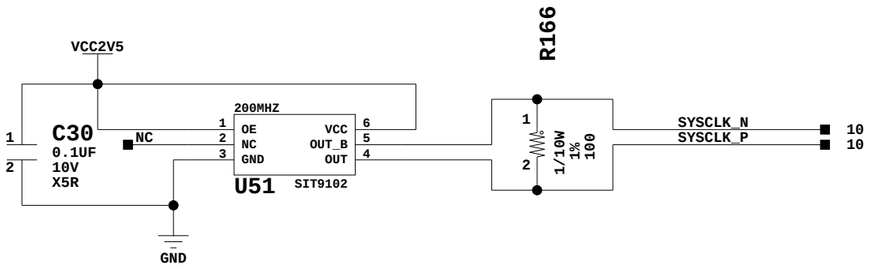
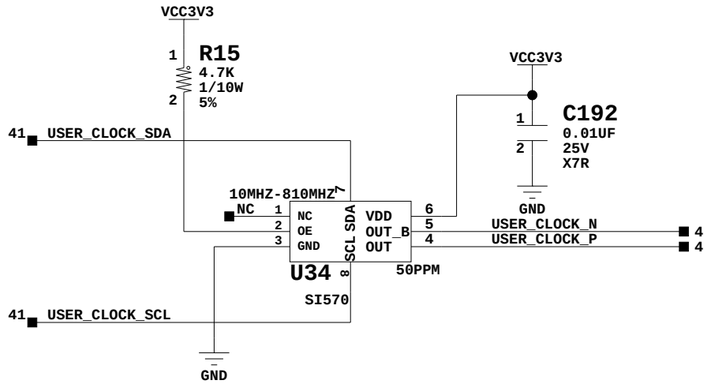
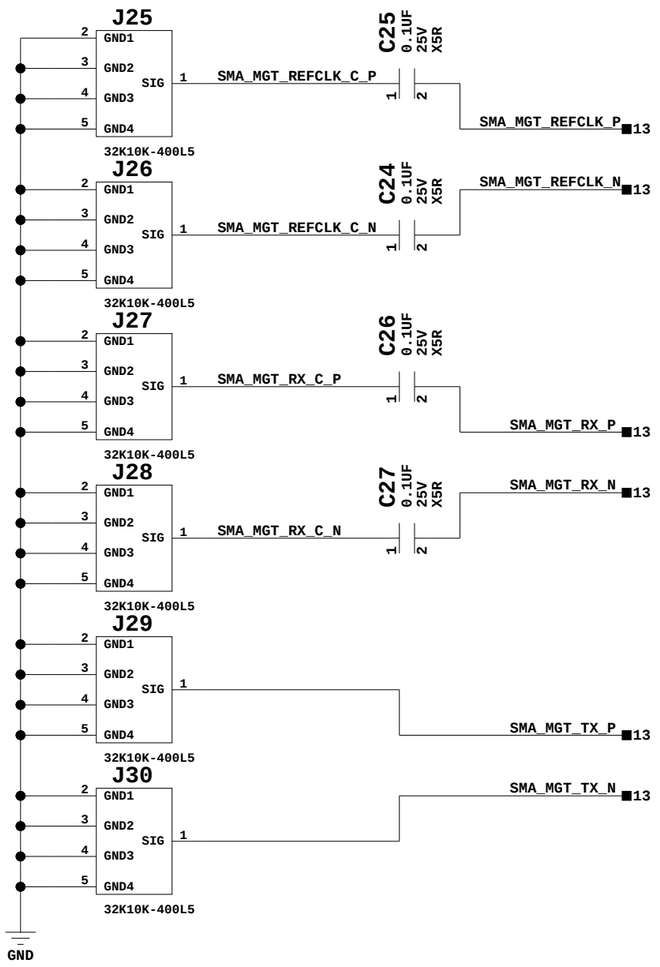
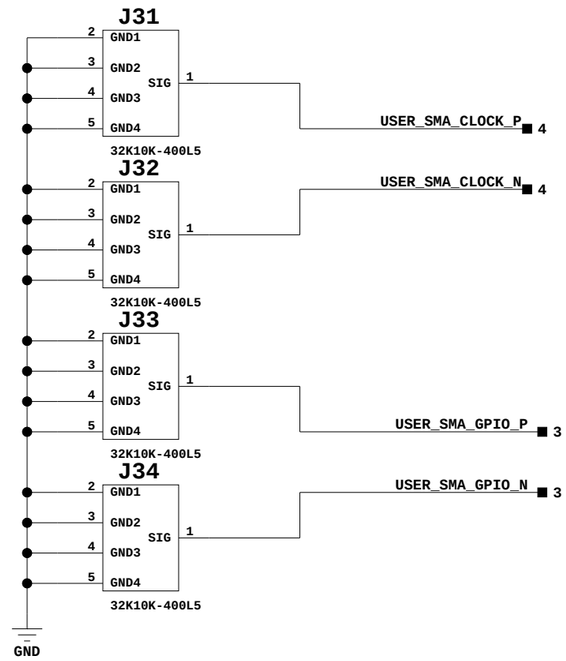




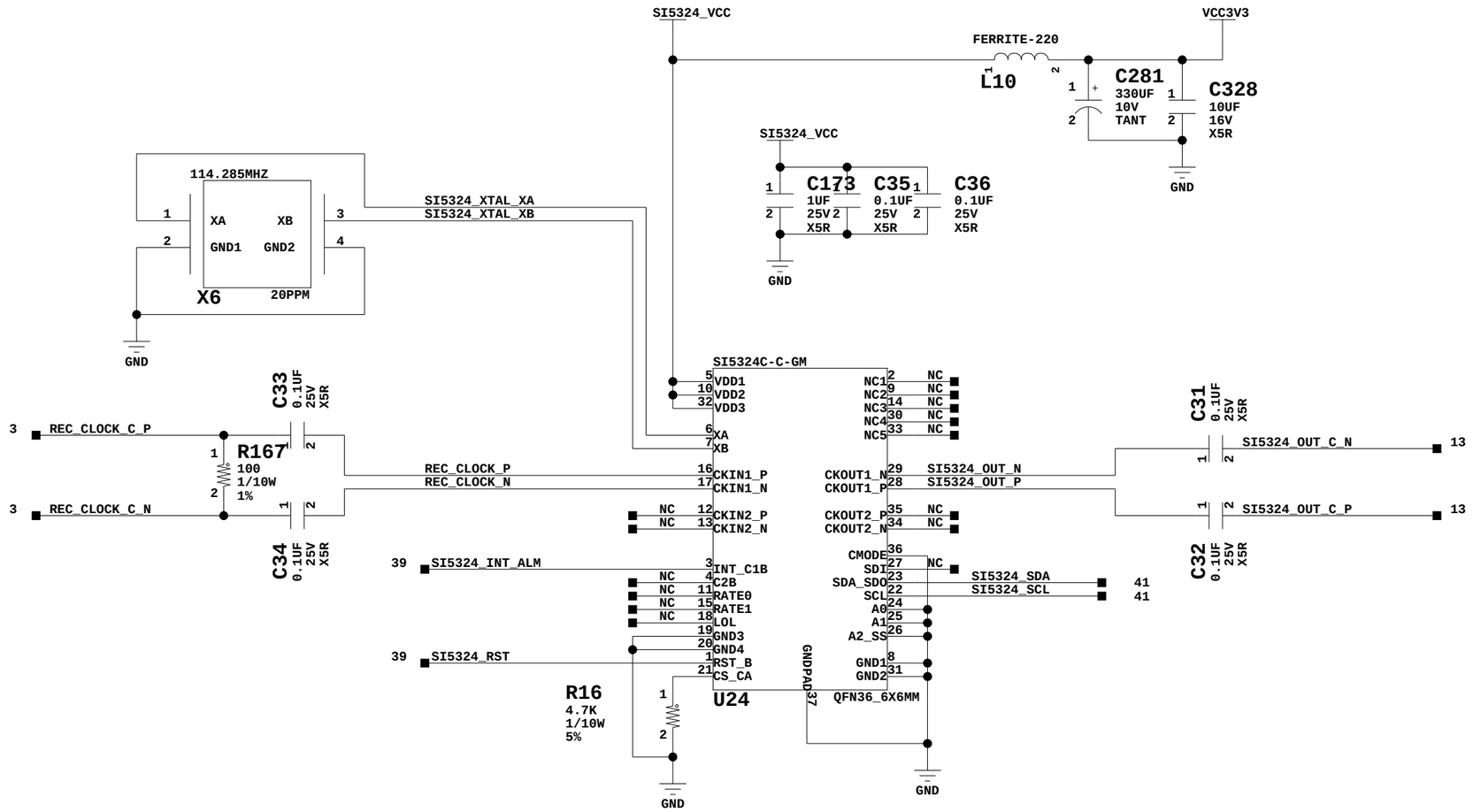




Clocks and SMA Connectors

XILINX

Title:	Clocks and SMA Connectors SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	32 of 57	Drawn By	BF



5324 Clock Recovery

Title:	5324 Clock Recovery SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N:	0431663
		PCB P/N:	1280586
		SCH P/N:	0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	33 of 57	Drawn By	BF

The PHY MDIP Pins below are
Media Dependent Interface Pins (MDIP),
and are all bidirectional pins.

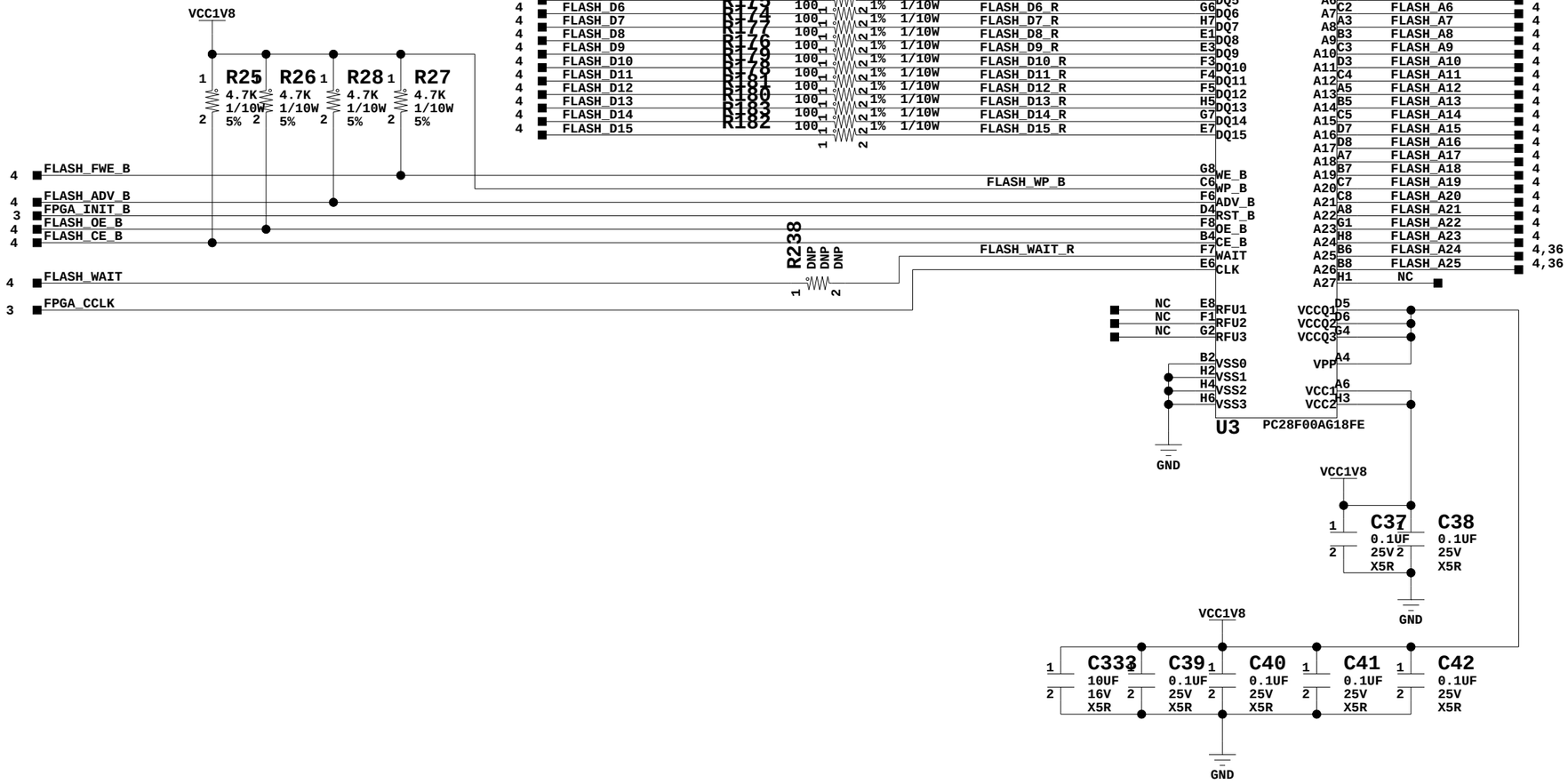
Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	111	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled. 125 CLK option disabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	111	GMII to Cu mode. Fiber/copper auto-detect diasabled. Sleep mode disabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	111	
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW interrupt 50Ohm SERDES option.

10/100/1000 PHY

XILINX

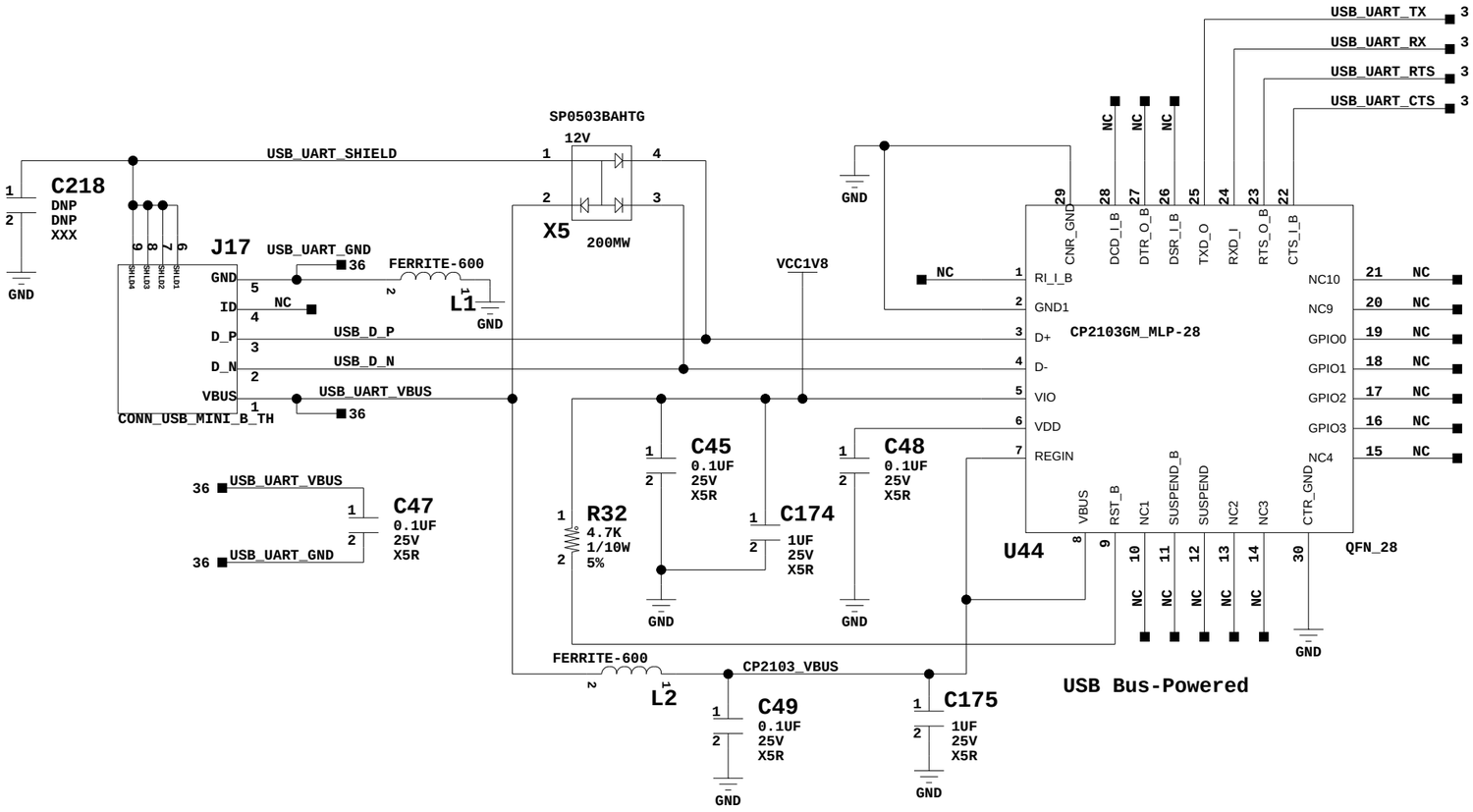
Title:	10/100/1000 PHY SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N:	0431663
		PCB P/N:	1280586
		SCH P/N:	0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size:	B	Rev:	01
Sheet	34 of 57	Drawn By	BF

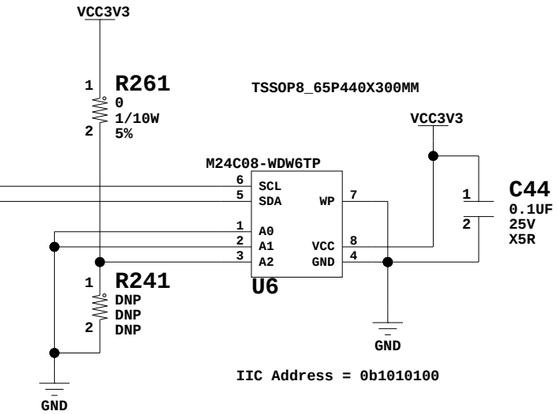


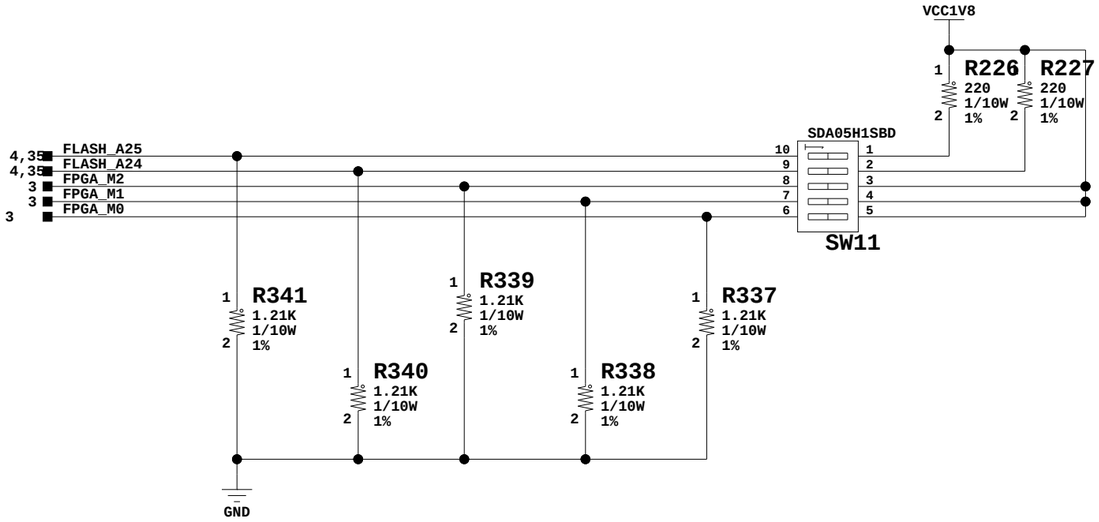
BPI FLASH

XILINX

Title:	BPI FLASH SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	35 of 57	Drawn By	BF

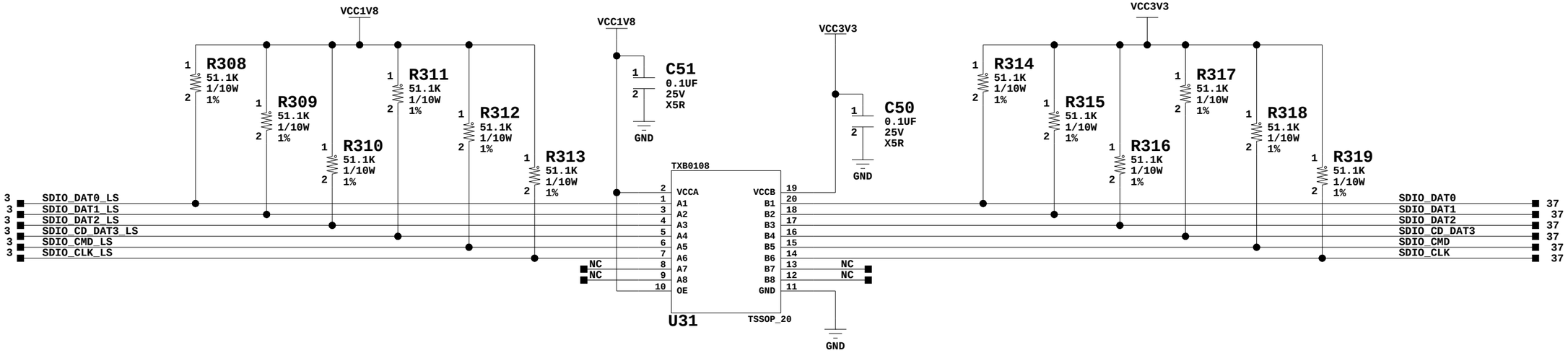


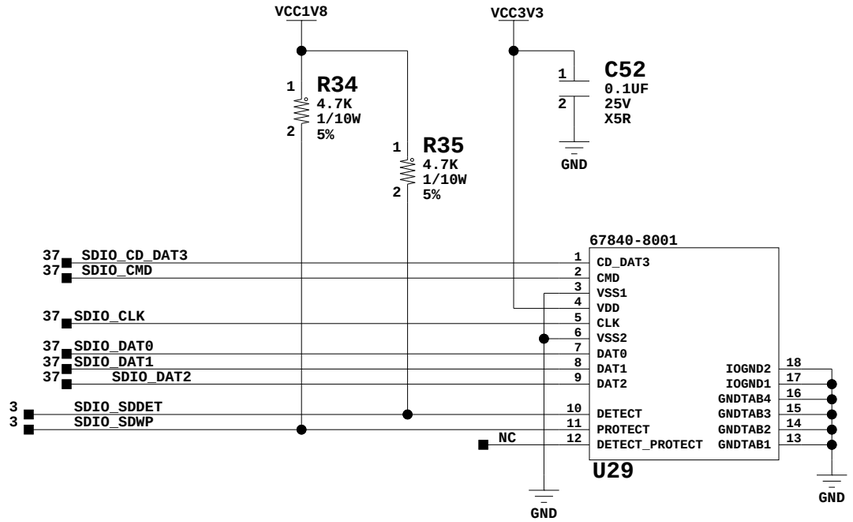




USB UART, EEPROM, Config DIPs

Title:	USB UART, EEPROM, Config DIPs SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	36 of 57	Drawn By	BF

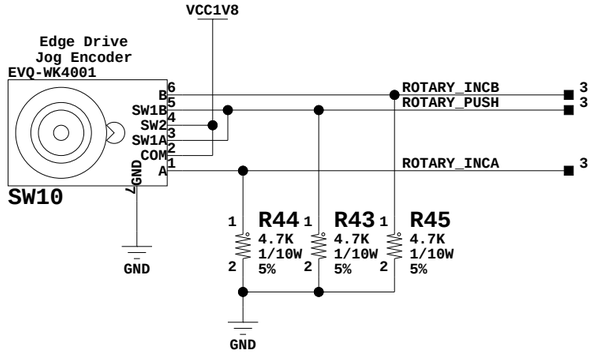


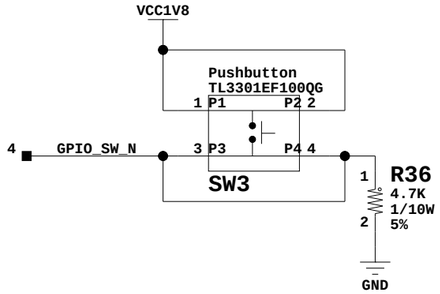


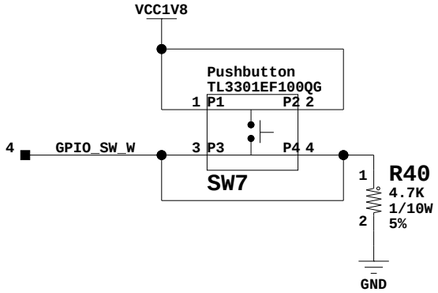
SD Card Connector

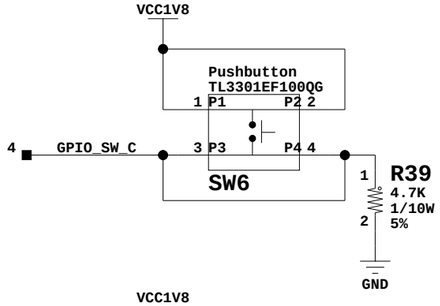
XILINX

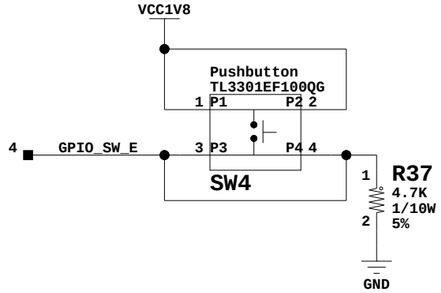
Title:	SD Card Connector SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	37 of 57	Drawn By	BF

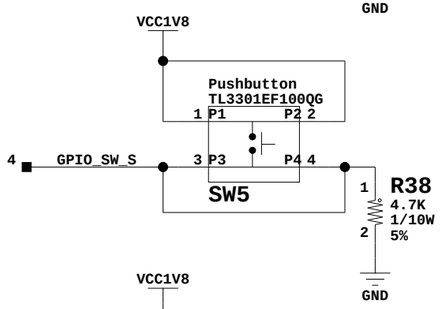




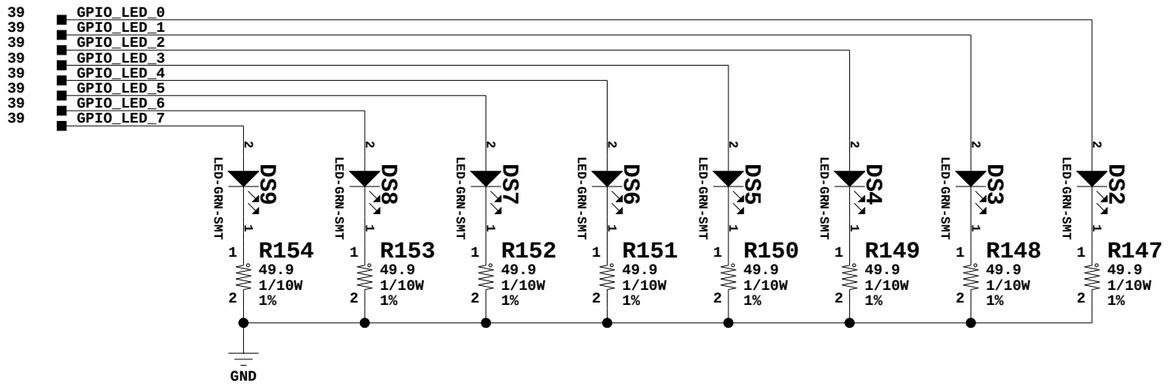


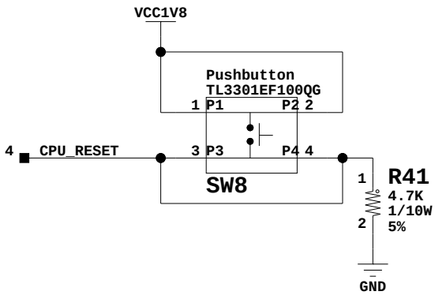


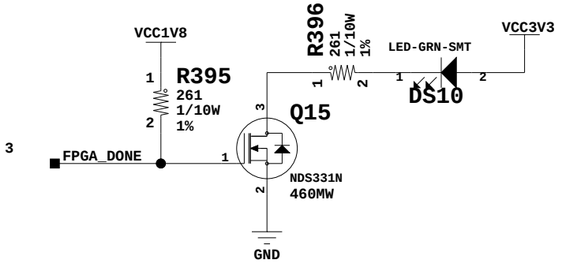


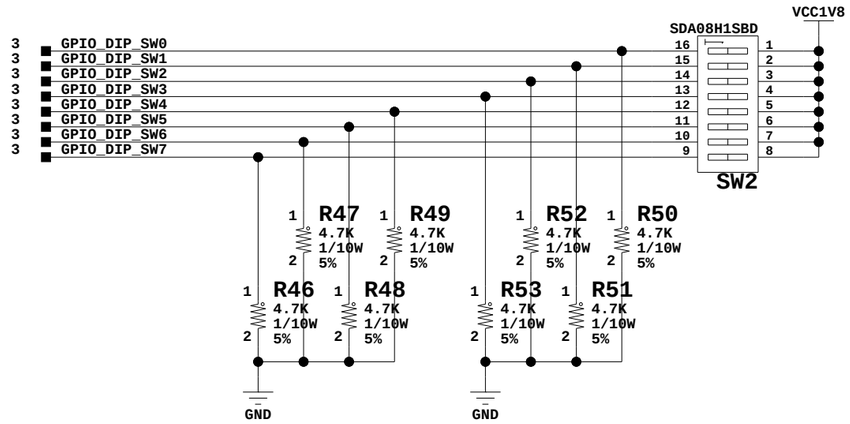


LEDs near top edge



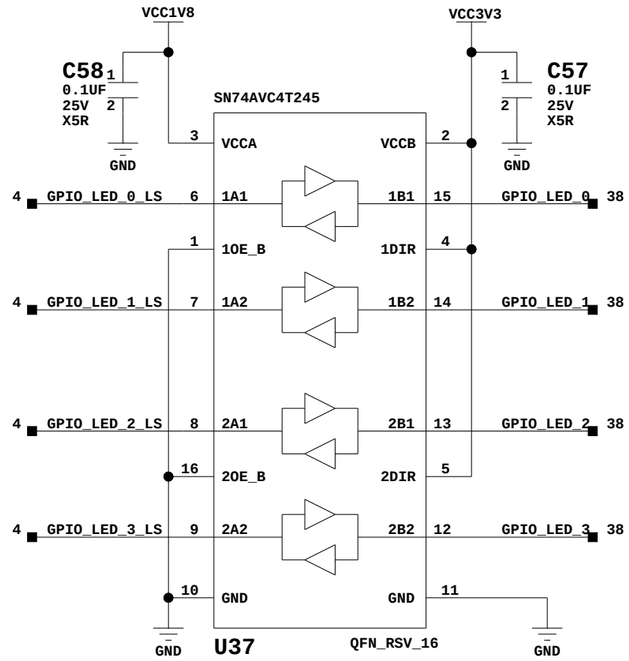


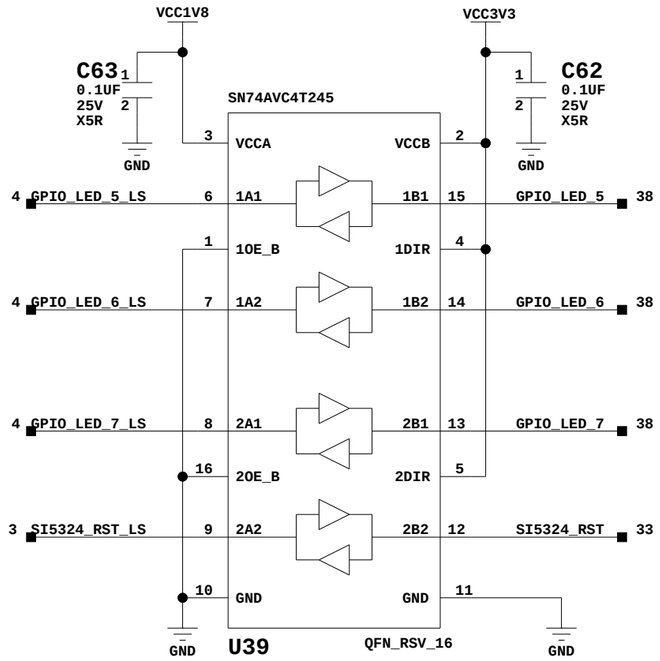


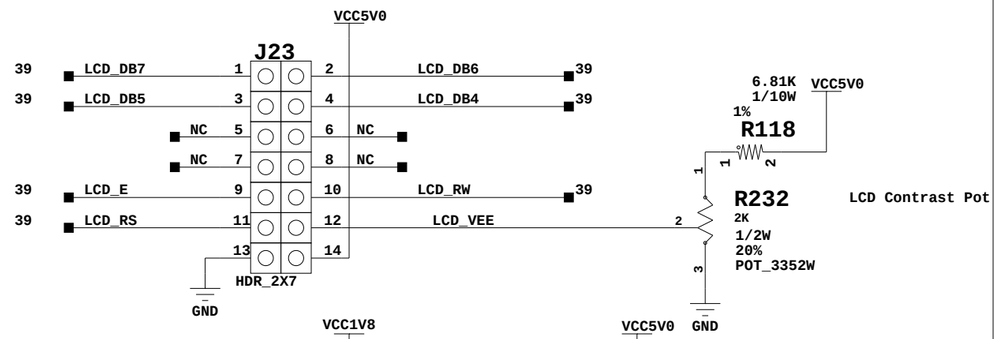


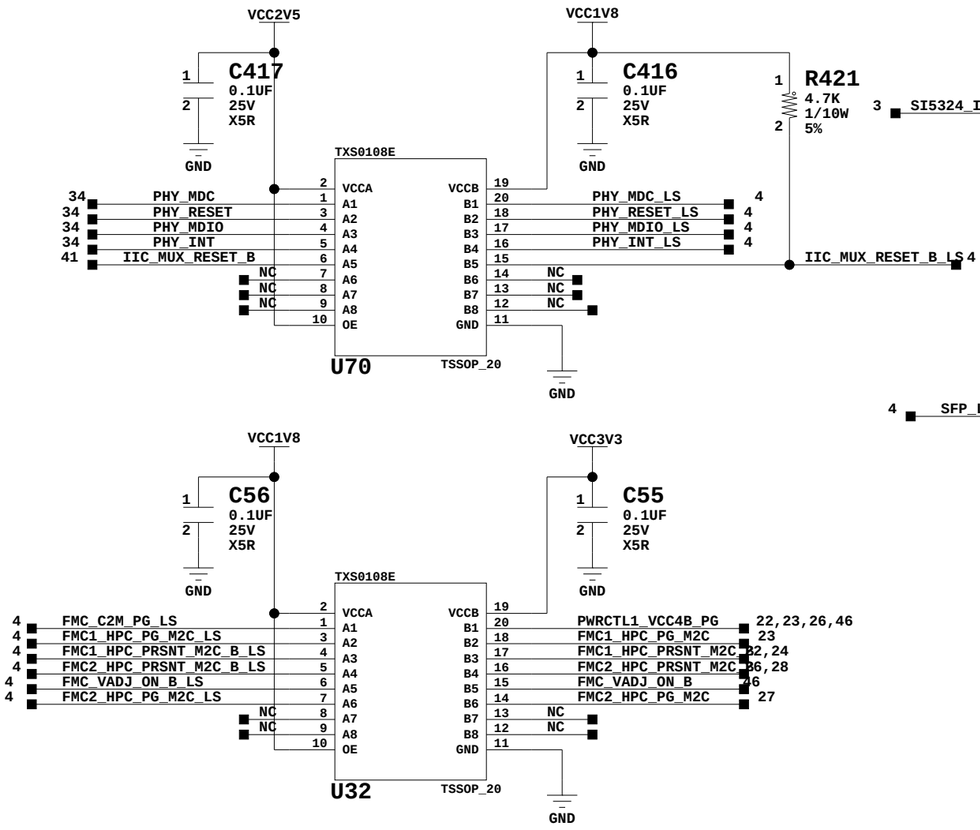
Buttons, Switches, LEDs, Rotary Encode

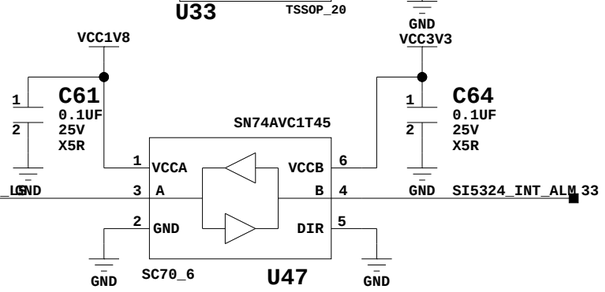
Title:	Buttons, Switches, LEDs, Rotary Encoder SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	38 of 57	Drawn By	BF

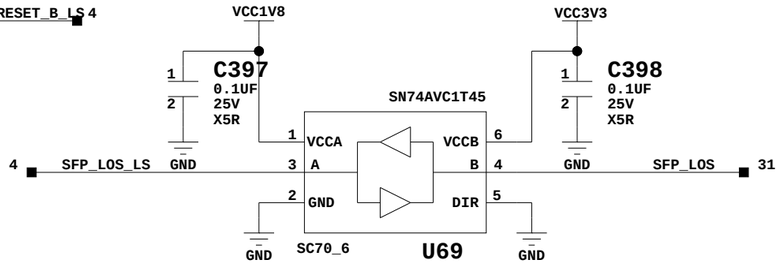






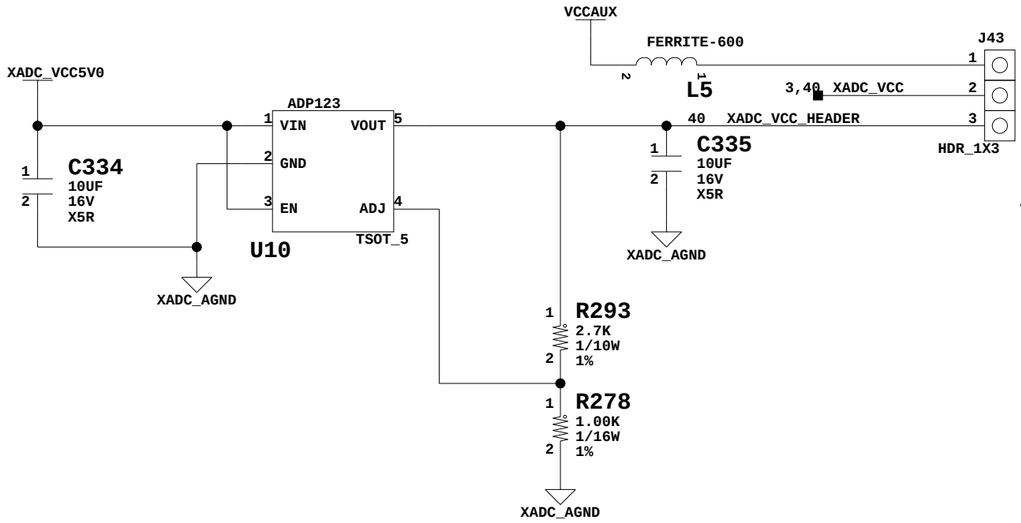


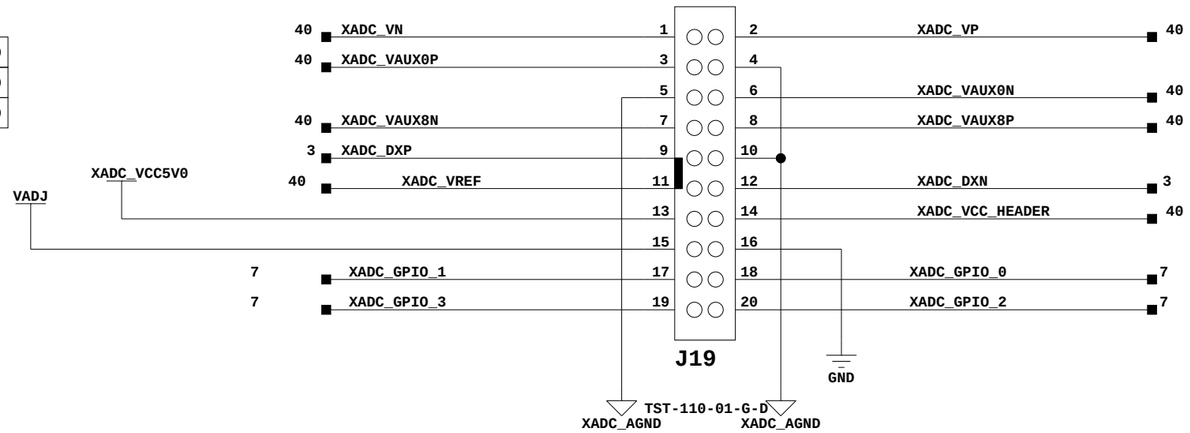


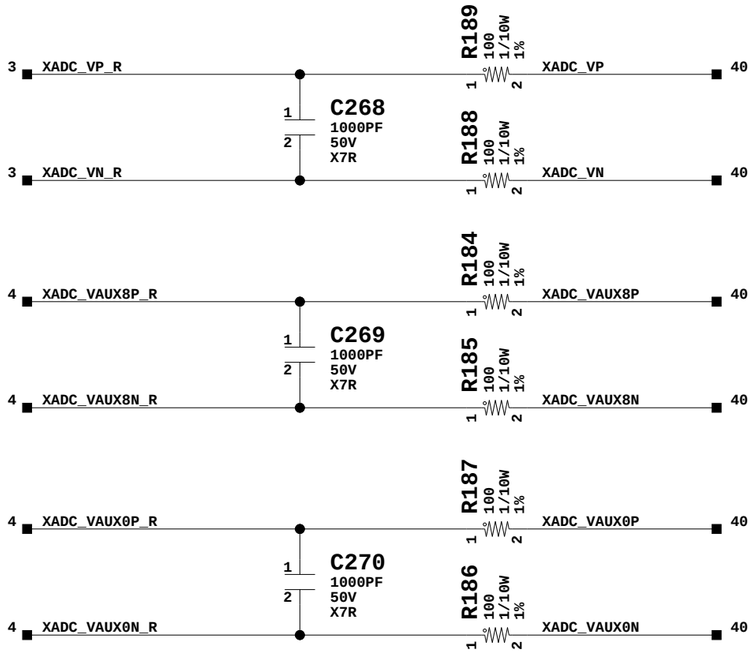


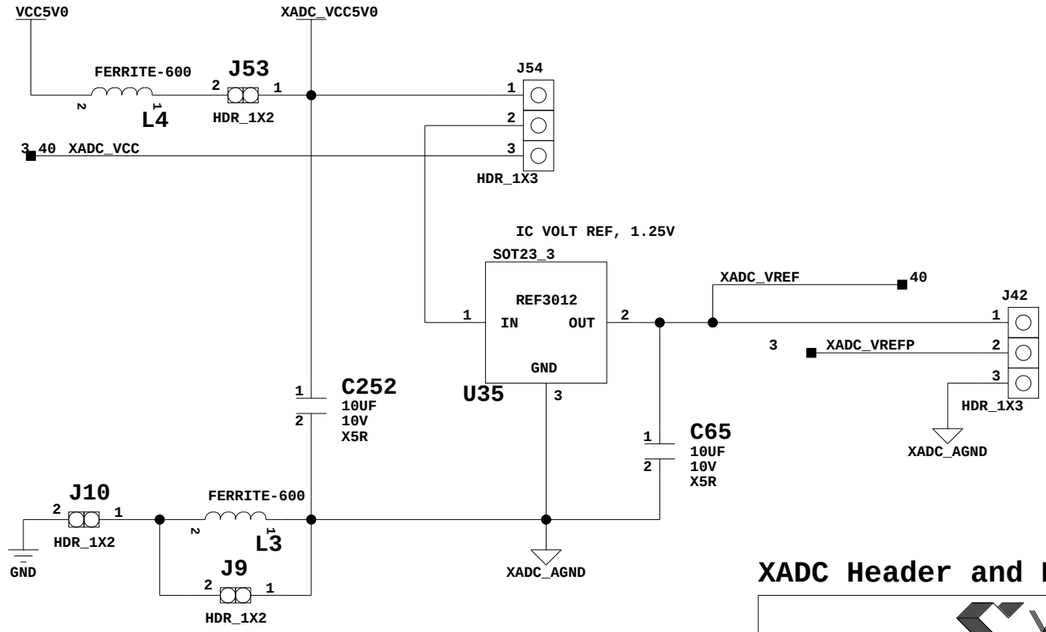
LCD, Level Shifters

Title:	LCD, Level Shifters SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N:	0431663
		PCB P/N:	1280586
		SCH P/N:	0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	39 of 57	Drawn By	BF





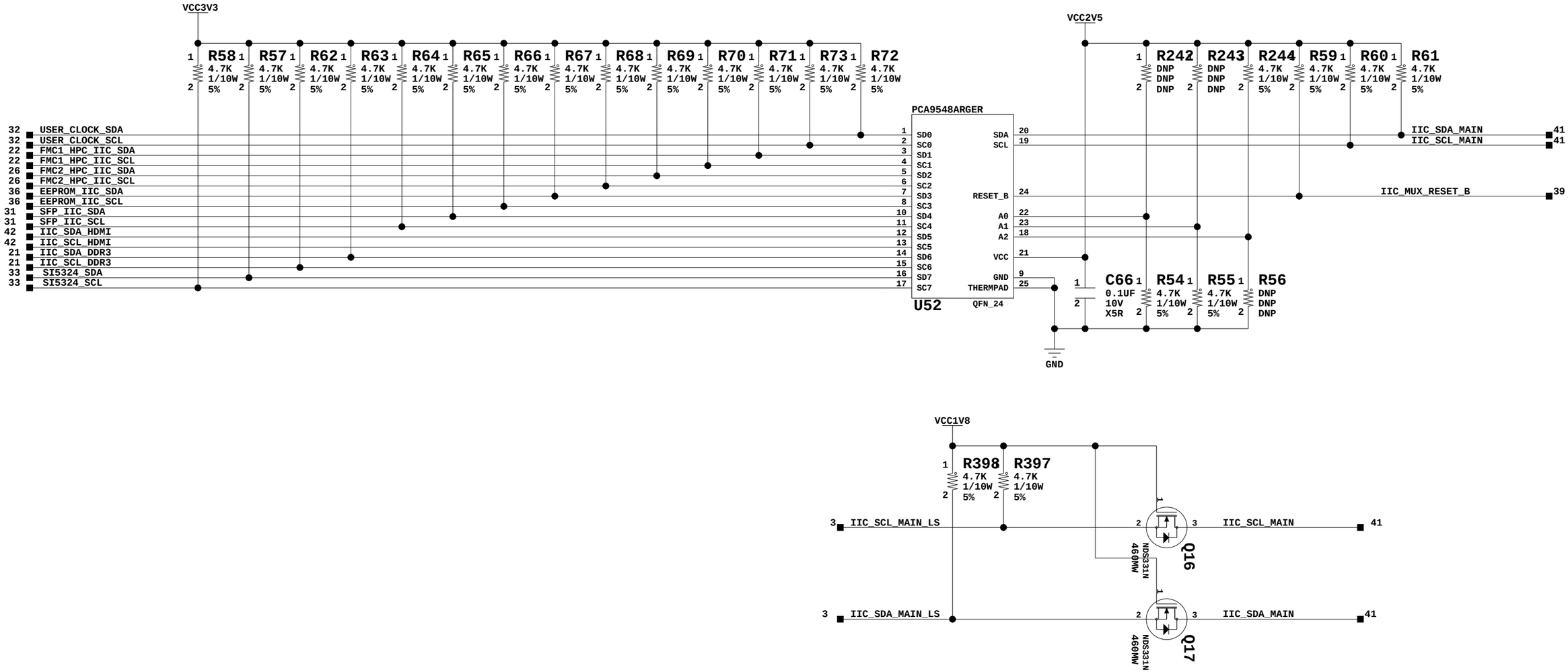




XADC Header and Reference

XILINX

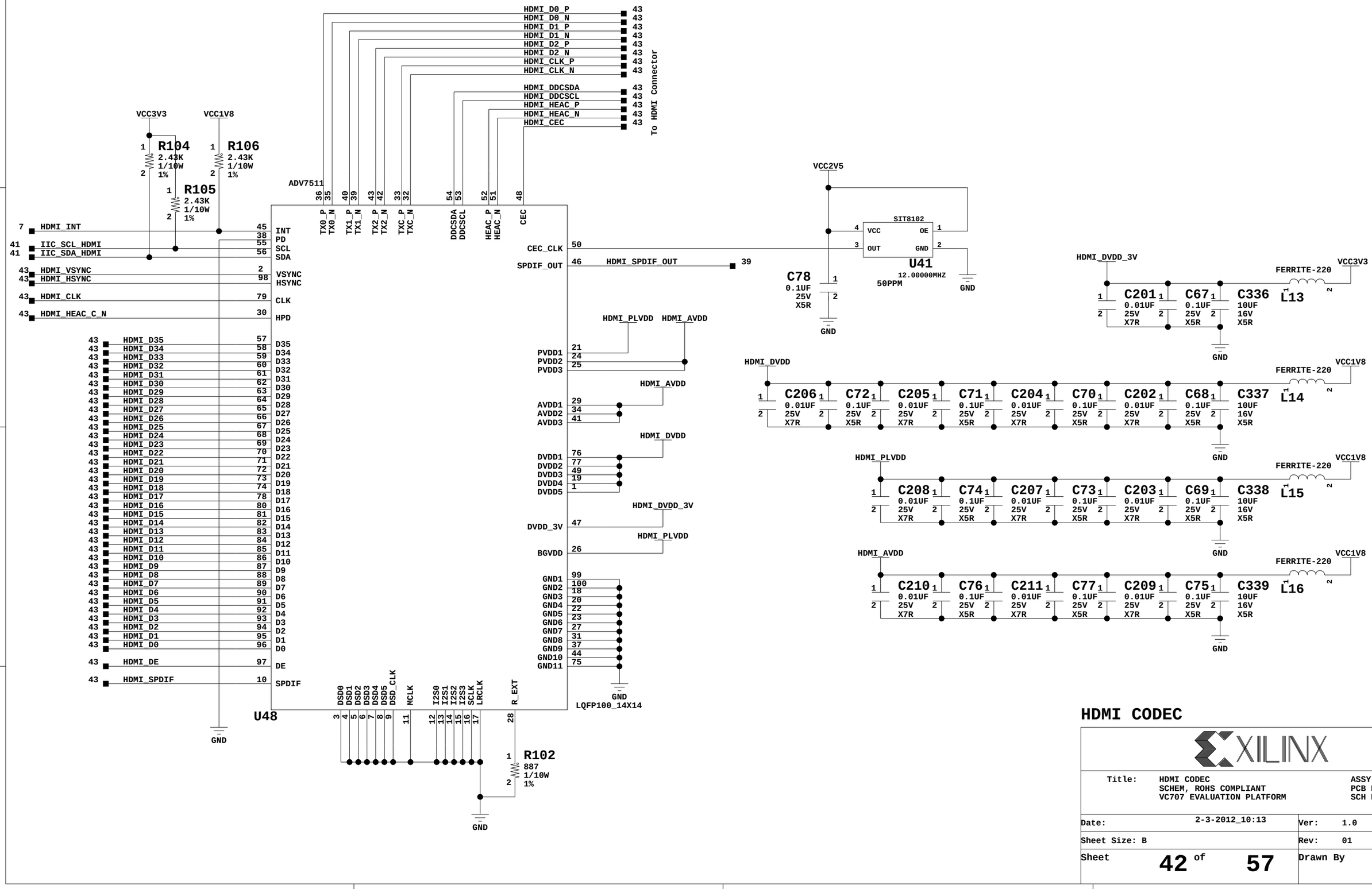
Title:	XADC Header and Reference SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	40 of 57	Drawn By	BF



IIC MUX

XILINX

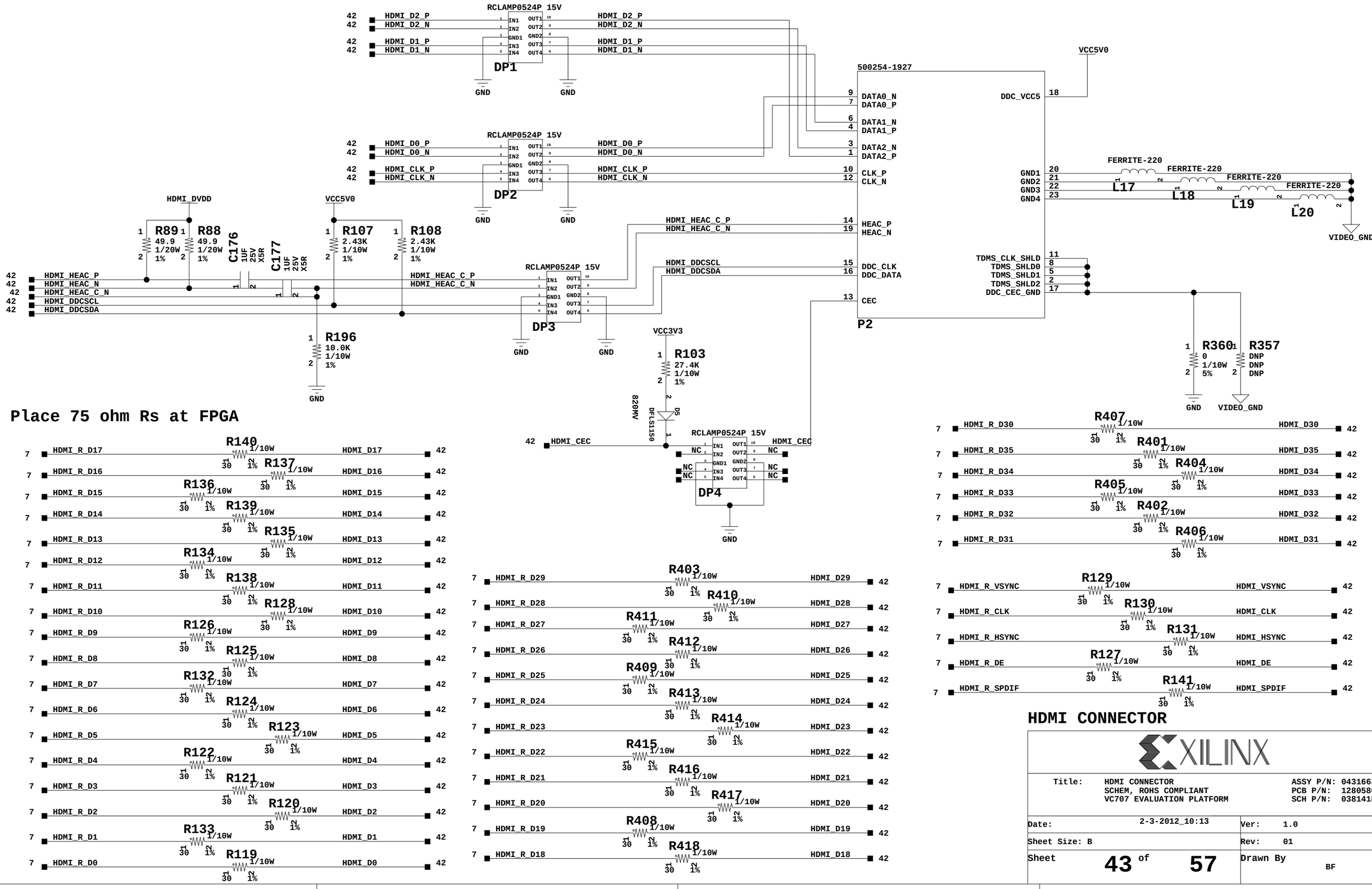
Title:	IIC MUX SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	41 of 57	Drawn By	BF

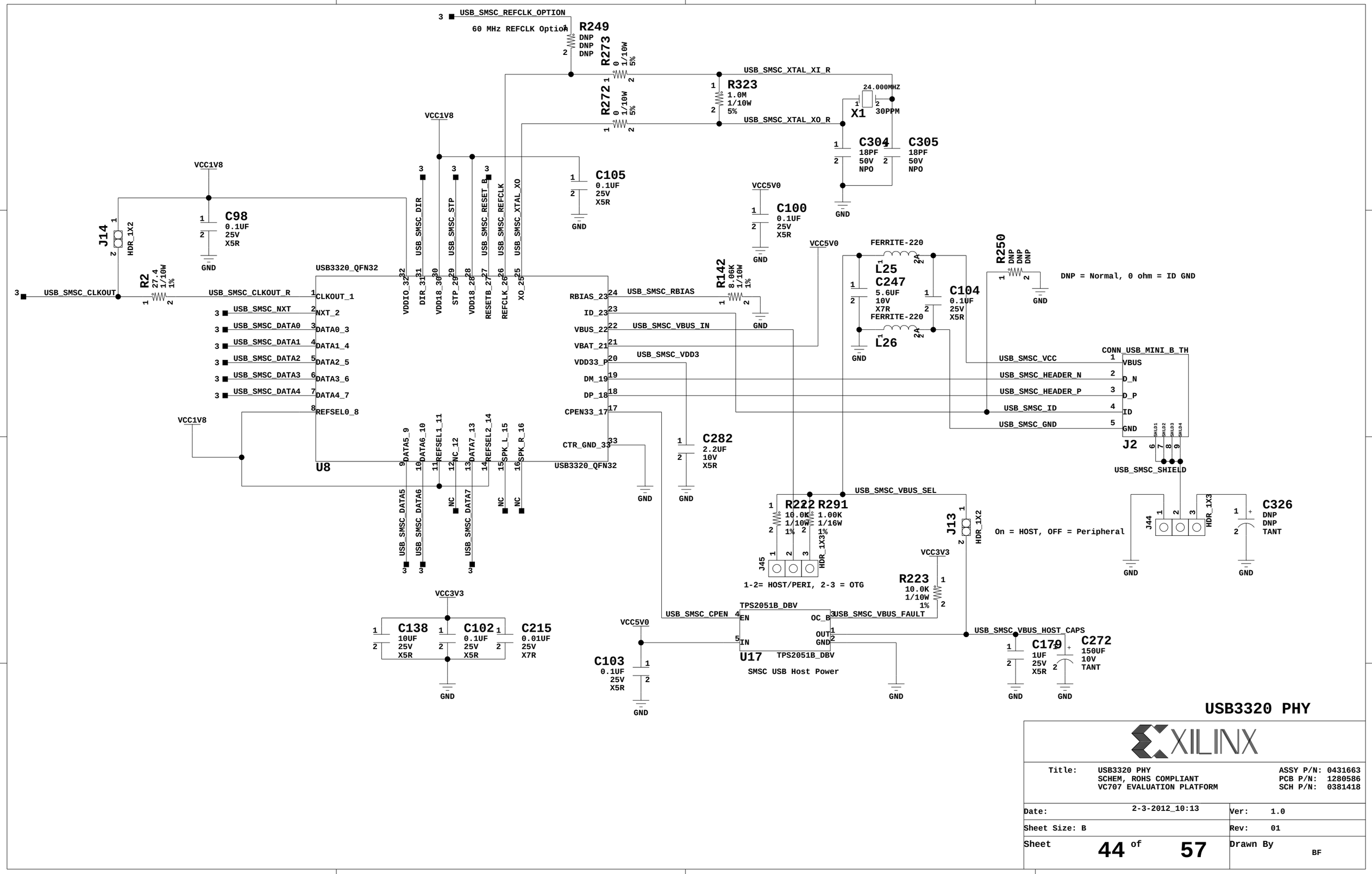


HDMI CODEC

XILINX

Title:	HDMI CODEC SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	42 of 57	Drawn By	BF

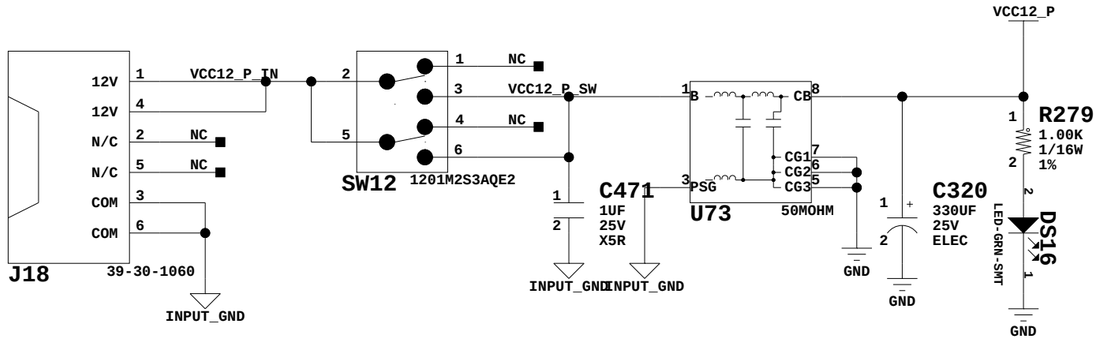

RCLAMP0524P 15V
DP1
DP2
DP3
DP4
GND
HDMI_DVDD
VCC5V0
VCC3V3
R89 49.9 1/20W 1%
R88 49.9 1/20W 1%
C176 1UF 25V X5R
C177 1UF 25V X5R
R107 2.43K 1/10W 1%
R108 2.43K 1/10W 1%
R196 10.0K 1/10W 1%
R103 27.4K 1/10W 1%
D5 DFLS150
HDMI_D2_P
HDMI_D2_N
HDMI_D1_P
HDMI_D1_N
HDMI_D0_P
HDMI_D0_N
HDMI_CLK_P
HDMI_CLK_N
HDMI_HEAC_P
HDMI_HEAC_N
HDMI_HEAC_C_P
HDMI_HEAC_C_N
HDMI_DDCSCL
HDMI_DDCSDA
HDMI_CEC
500254-1927
P2
DATA0_N
DATA0_P
DATA1_N
DATA1_P
DATA2_N
DATA2_P
CLK_P
CLK_N
HEAC_P
HEAC_N
DDC_CLK
DDC_DATA
CEC
DDC_VCC5
GND1
GND2
GND3
GND4
TDMS_CLK_SHLD
TDMS_SHLD0
TDMS_SHLD1
TDMS_SHLD2
DDC_CEC_GND
FERRITE-220
L17
L18
L19
L20
VIDEO_GND
R360 0 1/10W 5%
R357 DNP DNP DNP
Place 75 ohm Rs at FPGA
R140 R137 R136 R139 R135 R134 R138 R128 R126 R125 R132 R124 R123 R122 R121 R120 R133 R119
R403 R410 R411 R412 R409 R413 R414 R415 R416 R417 R408 R418
R407 R401 R404 R405 R402 R406
R129 R130 R131 R127 R141
HDMI_R_D17 HDMI_R_D16 HDMI_R_D15 HDMI_R_D14 HDMI_R_D13 HDMI_R_D12 HDMI_R_D11 HDMI_R_D10 HDMI_R_D9 HDMI_R_D8 HDMI_R_D7 HDMI_R_D6 HDMI_R_D5 HDMI_R_D4 HDMI_R_D3 HDMI_R_D2 HDMI_R_D1 HDMI_R_D0
HDMI_R_D29 HDMI_R_D28 HDMI_R_D27 HDMI_R_D26 HDMI_R_D25 HDMI_R_D24 HDMI_R_D23 HDMI_R_D22 HDMI_R_D21 HDMI_R_D20 HDMI_R_D19 HDMI_R_D18
HDMI_R_D30 HDMI_R_D35 HDMI_R_D34 HDMI_R_D33 HDMI_R_D32 HDMI_R_D31
HDMI_R_VSYNC HDMI_R_CLK HDMI_R_HSYNC HDMI_R_DE HDMI_R_SPDIF
HDMI CONNECTOR
XILINX
Title: HDMI CONNECTOR
SCHEM, ROHS COMPLIANT
VC707 EVALUATION PLATFORM
ASSY P/N: 0431663
PCB P/N: 1280586
SCH P/N: 0381418
Date: 2-3-2012_10:13
Ver: 1.0
Sheet Size: B
Rev: 01
Sheet 43 of 57
Drawn By BF

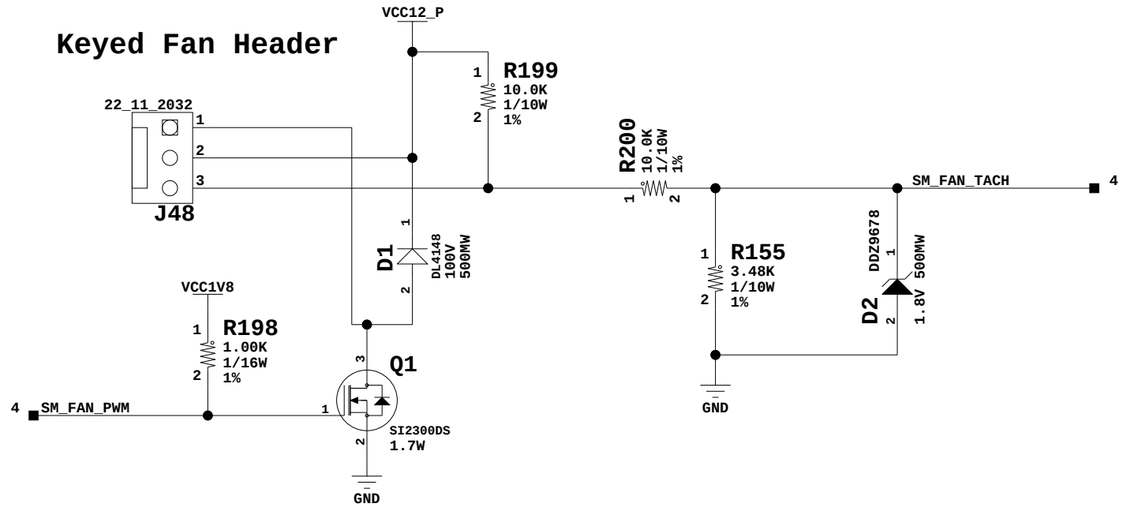


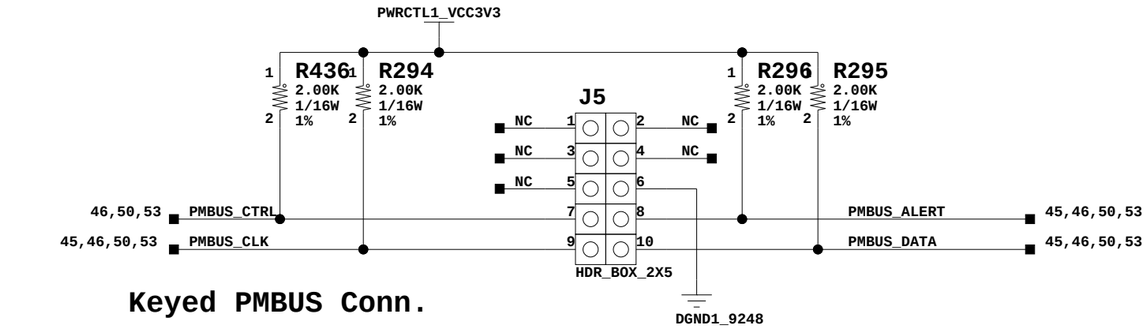
USB3320 PHY

XILINX

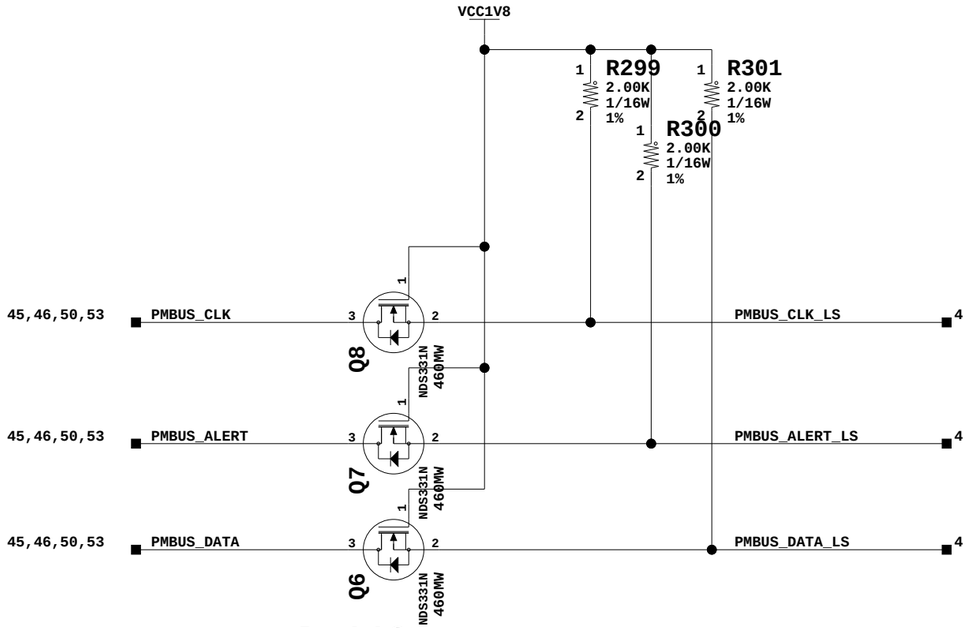
Title:	USB3320 PHY SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	44 of 57	Drawn By	BF



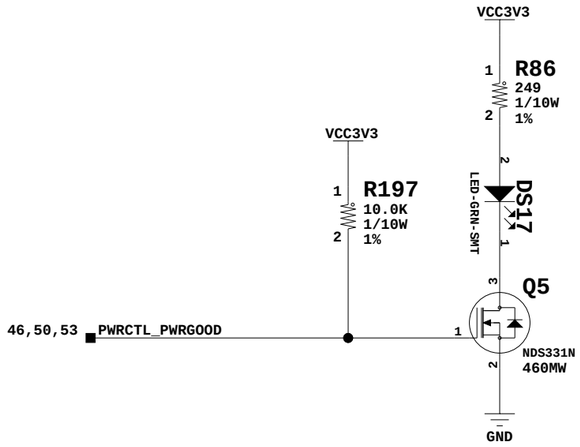




Keyed PMBUS Conn.

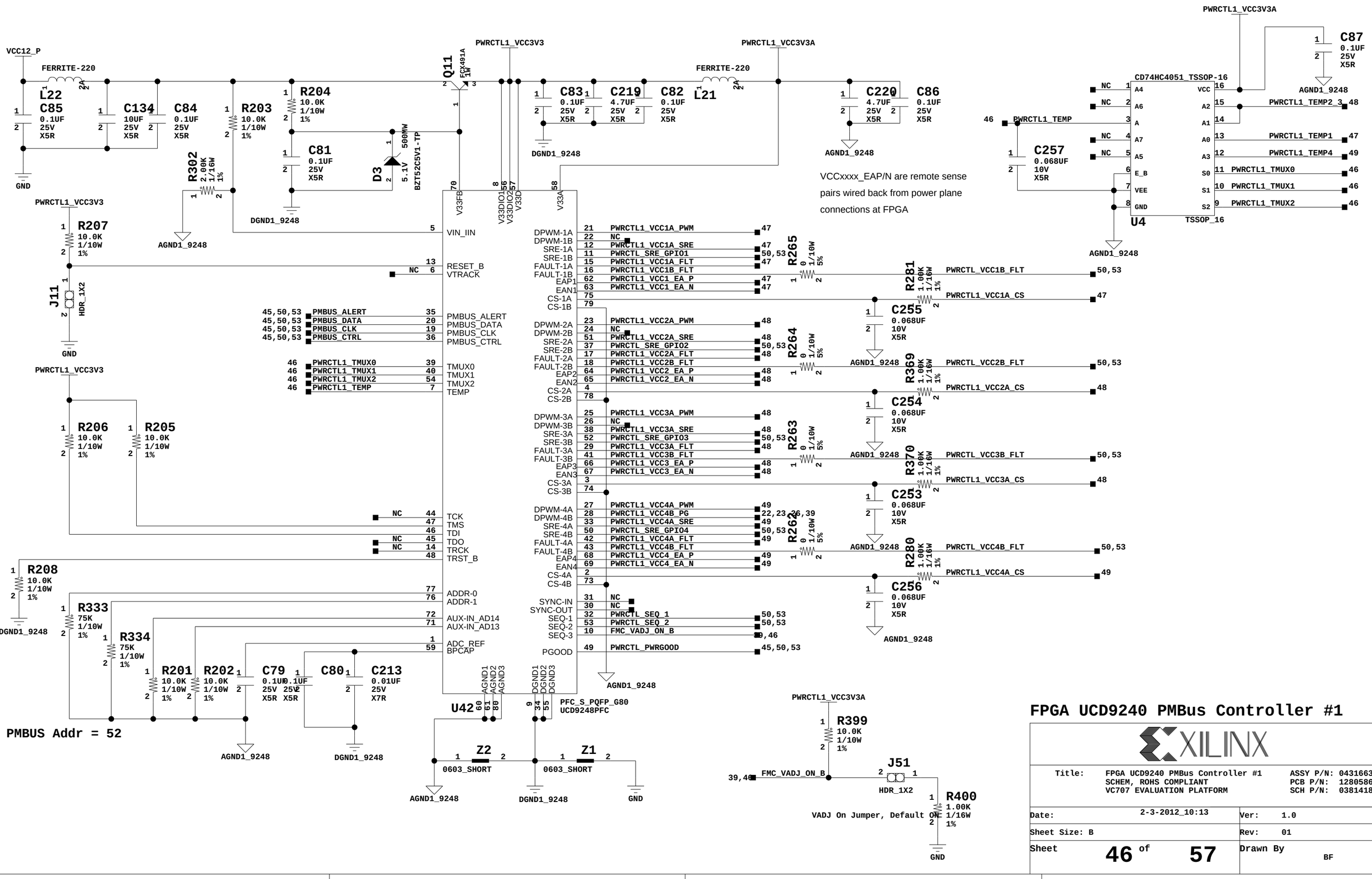


PMBUS Level-Shifter



Power Connector and switch, PMBus Head

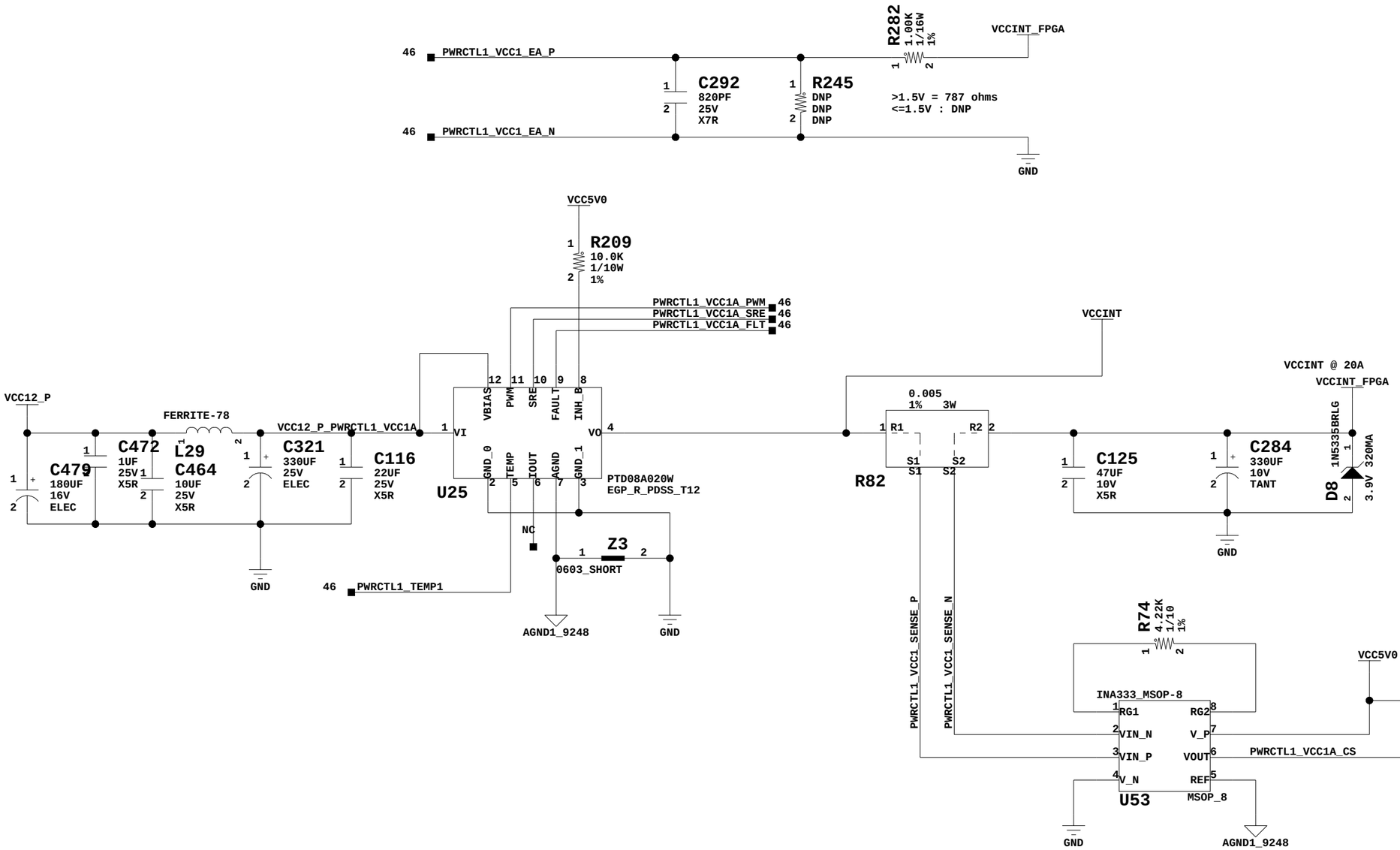
Title:	Power Connector and switch, PMBus Head SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418
Date: 2-3-2012_10:13		Ver: 1.0
Sheet Size: B		Rev: 01
Sheet 45 of 57		Drawn By BF



FPGA UCD9240 PMBus Controller #1

XILINX

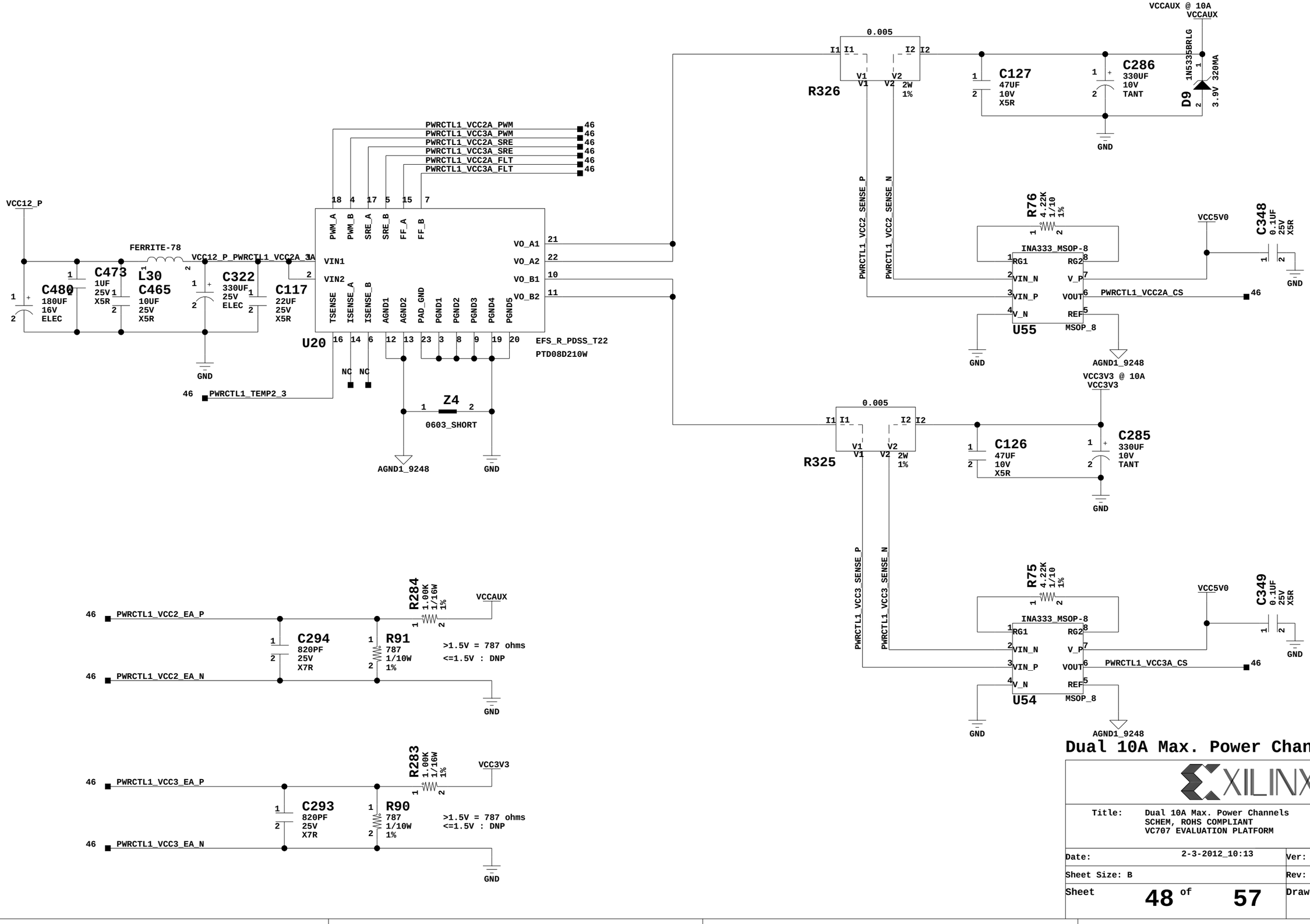
Title:	FPGA UCD9240 PMBus Controller #1 SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N:	0431663
		PCB P/N:	1280586
		SCH P/N:	0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	46 of 57	Drawn By	BF



PTD08A020W 20A Max. Power Channel

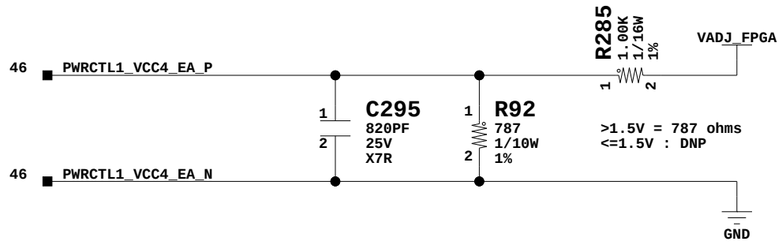
XILINX

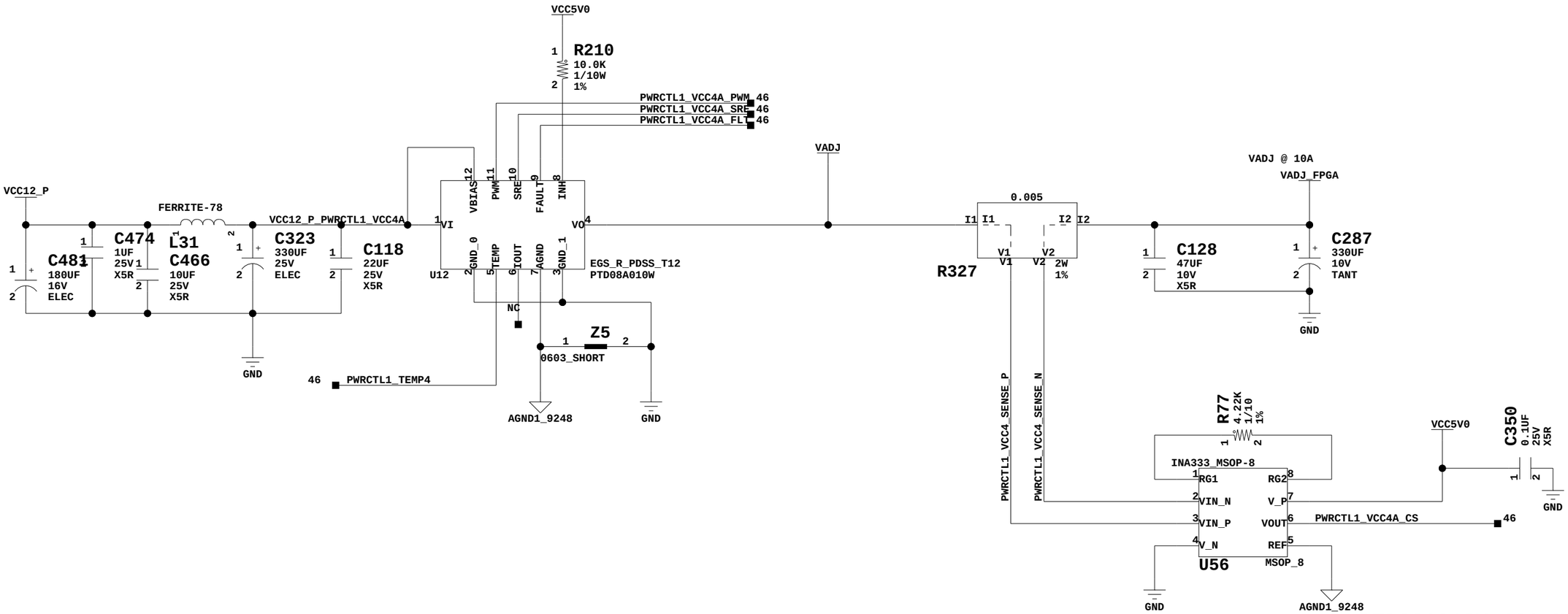
Title:	PTD08A010W 20A Max. Power Channel SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	47 of 57	Drawn By	BF



Dual 10A Max. Power Channels

Title:	Dual 10A Max. Power Channels SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418
Date:	2-3-2012_10:13	Ver: 1.0
Sheet Size: B		Rev: 01
Sheet	48 of 57	Drawn By BF

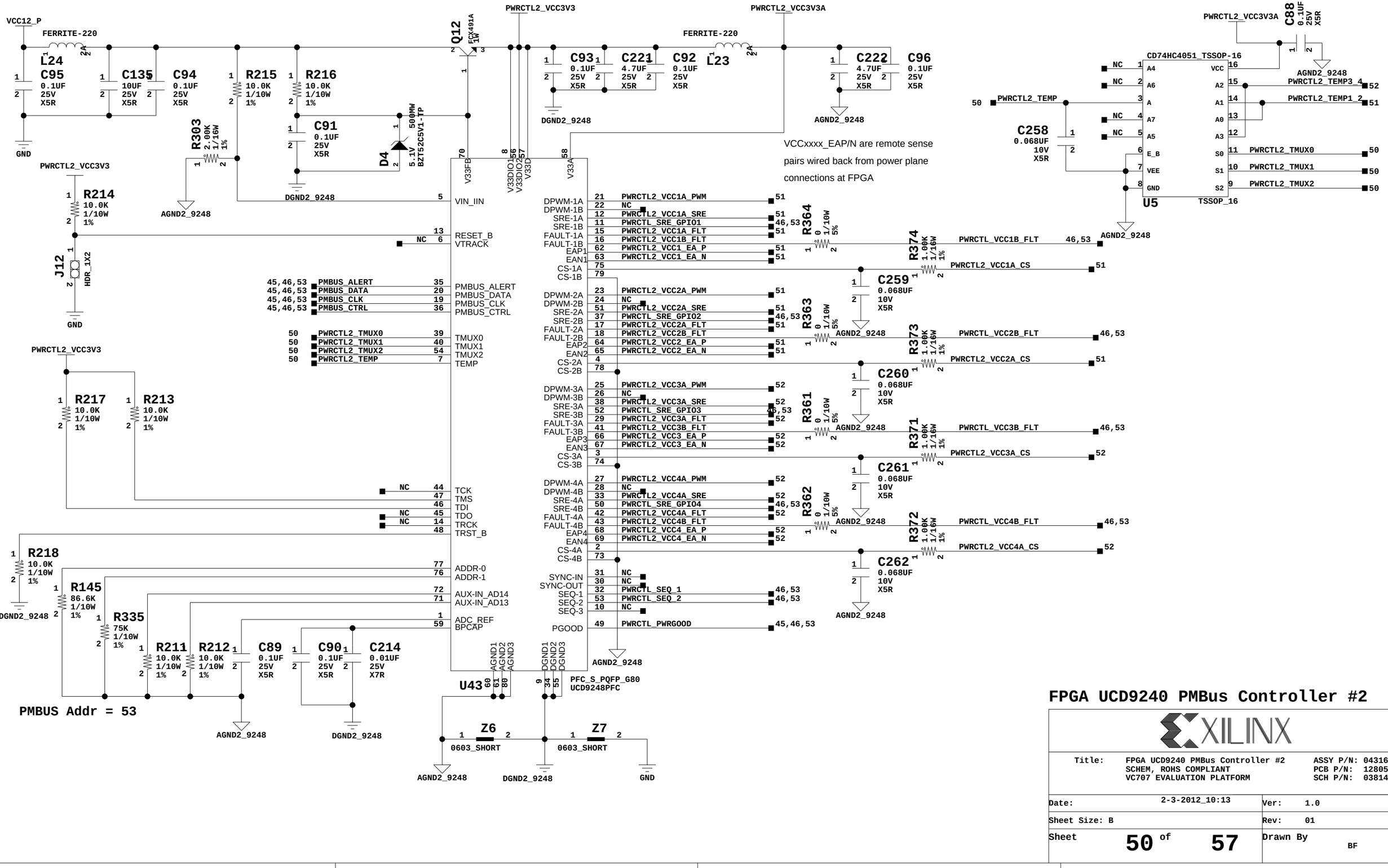


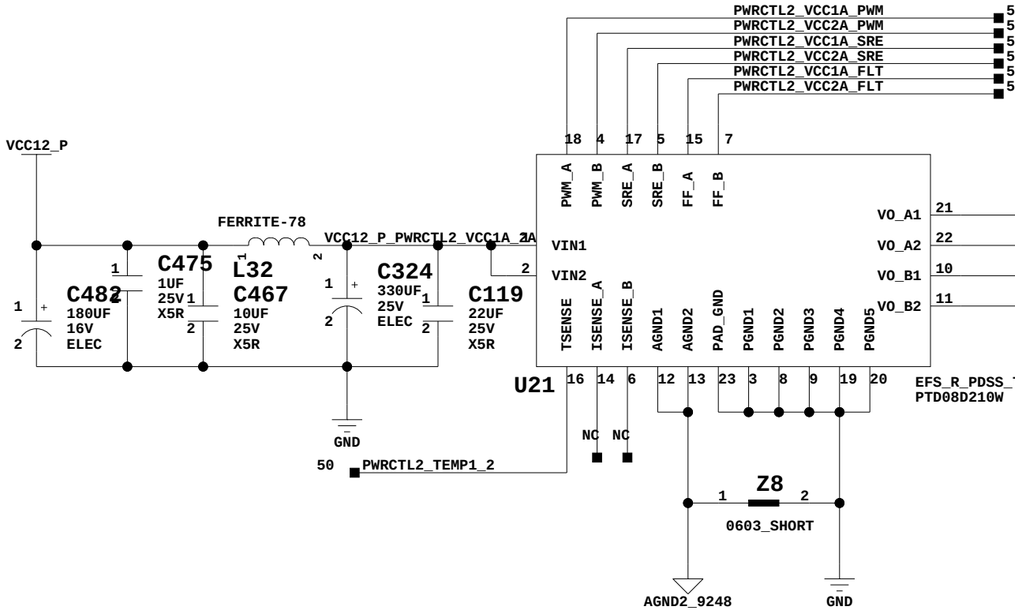


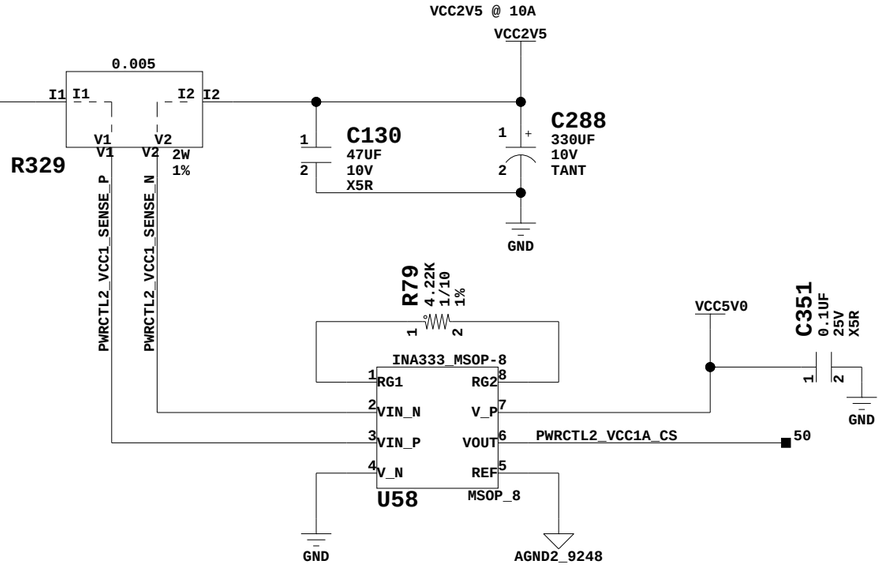
PTD08A010W 10A Max. Power Channel

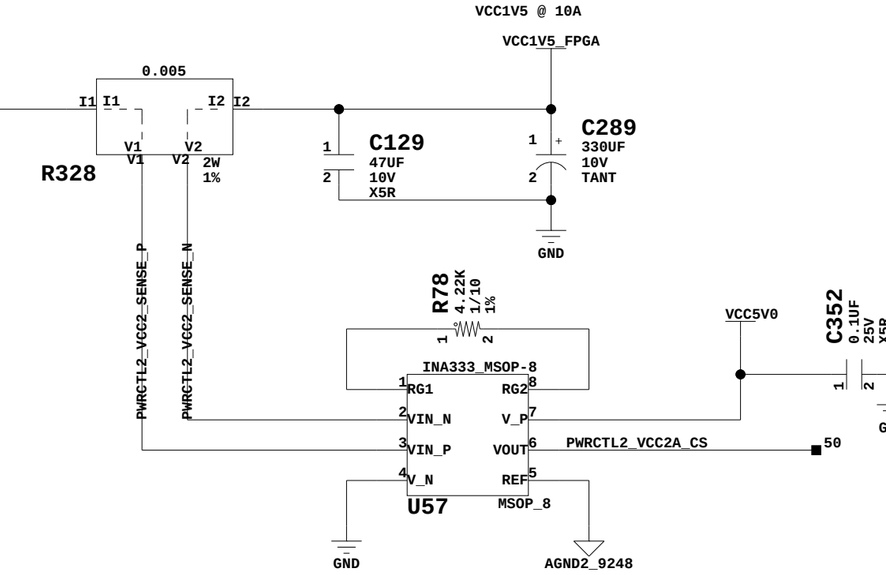
XILINX

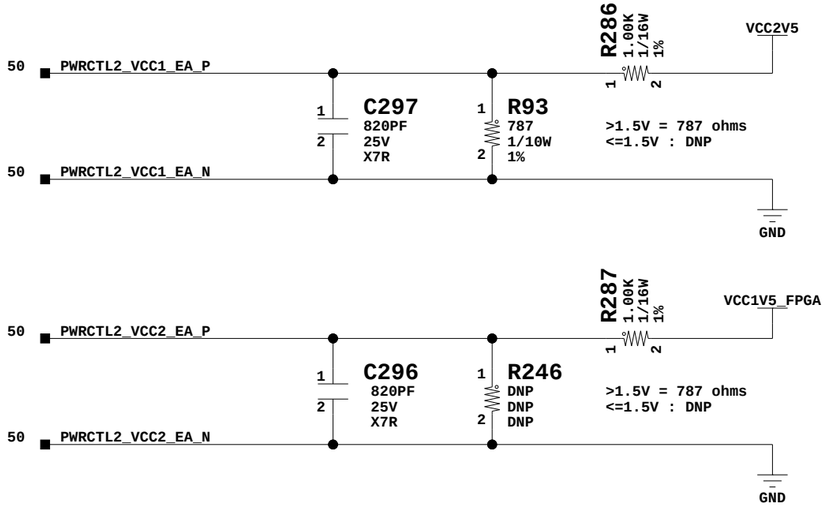
Title:	PTD08A010W 10A Max. Power Channel SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N:	0431663
		PCB P/N:	1280586
		SCH P/N:	0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	49 of 57	Drawn By	BF


VCC12_P
FERRITE-220
L24
C95 0.1UF 25V X5R
C135 10UF 25V X5R
C94 0.1UF 25V X5R
GND
R215 10.0K 1/10W 1%
R216 10.0K 1/10W 1%
R303 2.00K 1/16W 1%
C91 0.1UF 25V X5R
D4 5.1V 500MW BZT52C5V1-TP
AGND2_9248
DGND2_9248
Q12 FDV491A 1W
PWRCTL2_VCC3V3
PWRCTL2_VCC3V3A
C93 0.1UF 25V X5R
C221 4.7UF 25V X5R
C92 0.1UF 25V X5R
L23 FERRITE-220
C222 4.7UF 25V X5R
C96 0.1UF 25V X5R
VCCxxxx_EAP/N are remote sense pairs wired back from power plane connections at FPGA
C88 0.1UF 25V X5R
CD74HC4051_TSSOP-16
U5 TSSOP_16
PWRCTL_TEMP
C258 0.068UF 10V X5R
PWRCTL2_TEMP3_4
PWRCTL2_TEMP1_2
PWRCTL_TMUX0
PWRCTL_TMUX1
PWRCTL_TMUX2
R214 10.0K 1/10W 1%
J12 HDR_1X2
VIN_IIN
RESET_B
VTRACK
PMBUS_ALERT
PMBUS_DATA
PMBUS_CLK
PMBUS_CTRL
TMUX0
TMUX1
TMUX2
TEMP
R364 0 1/10W 5%
R374 1.00K 1/16W 1%
PWRCTL_VCC1B_FLT
PWRCTL_VCC1A_CS
C259 0.068UF 10V X5R
R363 0 1/10W 5%
R373 1.00K 1/16W 1%
PWRCTL_VCC2B_FLT
PWRCTL_VCC2A_CS
C260 0.068UF 10V X5R
R361 0 1/10W 5%
R371 1.00K 1/16W 1%
PWRCTL_VCC3B_FLT
PWRCTL_VCC3A_CS
C261 0.068UF 10V X5R
R362 0 1/10W 5%
R372 1.00K 1/16W 1%
PWRCTL_VCC4B_FLT
PWRCTL_VCC4A_CS
C262 0.068UF 10V X5R
PWRCTL2_VCC1A_PWM
PWRCTL2_VCC1A_SRE
PWRCTL_SRE_GPIO1
PWRCTL2_VCC1A_FLT
PWRCTL2_VCC1B_FLT
PWRCTL2_VCC1_EA_P
PWRCTL2_VCC1_EA_N
PWRCTL2_VCC2A_PWM
PWRCTL2_VCC2A_SRE
PWRCTL_SRE_GPIO2
PWRCTL2_VCC2A_FLT
PWRCTL2_VCC2B_FLT
PWRCTL2_VCC2_EA_P
PWRCTL2_VCC2_EA_N
PWRCTL2_VCC3A_PWM
PWRCTL2_VCC3A_SRE
PWRCTL_SRE_GPIO3
PWRCTL2_VCC3A_FLT
PWRCTL2_VCC3B_FLT
PWRCTL2_VCC3_EA_P
PWRCTL2_VCC3_EA_N
PWRCTL2_VCC4A_PWM
PWRCTL2_VCC4A_SRE
PWRCTL_SRE_GPIO4
PWRCTL2_VCC4A_FLT
PWRCTL2_VCC4B_FLT
PWRCTL2_VCC4_EA_P
PWRCTL2_VCC4_EA_N
PWRCTL_SEQ_1
PWRCTL_SEQ_2
PWRCTL_PWRGOOD
NC
TCK
TMS
TDI
TDO
TRCK
TRST_B
ADDR-0
ADDR-1
AUX-IN_AD14
AUX-IN_AD13
ADC_REF
BPCAP
R218 10.0K 1/10W 1%
R145 86.6K 1/10W 1%
R335 75K 1/10W 1%
R211 10.0K 1/10W 1%
R212 10.0K 1/10W 1%
C89 0.1UF 25V X5R
C90 0.1UF 25V X5R
C214 0.01UF 25V X7R
PMBUS Addr = 53
U43 PFC_S_PQFP_G80 UCD9248PFC
Z6 0603_SHORT
Z7 0603_SHORT
FPGA UCD9240 PMBus Controller #2
XILINX
Title: FPGA UCD9240 PMBus Controller #2
SCHEM, ROHS COMPLIANT
VC707 EVALUATION PLATFORM
ASSY P/N: 0431663
PCB P/N: 1280586
SCH P/N: 0381418
Date: 2-3-2012_10:13
Ver: 1.0
Sheet Size: B
Rev: 01
Sheet 50 of 57
Drawn By BF





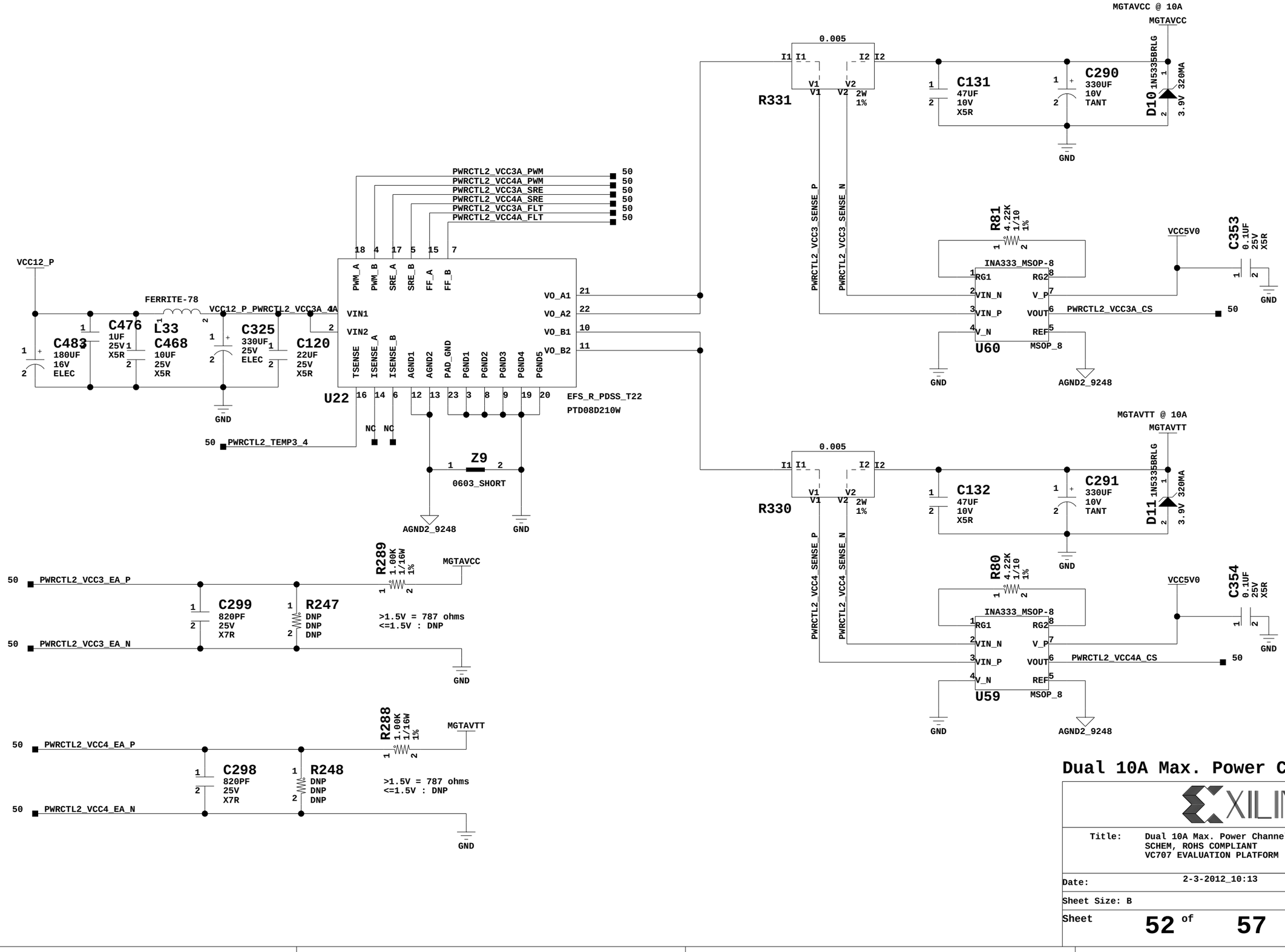




Dual 10A Max. Power Channels

XILINX

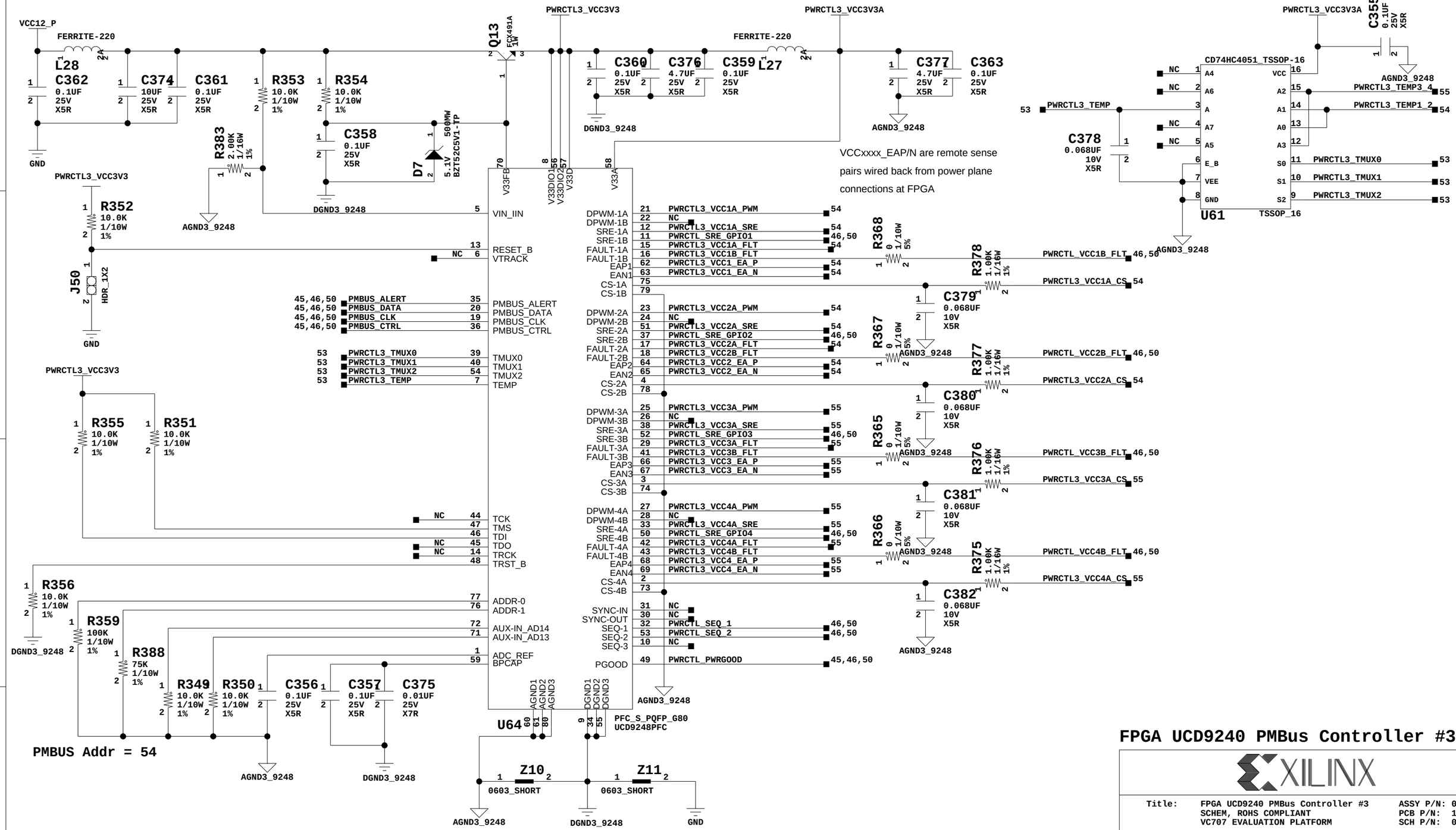
Title:	Dual 10A Max. Power Channels SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418
Date: 2-3-2012_10:13		Ver: 1.0
Sheet Size: B		Rev: 01
Sheet 51 of 57		Drawn By BF



Dual 10A Max. Power Channels

XILINX

Title:	Dual 10A Max. Power Channels SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	52 of 57	Drawn By	BF



FPGA UCD9240 PMBus Controller #3

XILINX

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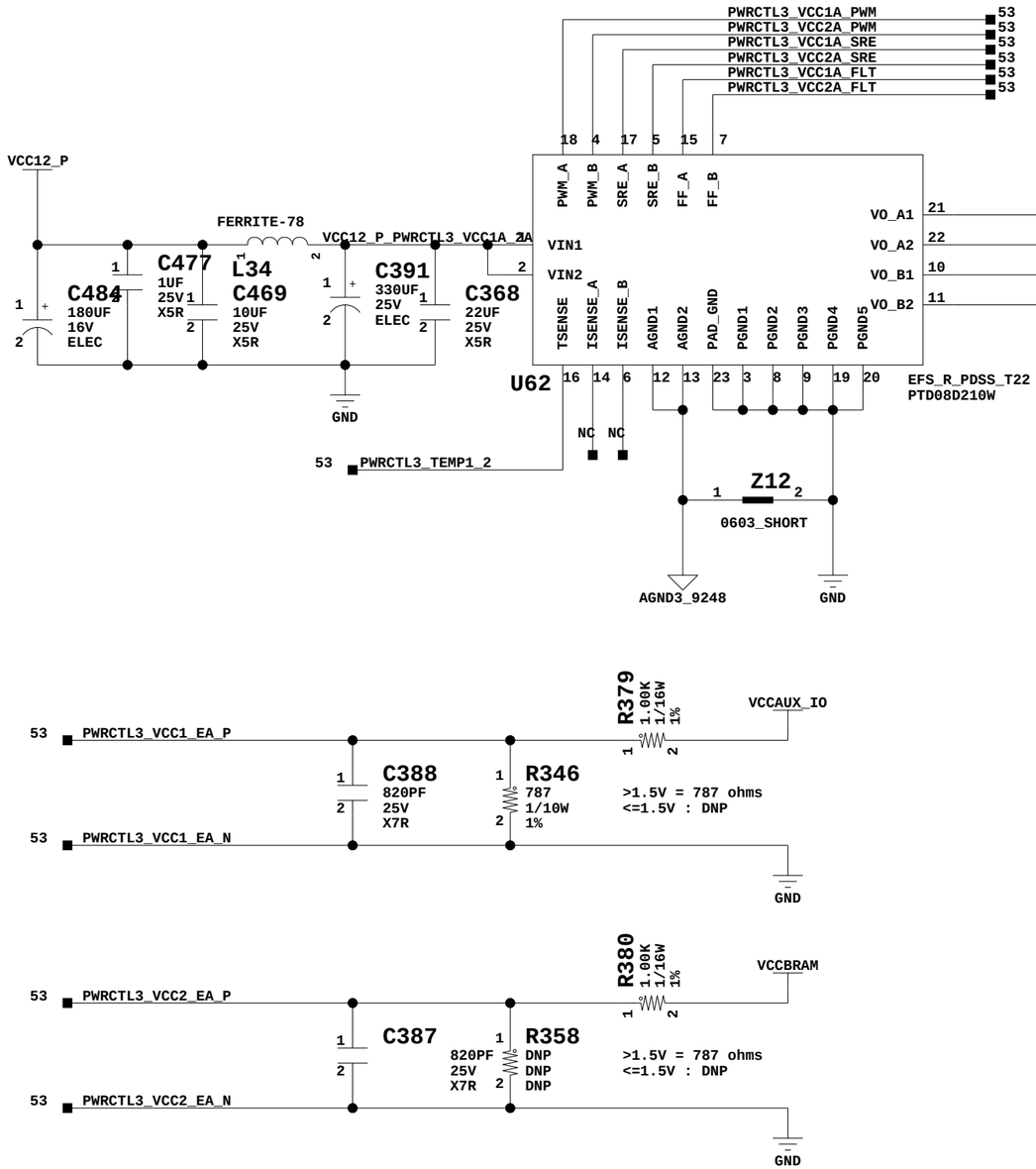
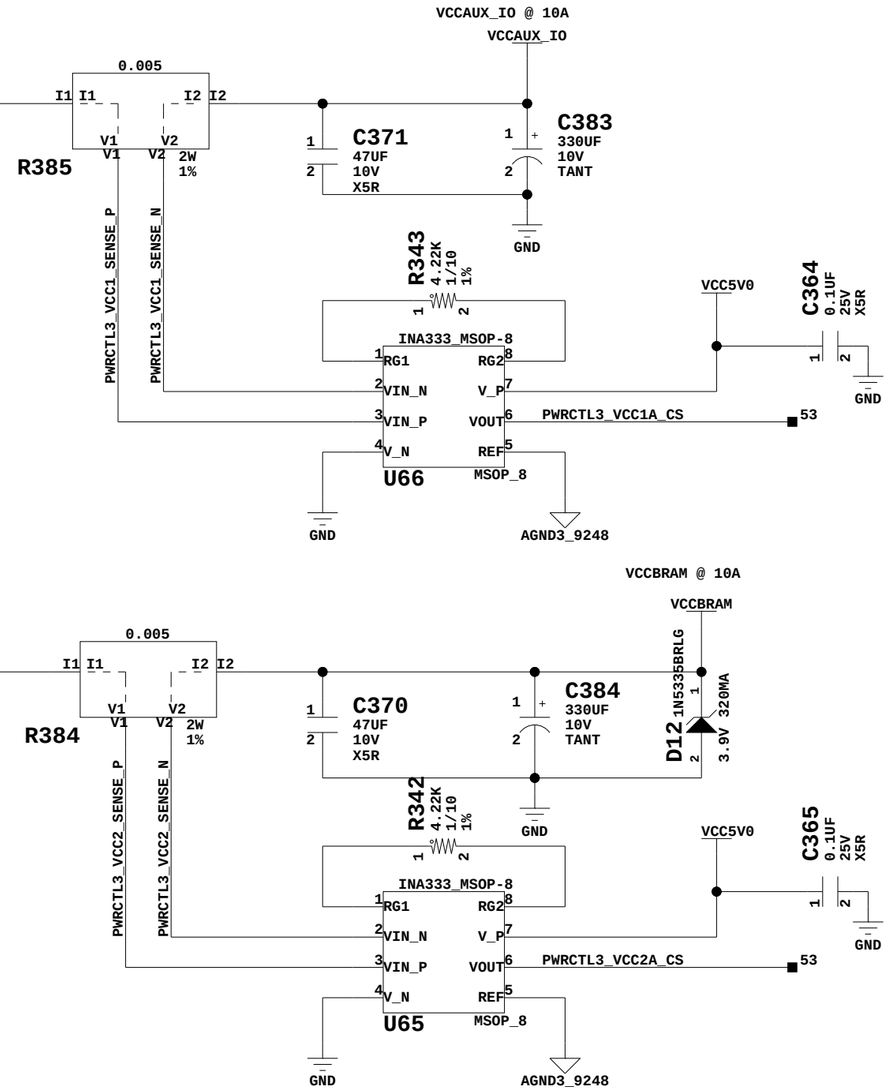
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	53 of 57	Drawn By	BF

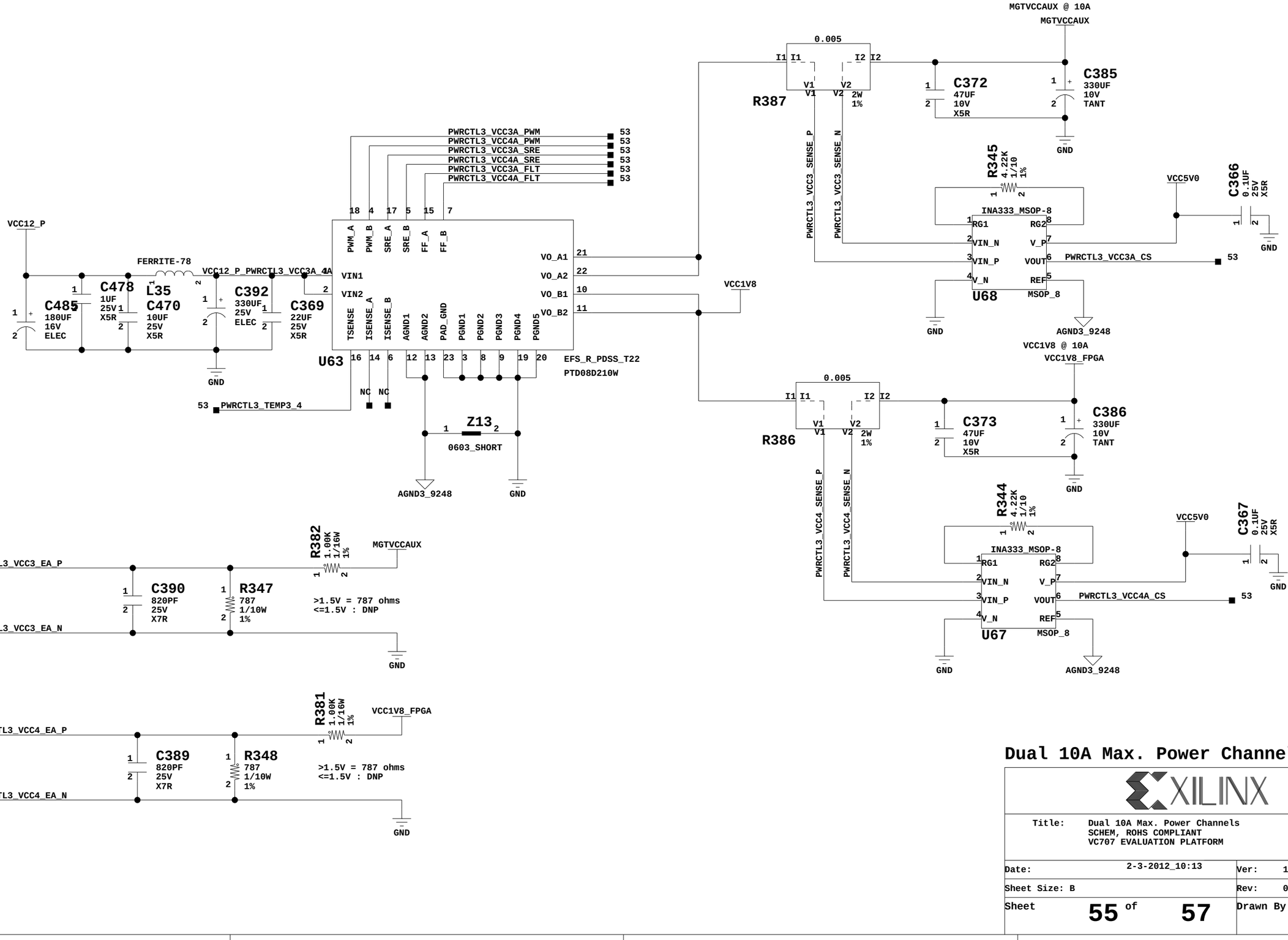




Dual 10A Max. Power Channels

XILINX

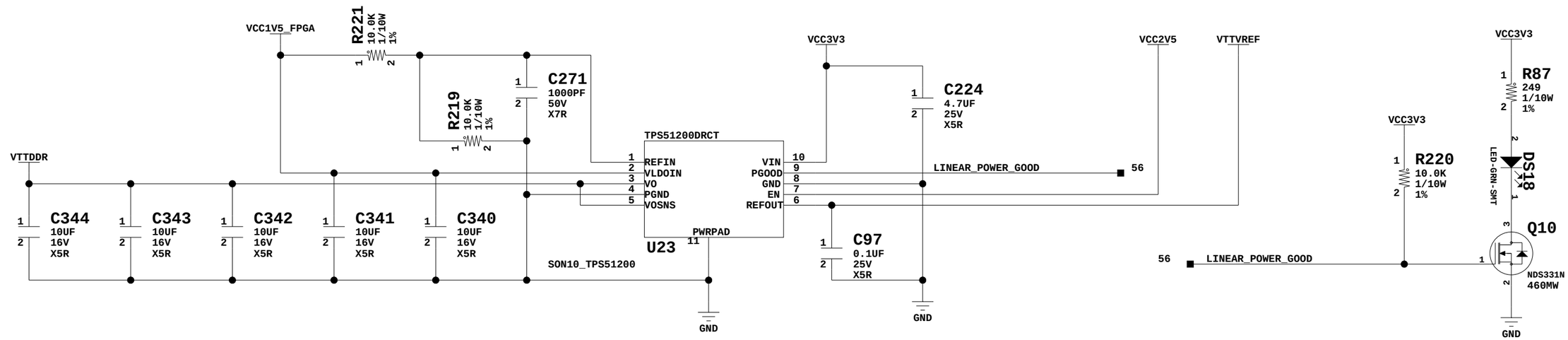
Title:	Dual 10A Max. Power Channels SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431663 1280586 0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	54 of 57	Drawn By	BF

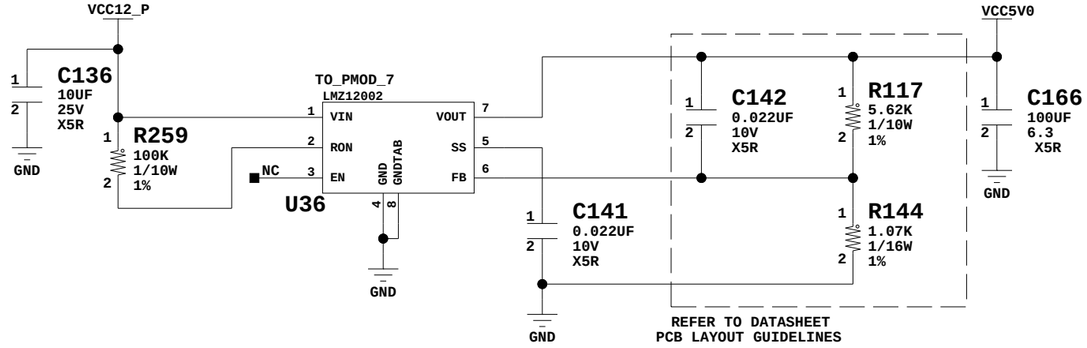


Dual 10A Max. Power Channels

XILINX

Title:	Dual 10A Max. Power Channels SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N:	0431663
		PCB P/N:	1280586
		SCH P/N:	0381418
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	55 of 57	Drawn By	BF

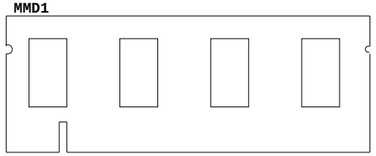




Linear Power Supplies

Title:	Linear Power Supplies SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418	
Date:	2-3-2012_10:13	Ver:	1.0
Sheet Size: B		Rev:	01
Sheet	56 of 57	Drawn By	BF

MMD1



DDR3_SODIMM

CBL1

4-Pin ATX Power — 6-Pin Molex Mini-fit Jr.

PCIe Adapter Cable

PCIE_ADAPTER_CABLE

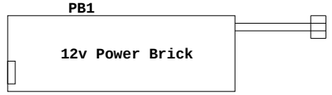
CBL2

110V Prong — IEC320-C13

Power Cord

PC_POWER_CABLE

PB1



PWR_BRICK_12V

CBL3

USB A — USB Mini-B

USB Mini-B Cable

USB_MINIB_CABLE

CBL4

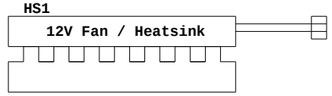
USB A — USB Mini-B

USB Mini-B Cable

USB_MINIB_CABLE

12V Fan Assembly, w/TACH Output

HS1

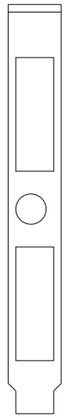


12VDC

MJB1 MJB2 MJB3 MJB4

JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN JUMPER_BLOCK_2-PIN

PL1



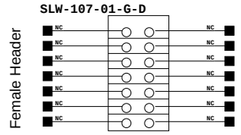
KC705_PCIE_PLATE

MSTK1

PCIE_POWER_STICKER

LCD Display Assembly

SLW-107-01-G-D

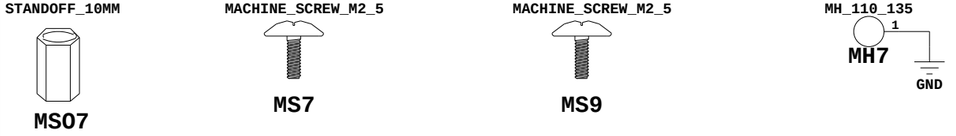


LCD1_J31

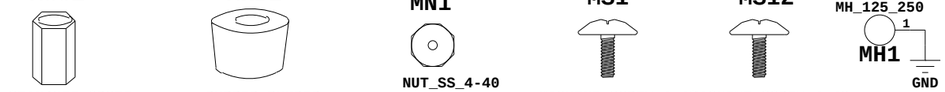
LCD1

LCD Mounting HW

STANDOFF_10MM — MACHINE_SCREW_M2_5 — MACHINE_SCREW_M2_5 — MH_110_135

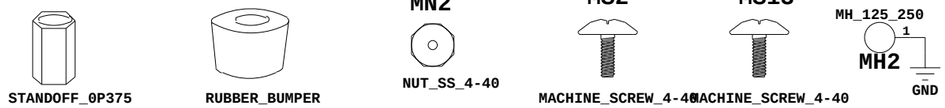


MS01 MRB1 MN1 MS1 MS12 MH_125_250 MH1



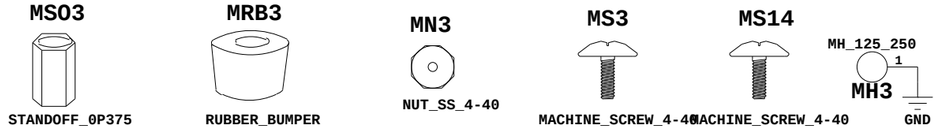
STANDOFF_0P375 — RUBBER_BUMPER — NUT_SS_4-40 — MACHINE_SCREW_4-40 — MACHINE_SCREW_4-40 — GND

MS02 MRB2 MN2 MS2 MS13 MH_125_250 MH2



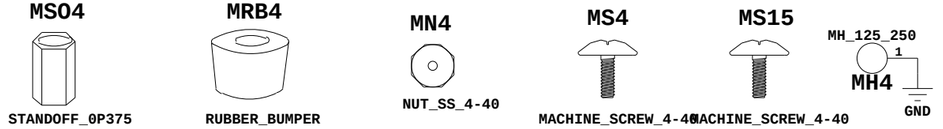
STANDOFF_0P375 — RUBBER_BUMPER — NUT_SS_4-40 — MACHINE_SCREW_4-40 — MACHINE_SCREW_4-40 — GND

MS03 MRB3 MN3 MS3 MS14 MH_125_250 MH3



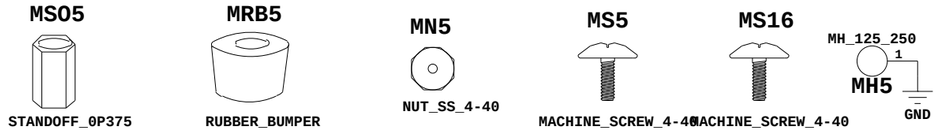
STANDOFF_0P375 — RUBBER_BUMPER — NUT_SS_4-40 — MACHINE_SCREW_4-40 — MACHINE_SCREW_4-40 — GND

MS04 MRB4 MN4 MS4 MS15 MH_125_250 MH4



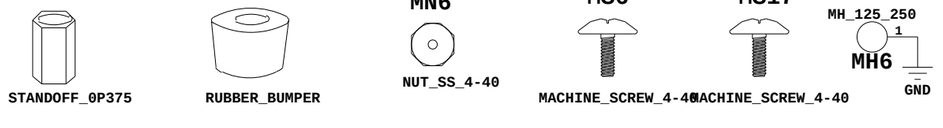
STANDOFF_0P375 — RUBBER_BUMPER — NUT_SS_4-40 — MACHINE_SCREW_4-40 — MACHINE_SCREW_4-40 — GND

MS05 MRB5 MN5 MS5 MS16 MH_125_250 MH5



STANDOFF_0P375 — RUBBER_BUMPER — NUT_SS_4-40 — MACHINE_SCREW_4-40 — MACHINE_SCREW_4-40 — GND

MS06 MRB6 MN6 MS6 MS17 MH_125_250 MH6



STANDOFF_0P375 — RUBBER_BUMPER — NUT_SS_4-40 — MACHINE_SCREW_4-40 — MACHINE_SCREW_4-40 — GND

Mechanical Components

XILINX

Title:	Mechanical Components SCHEM, ROHS COMPLIANT VC707 EVALUATION PLATFORM	ASSY P/N: 0431663 PCB P/N: 1280586 SCH P/N: 0381418
Date: 2-3-2012_10:13		Ver: 1.0
Sheet Size: B		Rev: 01
Sheet 57 of 57		Drawn By BF