

RFSoC UltraScale+ Evaluation Board

HW-Z1-ZCU208

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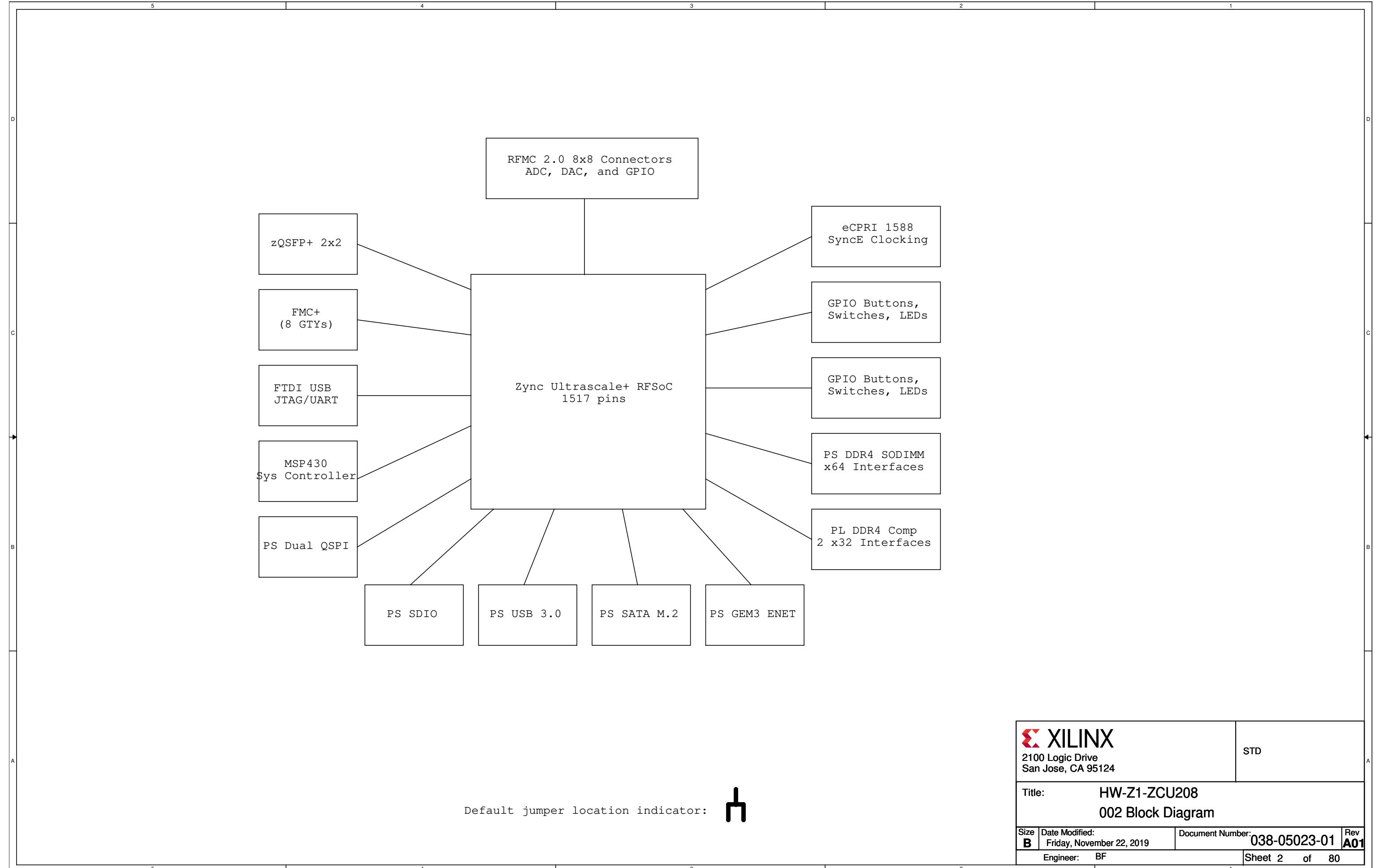
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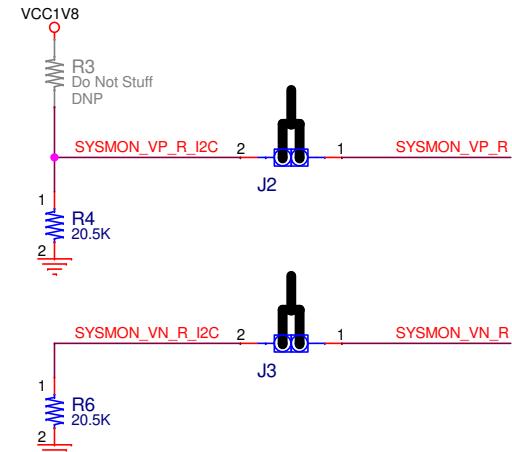
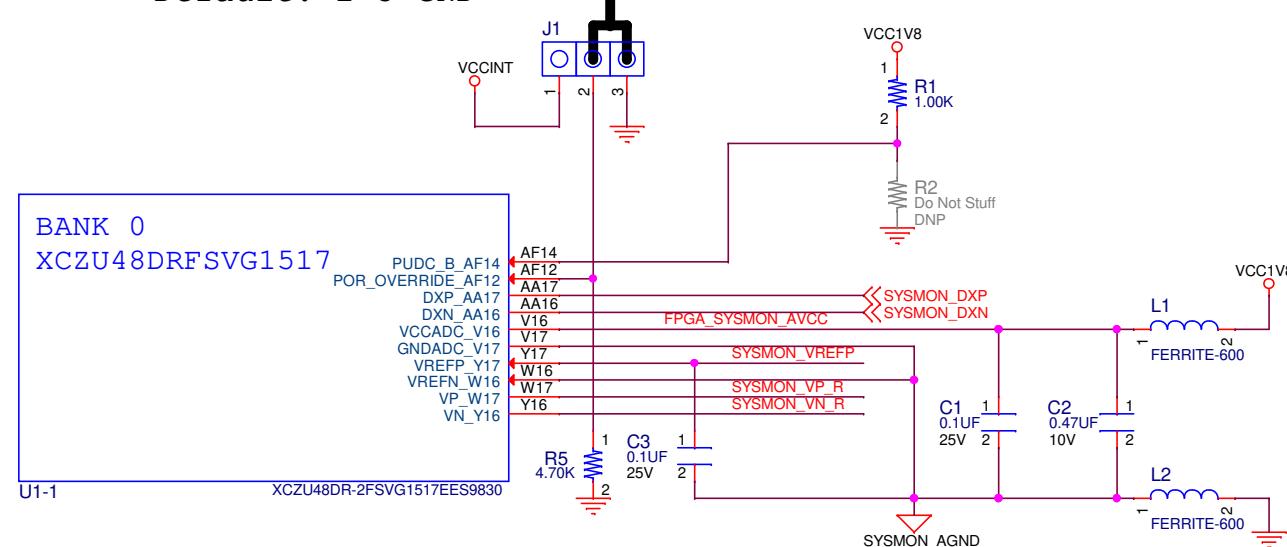
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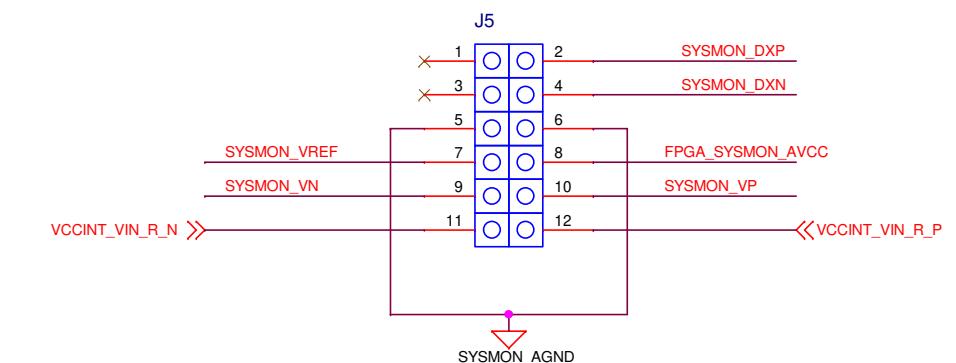
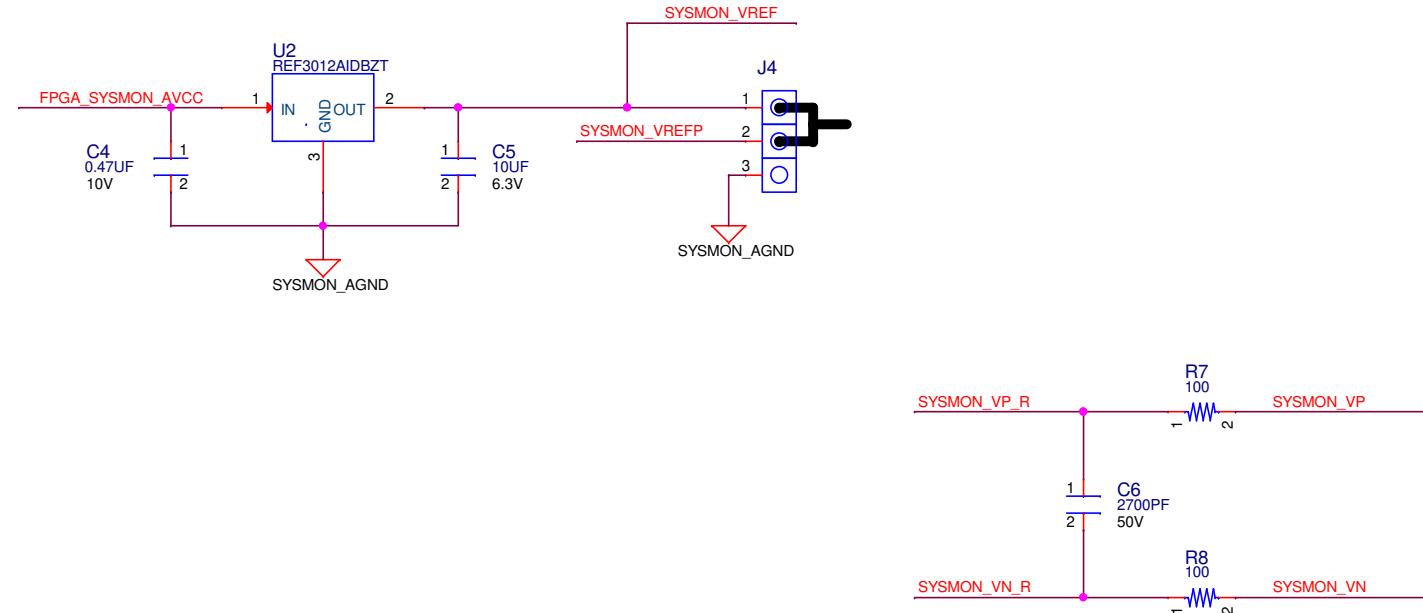


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Title: HW-Z1-ZCU208 002 Block Diagram			
Size: B	Date Modified: Friday, November 22, 2019	Document Number: 038-05023-01	Rev: A01
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POR_OVERRIDE select
Default: 2-3 GND



SYSMON I2C Address jumpers



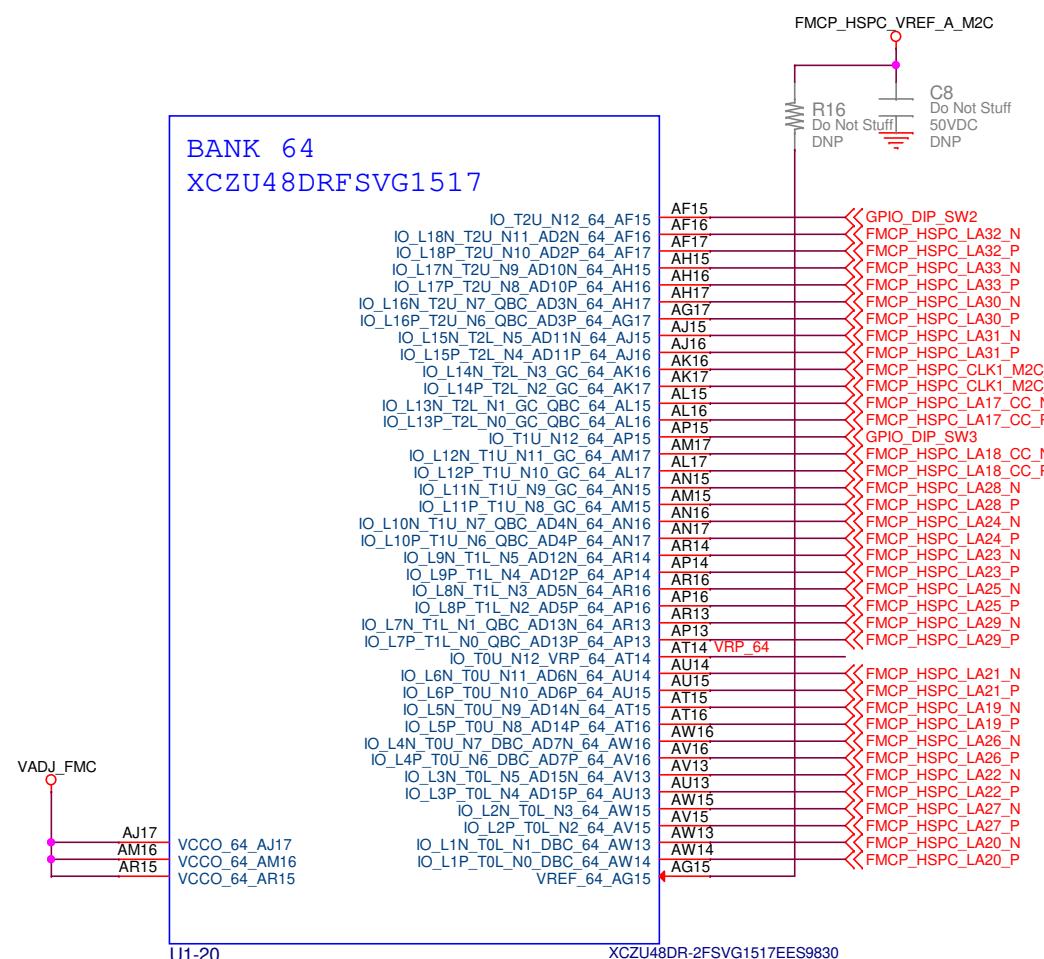
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Title: HW-Z1-ZCU208
003 Zynq Bank 0

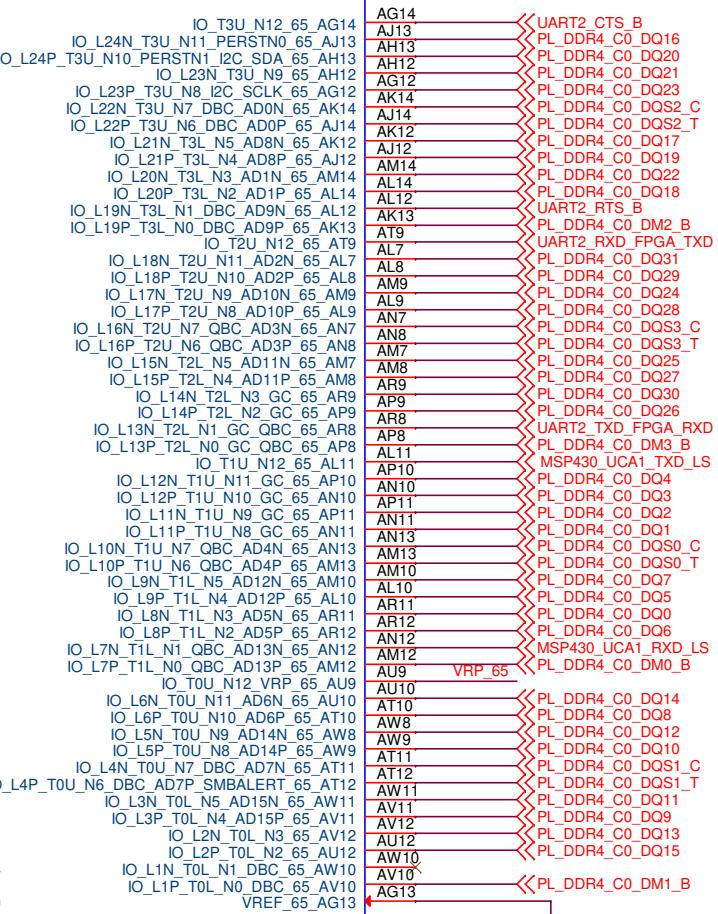
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BANK 64
XCZU48DRF SVG1517

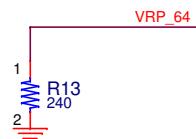


XCZU48DR-2FSVG1517EES9830

BANK 65
XCZU48DRF SVG1517



XCZU48DR-2FSVG1517EES9830



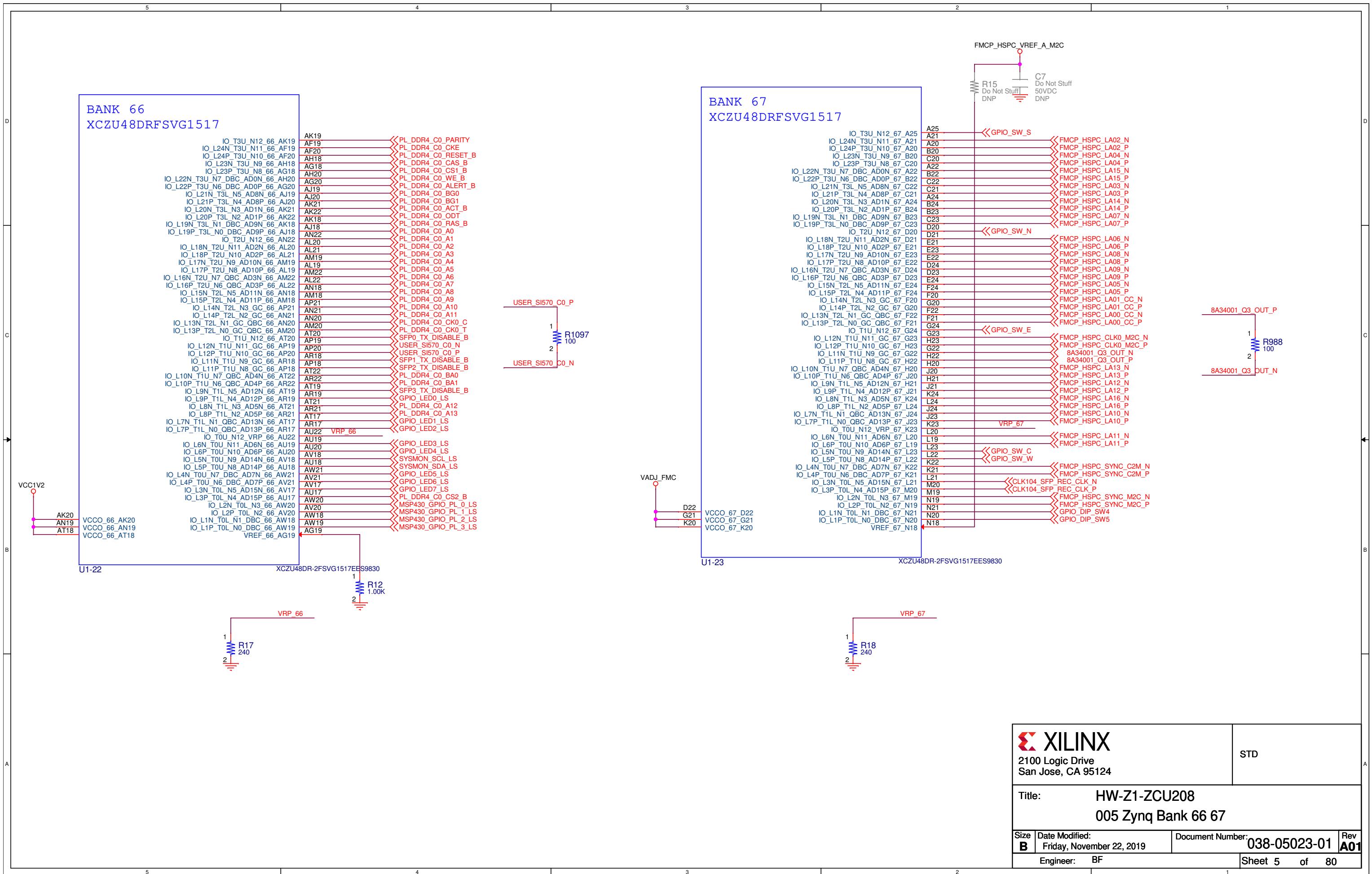
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Title: **HW-Z1-ZCU208**
004 Zynq Bank 64 65

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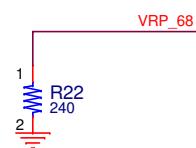
BANK 68
XCZU48DRF SVG1517

IO_T3U_N12_68_C11
IO_L24N_T3U_N11_68_A14
IO_L24P_T3U_N10_68_A15
IO_L23N_T3U_N9_68_A11
IO_L23P_T3U_N8_68_A12
IO_L22N_T3U_N7_DBC_AD0N_68_B15
IO_L22P_T3U_N6_DBC_AD0P_68_C15
IO_L21N_T3L_N5_AD8N_68_B13
IO_L21P_T3L_N4_AD8P_68_B14
IO_L20N_T3L_N3_AD1N_68_C13
IO_L20P_T3L_N2_AD1P_68_D13
IO_L19N_T3L_N1_DBC_AD9N_68_B12
IO_L19P_T3L_N0_DBC_AD9P_68_C12
IO_T2U_N12_68_D11
IO_L18N_T2U_N11_AD2N_68_D14
IO_L18P_T2U_N10_AD2P_68_E14
IO_L17N_T2U_N9_AD10N_68_E11
IO_L16N_T2U_N7_QBC_AD3N_68_E12
IO_L16P_T2U_N6_QBC_AD3P_68_E13
IO_L15N_T2L_N5_AD11N_68_F14
IO_L15P_T2L_N4_AD11P_68_G14
IO_L14N_T2L_N3_GC_68_H12
IO_L14P_T2L_N2_GC_68_H13
IO_L13N_T2L_N1_GC_QBC_68_G12
IO_L13P_T2L_N0_GC_QBC_68_G13
IO_T1U_N12_68_G10
IO_L12N_T1U_N11_GC_68_H10
IO_L12P_T1U_N10_GC_68_H11
IO_L11N_T1U_N9_GC_68_J10
IO_L11P_T1U_N8_GC_68_J11
IO_L10N_T1U_N7_QBC_AD4N_68_J13
IO_L10P_T1U_N6_QBC_AD4P_68_J14
IO_L9N_T1L_N5_AD12N_68_F10
IO_L9P_T1L_N4_AD12P_68_F11
IO_L8N_T1L_N3_AD5N_68_K10
IO_L8P_T1L_N2_AD5P_68_K11
IO_L7N_T1L_N1_QBC_AD13N_68_K12
IO_L7P_T1L_N0_QBC_AD13P_68_K13
IO_TOU_N12_VRP_68_F7
IO_L6N_TOU_N11_AD6N_68_F9
IO_L6P_TOU_N10_AD6P_68_G9
IO_L5N_TOU_N9_AD14N_68_G6
IO_L5P_TOU_N8_AD14P_68_G7
IO_L4N_TOU_N7_DBC_AD7N_68_G8
IO_L4P_TOU_N6_DBC_AD7P_68_H8
IO_L3N_TOL_N5_AD15N_68_H6
IO_L3P_TOL_N4_AD15P_68_H7
IO_L2N_TOL_N3_68_J9
IO_L2P_TOL_N2_68_K9
IO_L1N_TOL_N1_DBC_68_J7
IO_L1P_TOL_N0_DBC_68_J8
VREF_68_K14

VCC1V2
D12
G11
H14
VCCO_68_D12
VCCO_68_G11
VCCO_68_H14

U1-24

XCZU48DR-2FVG1517EES9830



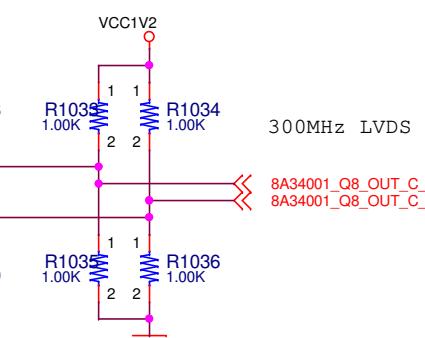
VRP_68

1
R20
1.00K
2

VRP_68

1
R21
1.00K
2

VRP_69



BANK 69
XCZU48DRF SVG1517

IO_T3U_N12_69_D19
IO_L24N_T3U_N11_69_A16
IO_L24P_T3U_N10_69_A17
IO_L23N_T3U_N9_69_D15
IO_L23P_T3U_N8_69_D16
IO_L22N_T3U_N7_DBC_AD0N_69_B17
IO_L22P_T3U_N6_DBC_AD0P_69_B18
IO_L21N_T3L_N5_AD8N_69_C16
IO_L21P_T3L_N4_AD8P_69_C17
IO_L20N_T3L_N3_AD1N_69_A19
IO_L20P_T3L_N2_AD1P_69_B19
IO_L19N_T3L_N1_DBC_AD9N_69_C18
IO_L19P_T3L_N0_DBC_AD9P_69_D18
IO_T2U_N12_69_E11
IO_L18N_T2U_N11_AD2N_69_E12
IO_L18P_T2U_N10_AD2P_69_E13
IO_L17N_T2U_N9_AD10N_69_E14
IO_L16N_T2U_N7_QBC_AD3N_69_E15
IO_L16P_T2U_N6_QBC_AD3P_69_E16
IO_L15N_T2L_N5_AD11N_69_F14
IO_L15P_T2L_N4_AD11P_69_G14
IO_L14N_T2L_N3_GC_68_H12
IO_L14P_T2L_N2_GC_68_H13
IO_L13N_T2L_N1_GC_QBC_68_G12
IO_L13P_T2L_N0_GC_QBC_68_G13
IO_T1U_N12_69_G10
IO_L12N_T1U_N11_GC_68_H10
IO_L12P_T1U_N10_GC_68_H11
IO_L11N_T1U_N9_GC_68_J10
IO_L11P_T1U_N8_GC_68_J11
IO_L10N_T1U_N7_QBC_AD4N_68_J13
IO_L10P_T1U_N6_QBC_AD4P_68_J14
IO_L9N_T1L_N5_AD12N_68_F10
IO_L9P_T1L_N4_AD12P_68_F11
IO_L8N_T1L_N3_AD5N_68_K10
IO_L8P_T1L_N2_AD5P_68_K11
IO_L7N_T1L_N1_QBC_AD13N_68_K12
IO_L7P_T1L_N0_QBC_AD13P_68_K13
IO_TOU_N12_VRP_69_F7
IO_L6N_TOU_N11_AD6N_68_F9
IO_L6P_TOU_N10_AD6P_68_G9
IO_L5N_TOU_N9_AD14N_68_G6
IO_L5P_TOU_N8_AD14P_68_G7
IO_L4N_TOU_N7_DBC_AD7N_68_G8
IO_L4P_TOU_N6_DBC_AD7P_68_H8
IO_L3N_TOL_N5_AD15N_68_H6
IO_L3P_TOL_N4_AD15P_68_H7
IO_L2N_TOL_N3_68_J9
IO_L2P_TOL_N2_68_K9
IO_L1N_TOL_N1_DBC_68_J7
IO_L1P_TOL_N0_DBC_68_J8
VREF_69_K14

VCC1V2
E15
F18
J17
VCCO_69_E15
VCCO_69_F18
VCCO_69_J17

U1-25

XCZU48DR-2FVG1517EES9830

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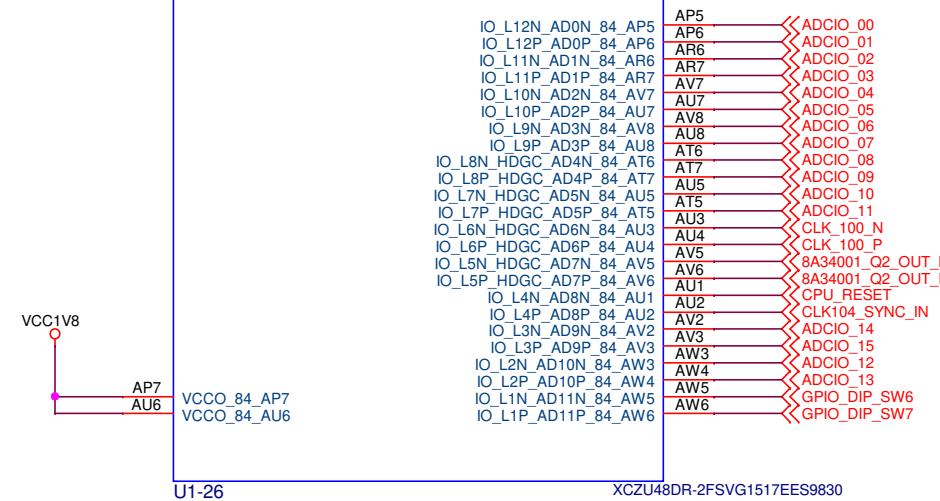
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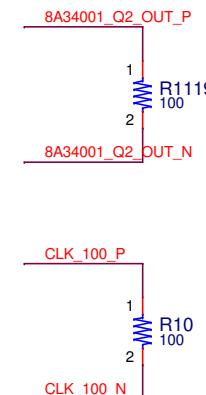
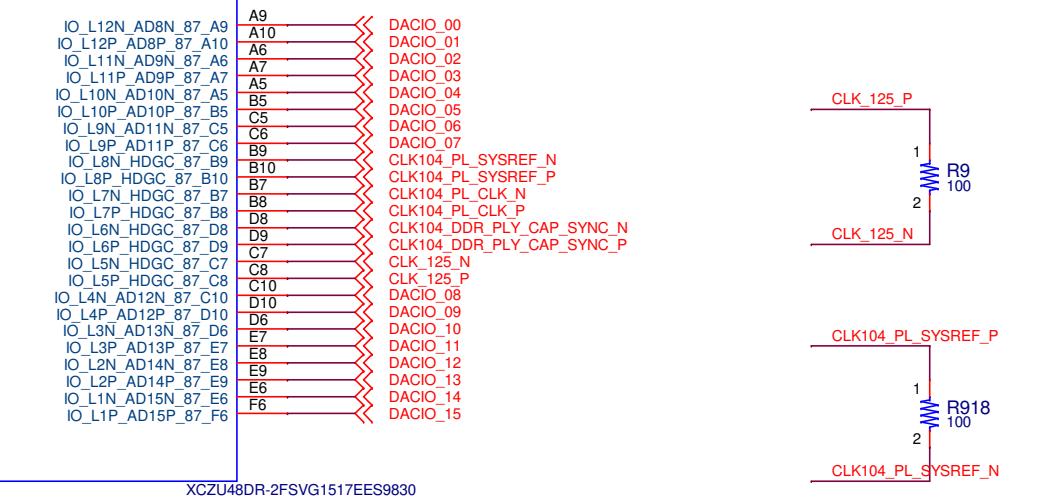
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006 Zynq Bank 68 69

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BANK 84
XCZU48DRFSVG1517



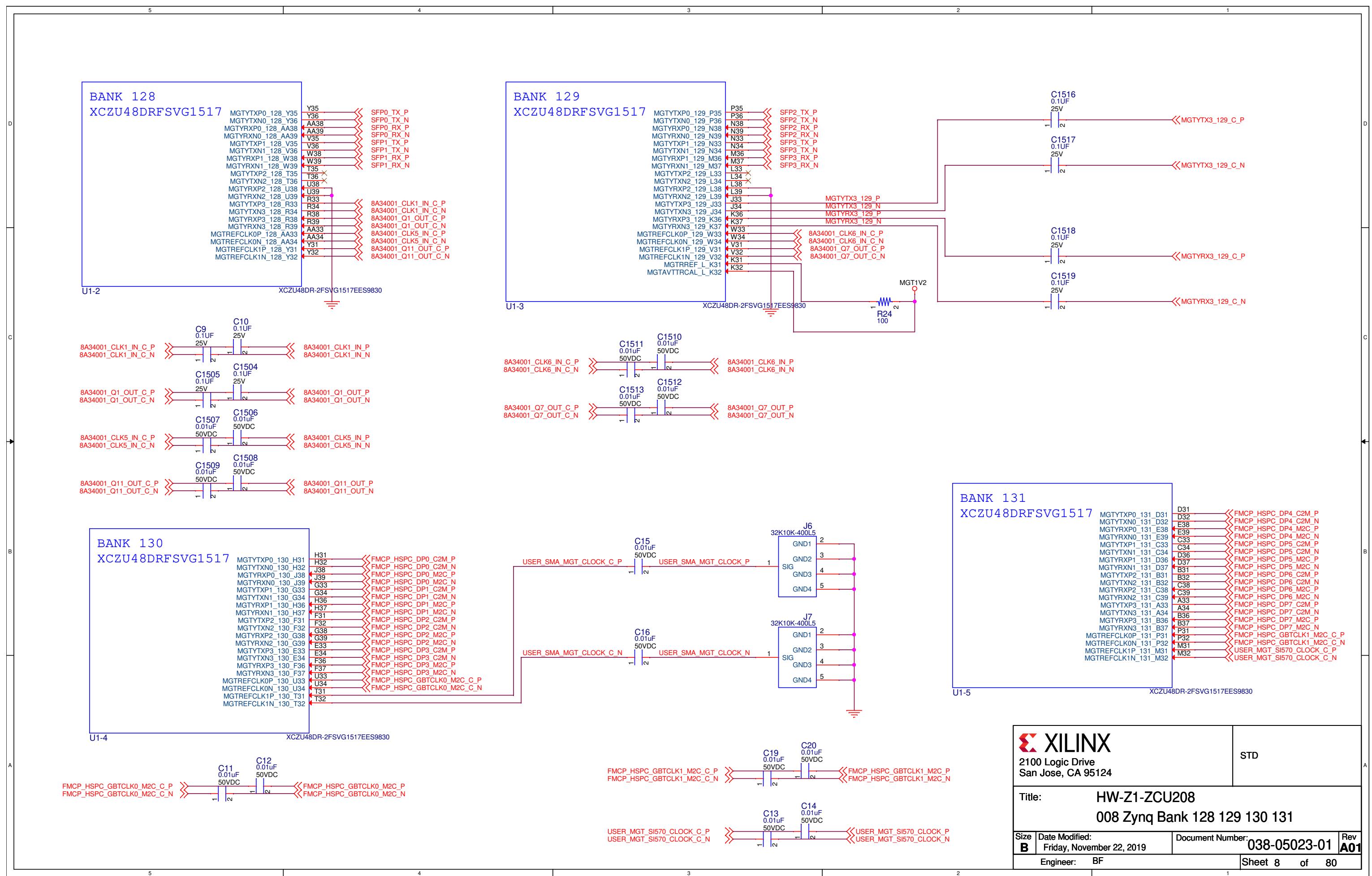
BANK 87
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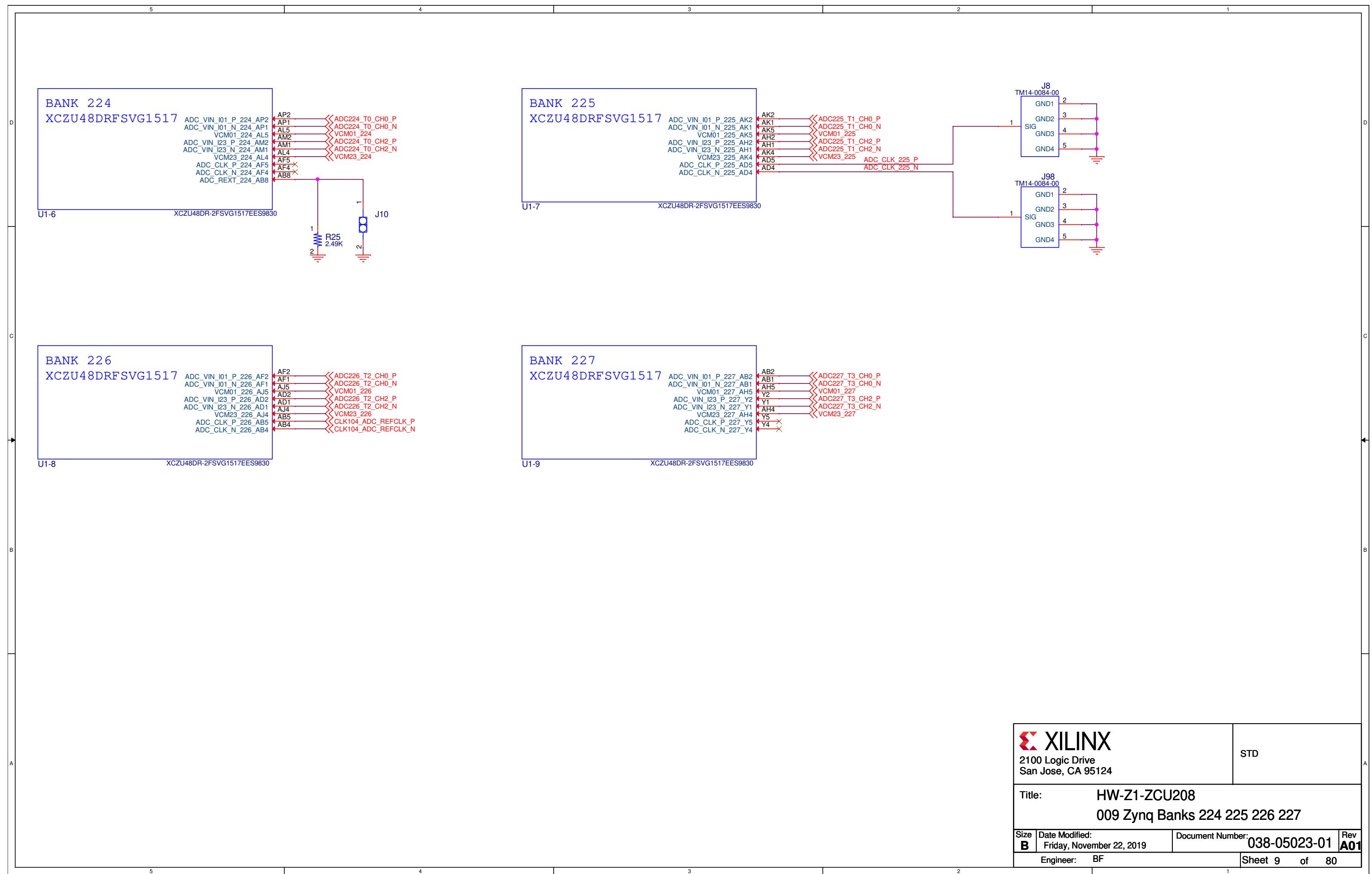


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Title: HW-Z1-ZCU208
007 Zynq Banks 84 87 88 89

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BANK 228

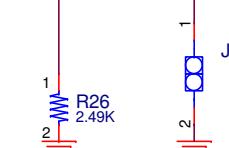
XCZU48DRF SVG1517

DAC_VOUT0_P_228_U2
DAC_VOUT0_N_228_U1
DAC_VOUT2_P_228_R2
DAC_VOUT2_N_228_R1
SYSREF_P_228_U5
SYSREF_N_228_U4
DAC_CLK_P_228_R5
DAC_CLK_N_228_R4
DAC_REXT_228_W8

U1-10

XCZU48DR-2FSVG1517EES9830

U1 DAC228_TO_CH0_P
U1 DAC228_TO_CH0_N
R2 DAC228_TO_CH2_P
R1 DAC228_TO_CH2_N
U5 CLK104_AMS_SYSREF_C_P
U4 CLK104_AMS_SYSREF_C_N
R5 CLK104_DAC_REFCLK_P
R4 CLK104_DAC_REFCLK_N
W8



R1056
CLK104_AMS_SYSREF_C
CLK104_AMS_SYSREF_C
CLK104_AMS_SYSREF_P
CLK104_AMS_SYSREF_N

0 ohms for DC connection

BANK 229

XCZU48DRF SVG1517

DAC_VOUT0_P_229_N2
DAC_VOUT0_N_229_N1
DAC_VOUT2_P_229_L2
DAC_VOUT2_N_229_L1

U1-11

XCZU48DR-2FSVG1517EES9830

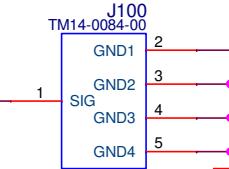
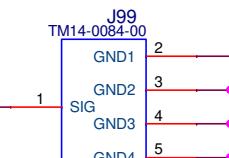
BANK 230

XCZU48DRF SVG1517

J2
J1 DAC230_T2_CH0_P
DAC_VOUT0_N_230_J1
DAC_VOUT2_P_230_G2
DAC_VOUT2_N_230_G1
DAC_CLK_P_230_N5
DAC_CLK_N_230_N4

U1-12

XCZU48DR-2FSVG1517EES9830



BANK 231

XCZU48DRF SVG1517

E2 DAC231_T3_CH0_P
E1 DAC231_T3_CH0_N
C2 DAC231_T3_CH2_P
C1 DAC231_T3_CH2_N

U1-13

XCZU48DR-2FSVG1517EES9830

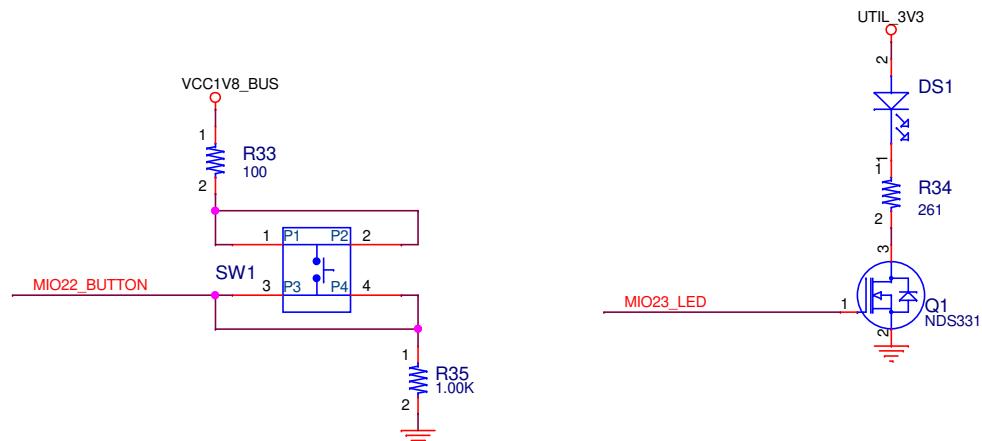
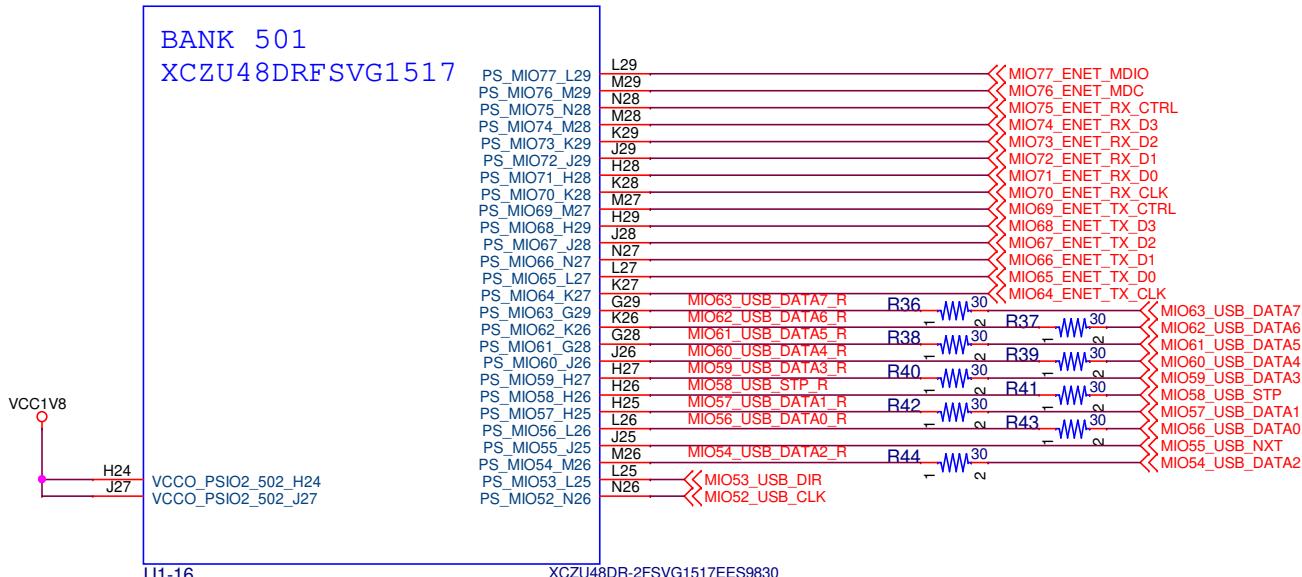
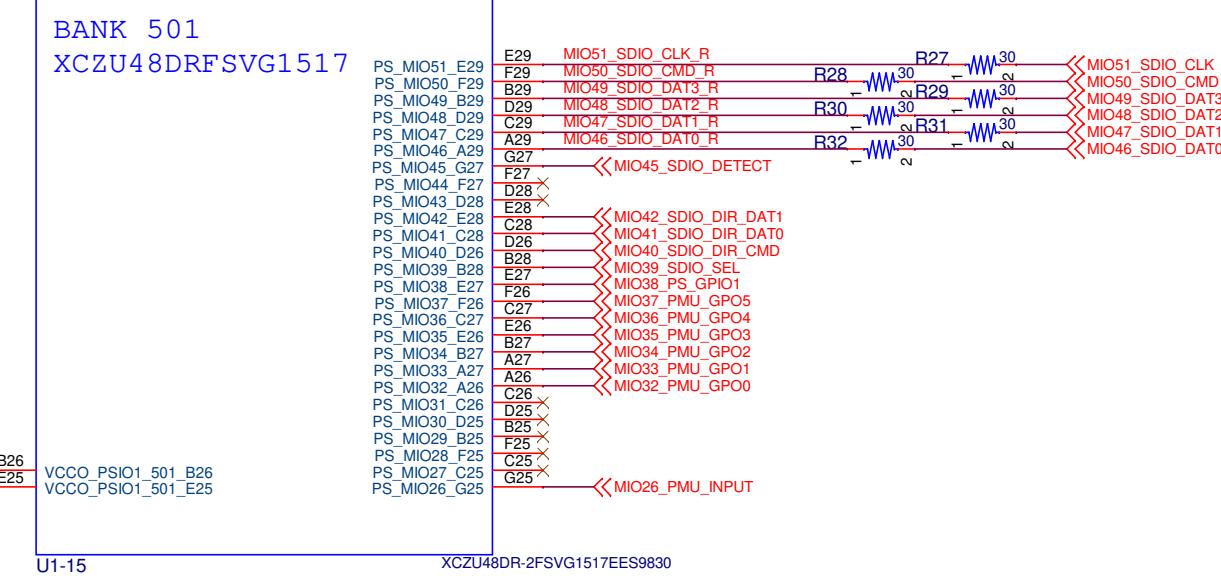
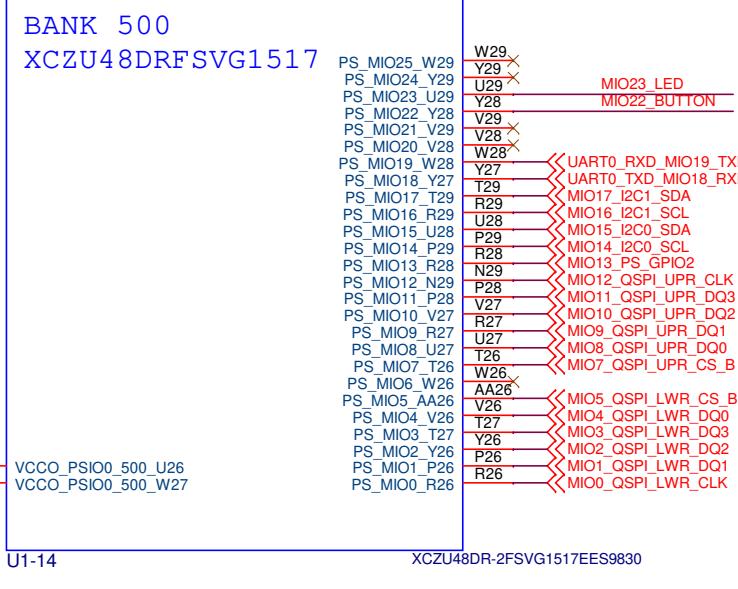


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010 Zynq Banks 228 229 230 231

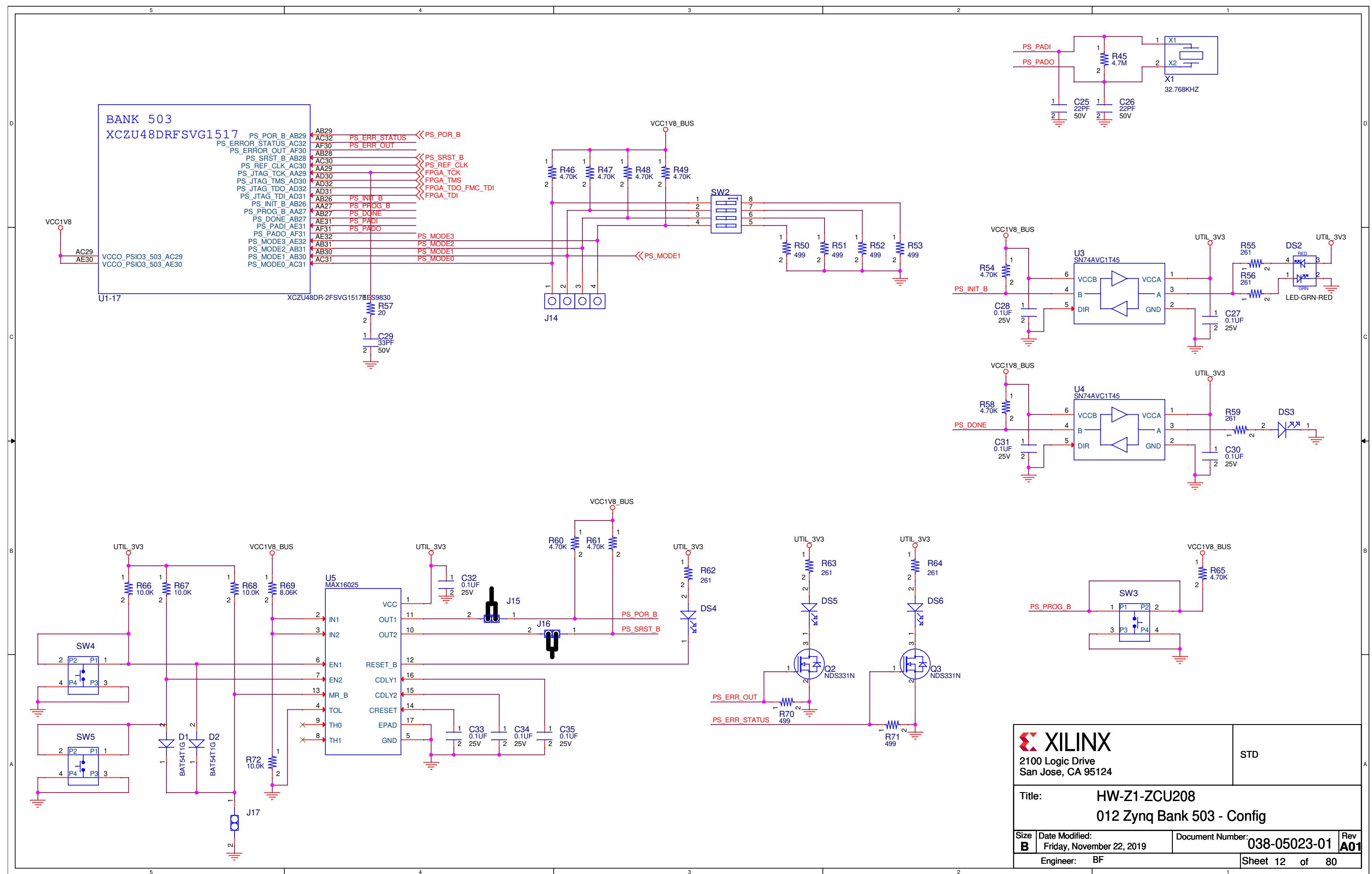
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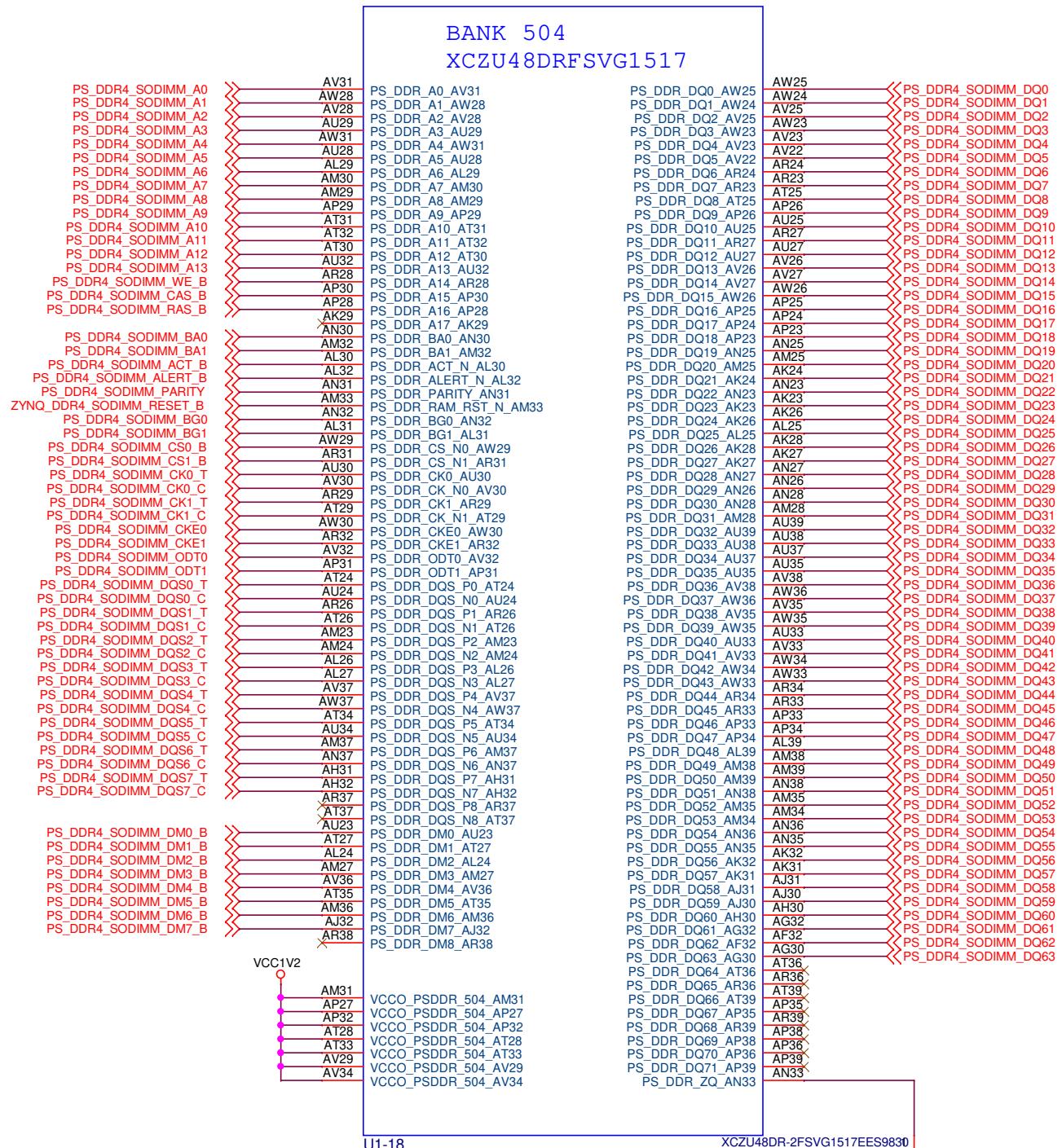


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Title: **HW-Z1-ZCU208**
011 Zynq Bank 500 501 502 - MIO

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U1-

XCZU48DR-2FSVG1517EES

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STD

Title: HW-Z1-ZCU208

013 Zynq Bank 504 - Memory

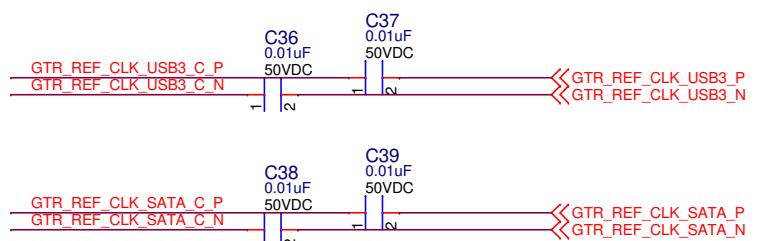
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BANK 505

XCZU48DRFSGV1517

PS_MGTRTXP0_505_AK36
 PS_MGTRTXN0_505_AK37
 PS_MGTRXP0_505_AJ38
 PS_MGTRRXN0_505_AJ39
 PS_MGTRTXP1_505_AH36
 PS_MGTRTXN1_505_AH37
 PS_MGTRXP1_505_AG38
 PS_MGTRRXN1_505_AG39
 PS_MGTRXP2_505_AF36
 PS_MGTRTXN2_505_AF37
 PS_MGTRRXP2_505_AE38
 PS_MGTRRXN2_505_AE39
 PS_MGTRXP3_505_AD36
 PS_MGTRTXN3_505_AD37
 PS_MGTRXP3_505_AC38
 PS_MGTRRXN3_505_AC39
 PS_MGTREFCLKOP_505_AJ34
 PS_MGTREFCLKON_505_AJ35
 PS_MGTREFCLK1P_505_AG34
 PS_MGTREFCLK1N_505_AG35
 PS_MGTREFCLK2P_505_AE34
 PS_MGTREFCLK2N_505_AE35
 PS_MGTREFCLK3P_505_AC34
 PS_MGTREFCLK3N_505_AC35
 PS_MGTRREF_505_AK34

U1-19
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 1 R74 500
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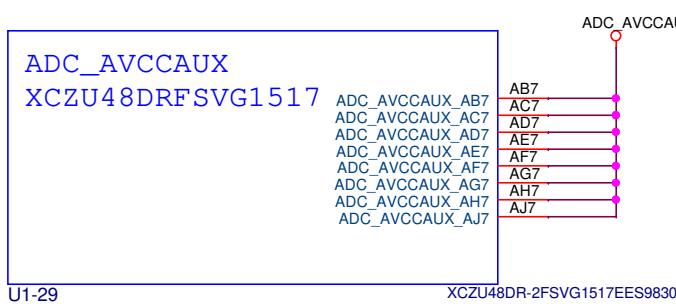
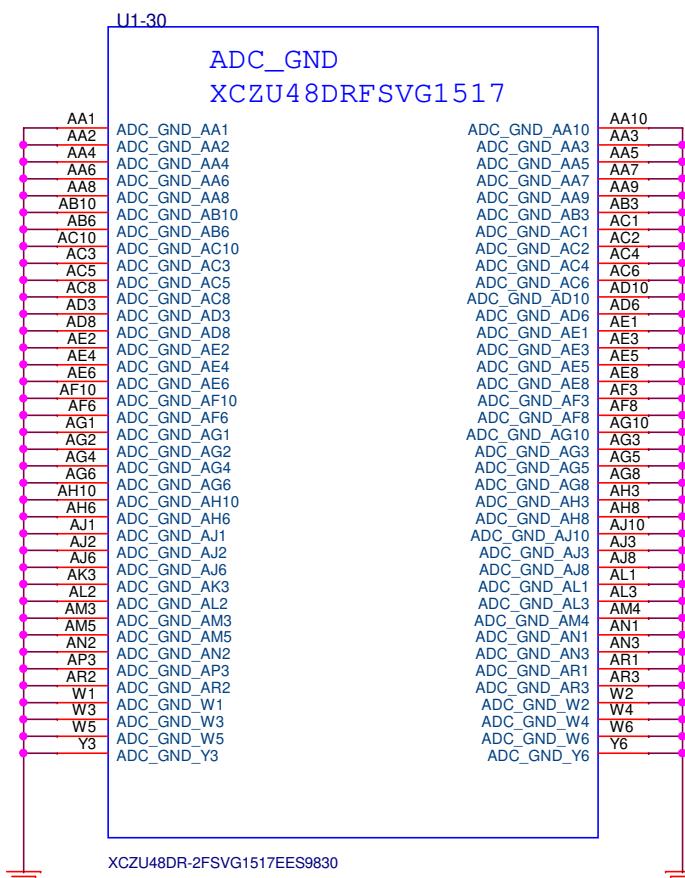
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STD

Title: HW-Z1-ZCU208
014 Zynq Bank 505 - GTR

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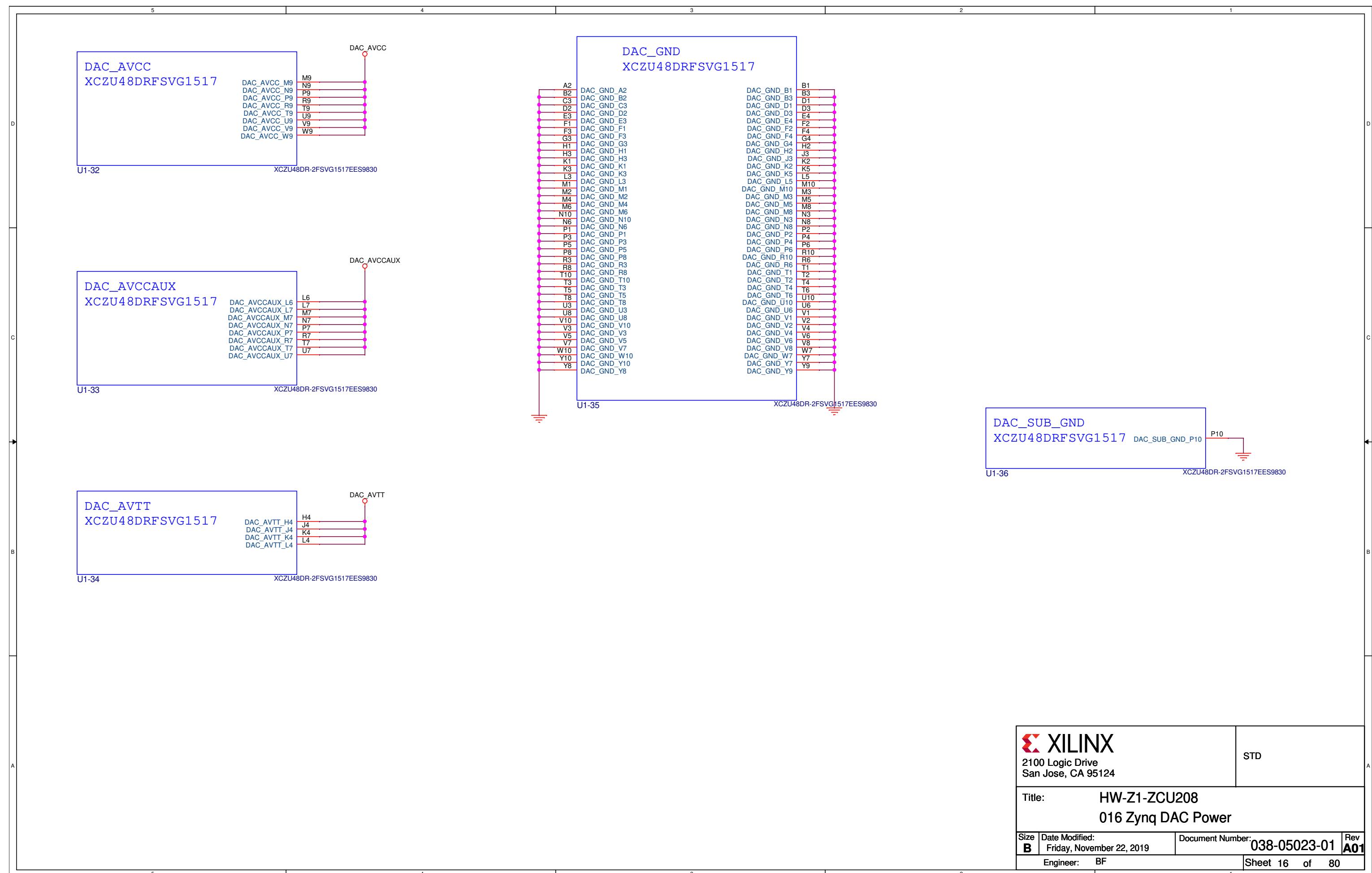

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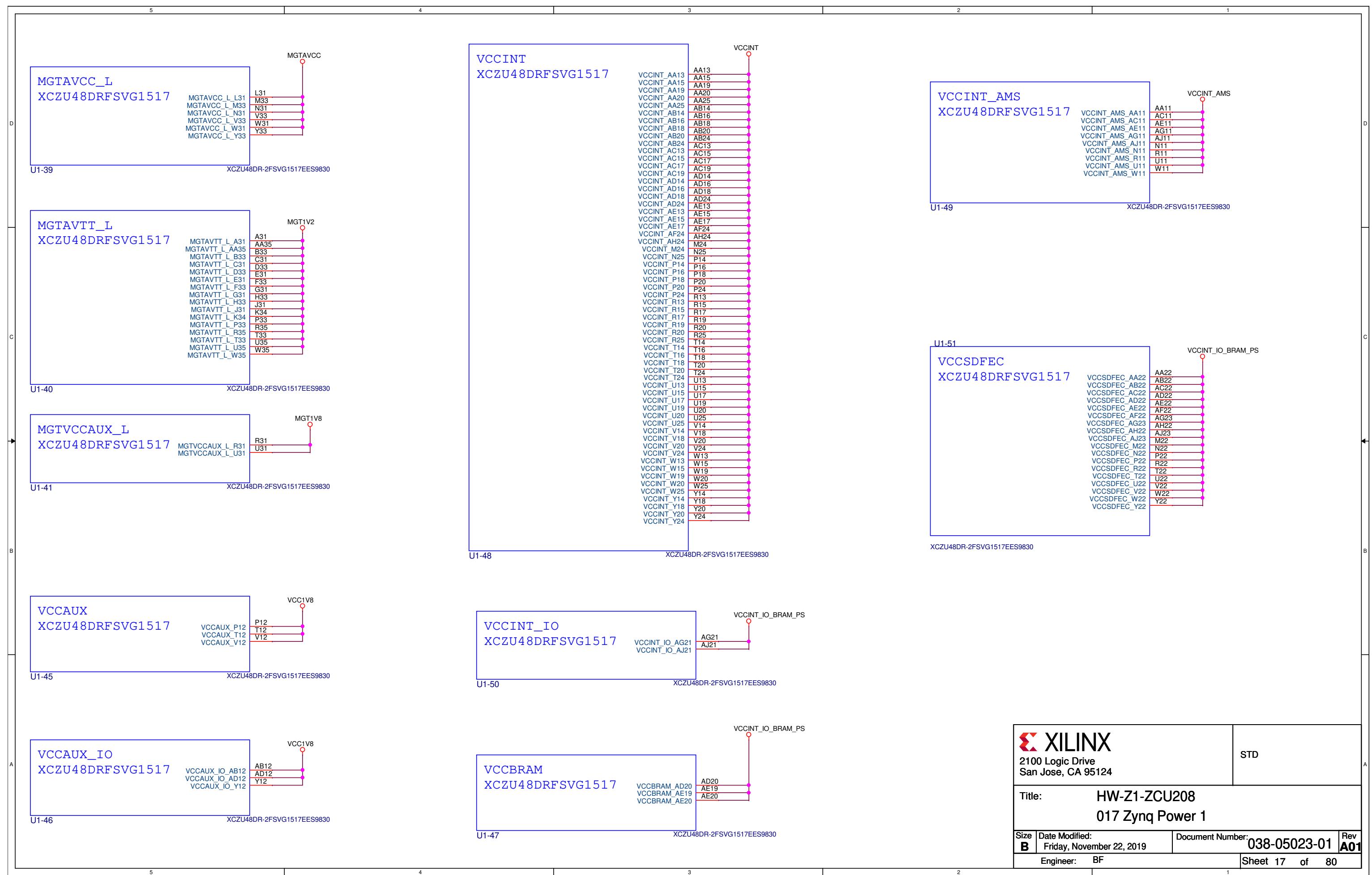
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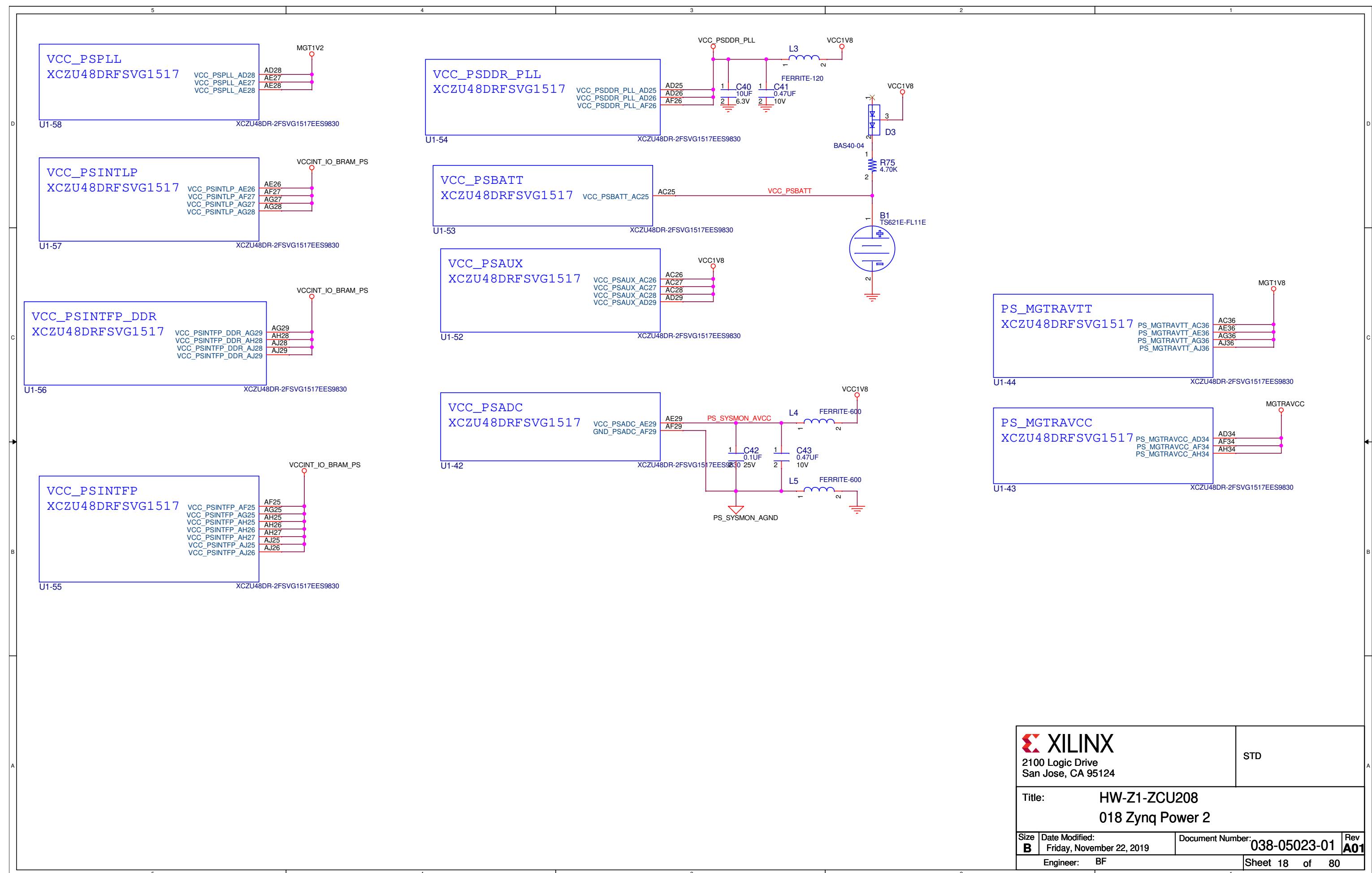
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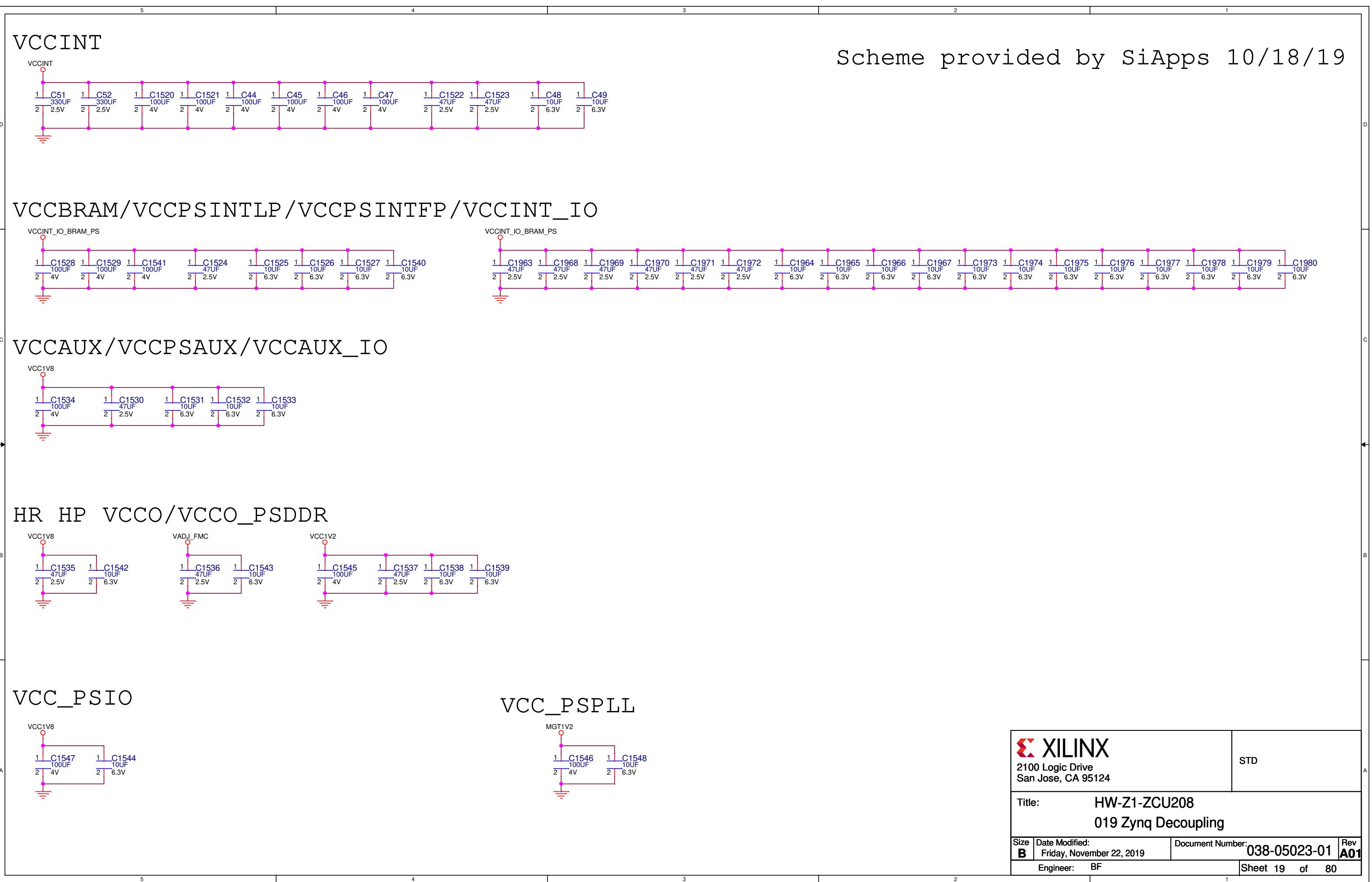
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015 Zynq ADC Power

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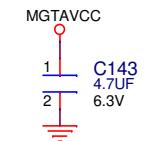




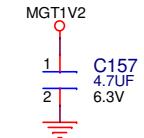




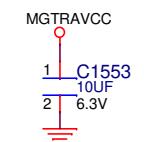
MGTAVCC



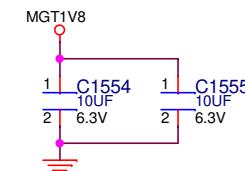
MGTAVTT/VCCPSPLL



MGTRAVCC

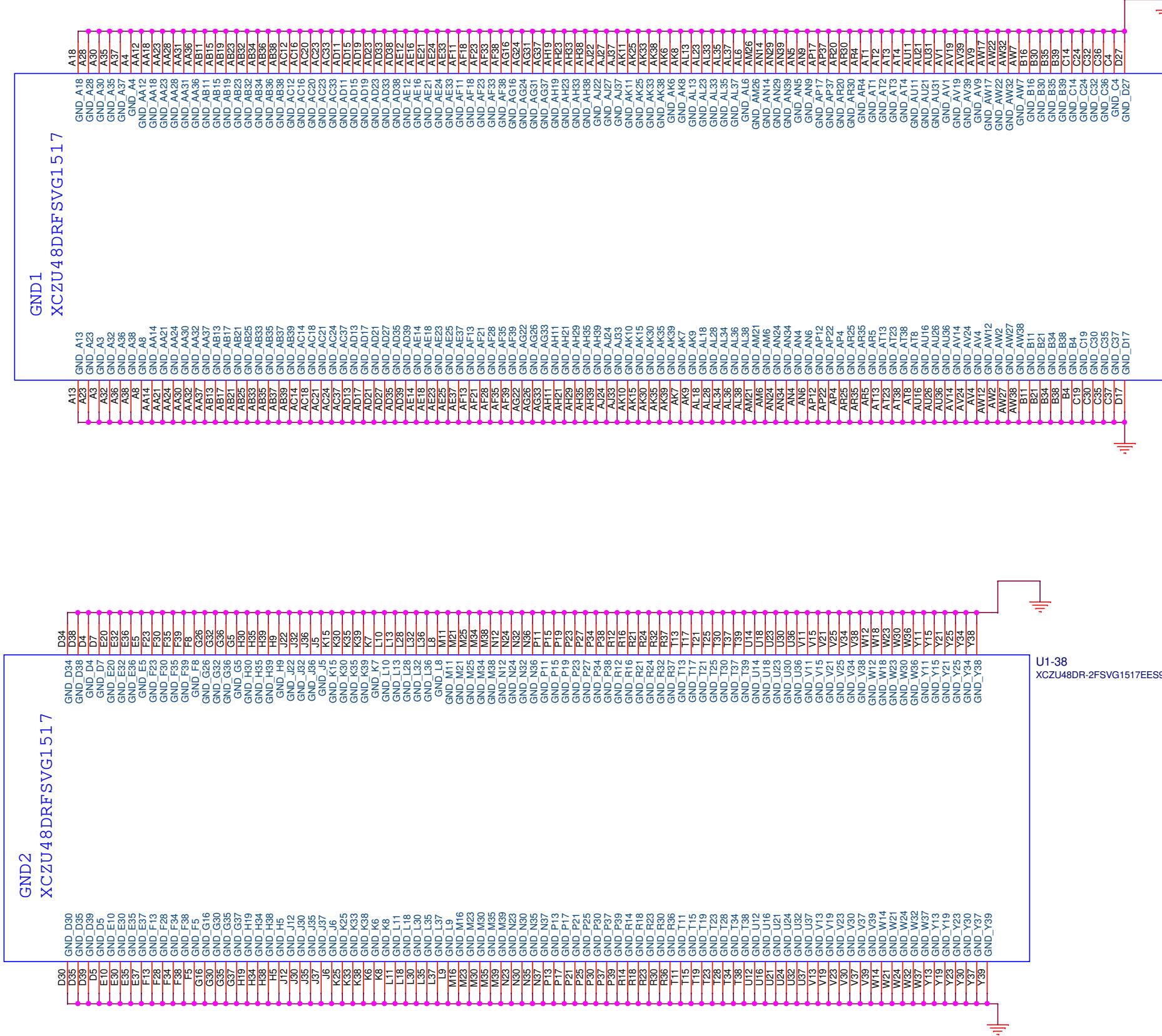


MGTVCCAUX/MGTRAVTT



AMS Scheme from UG583 1.15
GTY scheme from UG567 1.3
GTR scheme from Si Apps 5/10/19

		STD
Title: HW-Z1-ZCU208		
020 Zynq Decoupling 2		
Size	Date Modified: B Friday, November 22, 2019	Document Number: 038-05023-01 A01
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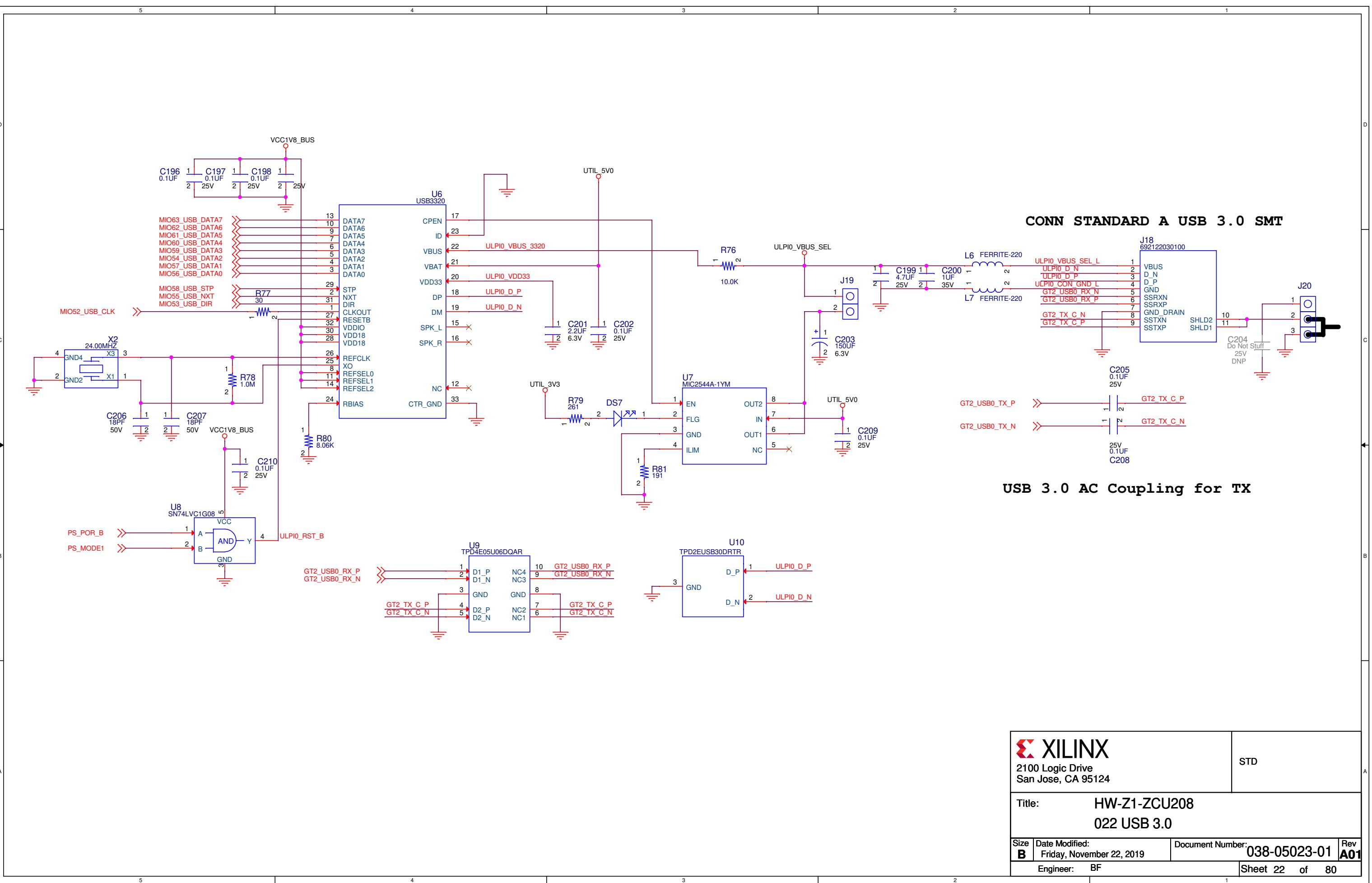


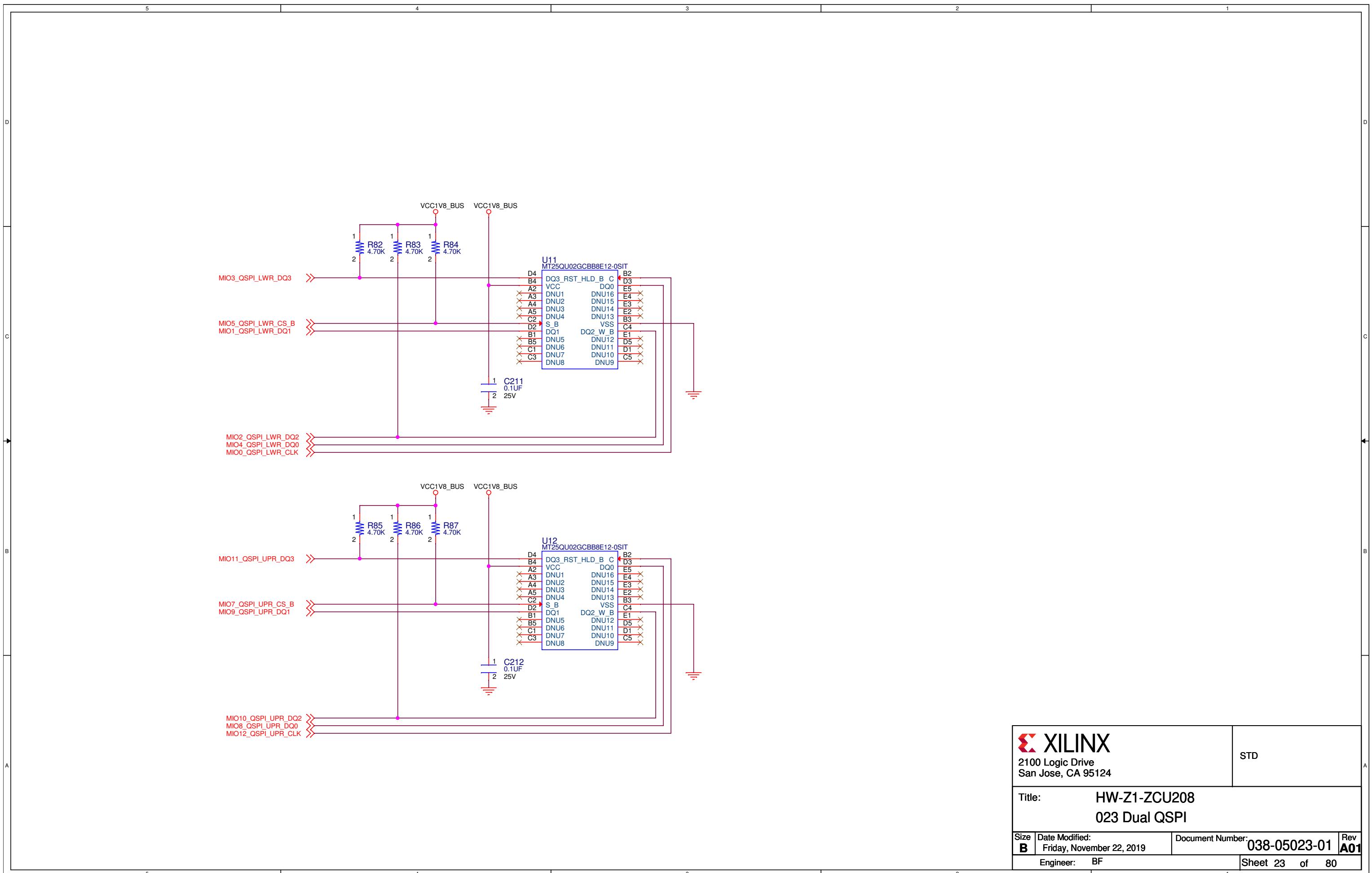
U1-37
XCZU48DR-2FSVG1517EES9830



Title: HW-Z1-ZCU208
021 Zynq GND

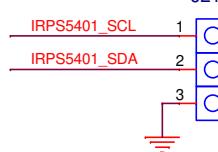
Size	Date Modified: Friday, November 22, 2019	Document Number: 038-05023-01	Rev A01
Engineer: BF		Sheet 21	of 80



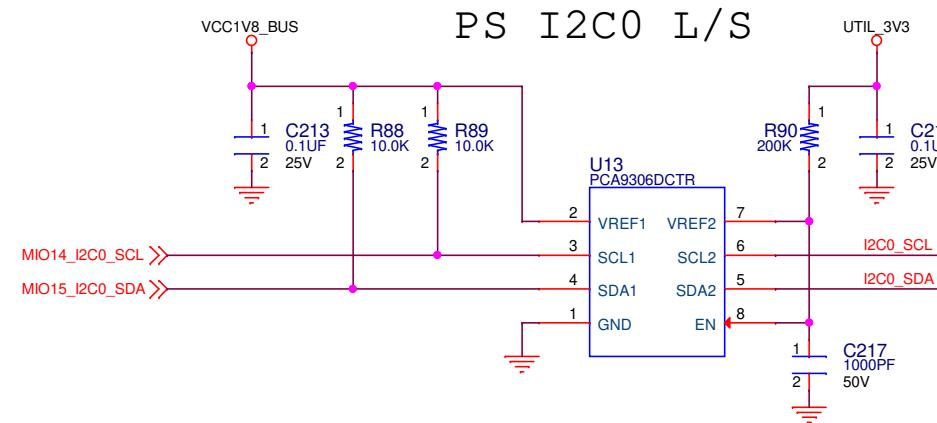


XILINX 2100 Logic Drive San Jose, CA 95124	STD
Title: HW-Z1-ZCU208 023 Dual QSPI	
Size: B	Date Modified: Friday, November 22, 2019
Engineer: BF	Document Number: 038-05023-01 Rev A01

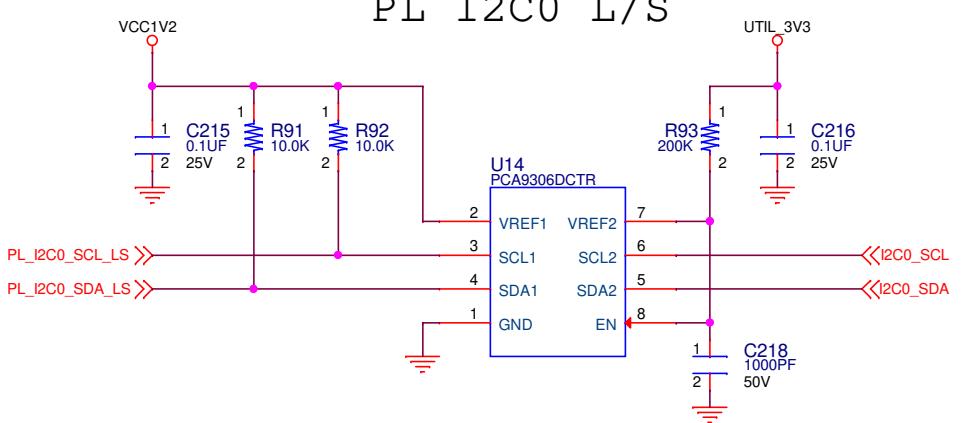
PMBUS Header



PS I₂C0 L/S



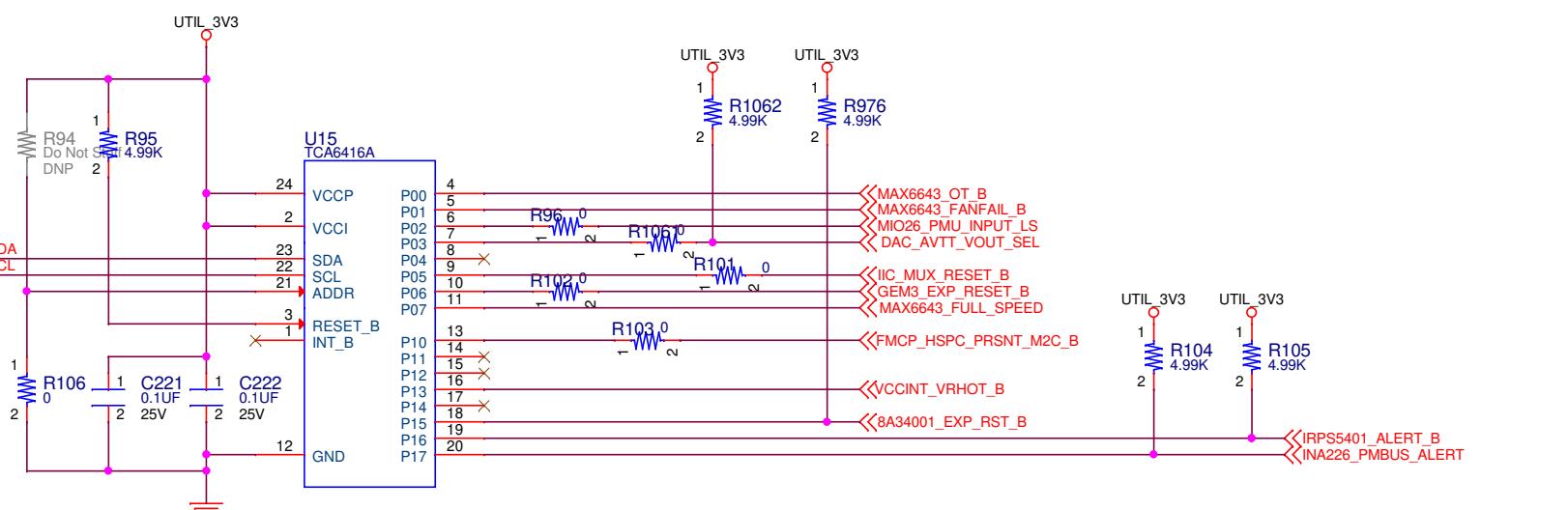
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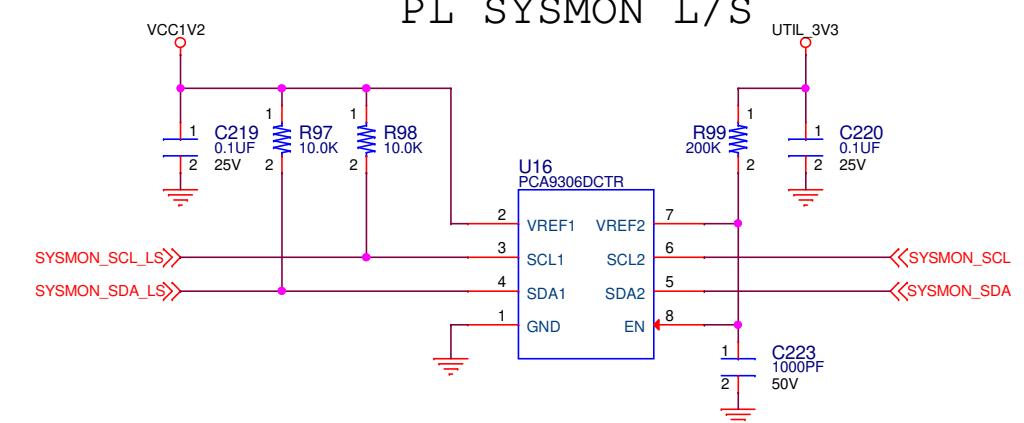
UTIL_3V3

UTIL_3V3

UTIL_3V3



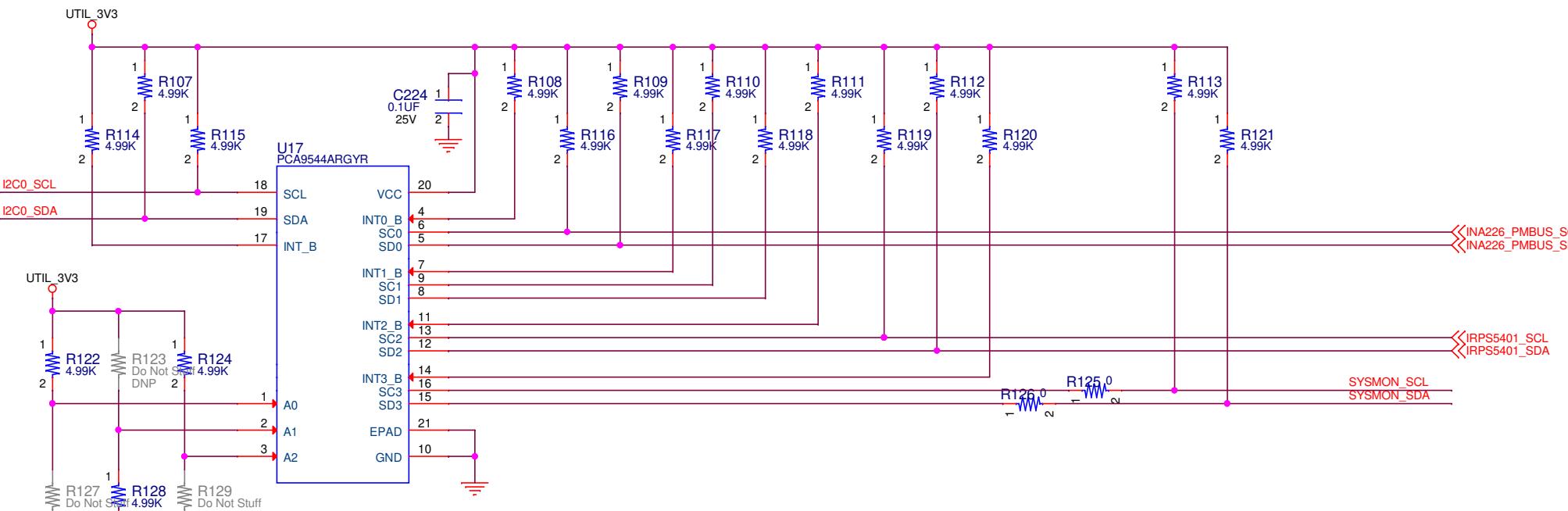
PL SYSMON L/S



UTIL_3V3

UTIL_3V3

UTIL_3V3



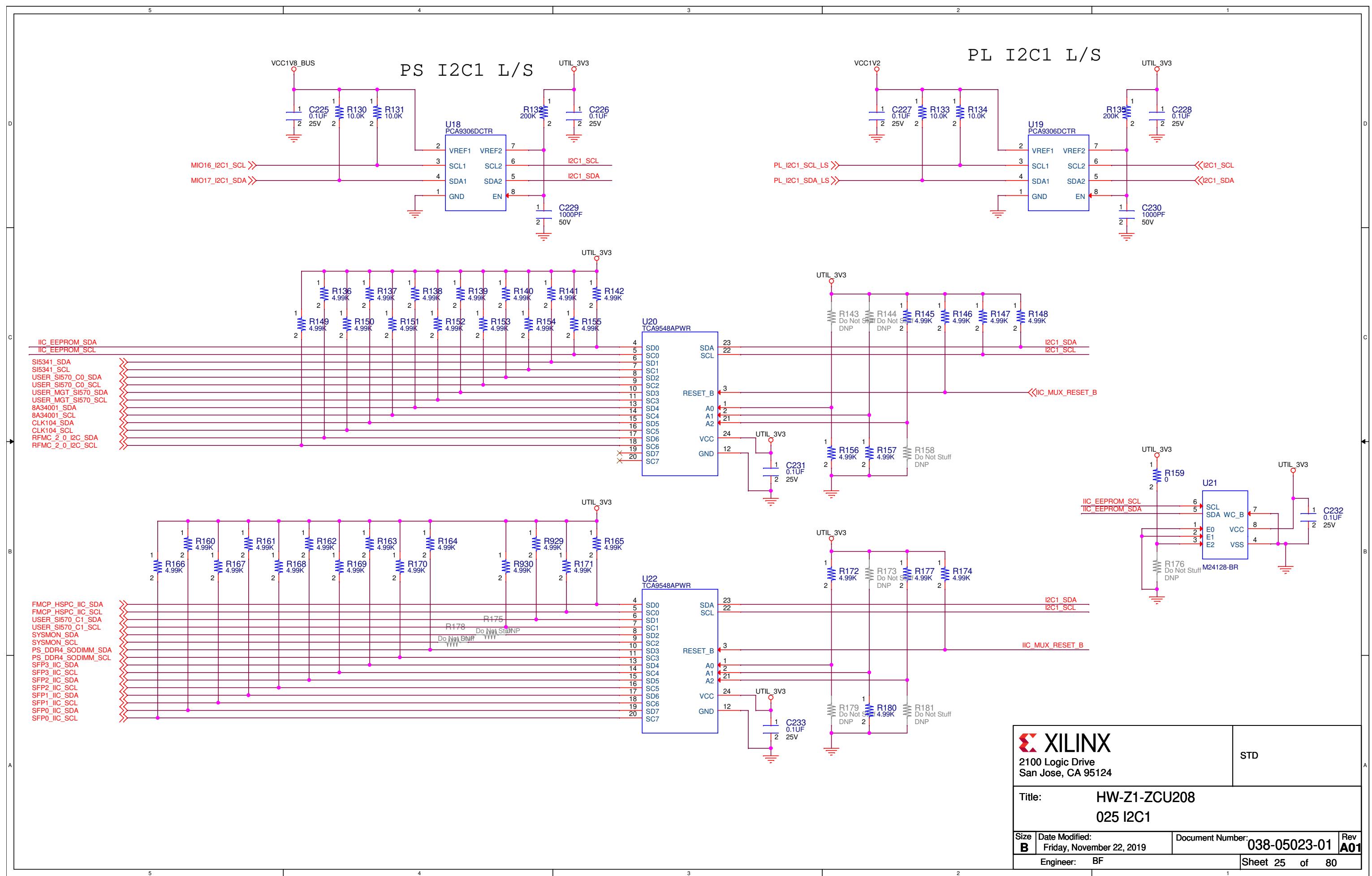
XILINX

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San Jose, CA 95124

STD

Title: HW-Z1-ZCU208
024 I₂C0

Size	Date Modified:	Document Number:
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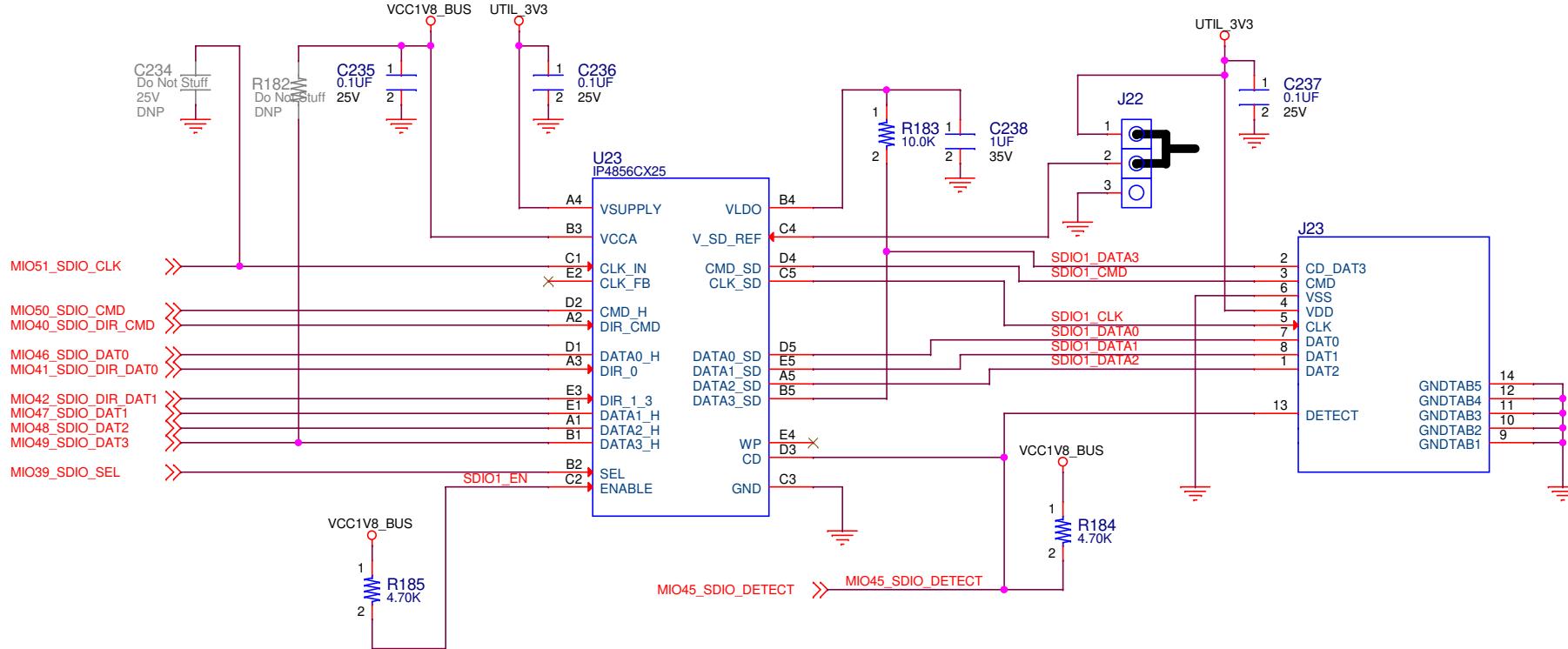
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2100 Logic Drive
San Jose, CA 95124

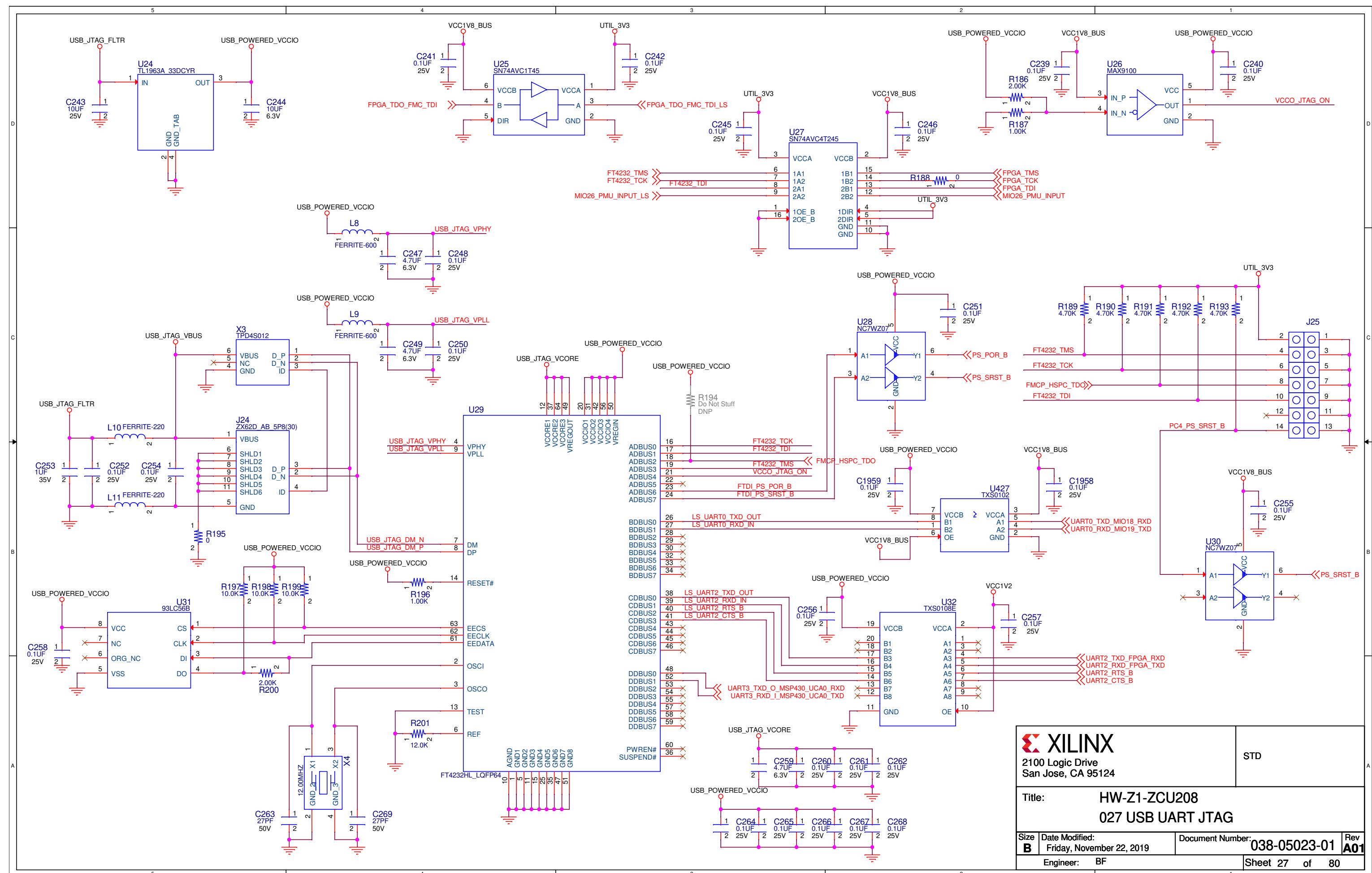
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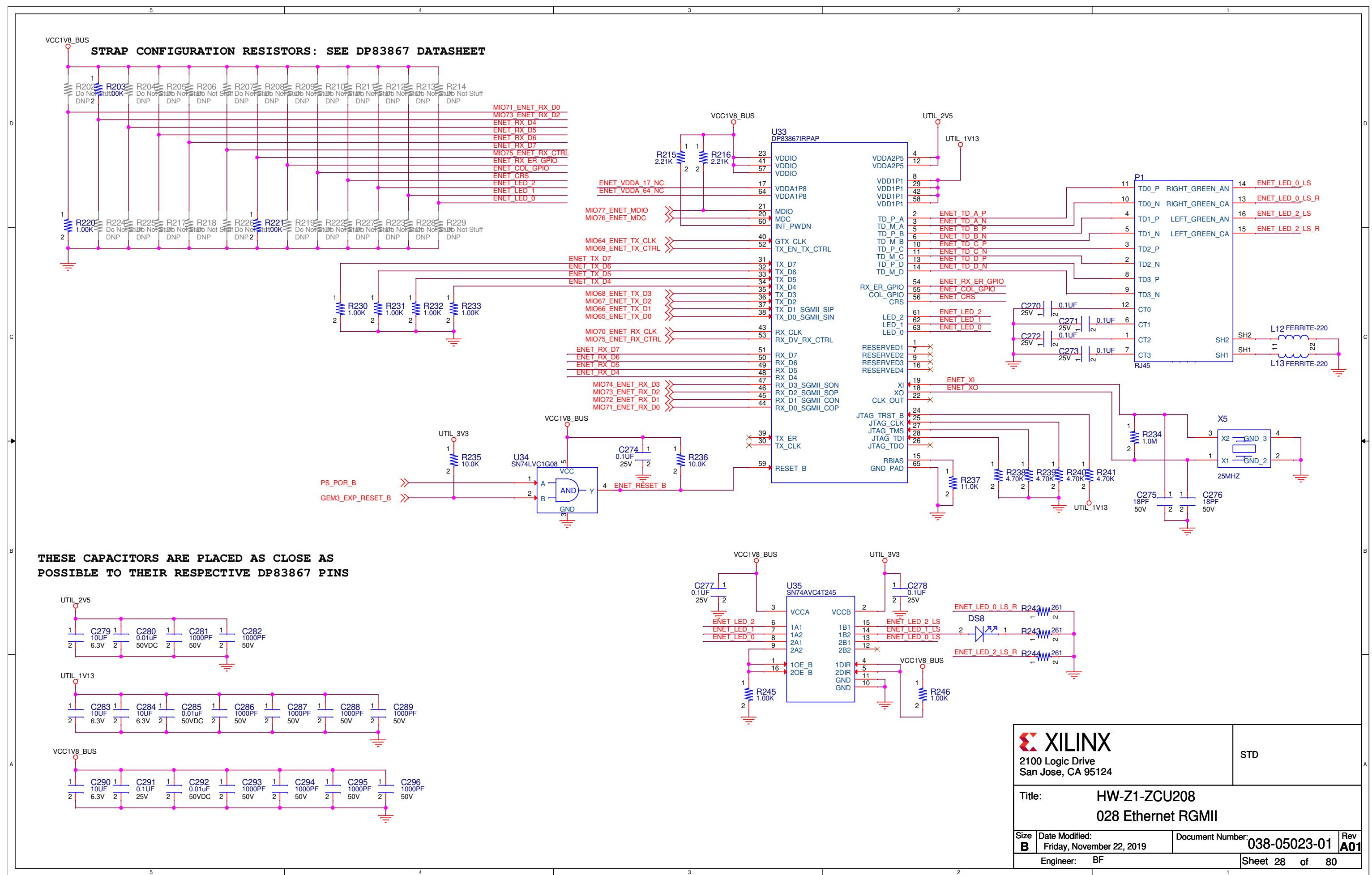
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025 I²C1

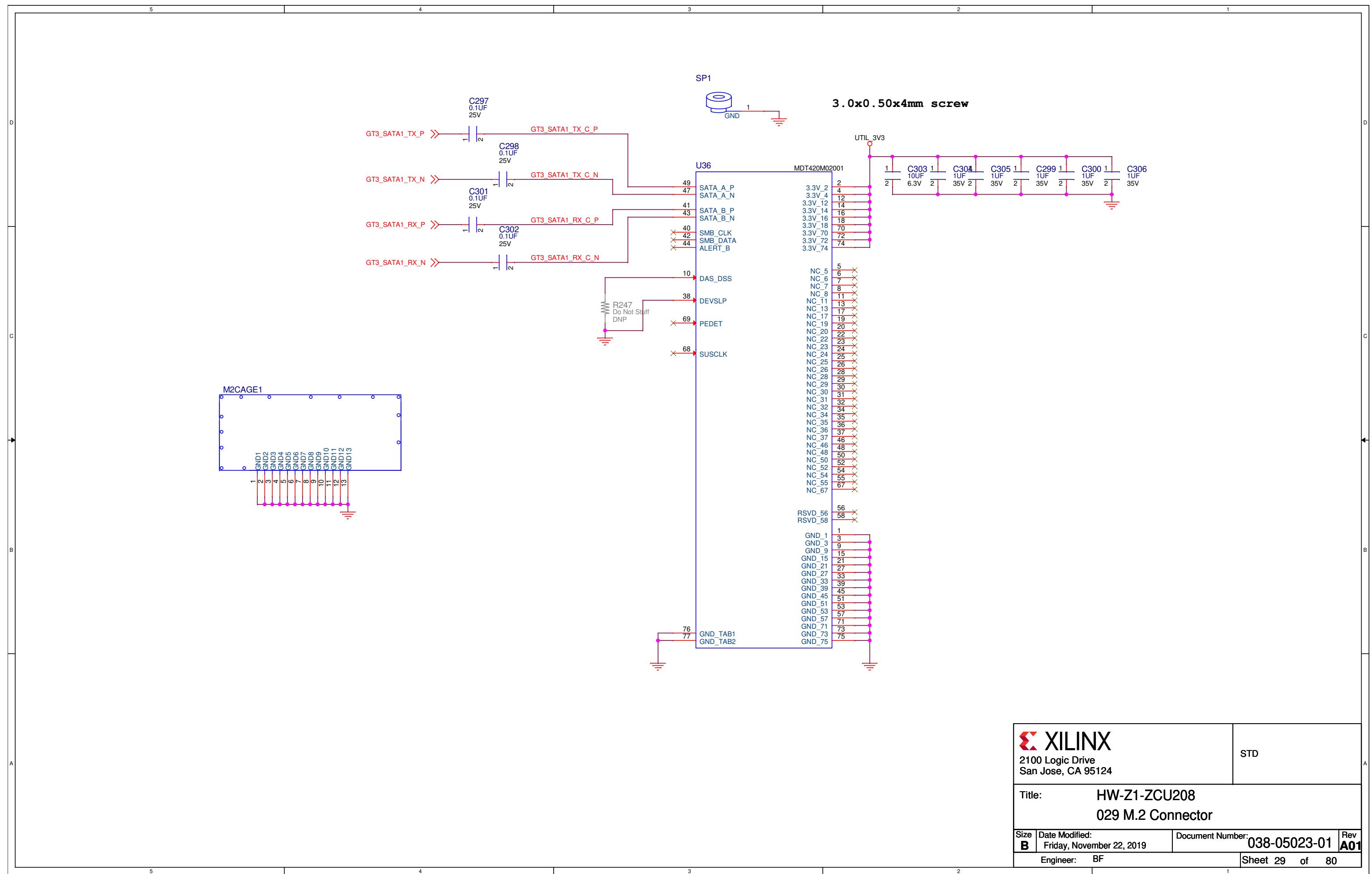
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Engineer: BF	Sheet 25 of 80		

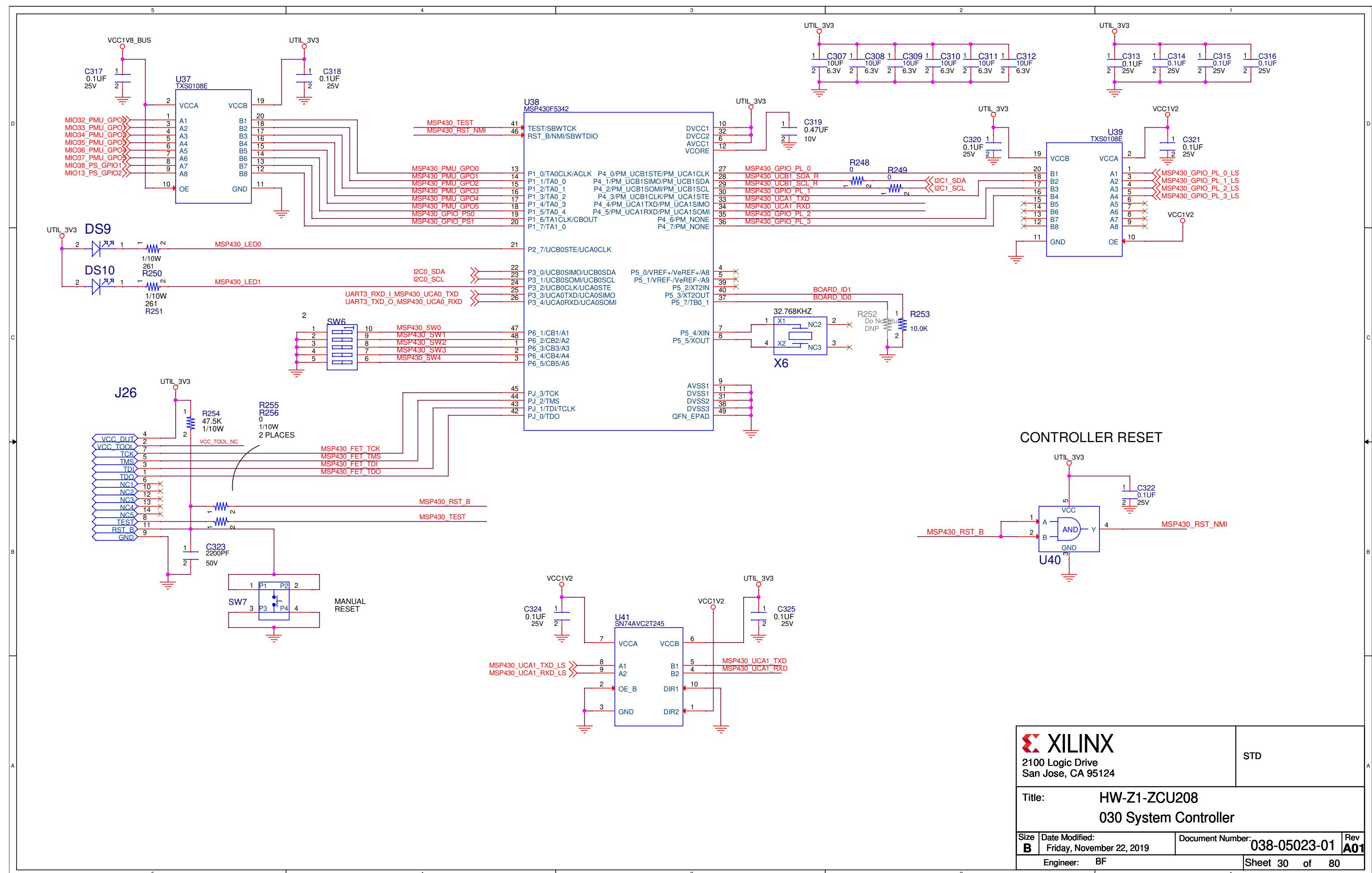


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2100 Logic Drive San Jose, CA 95124		
Title: HW-Z1-ZCU208		
026 SD 3.0		
Size: B	Date Modified: Friday, November 22, 2019	Document Number: 038-05023-01 Rev A01
Engineer: BF	Sheet 26 of 80	









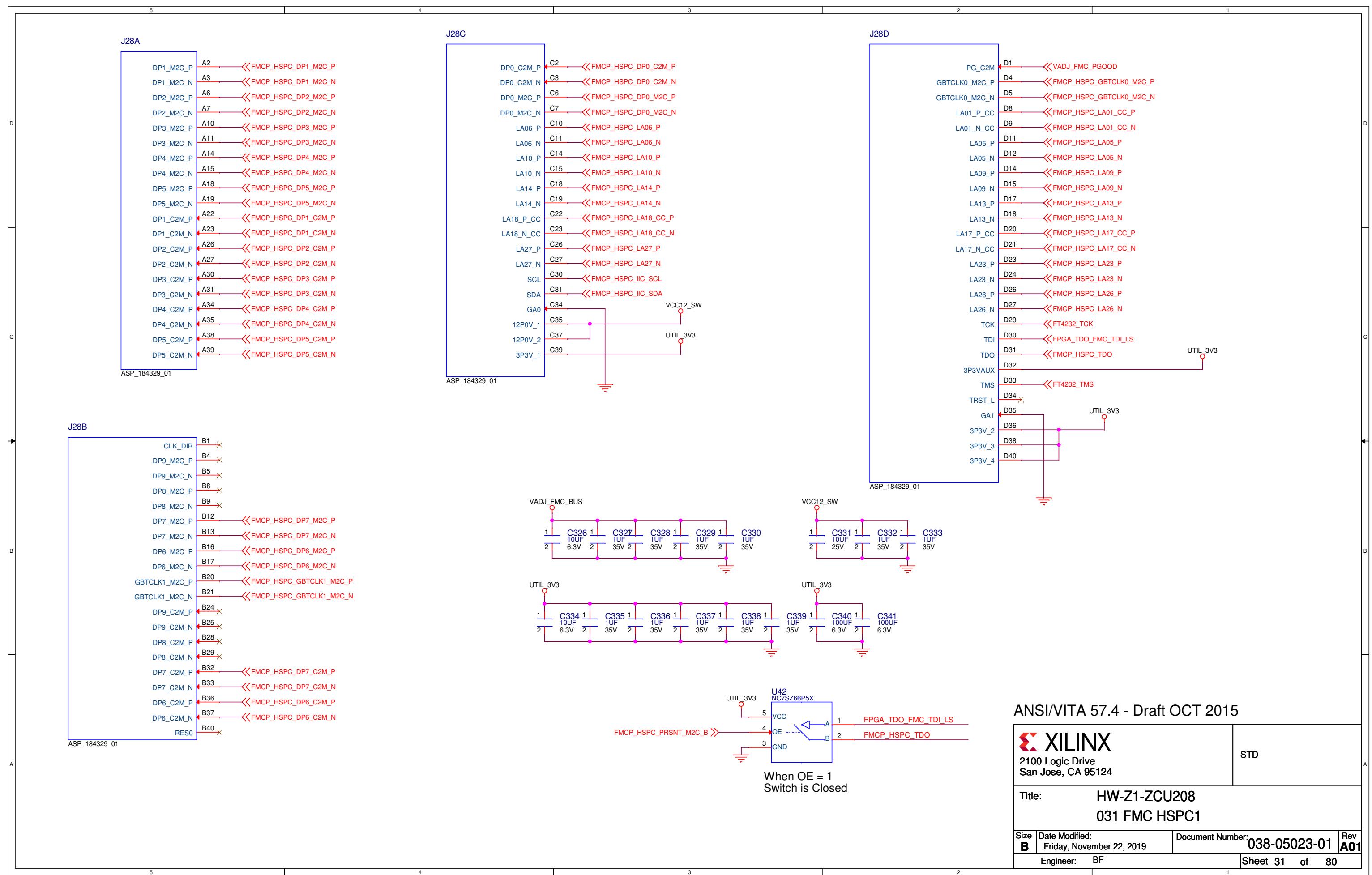
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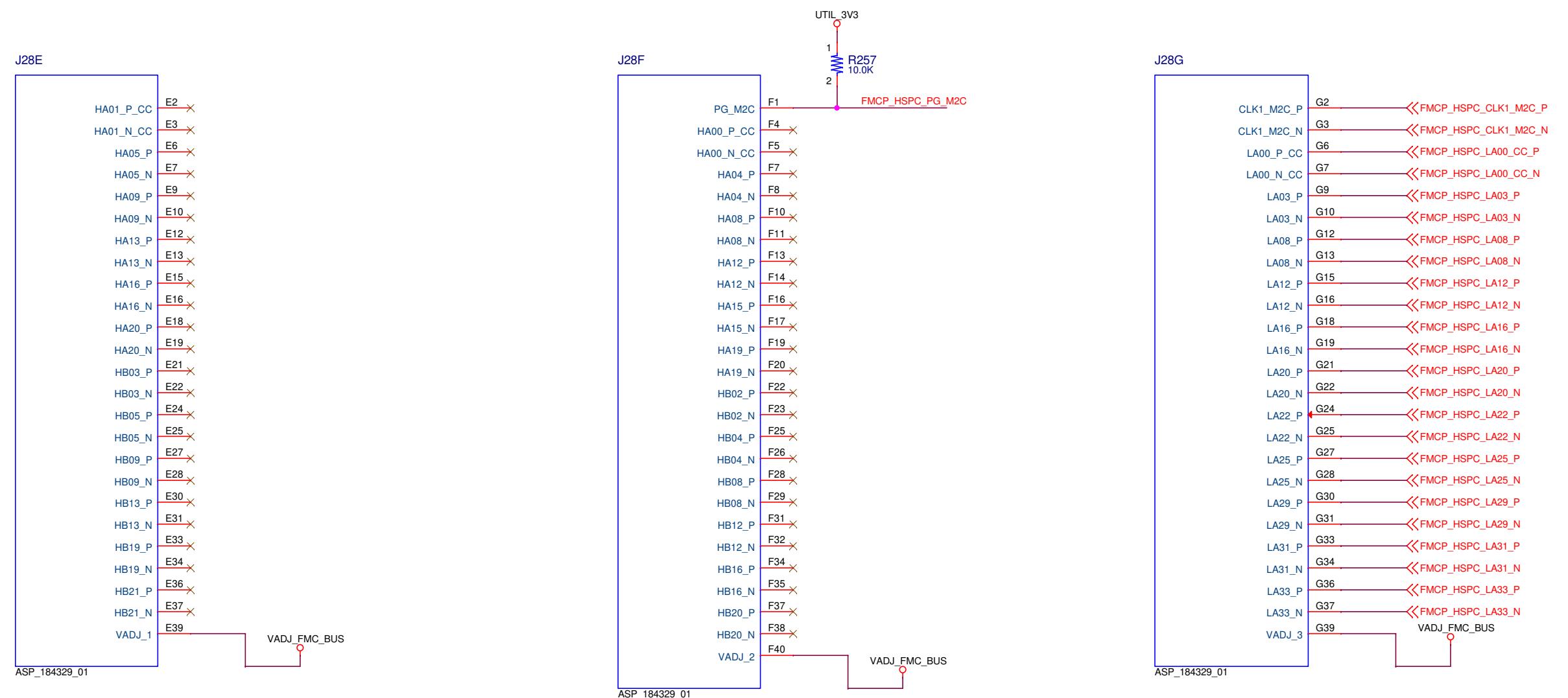
2100 Logic Drive
San Jose, CA 95124

STD

Title: **HW-Z1-ZCU208**
030 System Controller

Size	Date Modified:	Document Number:	Rev
B	Friday, November 22, 2019	038-05023-01	A01
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ANSI/VITA 57.4 - Draft OCT 2015

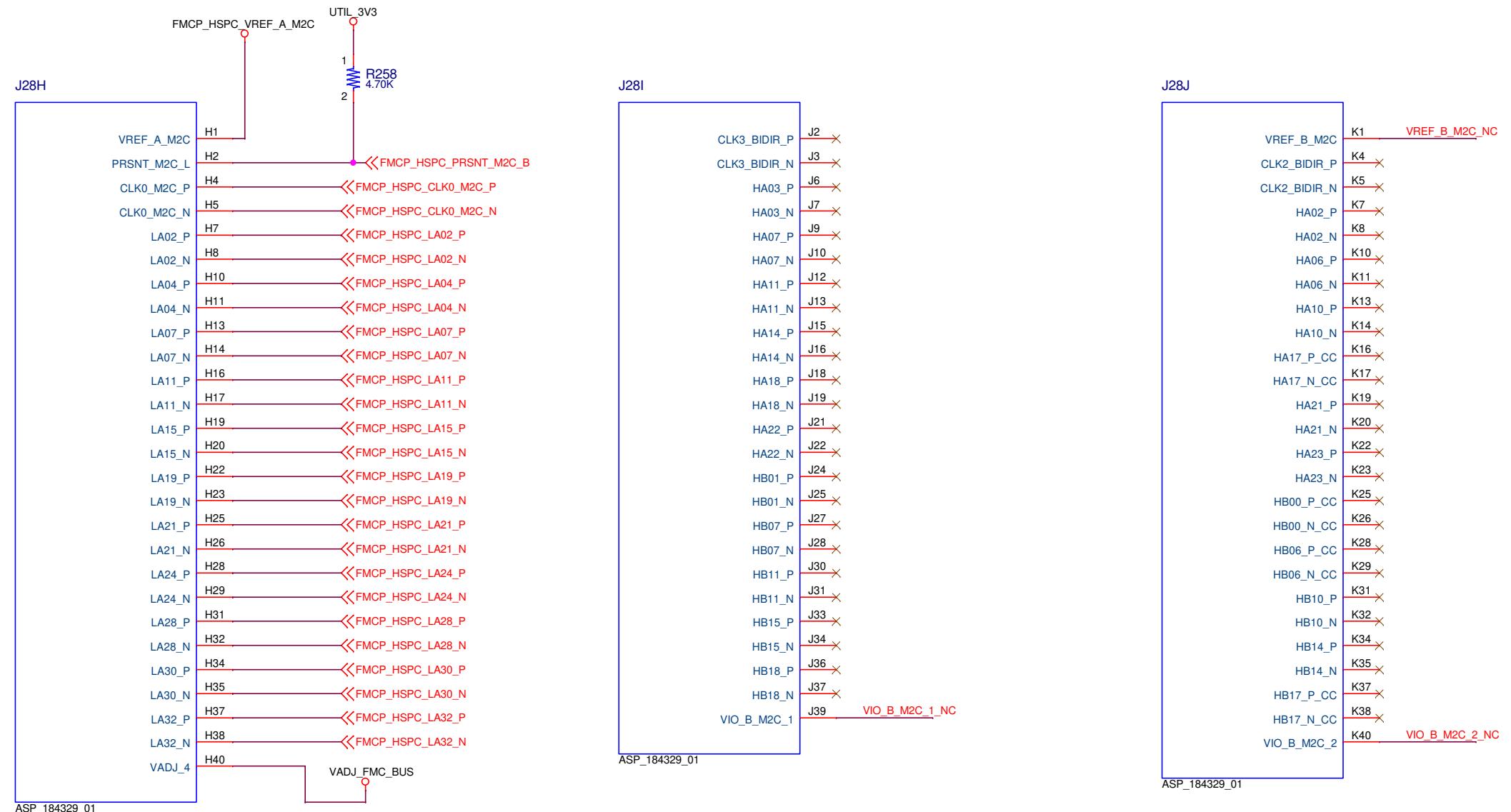


2100 Logic Drive
San Jose, CA 95124

STD

Title: HW-Z1-ZCU208
032 FMC HSPC2

Size	Date Modified:	Document Number:
B	Friday, November 22, 2019	038-05023-01 Rev A01
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ANSI/VITA 57.4 - Draft OCT 2015

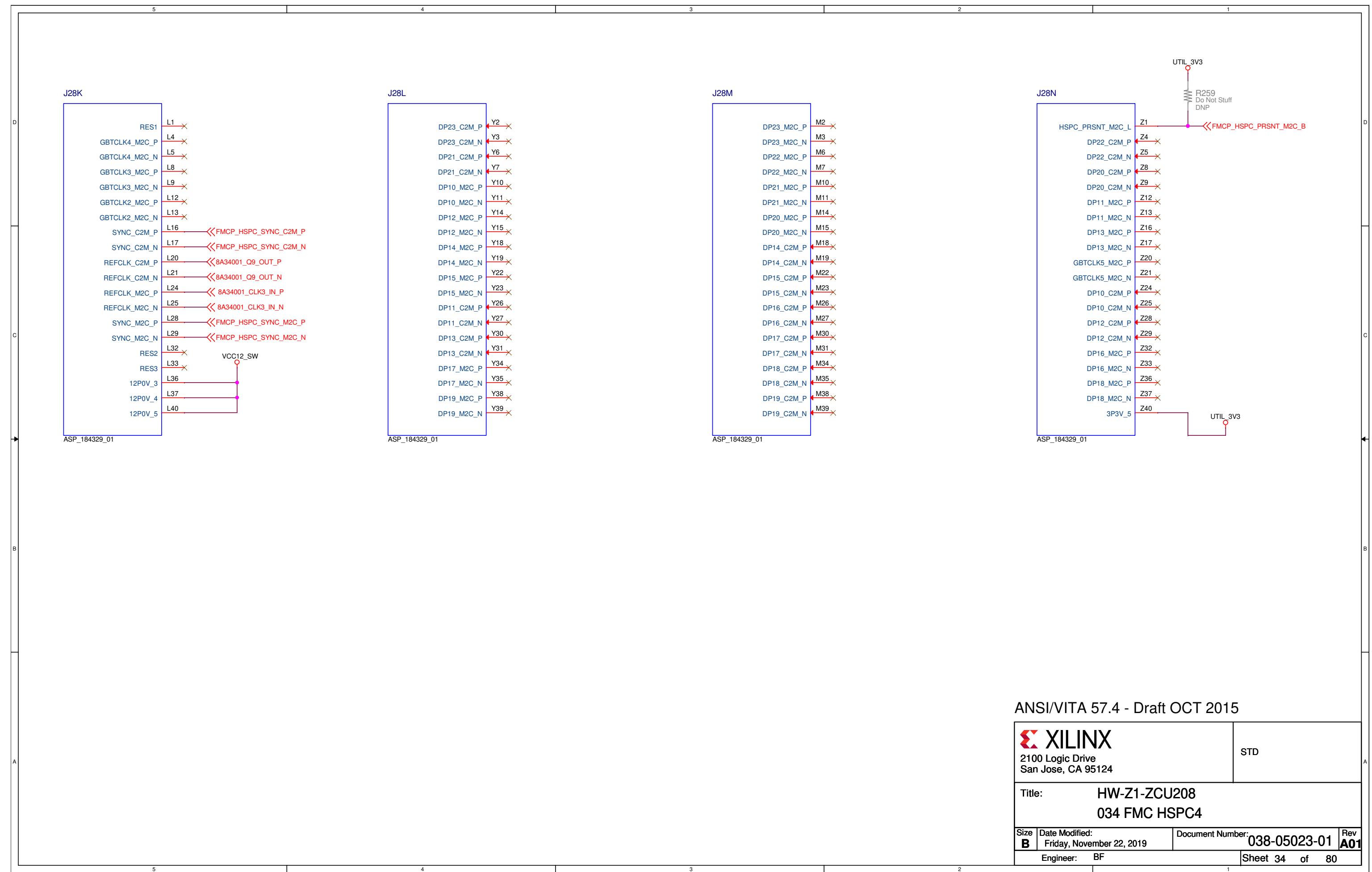


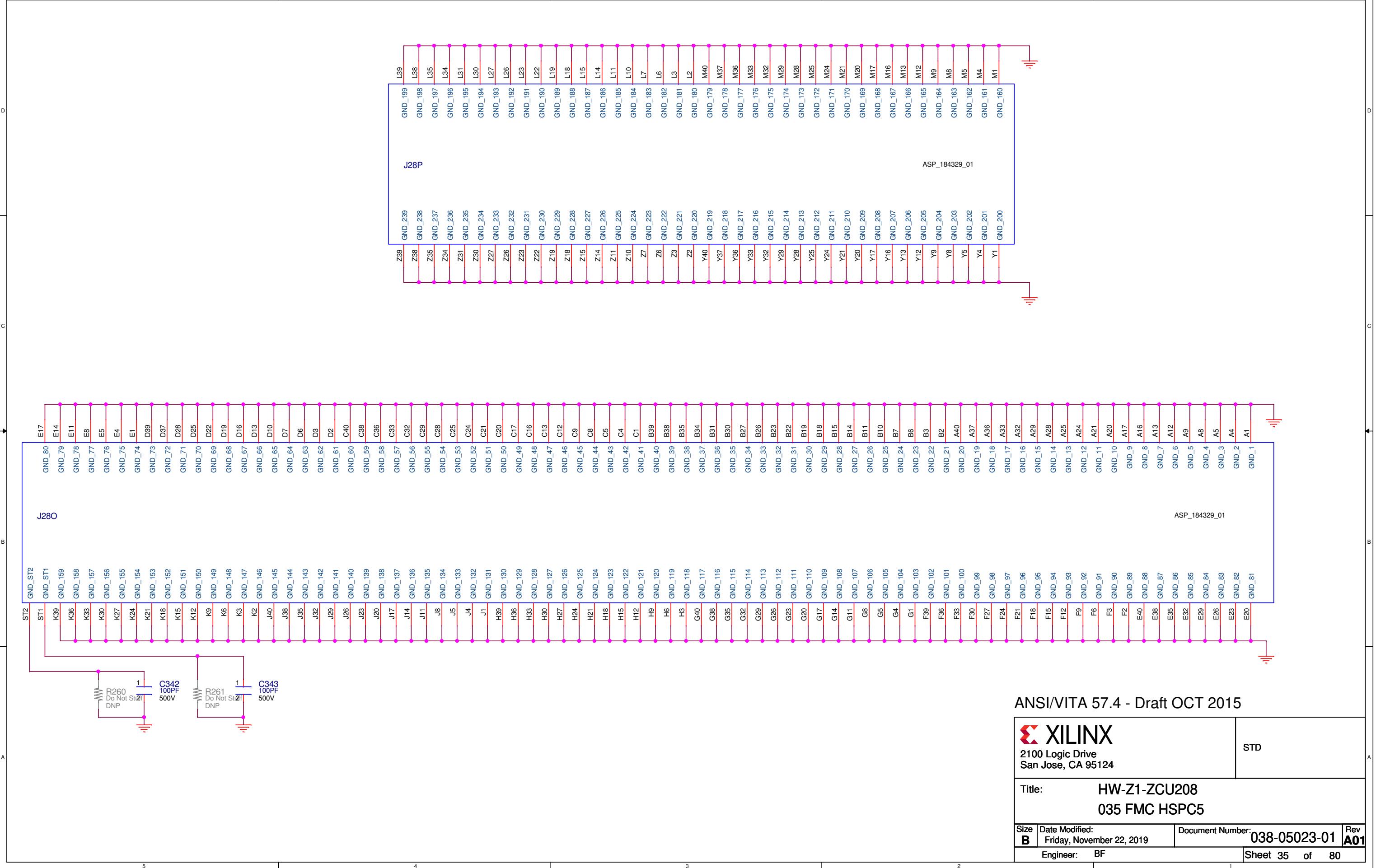
2100 Logic Drive
San Jose, CA 95124

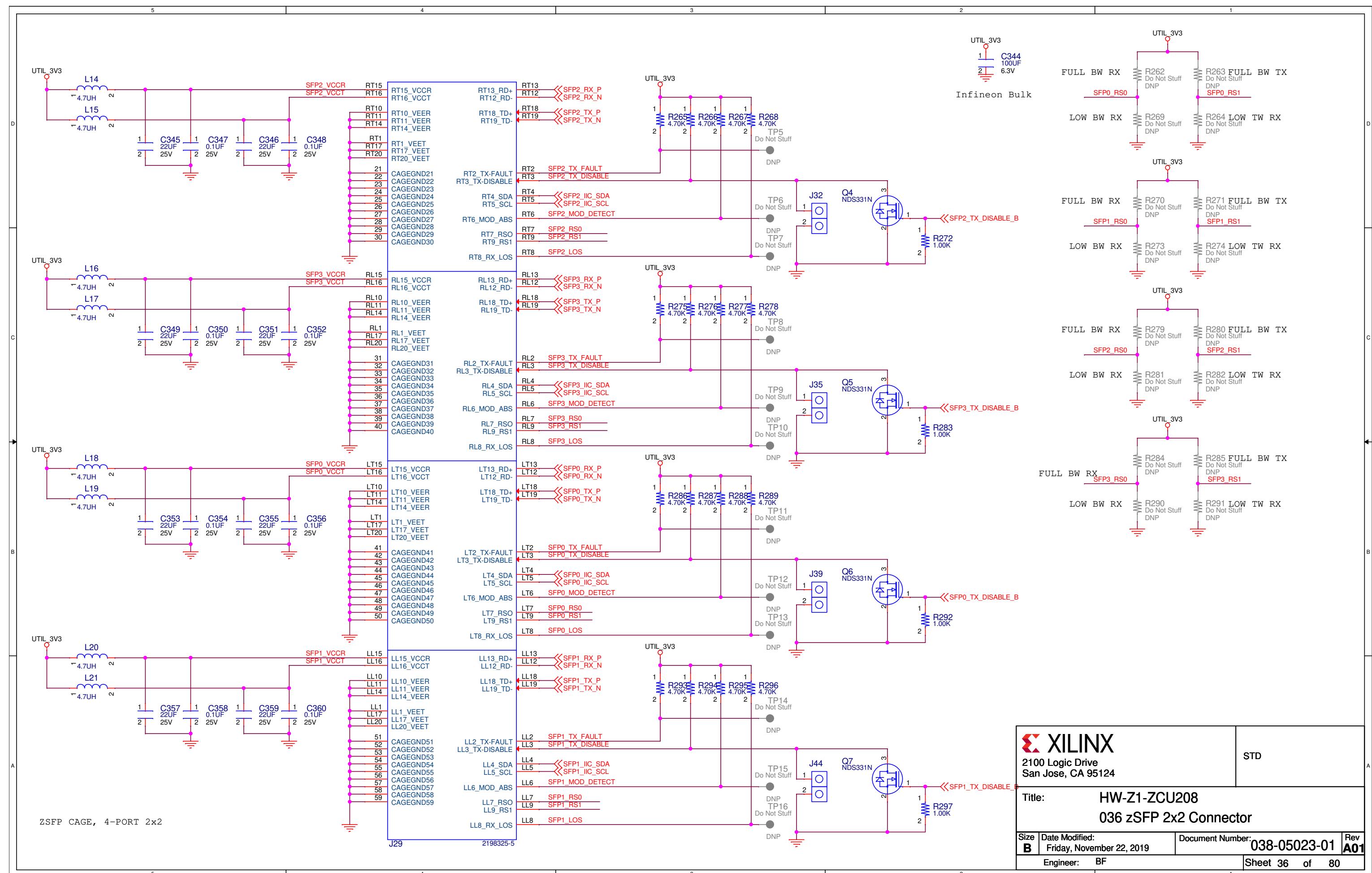
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Title: HW-Z1-ZCU208
033 FMC HSPC3

Size	Date Modified:	Document Number:	Rev
B	Friday, November 22, 2019	038-05023-01	A01
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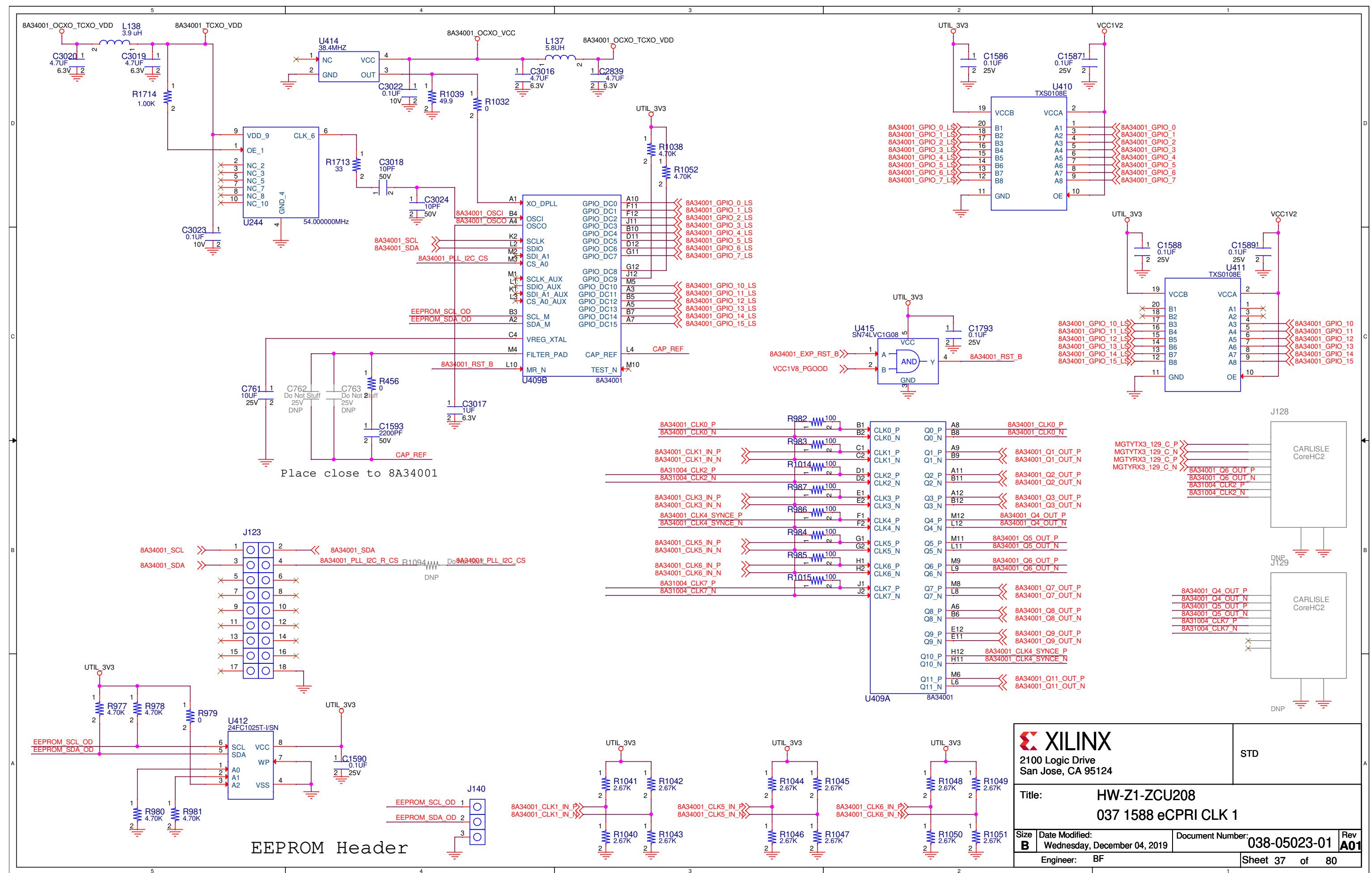
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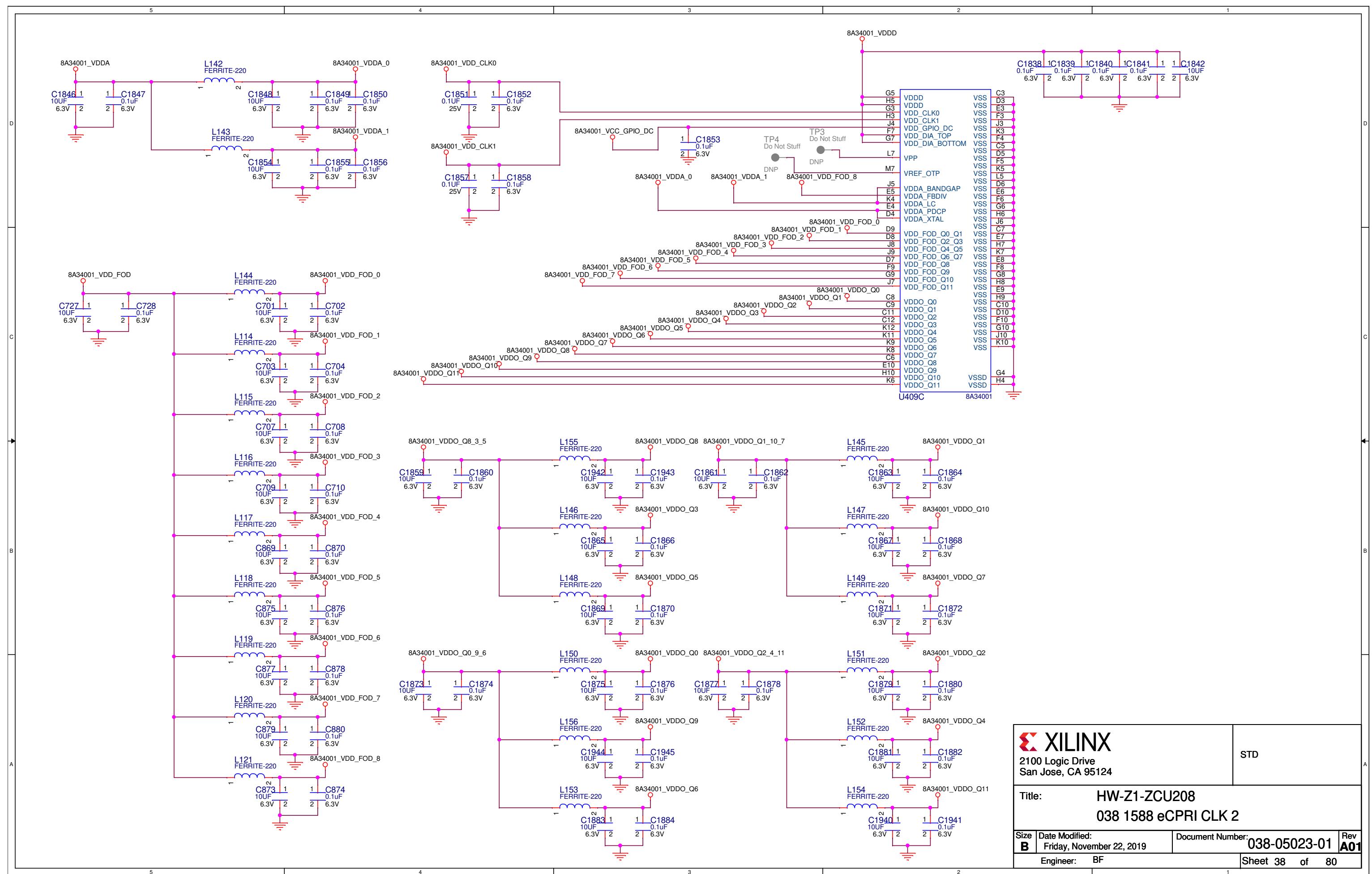
2100 Logic Drive
San Jose, CA 95124

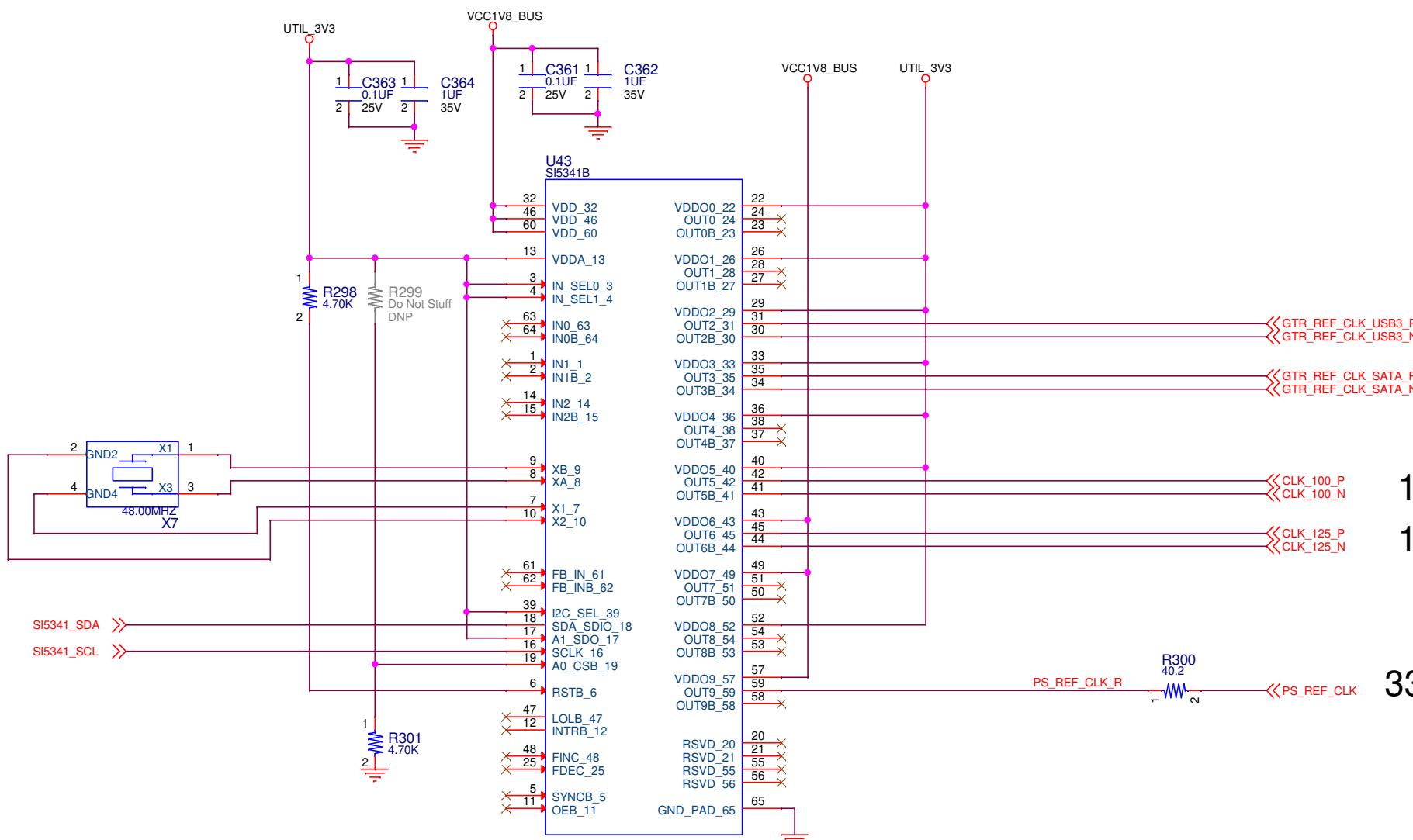
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Title: HW-Z1-ZCU208
036 zSFP 2x2 Connector

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		Engineer: BF Sheet 36 of 80







26 MHz LVDS
125 MHz LVDS

100 MHz LVDS
125 MHz LVDS

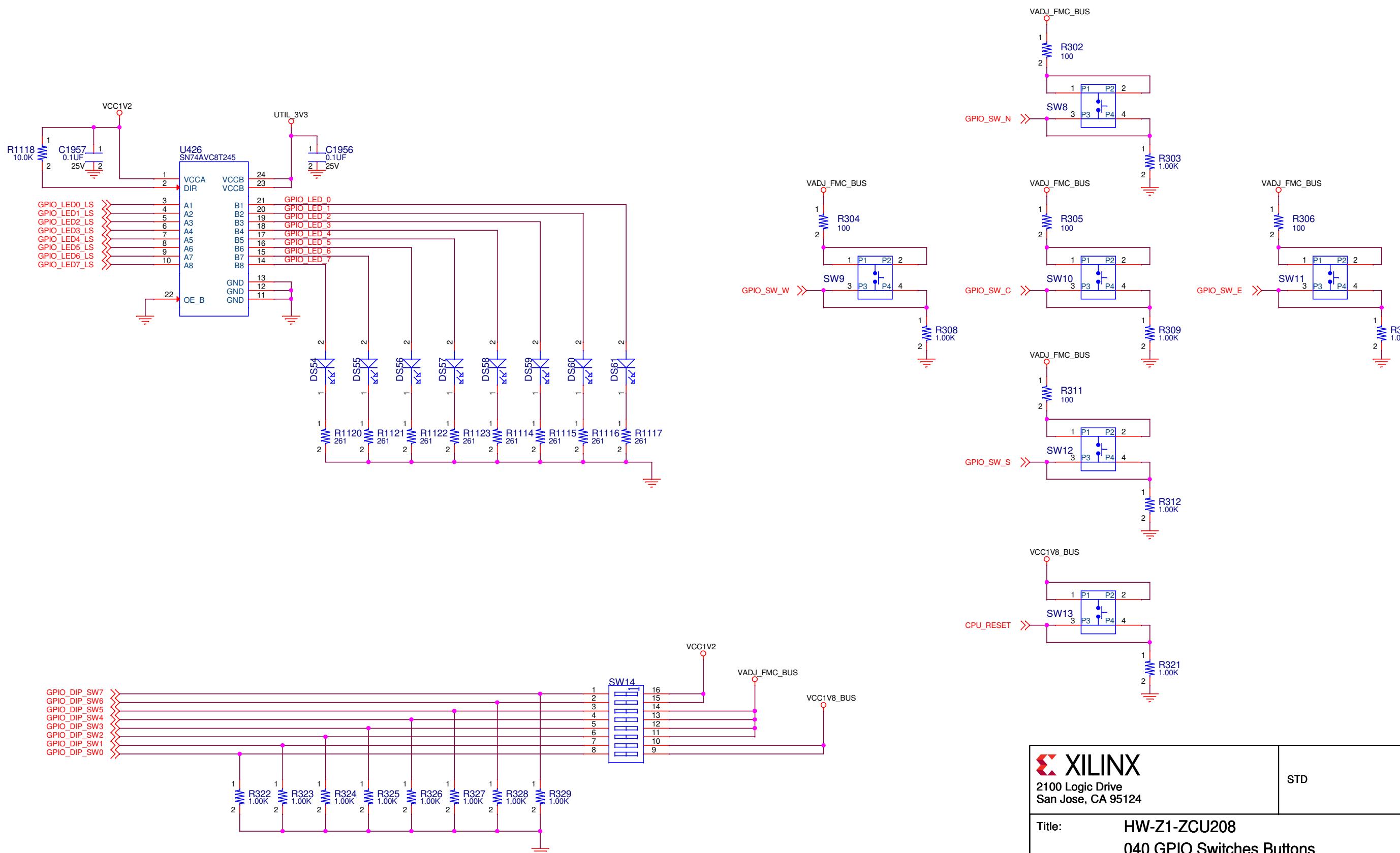
33.333333... (33 + 1/3 MHz)



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Title: HW-Z1-ZCU208
039 Fixed Clocks

Size	Date Modified: Friday, November 22, 2019	Document Number: 038-05023-01	Rev
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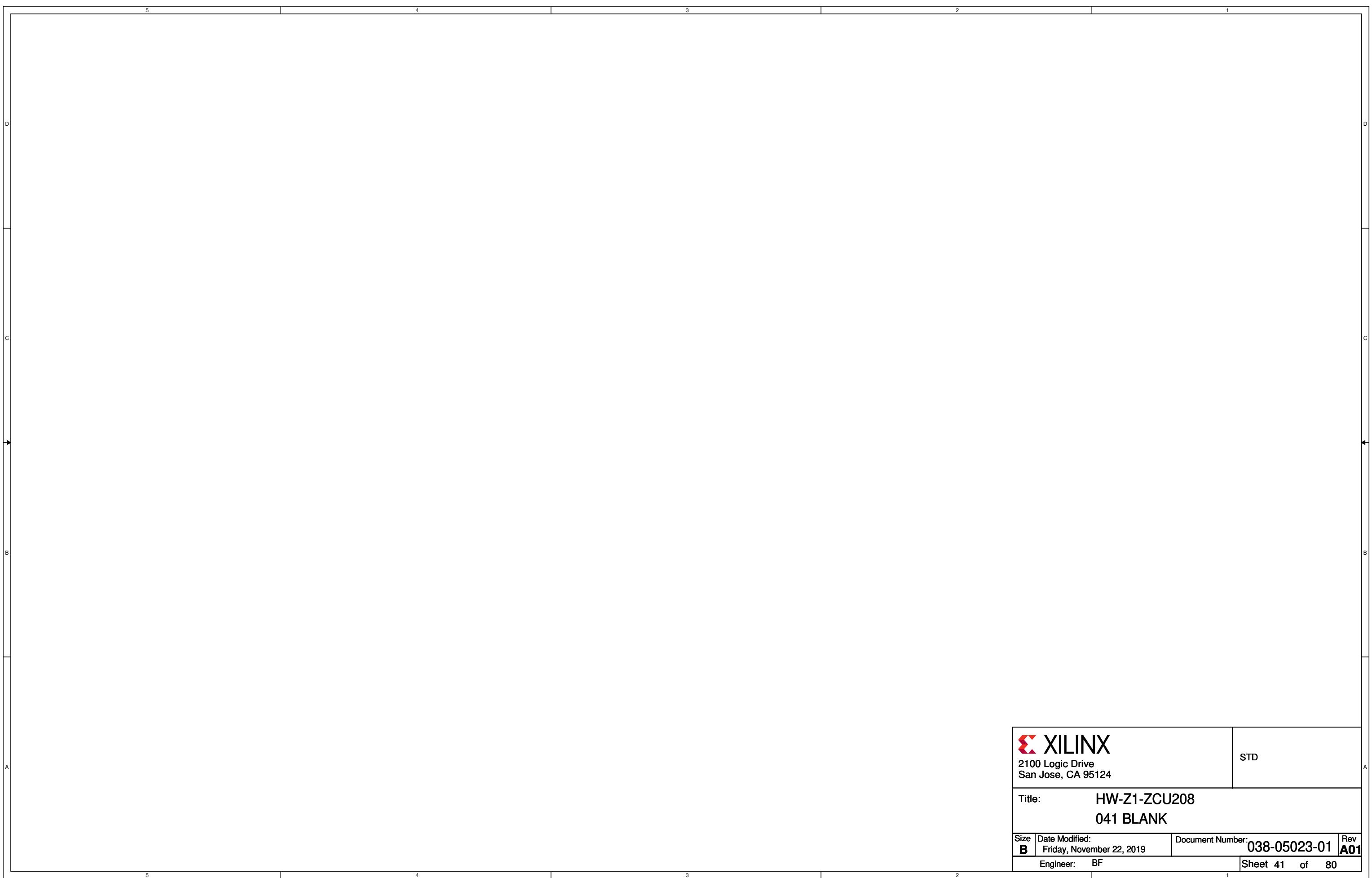
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San Jose, CA 95124

STD

Title: **HW-Z1-ZCU208**
040 GPIO Switches Buttons

Size	Date Modified:	Document Number:	Rev
B	Friday, November 22, 2019	038-05023-01	A01
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D				D			
C				C			
B				B			
A				A			
							
 XILINX 2100 Logic Drive San Jose, CA 95124 STD							
Title: HW-Z1-ZCU208 041 BLANK							
Size	Date Modified:	Document Number:	Rev				
B	Friday, November 22, 2019	038-05023-01	A01				
Engineer: BF		Sheet 41 of 80					

D

D

C

C

B

B

A

A

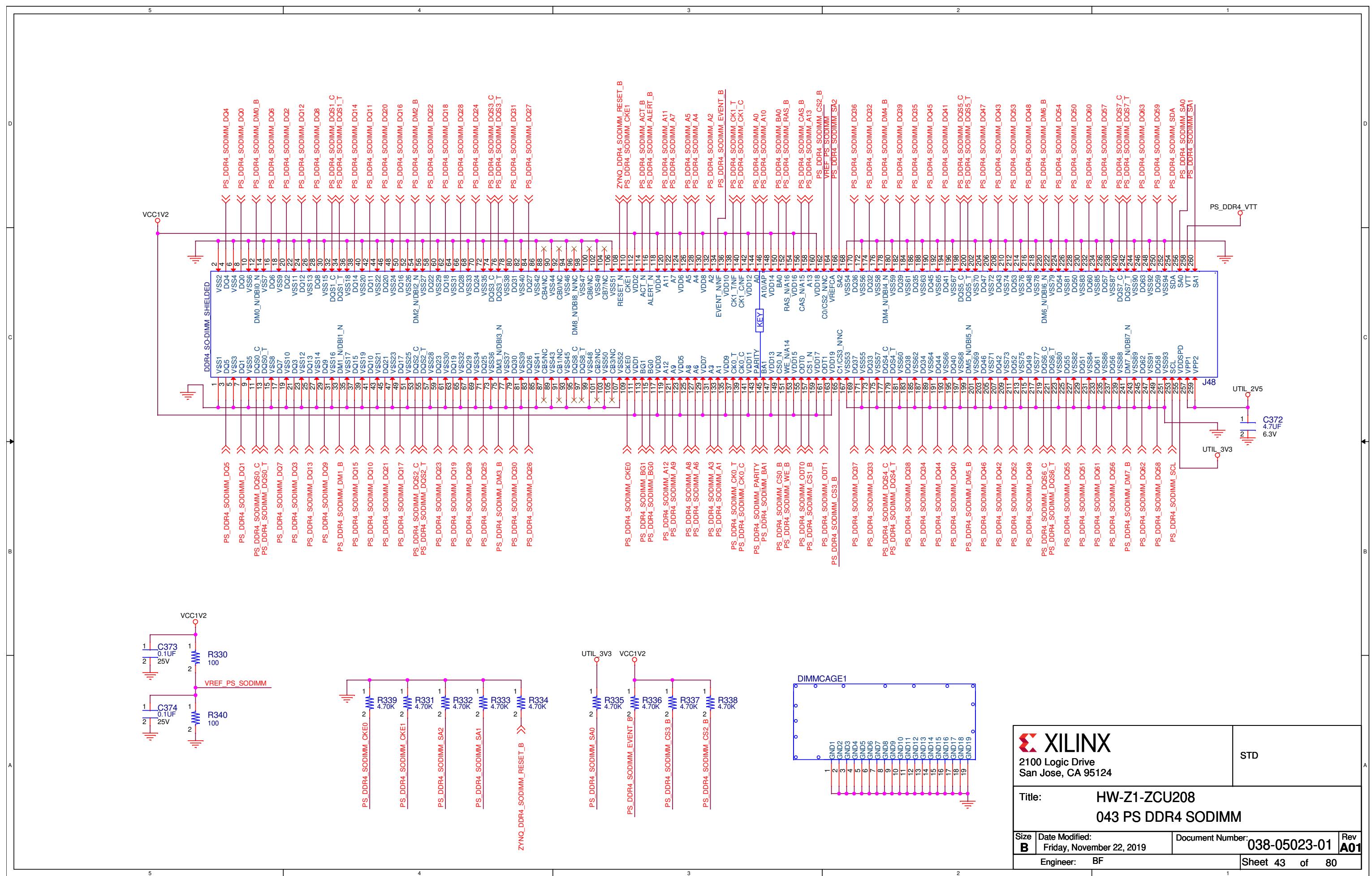


2100 Logic Drive
San Jose, CA 95124

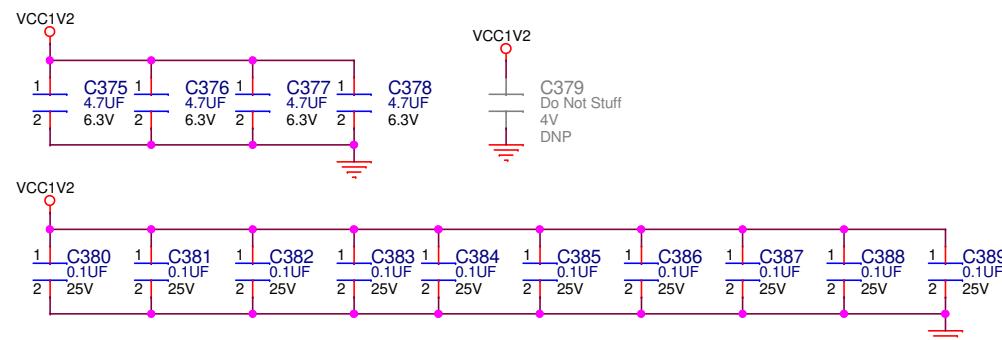
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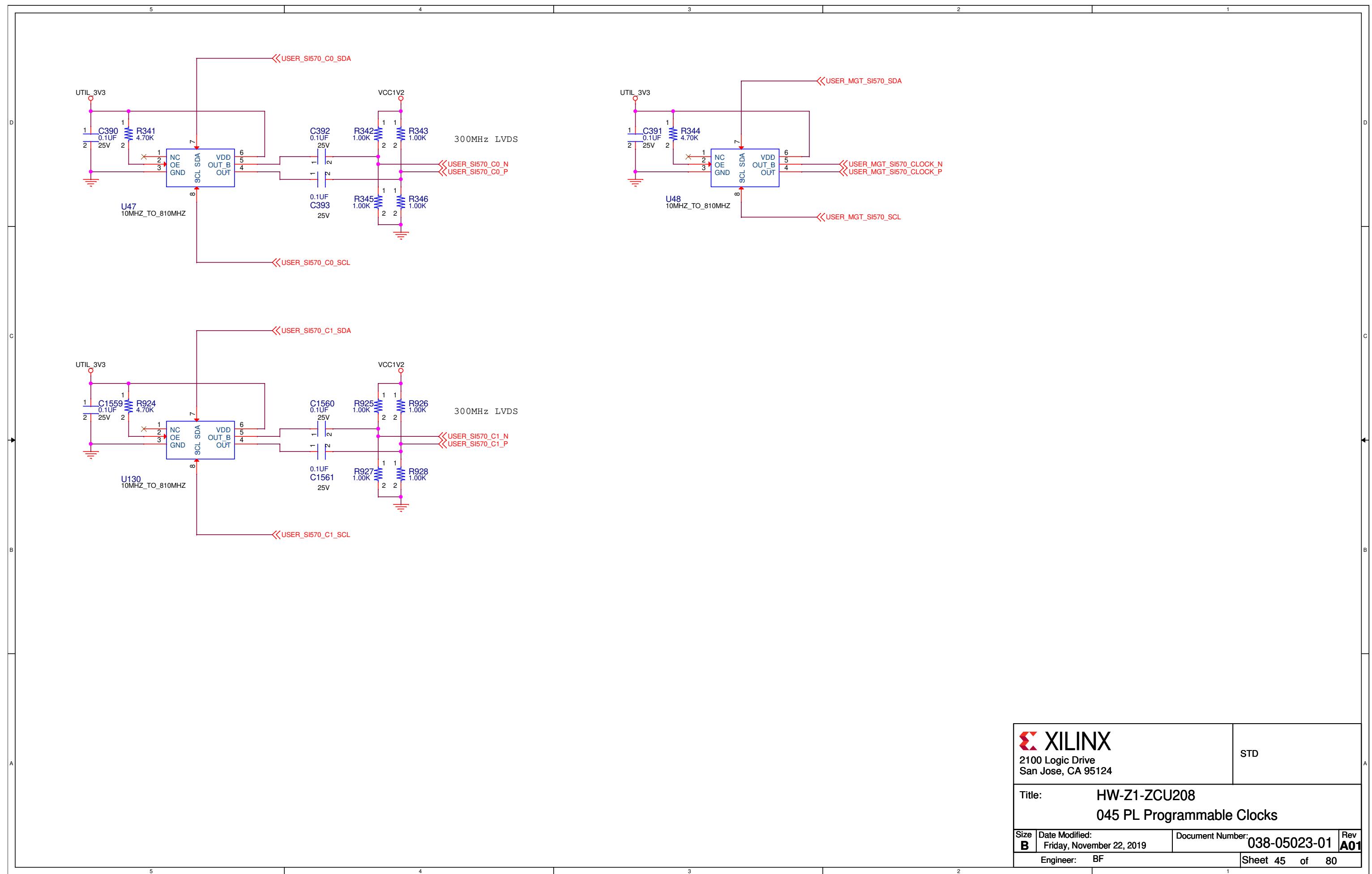
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B	Friday, November 22, 2019	038-05023-01	A01
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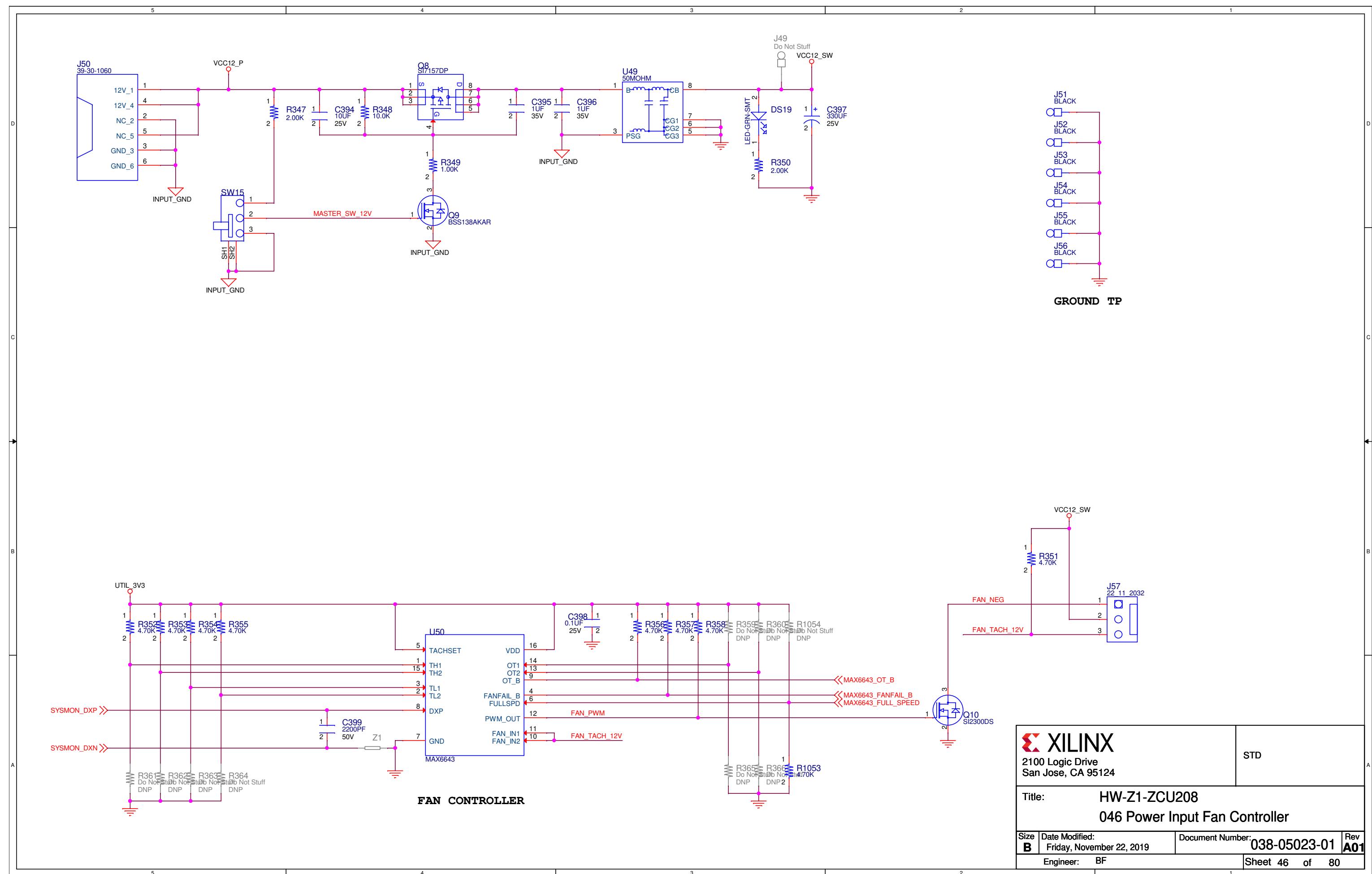
PS SODIMM DECOUPLING



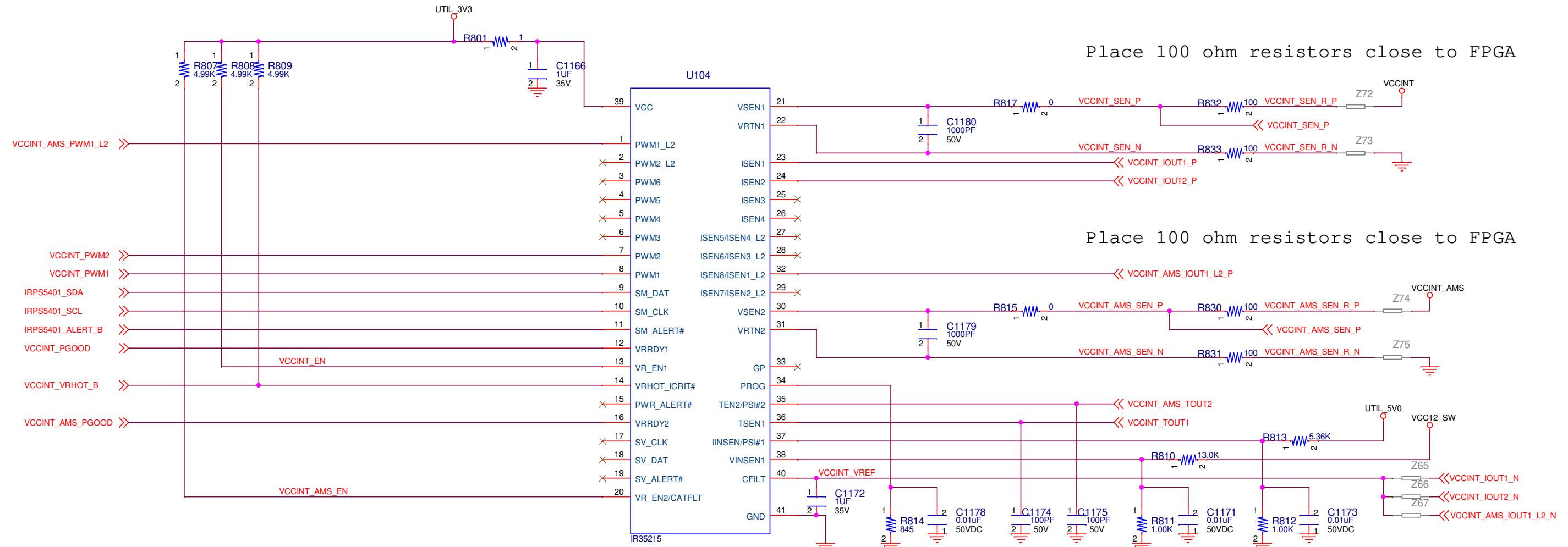
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	2100 Logic Drive San Jose, CA 95124	
Title: HW-Z1-ZCU208		
044 SODIMM Decoupling		
Size	Date Modified: B Friday, November 22, 2019	Document Number: 038-05023-01 Rev A01
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	XILINX	STD
2100 Logic Drive San Jose, CA 95124		
Title: HW-Z1-ZCU208		
045 PL Programmable Clocks		
Size: B	Date Modified: Friday, November 22, 2019	Document Number: 038-05023-01 Rev A01
Engineer: BF	Sheet 45 of 80	



REPLACE IC WITH CORRECT FIRMWARE P/N



ADDR: 0

7-BIT I2C ADDR: 0x10

7-BIT PMBUS ADDR: 0x40

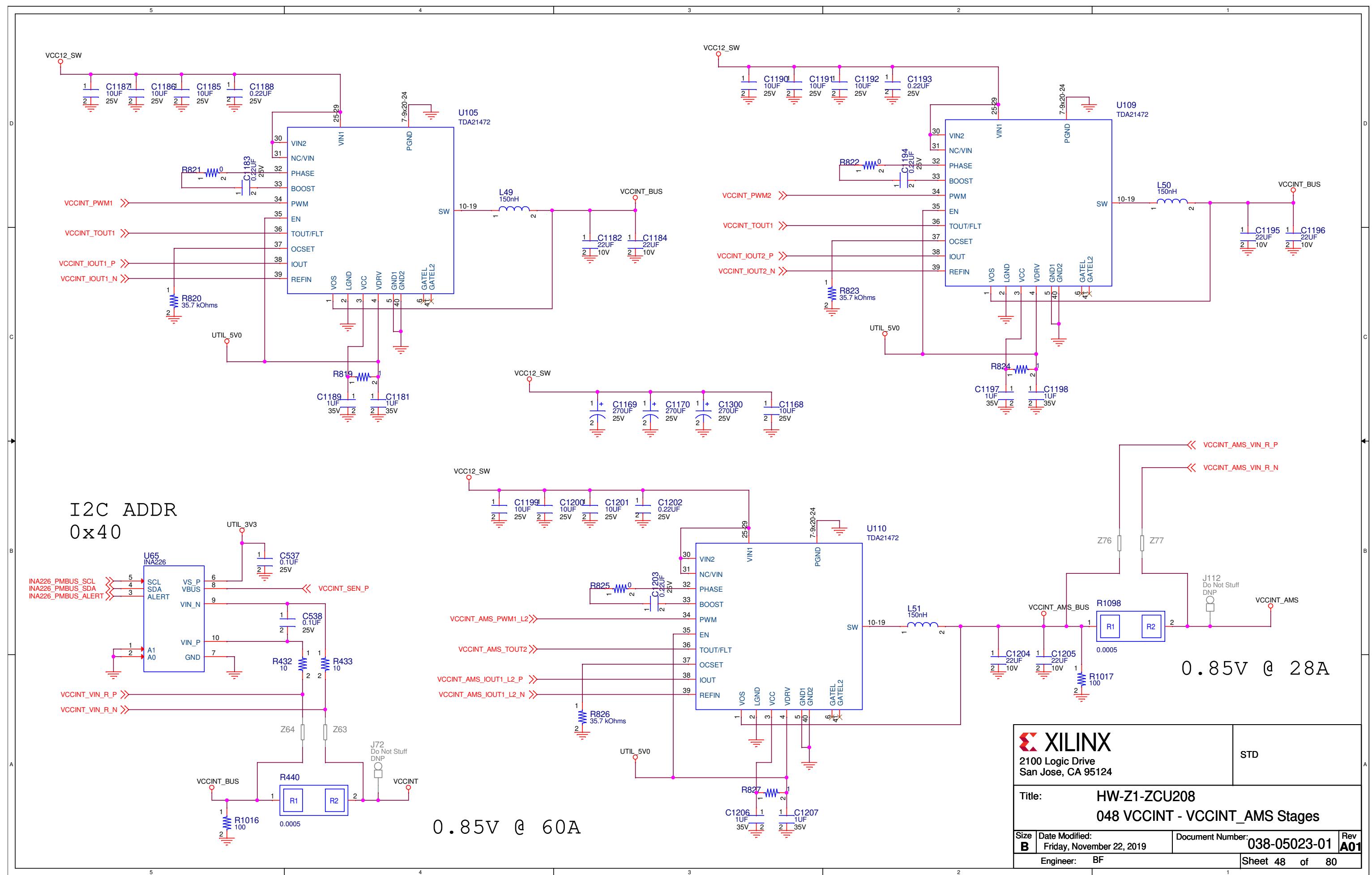
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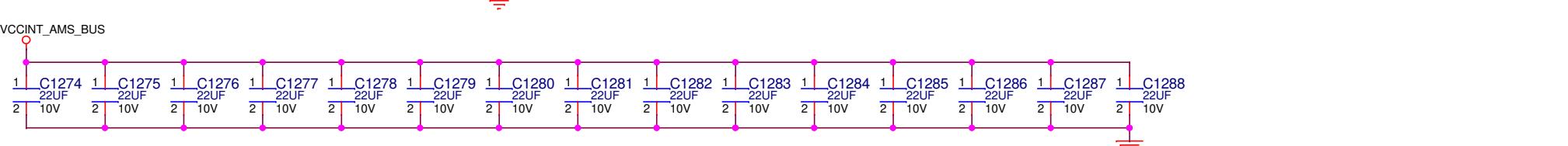
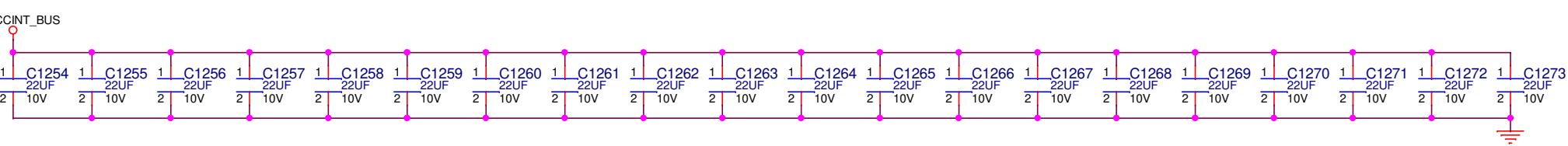
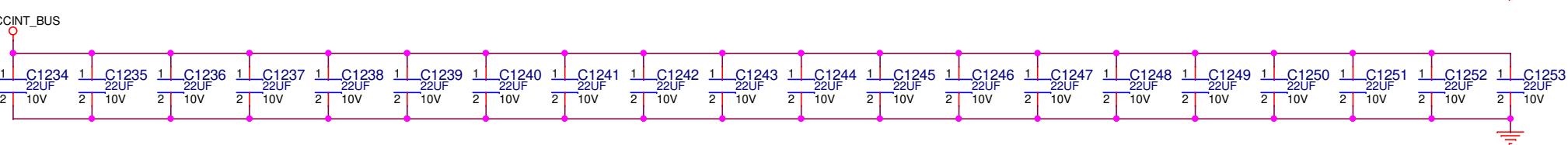
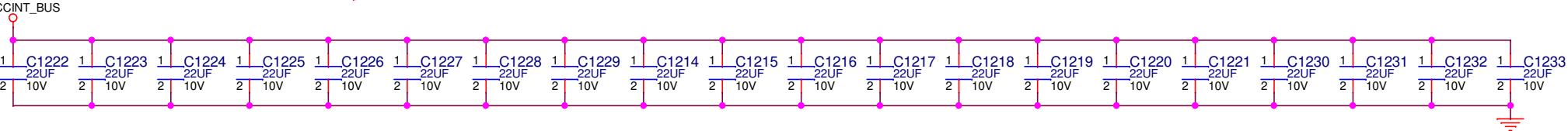
2100 Logic Drive
San Jose, CA 95124

STD

Title: HW-Z1-ZCU208
047 VCCINT - VCCINT_AMS PMIC1

Size	Date Modified:	Document Number:
B	Friday, November 22, 2019	038-05023-01 Rev A01
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XILINX

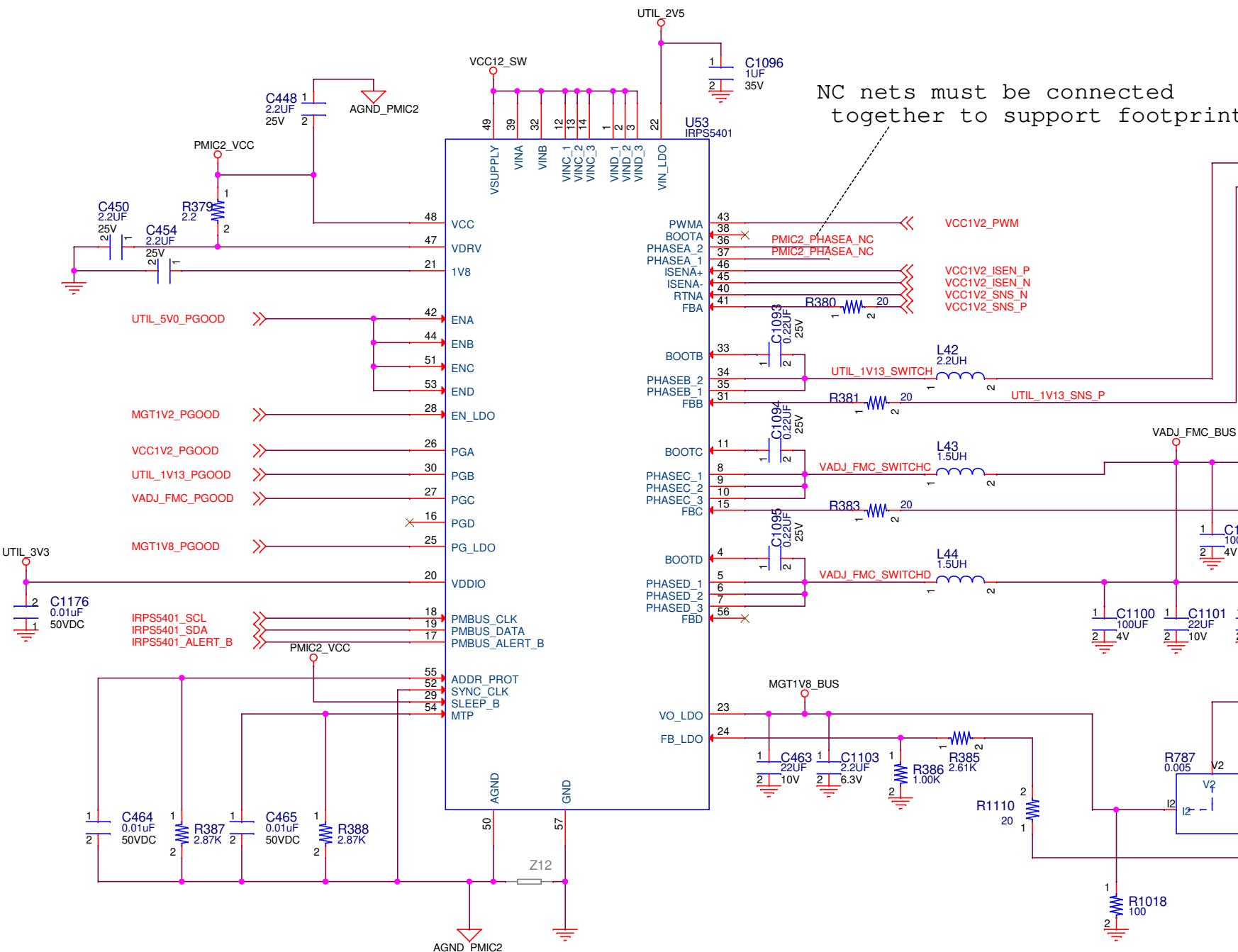
2100 Logic Drive
San Jose, CA 95124

STD

Title: HW-Z1-ZCU208
049 VCCINT - VCCINT_AMS Decap

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B	Friday, November 22, 2019	038-05023-01 Rev A01
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REPLACE IC WITH CORRECT FIRMWARE P/N



MTP : +4
7-BIT I2C ADDR: 0x14
7-BIT PMBUS ADDR: 0x44

1.13V @ 500mA

1.8V @ 6A

1.8V @ 500mA

XILINX

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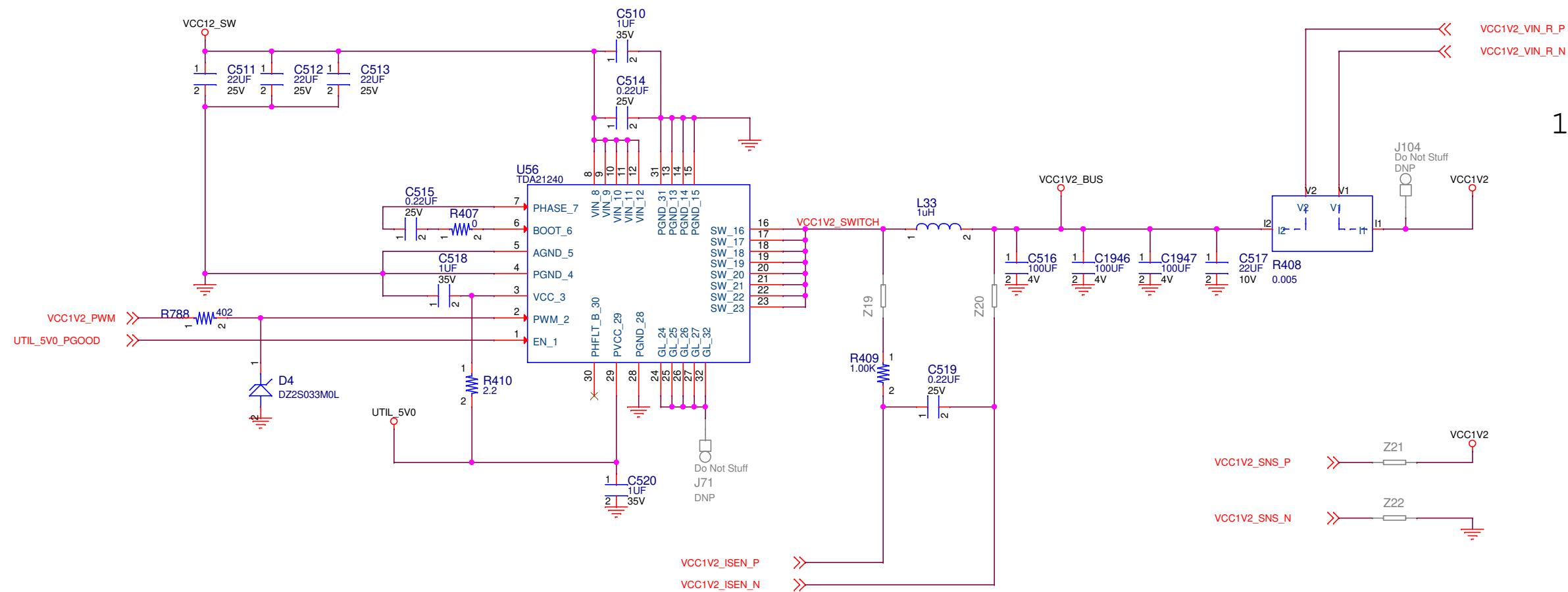
STD

Title: HW-Z1-ZCU208
050 PMIC 2

Size Date Modified: Document Number: Rev

B Friday, November 22, 2019 038-05023-01 A01

Engineer: BF Sheet 50 of 80

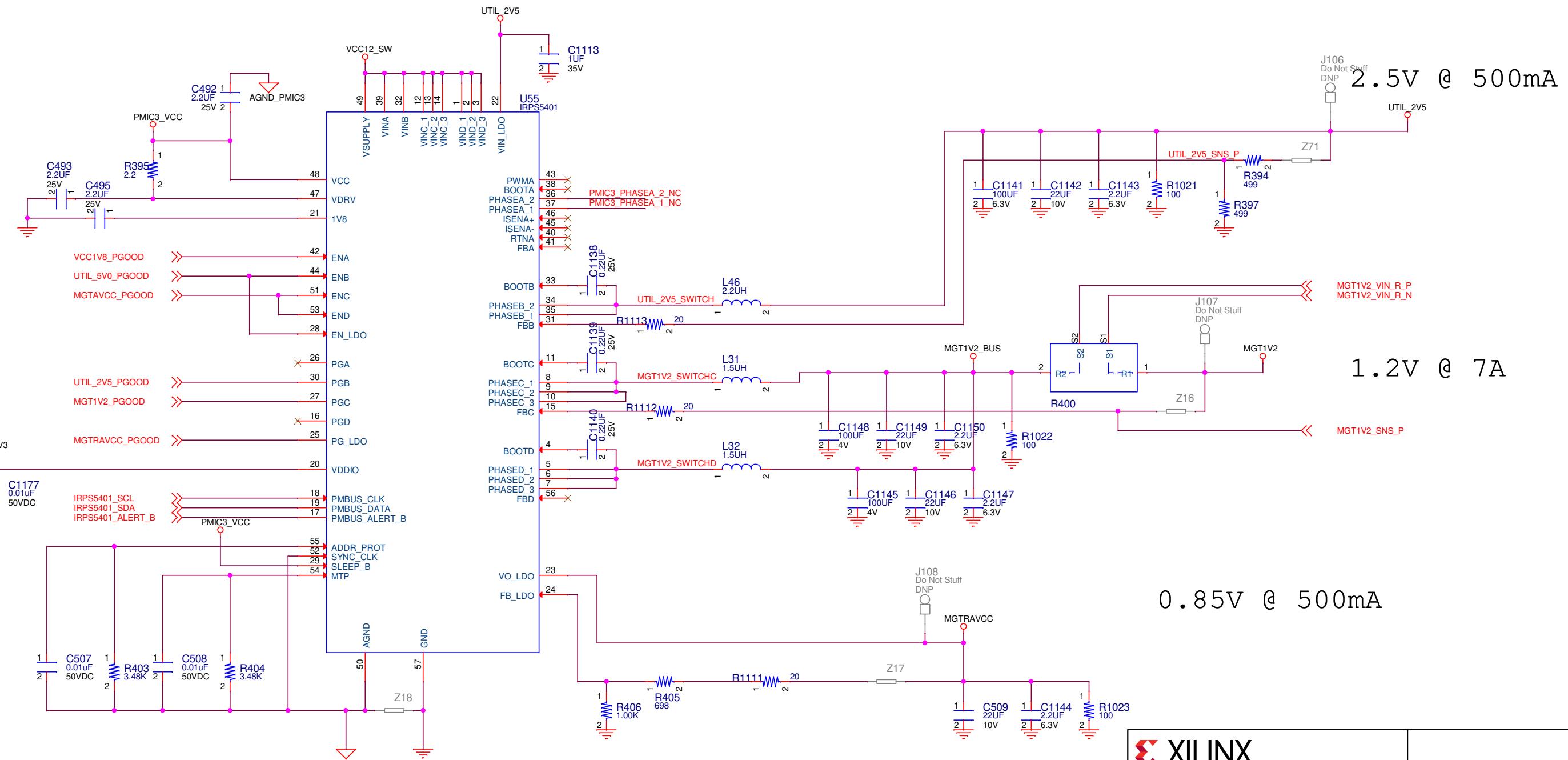


XILINX
2100 Logic Drive
San Jose, CA 95124

Title: HW-Z1-ZCU208
051 PMIC 2 Power Stage

Size: B	Date Modified: Friday, November 22, 2019	Document Number: 038-05023-01	Rev: A01
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REPLACE IC WITH CORRECT FIRMWARE P/N



MTP: +5

7-BIT I2C ADDR: 0x15

7-BIT PMBUS ADDR: 0x45

XILINX

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San Jose, CA 95124

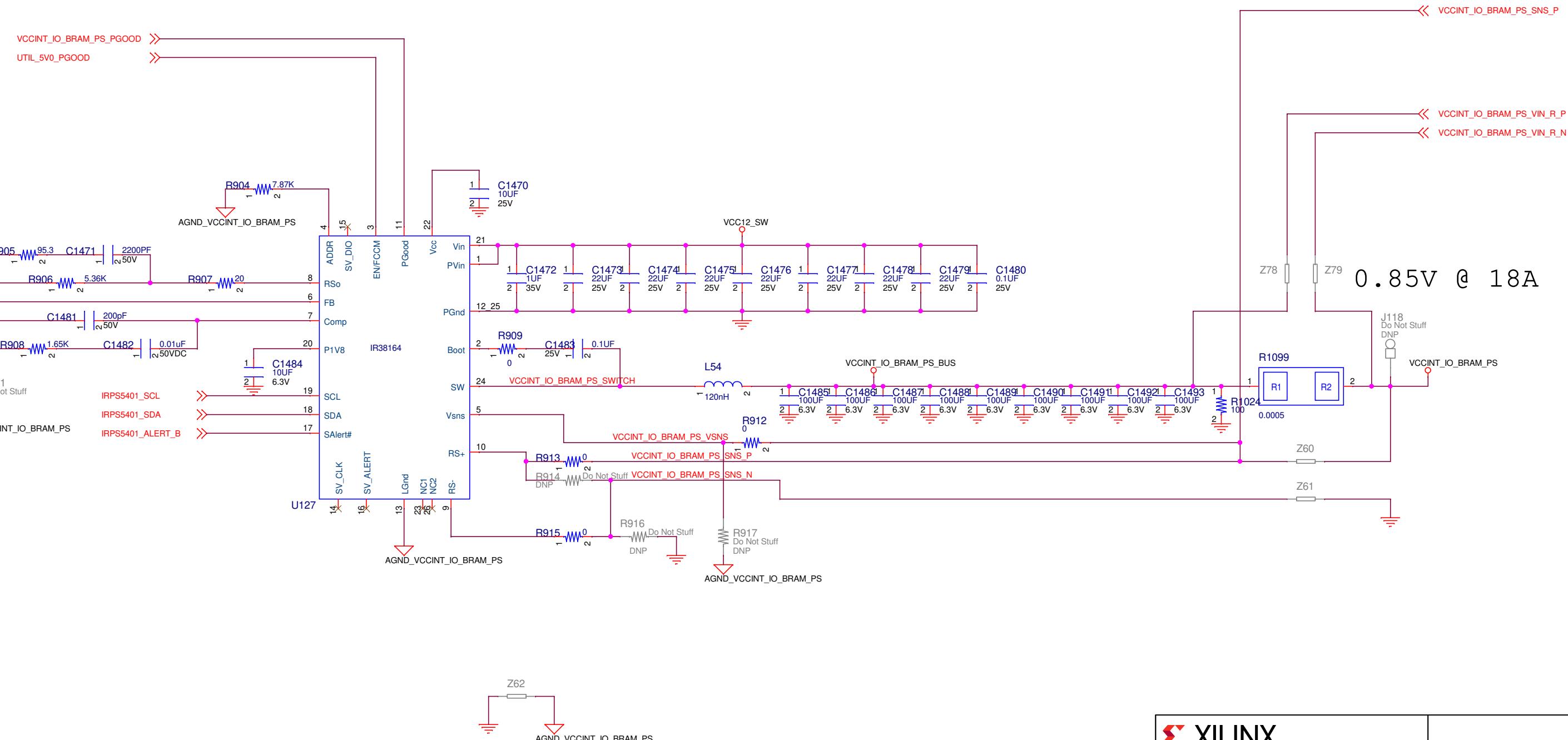
STD

Title: HW-Z1-ZCU208
052 PMIC 3

Size: **B** Date Modified: Tuesday, December 03, 2019 Document Number: 038-05023-01 Rev A01

Engineer: BF Sheet 52 of 80

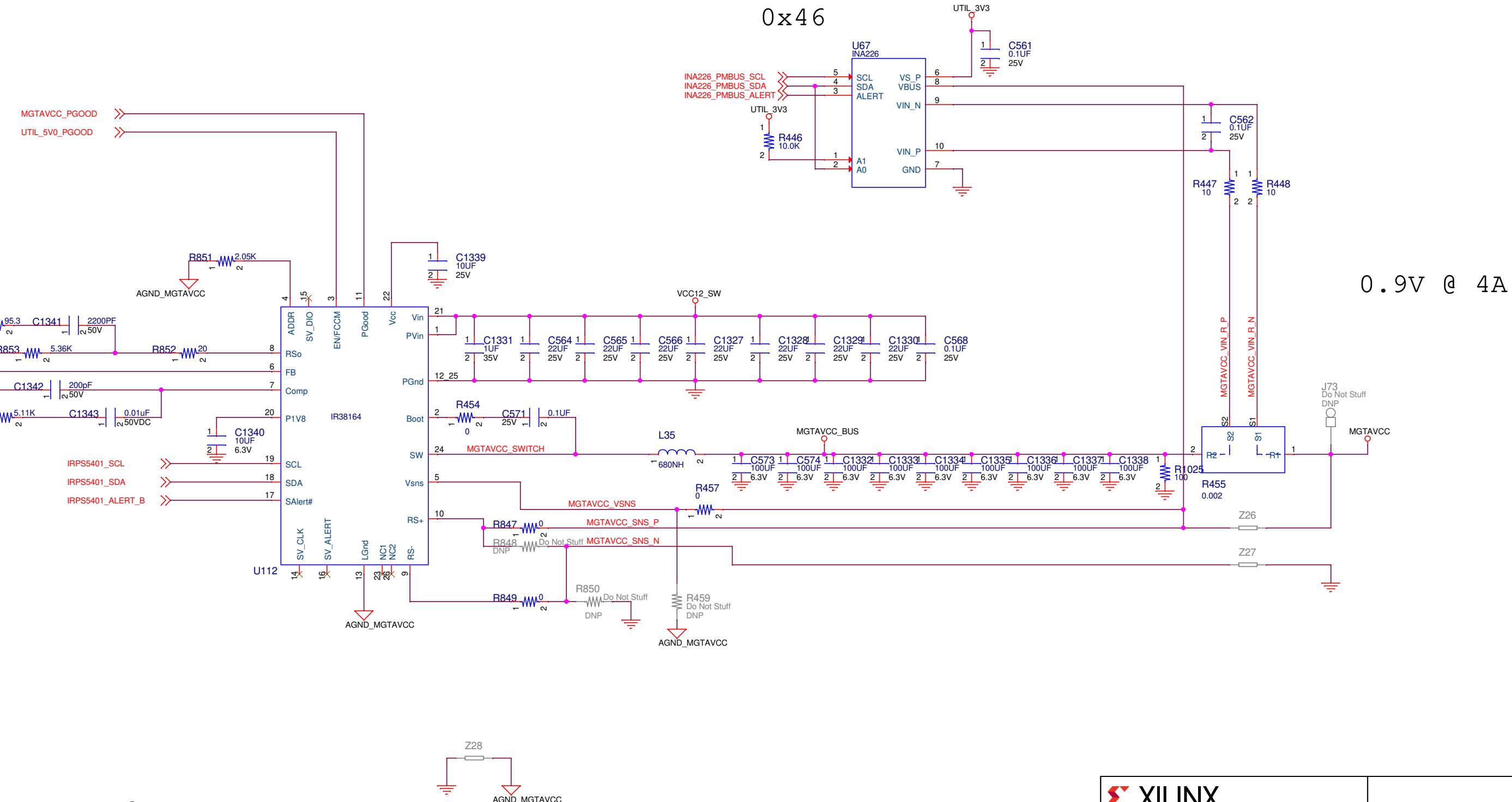
REPLACE IC WITH CORRECT FIRMWARE P/N



XILINX 2100 Logic Drive San Jose, CA 95124		STD
Title: HW-Z1-ZCU208 053 VCCINT_IO_BRAM_PS 18A Reg		
Size: B	Date Modified: Friday, November 22, 2019	Document Number: 038-05023-01 Rev A01
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REPLACE IC WITH CORRECT FIRMWARE P/N

I2C ADDR
0x46



OFFSET: +3

7-BIT I2C ADDR: 0x13

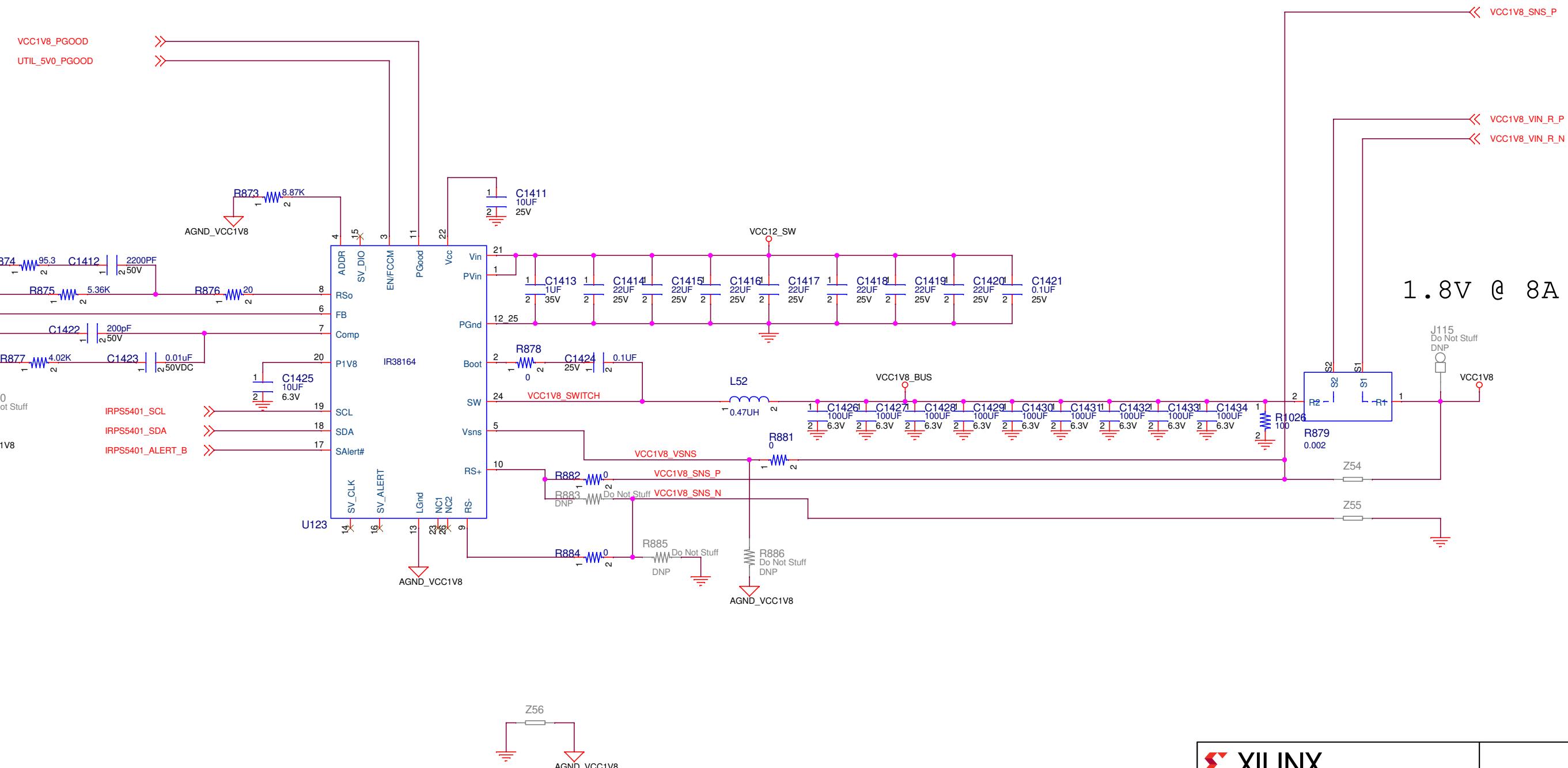
7-BIT PMBUS ADDR: 0x43

XILINX
2100 Logic Drive
San Jose, CA 95124

Title: HW-Z1-ZCU208
054 MGTAVCC 4A Regulator

Size: B	Date Modified: Friday, November 22, 2019	Document Number: 038-05023-01	Rev: A01
Engineer: BF		Sheet 54 of 80	

REPLACE IC WITH CORRECT FIRMWARE P/N

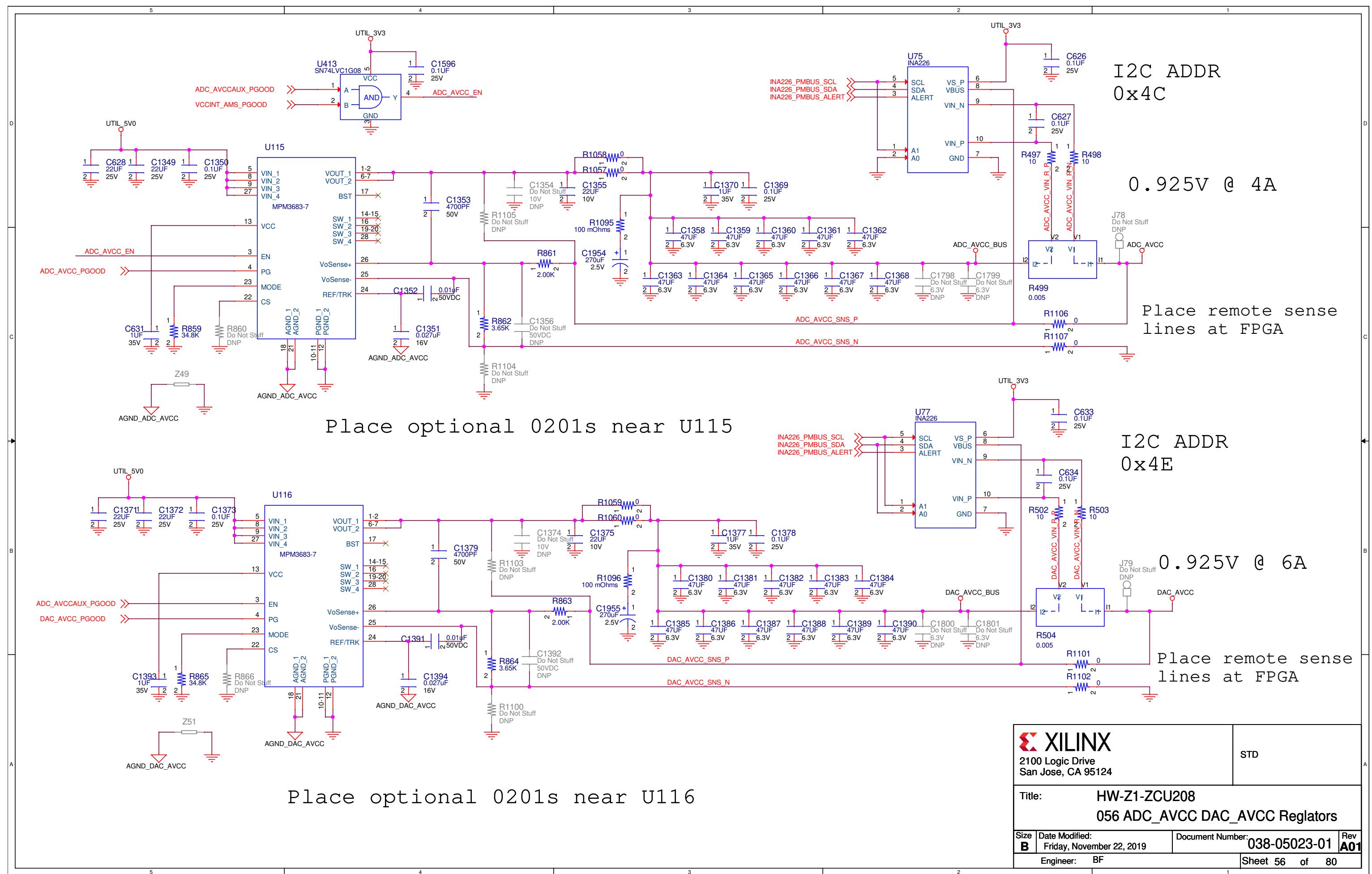


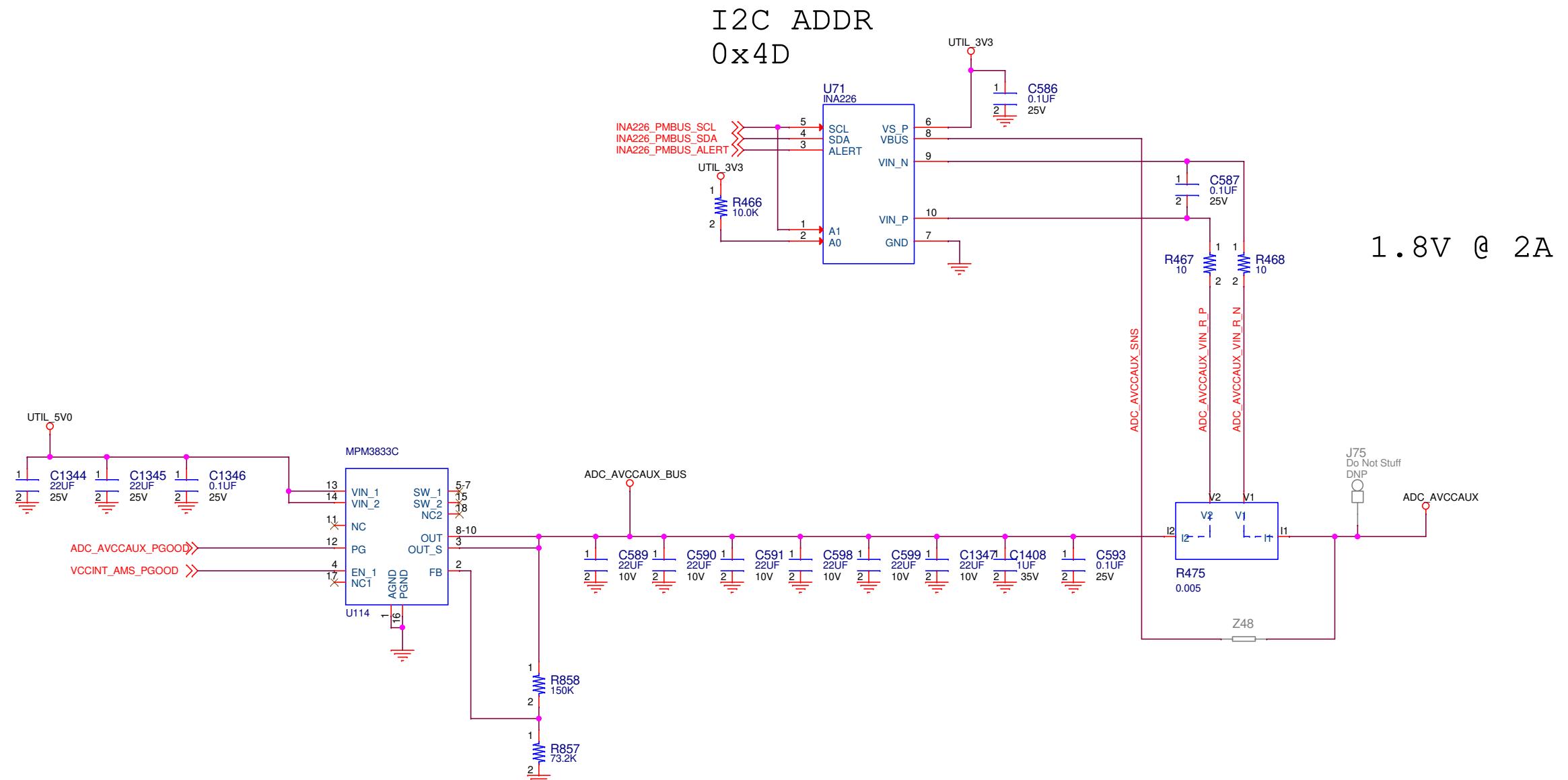
OFFSET: +12

7-BIT I2C ADDR: 0x1C

7-BIT PMBUS ADDR: 0x4C

XILINX 2100 Logic Drive San Jose, CA 95124		STD
Title: HW-Z1-ZCU208 055 VCC1V8 8A Reg		
Size: B	Date Modified: Friday, November 22, 2019	Document Number: 038-05023-01 Rev A01
Engineer: BF	Sheet 55 of 80	

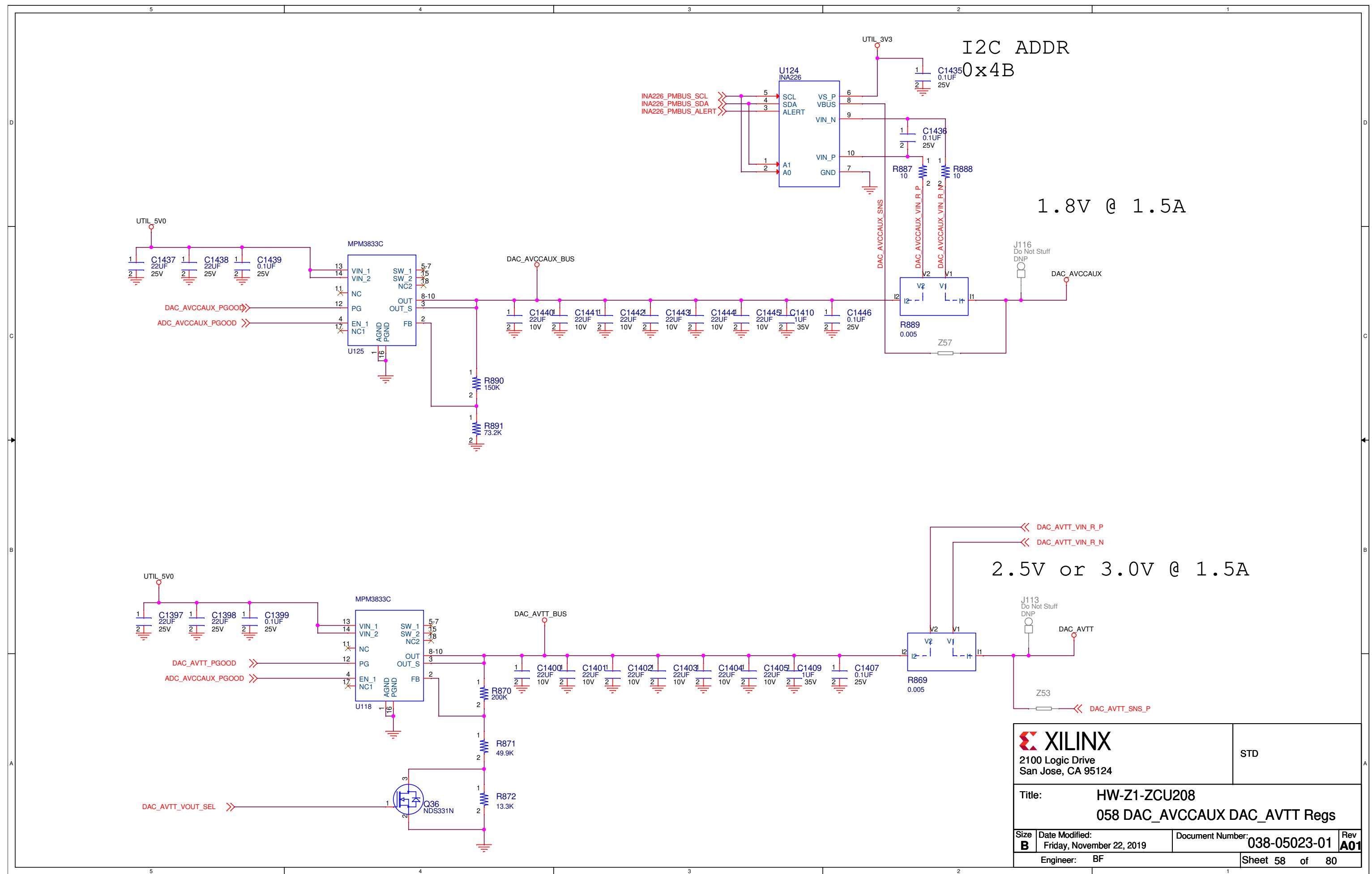


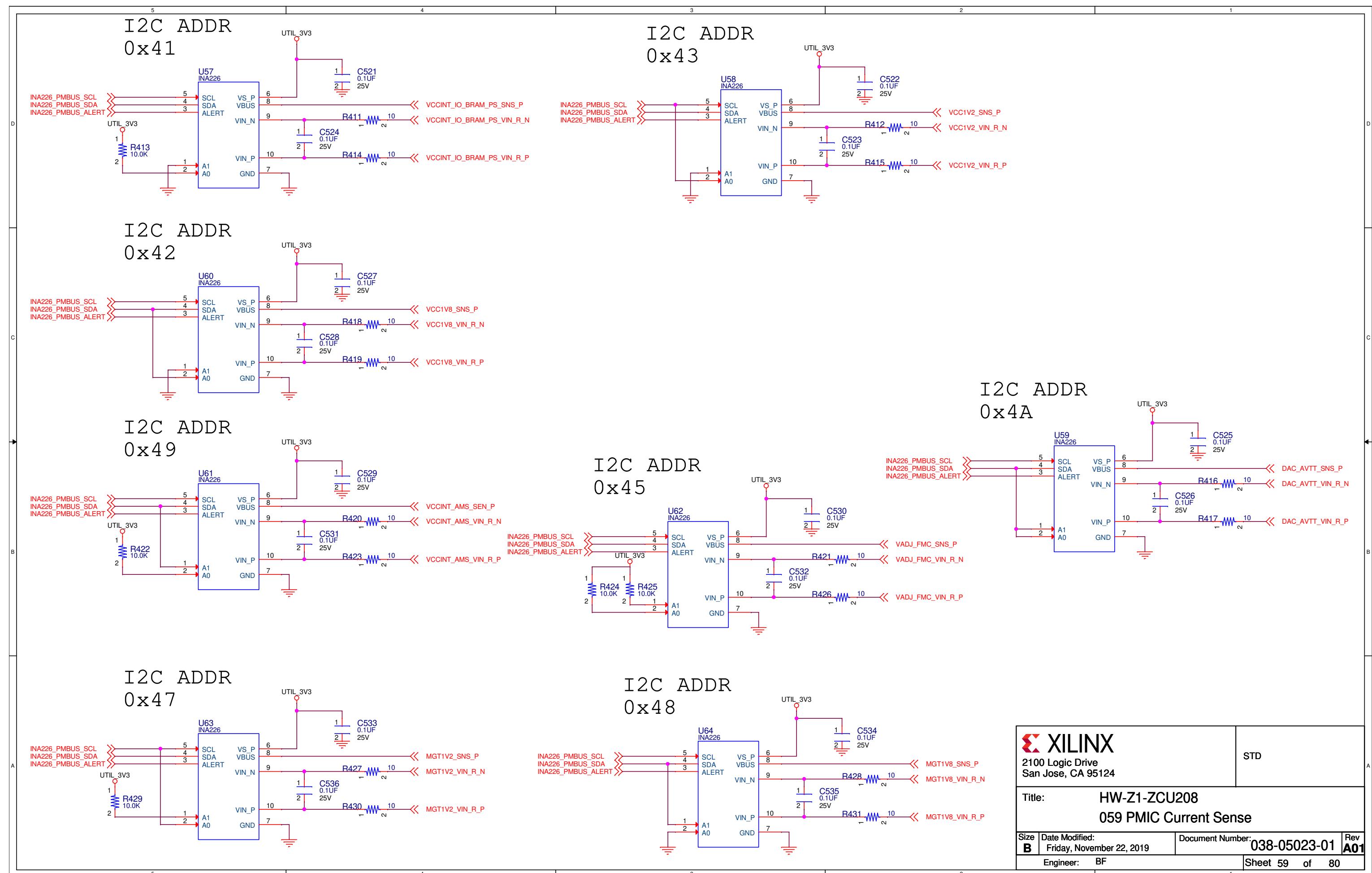


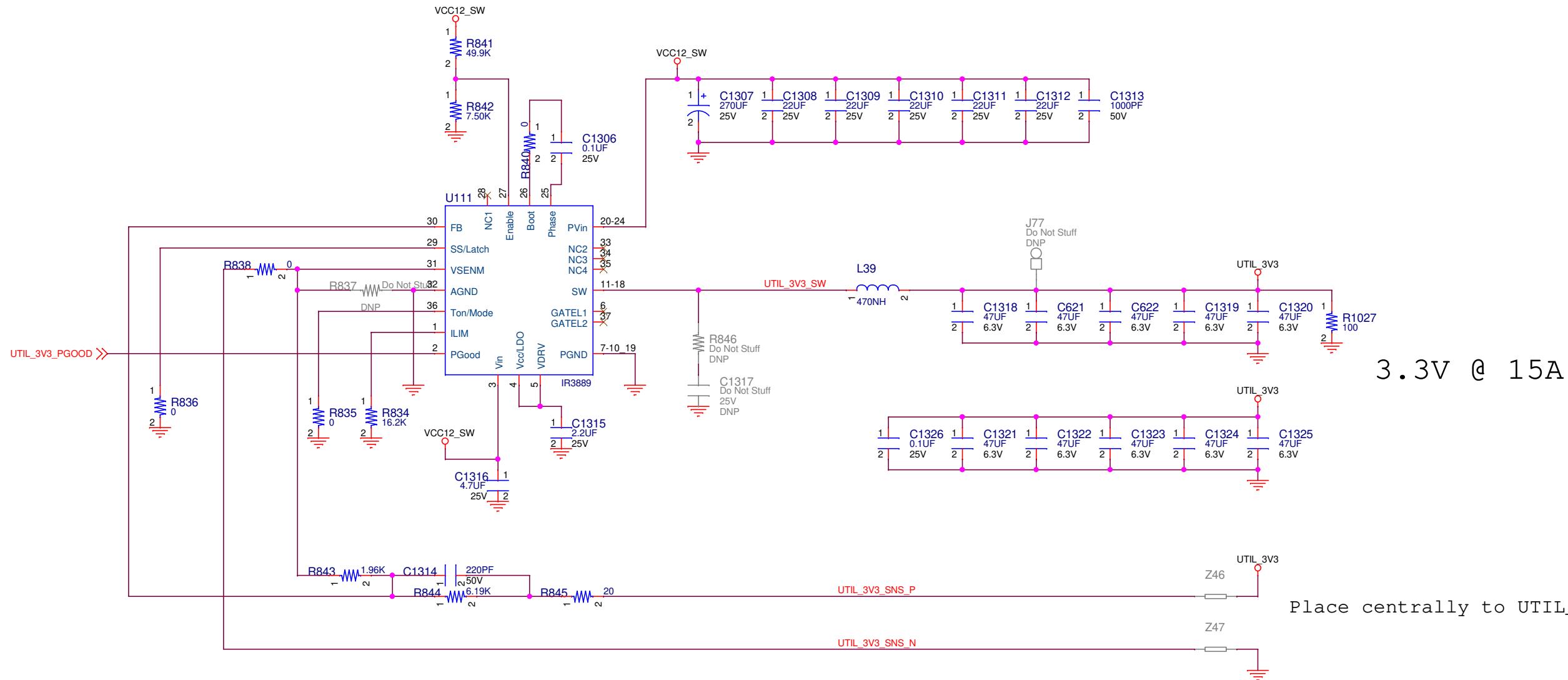
XILINX
2100 Logic Drive
San Jose, CA 95124

Title: **HW-Z1-ZCU208**
057 ADC_AVCCAUX 2A Regulator

Size	Date Modified:	Document Number:
B	Friday, November 22, 2019	038-05023-01 Rev A01
Engineer: BF		Sheet 57 of 80







3.3V @ 15A

Place centrally to UTIL_3V3 Load

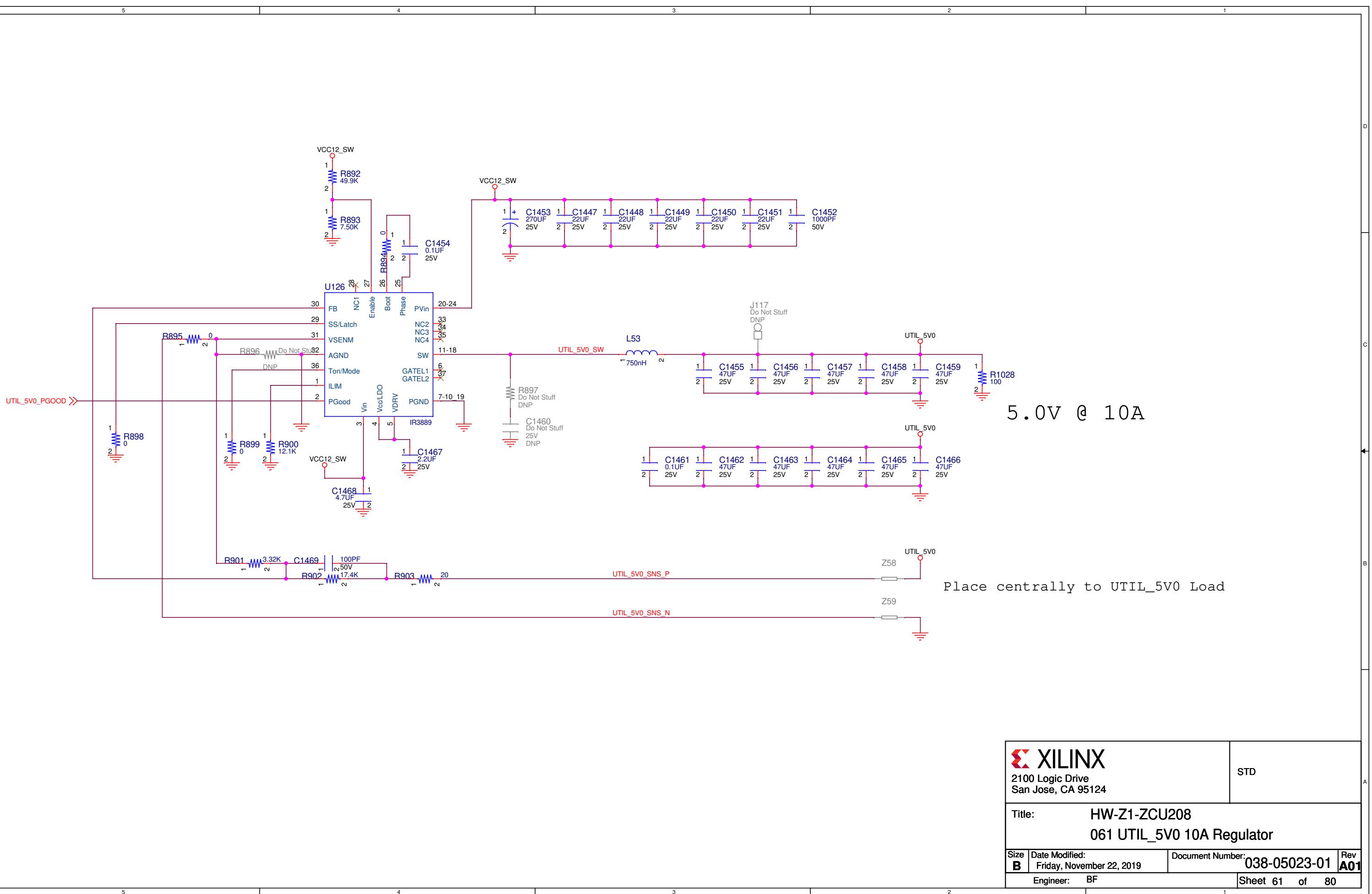


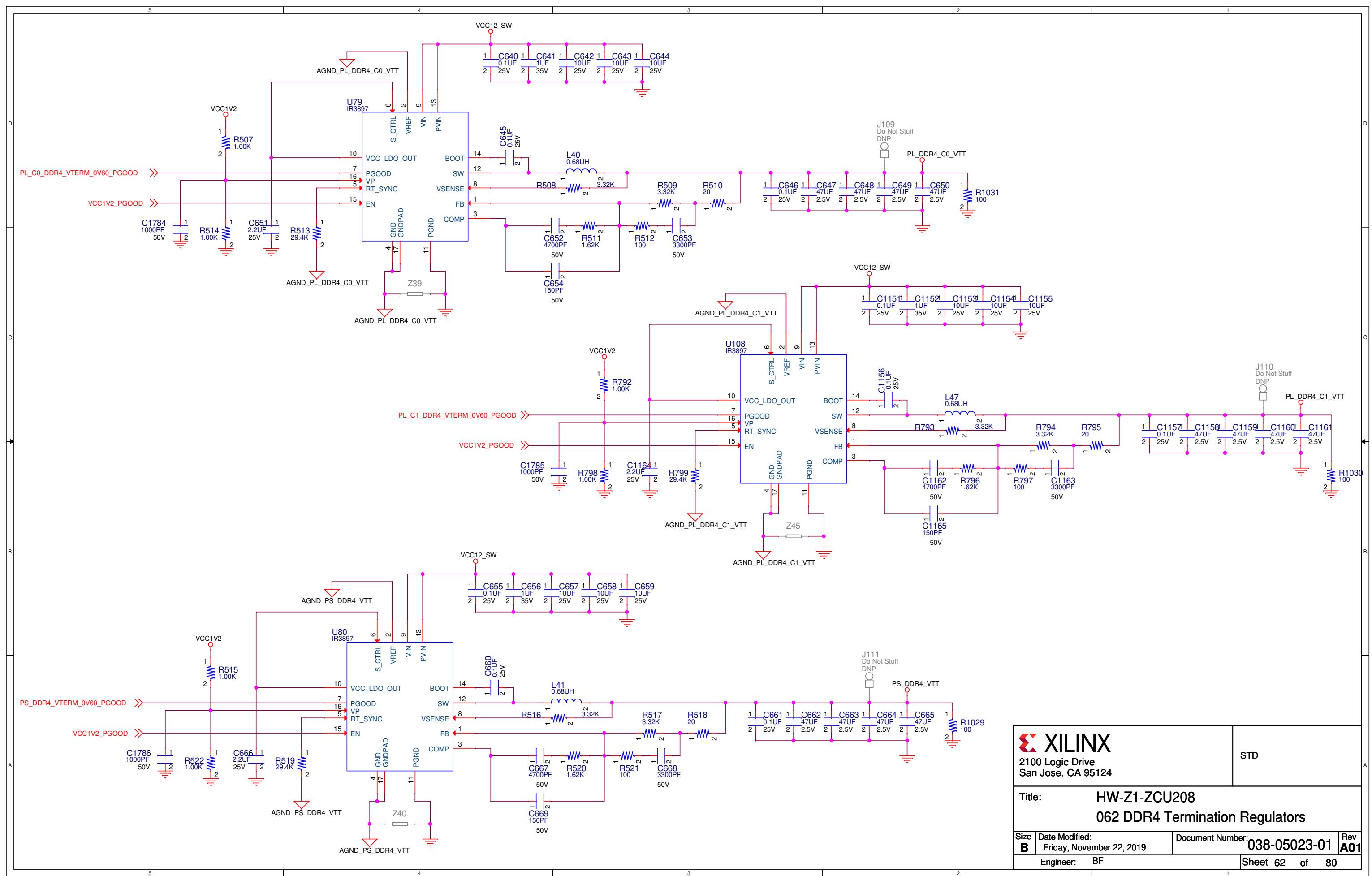
**2100 Logic Drive
San Jose, CA 95124**

Title: HW-Z1-ZCU208

060 UTIL_3V3 15A Regulator

Size	Date Modified: Friday, November 22, 2019	Document Number: 038-05023-01	Rev
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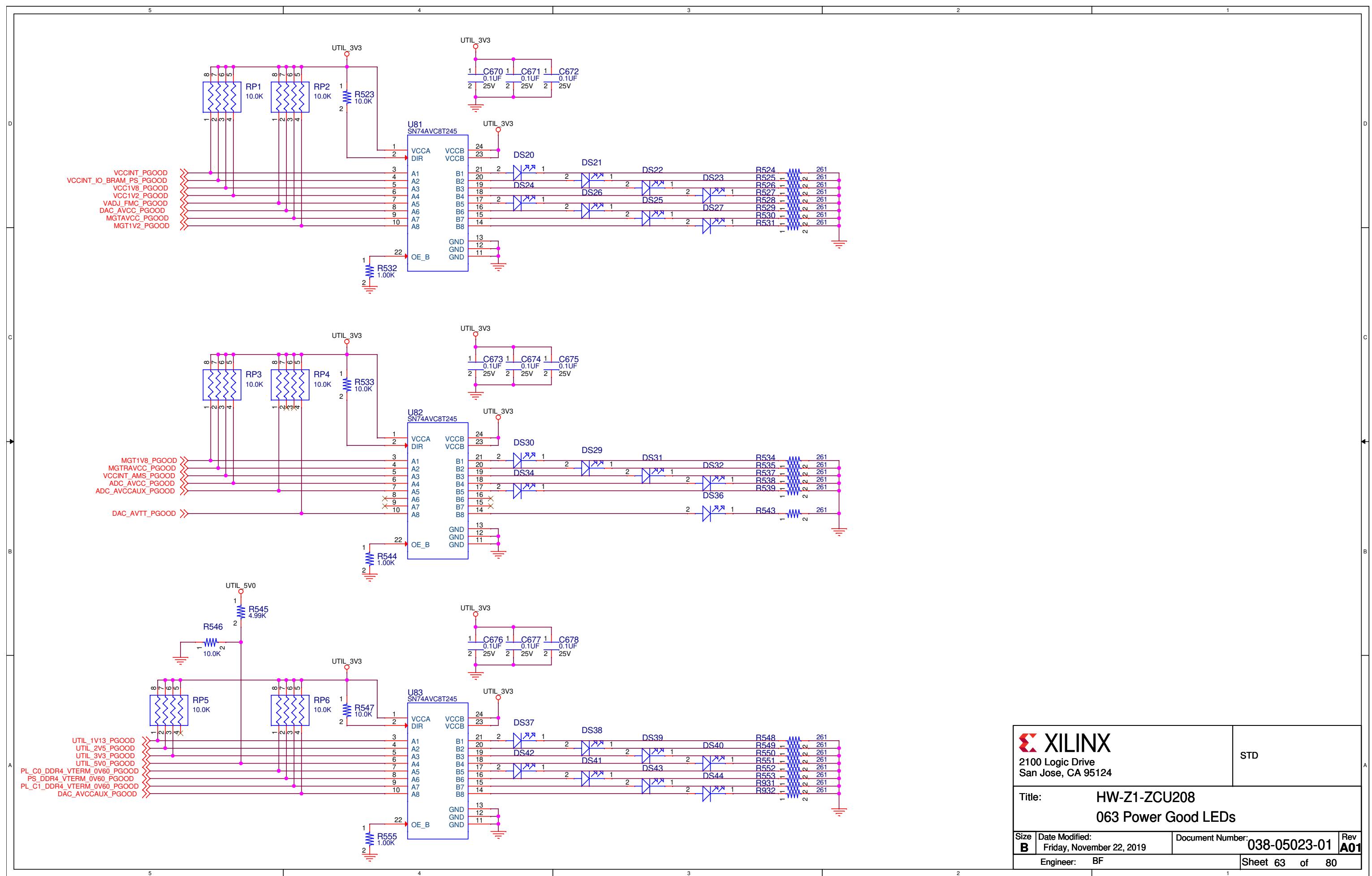




XILINX
2100 Logic Drive
San Jose, CA 95124

Title: HW-Z1-ZCU208
062 DDR4 Termination Regulators

Size: B	Date Modified: Friday, November 22, 2019	Document Number: 038-05023-01	Rev: A01
Engineer: BF		Sheet 62 of 80	



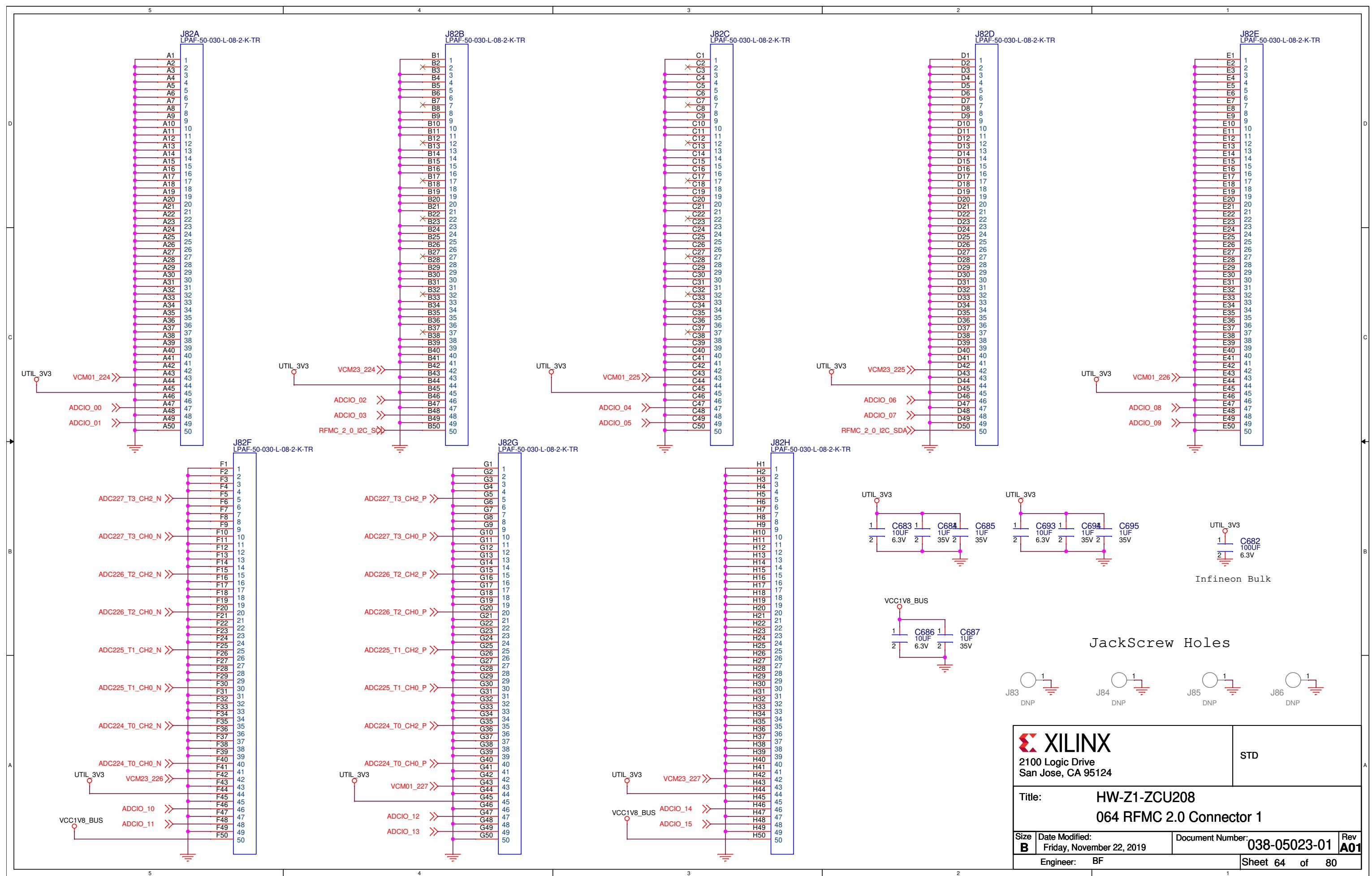
XILINX

2100 Logic Drive
San Jose, CA 95124

STD

Title: **HW-Z1-ZCU208**
063 Power Good LEDs

Size	Date Modified:	Document Number:
B	Friday, November 22, 2019	038-05023-01 Rev A01
Engineer:	BF	Sheet 63 of 80



XILINX

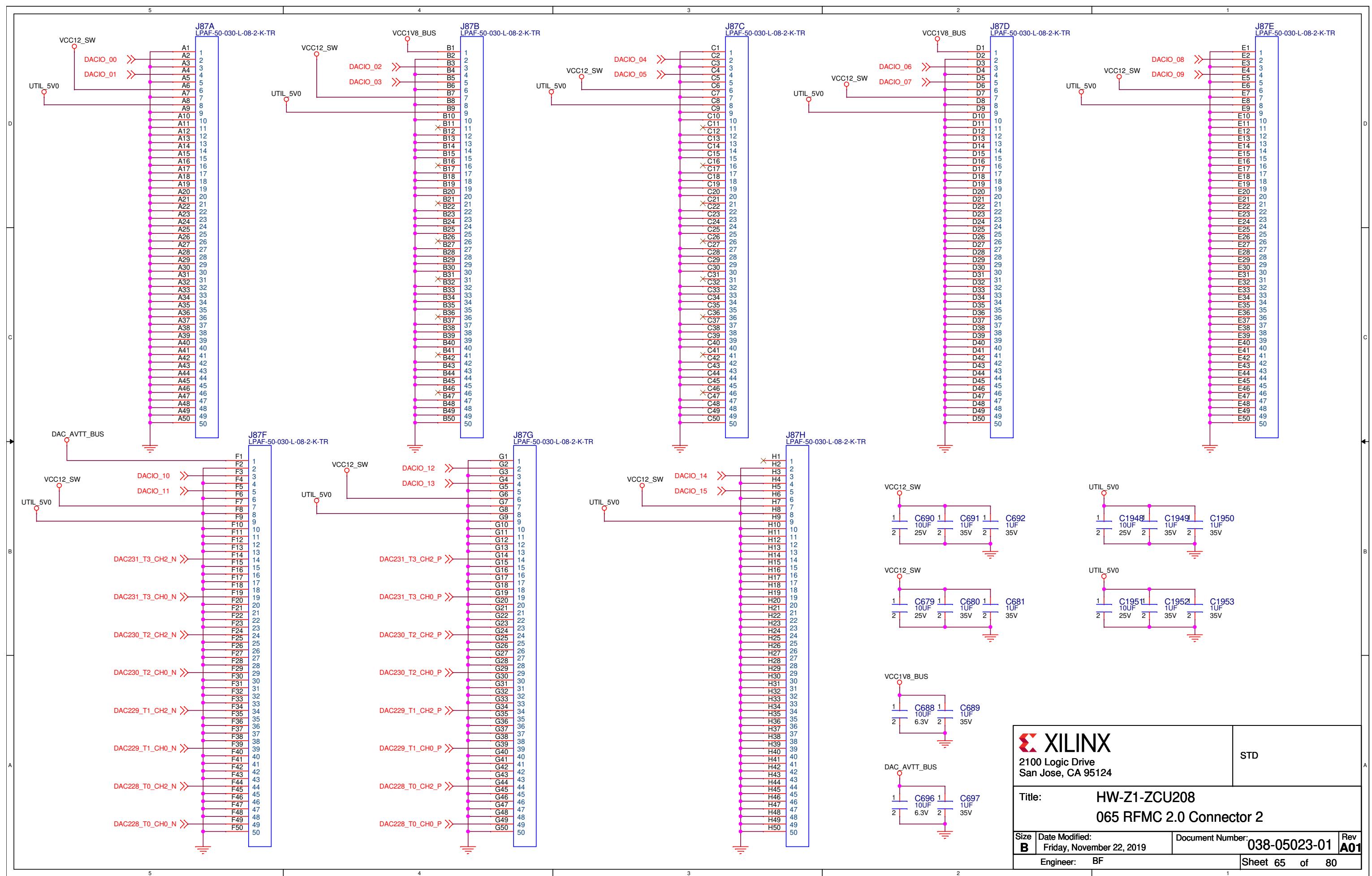
2100 Logic Drive
San Jose, CA 95124

STD

Title: **HW-Z1-ZCU208**
064 RFMC 2.0 Connector 1

Size Date Modified: **B** Friday, November 22, 2019 Document Number: **038-05023-01** Rev **A01**

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XILINX

2100 Logic Drive
San Jose, CA 95124

STD

Title: **HW-Z1-ZCU208**
065 RFMC 2.0 Connector 2

Size Date Modified: **B** Friday, November 22, 2019 Document Number: **038-05023-01** Rev **A01**

Engineer: **BF** Sheet 65 of 80

D

D

C

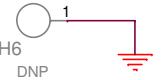
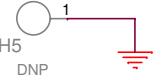
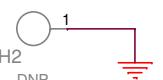
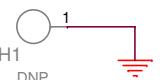
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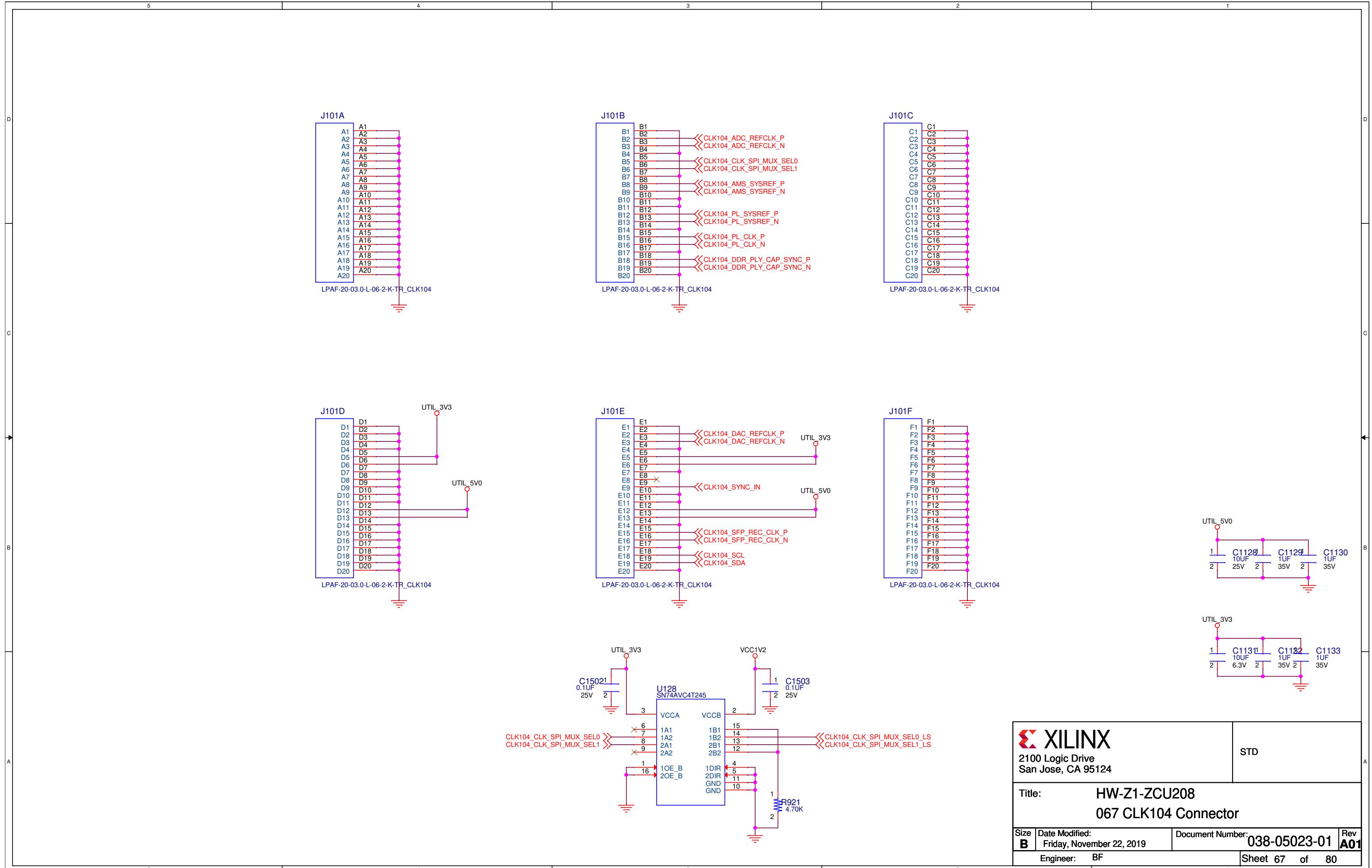
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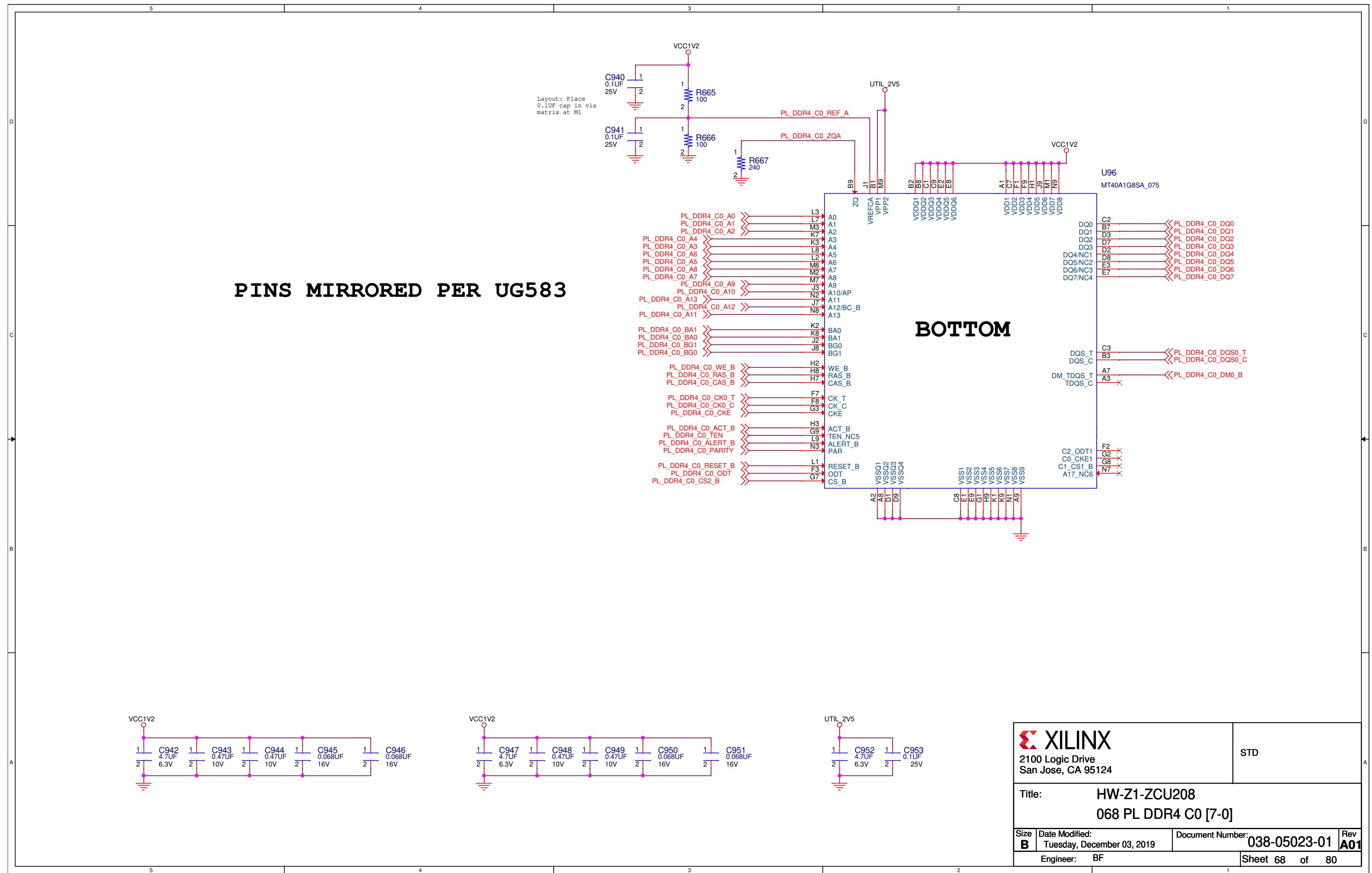
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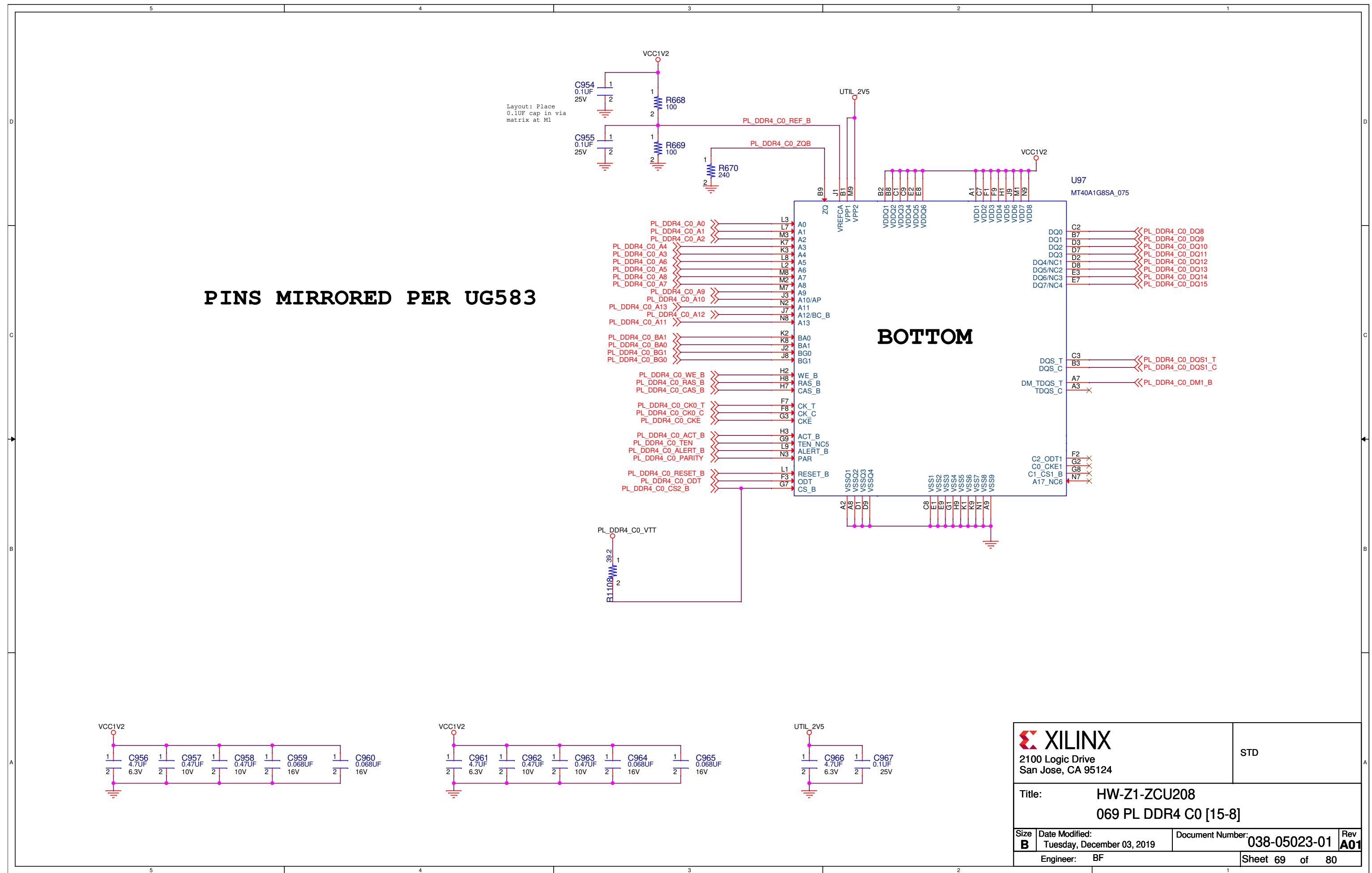
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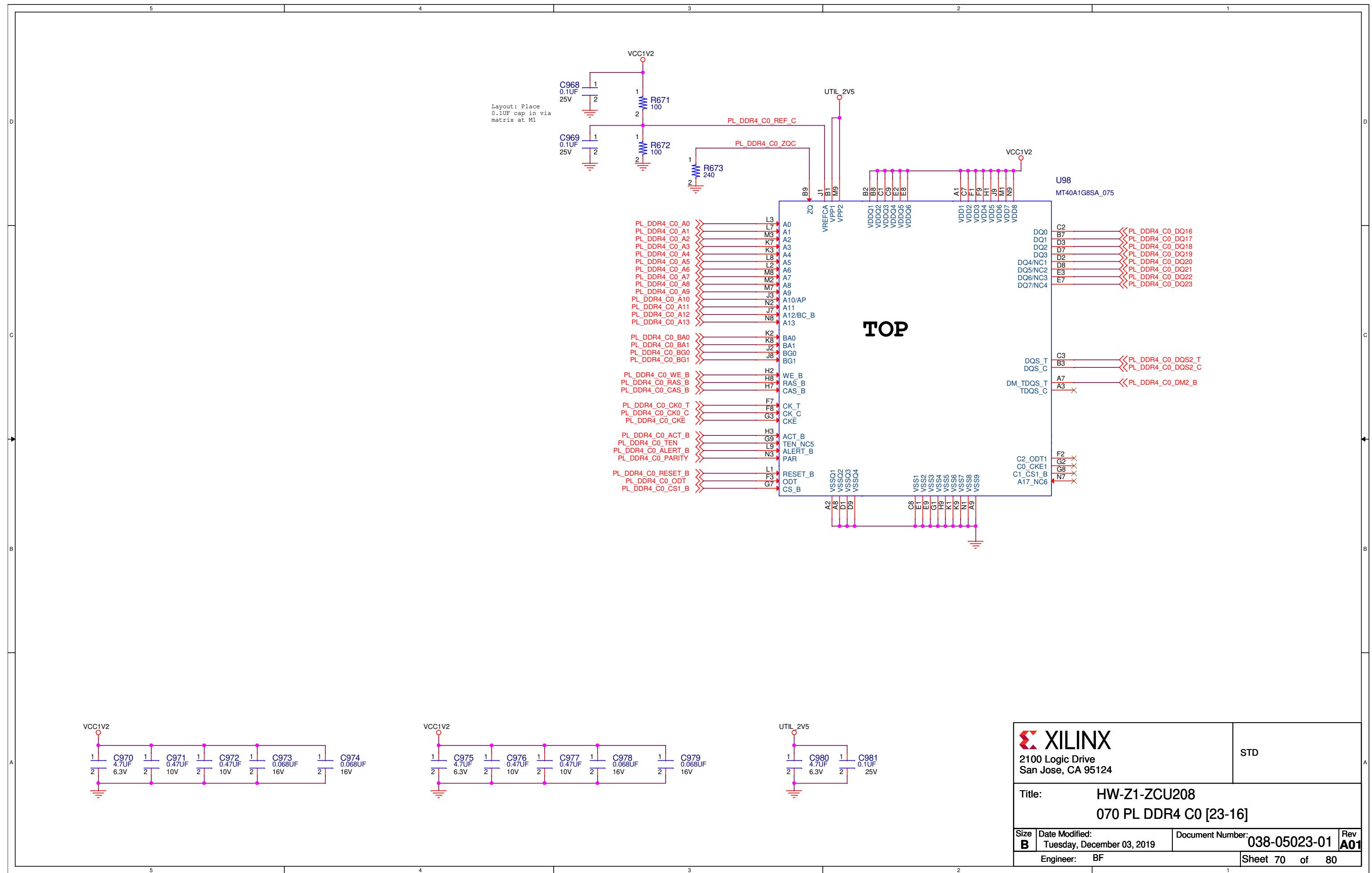


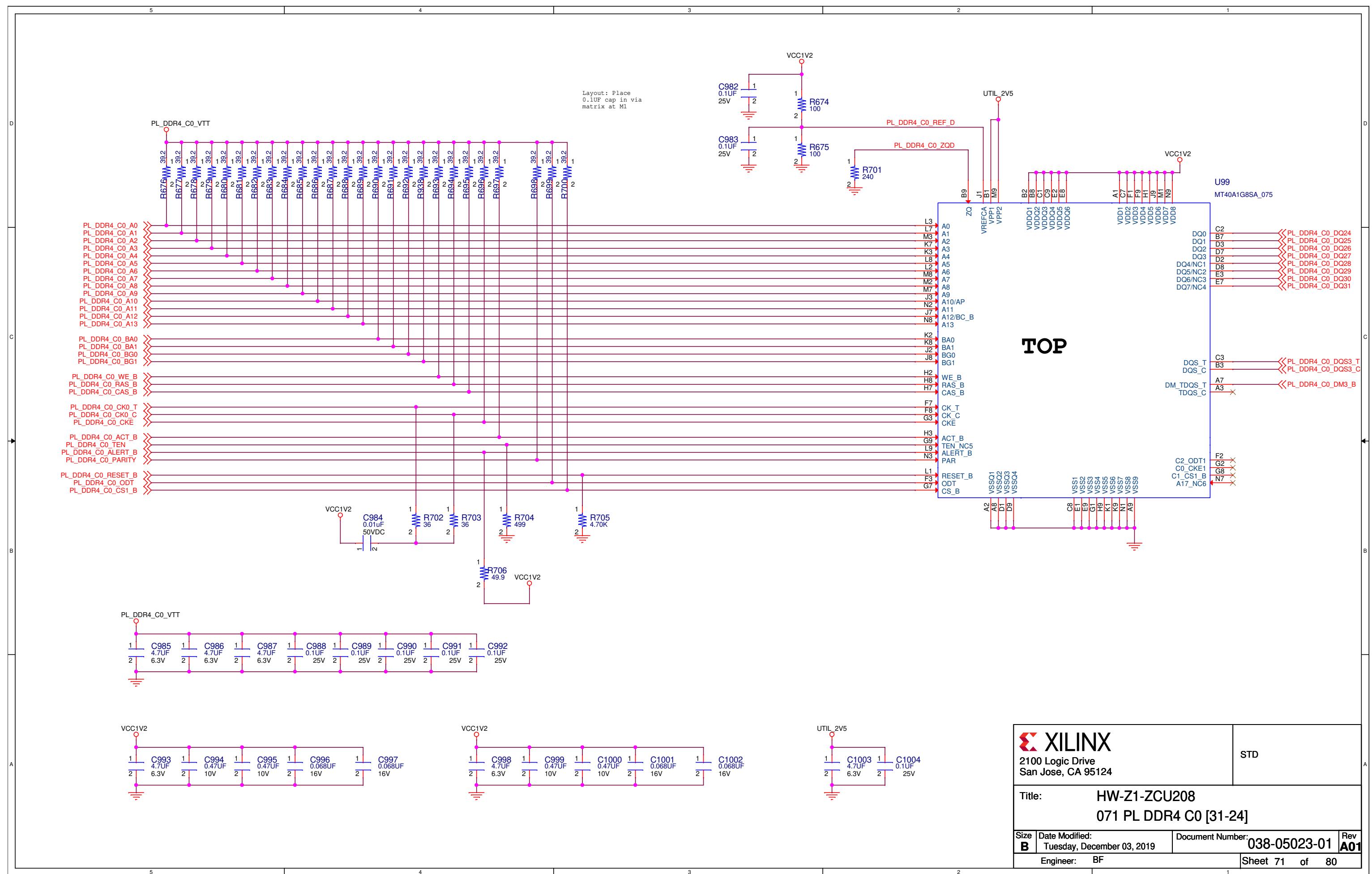
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2100 Logic Drive San Jose, CA 95124		
Title:	HW-Z1-ZCU208	
	066 Mechanicals	
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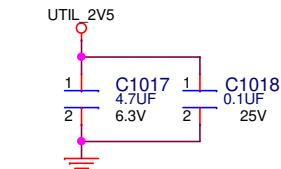
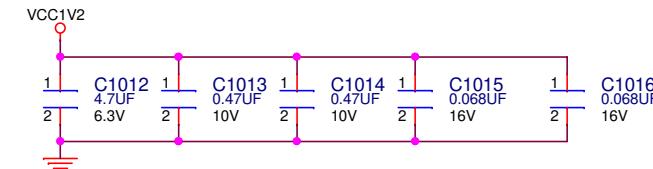
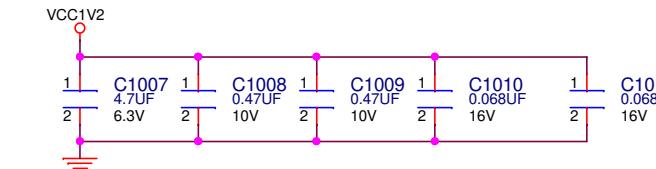








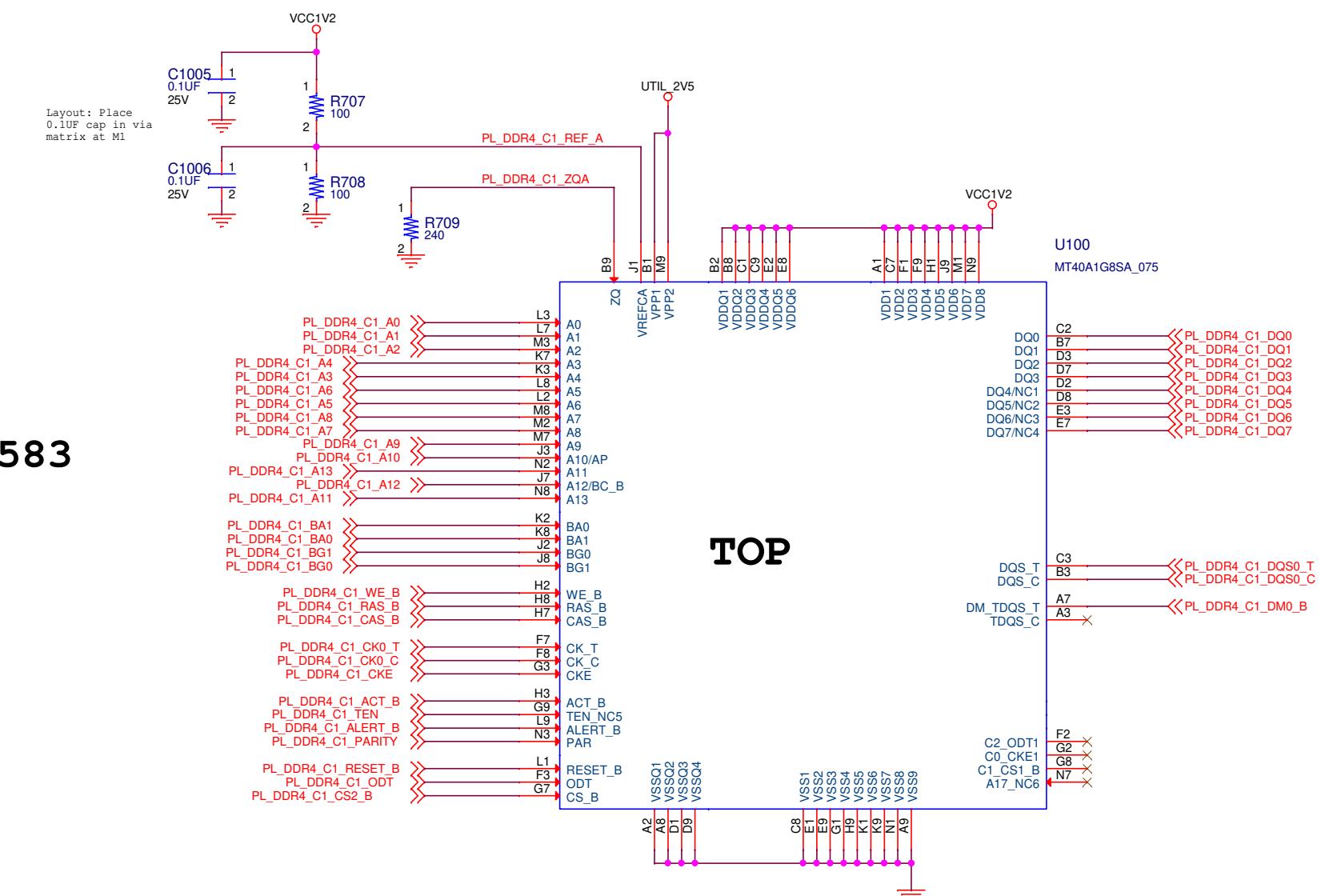




XILINX 2100 Logic Drive San Jose, CA 95124		STD
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PINS MIRRORED PER UG583

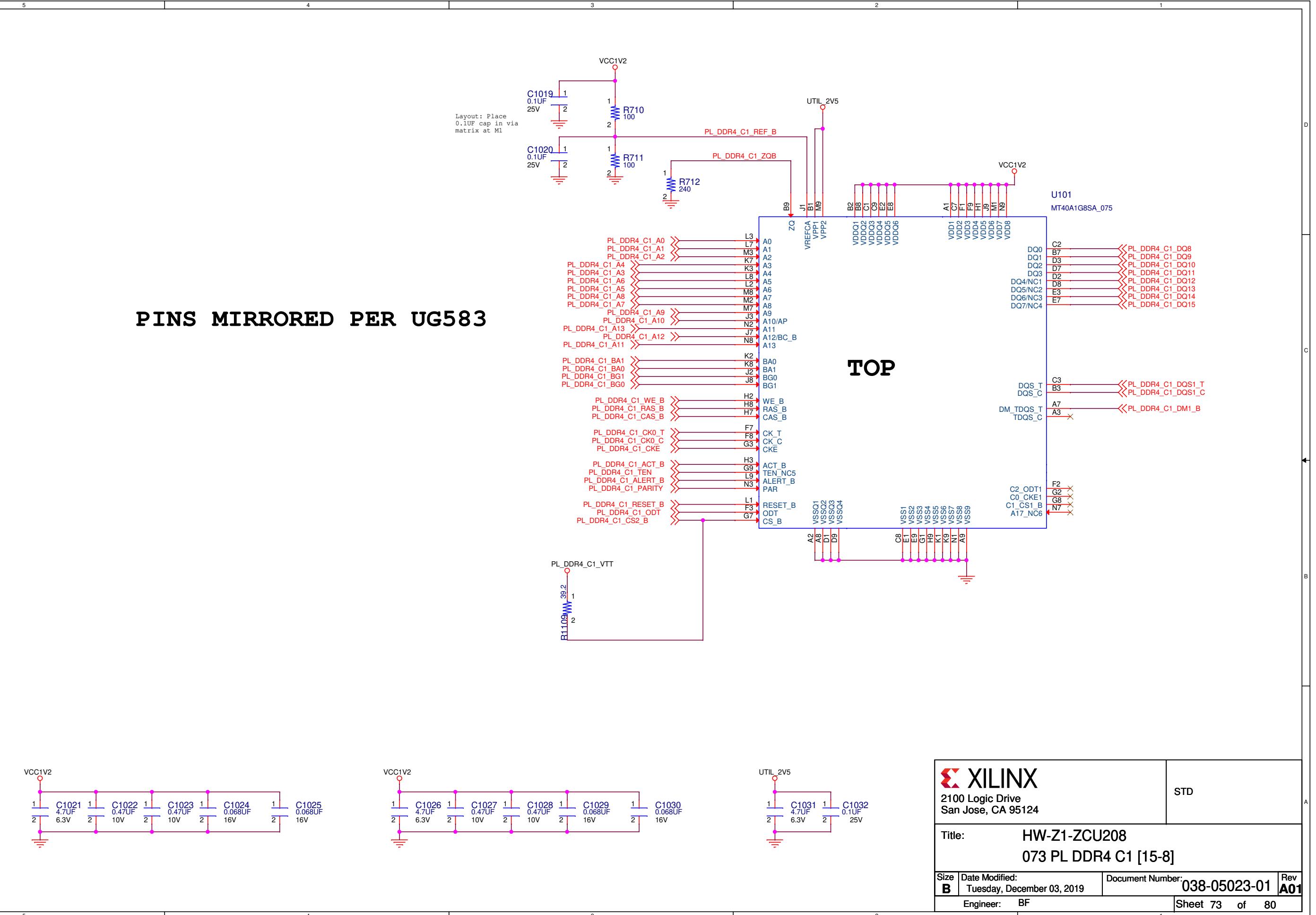
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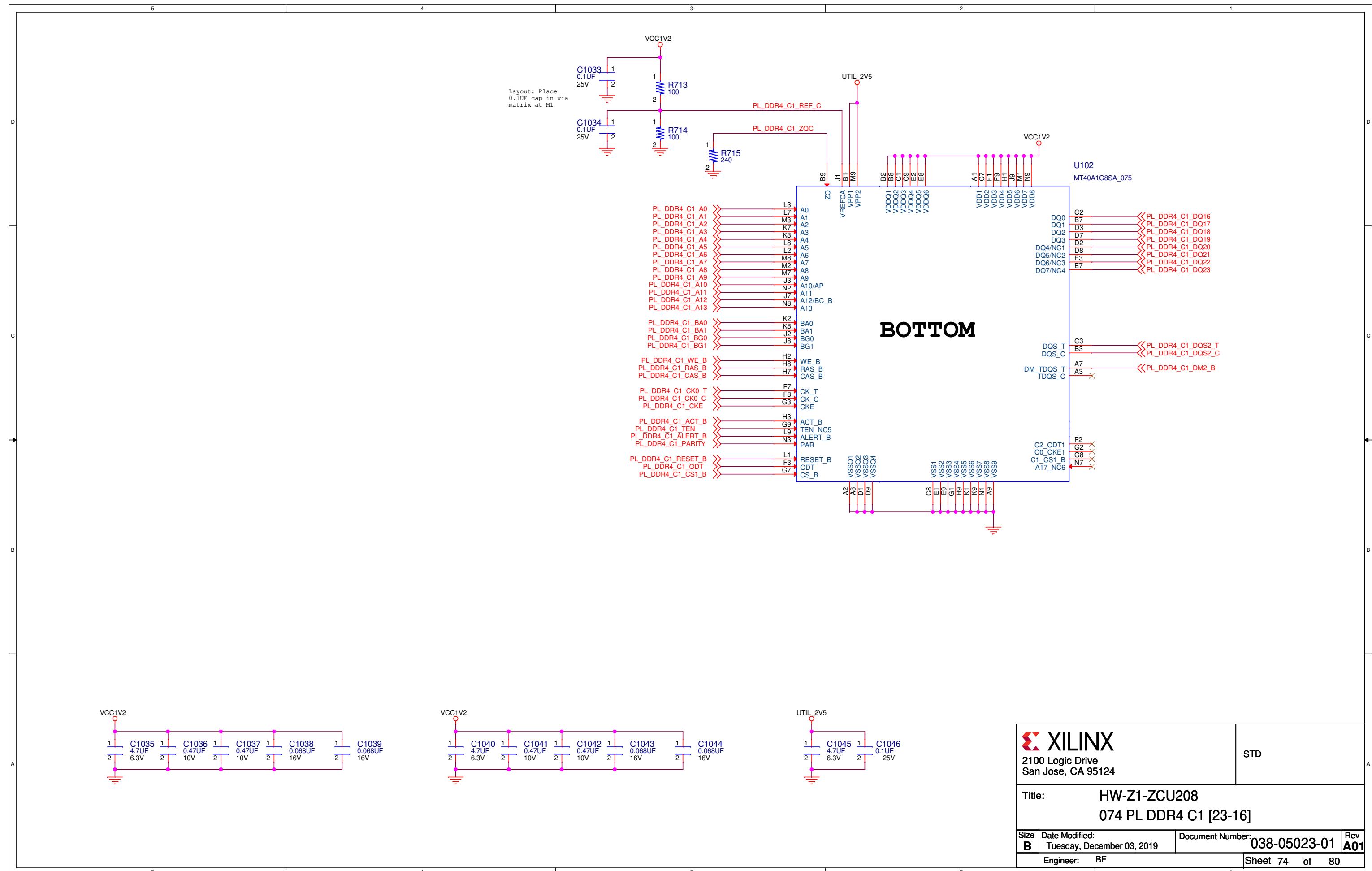


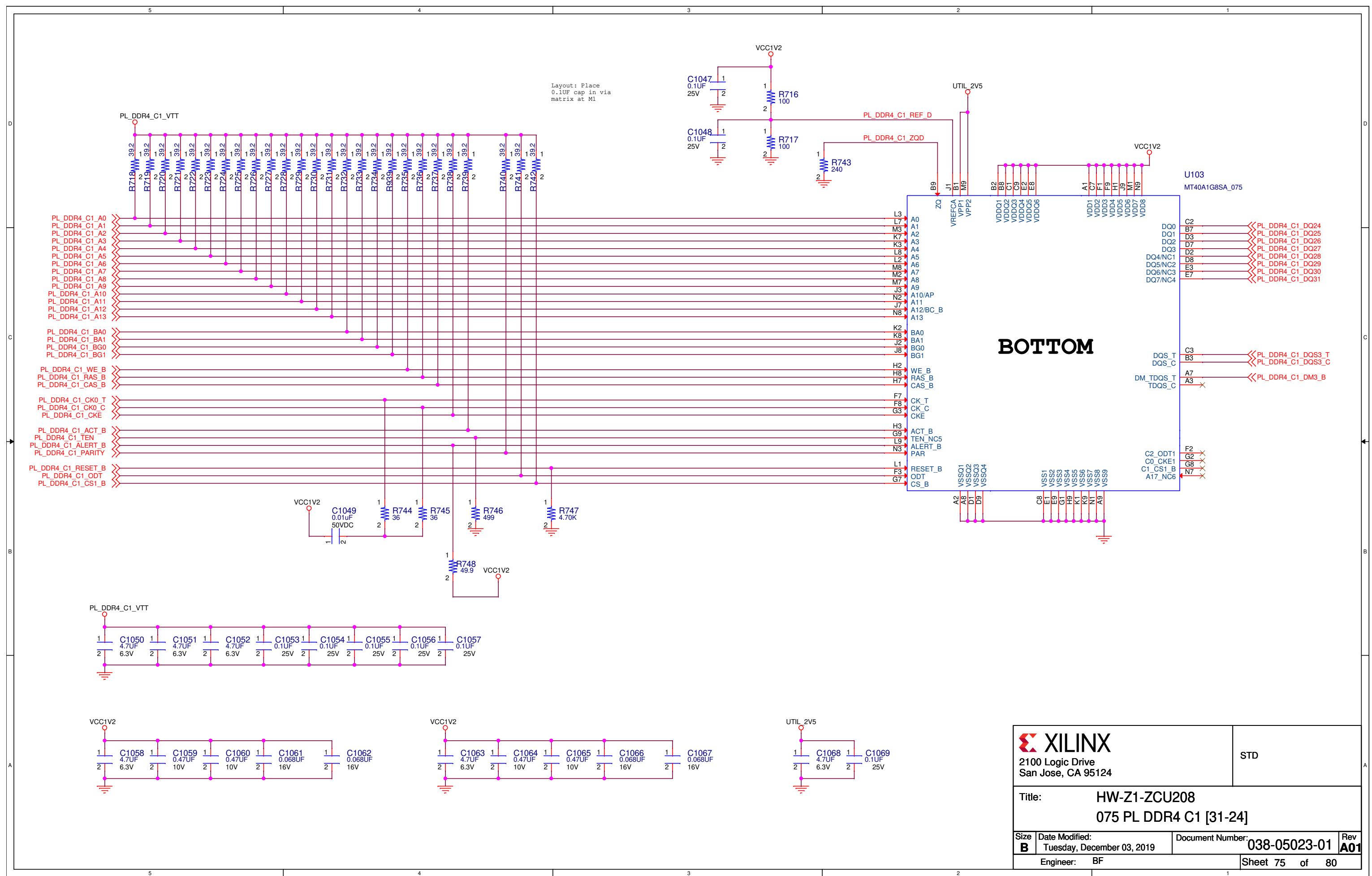
Layout: Place 0.1UF cap in via matrix at M1

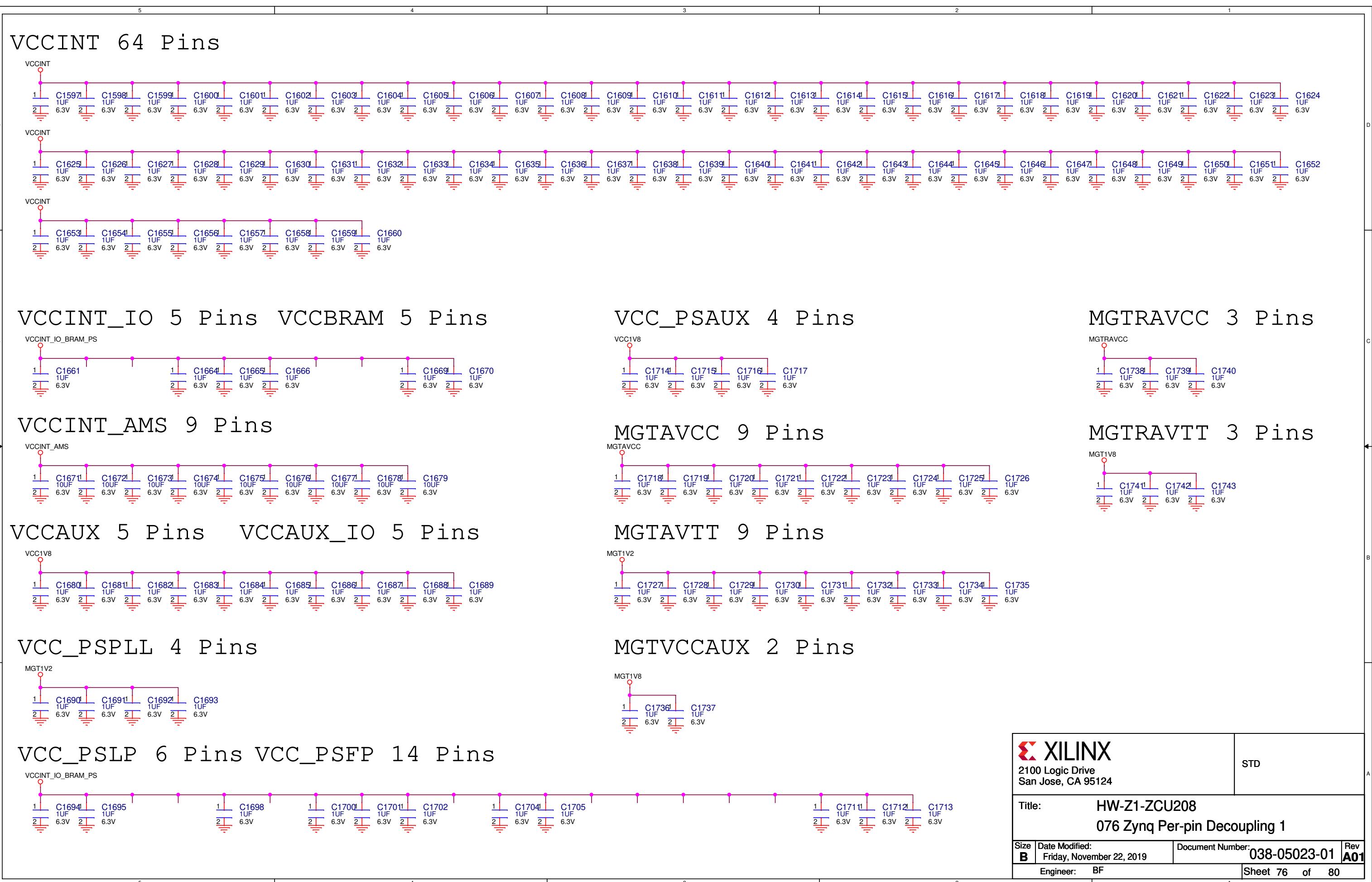
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5 4 3 2 1

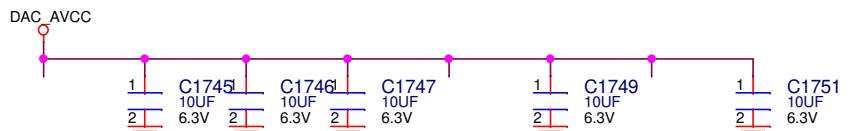




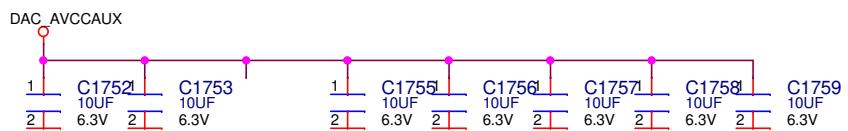




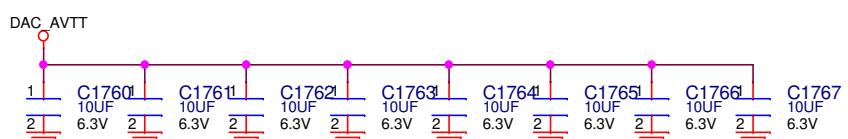
DAC_AVCC 8 Pins



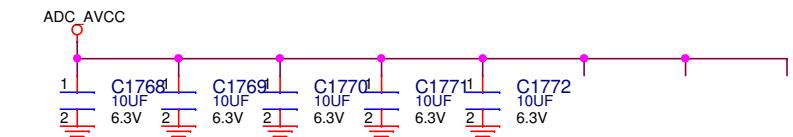
DAC_AVCCAUX 8 Pins



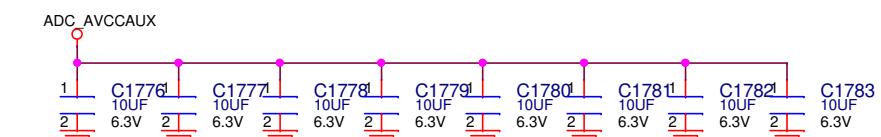
DAC_AVCCTT 8 Pins



ADC_AVCC 8 Pins



ADC_AVCCAUX 8 Pins

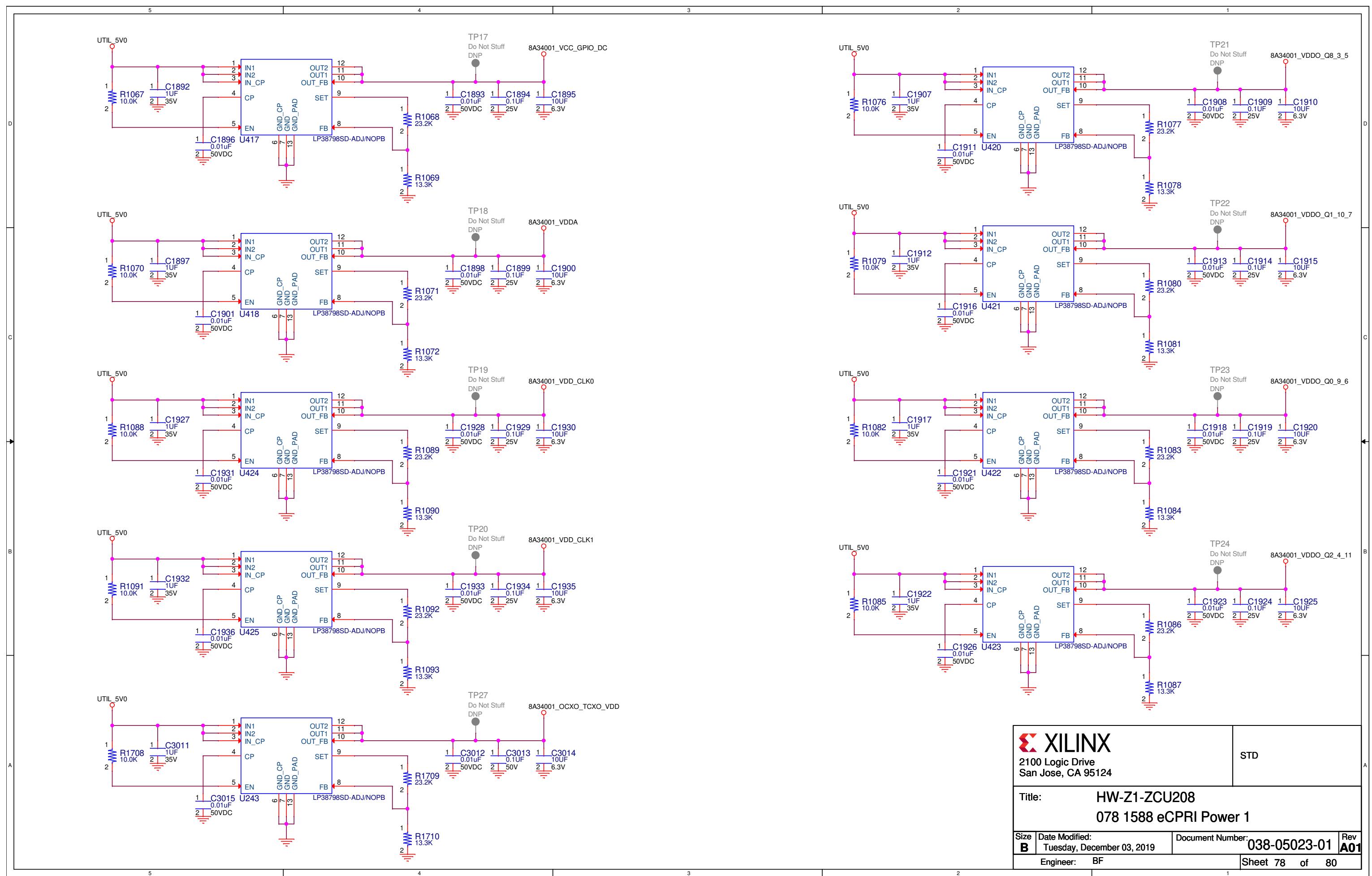


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077 Zynq Per-pin Decoupling 2

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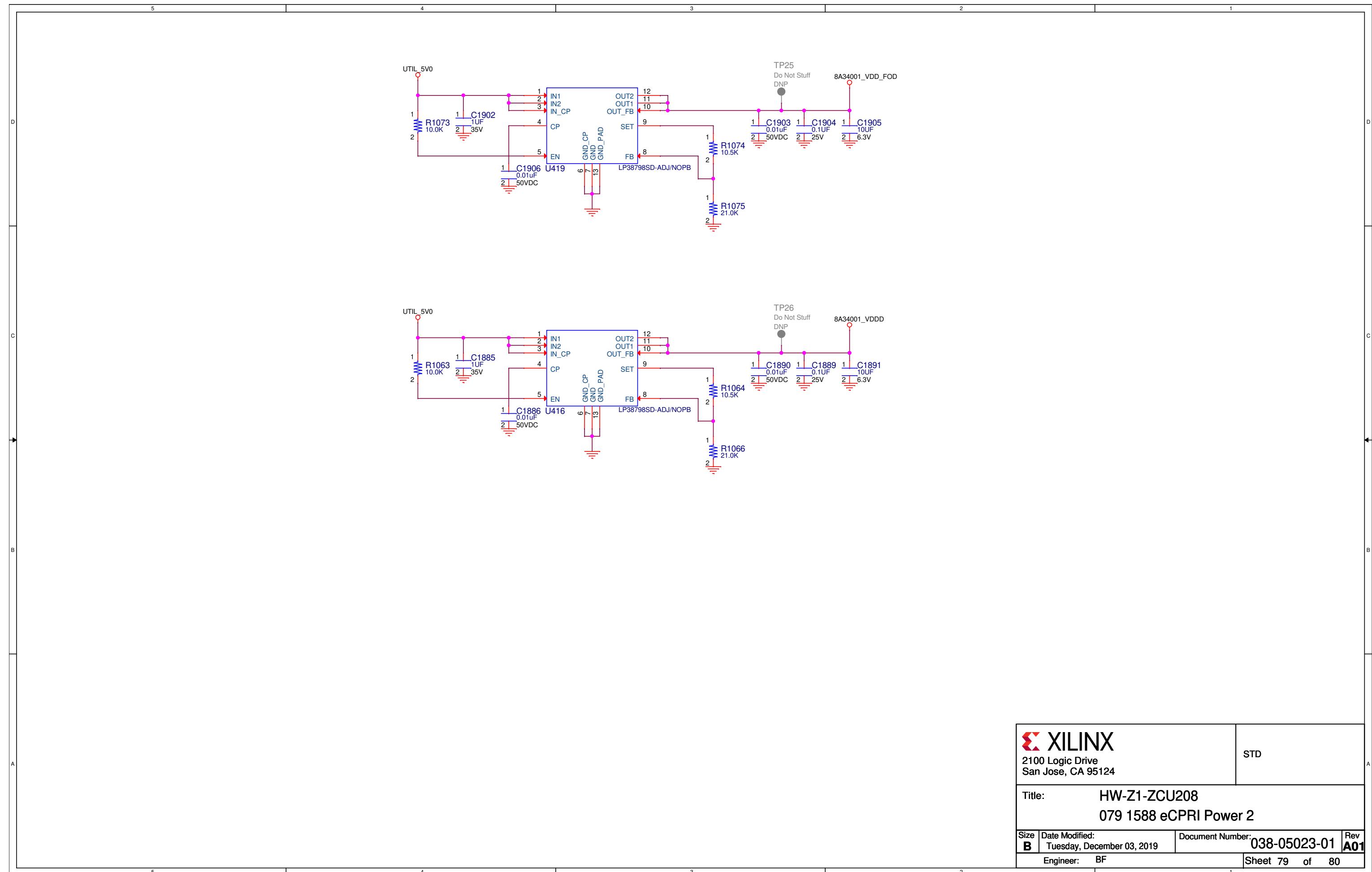
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Title: HW-Z1-ZCU208

078 1588 eCPRI Power 1

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XILINX 2100 Logic Drive San Jose, CA 95124		STD
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