VC707 Test Pattern Generator Flow

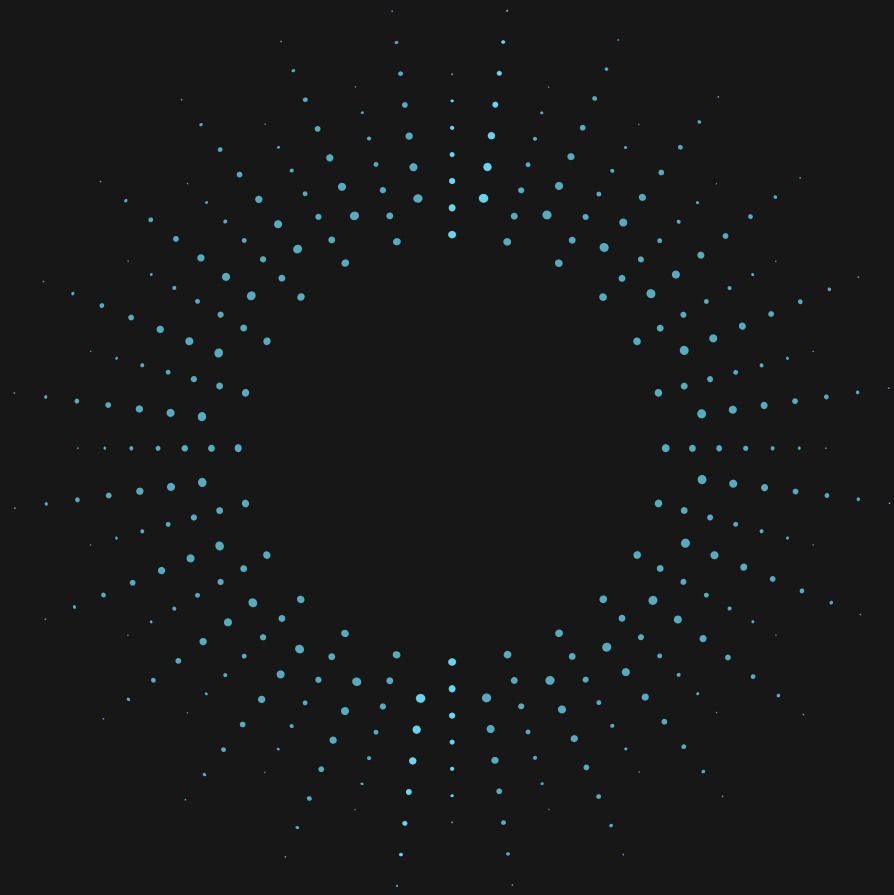
Field Application Engineer
Adaptive and Embedded Computing Group (AECG)

AMD
together we advance_

Revision History

Date	Version	Description
10/25/23	1.1	Fix block design bug on page 4, .24, 25 and add new problem on page 40.
10/24/23	1.0	Initial version for flow introduction.

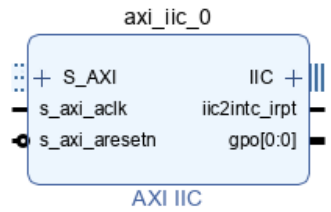
Vivado 2021.1 Part

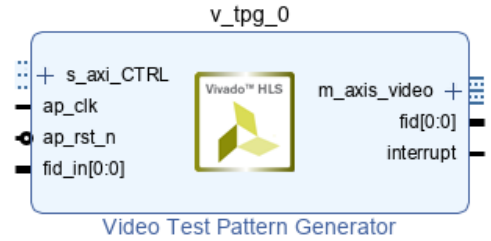


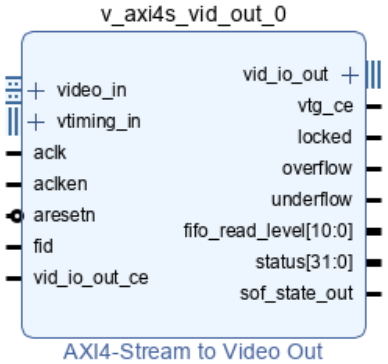
VC707 Test Pattern Generator Flow

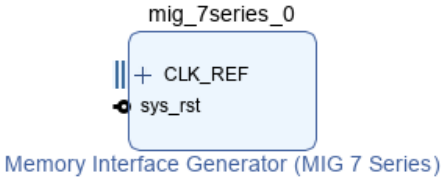
Block Design Steps

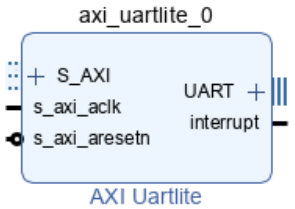
先召喚出這幾個 IP

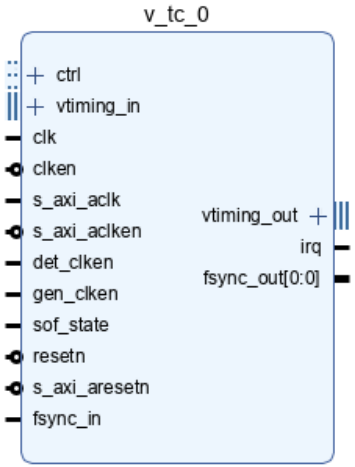


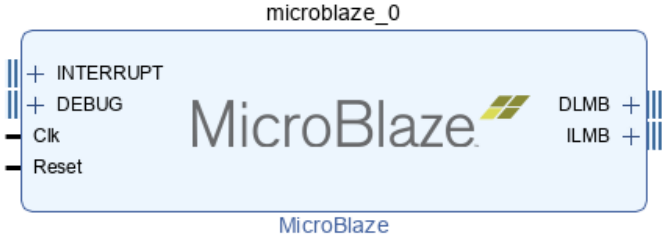




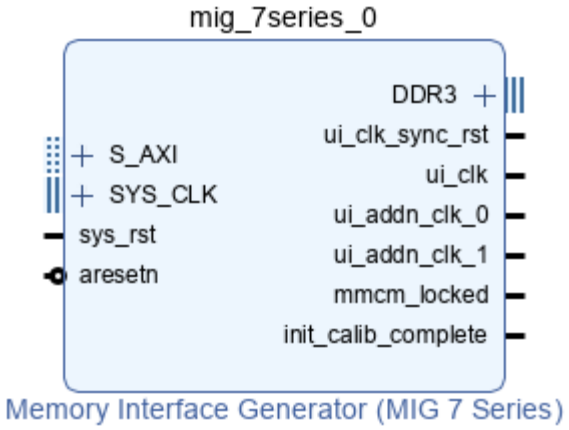




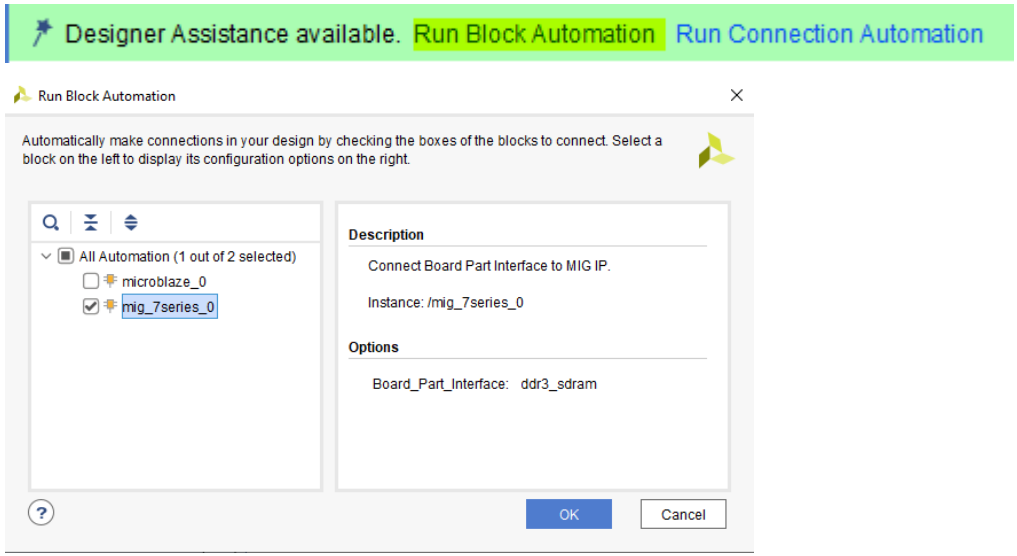




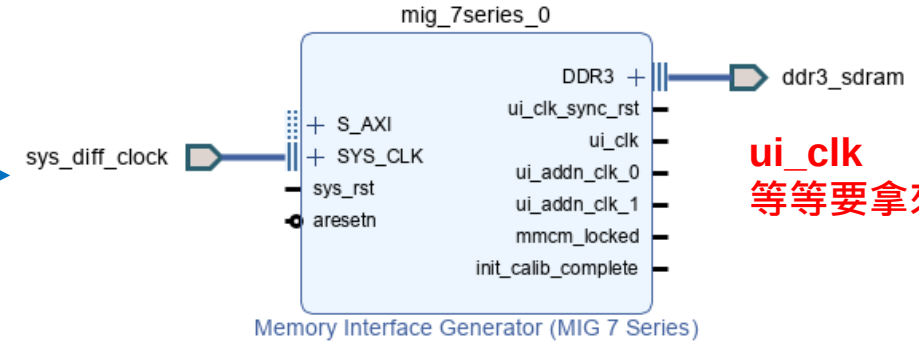
VC707 Test Pattern Generator Flow – MIG 7 Series



DDR3，影像緩存用
點選 Block Automation

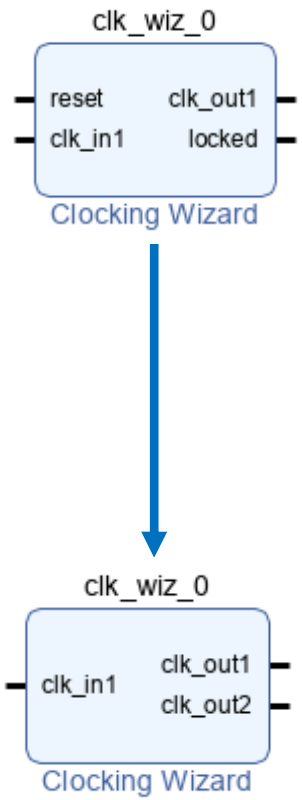


Run 完 IP 會有介面上的改變

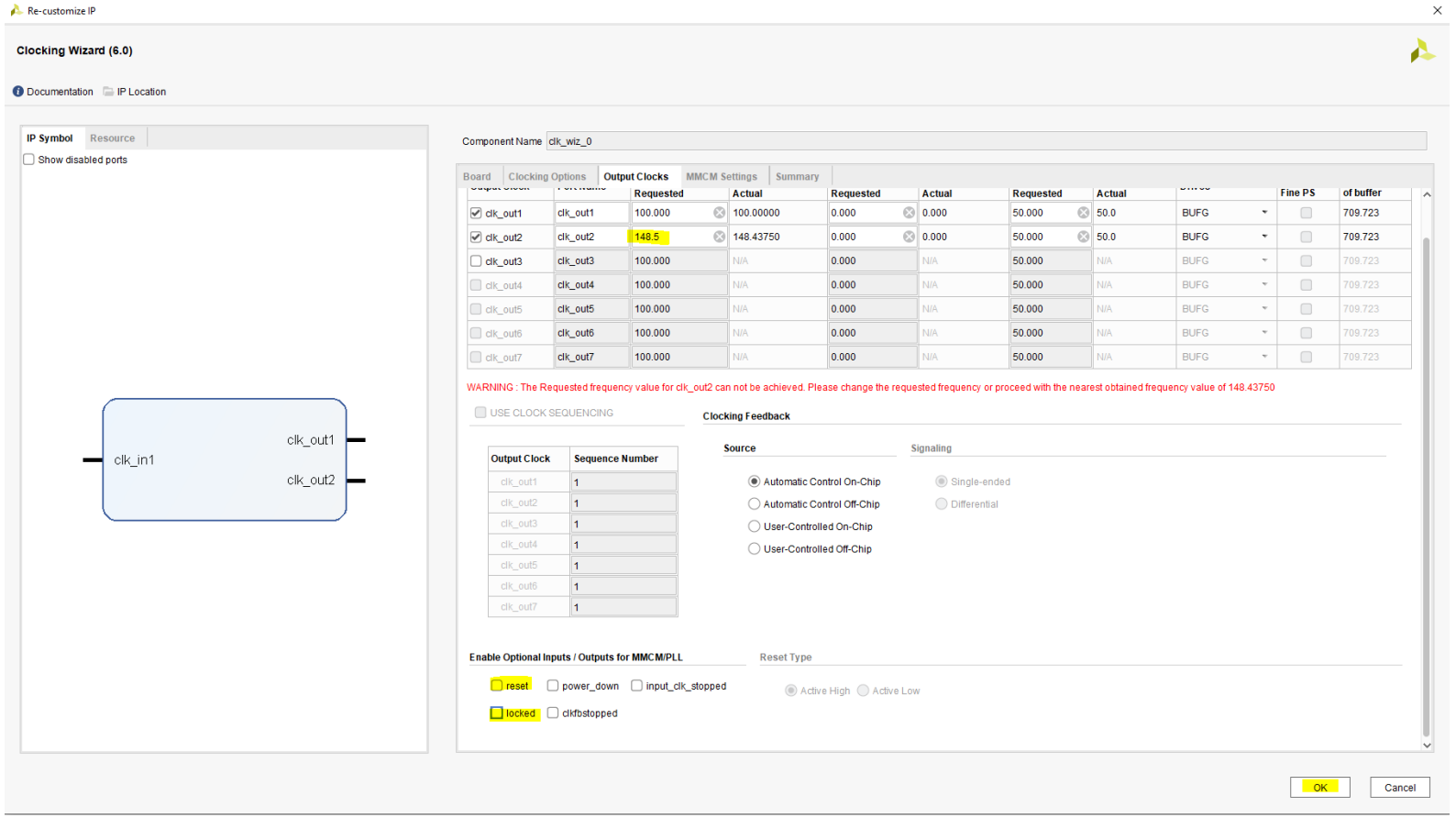


ui_clk
等等要拿來接 clocking wizard 的 input

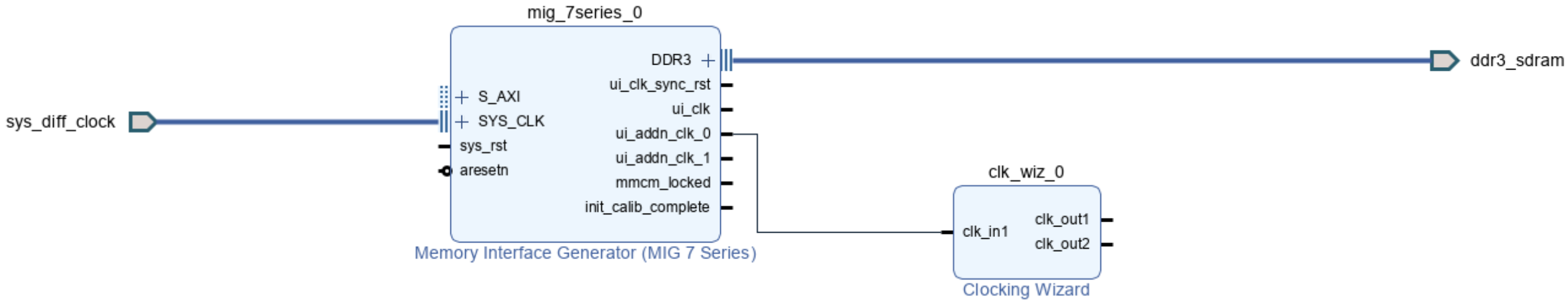
VC707 Test Pattern Generator Flow – clocking wizard



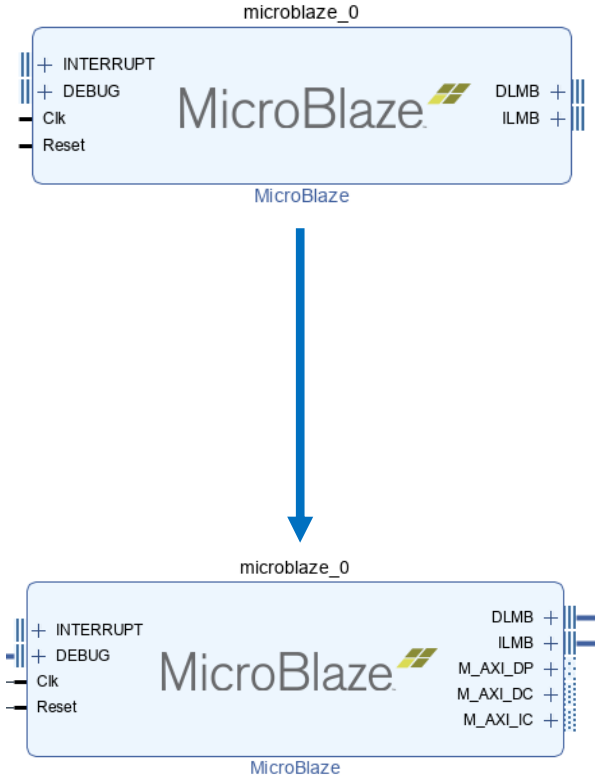
會分出兩個 clock 分別是 100MHz 和 148.5MHz
100MHz 給 Microblaze 吃，148.5MHz 給解析度 1080P 吃



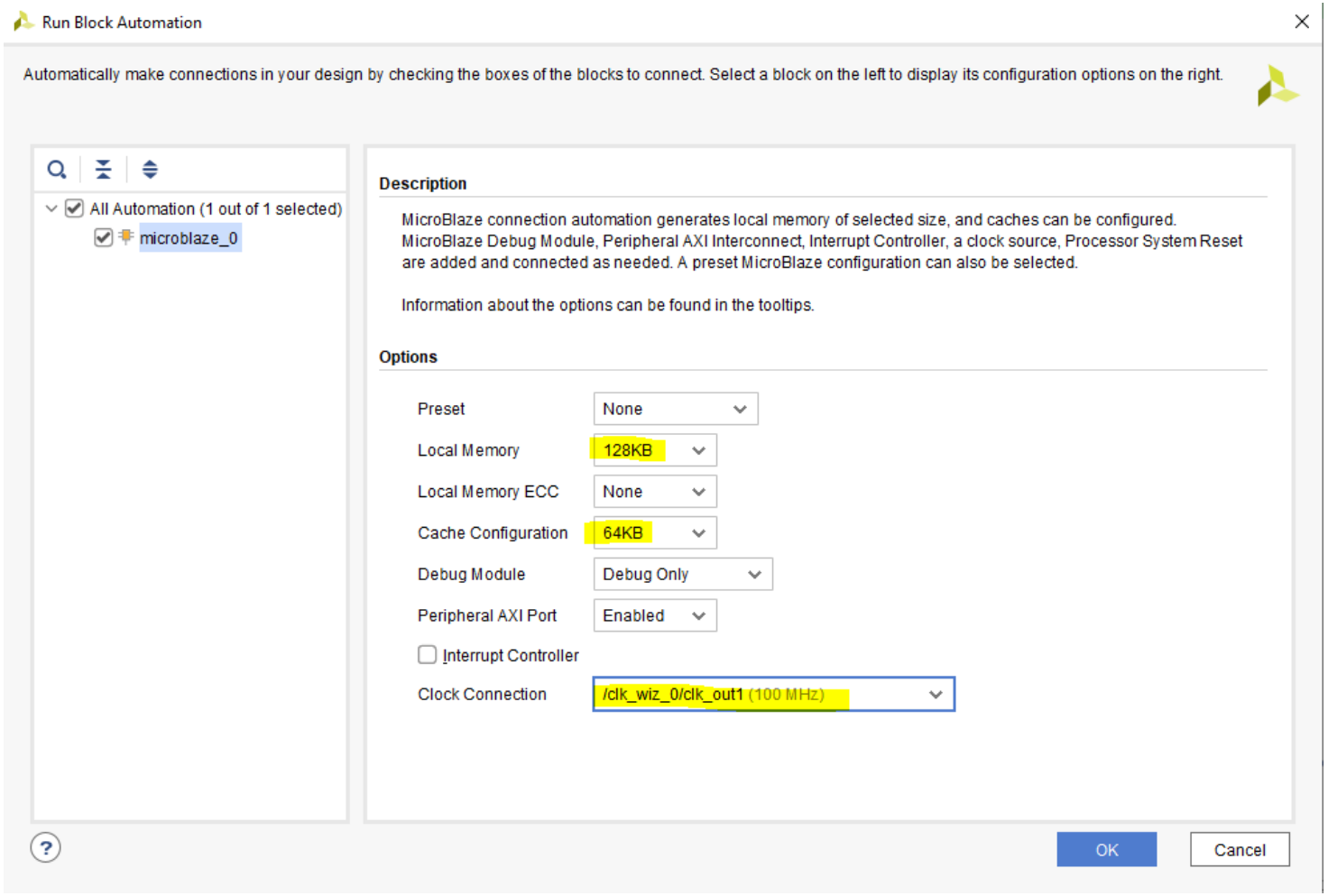
VC707 Test Pattern Generator Flow



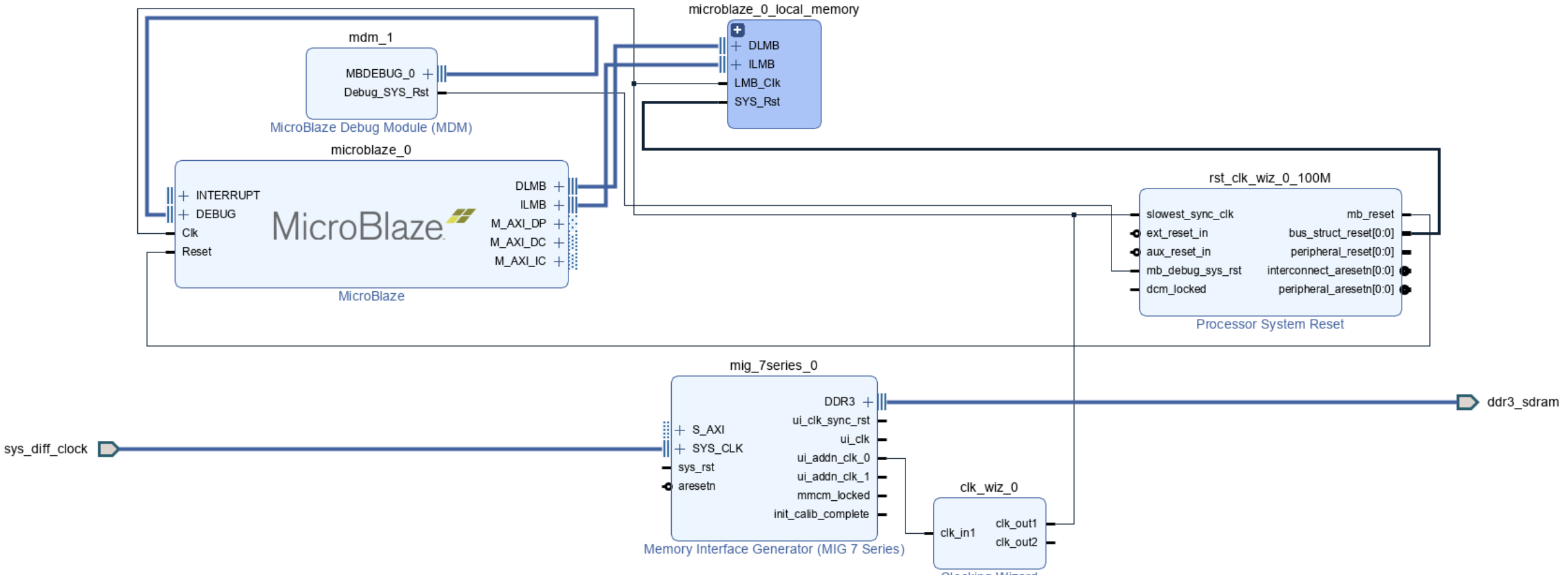
VC707 Test Pattern Generator Flow – Microblaze



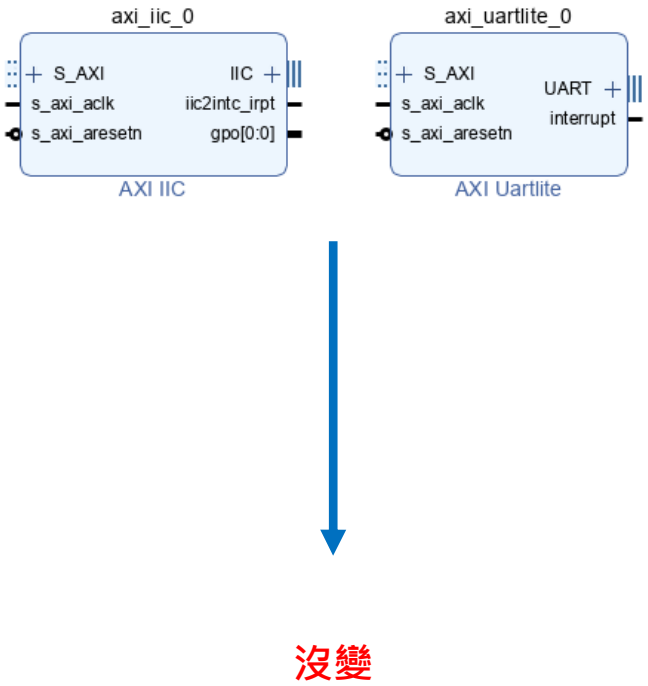
點選 Block Automation



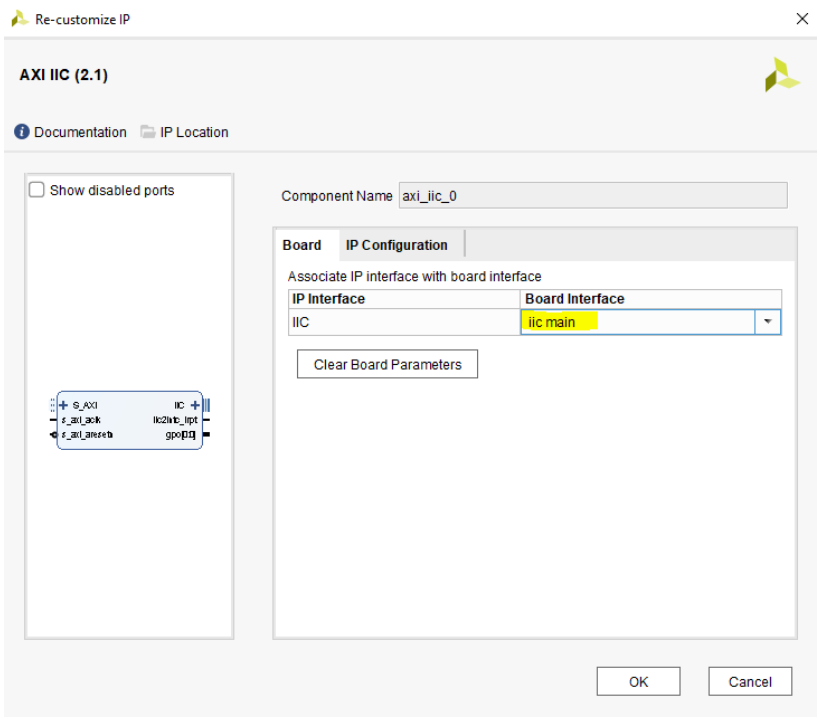
VC707 Test Pattern Generator Flow

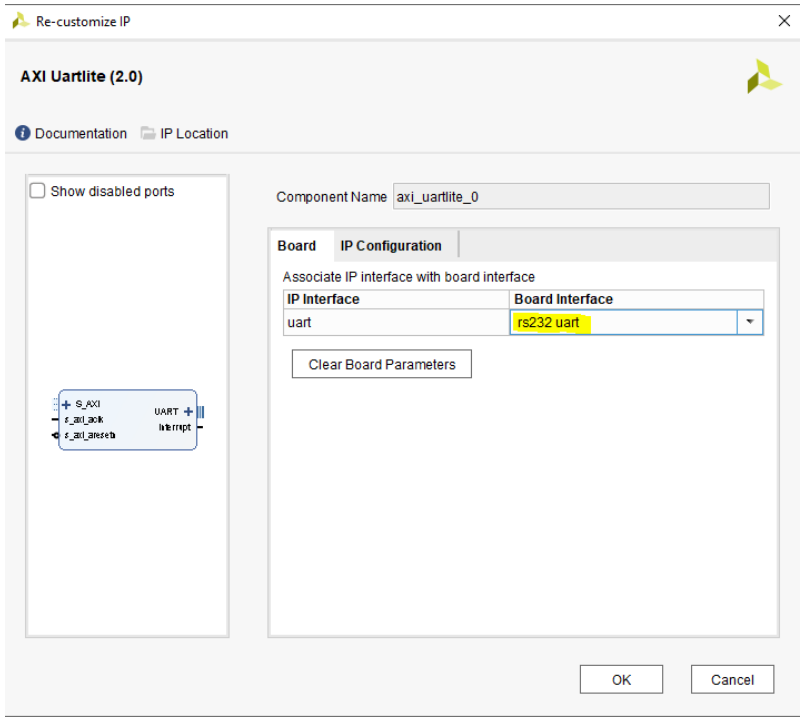


VC707 Test Pattern Generator Flow – UART & IIC

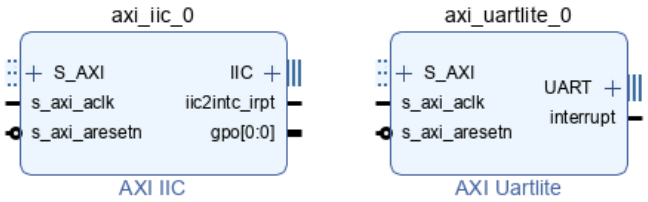


雙擊 IP 進行設定

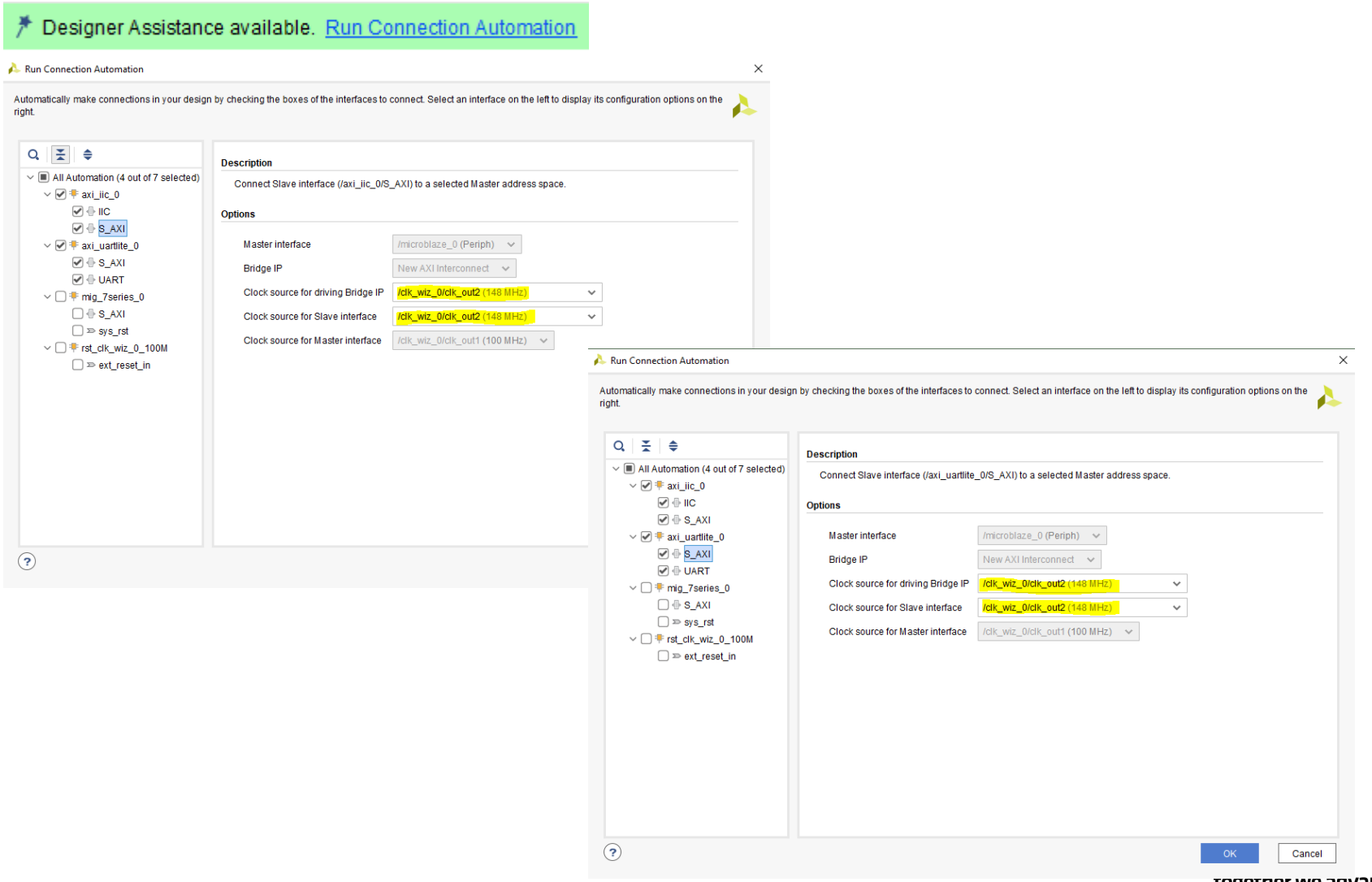




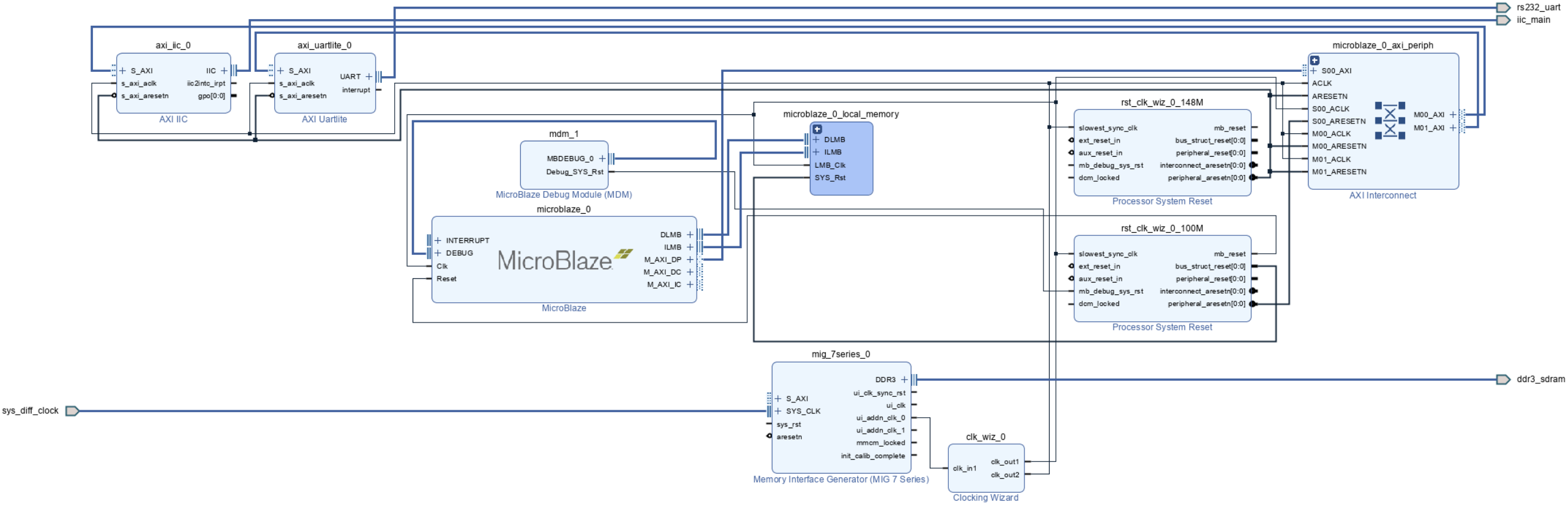
VC707 Test Pattern Generator Flow – UART & IIC



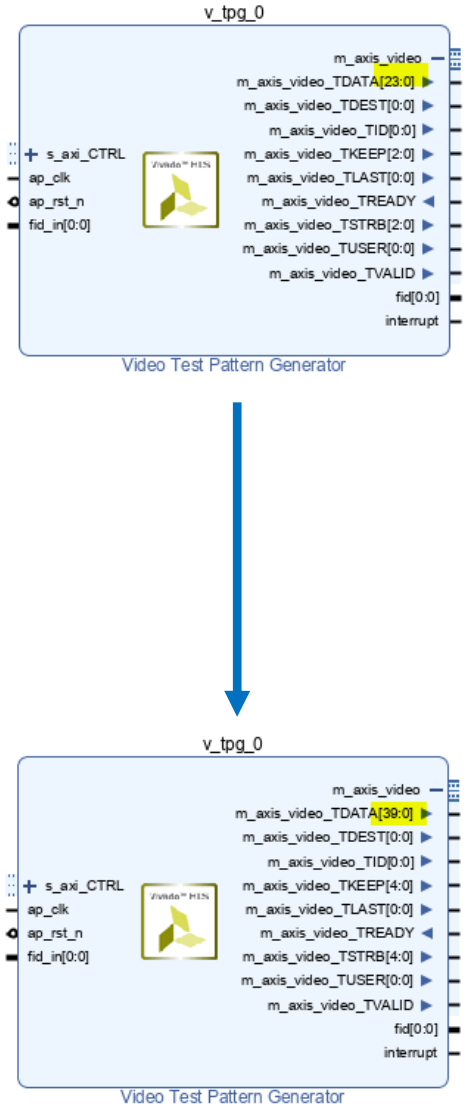
沒變



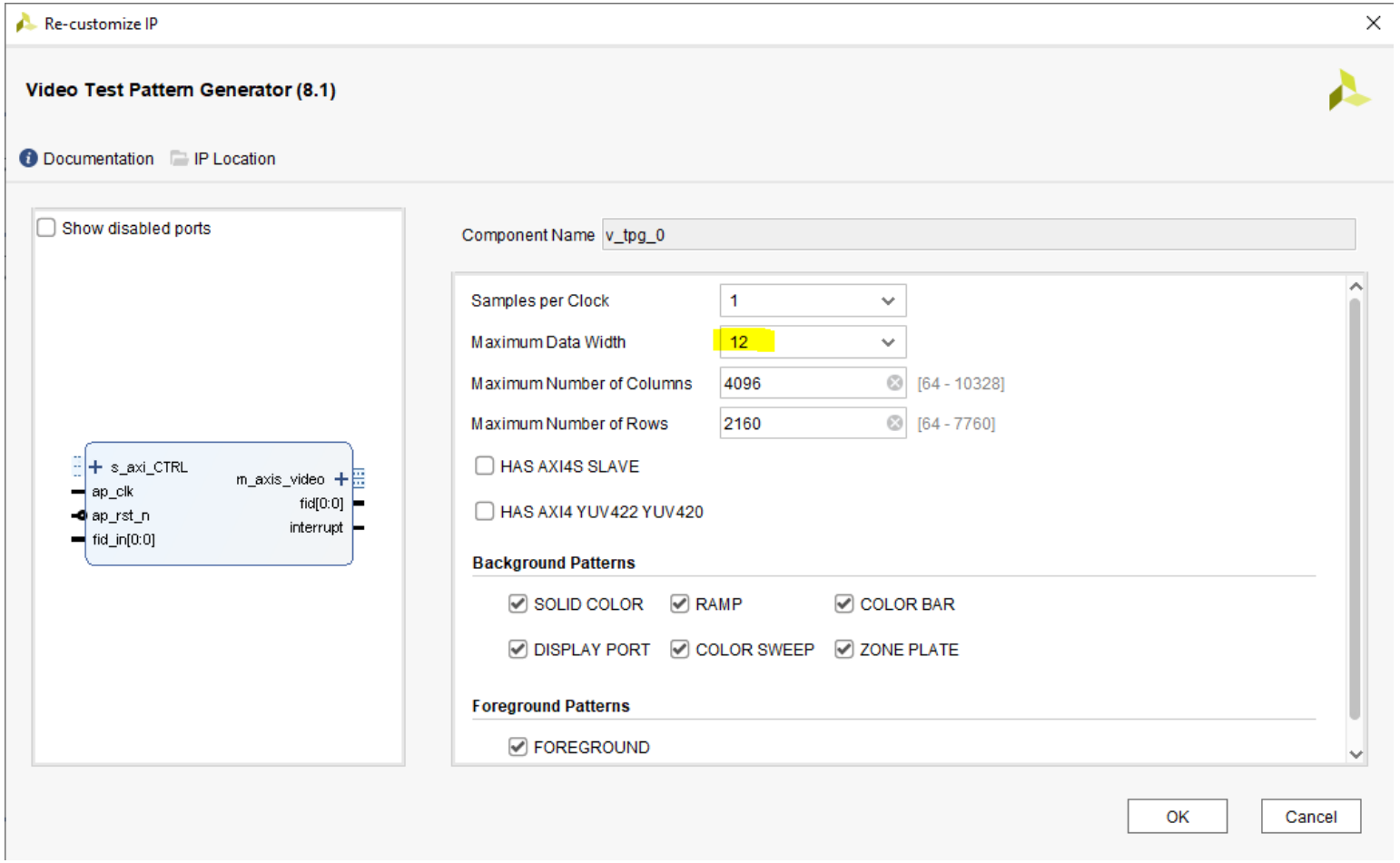
VC707 Test Pattern Generator Flow



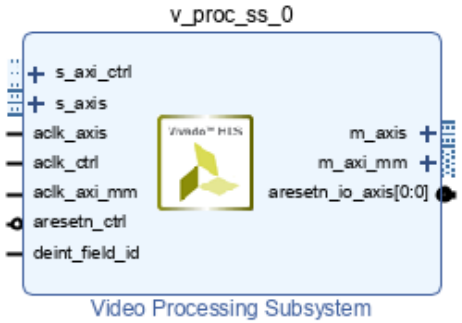
VC707 Test Pattern Generator Flow – Test Pattern Generator

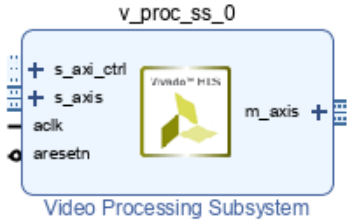


雙擊 IP 進行設定

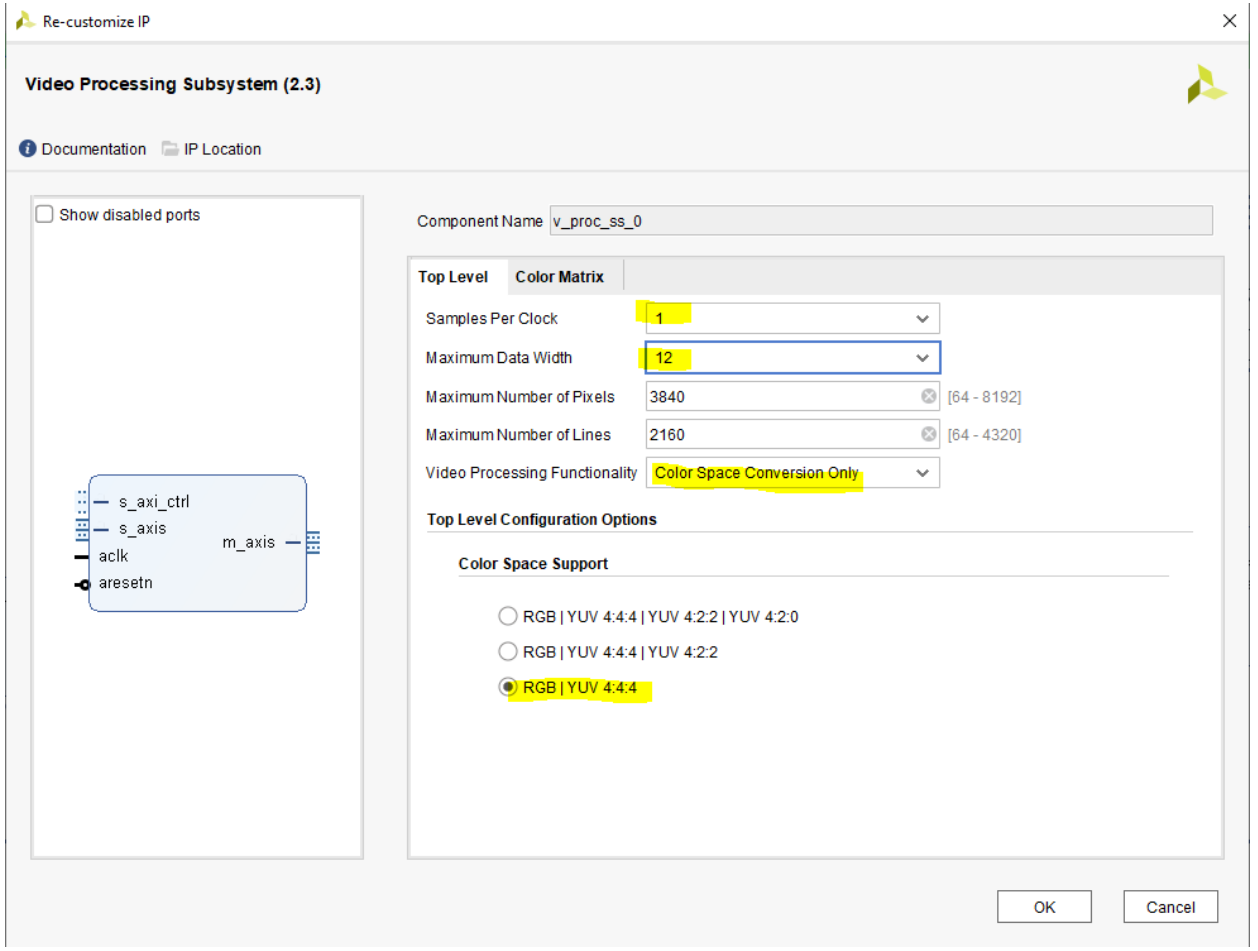


VC707 Test Pattern Generator Flow – Video Processing Subsystem

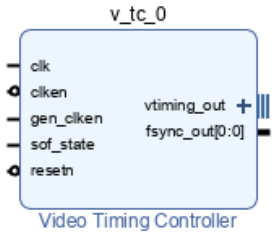




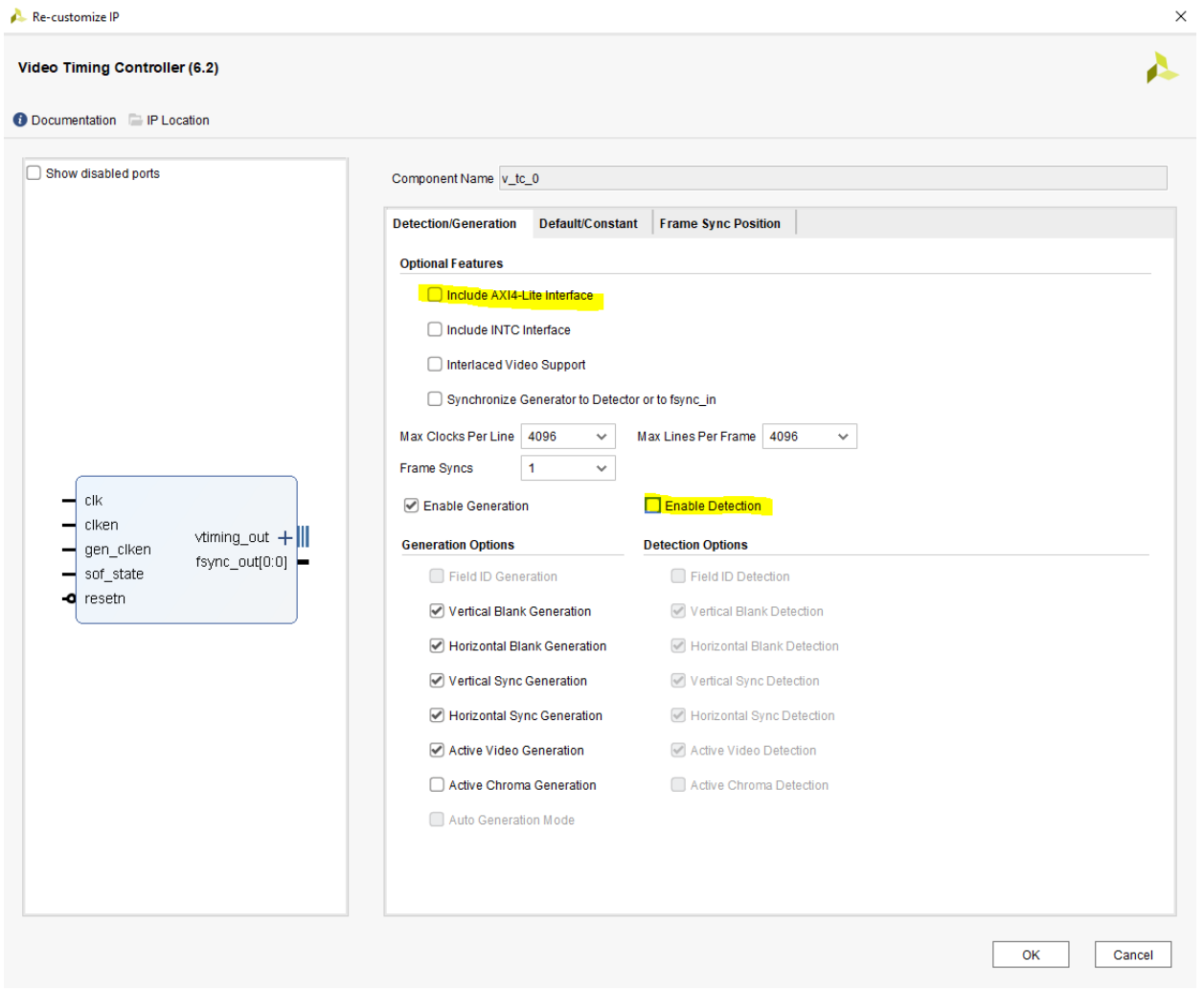
雙擊 IP 進行設定



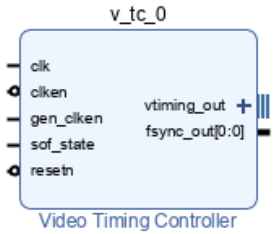
VC707 Test Pattern Generator Flow – Video Timing Controller



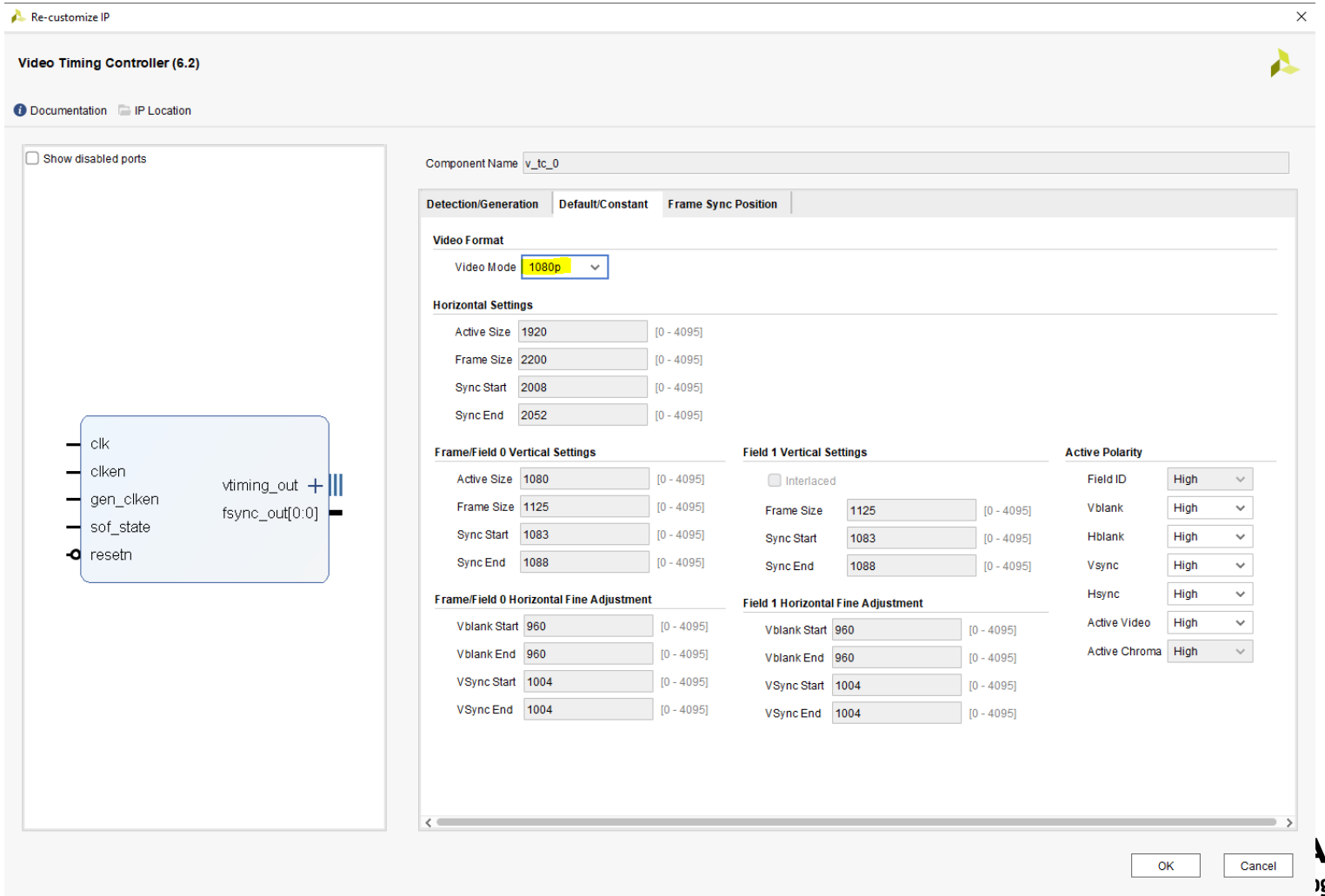
雙擊 IP 進行設定



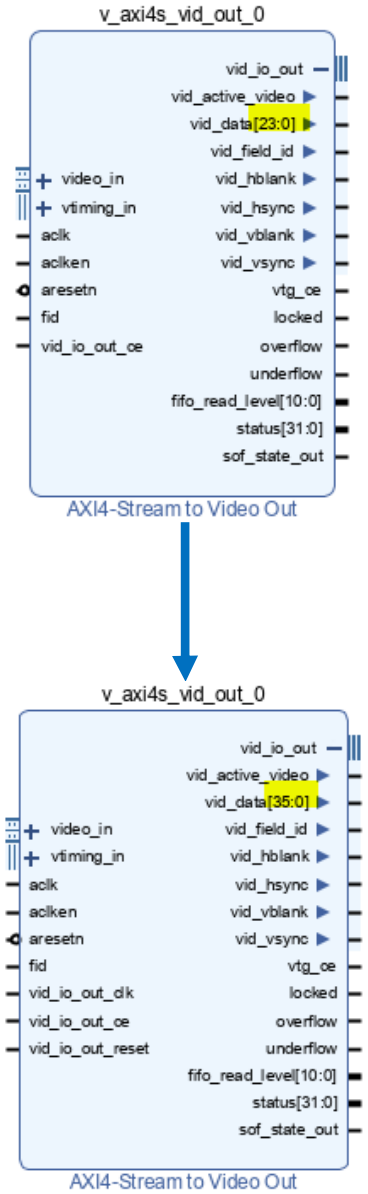
VC707 Test Pattern Generator Flow – Video Timing Controller



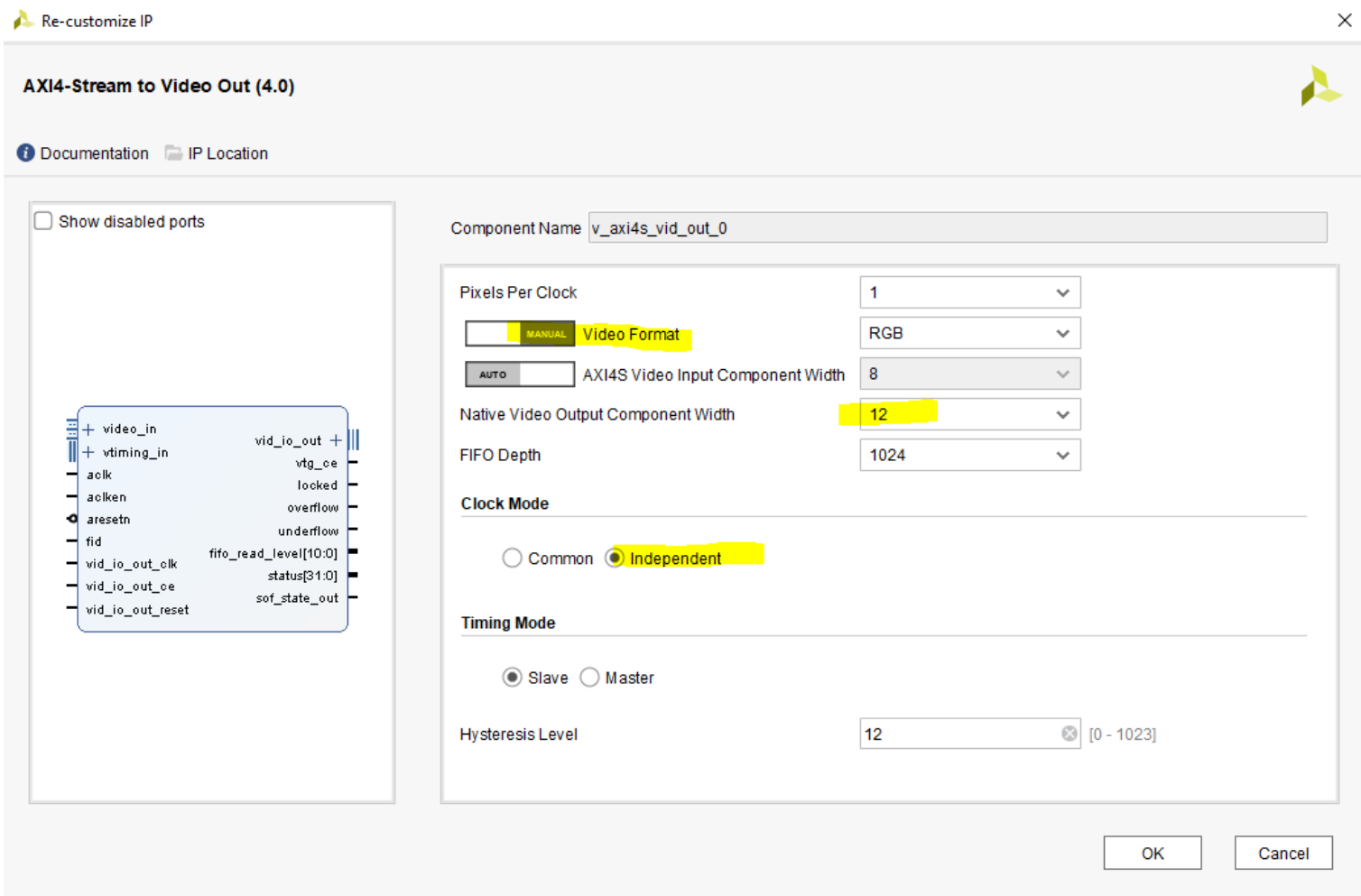
雙擊 IP 進行設定



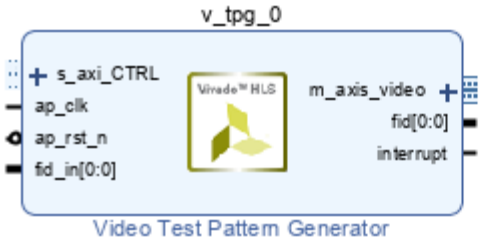
VC707 Test Pattern Generator Flow – AXI4-Stream to Video Out

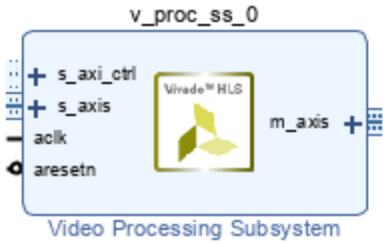


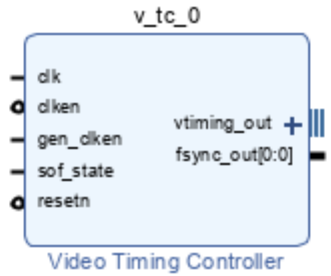
雙擊 IP 進行設定

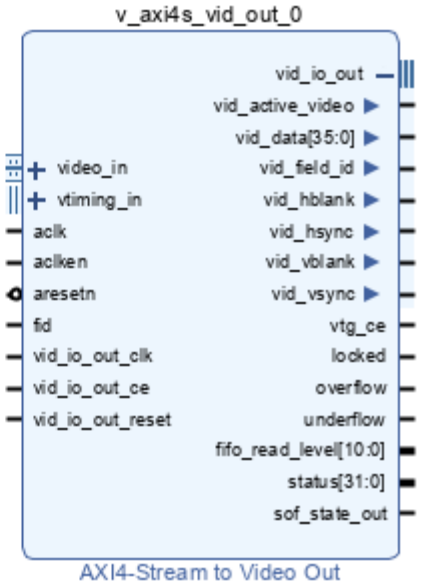


VC707 Test Pattern Generator Flow

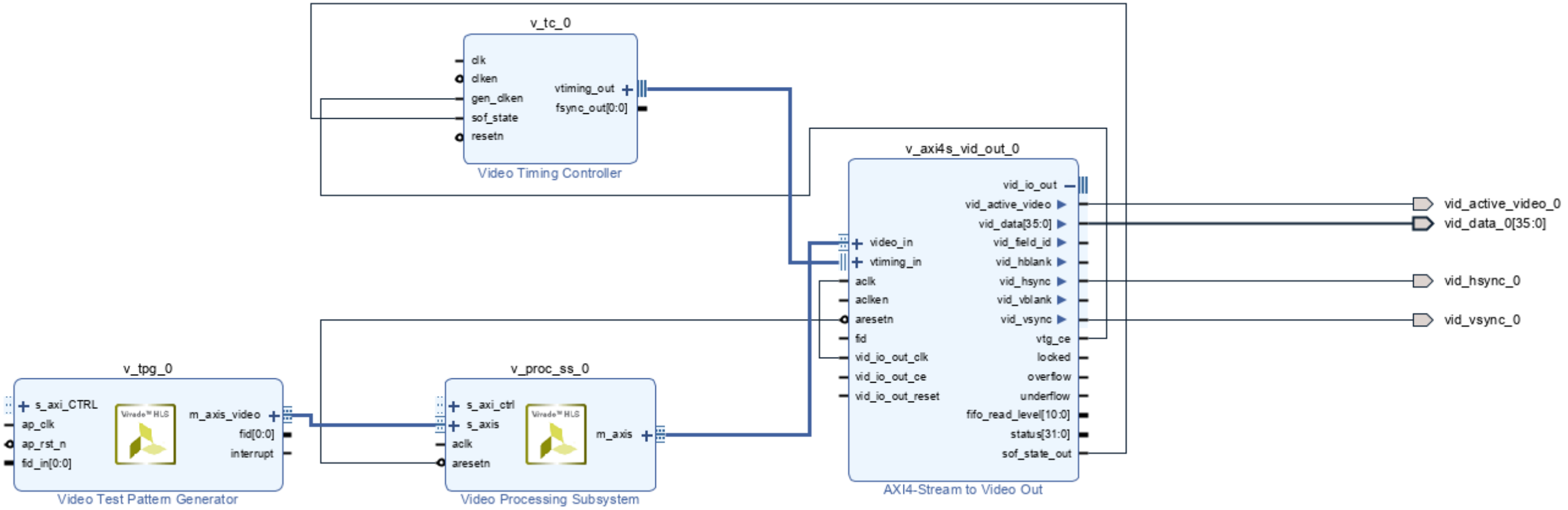




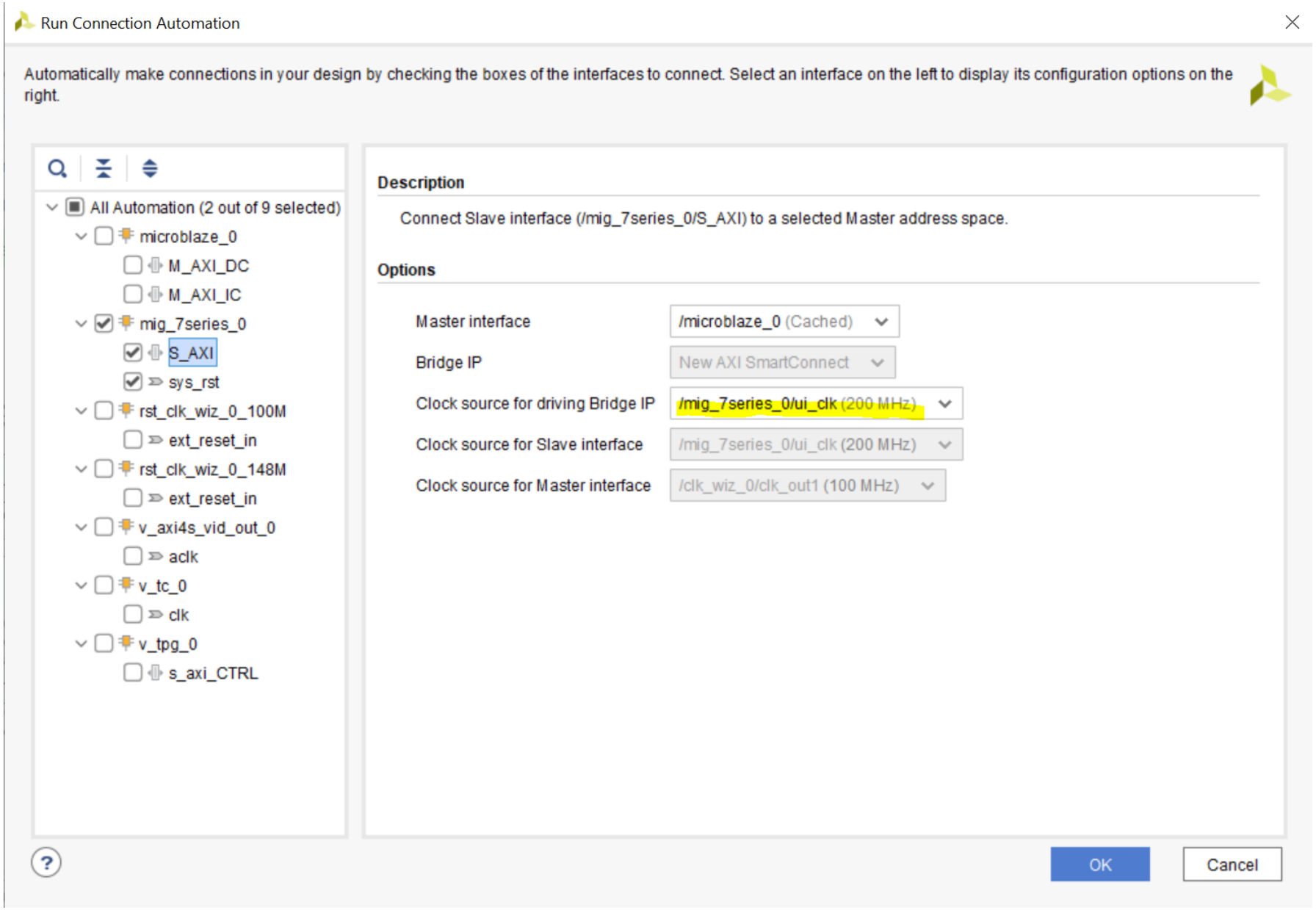




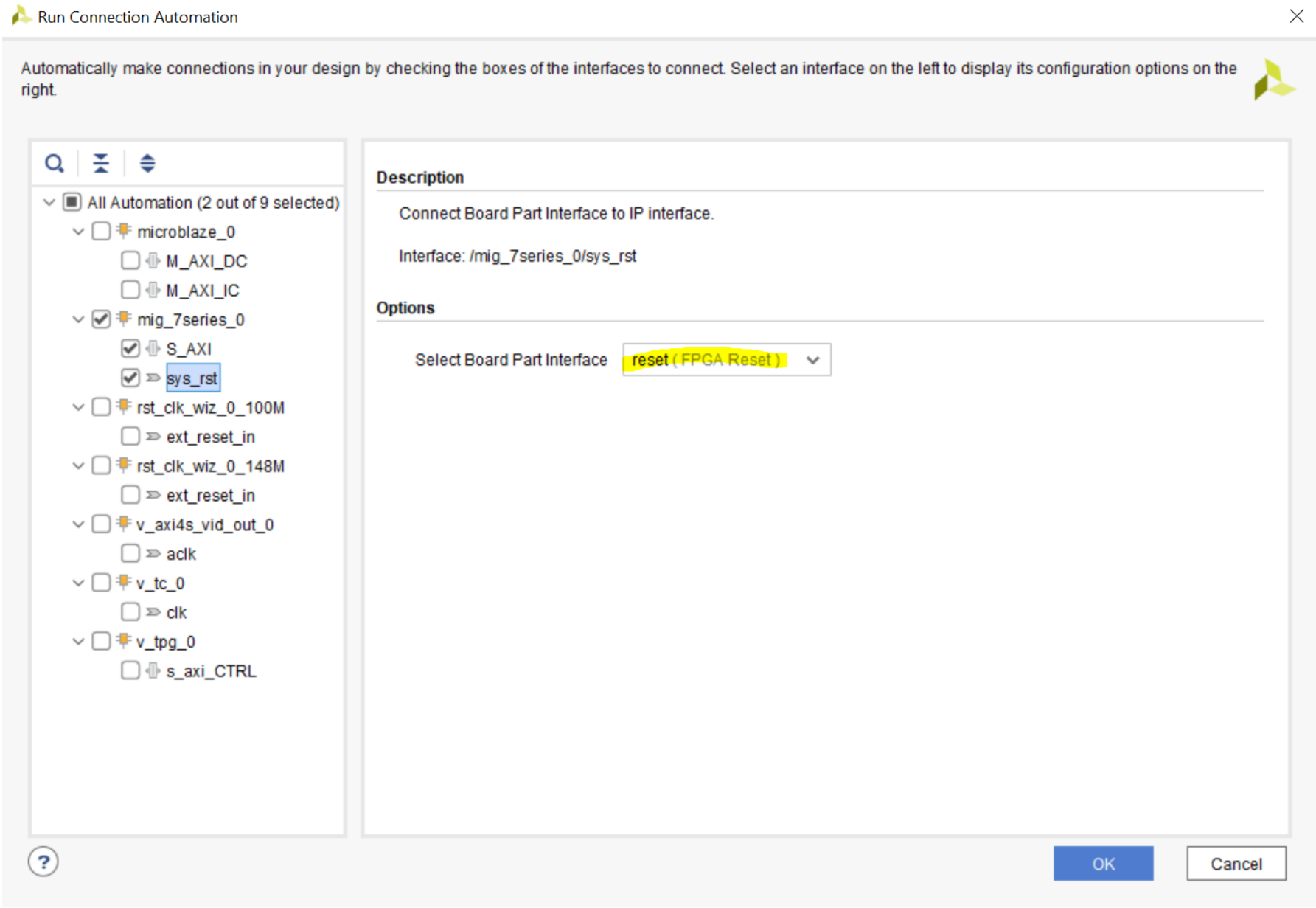
VC707 Test Pattern Generator Flow



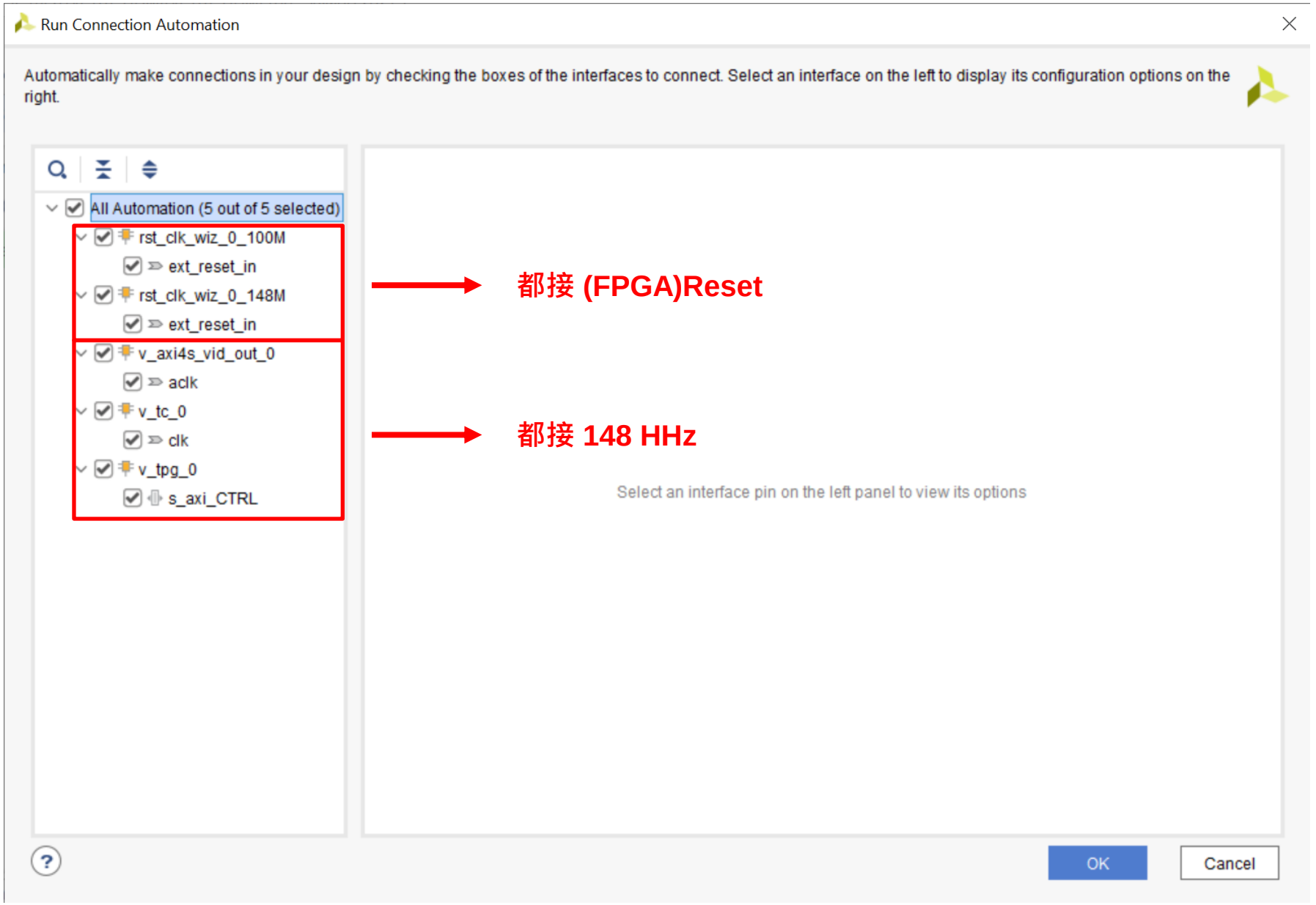
VC707 Test Pattern Generator Flow



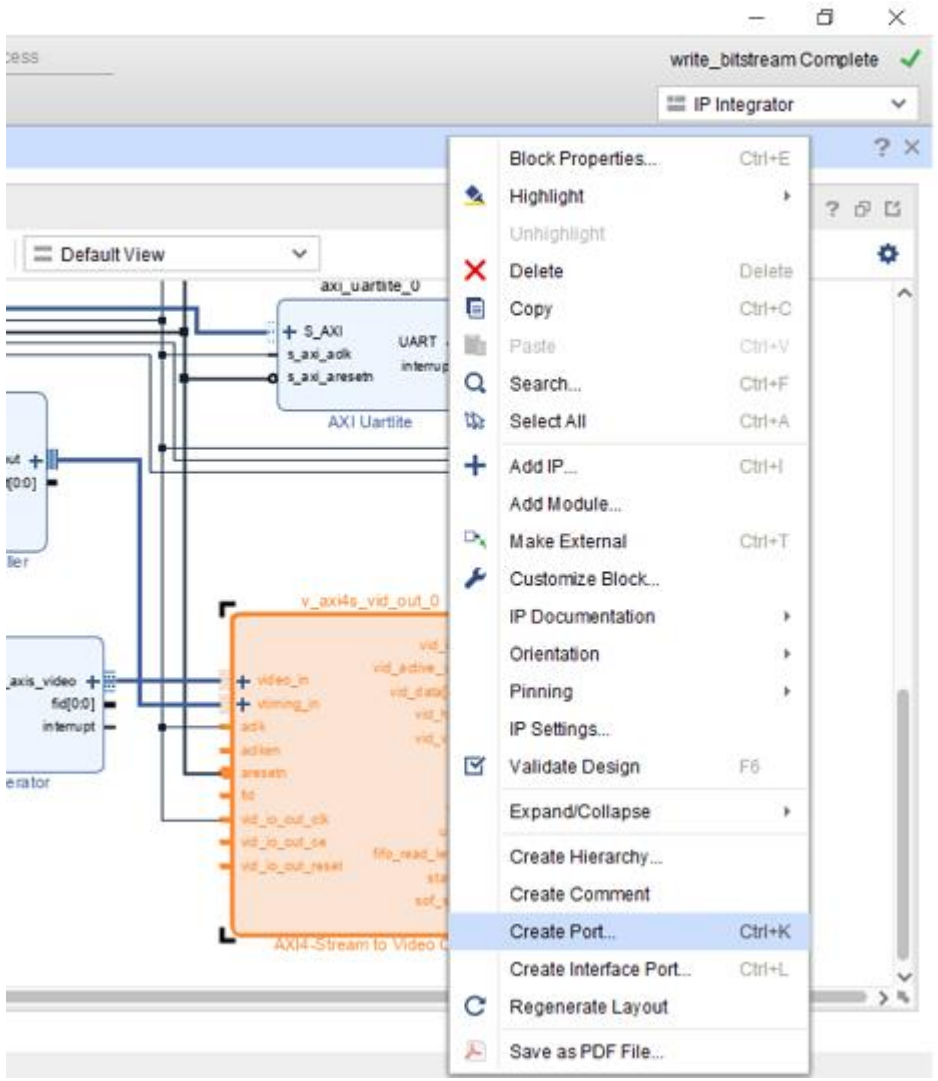
VC707 Test Pattern Generator Flow



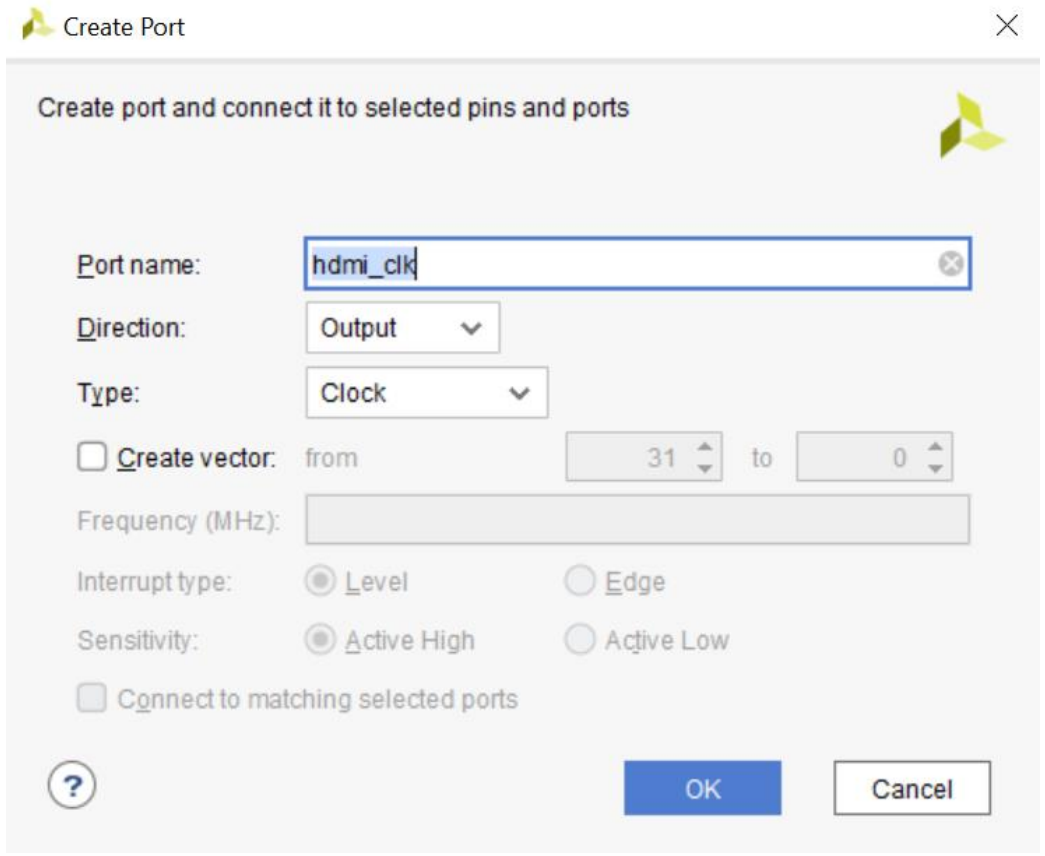
VC707 Test Pattern Generator Flow



VC707 Test Pattern Generator Flow

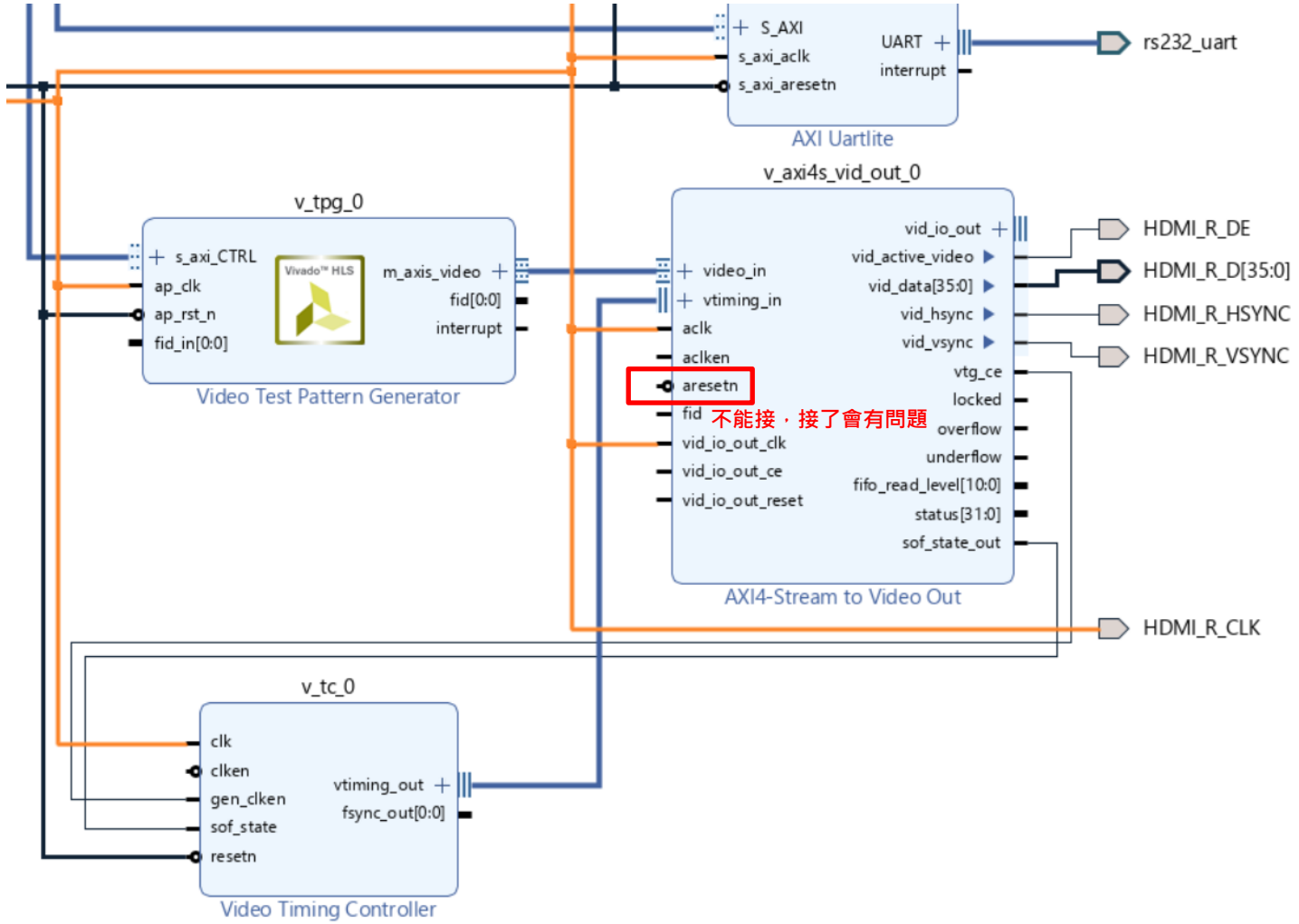


在 AXI4-Stream to Video Out 右鍵點選 Create Port 並輸入下圖資訊：



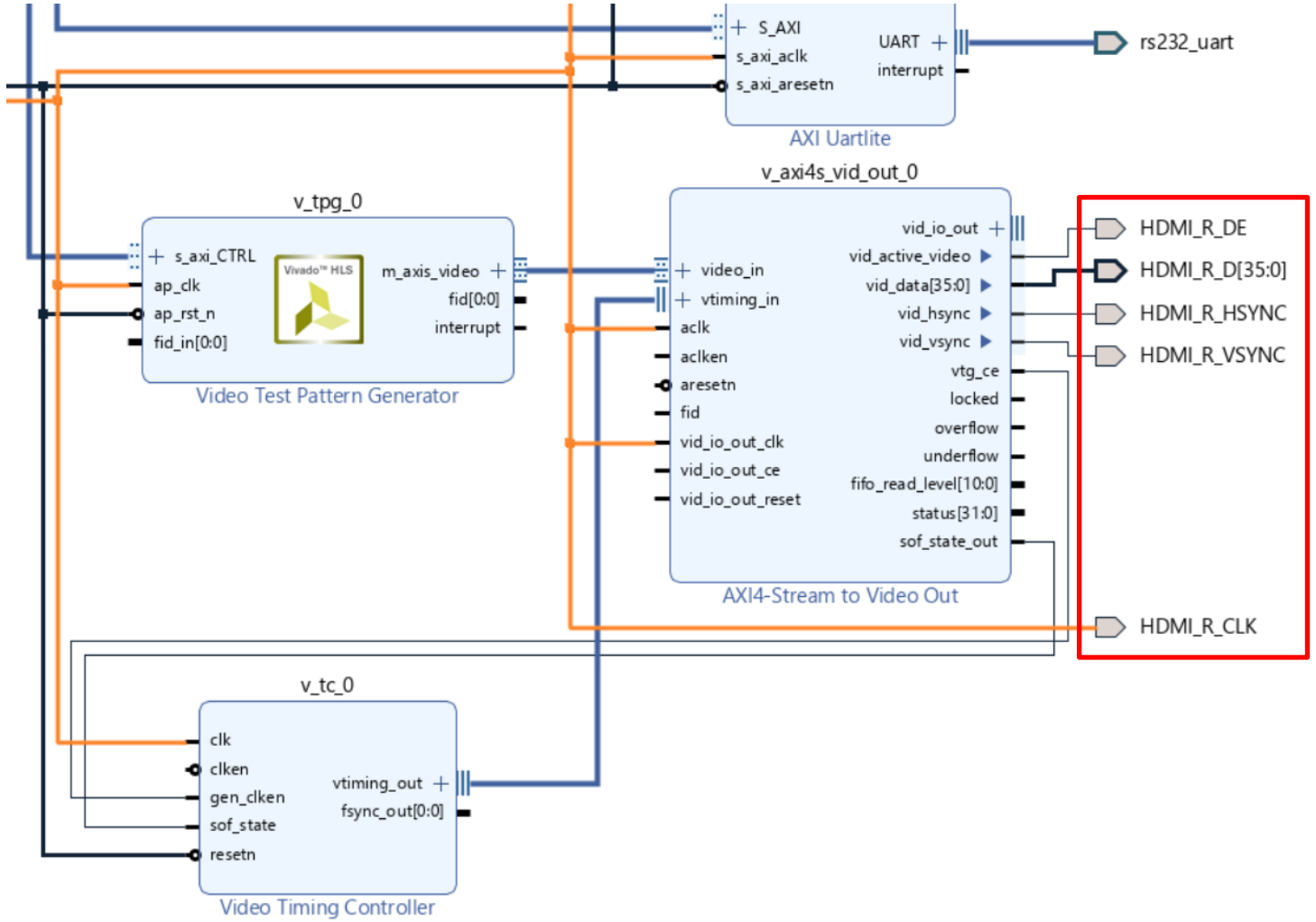
VC707 Test Pattern Generator Flow

連接 HDMI Clk 到 VTC clk



VC707 Test Pattern Generator Flow

撰寫 HDMI XDC，可以在以下網址找到寫好的作參考
VC707 XDC Constraints File: Sorted · GitHub
記得改成相對應的名字



VC707 Test Pattern Generator Flow

撰寫 HDMI XDC，可以在以下網址找到寫好的作參考

VC707 XDC Constraints File: Sorted · GitHub

記得改成相對應的名字，自己複製對照

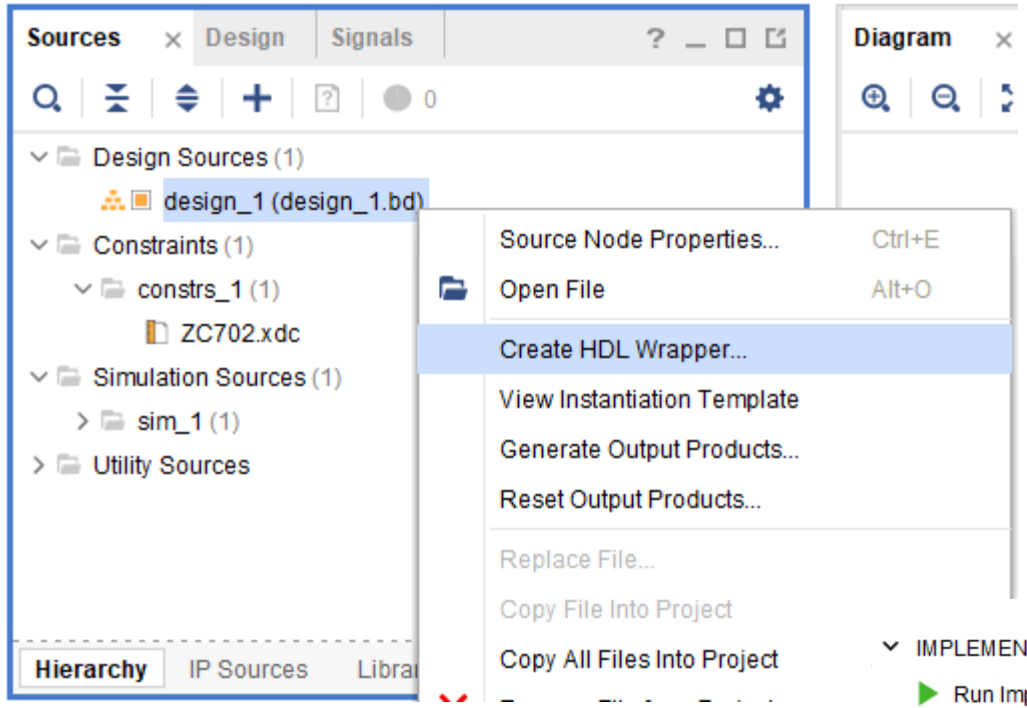
```
set_property PACKAGE_PIN AM22 [get_ports HDMI_R_D[0]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[0]]
set_property PACKAGE_PIN AL22 [get_ports HDMI_R_D[1]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[1]]
set_property PACKAGE_PIN AJ20 [get_ports HDMI_R_D[2]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[2]]
set_property PACKAGE_PIN AJ21 [get_ports HDMI_R_D[3]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[3]]
set_property PACKAGE_PIN AM21 [get_ports HDMI_R_D[4]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[4]]
set_property PACKAGE_PIN AL21 [get_ports HDMI_R_D[5]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[5]]
set_property PACKAGE_PIN AK22 [get_ports HDMI_R_D[6]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[6]]
set_property PACKAGE_PIN AJ22 [get_ports HDMI_R_D[7]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[7]]
set_property PACKAGE_PIN AL20 [get_ports HDMI_R_D[8]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[8]]
set_property PACKAGE_PIN AK20 [get_ports HDMI_R_D[9]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[9]]
set_property PACKAGE_PIN AK23 [get_ports HDMI_R_D[10]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[10]]
set_property PACKAGE_PIN AJ23 [get_ports HDMI_R_D[11]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[11]]
set_property PACKAGE_PIN AN21 [get_ports HDMI_R_D[12]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[12]]
set_property PACKAGE_PIN AP22 [get_ports HDMI_R_D[13]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[13]]
set_property PACKAGE_PIN AP23 [get_ports HDMI_R_D[14]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[14]]
set_property PACKAGE_PIN AN23 [get_ports HDMI_R_D[15]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[15]]
set_property PACKAGE_PIN AM23 [get_ports HDMI_R_D[16]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[16]]
set_property PACKAGE_PIN AN24 [get_ports HDMI_R_D[17]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[17]]
set_property PACKAGE_PIN AY24 [get_ports HDMI_R_D[18]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[18]]
set_property PACKAGE_PIN BB22 [get_ports HDMI_R_D[19]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[19]]
set_property PACKAGE_PIN BA22 [get_ports HDMI_R_D[20]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[20]]
set_property PACKAGE_PIN BA25 [get_ports HDMI_R_D[21]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[21]]
set_property PACKAGE_PIN AY25 [get_ports HDMI_R_D[22]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[22]]
set_property PACKAGE_PIN AY22 [get_ports HDMI_R_D[23]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[23]]
```

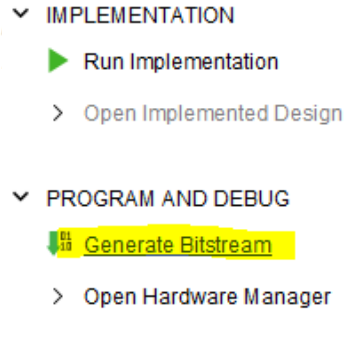
```
set_property PACKAGE_PIN AY23 [get_ports HDMI_R_D[24]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[24]]
set_property PACKAGE_PIN AV24 [get_ports HDMI_R_D[25]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[25]]
set_property PACKAGE_PIN AU24 [get_ports HDMI_R_D[26]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[26]]
set_property PACKAGE_PIN AW21 [get_ports HDMI_R_D[27]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[27]]
set_property PACKAGE_PIN AV21 [get_ports HDMI_R_D[28]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[28]]
set_property PACKAGE_PIN AT24 [get_ports HDMI_R_D[29]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[29]]
set_property PACKAGE_PIN AR24 [get_ports HDMI_R_D[30]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[30]]
set_property PACKAGE_PIN AU21 [get_ports HDMI_R_D[31]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[31]]
set_property PACKAGE_PIN AT21 [get_ports HDMI_R_D[32]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[32]]
set_property PACKAGE_PIN AW22 [get_ports HDMI_R_D[33]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[33]]
set_property PACKAGE_PIN AW23 [get_ports HDMI_R_D[34]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[34]]
set_property PACKAGE_PIN AV23 [get_ports HDMI_R_D[35]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[35]]
```

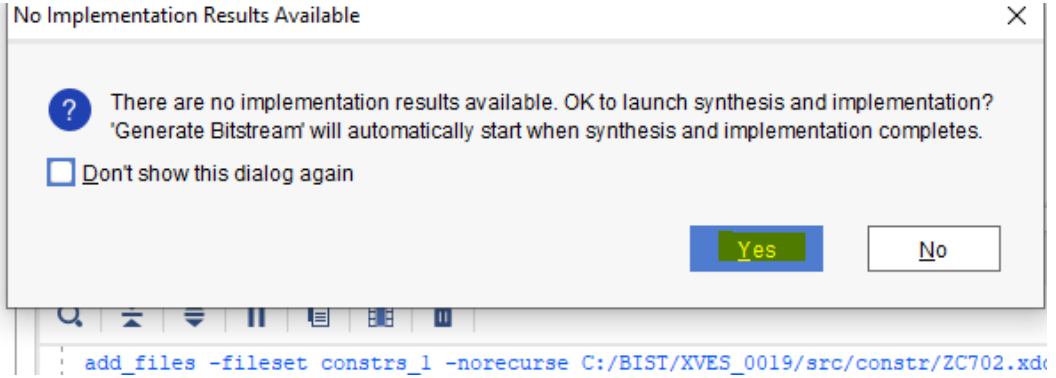
```
set_property PACKAGE_PIN AU23 [get_ports HDMI_R_CLK]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_CLK]
set_property PACKAGE_PIN AP21 [get_ports HDMI_R_DE]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_DE]
set_property PACKAGE_PIN AT22 [get_ports HDMI_R_VSYNC]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_VSYNC]
set_property PACKAGE_PIN AU22 [get_ports HDMI_R_HSYNC]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_HSYNC]
```

VC707 Test Pattern Generator Flow

Block Design Steps

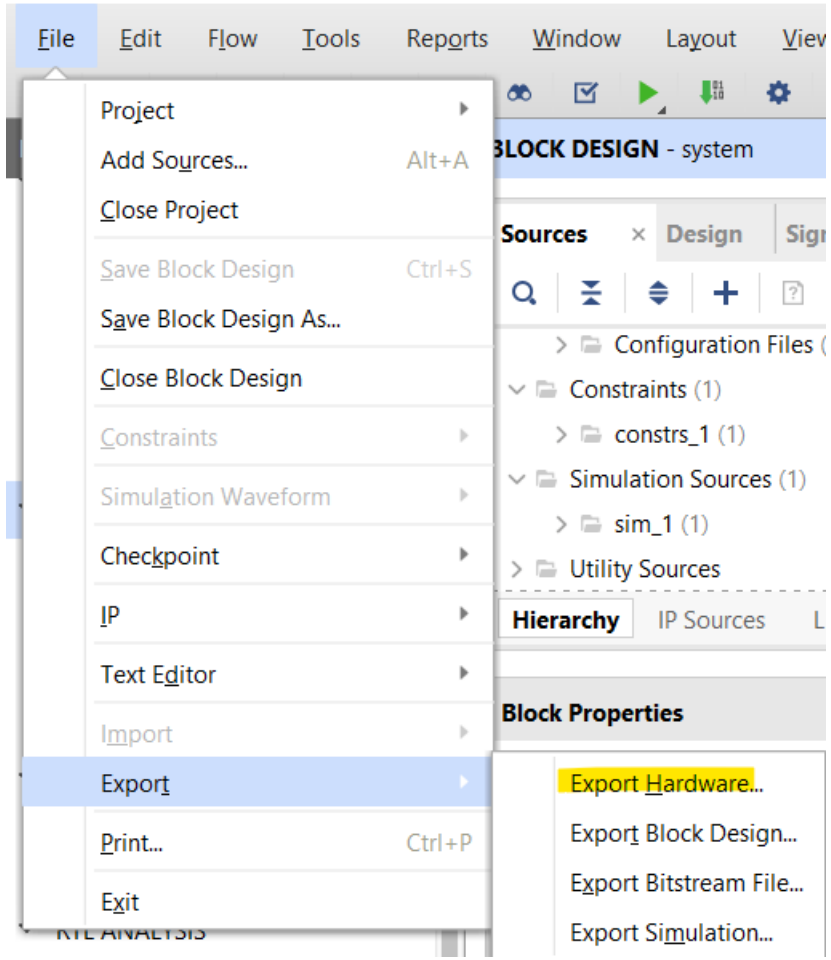


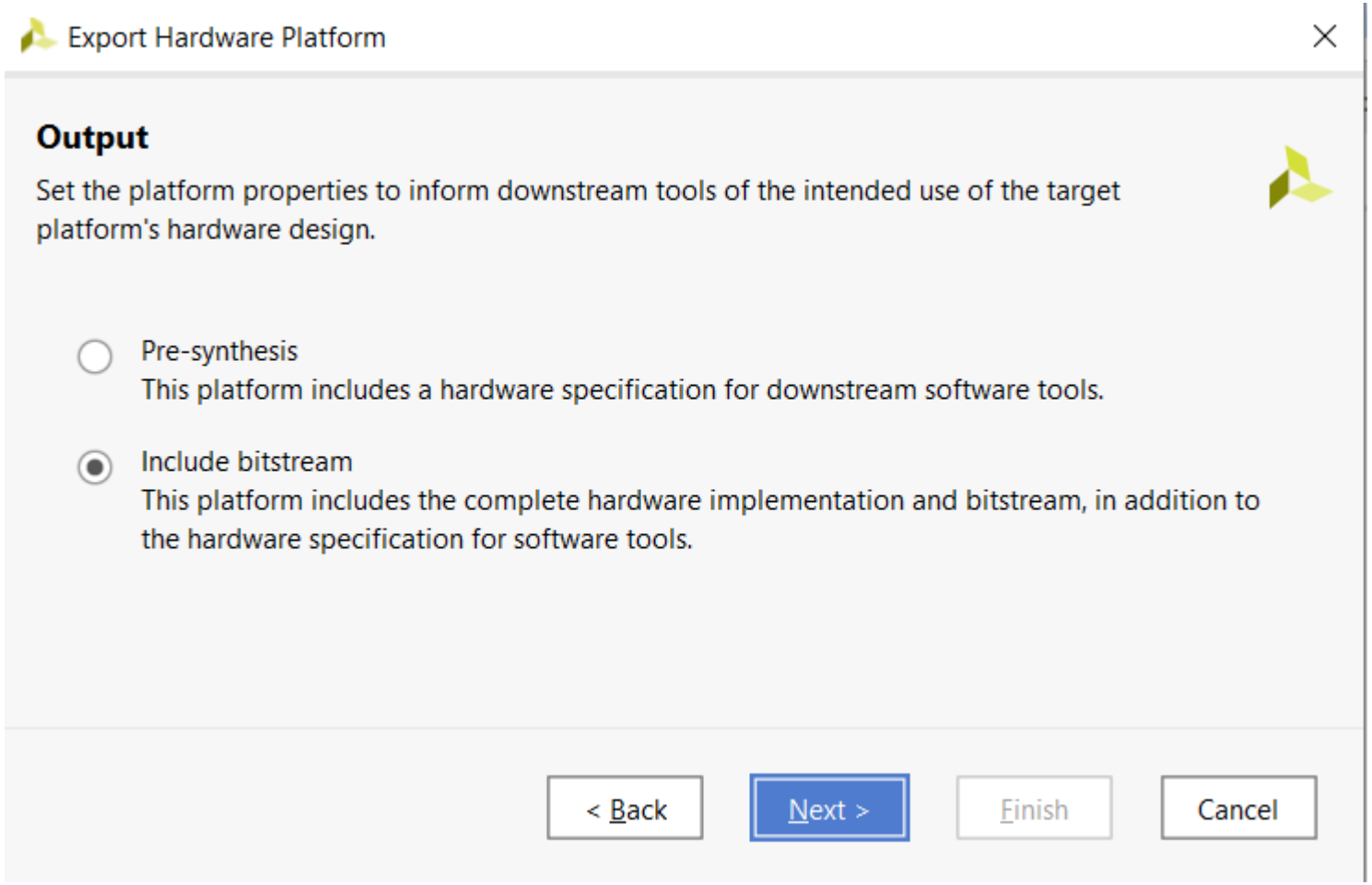




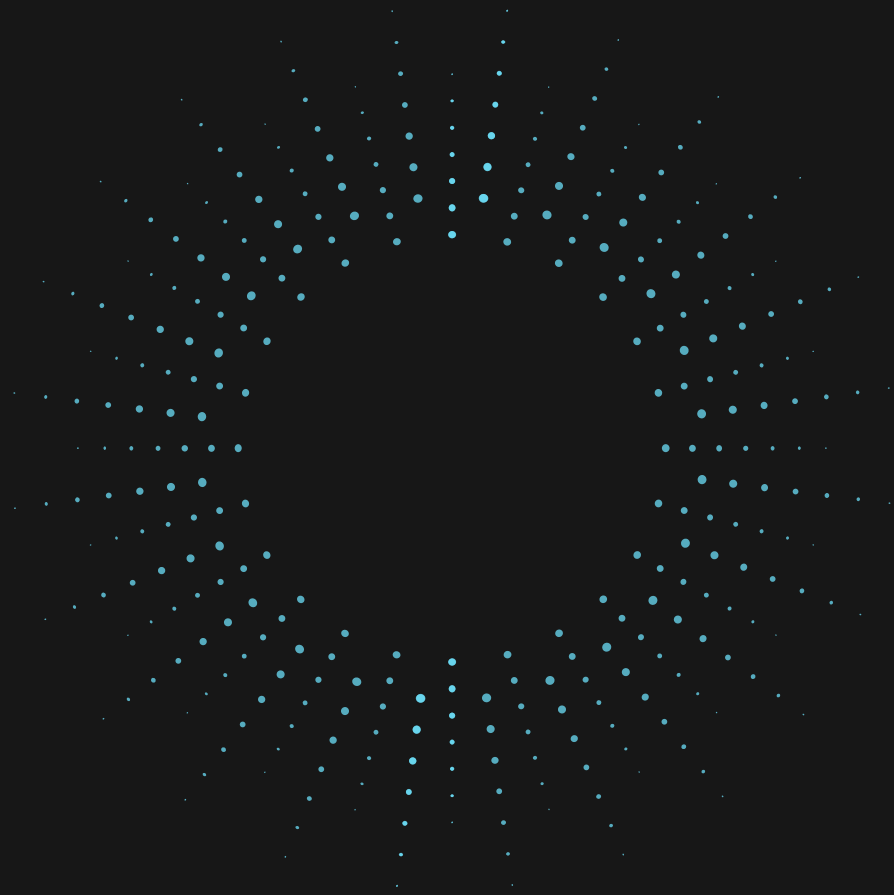

THIRTY-SEVEN
MINUTES
LATER...

VC707 Test Pattern Generator Flow

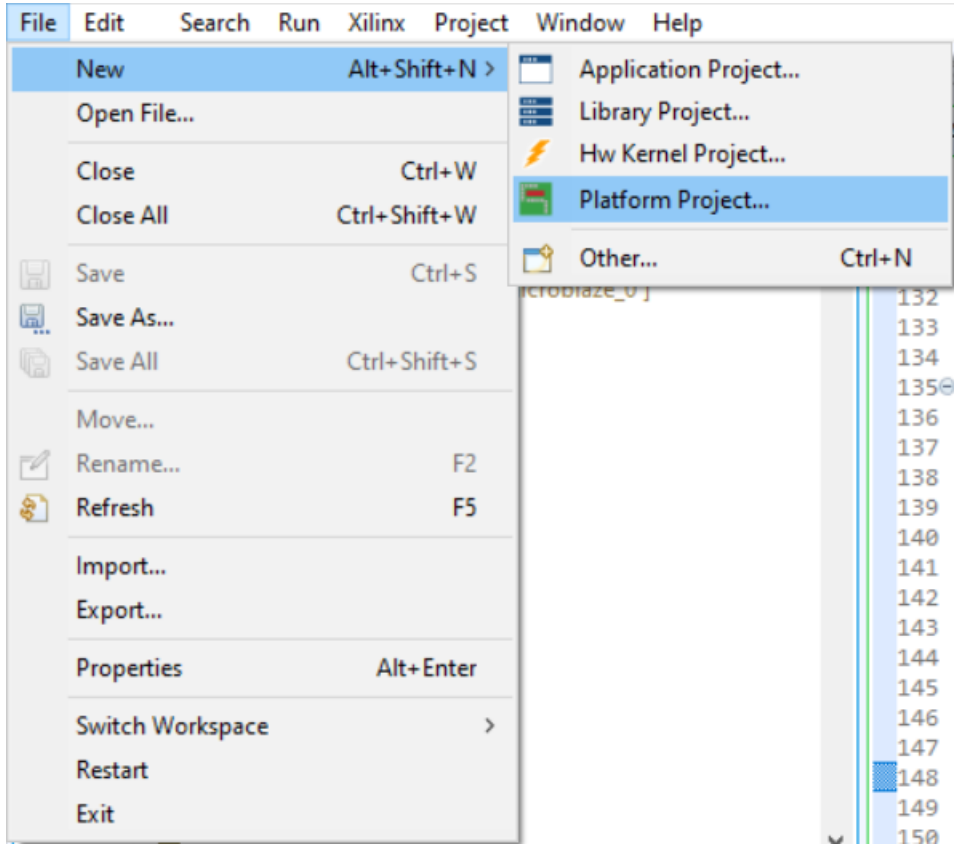


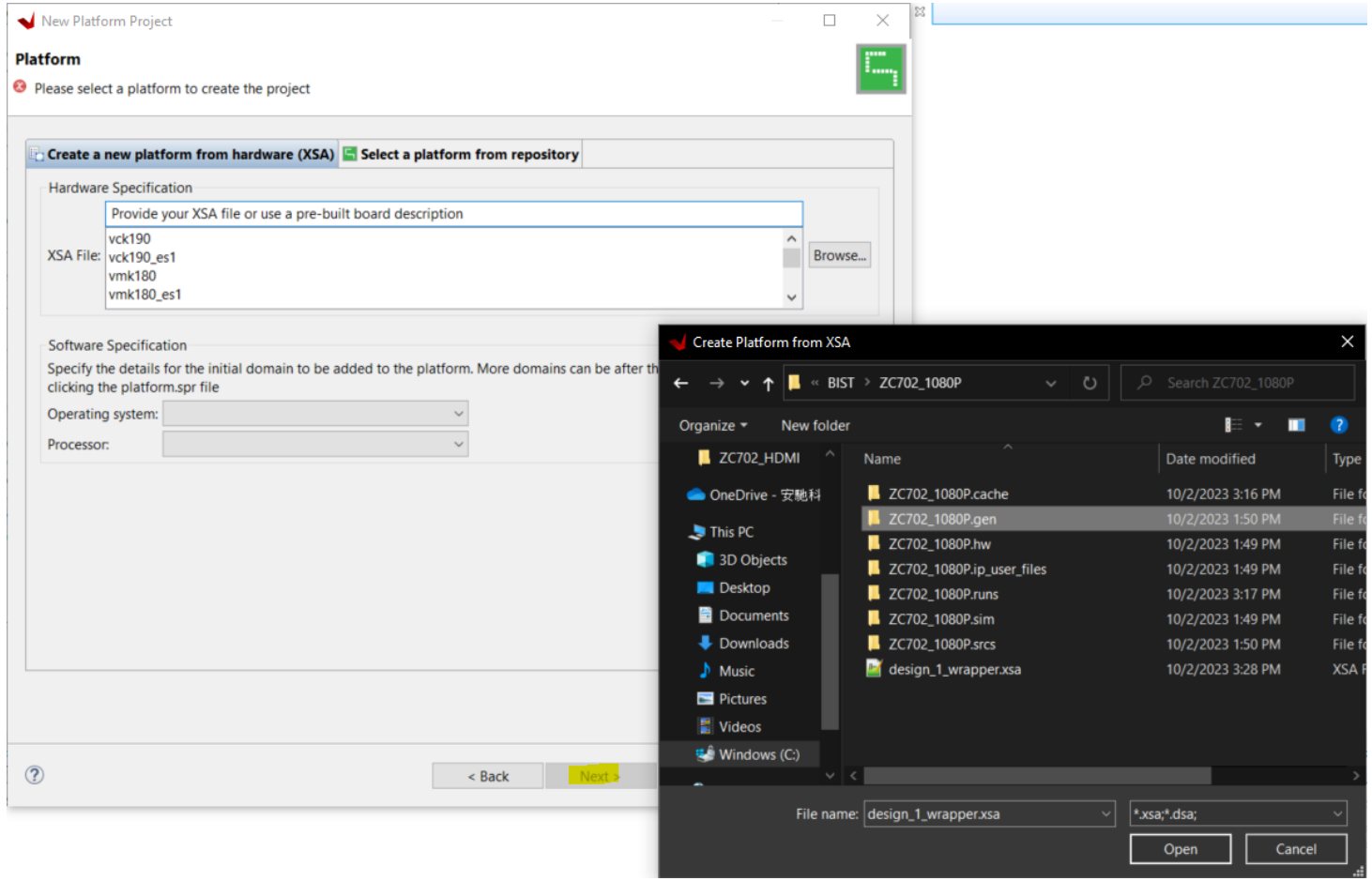


Vitis 2021.1 Part



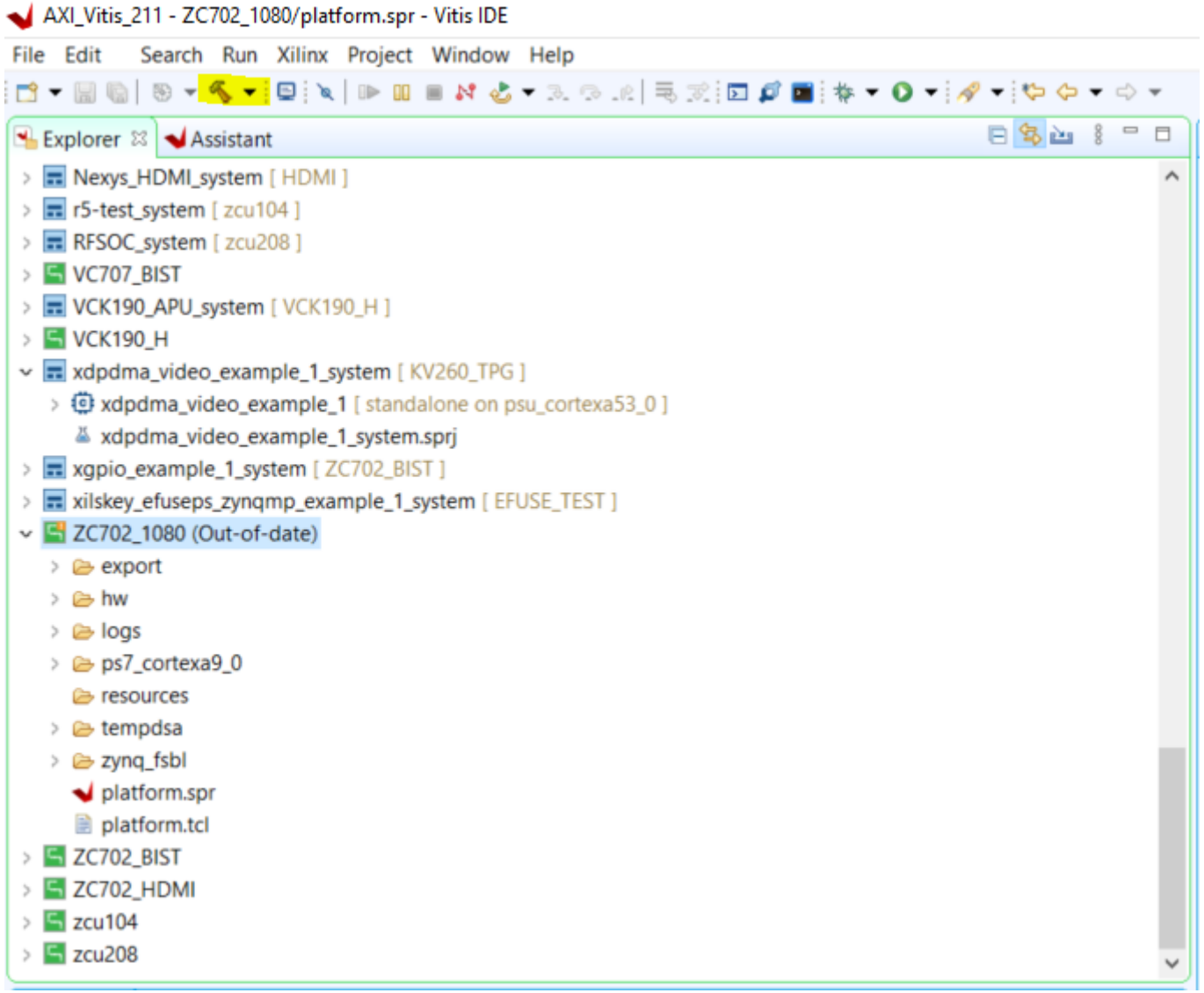
VC707 Test Pattern Generator Flow



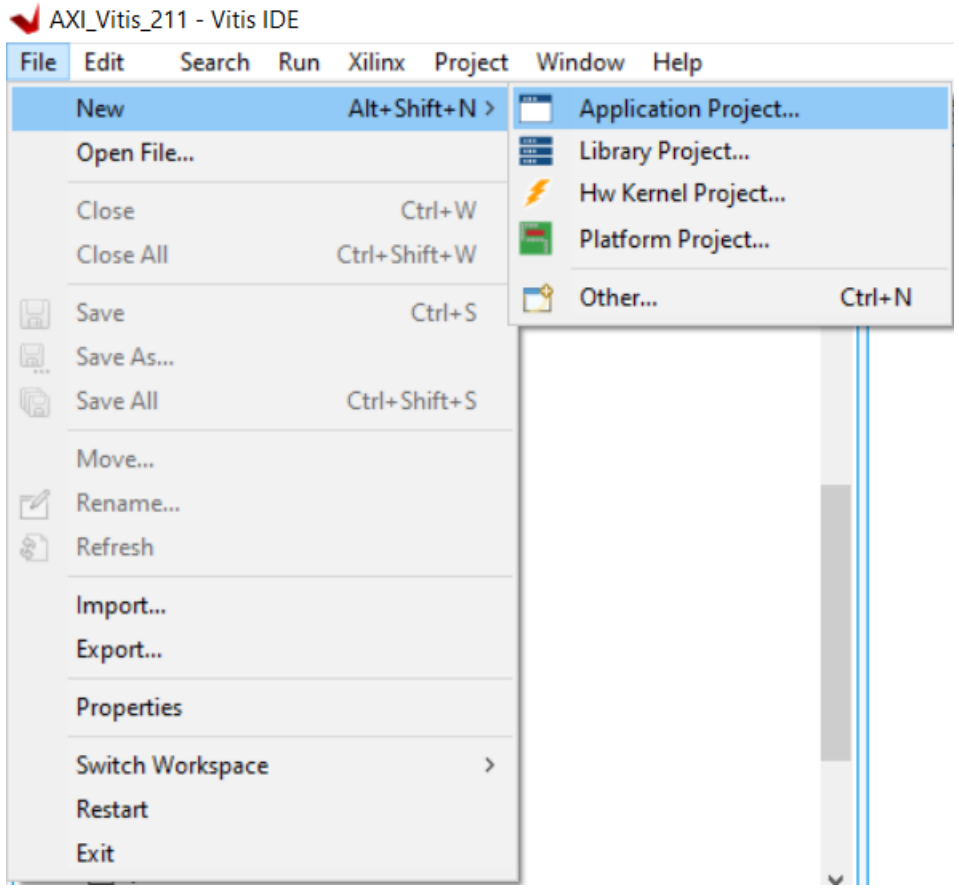


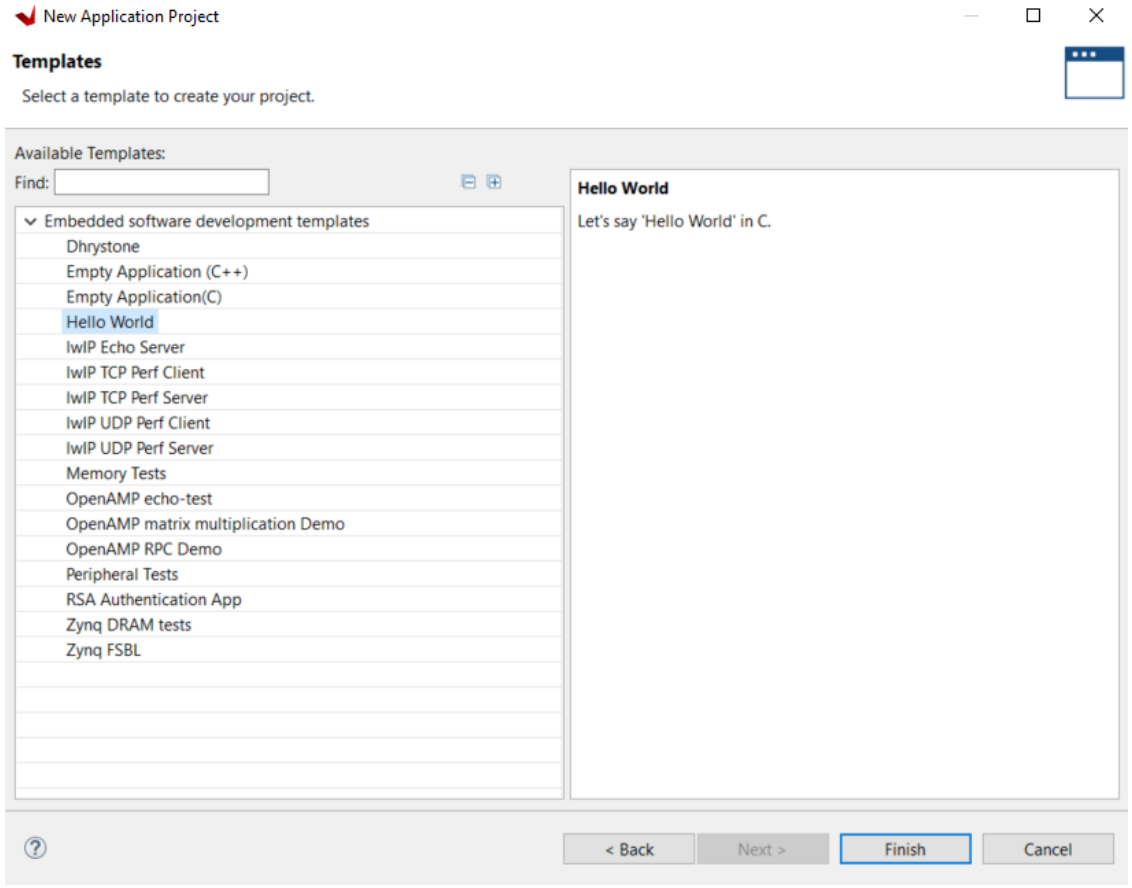
*** 實際檔案請按照自己設定的位置與名稱去開啟

VC707 Test Pattern Generator Flow



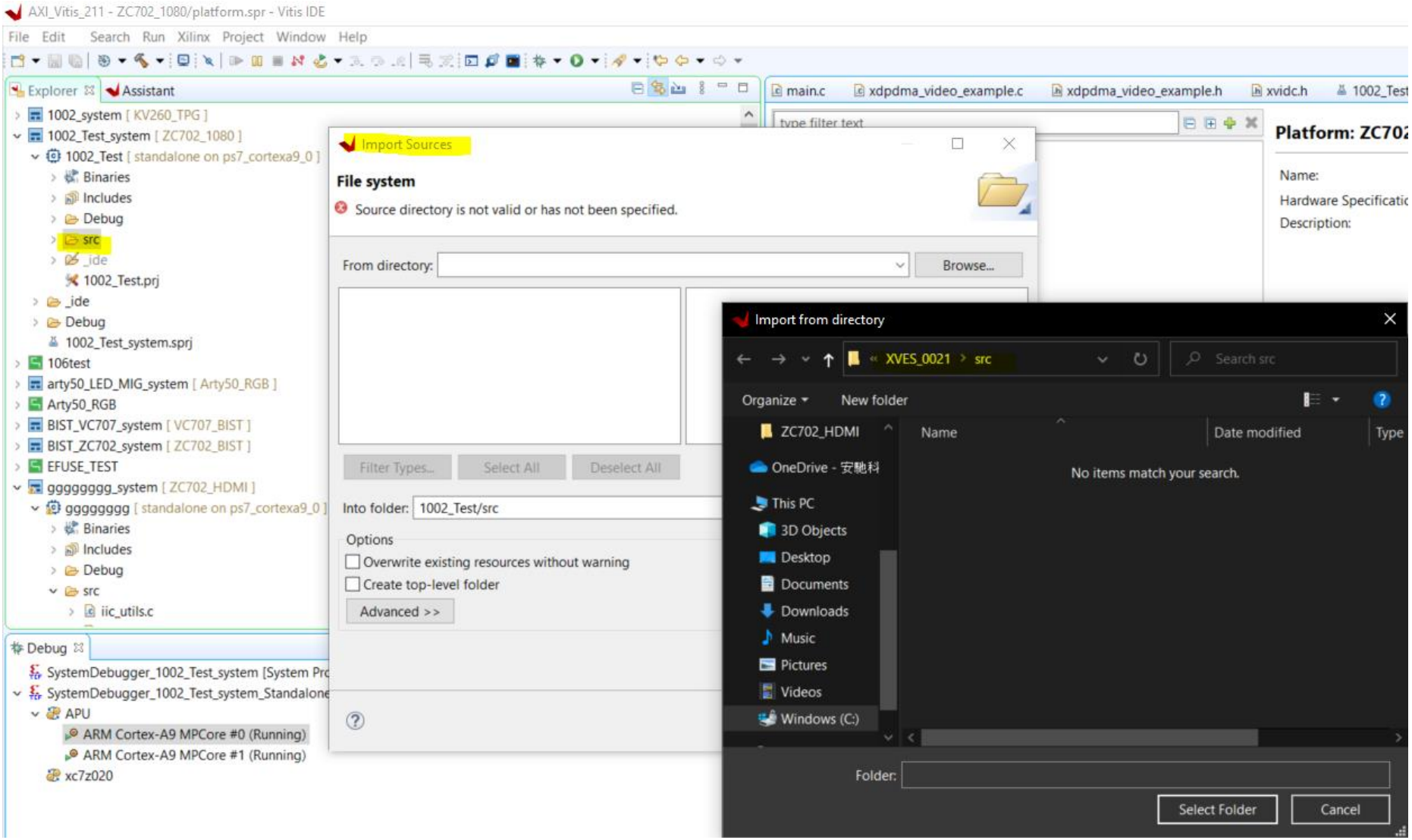
VC707 Test Pattern Generator Flow





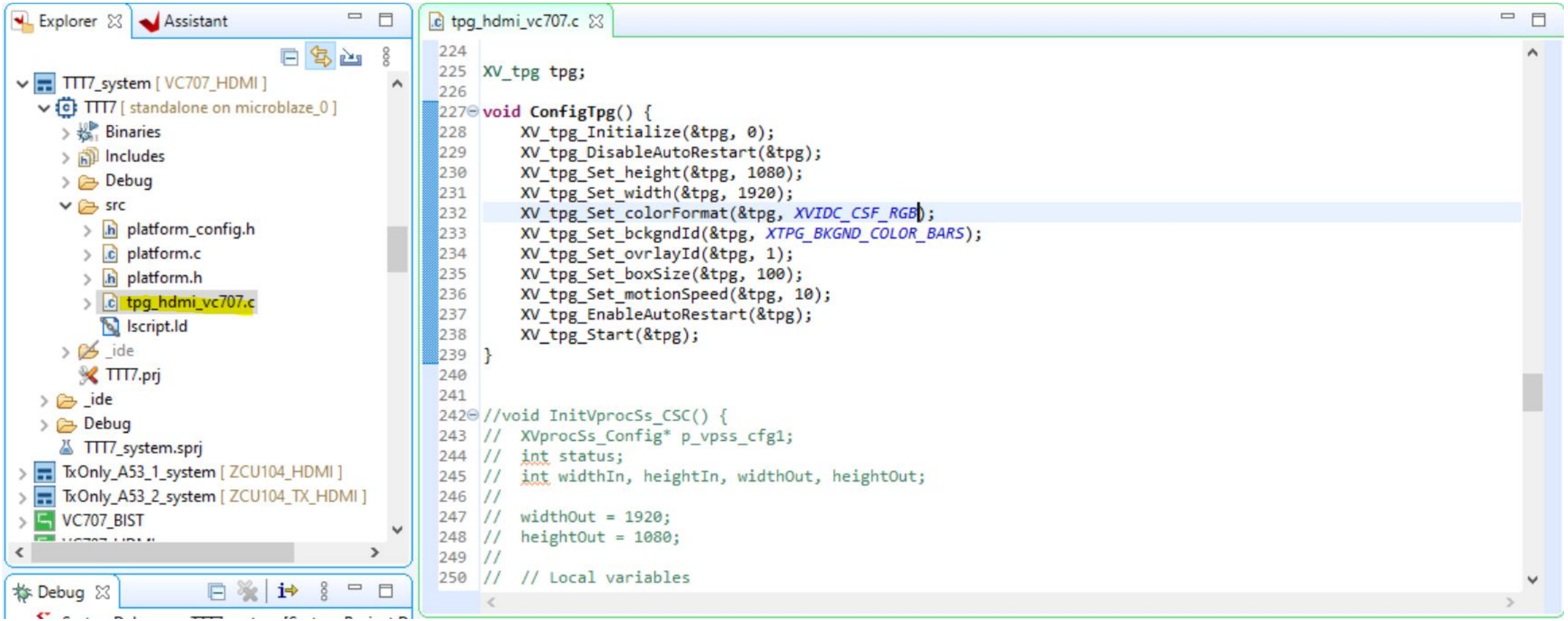
VC707 Test Pattern Generator Flow

helloworld.c 刪掉，然後新增一個文件 .c 檔，把以下 tpg_hdmi_vc707.c import 進去，日後再更新 code 內每個 function 功能

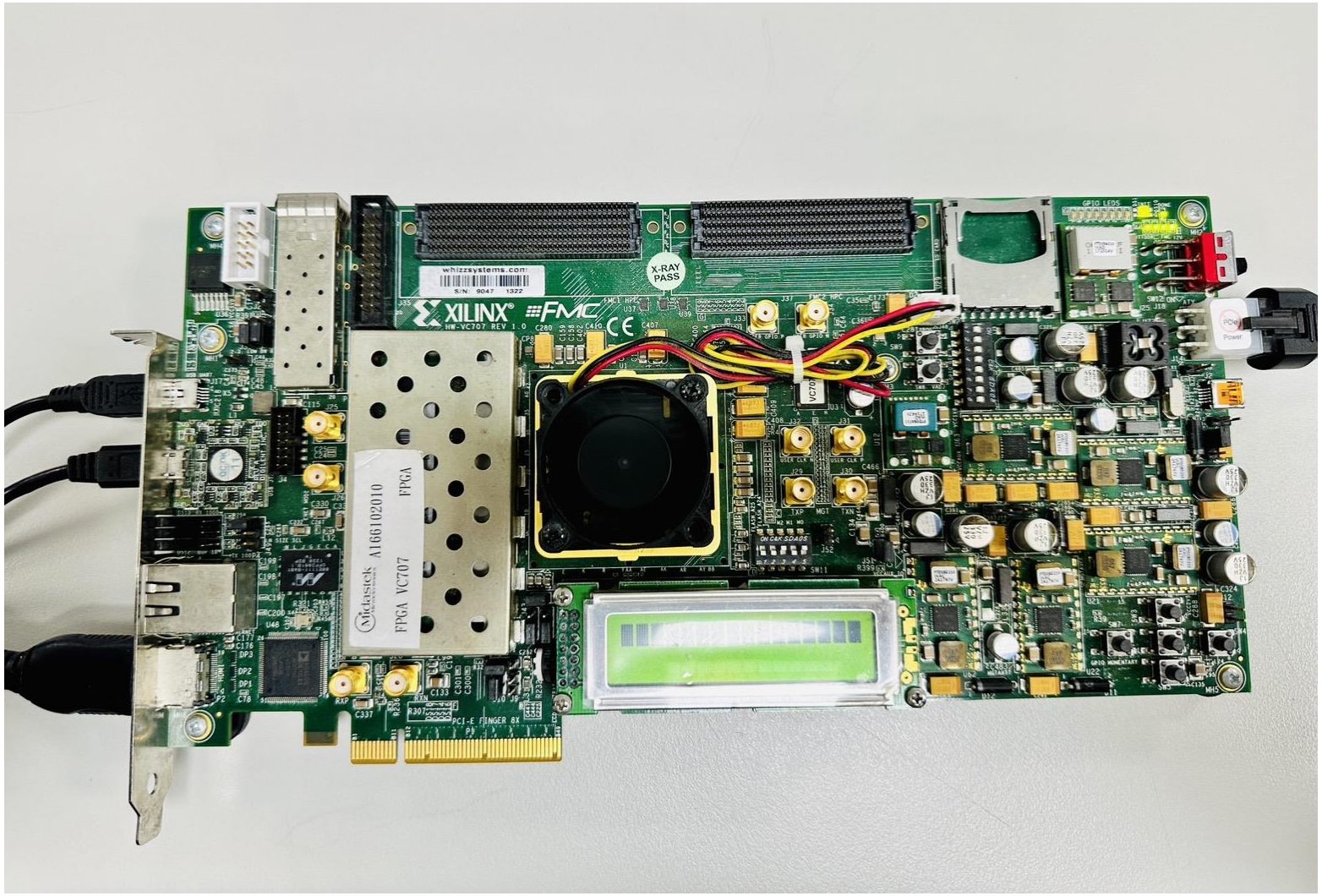


VC707 Test Pattern Generator Flow

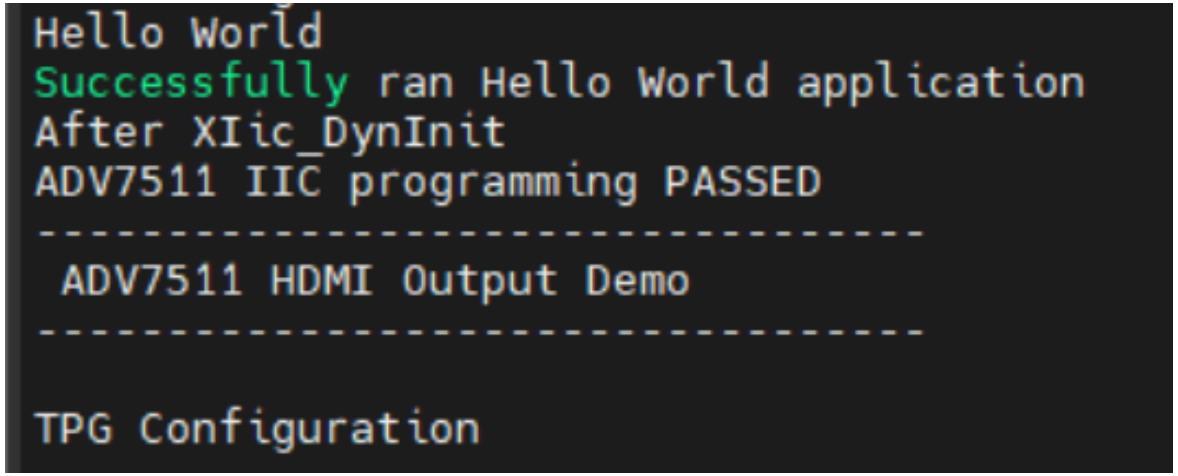
helloworld.c 刪掉，然後新增一個文件 .c 檔，把以下 tpg_hdmi_vc707.c import 進去，日後再更新 code 內每個 function 功能



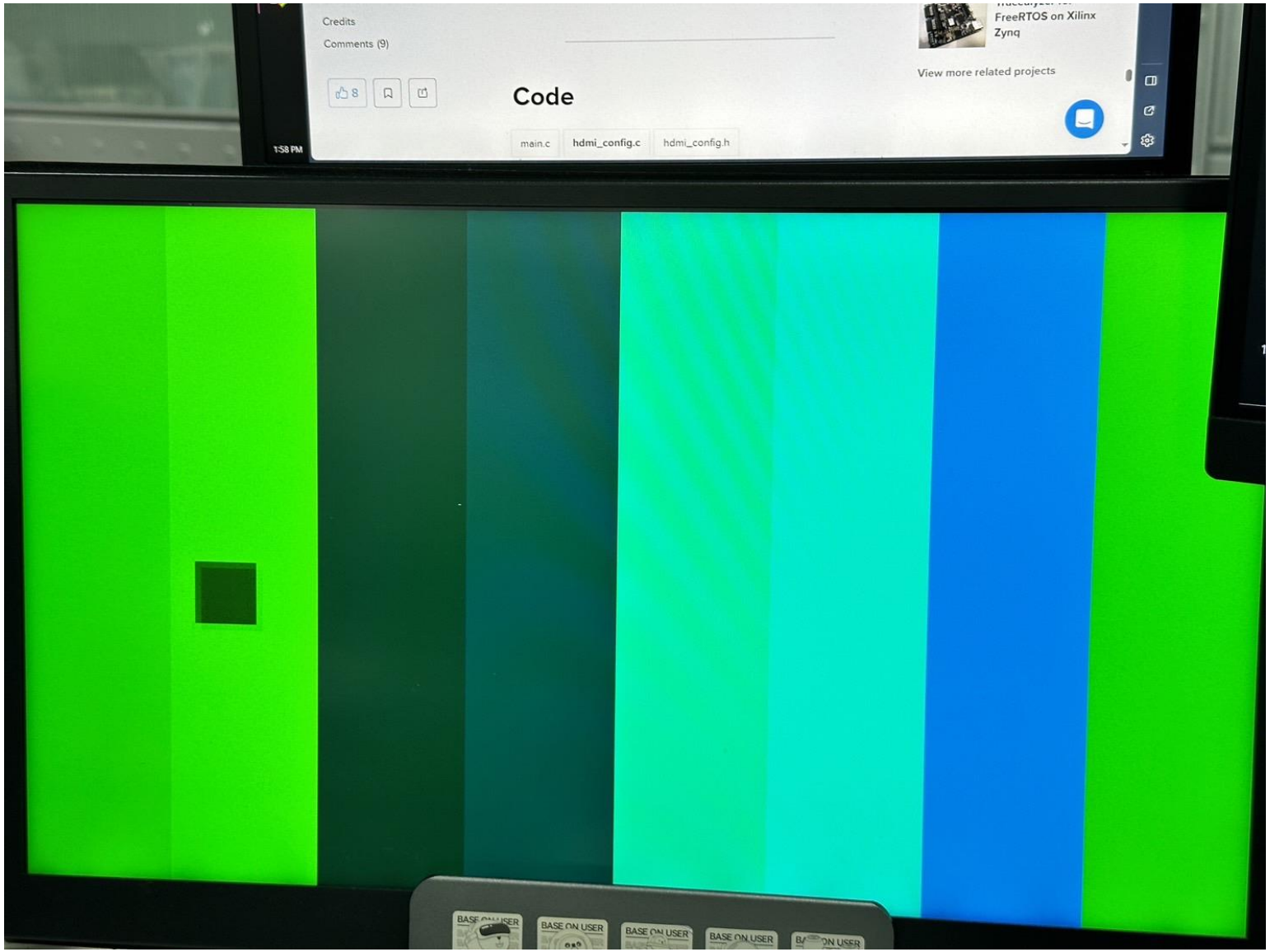
VC707 Hardware Setting



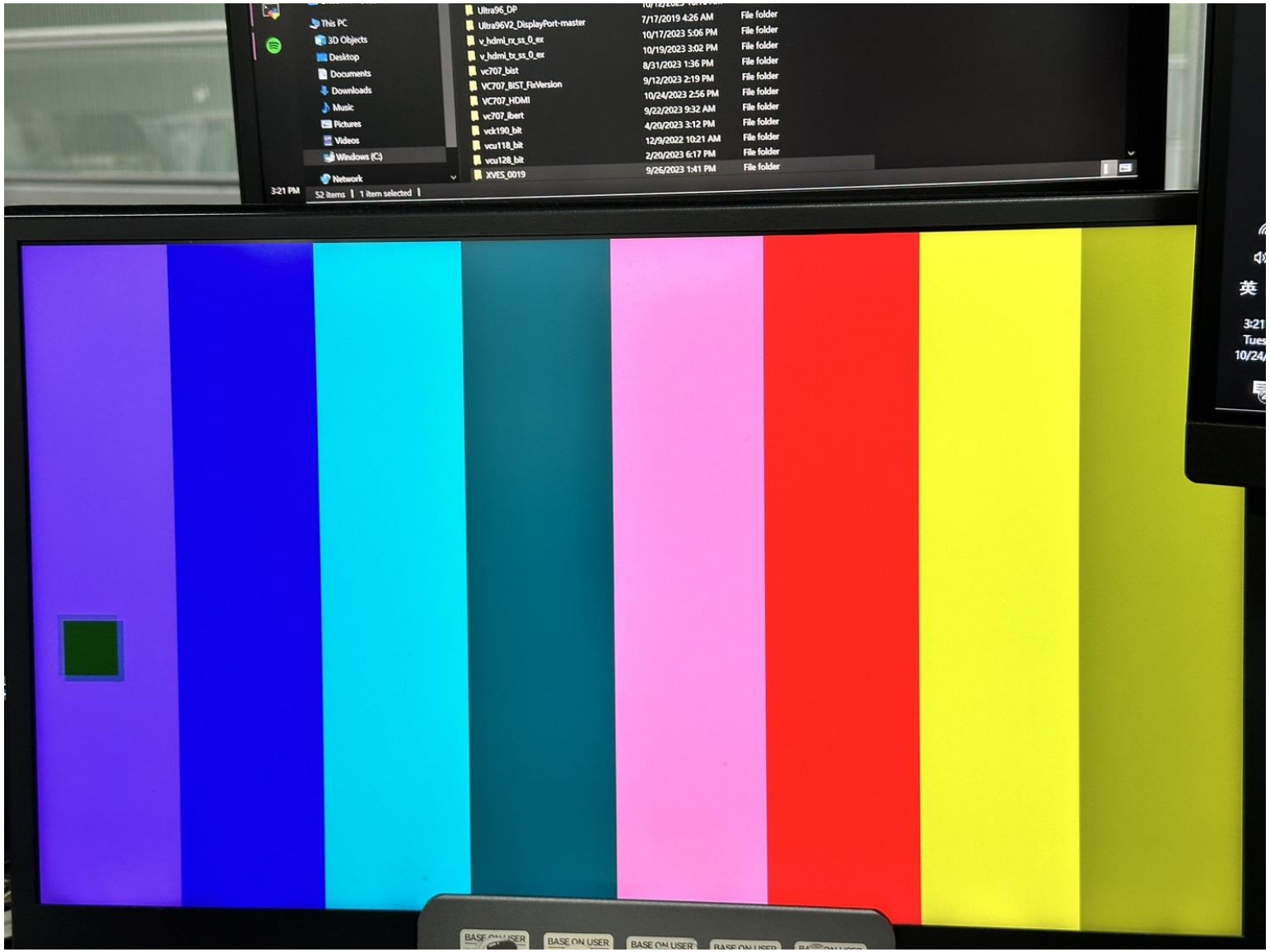
VC707 Test Pattern Generator Output Demo



VC707 Test Pattern Generator Output Demo



VC707 Test Pattern Generator Output Demo



VC707 Test Pattern Generator Output Demo Problem

1. Color Space 是錯誤的，顯示不出正確的彩條
2. 燒錄 VC707 有時候會出現 Microblaze instruction insert overrun，我也不知道為何
3. AXI4-Steam to Video Out 的 aresetn 不能接，感覺跟 Vitis C Code 設定有關係
4. 一定先讓 MIG 做 Block Automation 後產出 sys_diff_clock，再讓 MicroBlaze 做 Block Automation

Reference

1. Xilinx FPGA-HDMI1.4: You Must Know First ! - Hackster.io
2. https://www.hackster.io/adam-taylor/ac701-hdmi-test-pattern-generation-9aa148


AMD