



# **ZCU104(MPSoC) DP TPG Output Example**

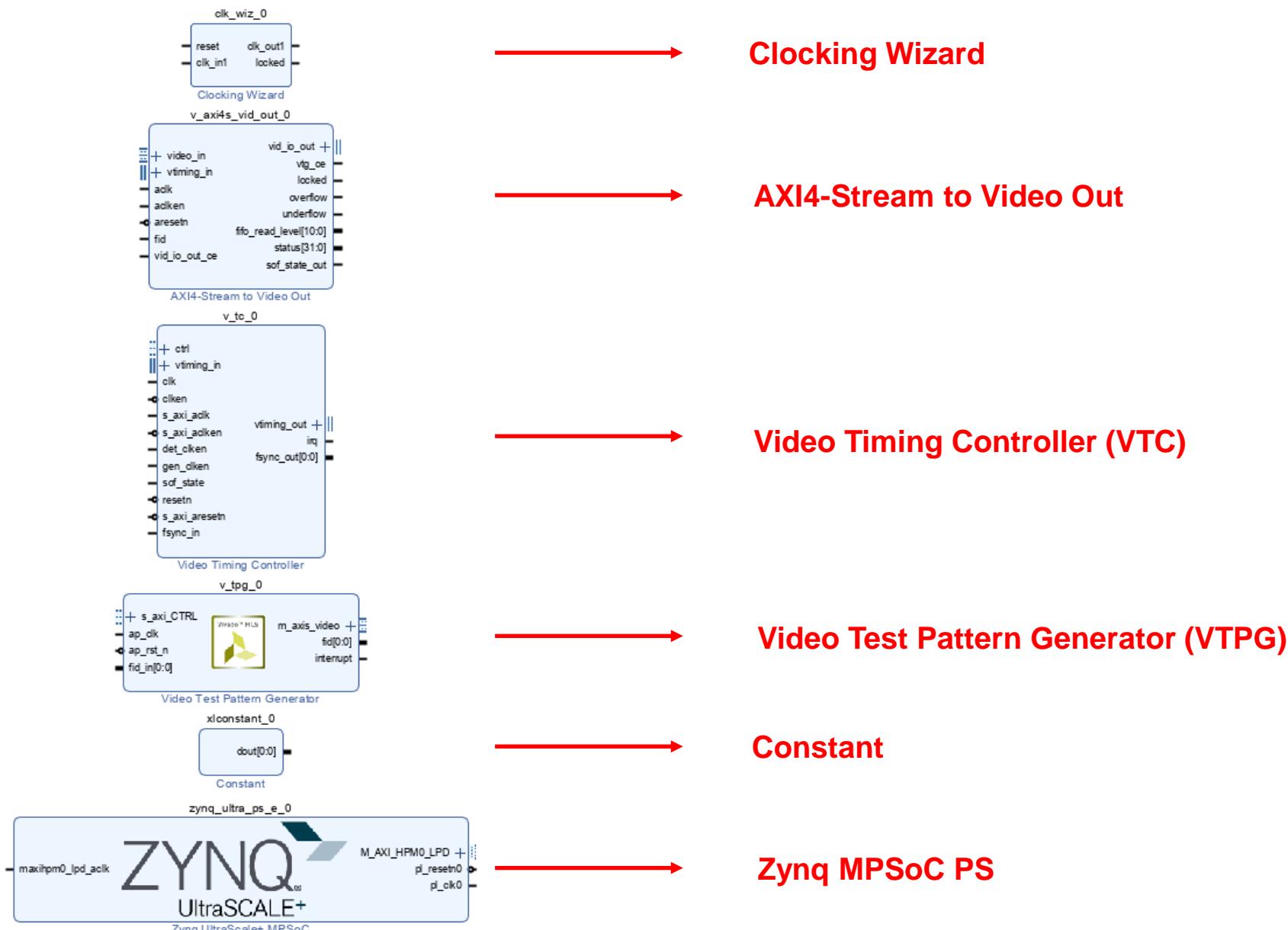
**Field Application Engineer**  
Adaptive and Embedded Computing Group (AECG)

# Vivado 2021.1 Part

# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

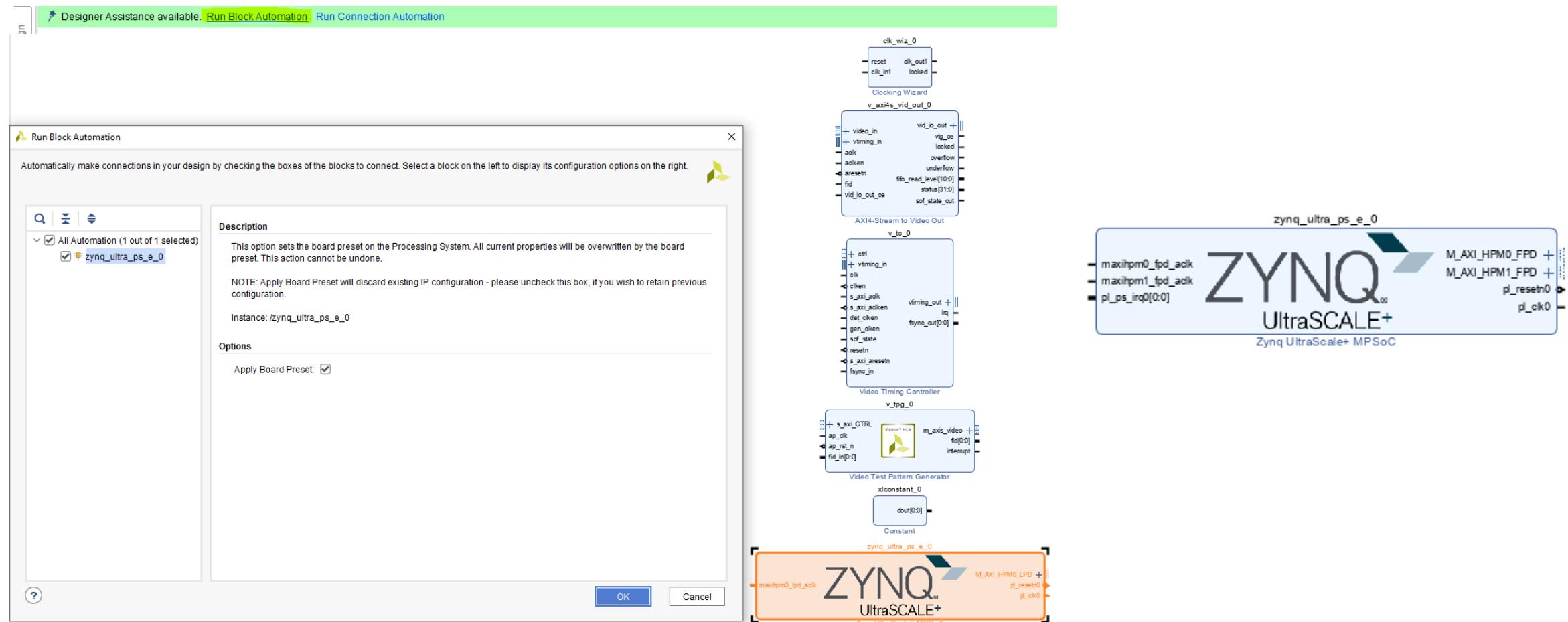
先召喚出六個 IP



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

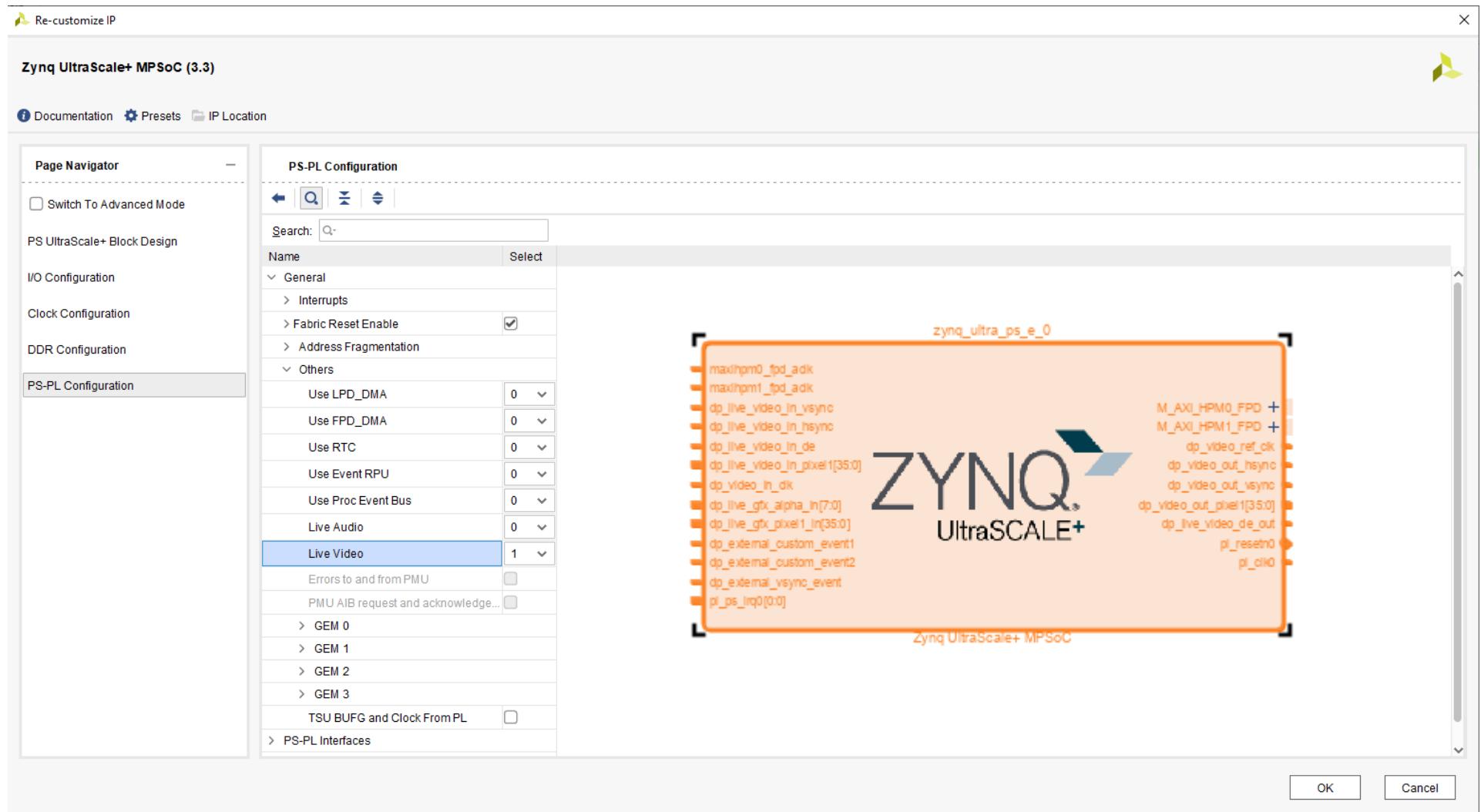
### Zynq MPSoC PS -1



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

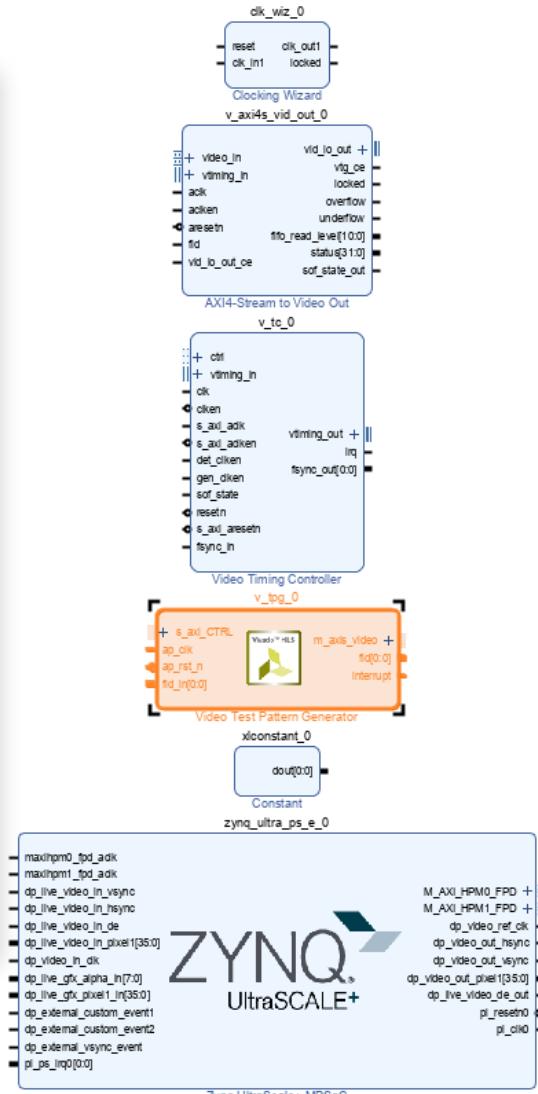
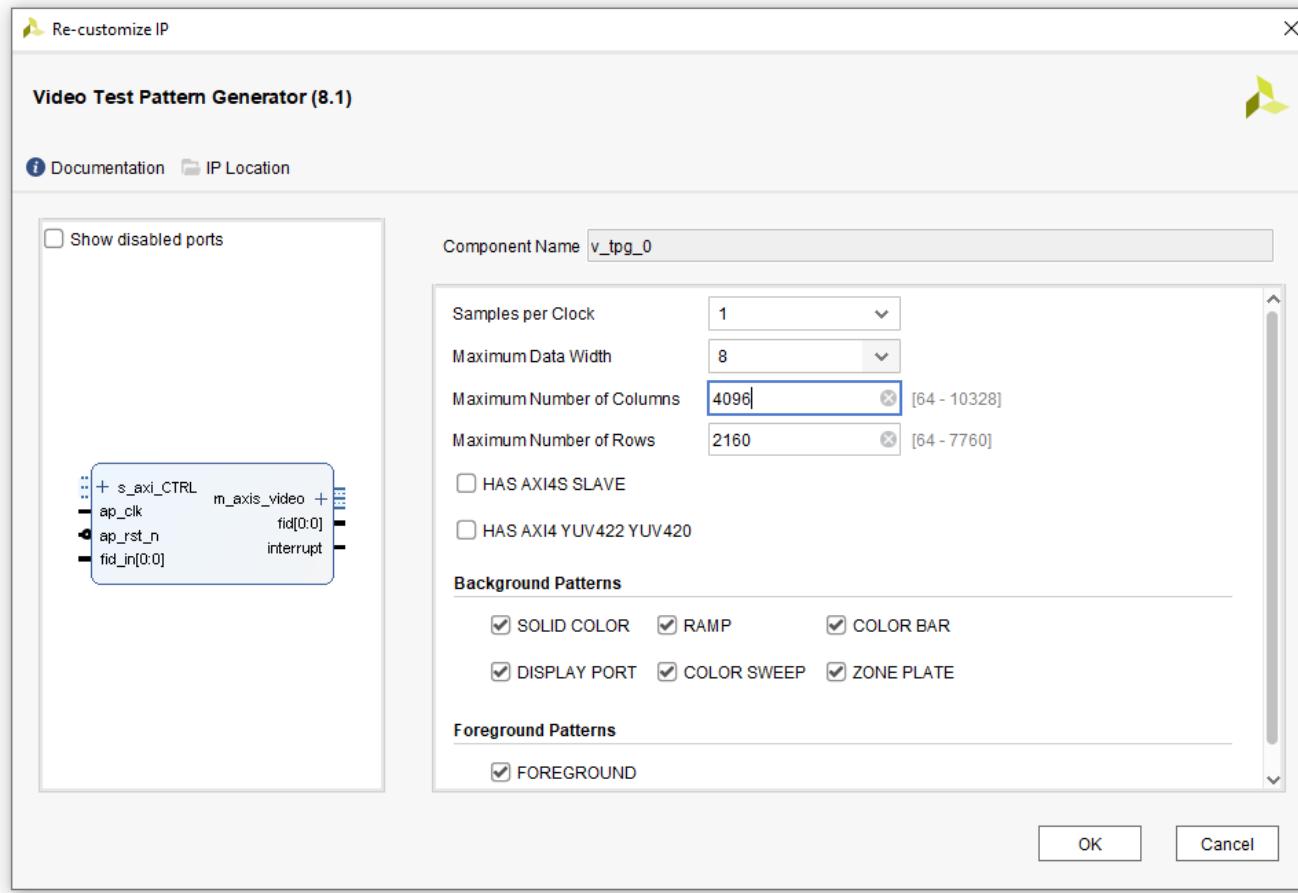
### Zynq MPSoC PS -2



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

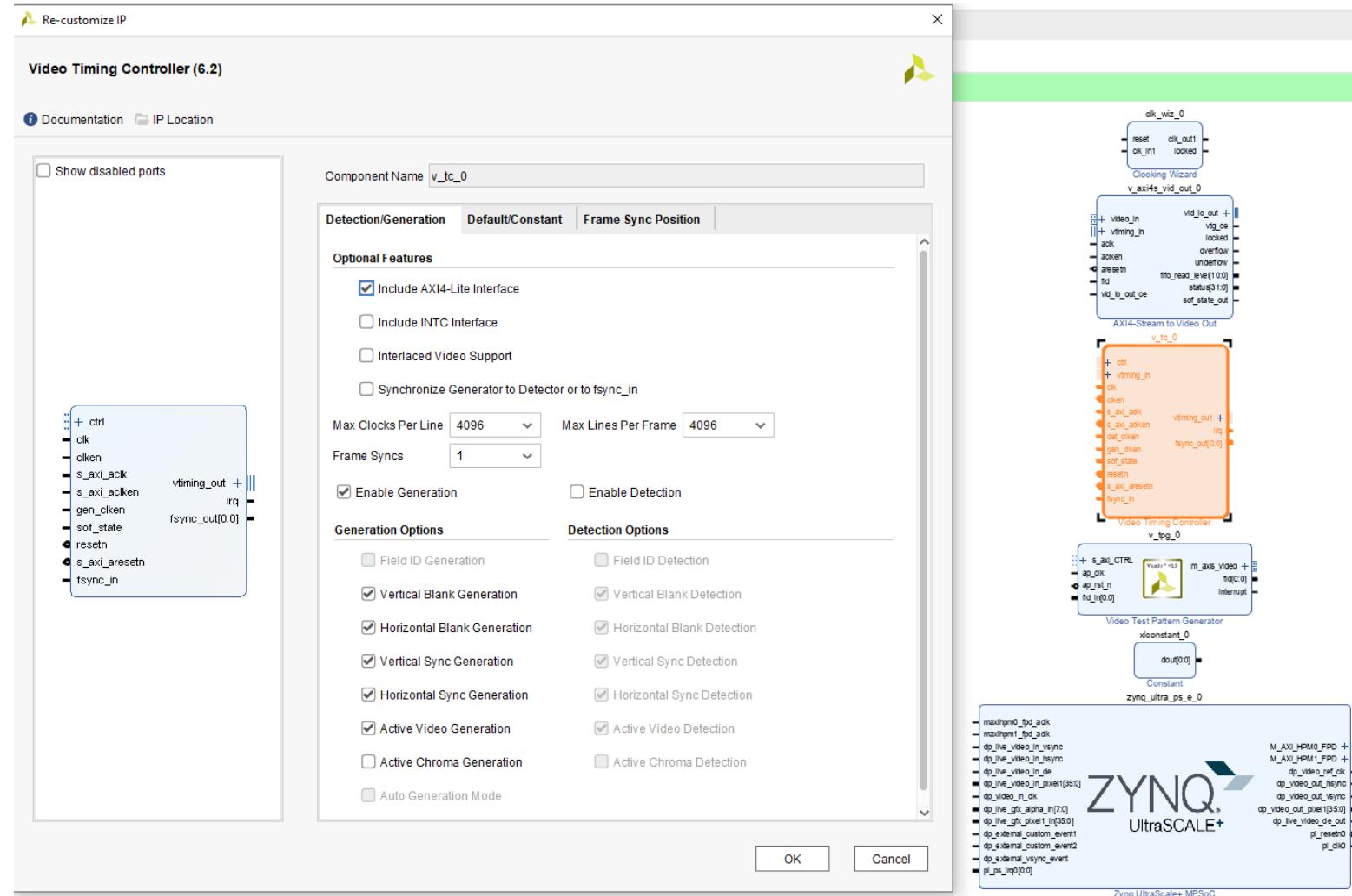
### Video Test Pattern Generator (VTPG)



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

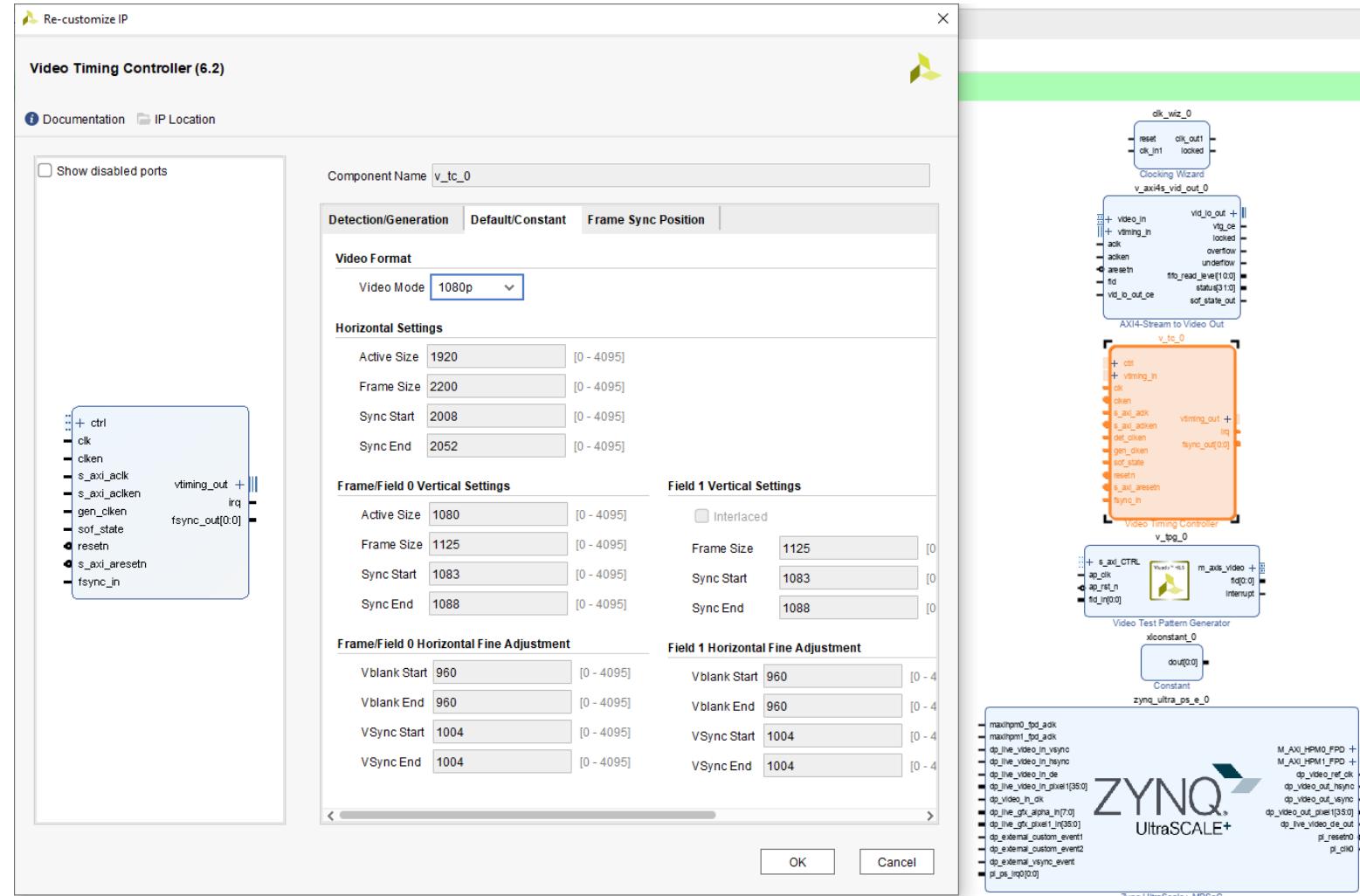
### Video Timing Controller (VTC) -1



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

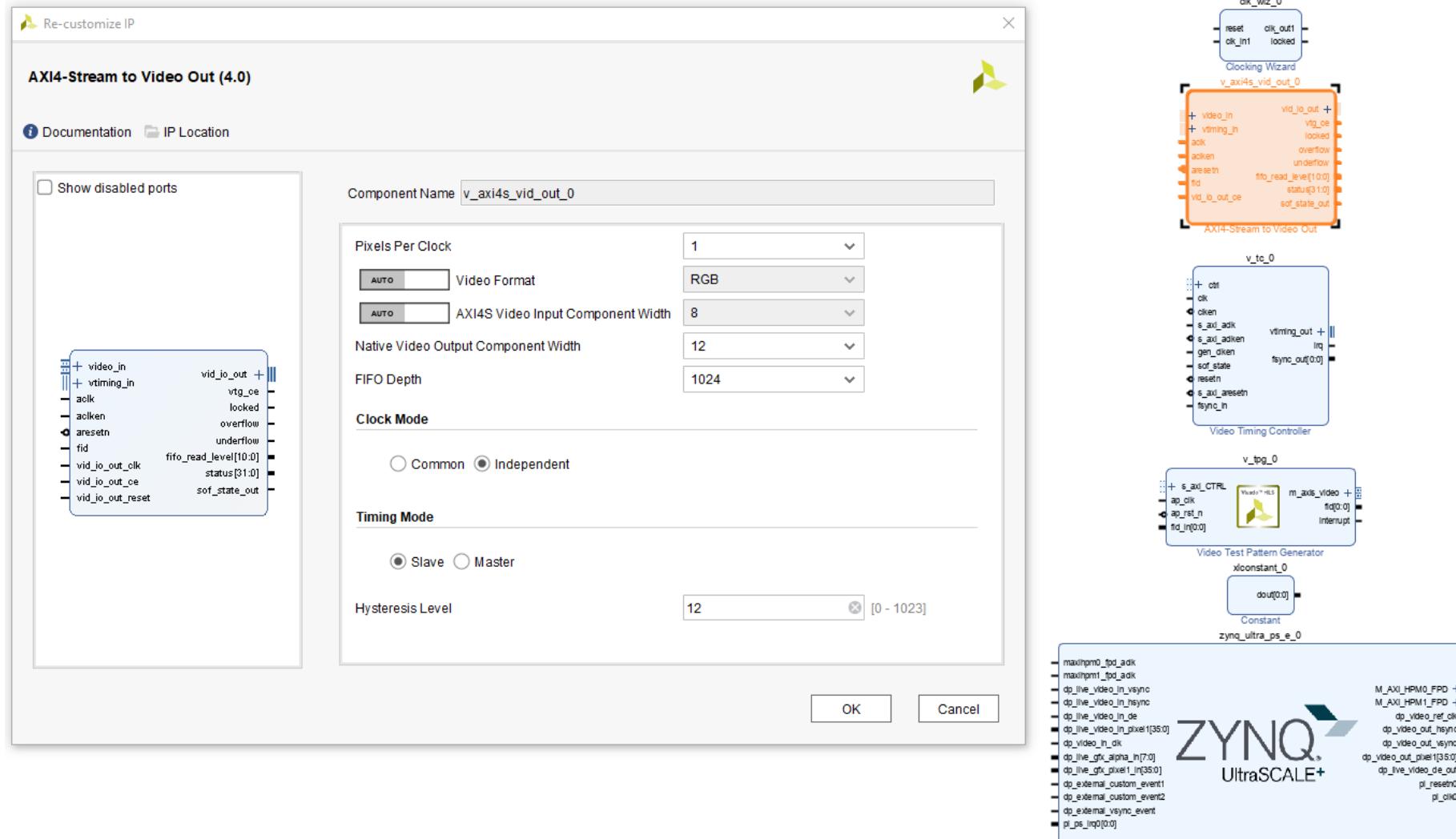
### Video Timing Controller (VTC) -2



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

### AXI4-Stream to Video Out



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

### Clocking Wizard - 1

**Clocking Wizard (6.0)**

Documentation IP Location

Component Name: clk\_wiz\_0

Board	Clocking Options	Output Clocks	MMCM Settings	Summary
<input checked="" type="checkbox"/> clk_out1	clk_out1	148.5	148.50000	Requested: 0.000 Actual: 0.000 Request: 50.000
<input type="checkbox"/> clk_out2	clk_out2	100.000	N/A	Requested: 0.000 Actual: N/A Request: 50.000
<input type="checkbox"/> clk_out3	clk_out3	100.000	N/A	Requested: 0.000 Actual: N/A Request: 50.000
<input type="checkbox"/> clk_out4	clk_out4	100.000	N/A	Requested: 0.000 Actual: N/A Request: 50.000
<input type="checkbox"/> clk_out5	clk_out5	100.000	N/A	Requested: 0.000 Actual: N/A Request: 50.000
<input type="checkbox"/> clk_out6	clk_out6	100.000	N/A	Requested: 0.000 Actual: N/A Request: 50.000
<input type="checkbox"/> clk_out7	clk_out7	100.000	N/A	Requested: 0.000 Actual: N/A Request: 50.000

USE CLOCK SEQUENCING

Output Clock	Sequence Number
clk_out1	1
clk_out2	1
clk_out3	1
clk_out4	1
clk_out5	1
clk_out6	1
clk_out7	1

Enable Optional Inputs / Outputs for MMCM/PLL

Reset Type: Active High

Phase Shift Mode: WAVE

Locked:

clkfbstopped:

**IP Symbol** **Resource**

Show disabled ports

**clk\_wiz\_0**

reset, clk\_out1, locked

**v\_axi4s\_vid\_out\_0**

video\_in, timing\_in, ack, acken, aresetn, ns, vid\_o\_out\_clk, vid\_o\_out\_ce, vid\_o\_out\_reset, vid\_o\_out\_tdata, vid\_o\_out\_tlast, vid\_o\_out\_tvalid, vid\_o\_out\_tuser, vga\_ce, overflow, undefow, mto\_read\_level[10:0], status[3:0], sof\_state\_out

**v\_to\_0**

dr, dki, dken, s\_axis\_tck, s\_axis\_tcken, gen\_tcken, soi\_tstate, reset, s\_axis\_tareset, tsync\_jn, vtiming\_out, vsync\_out[0:0]

**v\_tpg\_0**

t\_exl\_CTRL, ap\_clk, ap\_stn, rd\_h[0:0], m\_axis\_video, interrupt, xconstant\_0, out[0:0], Constant, zynq\_ultra\_ps\_e\_0

M\_AXI\_HPM0\_RPD, M\_AXI\_HPM1\_RPD, dp\_video\_ref\_clk, dp\_video\_out\_hsync, dp\_video\_out\_vsync, dp\_video\_out\_pixel[15:0], dp\_video\_out\_de\_out, pl\_resetn, pl\_clk0

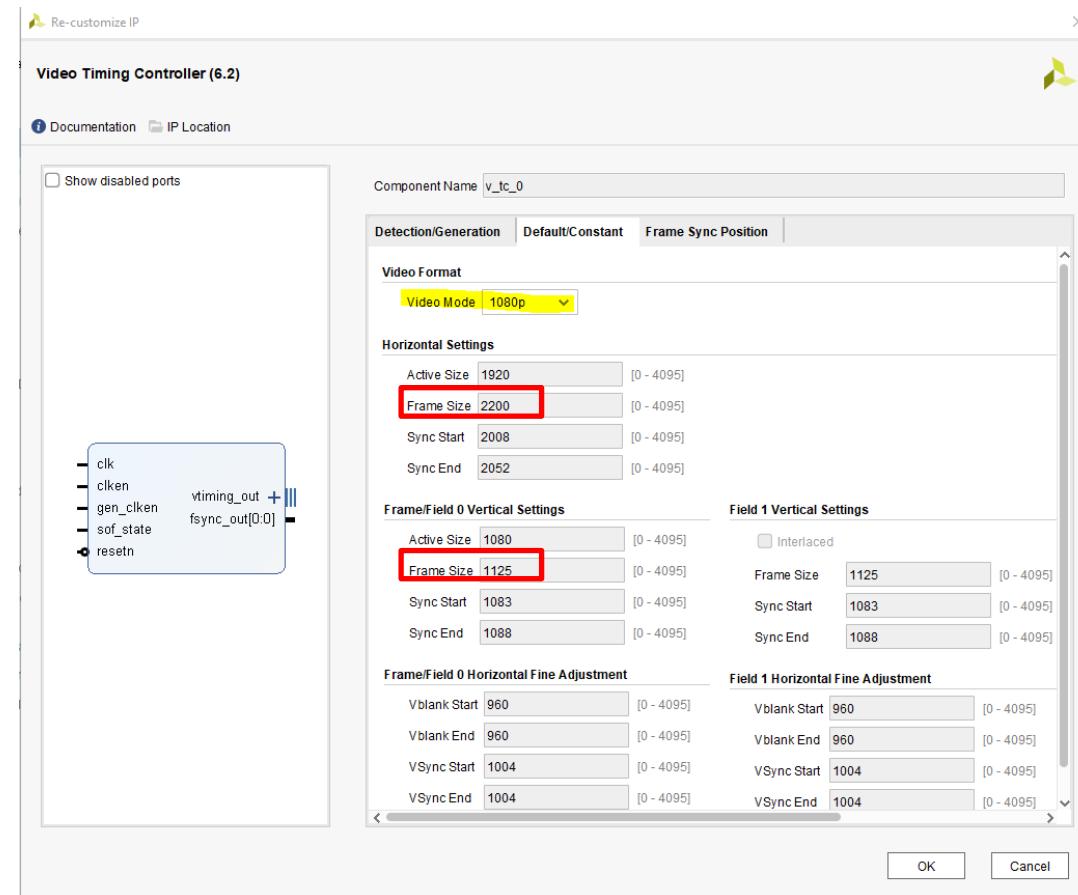
**ZYNQ UltraSCALE+**

AMD together we advance

# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

### Clocking Wizard - 2

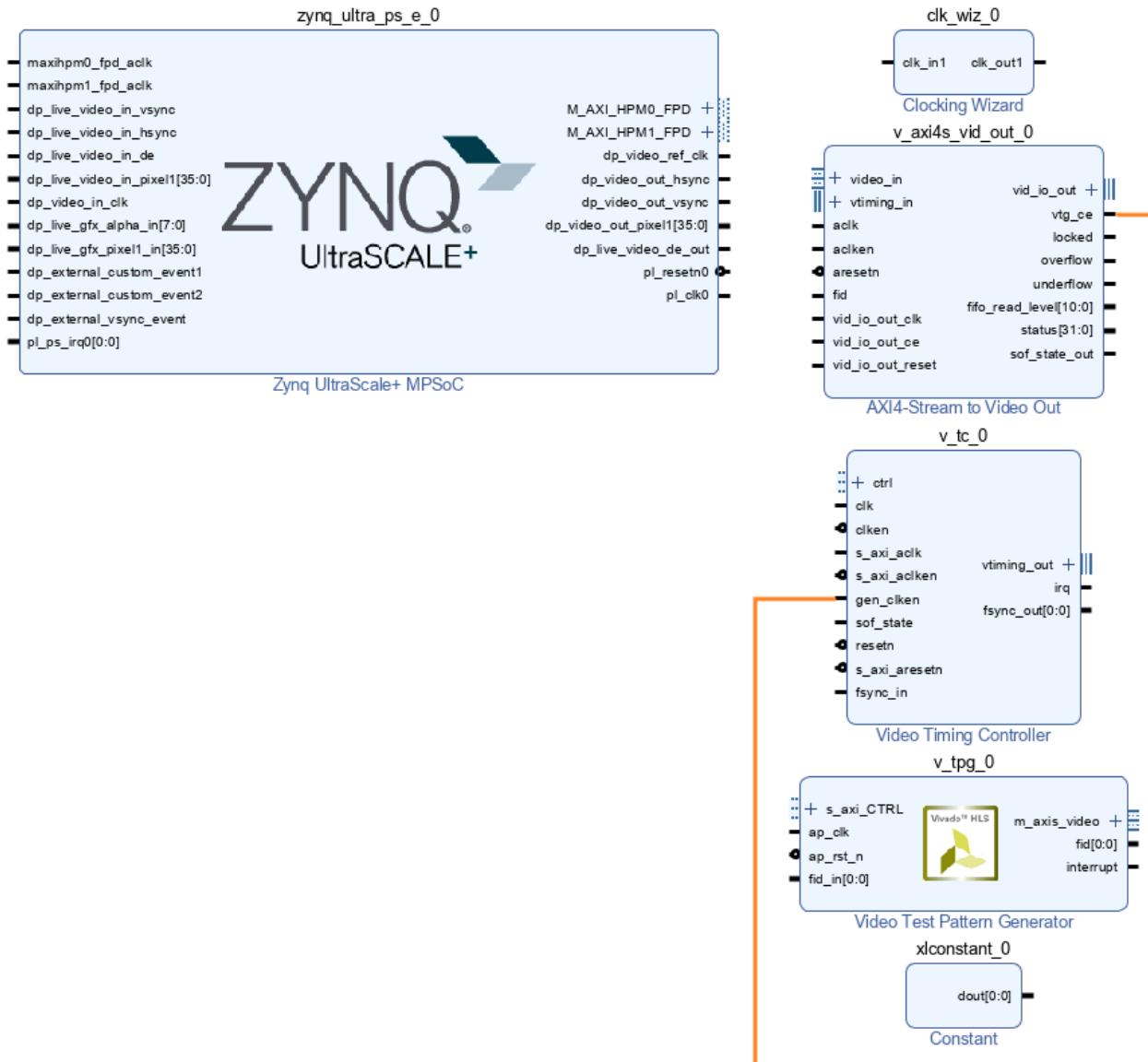


$$148.5 \text{ Mhz} = \frac{2200 \times 1125 \times 60}{10^6}$$

# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

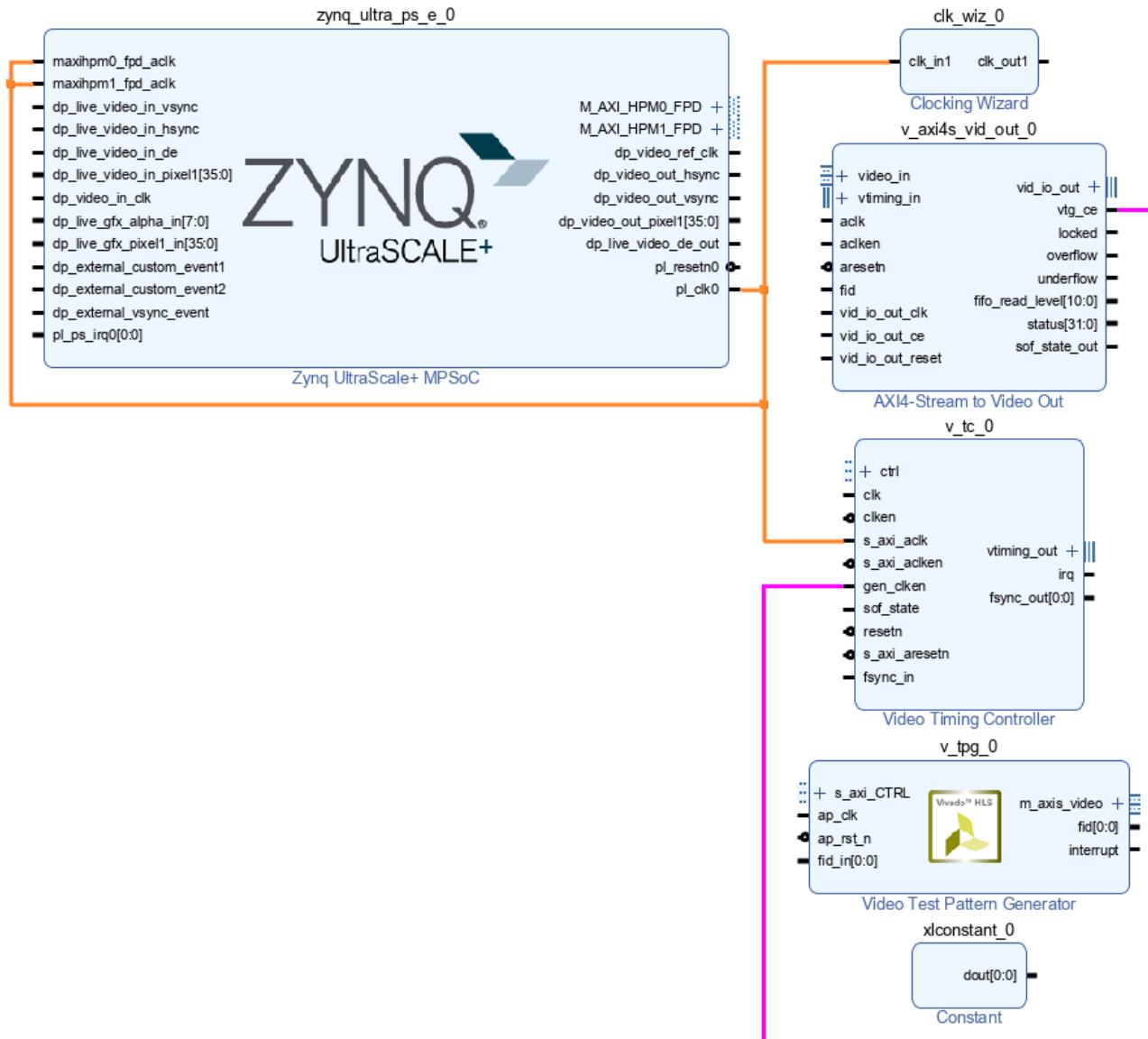
### Start Connection



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

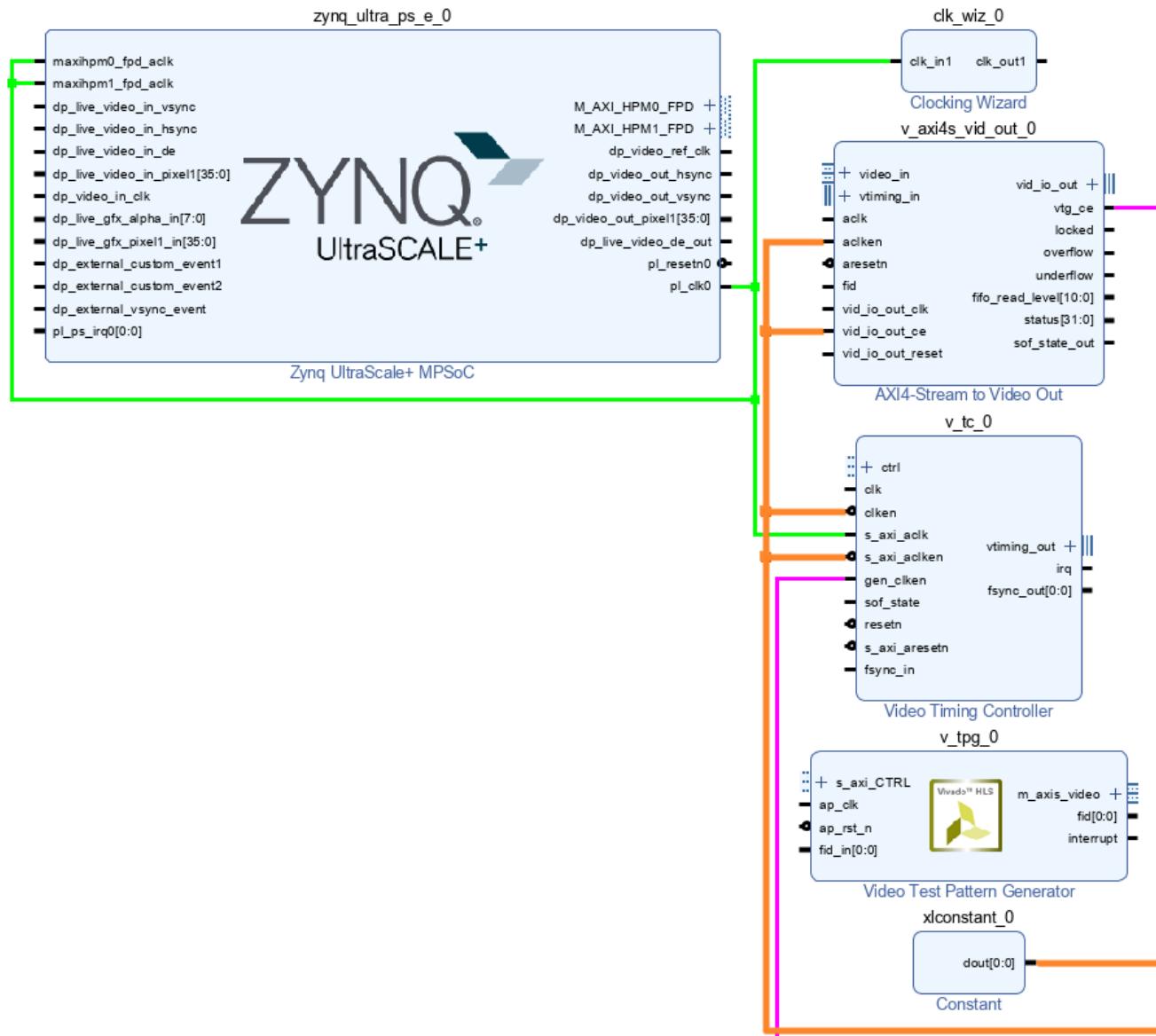
### Start Connection



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

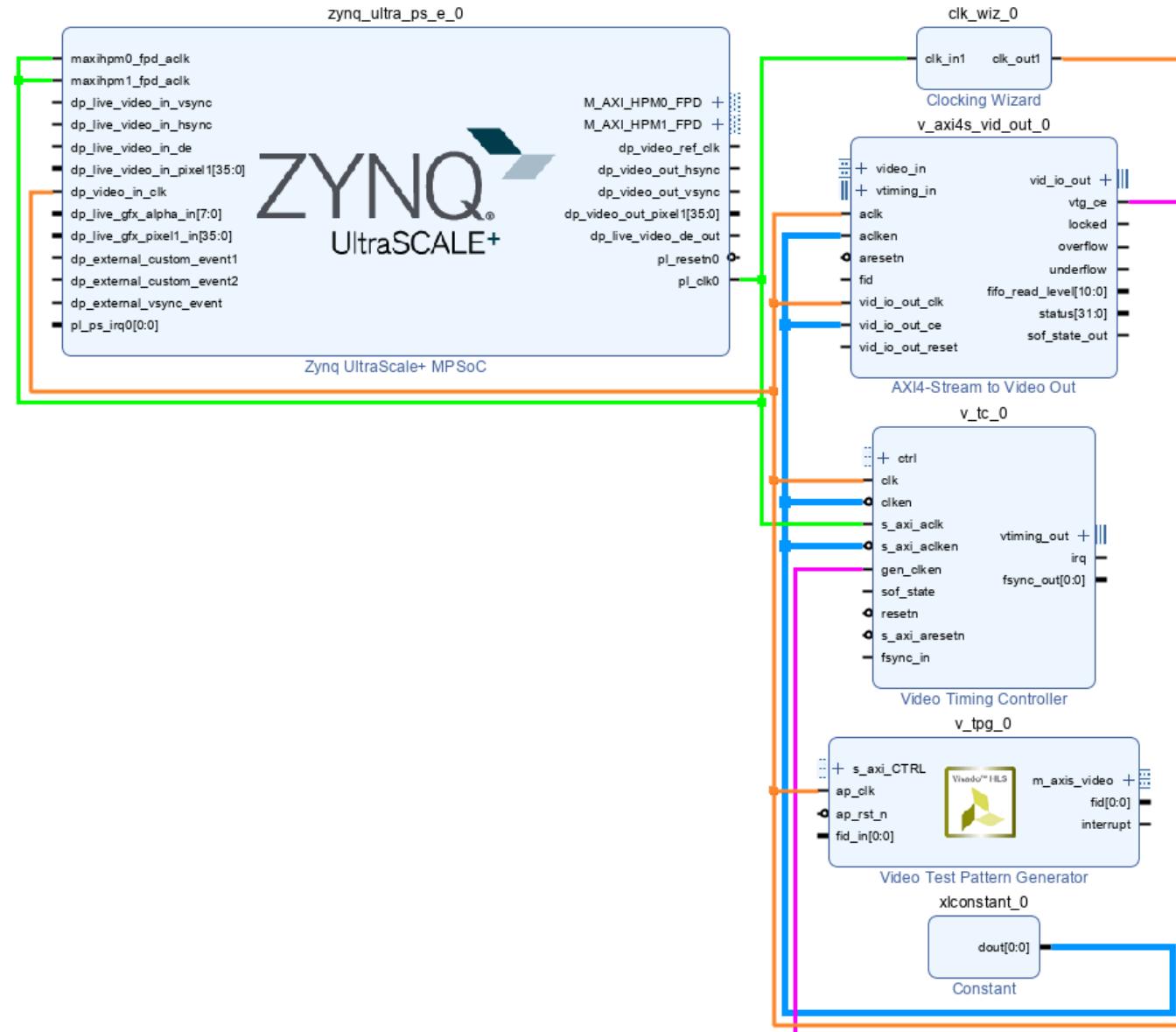
### Start Connection



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

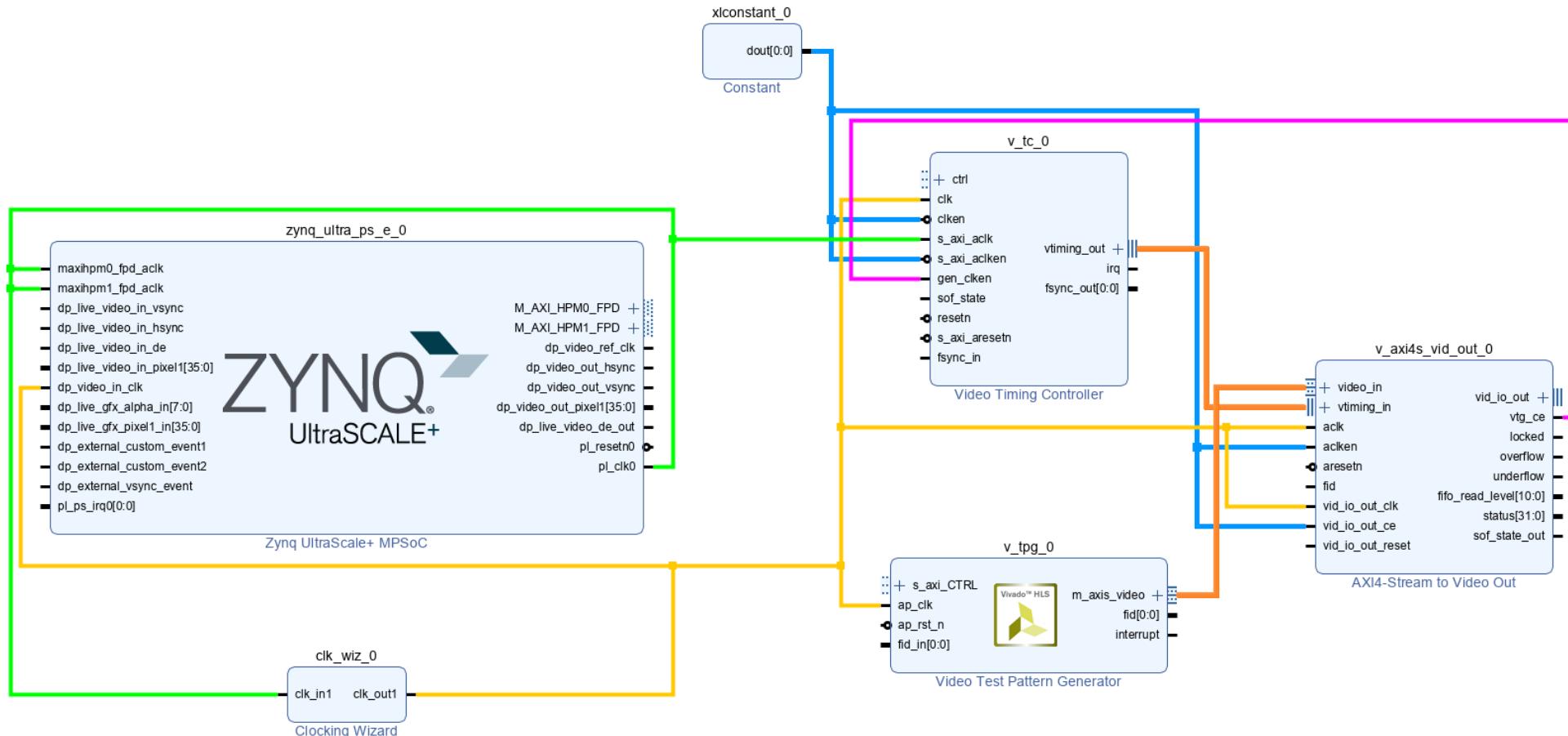
### Start Connection



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

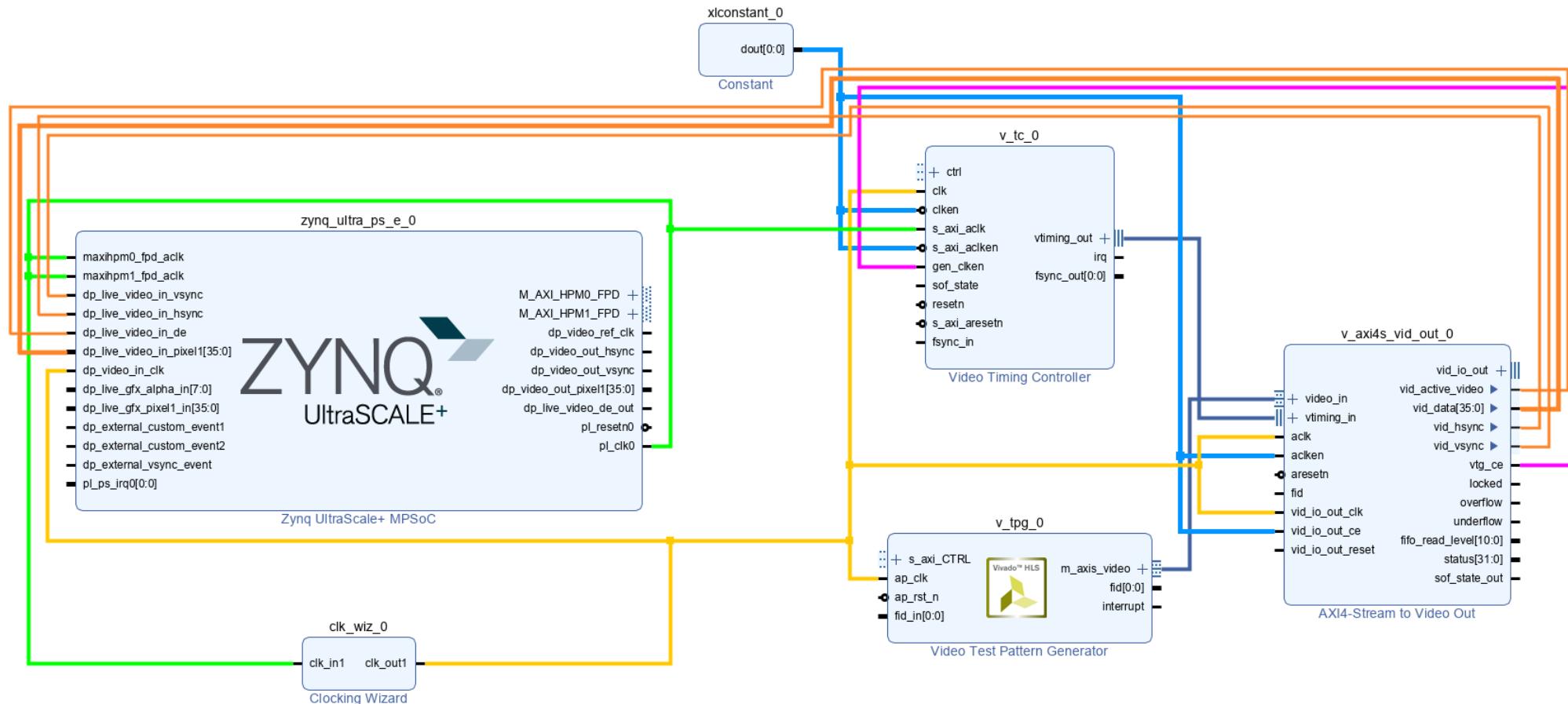
### Start Connection



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

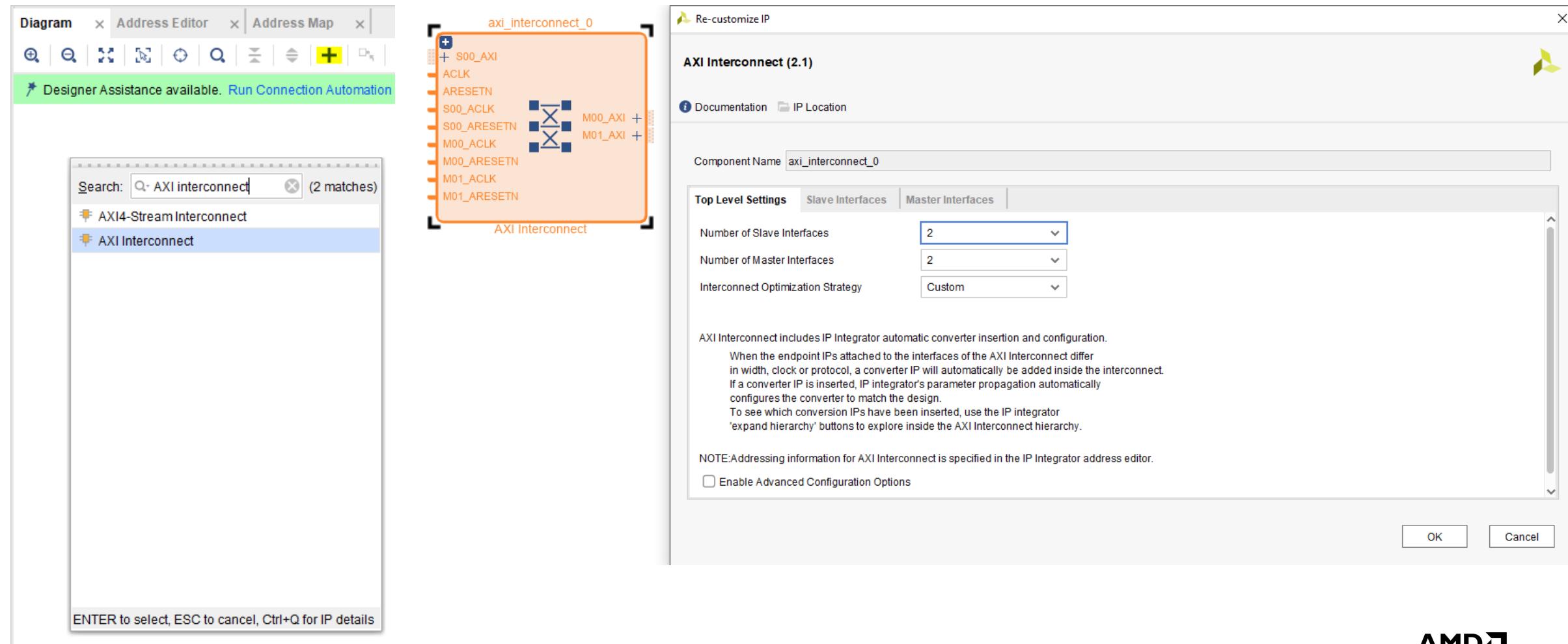
### Start Connection



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

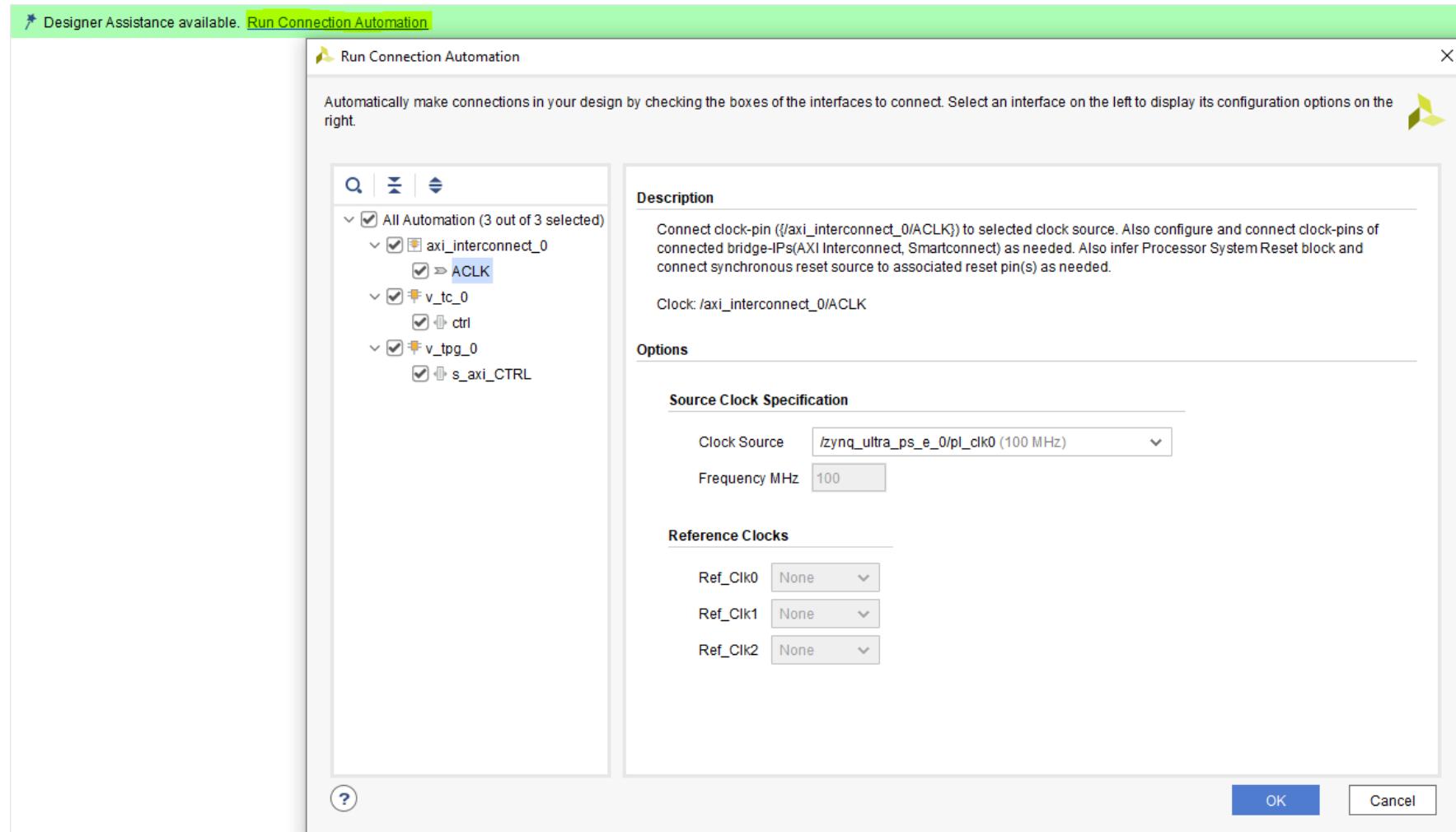
### Start Connection – Add AXI Interconnect IP



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

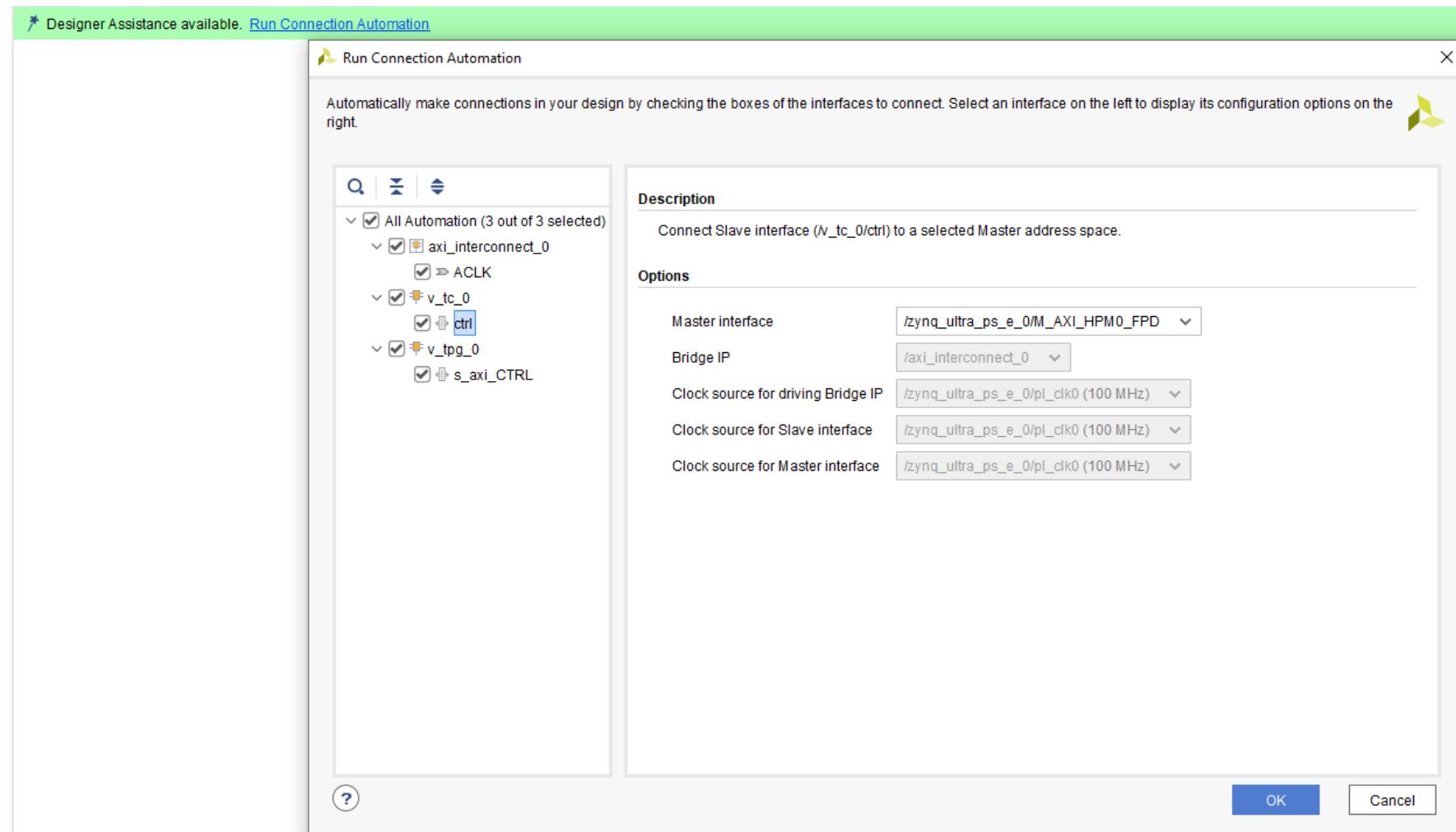
### Start Connection



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

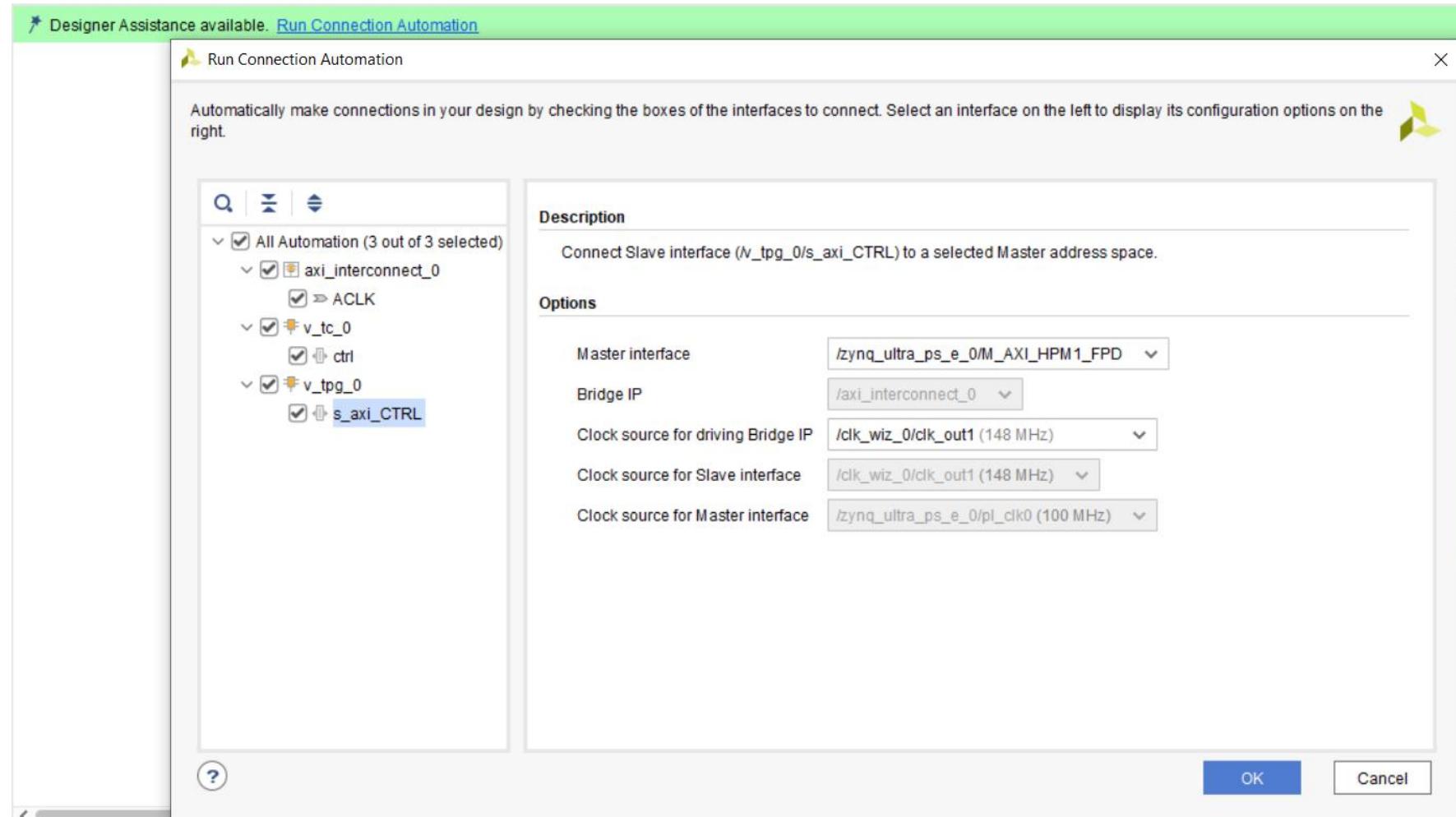
### Start Connection



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

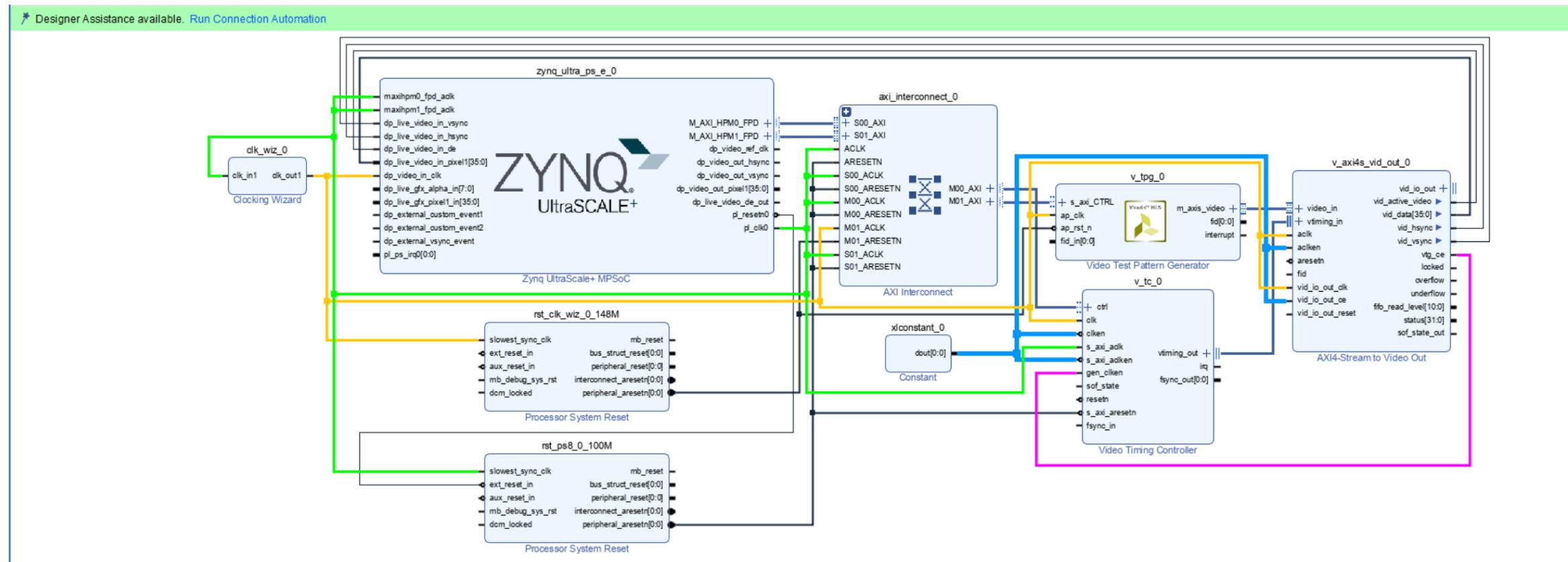
### Start Connection



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

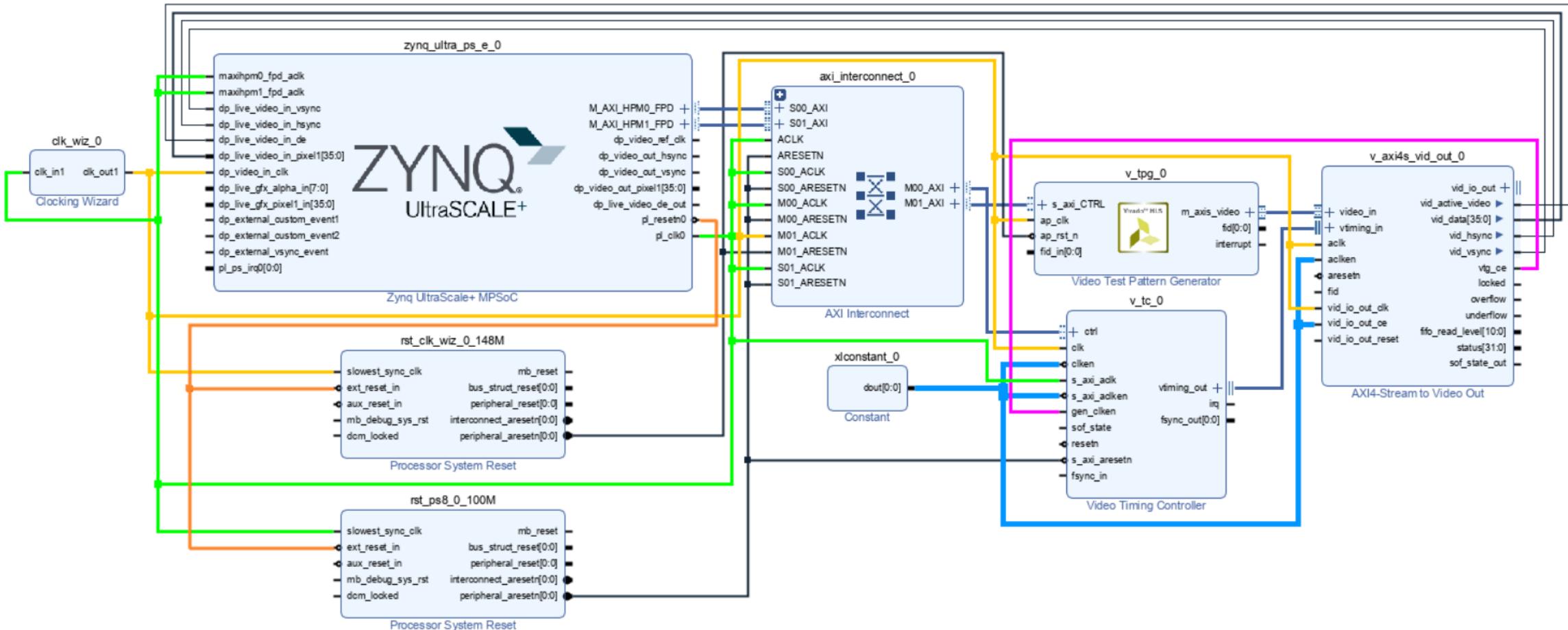
### Start Connection



# ZCU104(MPSoC) DP TPG Output Example

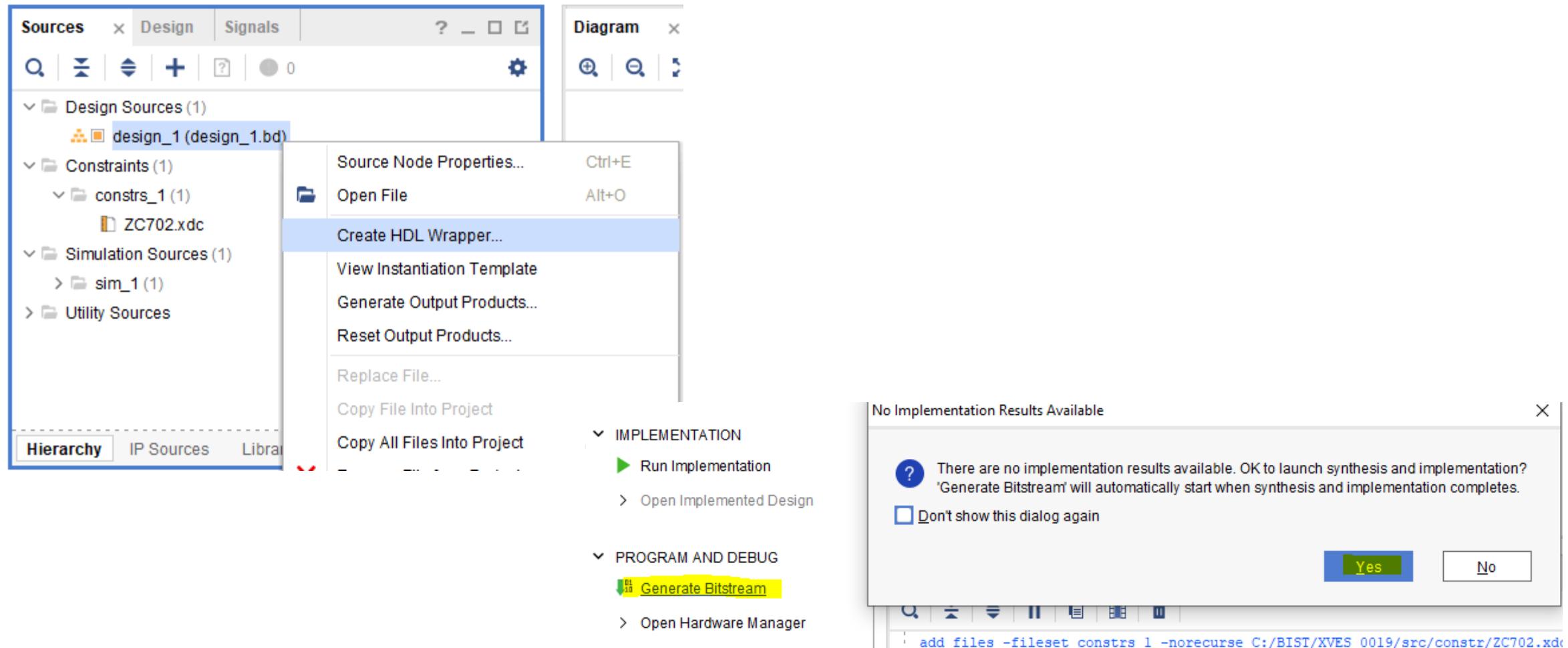
## Block Design Steps

### Start Connection



# ZCU104(MPSoC) DP TPG Output Example

## Block Design Steps

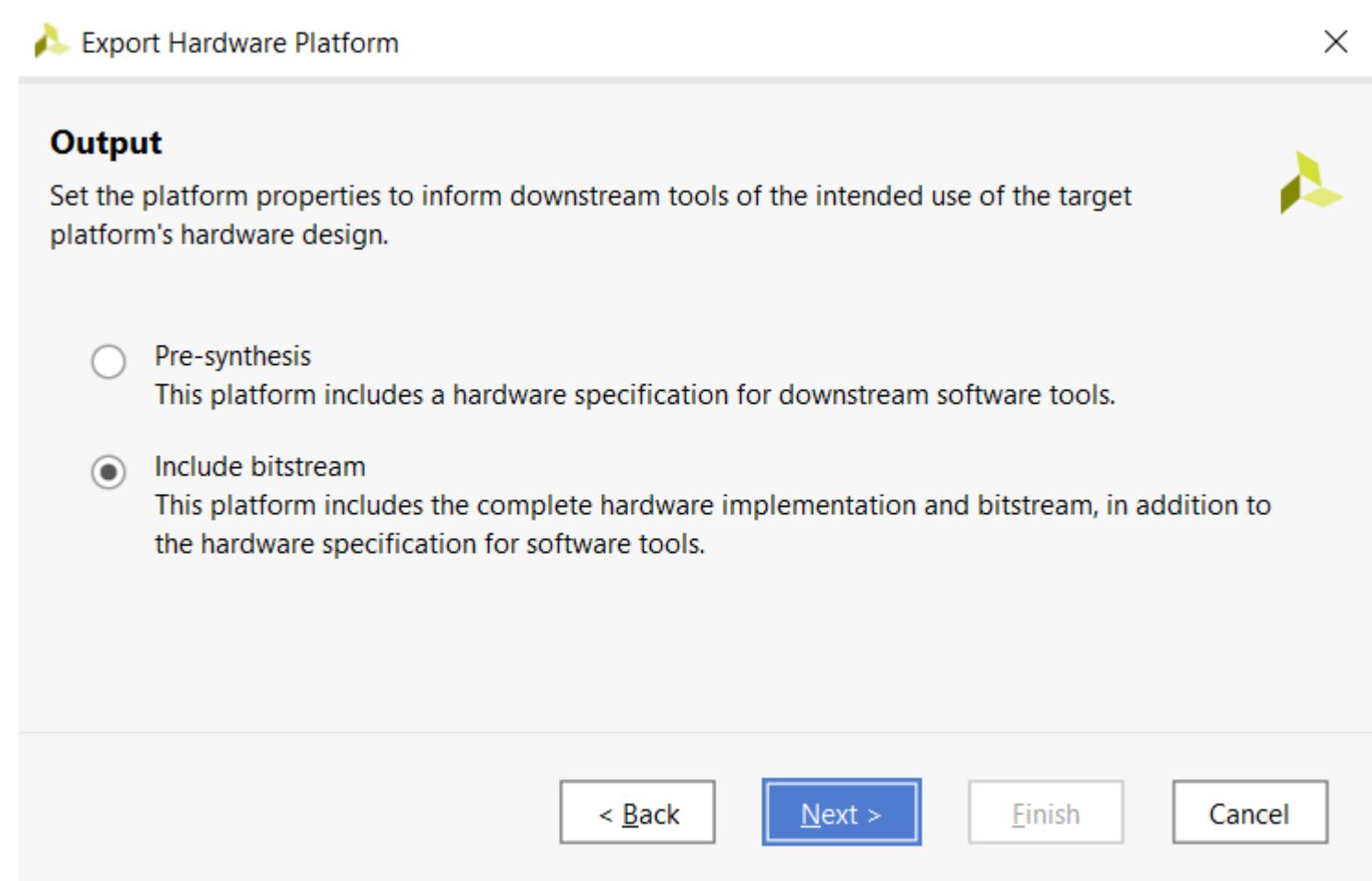
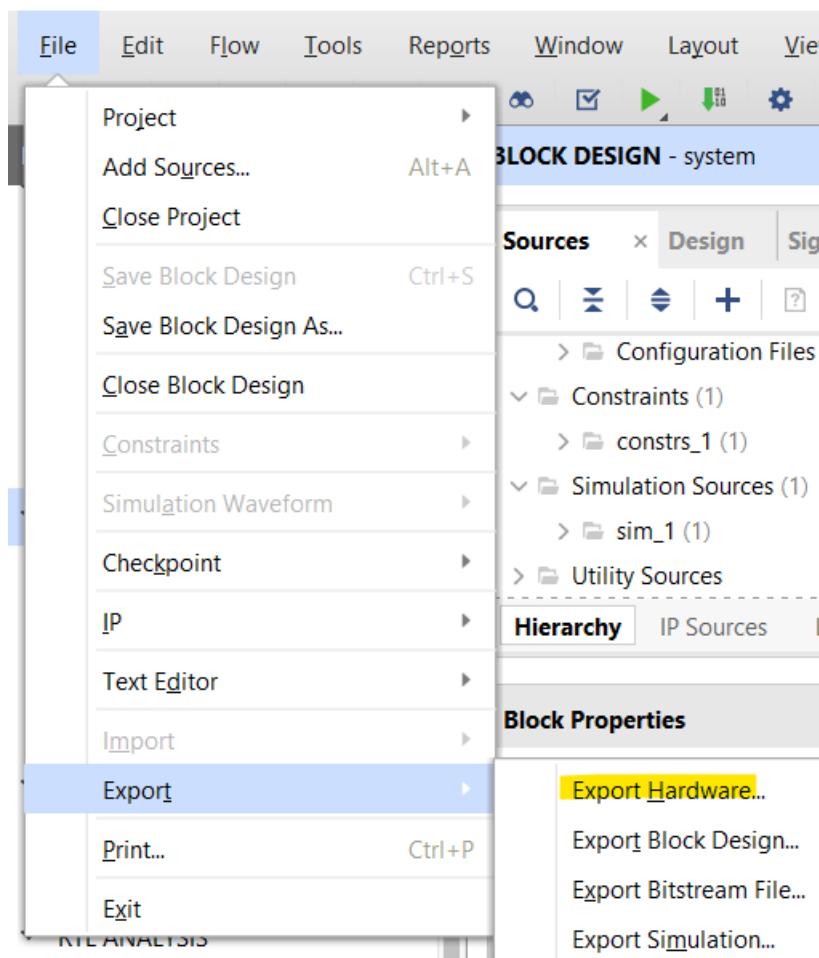




A black and white photograph showing a row of classical stone columns, likely Corinthian, standing in a straight line. The columns have fluted shafts and decorative capitals. The background is a plain, light-colored wall.

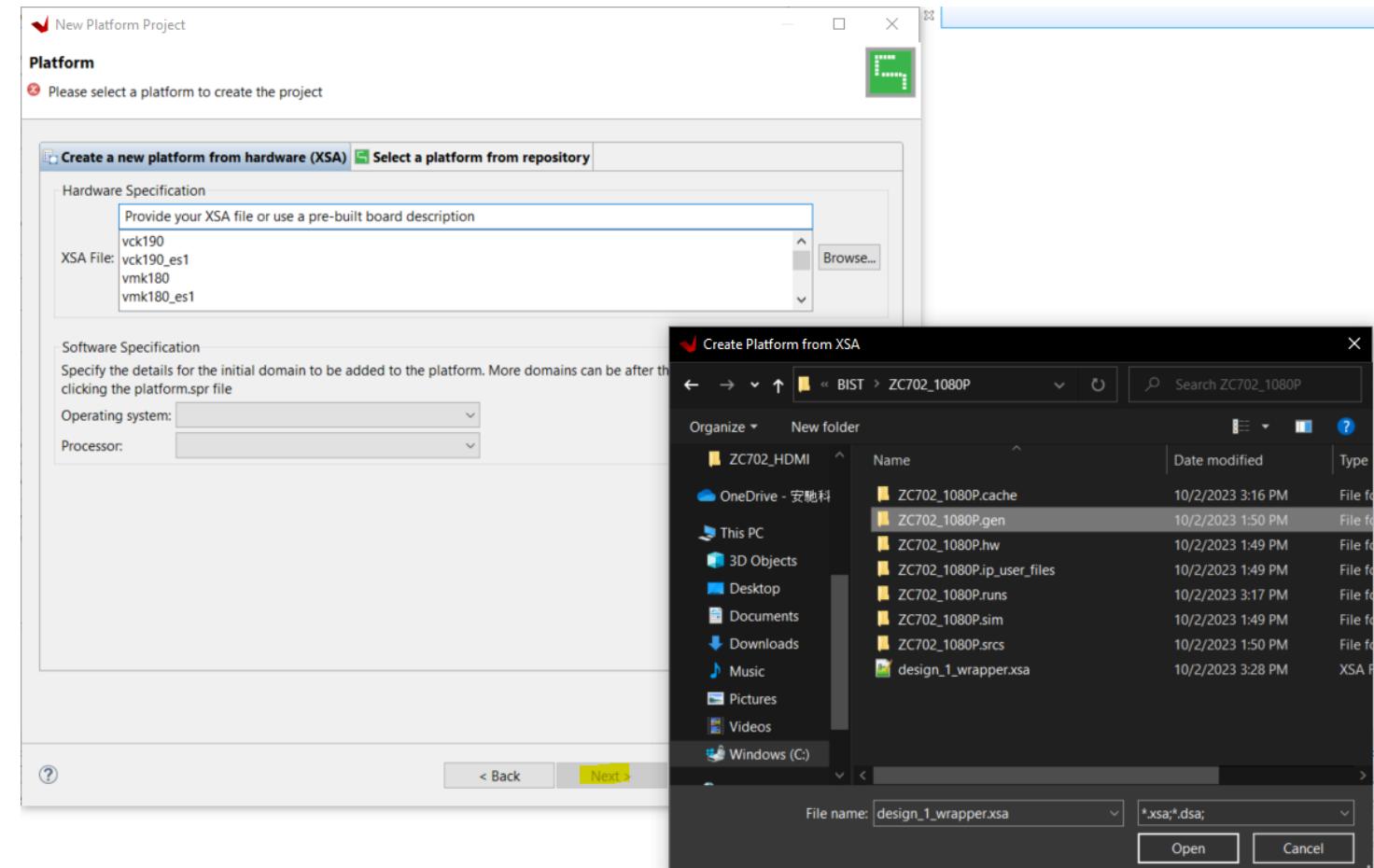
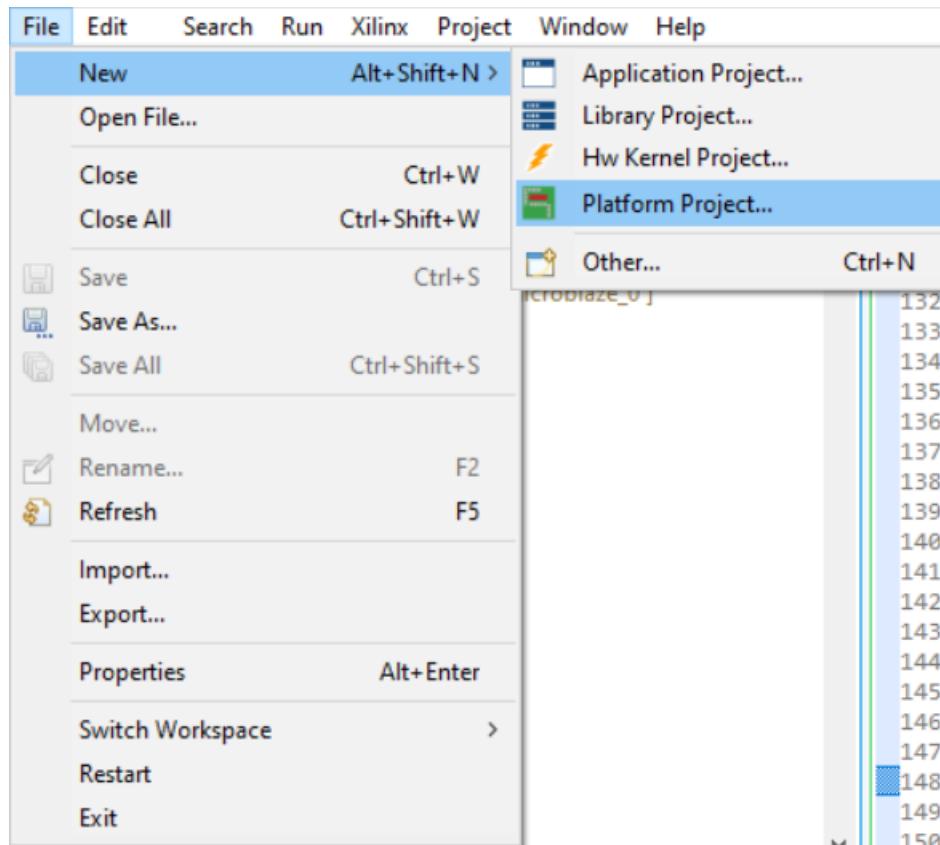
THIRTY-SEVEN  
MINUTES  
LATER....

# ZCU104(MPSoC) DP TPG Output Example



# Vitis 2021.1 Part

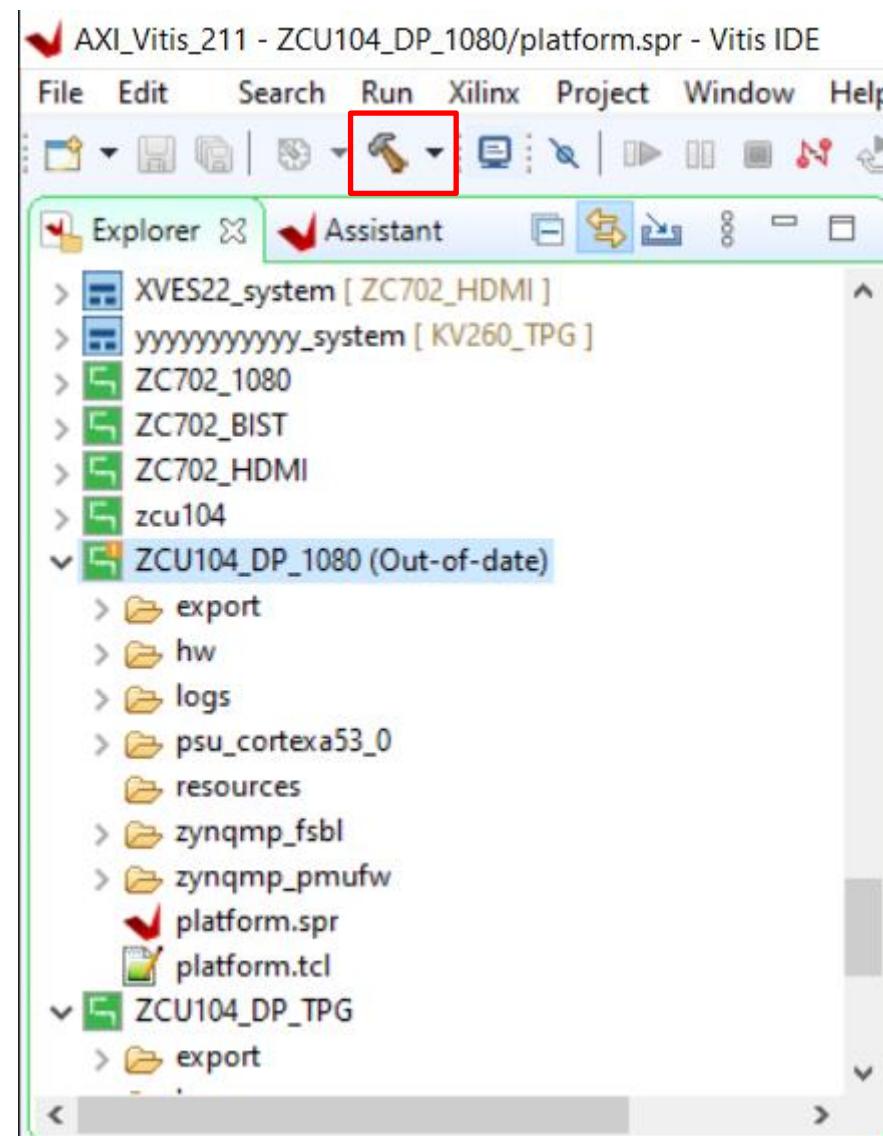
# ZCU104(MPSoC) DP TPG Output Example



\*\*\* 實際檔案請按照自己設定的位置與名稱去開啟

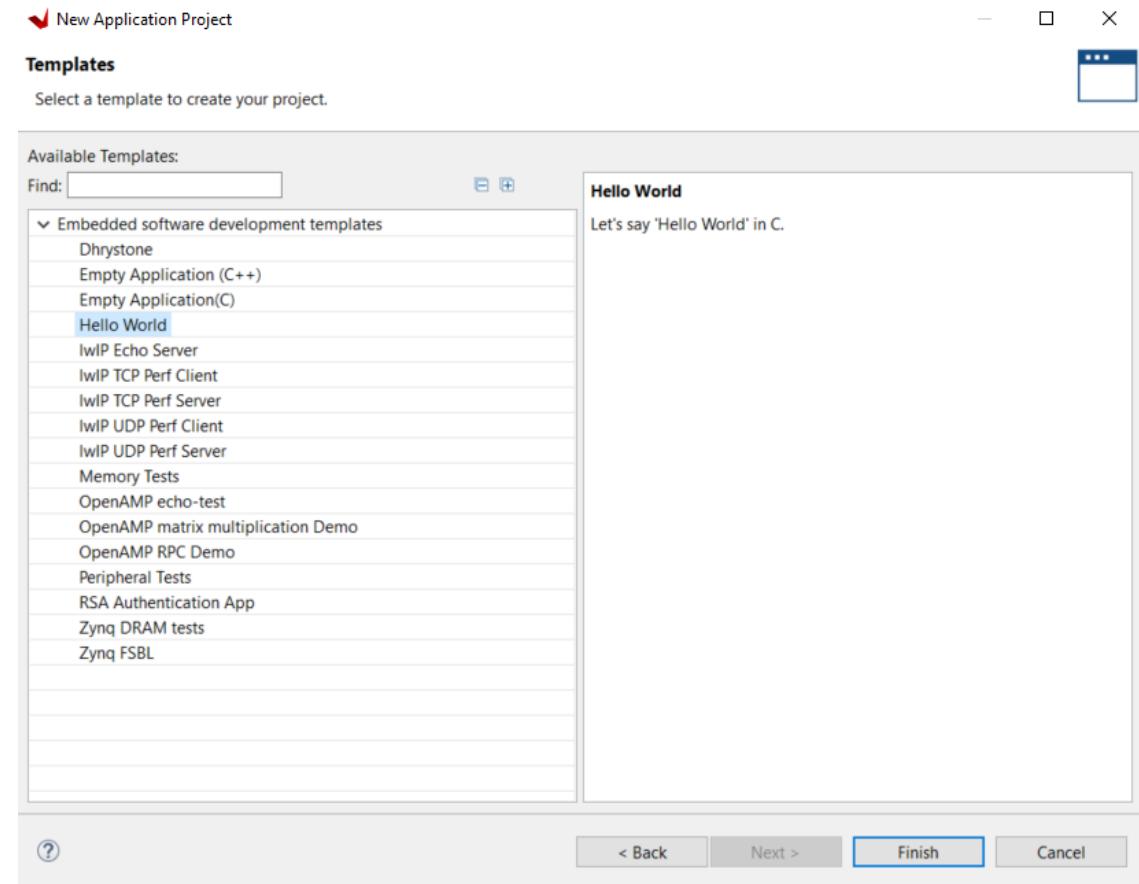
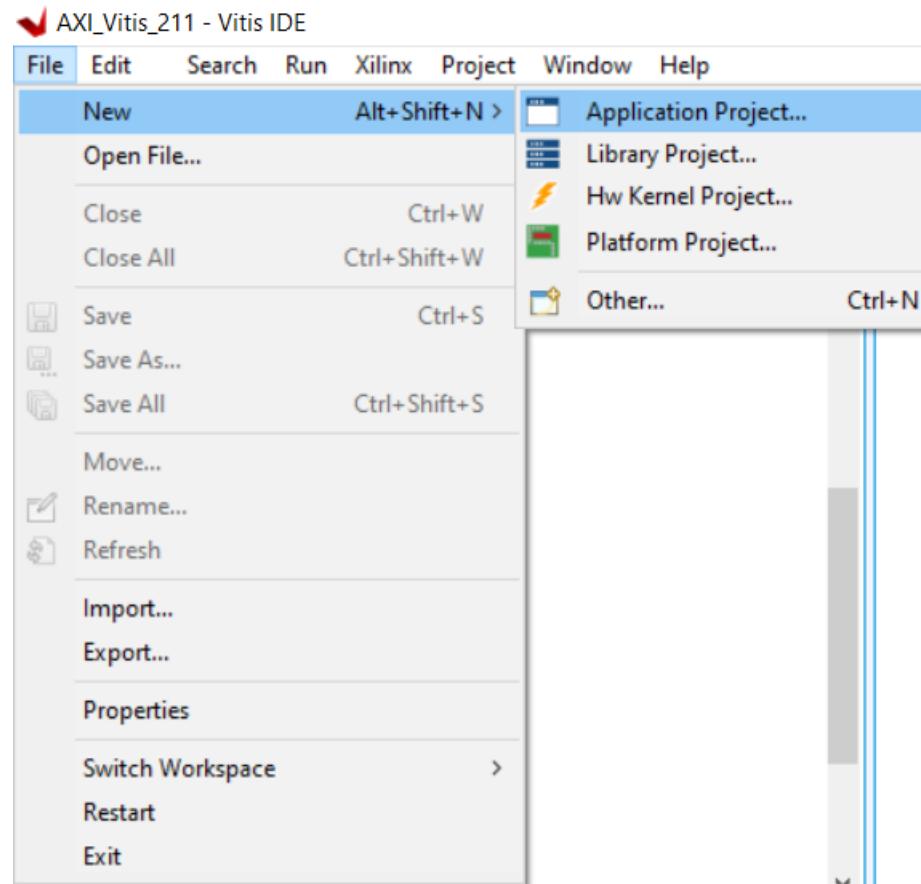
# ZCU104(MPSoC) DP TPG Output Example

記得 Build



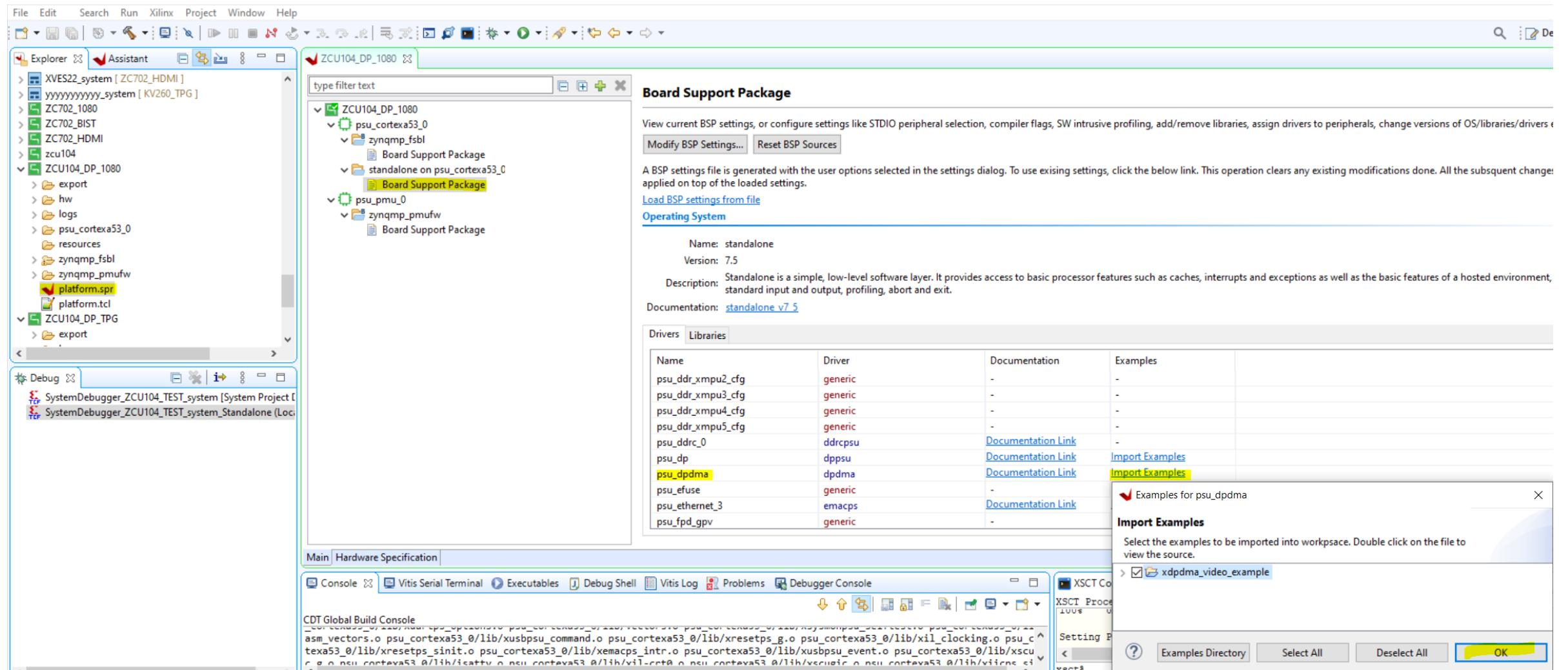
# ZCU104(MPSoC) DP TPG Output Example

這邊要開兩個 Application，一個是 Hello World，一個是 dpdma 的 example code



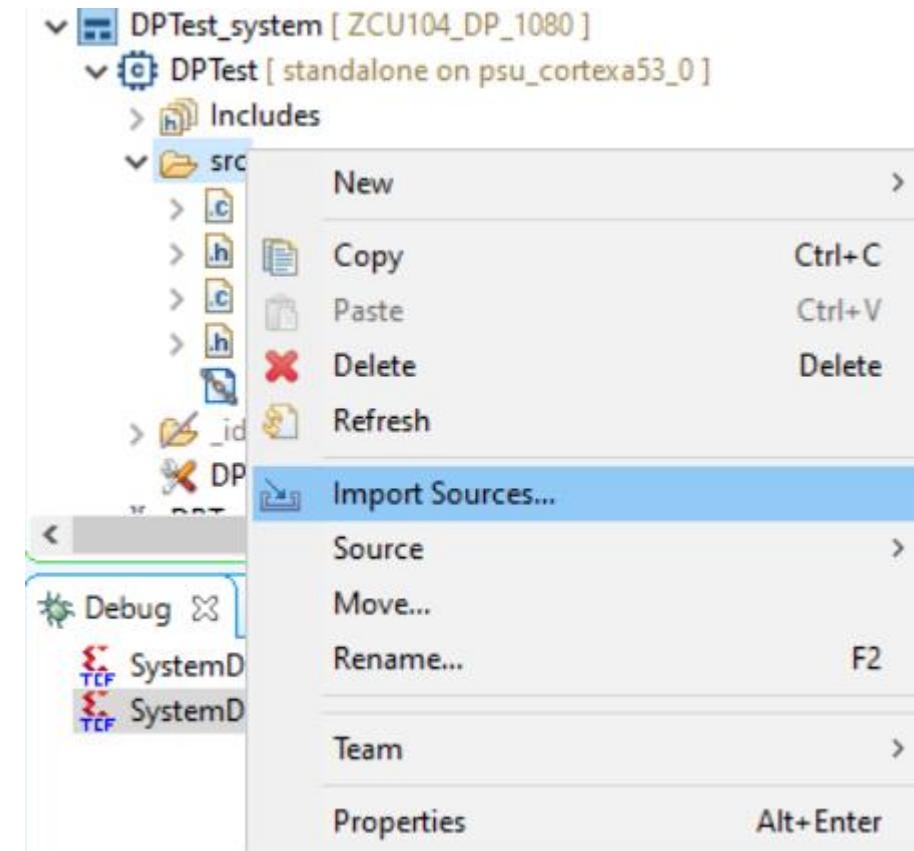
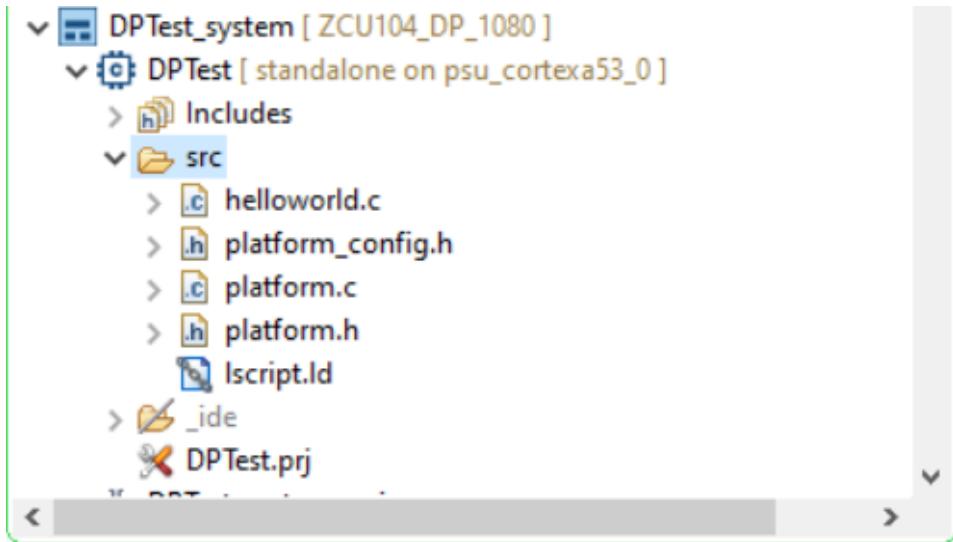
# ZCU104(MPSoC) DP TPG Output Example

這邊要開兩個 Application · 一個是 Hello World · 一個是 dpdma 的 example code



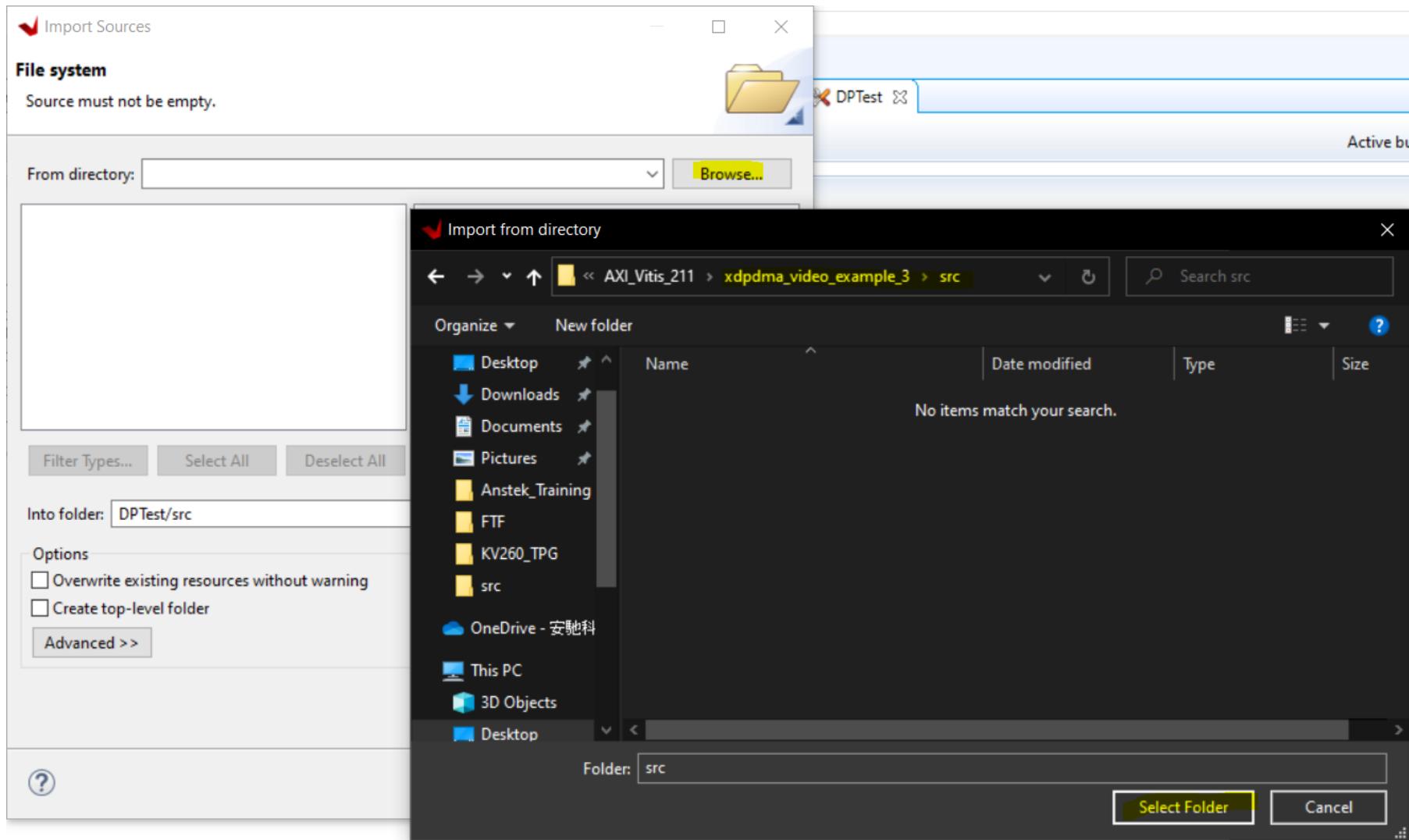
# ZCU104(MPSoC) DP TPG Output Example

到 Hello Word 的專案下 · import dpdma example code



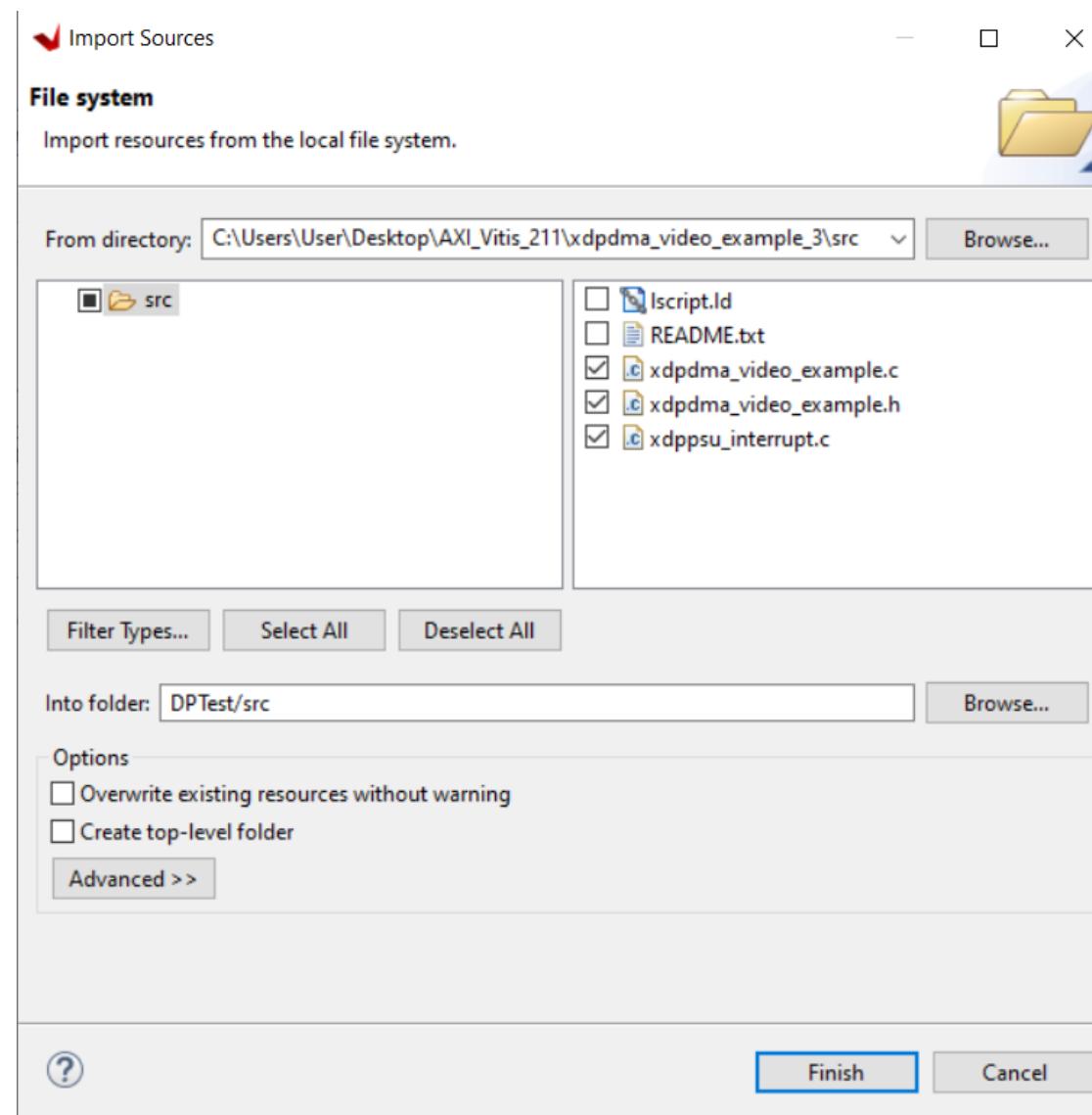
# ZCU104(MPSoC) DP TPG Output Example

到 Hello Word 的專案下 · import dpdma example code



# ZCU104(MPSoC) DP TPG Output Example

到 Hello Word 的專案下 · import dpdma example code



# ZCU104(MPSoC) DP TPG Output Example

開啟 `xpdma_video_example.c` 和 `xpdma_video_example.h` 更改 code

The screenshot shows a software development environment with two main windows:

- Explorer View:** Shows the project structure under "DPTest\_system [ ZCU104\_DP\_1080 ]". It includes subfolders like "Includes" and "SRC", which contain files such as "helloworld.c", "platform\_config.h", "platform.c", "platform.h", "xpdma\_video\_example.c", "xpdma\_video\_example.h", "xdppsu\_interrupt.c", and "lscript.ld".
- Code Editor:** Displays the content of `xpdma_video_example.c`. The code defines a function `int run_dppsu()` which disables DCache and ICache, prints a message, calls `DpdmaVideoExample`, and returns success or failure based on the status. A note at the bottom explains the purpose of the function.

```
64 //***** Type Definitions *****/
65
66 /**
67 * Main function to call the DPDMA Video example.
68 *
69 * @param    None
70 *
71 * @return   XST_SUCCESS if successful, otherwise XST_FAILURE.
72 *
73 * @note    None
74 *
75 */
76
77 int run_dppsu()
78 {
79     int Status;
80
81     Xil_DCacheDisable();
82     Xil_ICacheDisable();
83
84     xil_printf("DPDMA Generic Video Example Test \r\n");
85     Status = DpdmaVideoExample(&RunCfg);
86     if (Status != XST_SUCCESS) {
87         xil_printf("DPDMA Video Example Test Failed\r\n");
88         return XST_FAILURE;
89     }
90
91     xil_printf("Successfully ran DPDMA Video Example Test\r\n");
92
93     return XST_SUCCESS;
94 }
95
96 /**
97 *
98 * The purpose of this function is to illustrate how to use the XDpDma device
99 * driver in Graphics overlay mode.
100 */
101
```

# ZCU104(MPSoC) DP TPG Output Example

開啟 `xpdma_video_example.c` 和 `xpdma_video_example.h` 更改 code

modify

`XAVBuf_InputVideoSelect(AVBufPtr, XAVBUF_VIDSTREAM1_NONE, XAVBUF_VIDSTREAM2_NONLIVE_GFX);` to  
`XAVBuf_InputVideoSelect(AVBufPtr, XAVBUF_VIDSTREAM1_LIVE, XAVBUF_VIDSTREAM2_NONLIVE_GFX);`

# ZCU104(MPSoC) DP TPG Output Example

開啟 `xpdma_video_example.c` 和 `xpdma_video_example.h` 更改 code

The screenshot shows a software development environment with the following interface elements:

- Explorer View:** Shows the project structure under "DPTest\_system [ZCU104\_DP\_1080]". It includes "Binaries", "Includes", "Debug", and a "src" folder containing "helloworld.c", "platform\_config.h", "platform.c", "platform.h", "xpdma\_video\_example.c", "xpdma\_video\_example.h", "xdppsu\_interrupt.c", and "lscript.ld".
- Debug View:** Shows two debug sessions: "SystemDebugger\_DPTest\_system [System Project Debug]" and "SystemDebugger\_DPTest\_system\_Standalone (Local)".
- Code Editor:** Displays the content of `xpdma_video_example.c`. The code defines a function `u8 *GraphicsOverlay(u8* Frame, Run_Config *RunCfgPtr)` which iterates through the buffer indices. The line `RGB[A][Index] = 0xF00000FF;` is highlighted in blue, indicating it is selected or being edited.

```
*          rendered frame
*
* @return  Returns a pointer to the frame.
*
* @note   None.
*
*****
322 u8 *GraphicsOverlay(u8* Frame, Run_Config *RunCfgPtr)
323 {
324     u64 Index;
325     u32 *RGB[A];
326     RGB[A] = (u32 *) Frame;
327     /*
328      * Red at the top half
329      * Alpha = 0x0F
330      */
331     for(Index = 0; Index < (BUFFERSIZE/4) /2; Index++) {
332         RGB[A][Index] = 0x0F0000FF;
333     }
334     for(; Index < BUFFERSIZE/4; Index++) {
335         /*
336          * Green at the bottom half
337          * Alpha = 0xF0
338          */
339         RGB[A][Index] = 0x0F0000FF;
340     }
341 }
342 }
```

modify  
0xF000FF00 to 0x0F0000FF

# ZCU104(MPSoC) DP TPG Output Example

開啟 `xpdma_video_example.c` 和 `xpdma_video_example.h` 更改 code

The screenshot shows a software development environment with two main windows. The left window is the 'Explorer' view, displaying the project structure under 'arty50\_LED\_MIG\_system [Arty50\_RGB]'. It includes sub-folders like 'Arty50\_RGB', 'BIST\_VC707\_system [VC707\_BIST]', 'BIST\_ZC702\_system [ZC702\_BIST]', and 'DPTTest\_system [ZCU104\_DP\_1080]'. Under 'DPTTest\_system', there is a 'DPTTest' folder containing 'Includes' and 'src' sub-folders. The 'src' folder contains files such as 'helloworld.c', 'platform\_config.h', 'platform.c', 'platform.h', 'xpdma\_video\_example.c', 'xpdma\_video\_example.h', 'xdpsu\_interrupt.c', and 'lscript.ld'. The right window is the 'Code Editor' showing the content of 'xpdma\_video\_example.c'. The code includes declarations for structures like `Run_Config`, function prototypes for `int run_dppsu()` and `DpdmaVideoExample`, and comments for variable definitions.

```
/*-----[Types]-----*/
typedef struct {
    XDpPsu *DpPsuPtr;
    XScuGic *IntrPtr;
    XAVBuf *AVBufPtr;
    XDpDma *DpDmaPtr;

    XVidC_VideoMode VideoMode;
    XVidC_ColorDepth Bpc;
    XDpPsu_ColorEncoding ColorEncode;

    u8 UseMaxLaneCount;
    u8 UseMaxLinkRate;
    u8 LaneCount;
    u8 LinkRate;
    u8 UseMaxCfgCaps;
    u8 EnSynchClkMode;

    u32 PixClkHz;
} Run_Config;

/********************* Function Prototypes *****************/
int run_dppsu();

int DpdmaVideoExample(Run_Config *RunCfgPtr);
void InitRunConfig(Run_Config *RunCfgPtr);
int InitDpDmaSubsystem(Run_Config *RunCfgPtr);
void SetupInterrupts(Run_Config *RunCfgPtr);
u8* GraphicsOverlay(u8* Frame, Run_Config *RunCfgPtr);

/* DisplayPort interrupt related functions */
void DpPsu_SetupVideoStream(Run_Config *RunCfgPtr);

void DpPsu_Run(Run_Config *RunCfgPtr);
void DpPsu_IsrHpdEvent(void *ref);
void DpPsu_IsrHpdPulse(void *ref);

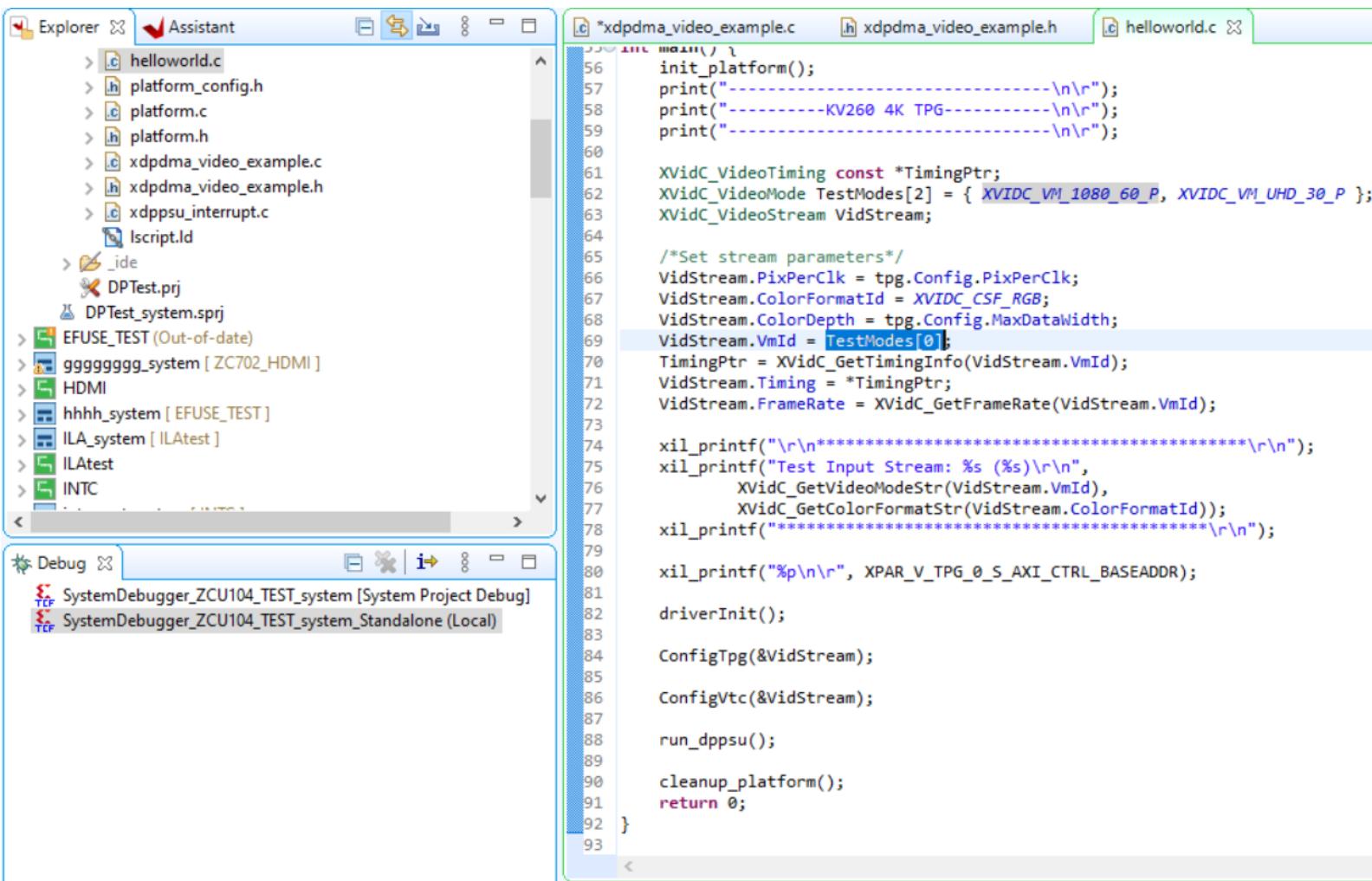
/********************* Variable Definitions *****************/
<
```

# ZCU104(MPSoC) DP TPG Output Example

更改 helloworld.c code，可以參考以下這篇

<https://www.hackster.io/nikilthapa/4k-tpg-video-streaming-in-kria-kv260-baremetal-part-2-62fca5>

因為是 1920x1080，記得修改一下 code 如下：



The screenshot shows the Quartus Prime IDE interface. The left pane displays the project structure under 'Explorer' with files like helloworld.c, platform\_config.h, platform.c, platform.h, xdpdma\_video\_example.c, xdpdma\_video\_example.h, xdppsu\_interrupt.c, and lscript.ld. Below that is the '\_ide' section with DPTTest.prj and DPTTest\_system.sprj. The bottom-left pane shows the 'Debug' window with two entries: SystemDebugger\_ZCU104\_TEST\_system [System Project Debug] and SystemDebugger\_ZCU104\_TEST\_system\_Standalone (Local). The right pane is the 'Source Editor' showing the content of helloworld.c. The code initializes the platform, prints system information, sets up a video stream with timing parameters, and prints stream details. A specific line of code is highlighted: VidStream.VmId = testModes[0];. The code also includes comments for setting stream parameters and printing stream details.

```
main()\n{\n    init_platform();\n    print("-----\n-----KV260 4K TPG-----\n-----\n");\n\n    XVidC_VideoTiming const *TimingPtr;\n    XVidC_VideoMode TestModes[2] = { XVIDC_VM_1080_60_P, XVIDC_VM_UHD_30_P };\n    XVidC_VideoStream VidStream;\n\n    /*Set stream parameters*/\n    VidStream.PixPerClk = tpg.Config.PixPerClk;\n    VidStream.ColorFormatId = XVIDC_CSF_RGB;\n    VidStream.ColorDepth = tpg.Config.MaxDataWidth;\n    VidStream.VmId = testModes[0];\n    TimingPtr = XVidC_GetTimingInfo(VidStream.VmId);\n    VidStream.Timing = *TimingPtr;\n    VidStream.FrameRate = XVidC_GetFrameRate(VidStream.VmId);\n\n    xil_printf("\r\n*****\r\n");\n    xil_printf("Test Input Stream: %s (%s)\r\n",\n              XVidC_GetVideoModeStr(VidStream.VmId),\n              XVidC_GetColorFormatStr(VidStream.ColorFormatId));\n    xil_printf("*****\r\n");\n\n    xil_printf("%p\r\n", XPAR_V_TPG_0_S_AXI_CTRL_BASEADDR);\n\n    driverInit();\n\n    ConfigTpg(&VidStream);\n\n    ConfigVtc(&VidStream);\n\n    run_dppsu();\n\n    cleanup_platform();\n\n    return 0;\n}
```

# ZCU104(MPSoC) DP TPG Output Example

## Build and Run

The screenshot shows the Vitis IDE interface with the following components:

- Explorer View:** Shows the project structure under "DPTest\_system [ ZCU104\_DP\_1080 ]". The "src" folder contains files: helloworld.c, platform\_config.h, platform.c, platform.h, xdpdma\_video\_example.c, xdpdma\_video\_example.h, xdppsu\_interrupt.c, lscript.ld, .ide, DPTest.prj, and Debug. It also lists "Binaries" and "Includes".
- Code Editor:** Displays the content of `xdpdma_video_example.c`. The code includes initialization of the platform, setting up a VideoStream, and printing configuration details like "KV260 4K TPG" and "XVIDC\_VM\_1080\_60\_P".
- Debug View:** Shows the "SystemDebugger\_ZCU104\_TEST\_system [System Project Debug]" and "SystemDebugger\_ZCU104\_TEST\_system\_Standalone (Local)" configurations.
- Console View:** Shows the CDT Global Build Console output. It indicates a build finished at 11:13:06, took 15.318ms, and generated a Xilinx Project File (ZCU104\_DP\_1080.xpf). It also shows the creation of a BOOT.BIN file and the execution of bootgen.

# ZCU104 Hardware Setting



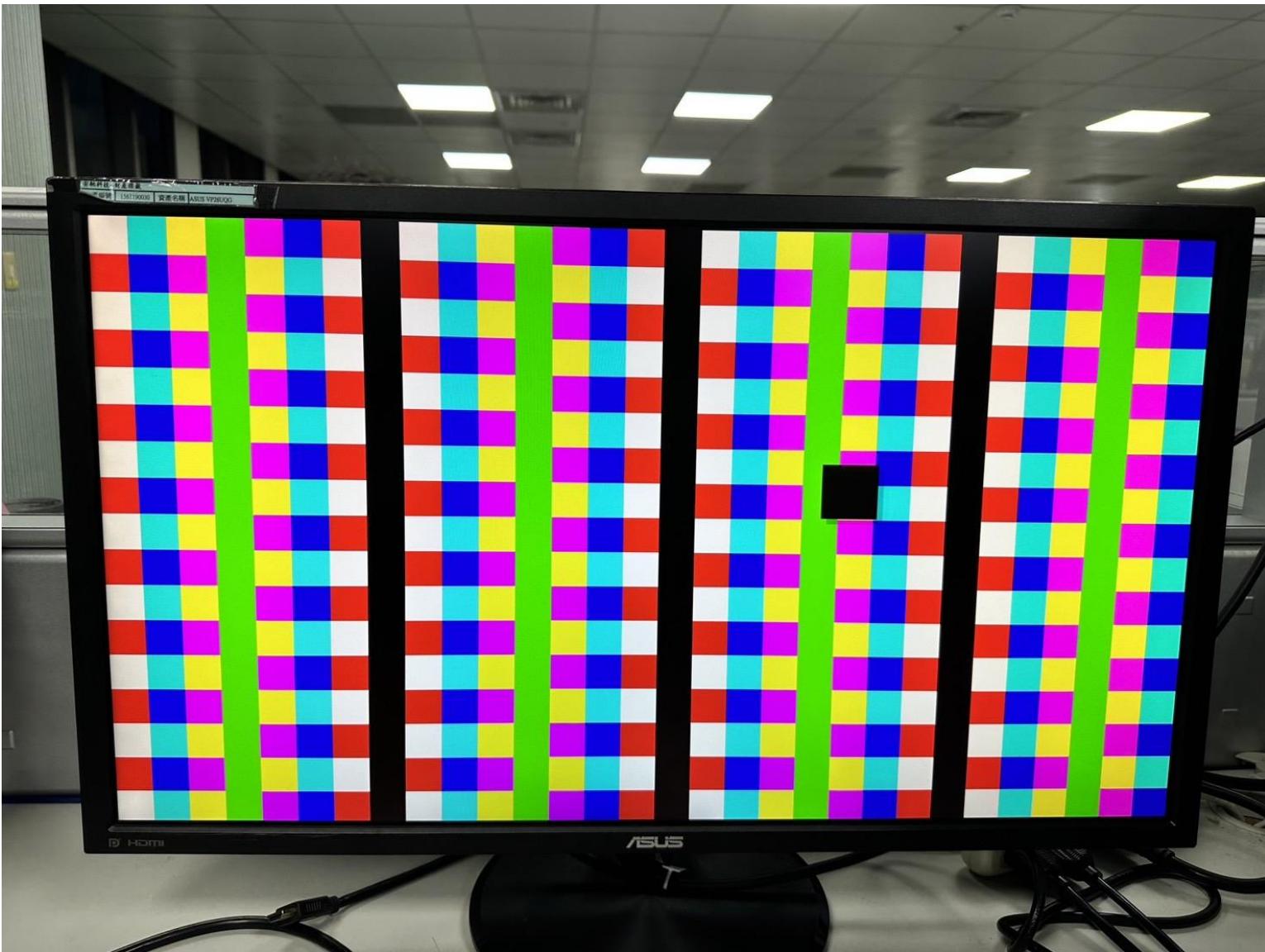
# ZCU104(MPSoC) DP TPG Output Example

```
Xilinx Zynq MP First Stage Boot Loader
Release 2021.1  Oct 12 2023 - 15:46:07
PMU-FW is not running, certain applications may not be supported.
-----
-----KV260 4K TPG-----
-----

*****
Test Input Stream: 1920x1080@60Hz (RGB)
*****
A0010000
DPDMA Generic Video Example Test
Generating Overlay.....
HPD event ..... ! Connected.
Lane count =    2
Link rate =    20

Starting Training ...
    ! Training succeeded.
DONE!
..... HPD event
Successfully ran DPDMA Video Example Test
```

# ZCU104(MPSoC) DP TPG Output Example



# Reference

- <https://www.hackster.io/nikilthapa/4k-tpg-video-streaming-in-kria-kv260-baremetal-part-1-c0c9d6>
- <https://www.hackster.io/nikilthapa/4k-tpg-video-streaming-in-kria-kv260-baremetal-part-2-62fca5>
- <https://www.hackster.io/news/microzed-chronicles-displayport-controller-part-one-25734db13fad>
- <https://www.hackster.io/news/microzed-chronicles-displayport-controller-part-two-1fa042f7a242>
- [https://github.com/ATaylorCEngFIET/Ultra96V2\\_DisplayPort/tree/master/display\\_port/display\\_port.sdk/dispport/src](https://github.com/ATaylorCEngFIET/Ultra96V2_DisplayPort/tree/master/display_port/display_port.sdk/dispport/src)

**AMD**