



VPK120 BEAM & System Controller

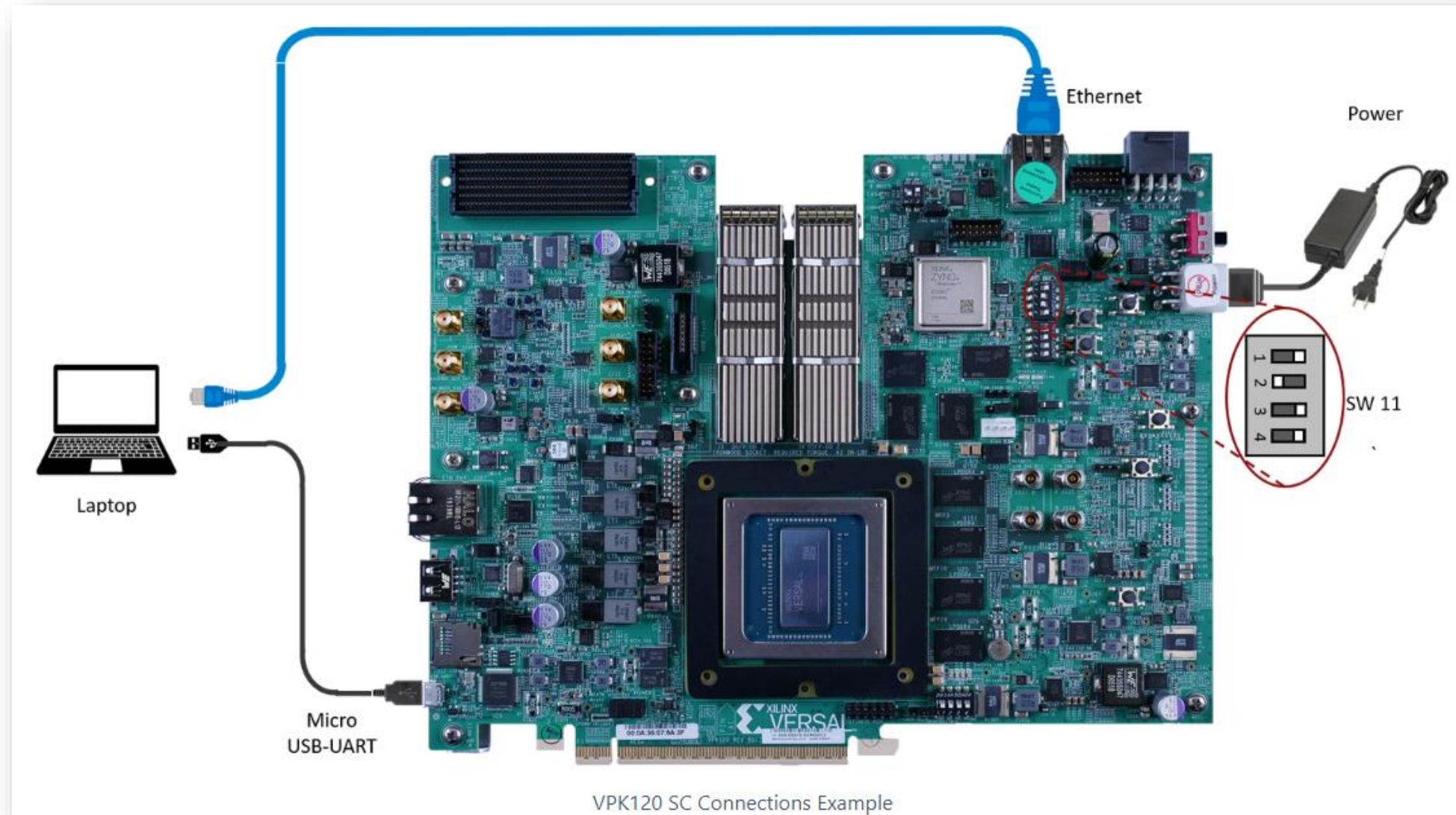
BEAM

BEAM

BEAM is a web based GUI application to monitor and modify parameters of the evaluation board. The BEAM web page connects to a web server running on the system controller and provides a home screen which provides navigation to board specific test interfaces and related product pages.

The screenshot displays the Xilinx BEAM web interface. At the top, the Xilinx logo and the title "Board Evaluation and Management" are visible. A navigation bar includes links for "Help", "About", and "Home". The main heading reads "Welcome & Get Started with Versal AI Core Series VCK190 Evaluation Kit". The central content area features a large image of the VCK190 evaluation board. To the left of the board image, there is a smaller image of the Versal AI Core chip with the text "XILINX VERSAL AI CORE" and "Industry's First ACAP". Below this, a red button labeled "About Versal ACAP" is present. To the right of the board image, the Xilinx Versal logo is shown, followed by the text "Industry's First ACAP" and "Adaptive Compute Acceleration Platform". Below this text is a red button labeled "Visit Product Page". On the right side of the interface, a vertical sidebar contains four buttons: "Test The Board", "Obtain linux Prompts", "Run Demos & Designs", and "Develop using Tools". The "Obtain linux Prompts" button has a right-pointing arrow next to it.

Board setup and Connections



Board setup and Connections

1. Of the three COM ports that are assigned when connecting a cable to the debug port, connect your terminal program to the highest com port. Configure the port with 115200,8,n,1.
2. The board and Windows PC with Ethernet can be connected directly. Alternatively, the board can be in a network with a DHCP server running to provide the address.
3. Login to the system controller using the serial terminal using the username **petalinux** and if prompted for a password, enter the password that you set up for the first time login.
4. For the first time login, there will be a prompt to set a password. Set a password that you can remember for the next login.

```
[ 19.745177] TCP: request_sock_TCP: Possible SYN flooding on port 0
.[ 25.157128] scwebun.sh[1592]: rm: can't remove '/home/pe
[ 25.630991] audit: type=1006 audit(4290772493.043:2): pid=
[ 25.643704] audit: type=1300 audit(4290772493.043:2): arch
id=0 euid=0 suid=0 fsuid=0 egid=0 sgid=0 fsgid=0 tty=(none) s
[ 25.669498] audit: type=1327 audit(4290772493.043:2): proc
.....
*****
*
*      BEAM Tool Web Address      *
*
*      No IP address is assigned  *
*
*****
```

Board setup and Connections

For some boards shipping from the factory, a login for the system controller console session will not appear, but instead the following banner appears in the console output:

```
*****
*   Enter these key-sequence to exit Board Framework   *
*                                                         *
*               EXT<Enter key><Tab key>                  *
*****
```

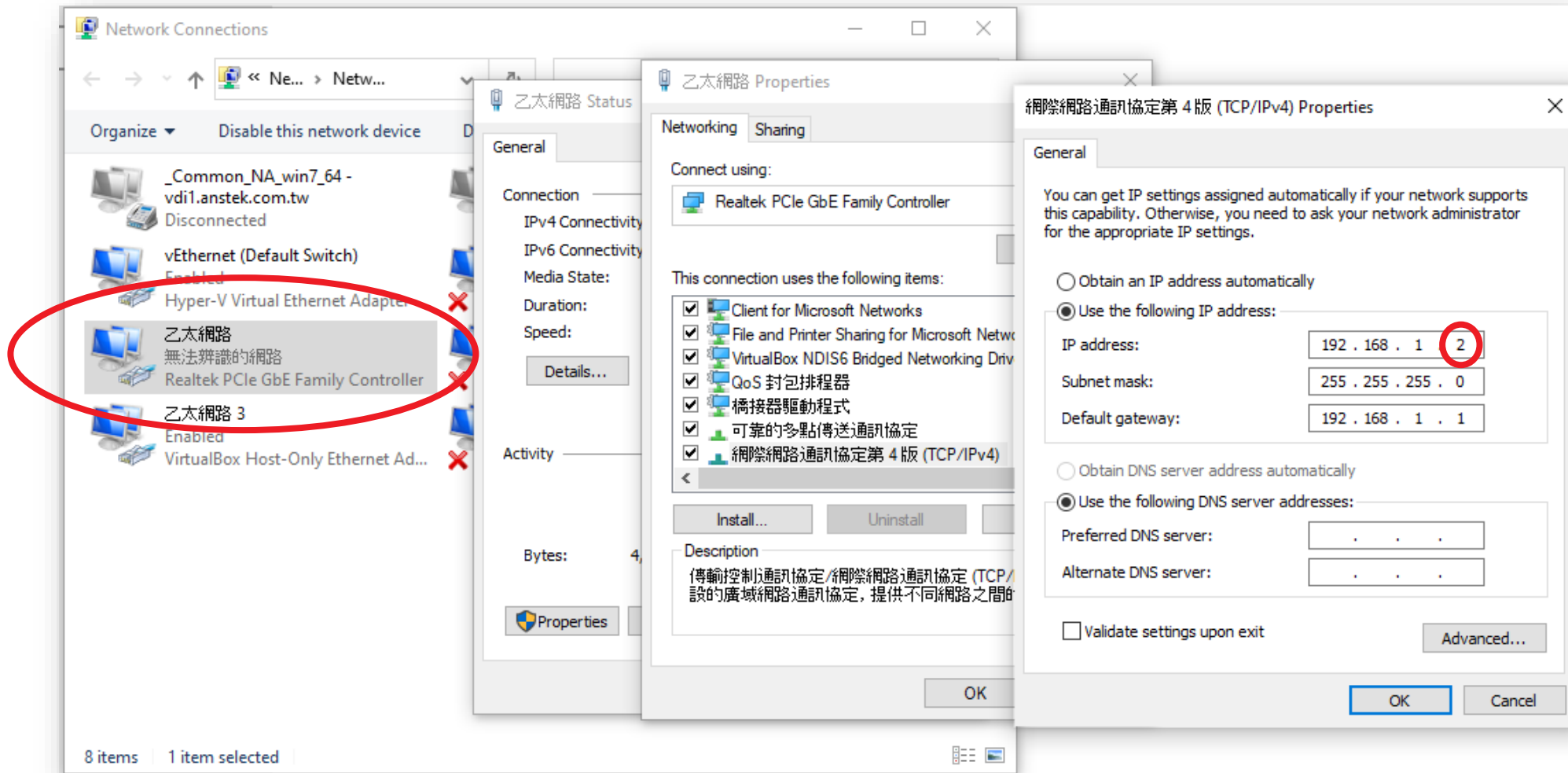
Enter the keyboard sequence as indicated EXT<Enter key><Tab key> to gain access to the command prompt.

```
*****
*   Enter these key-sequence to exit Board Framework   *
*                                                         *
*               EXT<Enter key><Tab key>                  *
*****
[ 54.108846] TCP: request_sock_TCP: Possible SYN flooding on port 2542. Sending cookies.  Check SNMP counters.
Connect to this XSDB server use host xilinx-versal-system-controller-2021_2 and port 54321
[ 54.62 ]      DONE
Starting tcf-agent: OK

root@xilinx-versal-system-controller-2021_2:~#
```


Windows PC IP Settings

Make sure that the last digit of the IP Address on the Windows PC is different to what is being set on the Board.



Board IP Setting

enter the below command to override the IP address configured through the DHCP and to set the required static IP in the target board. use the below command to set the IP:

```
sudo ifconfig eth0 192.168.1.11
```

Verify/check the IP address of the board on the session.

```
sudo ifconfig
```

Ping the Windows PC with the below command via the session.

Press Ctrl + C to stop ping on session.

```
ping <host_ip>
```

Ex: ping 192.168.1.11

```
*****
*
*      BEAM Tool Web Address      *
*
*      No IP address is assigned  *
*
*****

xilinx-versal-system-controller-20222 login: petalinux
Password:
[  94.978260] audit: type=1006 audit(4290772562.391:3): pid=3127 uid=0 old-auid=42949
[  94.990967] audit: type=1300 audit(4290772562.391:3): arch=c00000b7 syscall=64 succ
id=0 euid=0 suid=0 fsuid=0 egid=0 sgid=0 fsgid=0 tty=(none) ses=2 comm="(systemd)" exe
[  95.016684] audit: type=1327 audit(4290772562.391:3): proctitle="(systemd)"
xilinx-versal-system-controller-20222:~$ sudo ifconfig eth0 192.168.1.11
Password:
xilinx-versal-system-controller-20222:~$ sudo ifconfig
eth0      Link encap:Ethernet  HWaddr CE:82:0D:94:18:31
          inet addr:192.168.1.11  Bcast:192.168.1.255  Mask:255.255.255.0
          inet6 addr: fe80::cc82:dff:fe94:1831/64 Scope:Link
          UP BROADCAST RUNNING MULTICAST  MTU:1500  Metric:1
          RX packets:142  errors:0  dropped:0  overruns:0  frame:0
          TX packets:42  errors:0  dropped:0  overruns:0  carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:8391 (8.1 KiB)  TX bytes:5463 (5.3 KiB)
          Interrupt:38

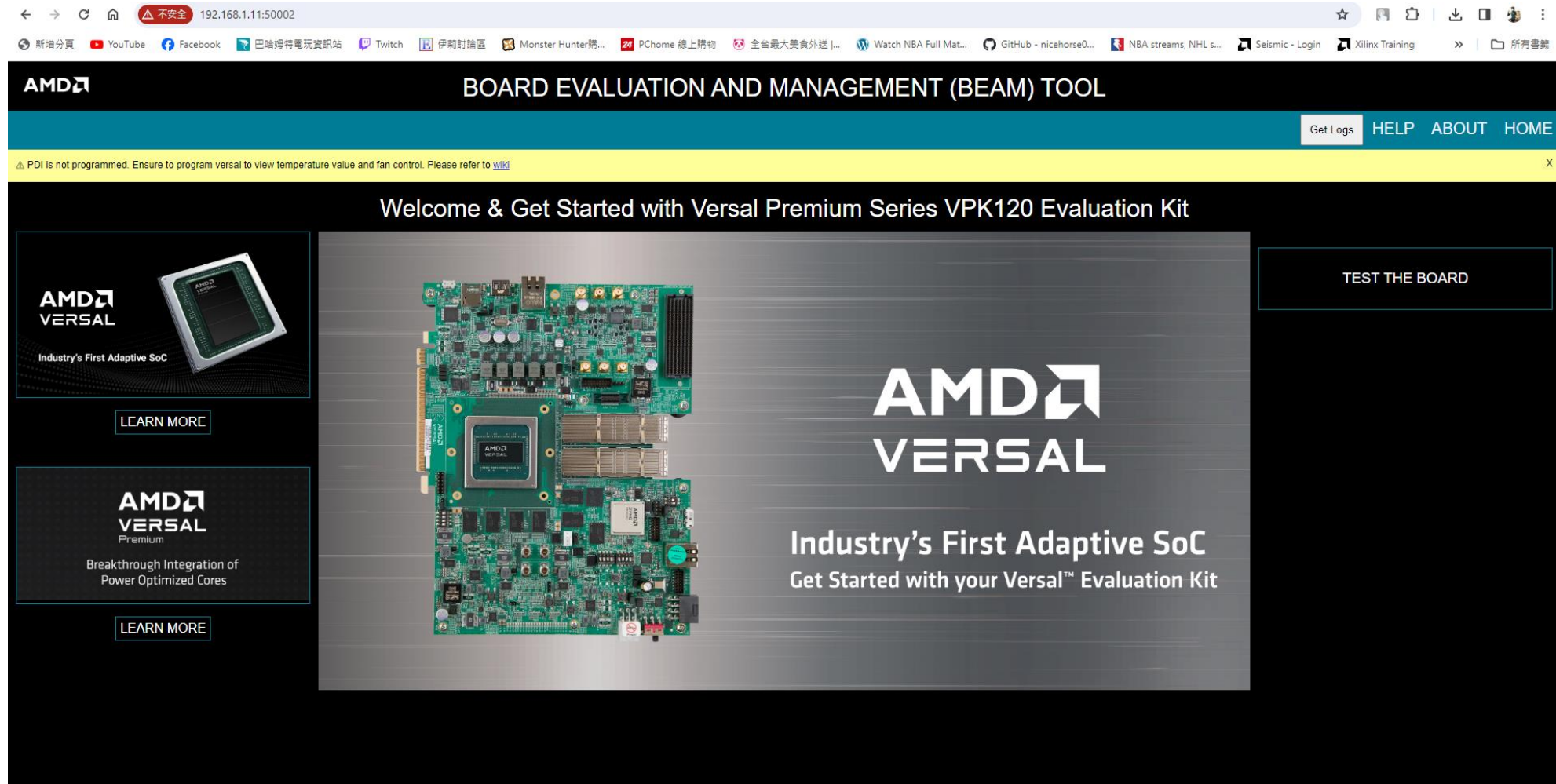
lo        Link encap:Local Loopback
          inet addr:127.0.0.1  Mask:255.0.0.0
          inet6 addr: ::1/128 Scope:Host
          UP LOOPBACK RUNNING  MTU:65536  Metric:1
          RX packets:13911  errors:0  dropped:0  overruns:0  frame:0
          TX packets:13911  errors:0  dropped:0  overruns:0  carrier:0
          collisions:0 txqueuelen:1000
          RX bytes:2110333 (2.0 MiB)  TX bytes:2110333 (2.0 MiB)

xilinx-versal-system-controller-20222:~$ ping 192.168.1.11
PING 192.168.1.11 (192.168.1.11): 56 data bytes
64 bytes from 192.168.1.11: seq=0 ttl=64 time=0.103 ms
64 bytes from 192.168.1.11: seq=1 ttl=64 time=0.124 ms
64 bytes from 192.168.1.11: seq=2 ttl=64 time=0.122 ms
64 bytes from 192.168.1.11: seq=3 ttl=64 time=0.125 ms
64 bytes from 192.168.1.11: seq=4 ttl=64 time=0.129 ms
64 bytes from 192.168.1.11: seq=5 ttl=64 time=0.124 ms
64 bytes from 192.168.1.11: seq=6 ttl=64 time=0.112 ms
64 bytes from 192.168.1.11: seq=7 ttl=64 time=0.122 ms
64 bytes from 192.168.1.11: seq=8 ttl=64 time=0.139 ms
64 bytes from 192.168.1.11: seq=9 ttl=64 time=0.119 ms
^C
--- 192.168.1.11 ping statistics ---
10 packets transmitted, 10 packets received, 0% packet loss
round-trip min/avg/max = 0.103/0.121/0.139 ms
xilinx-versal-system-controller-20222:~$
```


Launching the GUI

On the Windows PC, Open the Chrome web browser.

Enter <ip of system_controller>:50002 in the address bar of the web browser. (Ex: 192.168.1.11:50002)



Test the Board

The “Test the board” screen contains board image, device details, and boot mode. It contains navigation options to Board settings and Board interface test screens.

Versal Junction Temp

- °C

Board Settings

Board Interface Test

FMC+

QSFPP-DD

System Controller XCZU4EG

System Controller Ethernet

PCIe® ATX Power Connector

Power Switch

Power Connector

Mode Pin DIP Switch (SW1)

SMTs

LPDDR4 Components (6 x 2GB)

User LED

Versal VP1202 XCVP1202-2MSEVSA2785 ACAP

PCIe Gen5 x8

Status LEDs (Done, Error)

IEEE Std1588 (eCPRI) SMA Connectors

Versal® ACAP Ethernet

USB Type A UART

microSD (Versal ACAP)

USB JTAG

AMD
VERSAL

Silicon Revision : **PROD**

Manufacturer : **XILINX**

Product Name : **VPK120**

Board Serial Number : **962249155254**

Board Part Number : **430507201**

Board Revision : **B01**

SC MAC : **00:0a:35:07:db:4f**

Versal MAC : **00:0a:35:07:db:50**

Boot Mode:

Active:-

Change:

JTAG

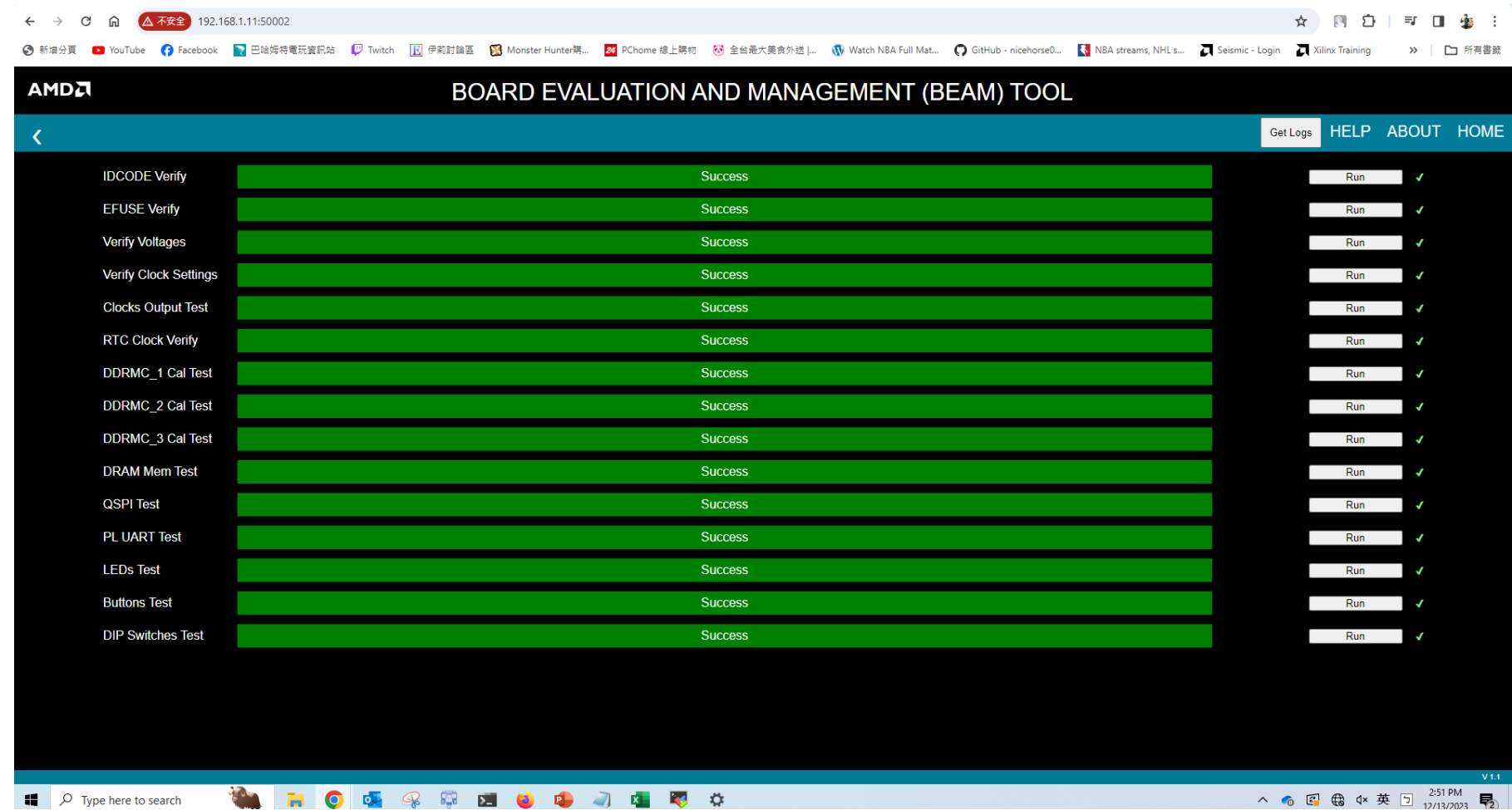
Set

Reset:

Reset

Board Interface Test

From the Home screen, click on the “Test The Board” panel and then click the “Board Interface Test” button to display the Board Interface Test (BIT) section.



Linux Image Updates

- If the displayed screen during boot differs from the demonstrated image, you may need to update the Linux image.

```
[ 19.745177] TCP: request_sock_TCP: Possible SYN flooding on port 0.
.[ 25.157128] scwebun.sh[1592]: rm: can't remove '/home/pe
[ 25.630991] audit: type=1006 audit(4290772493.043:2): pid=
[ 25.643704] audit: type=1300 audit(4290772493.043:2): arch=
id=0 euid=0 suid=0 fsuid=0 egid=0 sgid=0 fsgid=0 tty=(none) s
[ 25.669498] audit: type=1327 audit(4290772493.043:2): proc
.....
*****
*                               *
*   BEAM Tool Web Address       *
*                               *
*   No IP address is assigned   *
*                               *
*****
```

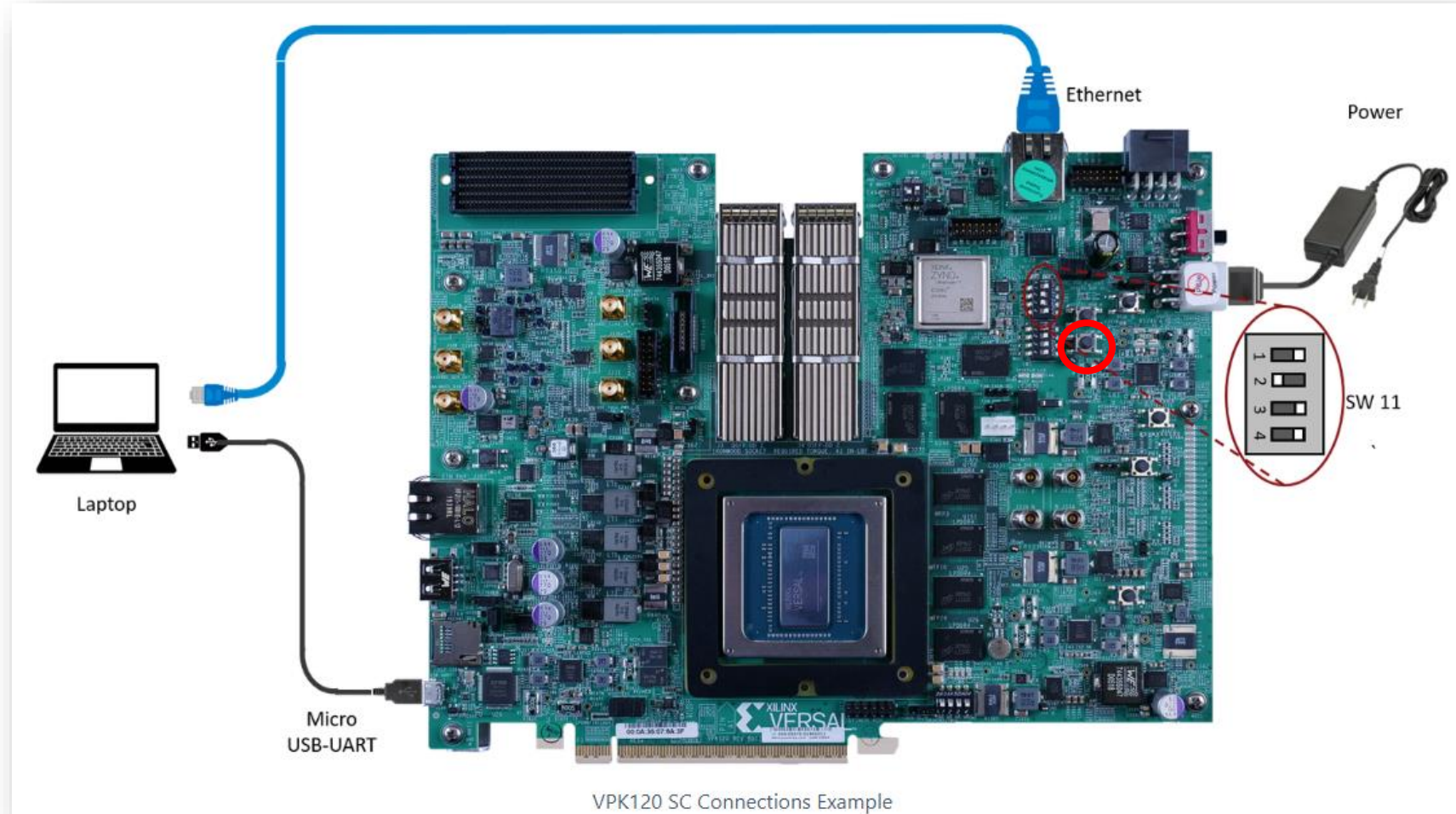
```
*****
* Enter these key-sequence to exit Board Framework *
*                               *
*                               *
*   EXT<Enter key><Tab key>     *
*                               *
*****
```

SC Linux Image	Description & Updates	Board Supported	Download Link
SC Update 0 (2021.2 base)	Early Access BEAM release	VPK120ES	None - Factory deployed only
SC Update 1 (2022.1 base)	Initial BEAM production release	VPK120ES, VPK120, VPK180ES	Xilinx Download
SC Update 2 (2022.2 base)	BEAM based active fan control	VPK120ES, VPK120, VPK180ES, VPK180, VHK158ES	Xilinx Download
SC Update 3 (2022.2 base)	BEAM, SC fan control, bug fixes & feature enhancements	VPK120ES, VPK120, VPK180ES, VPK180, VHK158ES, VHK158, VEK280ES	Xilinx Download
SC Update 4 (2022.2 base)	BEAM, SC fan Control, various bug fixes & feature enhancements	VPK120ES, VPK120, VPK180ES, VPK180, VHK158ES, VHK158, VEK280ES	Xilinx Download
SC Update 5 (2022.2 base)	Add support for VEK280, bug fix release	VPK120ES, VPK120, VPK180ES, VPK180, VHK158ES, VHK158, VEK280ES, VEK280	Xilinx Download

Board setup and Connections

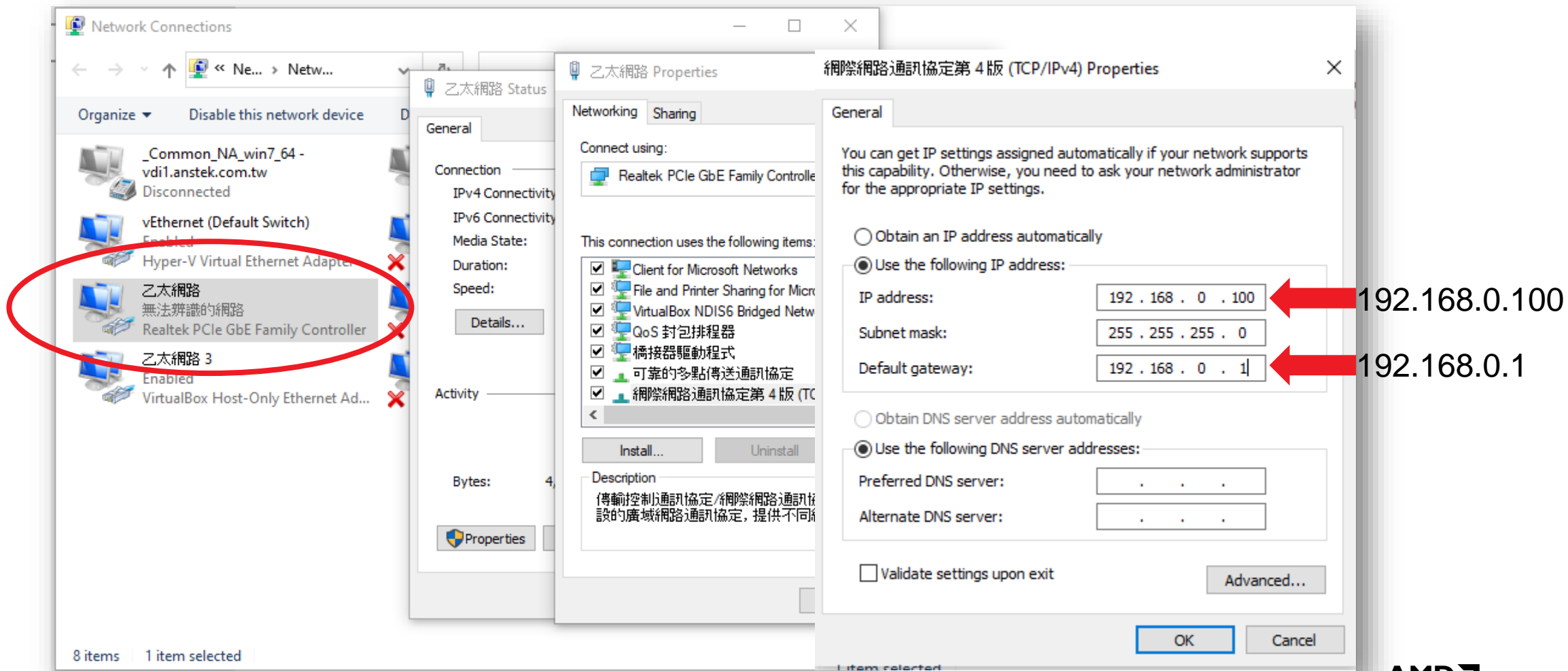
No changes are required in the development board configuration.

The tool is launched by holding the SC FWUEN pushbutton during a power-on of the evaluation board.



Windows PC IP Settings

Make sure that the last digit of the IP Address on the Windows PC is different to what is being set on the Board.



Board setup and Connections

update the Linux image download the desired SC Linux image and use the Image Recovery applicatoin “Image Wic (eMMC)” radial selection and the “Browse” button to select the downloaded <linux-image-name>.wic.

If the file downloaded was in a compressed format (e.g. .xz) then use a compression tool (e.g. 7Zip) on your Host PC to first decompress the file to a native *.wic format prior to using the Image Recovery Tool.

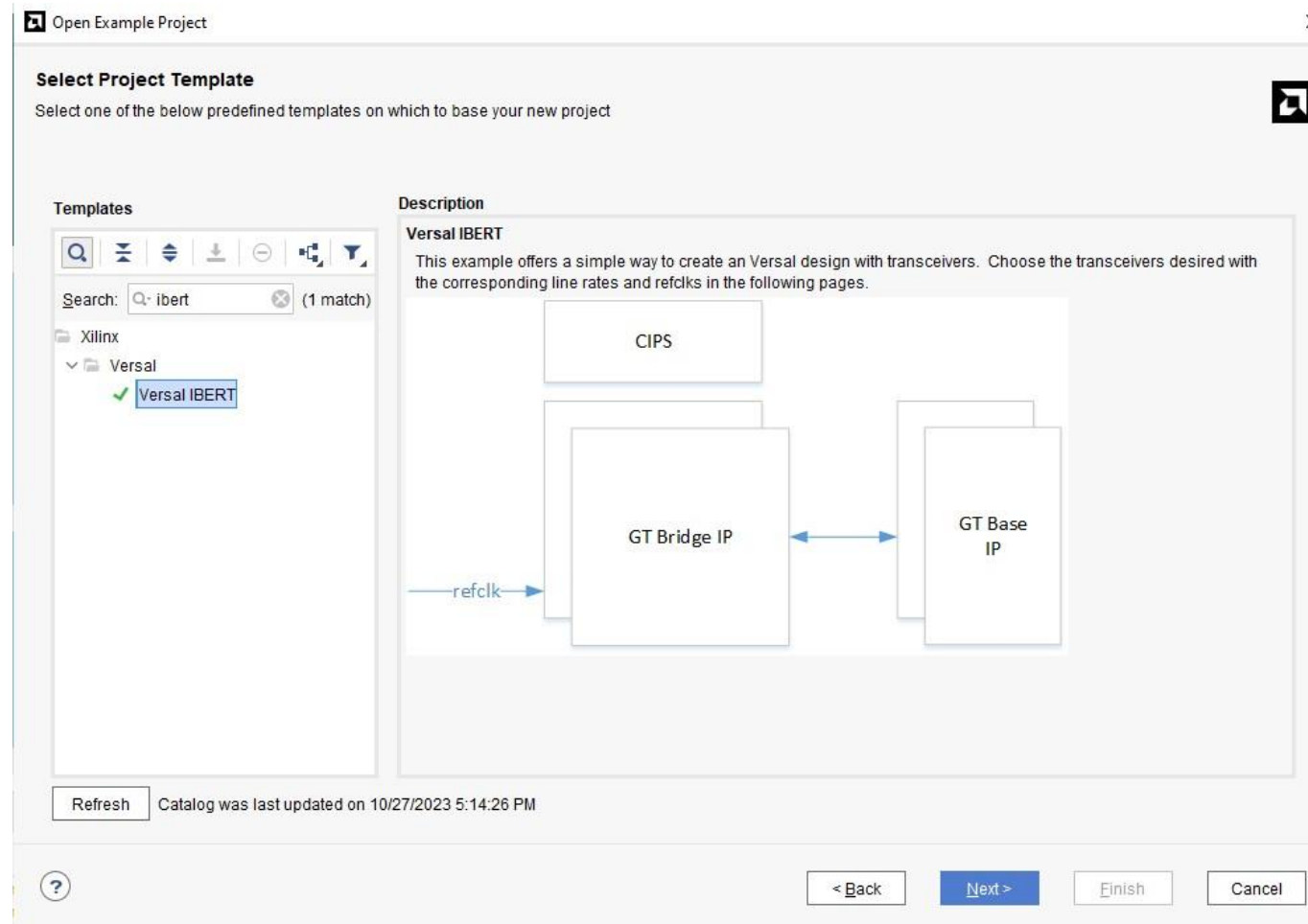
The screenshot shows the Xilinx Boot Image Recovery Tool web interface. It includes sections for System Board Information, Carrier Card Information, Boot Image Status, and Recover Image. The Recover Image section has a 'Browse' button, a file selection area, and an 'Upload' button. Annotations are as follows: 1. A large arrow points from the 'Image B (QSPI)' radio button to the 'Upload' button. 2. An arrow points from the 'Browse' button to a file named 'petalinux-sdimage_xilinx-versal-system-controller-v2022.2_11062054_update5A.wic' in a file explorer window. 3. An arrow points from the text 'This process will take approximately 40 to 50 minutes.' to the 'Upload' button.

3 This process will take approximately 40 to 50 minutes.

Versal IBERT

Versal IBERT Example Design

The design consists of a specific flow that will ensure success and repeatability by leveraging built in Vivado example designs and flows. This same flow can be used with deviations later, in order to test different bandwidths, GTs or other board capabilities. The design can be simply explained with the following block diagram



Versal IBERT Example Design

In the Default Part selection, click on the Part column header, which will sort the parts repeatably¹³. Scroll nearly 5/6 of the way down and select **xcvp1202-vsva2785-2MP(or2MHP)-e-S**

Open Example Project

Default Part
Choose a default AMD part for your project.

Search: (40 matches)

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	BUFGs	Gb Transc
xcvp1102-vsva2785-2MP-e-L	2785	486	719872	1439744	1405	453	1904	14953	72
xcvp1102-vsva2785-2MP-e-S	2785	486	719872	1439744	1405	453	1904	14953	72
xcvp1102-vsva2785-2MP-i-L	2785	486	719872	1439744	1405	453	1904	14953	72
xcvp1102-vsva2785-2MP-i-S	2785	486	719872	1439744	1405	453	1904	14953	72
xcvp1202-vsva2785-2MHP-e-L	2785	702	900224	1800448	1341	677	3984	20037	48
xcvp1202-vsva2785-2MHP-e-S	2785	702	900224	1800448	1341	677	3984	20037	48
xcvp1202-vsva2785-2MHP-i-L	2785	702	900224	1800448	1341	677	3984	20037	48
xcvp1202-vsva2785-2MHP-i-S	2785	702	900224	1800448	1341	677	3984	20037	48
xcvp1202-vsva2785-2MP-e-L	2785	702	900224	1800448	1341	677	3984	20037	48
xcvp1202-vsva2785-2MP-e-S	2785	702	900224	1800448	1341	677	3984	20037	48
xcvp1202-vsva2785-2MP-i-L	2785	702	900224	1800448	1341	677	3984	20037	48
xcvp1202-vsva2785-2MP-i-S	2785	702	900224	1800448	1341	677	3984	20037	48
xcvp1402-vsva2785-2MP-e-L	2785	530	1020928	2041856	1981	645	2672	20933	88
xcvp1402-vsva2785-2MP-e-S	2785	530	1020928	2041856	1981	645	2672	20933	88
xcvp1402-vsva2785-2MP-i-L	2785	530	1020928	2041856	1981	645	2672	20933	88
xcvp1402-vsva2785-2MP-i-S	2785	530	1020928	2041856	1981	645	2672	20933	88
xcvp1502-vsva2785-2MHP-e-L	2785	702	1720448	3440896	2541	1301	7440	35286	84
xcvp1502-vsva2785-2MHP-e-S	2785	702	1720448	3440896	2541	1301	7440	35286	84

Versal IBERT Example Design

Here we can select the GTYP/GTM for our IBERT design.
The GTs are broken up into a left and right side well as broken into QUADS

Open Example Project

Select Design Preset

Choose which preset design to use based on the description.

Left Side

Right Side

Quad Enable	Refclk Source	Line Rate (max: 32.0 Gbps)	Refclk (max: 820.0 MHz)
<input checked="" type="checkbox"/> GTYP QUAD 106	GTYP REFCLK X0Y12	10.3125	156.25

< BackNext >

Open Example Project

Select Design Preset

Choose which preset design to use based on the description.

Left Side

Right Side

Quad Enable	Refclk Source	Line Rate (max: 32.0 Gbps)	Refclk (max: 820.0 MHz)
<input checked="" type="checkbox"/> GTYP QUAD 200	GTYP REFCLK X1Y0	10.3125	156.25
<input checked="" type="checkbox"/> GTYP QUAD 201	GTYP REFCLK X1Y2	10.3125	156.25

Quad Enable	Refclk Source	Line Rate (max: 112.0 Gbps)	Refclk (max: 820.0 MHz)
<input checked="" type="checkbox"/> GTM QUAD 202	GTM REFCLK X0Y0	53.125	156.25
<input checked="" type="checkbox"/> GTM QUAD 203	GTM REFCLK X0Y2	53.125	156.25
<input checked="" type="checkbox"/> GTM QUAD 204	GTM REFCLK X0Y4	53.125	156.25
<input checked="" type="checkbox"/> GTM QUAD 205	GTM REFCLK X0Y6	53.125	156.25
<input checked="" type="checkbox"/> GTM QUAD 206	GTM REFCLK X0Y8	53.125	156.25

< BackNext >FinishCancel

It is recommended to maintain the frequency of the reference clock at 156.25MHz.

Versal Transceiver Mapping

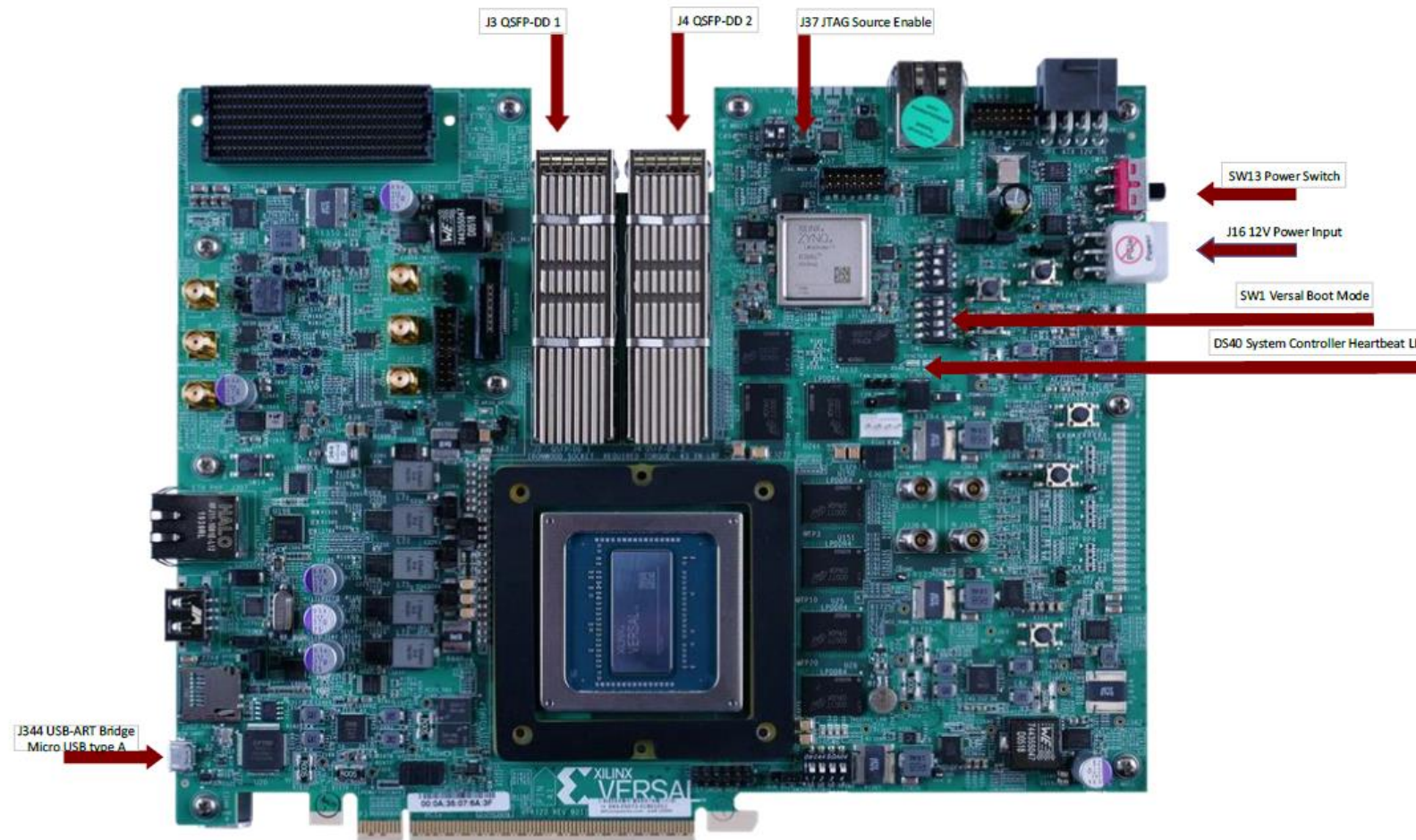
- In the User Guide, the Transceiver Mapping table has more detail as the included hardened IP blocks associated with specific transceiver quads are mapped out including which clocks are associated with each quad
- This might be used if testing and tuning specific QUADs to be used with specific hardened IP is necessary for future designs
- The **default value of 156.25 MHz** has already been programmed at the factory for the clock source. This mean the **8A34001** (U219).
- If a different frequency is desired, refer to the BoardUI programming tool as well as Renesas programming instructions.

Table: Transceiver Mapping

VPK120 XCVP1202 VSVA2785 GTY/GTM Mapping									
[Unused]	ch3	GTYP Quad 106 X0Y6	PCle X0Y1			MRMAC X0Y1	GTM Quad 206 X0Y4	ch3	GTM SMA
[Unused]	ch2							ch2	8A34001 1PPS Clocks
[Unused]	ch1							ch1	[Unused]
[Unused]	ch0							ch0	[Unused]
[Unused]	refclk1							refclk1	8A34001 CLK6 IN
[Unused]	refclk0							refclk0	8A34001 Q7 OUT
PCle Lane 0	ch3	GTYP Quad 105 X0Y5	CPM5				GTM Quad 205 X0Y3	ch3	QSFPDD1 Lane 1
PCle Lane 1	ch2							ch2	QSFPDD1 Lane 5
PCle Lane 2	ch1							ch1	QSFPDD1 Lane 2
PCle Lane 3	ch0							ch0	QSFPDD1 Lane 6
[Unused]	refclk1							refclk1	[Unused]
PCle Edge Clock 0	refclk0							refclk0	8A34001 Q8 BUF0
						DCMAC X0Y0			
PCle Lane 4	ch3	GTYP Quad 104 X0Y4	CPM5 (HSDP)				GTM Quad 204 X0Y2	ch3	QSFPDD1 Lane 3
PCle Lane 5	ch2							ch2	QSFPDD1 Lane 7
PCle Lane 6	ch1							ch1	QSFPDD1 Lane 4
PCle Lane 7	ch0							ch0	QSFPDD1 Lane 8
[Unused]	refclk1							refclk1	8A34001 CLK5 IN MUX1
PCle Edge Clock 1	refclk0							refclk0	8A34001 Q8 BUF1

Board Component Location

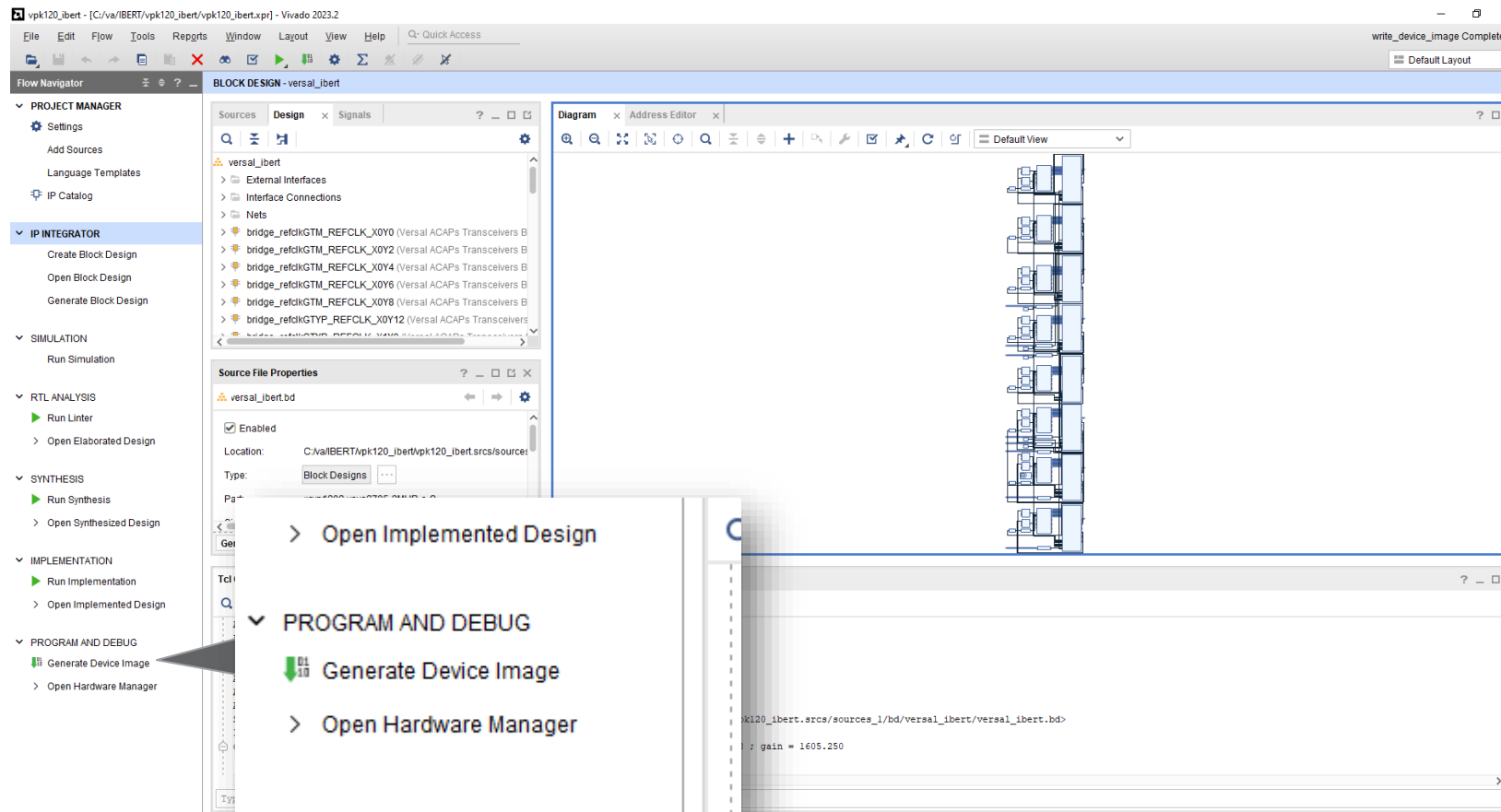
Ensure the included loopback adapter (Multilane ML4062-LB-112) is inserted and FULLY seated in the QSFPDD-1 (J3) cage / connector (If you are using the official PDI file provided in RDF0636,)



Generate Device Image

Once the project is initialized, as mentioned in the beginning overview, now is the time to review settings, by opening the Block Design and then opening the details of the various IP generated for you

Once satisfied, or if you do not wish to review, select **Generate Device Image** from the Flow Navigator



Modify Refclk Frequency

Before programming, it is necessary to adjust the frequency of 8A34001 to 156.25. You can use either BoardUI or BEAM to utilize the System Controller for adjustment.

Get ClockSet ClockSet Boot ClockRestore Clock

Upload clock files

<input checked="" type="checkbox"/>	Clock Name	Range	Frequency	Set All
<input checked="" type="checkbox"/>	User1 FMC Si570	(10.000 MHz - 810.000 MHz)		Set
<input checked="" type="checkbox"/>	Versal Sys Clk Si570	(10.000 MHz - 160.000 MHz)		Set
<input checked="" type="checkbox"/>	LPDDR4 CLK1 Si570	(10.000 MHz - 810.000 MHz)		Set
<input checked="" type="checkbox"/>	LPDDR4 CLK2 Si570	(10.000 MHz - 810.000 MHz)		Set
<input checked="" type="checkbox"/>	LPDDR4 CLK3 Si570	(10.000 MHz - 810.000 MHz)		Set
<input checked="" type="checkbox"/>	8A34001	-	8A34001_2020-031 Default 8A34001_2020-0318_156MHz User	Set

☒ 8A34001

CLK0 - From 8A34001 Q0; Q0 - To 8A34001 CLK0: 156.25MHz

Q10 - To SMA J328: 156.25MHz

Q11 - To N.C.:

CLK1 - From Bank 703; Q1 - To Bank 206 GTM RX2: 156.25MHz

CLK2 - From Bank 206 GTM TX2; Q2 - To Bank 703: 156.25MHz

CLK3 - From 8A34001 Q4; Q3 - To SMA J339: 156.25MHz

CLK4 - From SMA J330-331; Q4 - To 8A34001 CLK3: 156.25MHz

CLK5 - From Bank 202/204 GTM REFCLK1; Q5 - To FMC REFCLK C2M: 156.25MHz

CLK6 - From Bank 206 GTM REFCLK1; Q6 - To Bank 711: 156.25MHz

CLK7 - From FMC REFCLK M2C; Q7 - To Bank 206 GTM REFCLK0: 156.25MHz

Q8 - To Bank 204/205 GTM REFCLK0: 156.25MHz

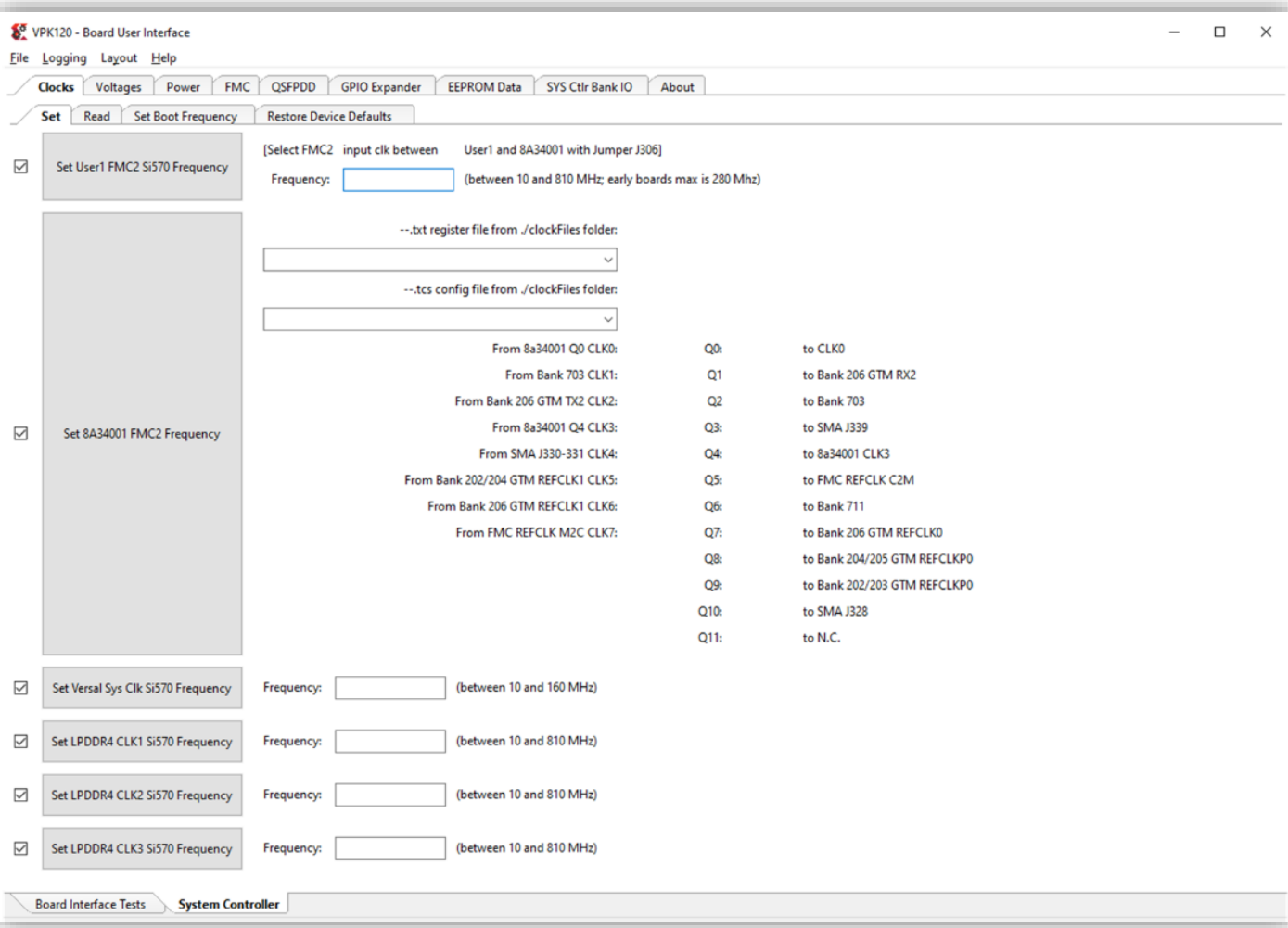
Q9 - To Bank 202/203 GTM REFCLK0: 156.25MHz

Get

✓

NOTE: these frequencies represent the last clock set operation and not the actual output frequencies generated by the device.

Modify Refclk Frequency

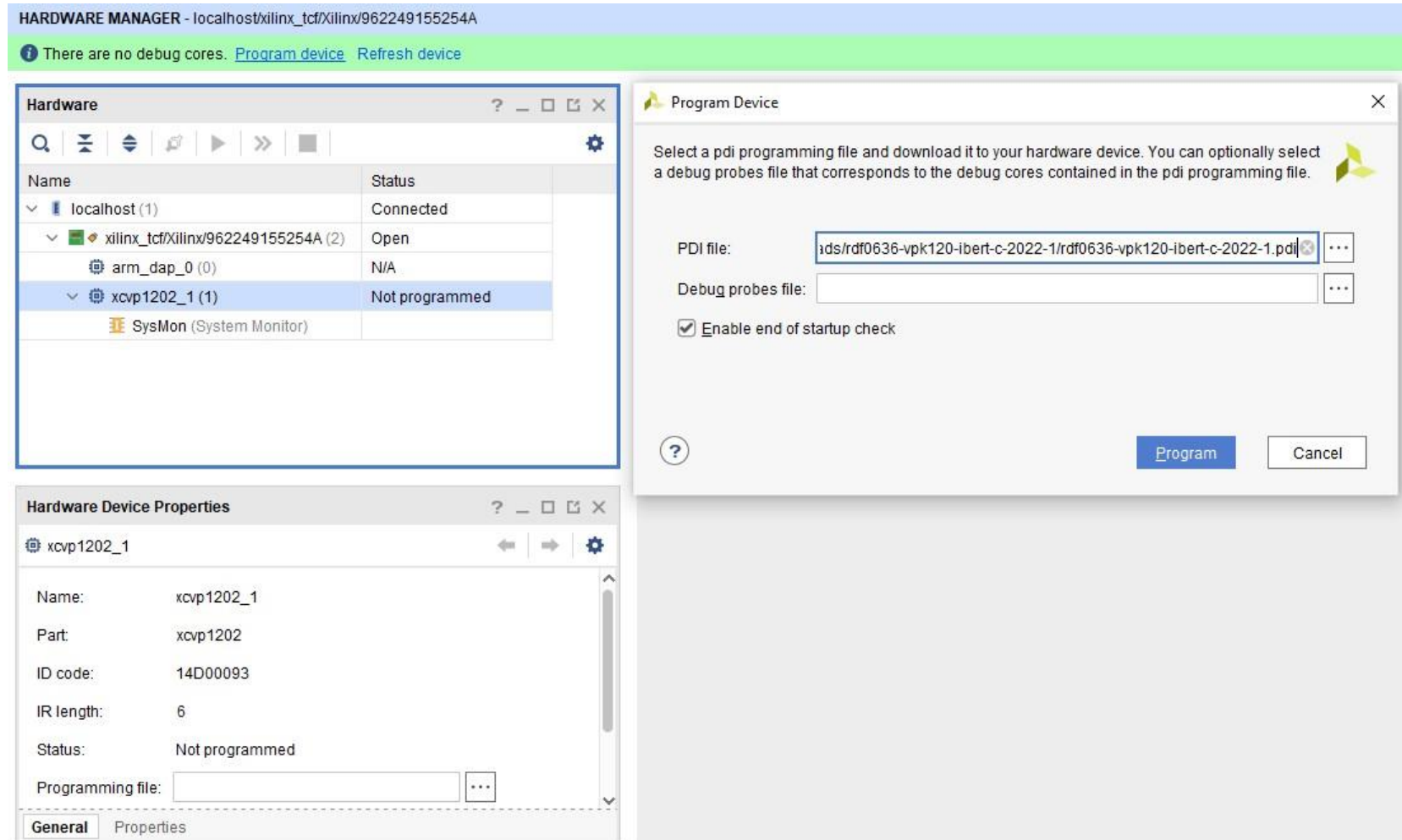


A brief summary is provided here.

- 1.Ensure the Skyworks/Silicon Labs VCP USB-UART drivers are installed. See the *Silicon Labs CP210x USB-to-UART Installation Guide* ([UG1033](#)).
- 2.Download the board user interface host PC application from the [VPK120 Evaluation Board](#) website.
- 3.Connect a USB cable to VPK120 USB-UART USB-A connector (J344).
- 4.Power-cycle the VPK120.
- 5.Launch the board user interface application.

Program Device

If you are programming the prebuilt PDI, select the file here and program.
Once completed, the IBERT Real-Time Scan Plots are opened



Create Links

In the Serial I/O Links tab, select Create Links.

Note: Depending on configuration, it can be prohibitively long to run “Auto-detect links”

- In the following pop-up dialog, select a 1:1 for each channel such that the New Links area is populated as shown. This is done by clicking the large + while you have two channels selected

TX GTs

Search:

- ▶ IBERT_0.Quad_204.CH_0.TX
- ▶ IBERT_0.Quad_204.CH_1.TX
- ▶ IBERT_0.Quad_204.CH_2.TX
- ▶ IBERT_0.Quad_204.CH_3.TX

RX GTs

Search:

- ◀ IBERT_0.Quad_204.CH_0.RX
- ◀ IBERT_0.Quad_204.CH_1.RX
- ◀ IBERT_0.Quad_204.CH_2.RX
- ◀ IBERT_0.Quad_204.CH_3.RX

New Links

+ -

No content

☒ Create link group

Link group description:

☒ Open Serial I/O Analyzer layout



TX GTs

Search:

RX GTs

Search:

New Links

+ -

Description	TX	RX	Internal Loopback
Link 0	IBERT_0.Quad_204.CH_0.TX	IBERT_0.Quad_204.CH_0.RX	<input type="checkbox"/>
Link 1	IBERT_0.Quad_204.CH_1.TX	IBERT_0.Quad_204.CH_1.RX	<input type="checkbox"/>
Link 2	IBERT_0.Quad_204.CH_2.TX	IBERT_0.Quad_204.CH_2.RX	<input type="checkbox"/>
Link 3	IBERT_0.Quad_204.CH_3.TX	IBERT_0.Quad_204.CH_3.RX	<input type="checkbox"/>

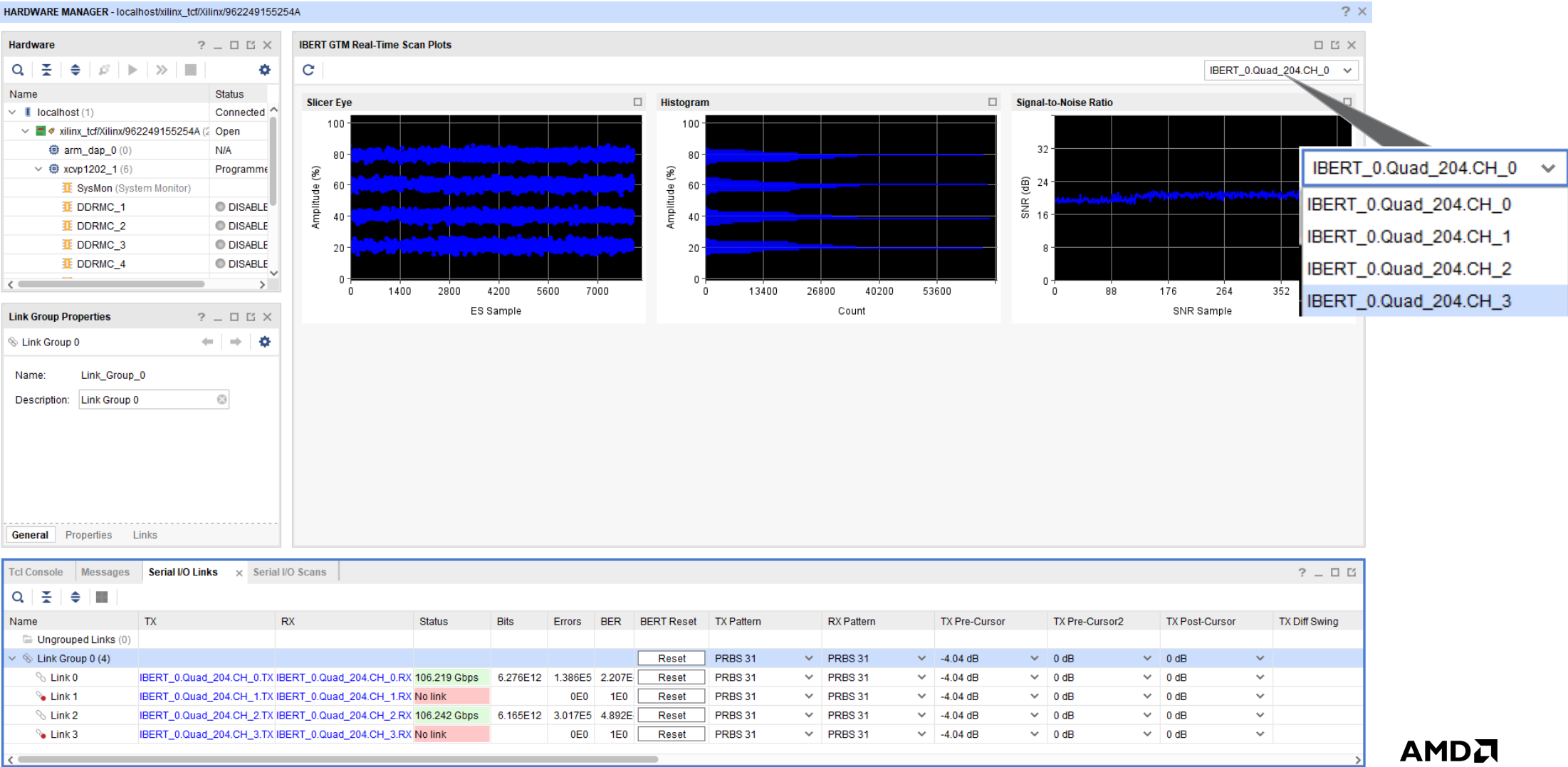
☒ Create link group

Link group description:

☒ Open Serial I/O Analyzer layout

Versal IBERT View

Using this, you can view each individual channel's plots.



PLL Status

- Verify is that the PLLS are locked. Scroll the tab to the right and locate the PLL columns
- If the PLL does not show lock, please review whether the refclk is set correctly.

RX PLL Status	TX PLL Status
Locked	Locked
Locked	Locked
Locked	Locked
Locked	Locked

Parameter adjustment.

For the VPK120, example performance tuning has been completed and it is suggested to change the TX Pre-Cursor, TX Pre-Cursor2, TX Post-Cursor and TX Main-Cursor for Link 0 as suggested in the following image

TX Pre-Cursor	TX Pre-Cursor2	TX Post-Cursor	TX Main-Cursor
Multiple	Multiple	Multiple	Multiple
-4.04 dB	0 dB	0 dB	0.998 Vdd
User Design	User Design	User Design	User Design
User Design	User Design	User Design	User Design
User Design	User Design	User Design	User Design

As these are critical tunes, we will now need to reset the link

TX Reset

Reset

RX Reset

Reset

Reset

Reset

Reset Link Property...

Cancel

Appendix

Appendix

Versal Evaluation Board - System Controller

<https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/2273738753/Versal+Evaluation+Board+--+System+Controller>

VPK120 Evaluation Board User Guide (UG1568)

<https://docs.xilinx.com/r/en-US/ug1568-vpk120-eval-bd/Additional-Resources-and-Legal-Notices>

RDF0636 - VPK120 IBERT Example Design

<https://www.xilinx.com/products/boards-and-kits/vpk120.html#resources>