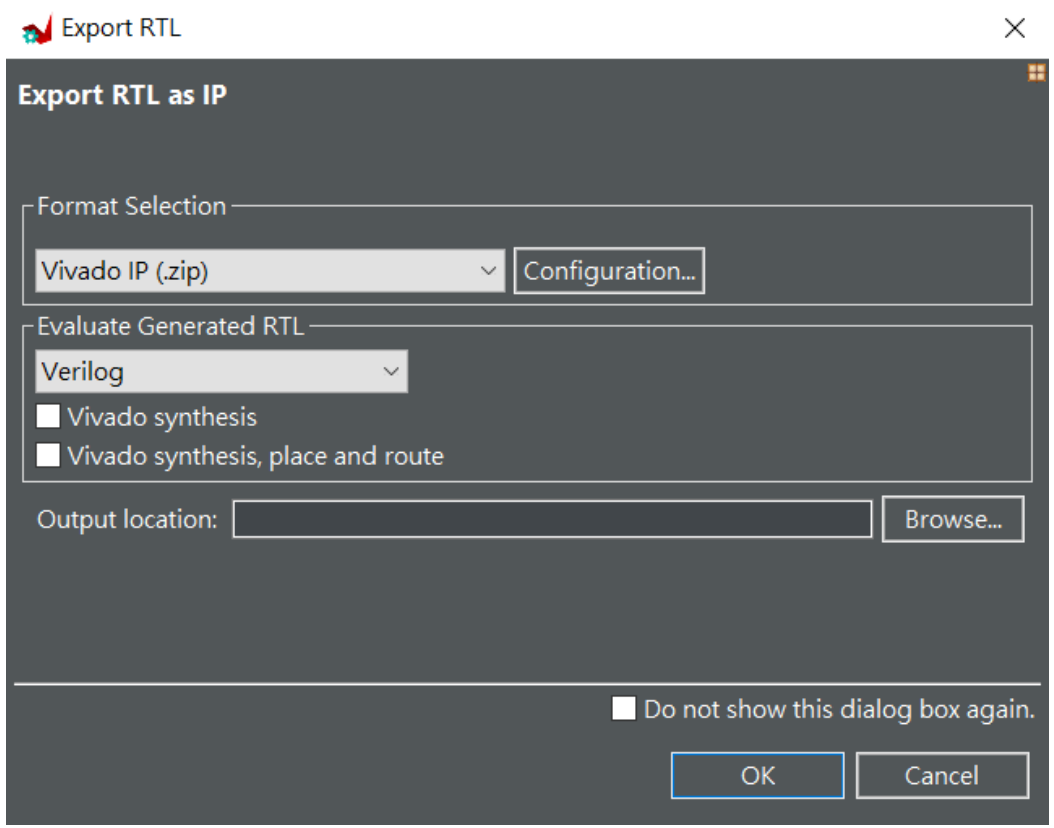
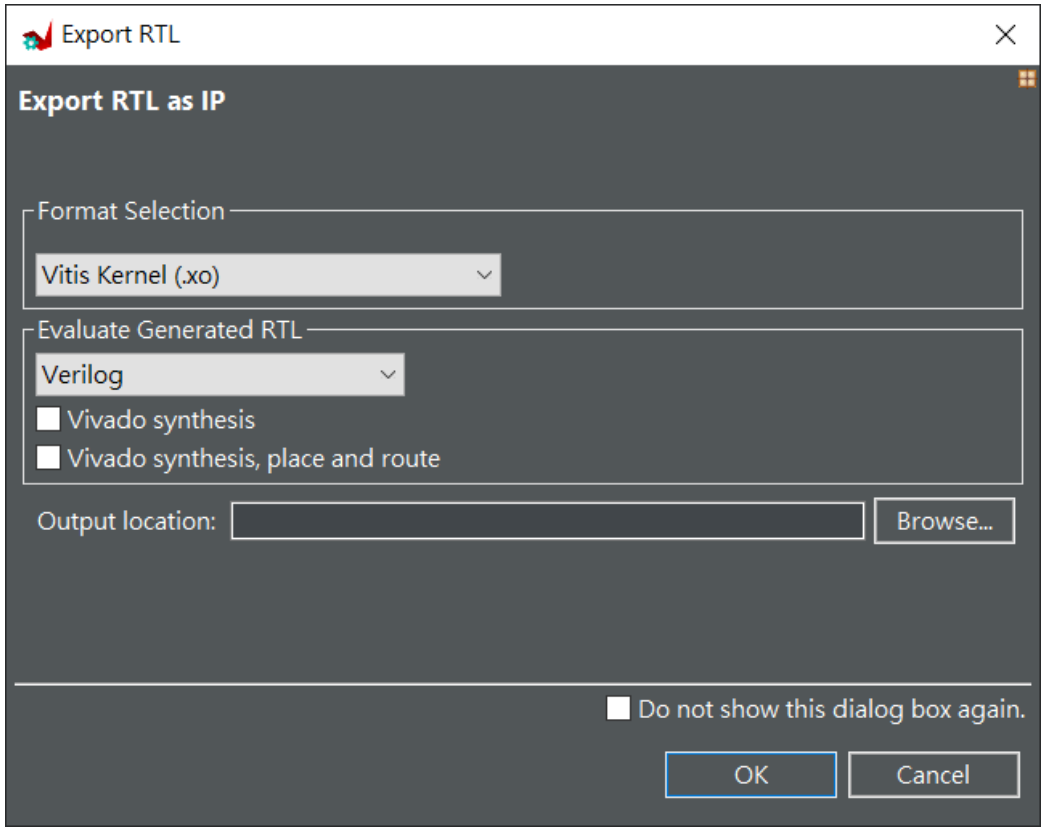
Vivado HLS 與 Vitis HLS 差異

導出 IP

- Vitis HLS 導出 IP：
  - Vivado IP：用於 Vivado 設計流程。
  - Vitis Kernel：用於 Vitis 應用加速流程，並且會自動推斷接口介面，輸出 .xo 檔。
  - Synthesized Checkpoint
  - Vivado IP for System Generator





其他差異

- **UG1391： Vitis HLS Migration Guide**

默认控制设置	Vivado_hls	Vitis_hls
config_compile -pipeline_loops	0	64
config_export -vivado_optimization_level	2	0
set_clock_uncertainty	12.5	27%
config_export -vivado_optimization_level	20	255
config_interface -m_axi_alignment_byte_size	不适用	0
config_interface -m_axi_max_widen_bitwidth	不适用	0
config_export -vivado_phys_opt	place	none
config_interface -m_axi_addr64	false	true
config_schedule -enable_dsp_full_reg	false	true
config_rtl -module_auto_prefix	false	true
interface 编译指示默认设置	ip 模式	ip 模式

- **目前，針對Vitis HLS，Xilinx已經提供了如下文檔和設計案例：**
  - UG1399：Vitis High-Level Synthesis User Guide
  - Vitis HLS examples: https://github.com/Xilinx/HLS-Tiny-Tutorials
- **HLS 視頻庫：適用於視頻實用工具和功能的 hls_video.h 已棄用，並替換為 Vitis 視覺庫。**
- **任意精度類型：Vitis HLS 不支持 C 語言任意精度類型，建議改用 C++ 作為任意精度類型。**

其他差異 – 自動優化

```
void example(int a[50], int b[50]) {
  int buff[50];
  for (size_t i = 0; i < 50; ++i) {
    buff[i] = a[i];
    buff[i] = buff[i] + 100;
    b[i] = buff[i];
  }
}
```

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00 ns	3.490 ns	1.25 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
101	101	1.010 us	1.010 us	101	101	none

Detail

Instance

Loop

	Latency (cycles)			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- Loop 1	100	100	2	-	-	50	no

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	65	-
FIFO	-	-	-	-	-
Instance	-	-	-	-	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	30	-
Register	-	-	21	-	-
Total	0	0	21	95	0
Available	624	1728	460800	230400	96
Utilization (%)	0	0	~0	~0	0

Synthesis Summary Report of 'example'

General Information

Date:	Fri Mar 5 14:48:24 2021
Version:	2020.1 (Build 2902540 on Wed May 27 20:16:15 MDT 2020)
Project:	test
Solution:	solution1 (Vivado IP Flow Target)
Product family:	zynquplus
Target device:	xczu7ev-ffvc1156-2-e

Performance&Resource Estimates

Modules Loops

Modules && Loops	Issue Type	atency(cycles)	Latency(ns)	Iteration Latency	Interval	Trip Count	Pipeline	BRAM	DSP	FF	LUT	Slack
example		52	520.000	-	53	-	no	0	0	18	114	-
VITIS_LOOP_3_1		50	500.000	2	1	50	yes	-	-	-	-	-