



VC707 IBERT Flow

Field Application Engineer

Adaptive and Embedded Computing Group (AECG)

Revision History

Date	Version	Description
10/25/23	1.0	Initial version for flow introduction.

© Copyright 2021 Xilinx, Inc. Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Vivado, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.

NOTICE OF DISCLAIMER: The information disclosed to you hereunder (the "Information") is provided "AS-IS" with no warranty of any kind, express or implied. Xilinx does not assume any liability arising from your use of the Information. You are responsible for obtaining any rights you may require for your use of this Information. Xilinx reserves the right to make changes, at any time, to the Information without notice and at its sole discretion. Xilinx assumes no obligation to correct any errors contained in the Information or to advise you of any corrections or updates. Xilinx expressly disclaims any liability in connection with technical support or assistance that may be provided to you in connection with the Information. XILINX MAKES NO OTHER WARRANTIES, WHETHER EXPRESS, IMPLIED, OR STATUTORY, REGARDING THE INFORMATION, INCLUDING ANY WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NONINFRINGEMENT OF THIRD-PARTY RIGHTS.

Vivado 2019.2 Part

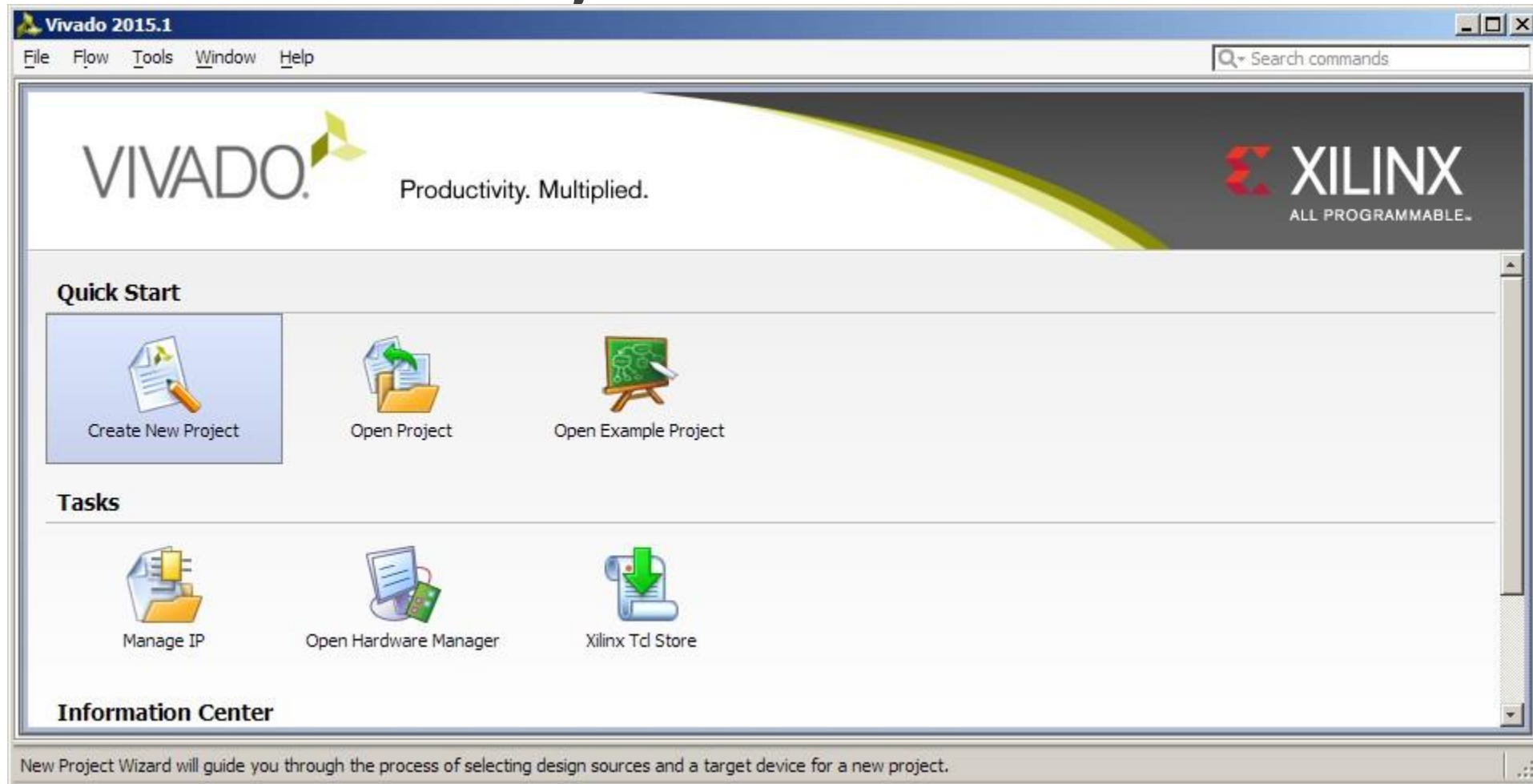
version newer than 2019.2 will not support vc707 ibert debug core

Create IBERT Design for Bank 113

➤ Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2015.1 → Vivado

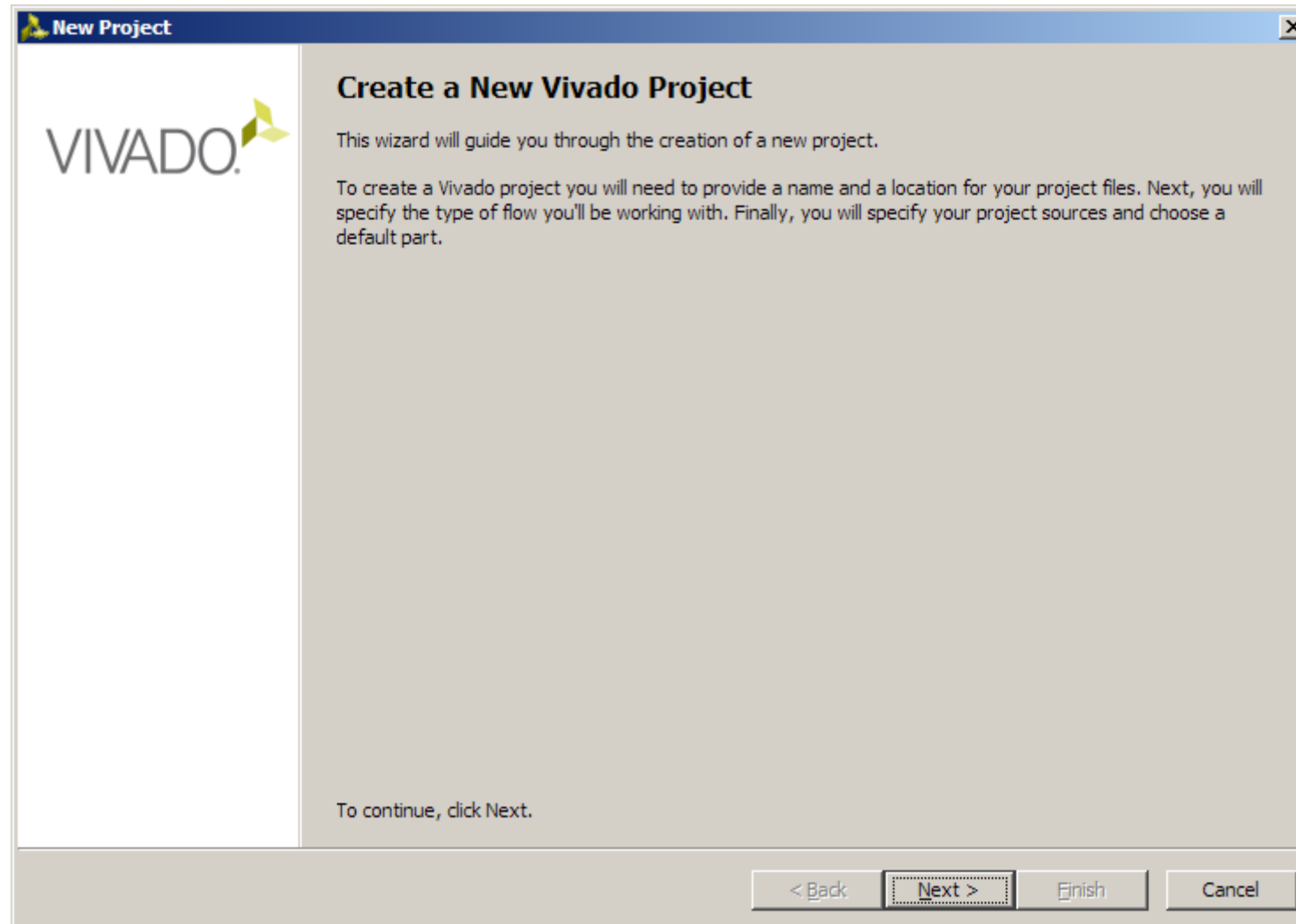
➤ Select Create New Project



Note: Presentation applies to the VC707

Create IBERT Design for Bank 113

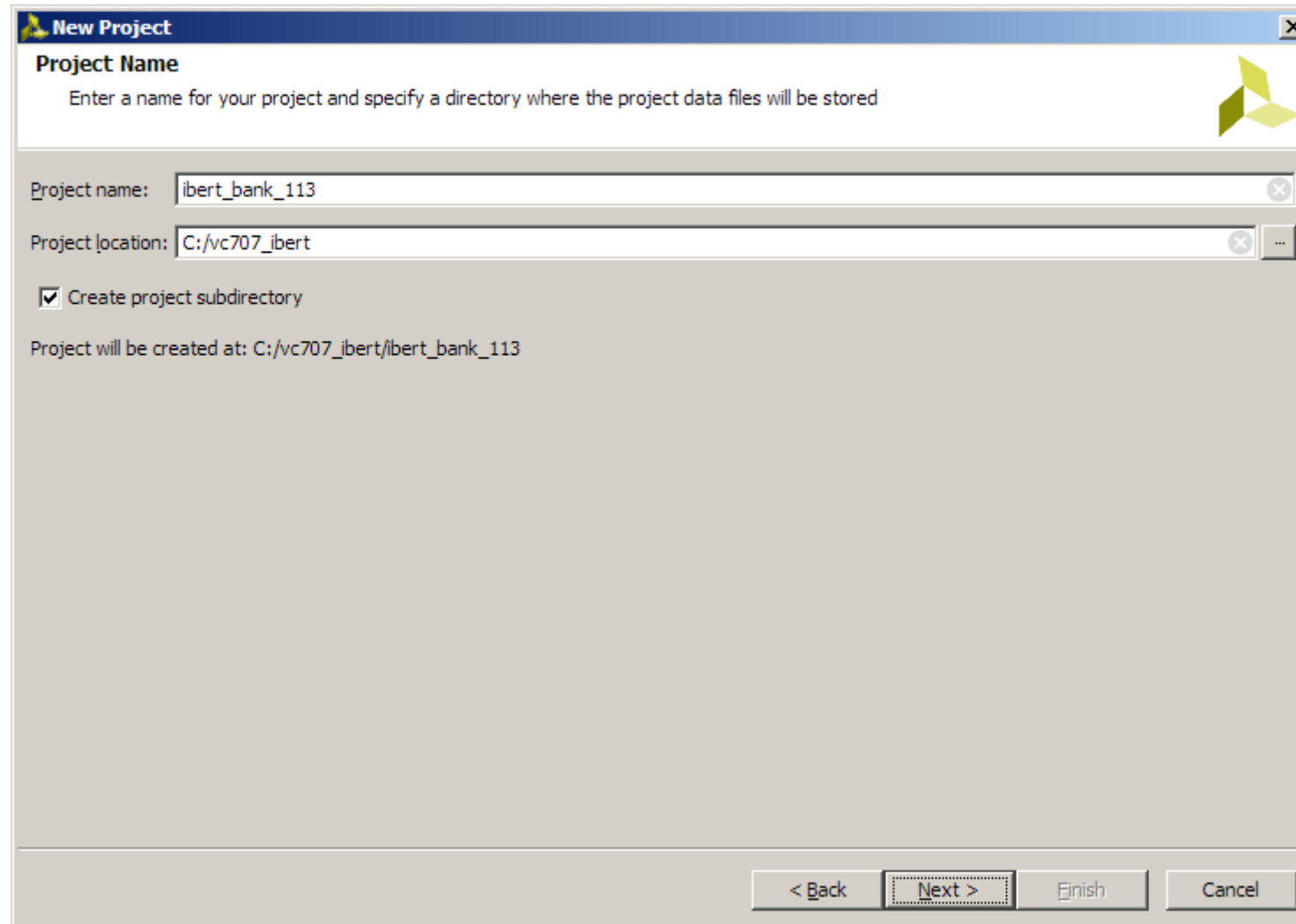
➤ Click Next



Note: Presentation applies to the VC707

Create IBERT Design for Bank 113

- Set the Project name and location to ibert_bank_113 and C:/vc707_ibert; check Create project subdirectory

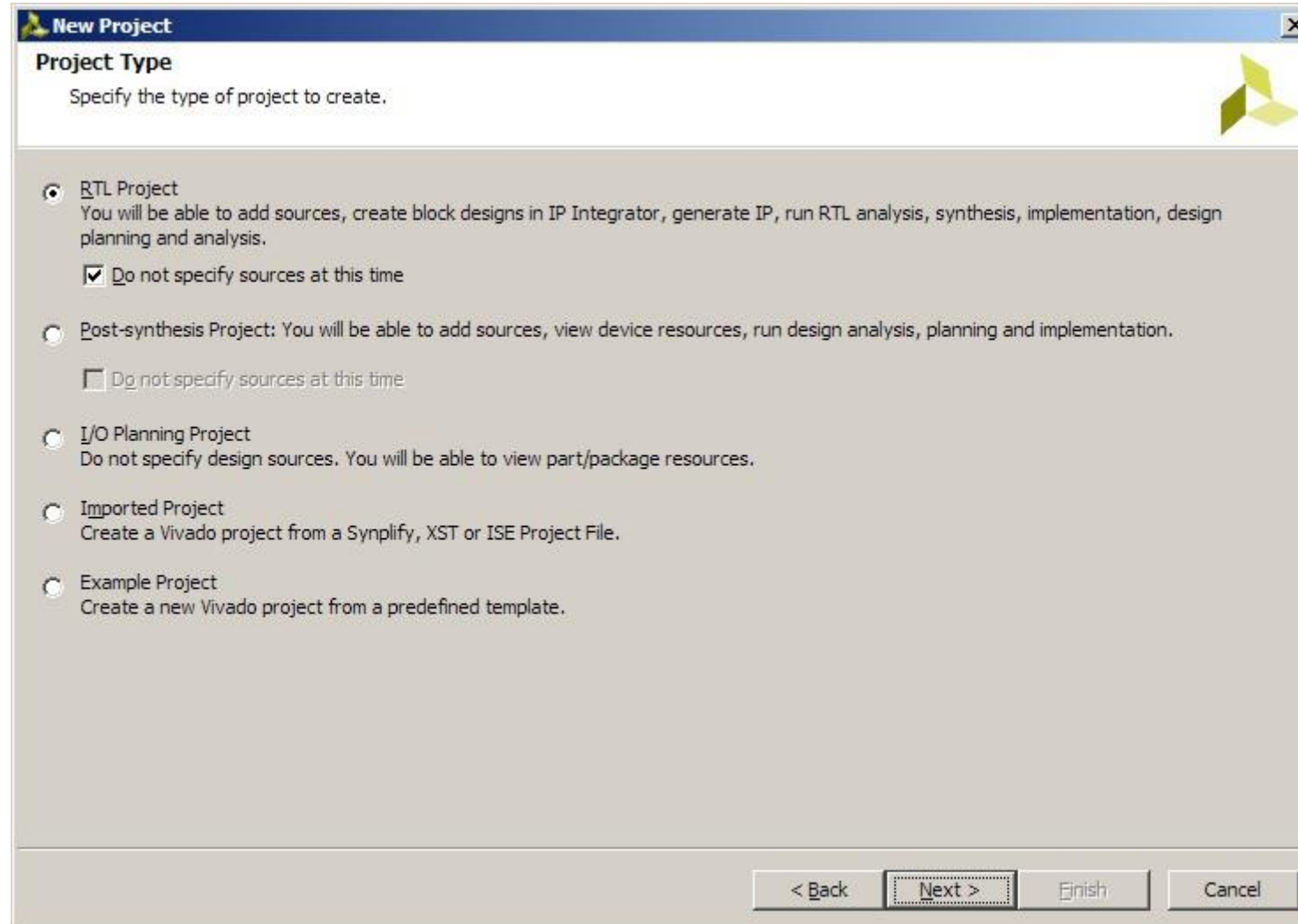


Note: Vivado generally requires forward slashes in paths

Create IBERT Design for Bank 113

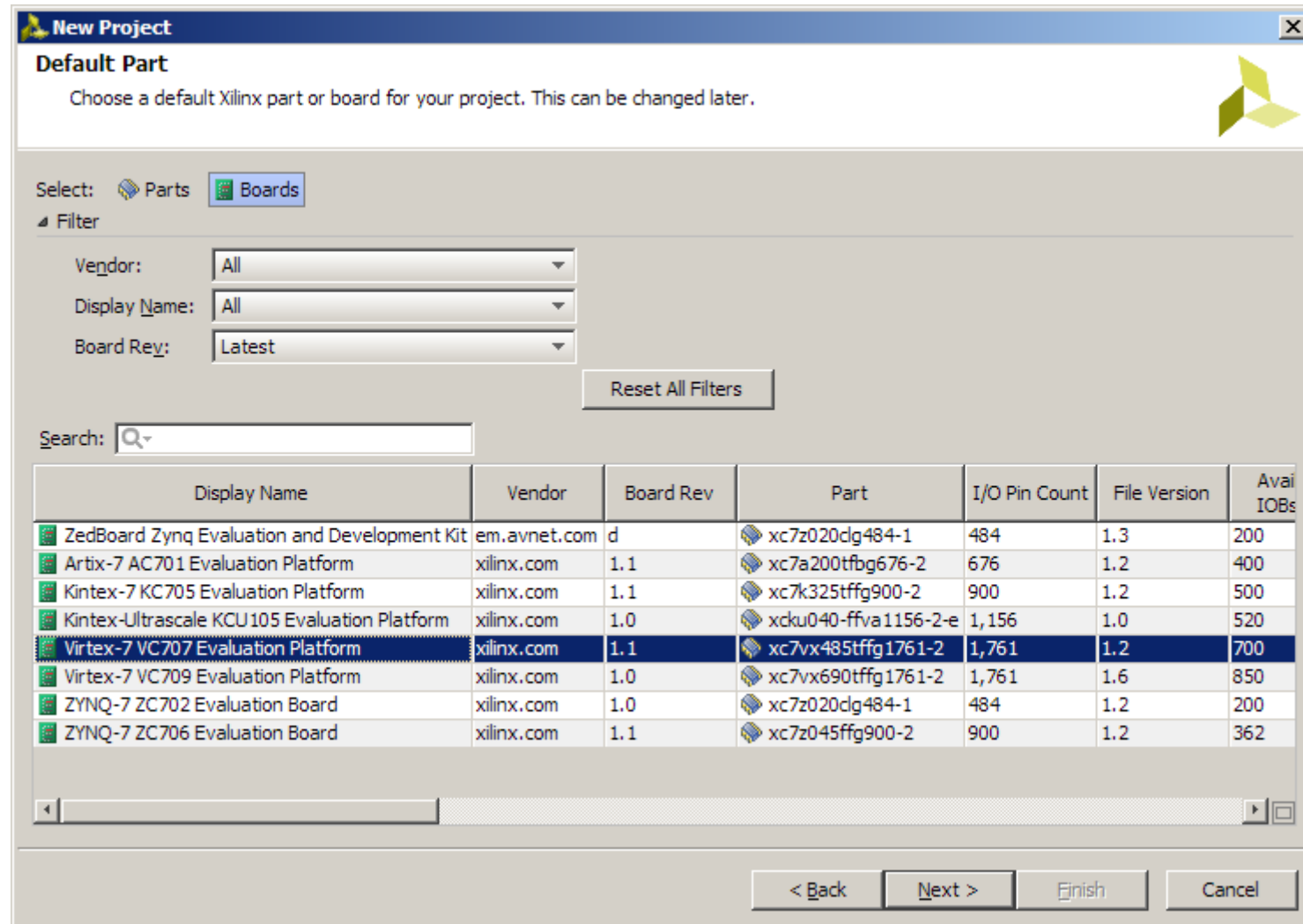
➤ Select RTL Project

- Select **Do not specify sources at this time**



Create IBERT Design for Bank 113

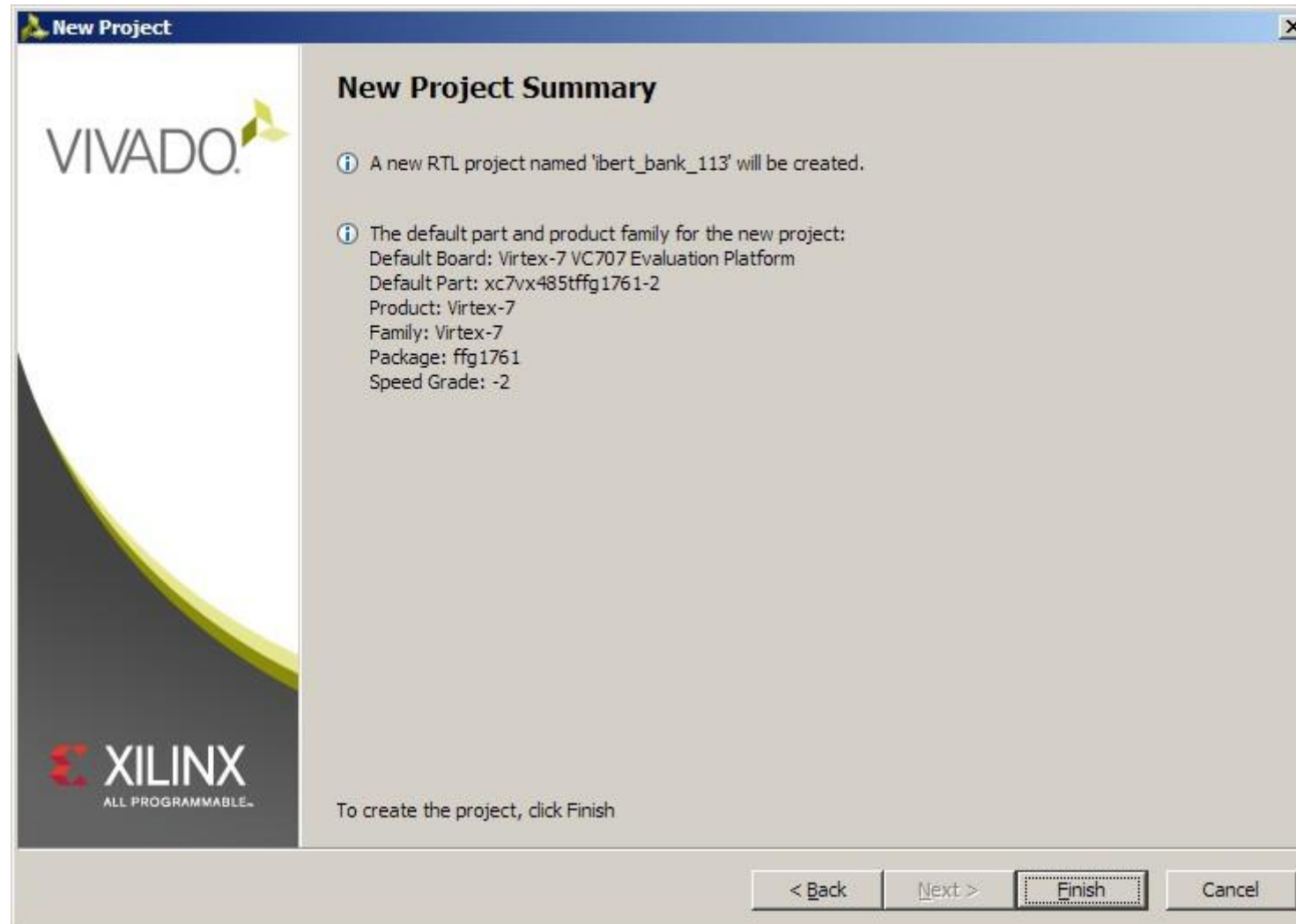
➤ Select the VC707 Board



Note: Presentation applies to the VC707

Create IBERT Design for Bank 113

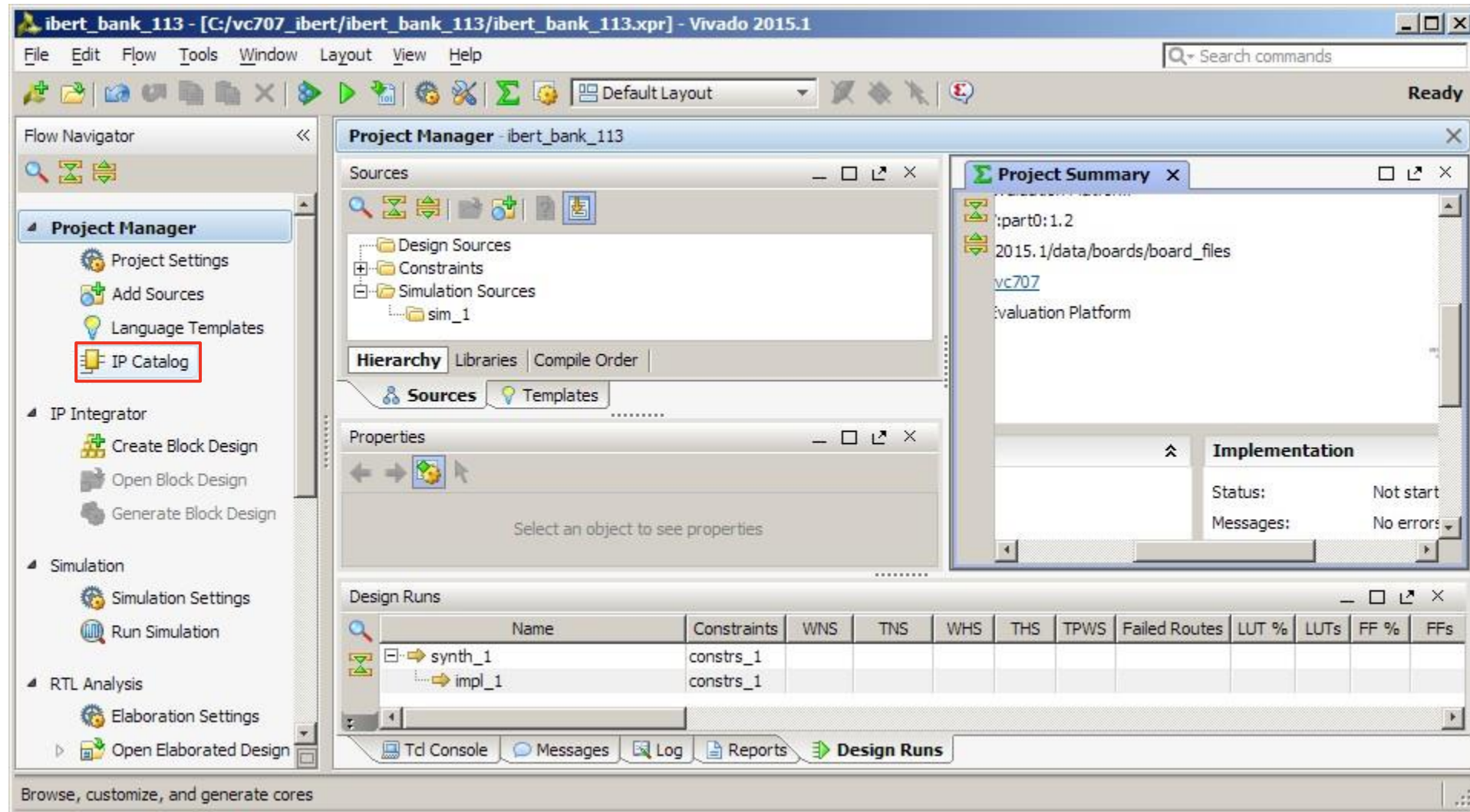
➤ Click Finish



Note: Presentation applies to the VC707

Create IBERT Design for Bank 113

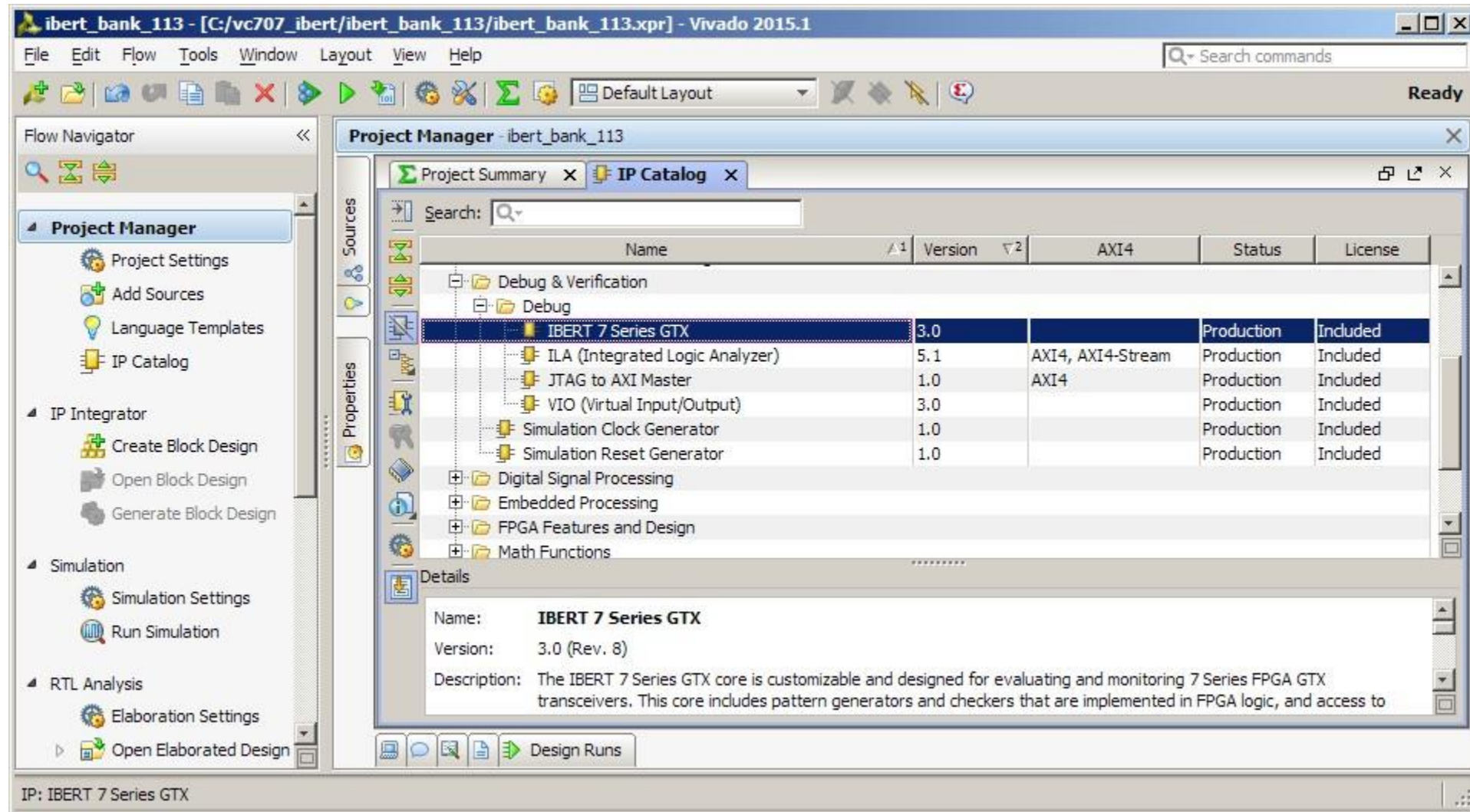
➤ Click on IP Catalog



Note: Presentation applies to the VC707

Create IBERT Design for Bank 113

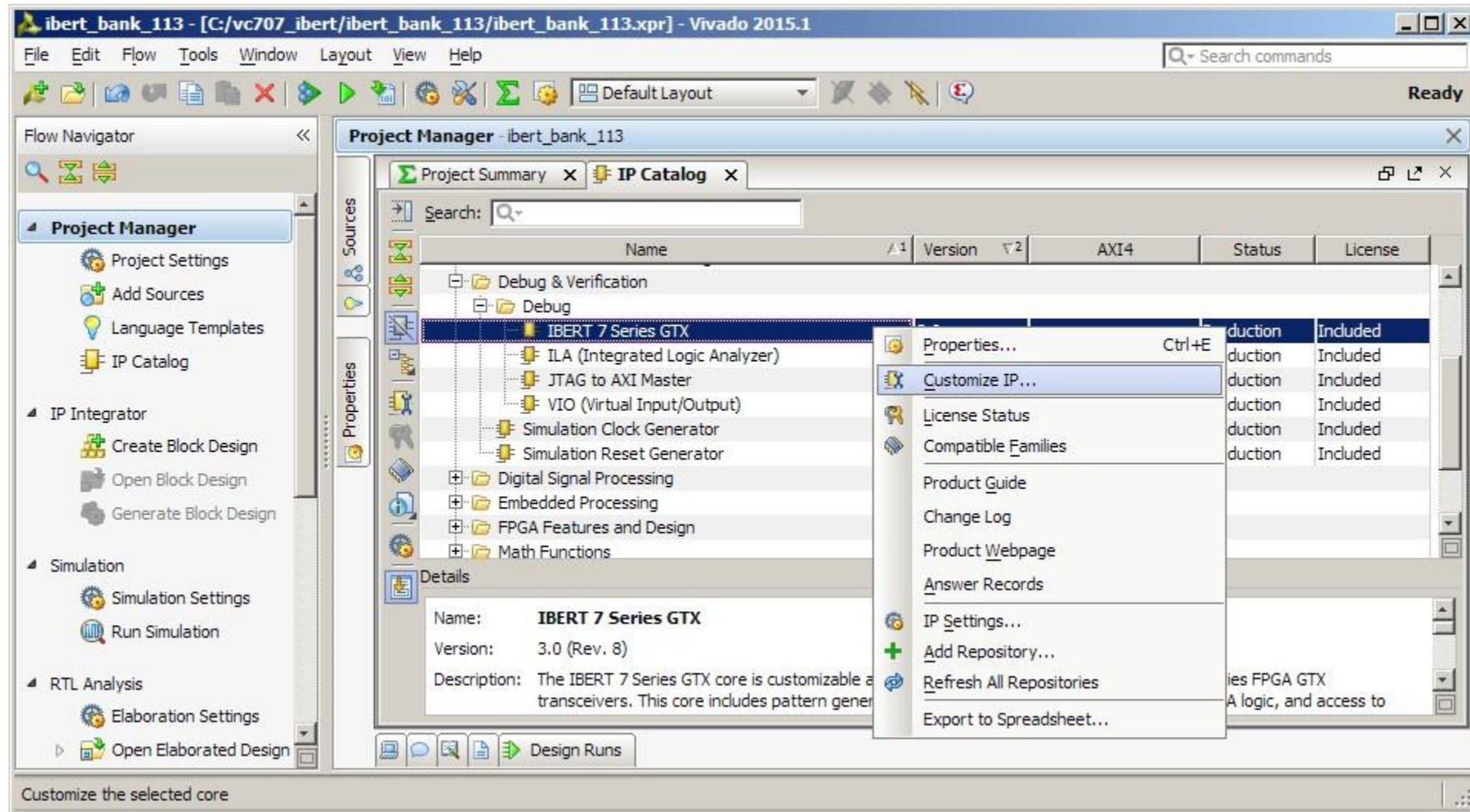
➤ Select IBERT 7 Series GTX, v3.0 under Debug & Verification



Note: Presentation applies to the VC707

Create IBERT Design for Bank 113

➤ Right click on IBERT 7 Series GTX and select Customize IP...



Note: Presentation applies to the VC707

Create IBERT Design for Bank 113

- Set the Component name: `ibert_bank_113`
- Under the Protocol Definition tab
 - Silicon Version: **General ES / Production**
 - Protocol: LineRate: **10.000**, DataWidth: **40** Refclk: **125.000** Quad Count: **1**

Customize IP

IBERT 7 Series GTX (3.0)

Documentation IP Location Switch to Defaults

☐ Show disabled ports

Component Name: `ibert_bank_113`

Protocol Definition Protocol Selection Clock Settings Summary

Silicon Version

☒ General ES/Production
☐ Initial ES

The maximum number of quads available for this device is 7

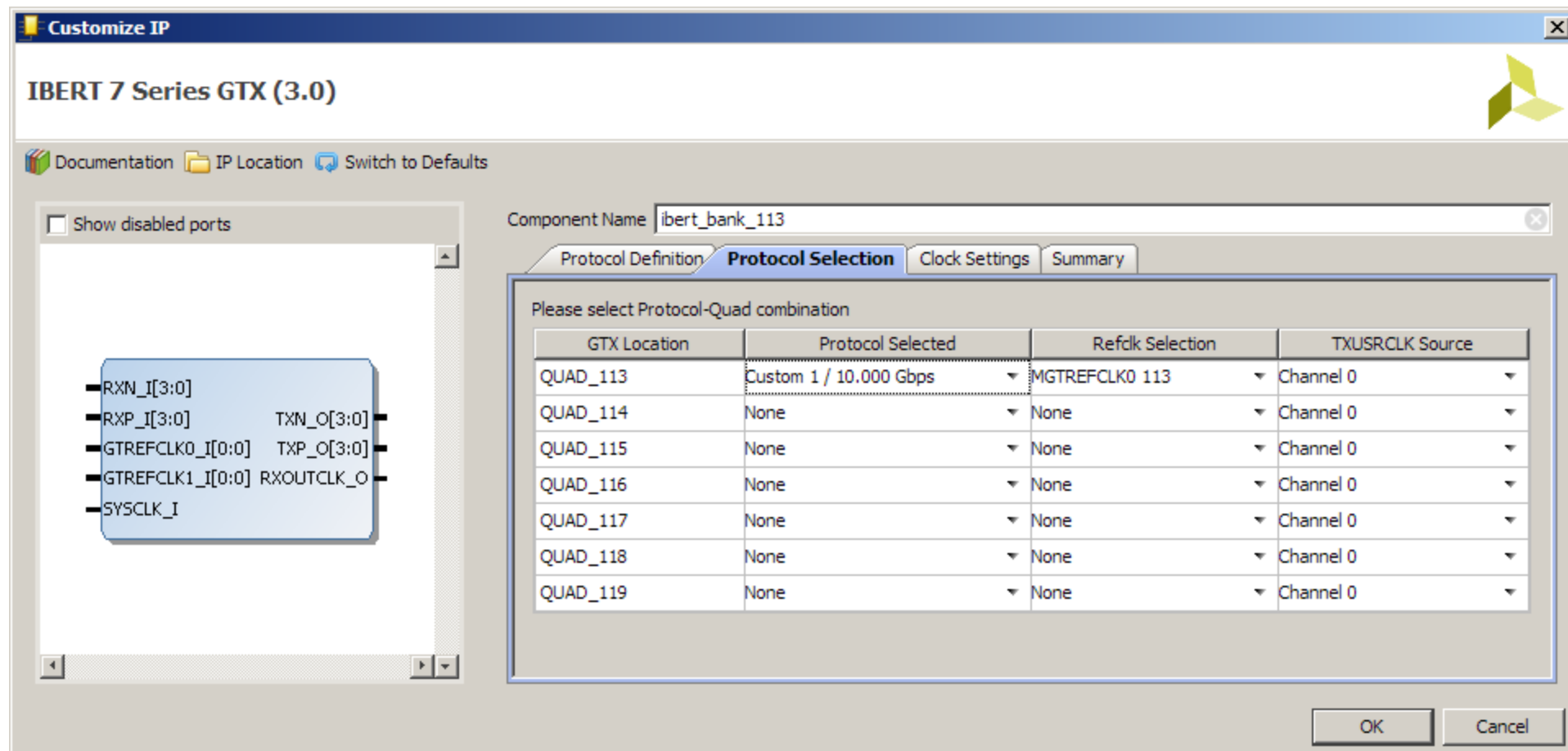
Number of Protocols: 1

Protocol	LineRate(Gbps)	DataWidth	Refclk(MHz)	Quad Count	Quad PLL
Custom 1	10.000	40	125.000	1	<input checked="" type="checkbox"/>

OK Cancel

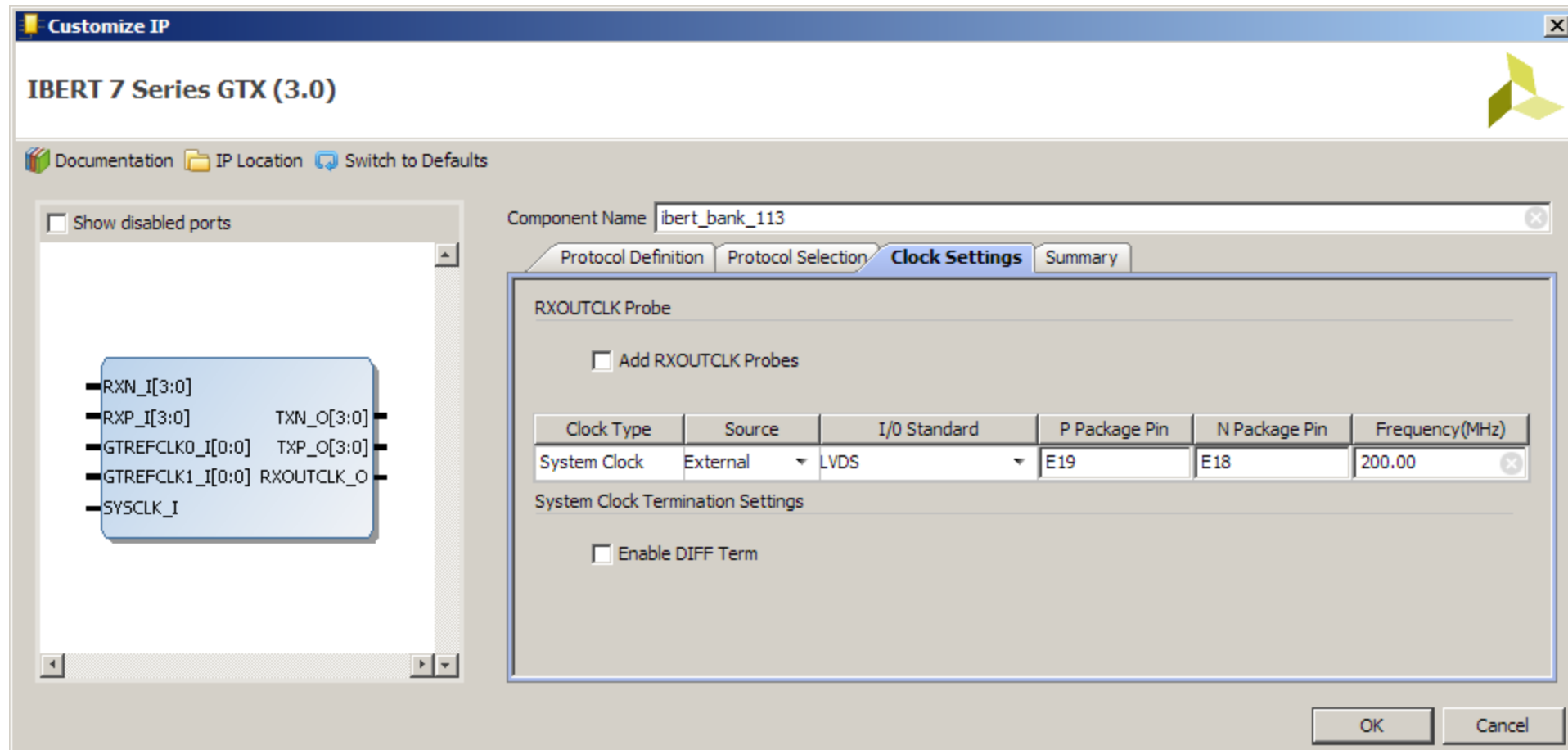
Create IBERT Design for Bank 113

- Under the Protocol Selection tab
- Set QUAD_113 to
 - Custom 1 / 10.000 Gbps, and MGTREFCLK0 113



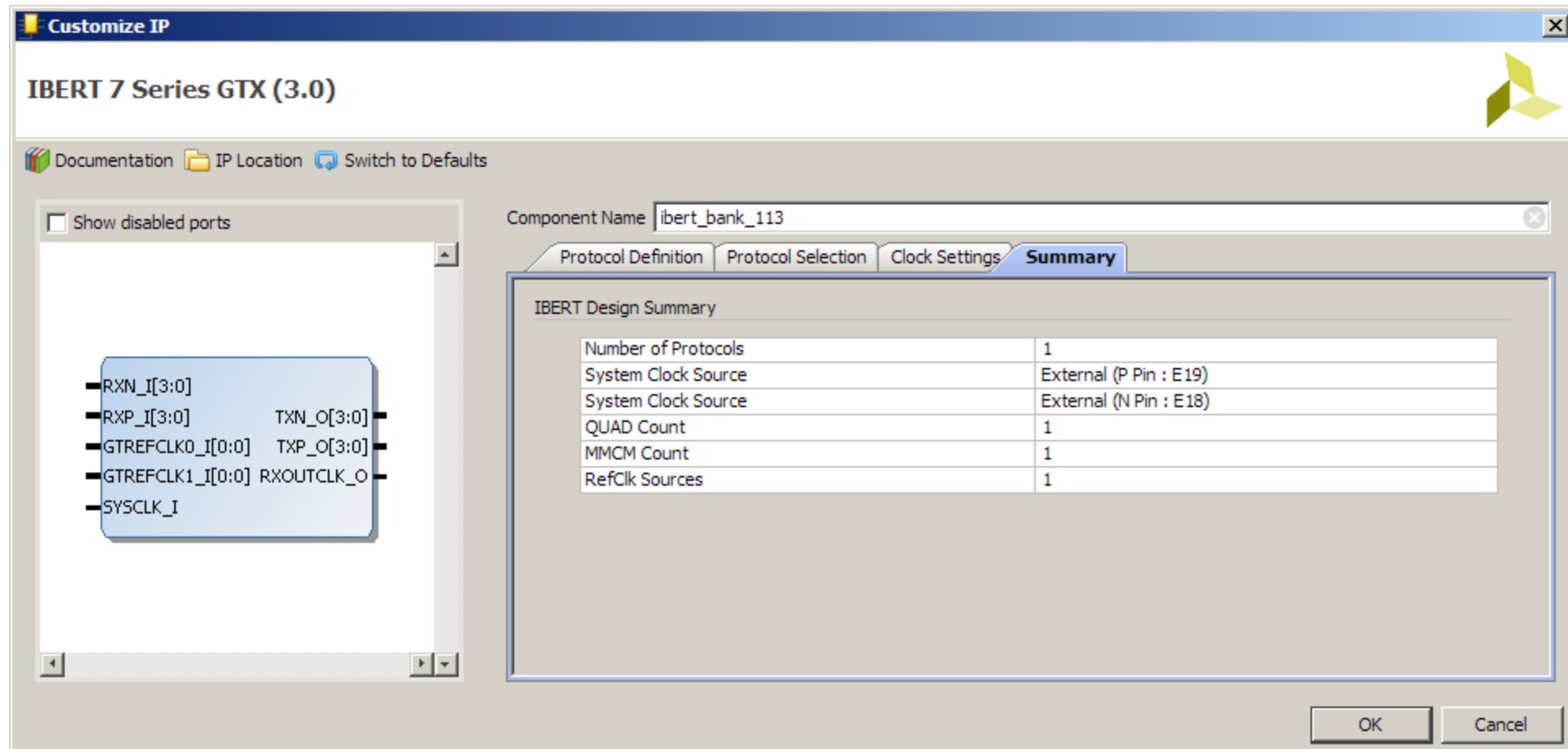
Create IBERT Design for Bank 113

- Under the Clock Settings tab, set the System Clock:
 - LVDS, P Pin Location: **E19**, N Pin Location: **E18**



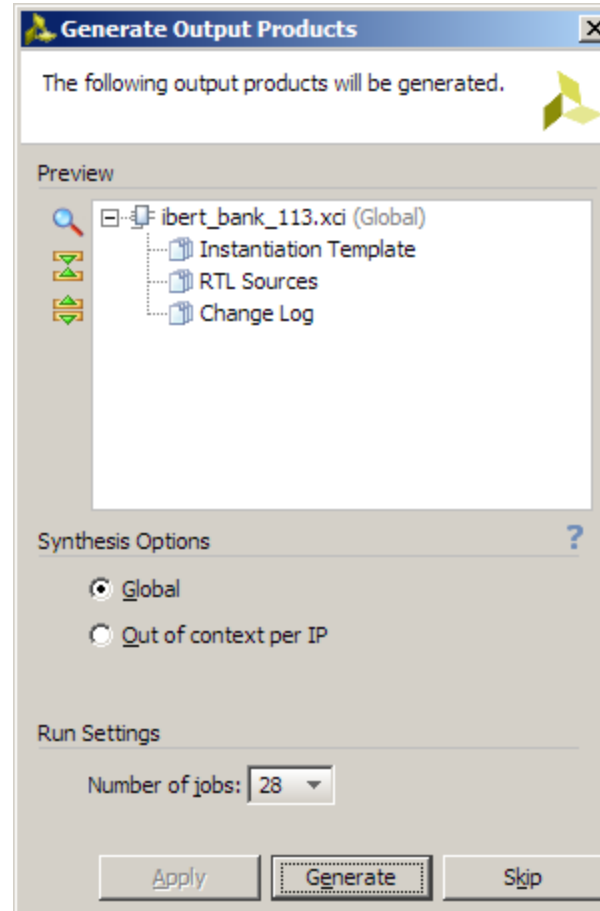
Create IBERT Design for Bank 113

➤ Review the summary and click OK



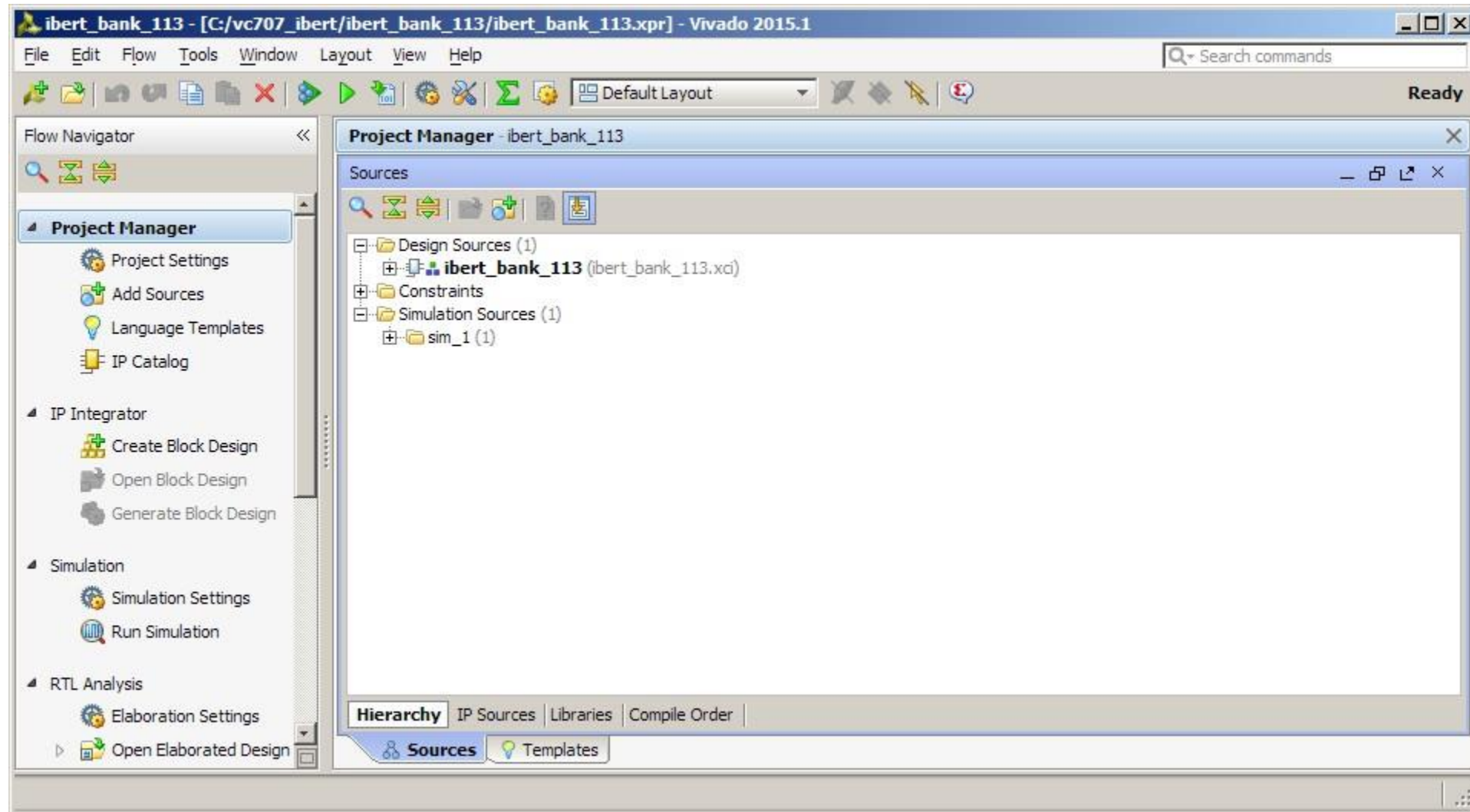
Create IBERT Design for Bank 113

➤ Click Generate



Create IBERT Design for Bank 113

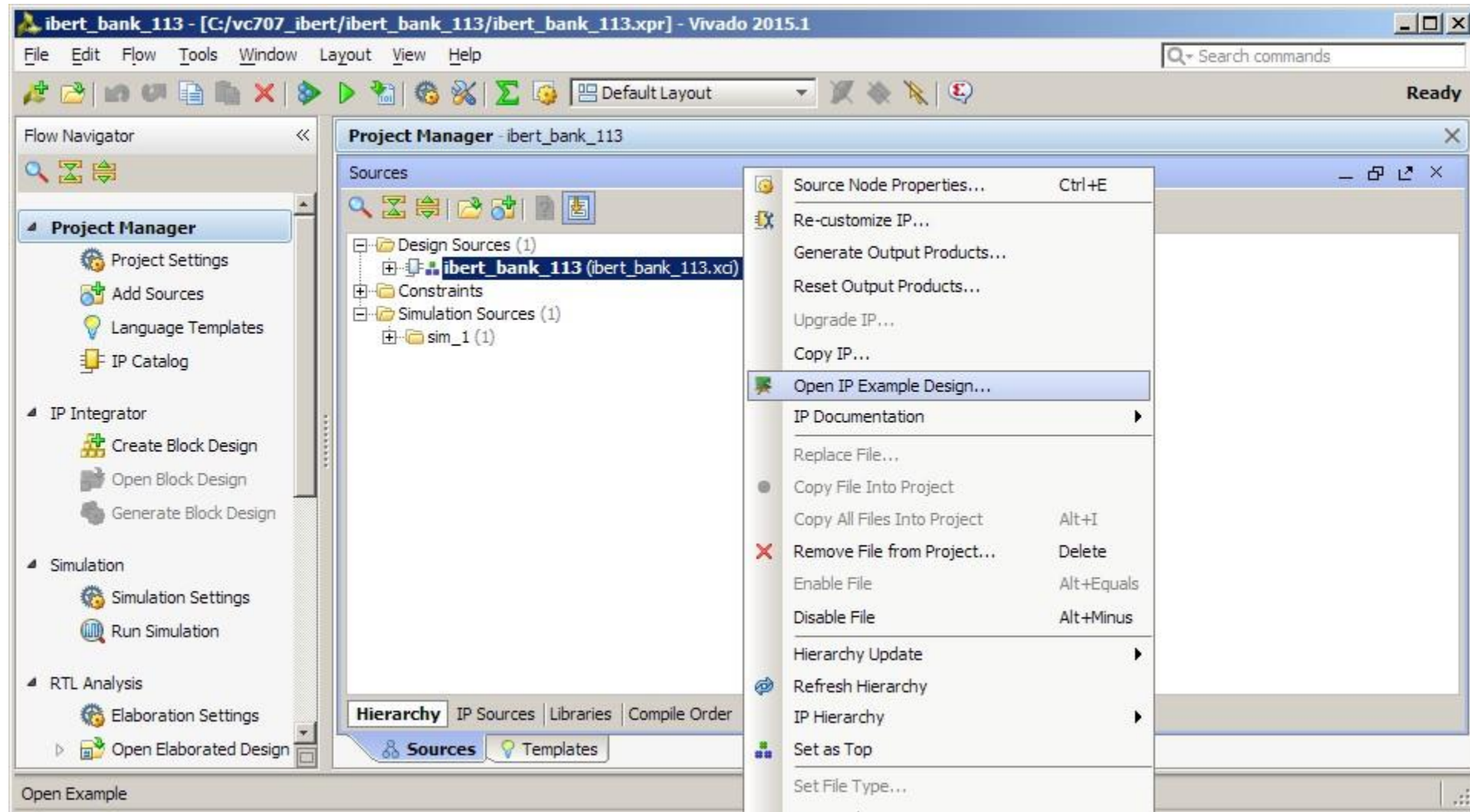
➤ Bank 113 IBERT design appears in Design Sources



Note: Presentation applies to the VC707

Compile Example Design

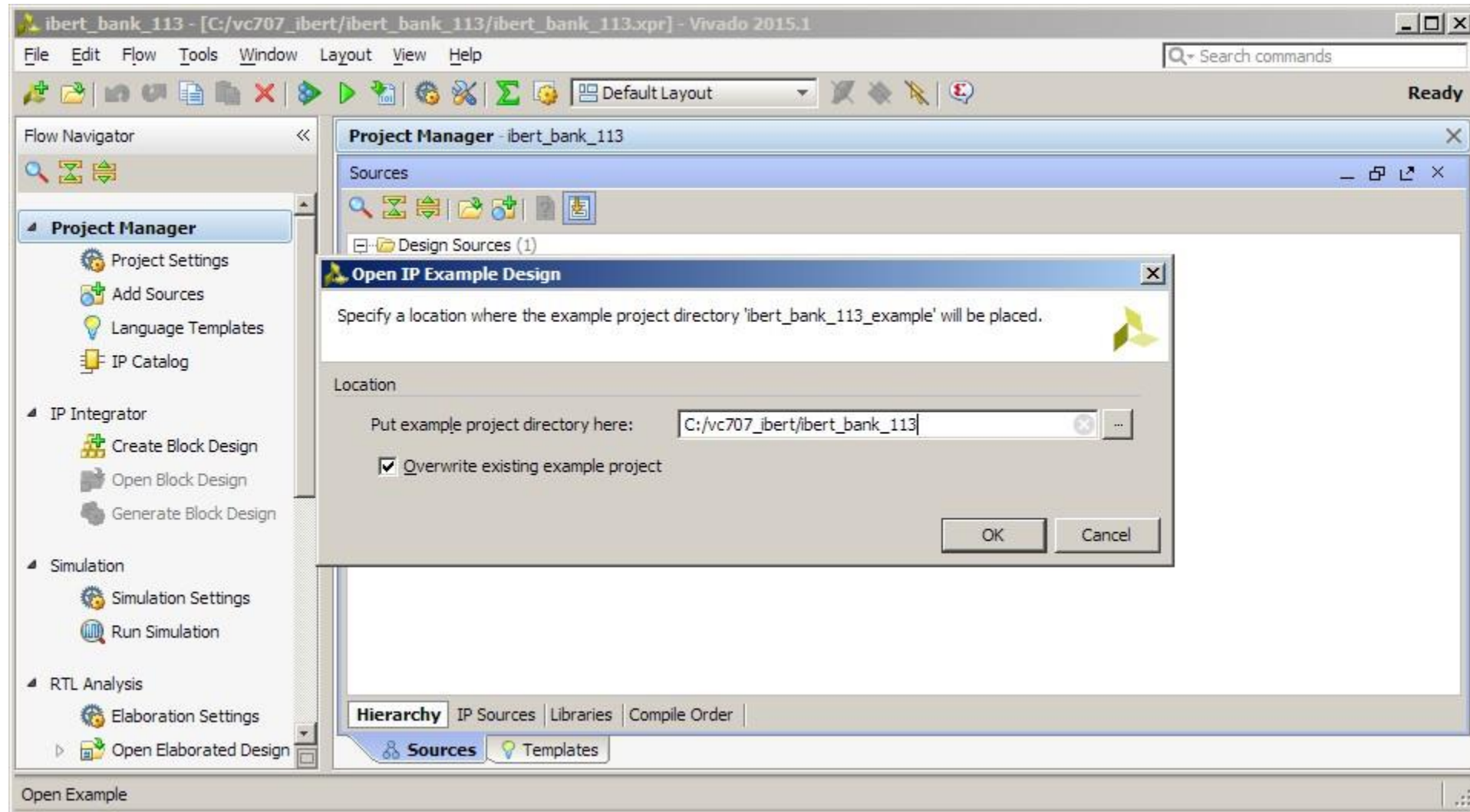
➤ Right click on `ibert_bank_113` and select **Open IP Example Design...**



Note: Presentation applies to the VC707

Compile Example Design

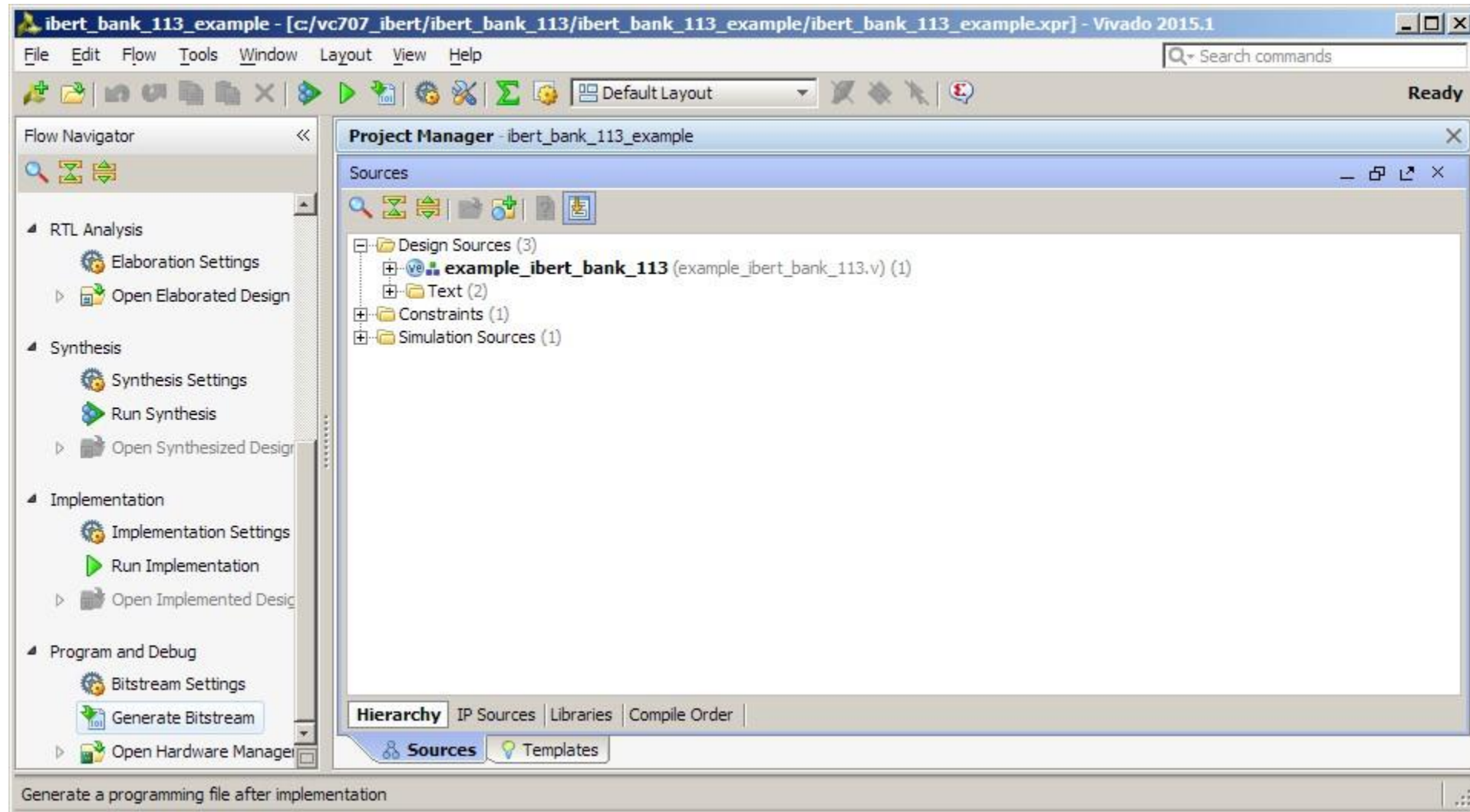
➤ Set the location to C:/vc707_ibert/ibert_bank_113 and click OK



Note: Presentation applies to the VC707

Compile Example Design

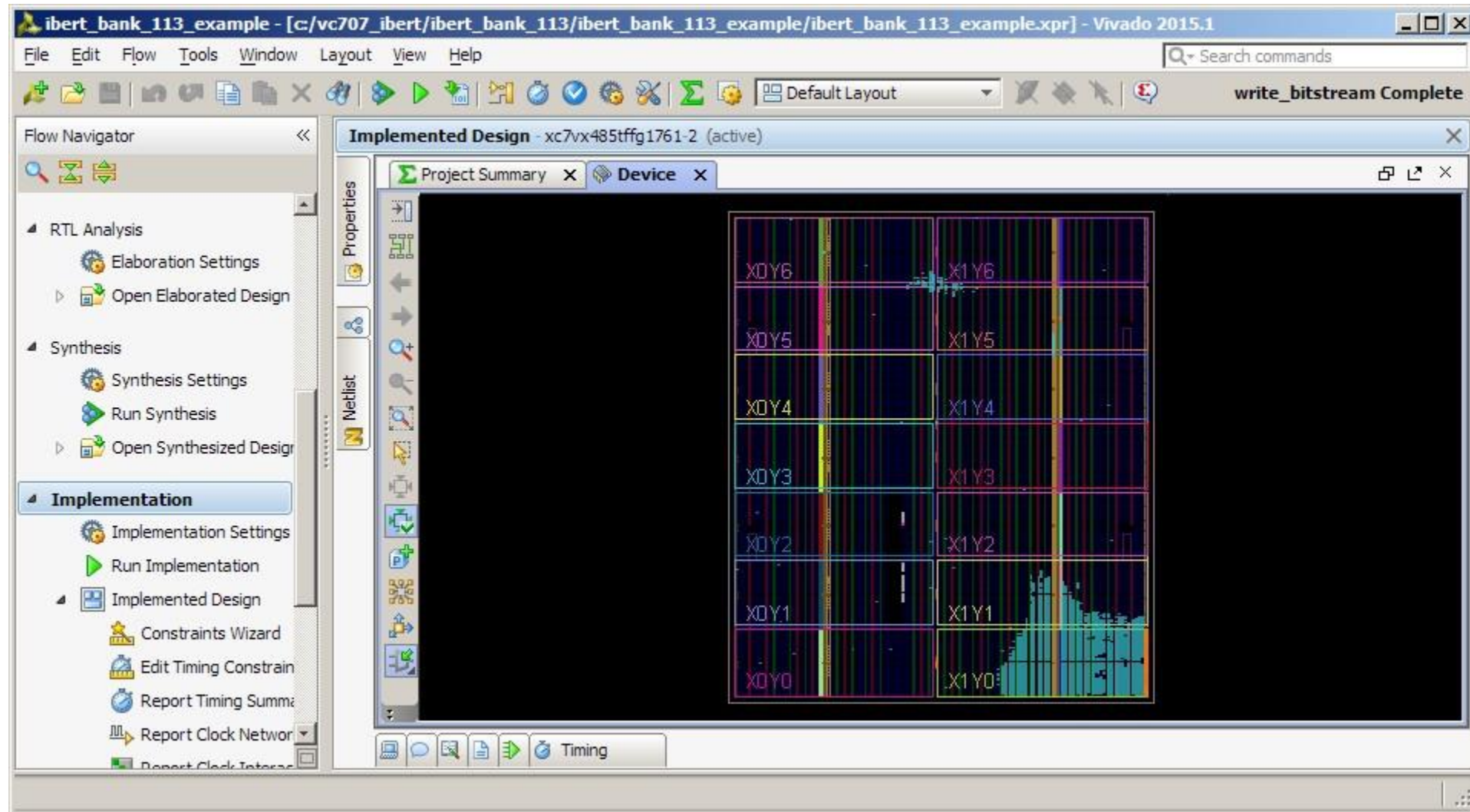
- A new project is created
- Click Generate Bitstream



Note: The original project window can be closed

Compile Example Design

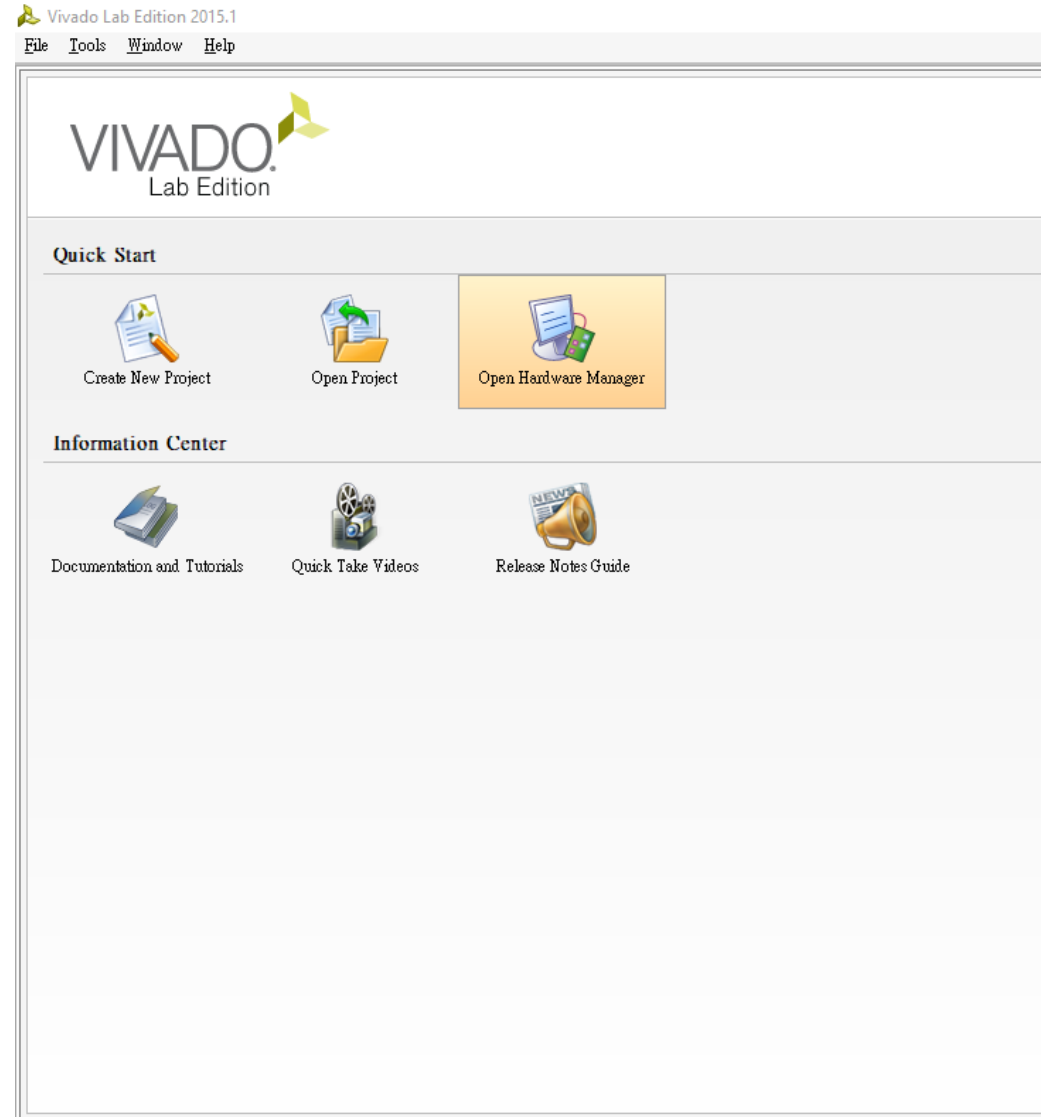
➤ Open and view the Implemented Design



Note: Presentation applies to the VC707

Open Hardware Manager(Vivado Lab 2015.1)

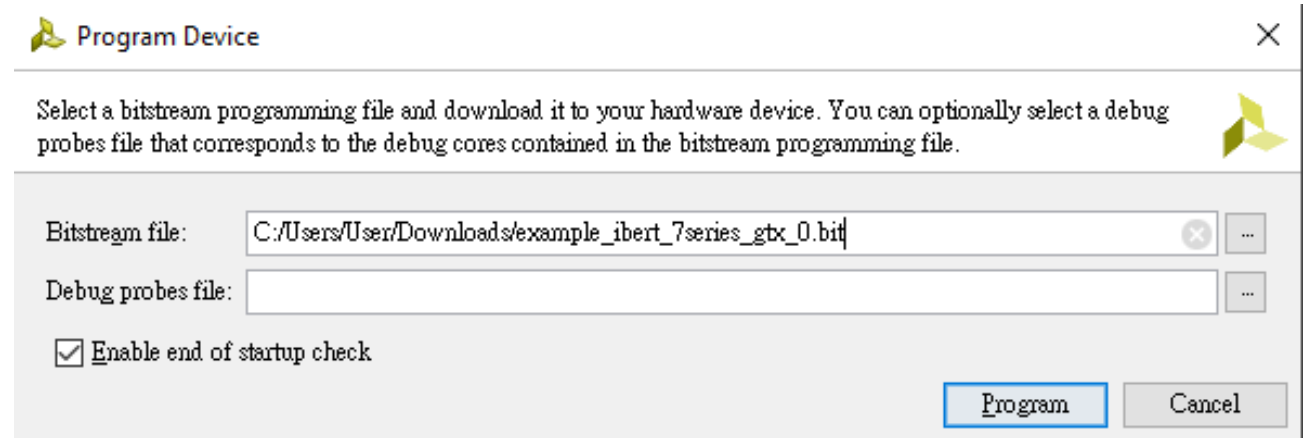
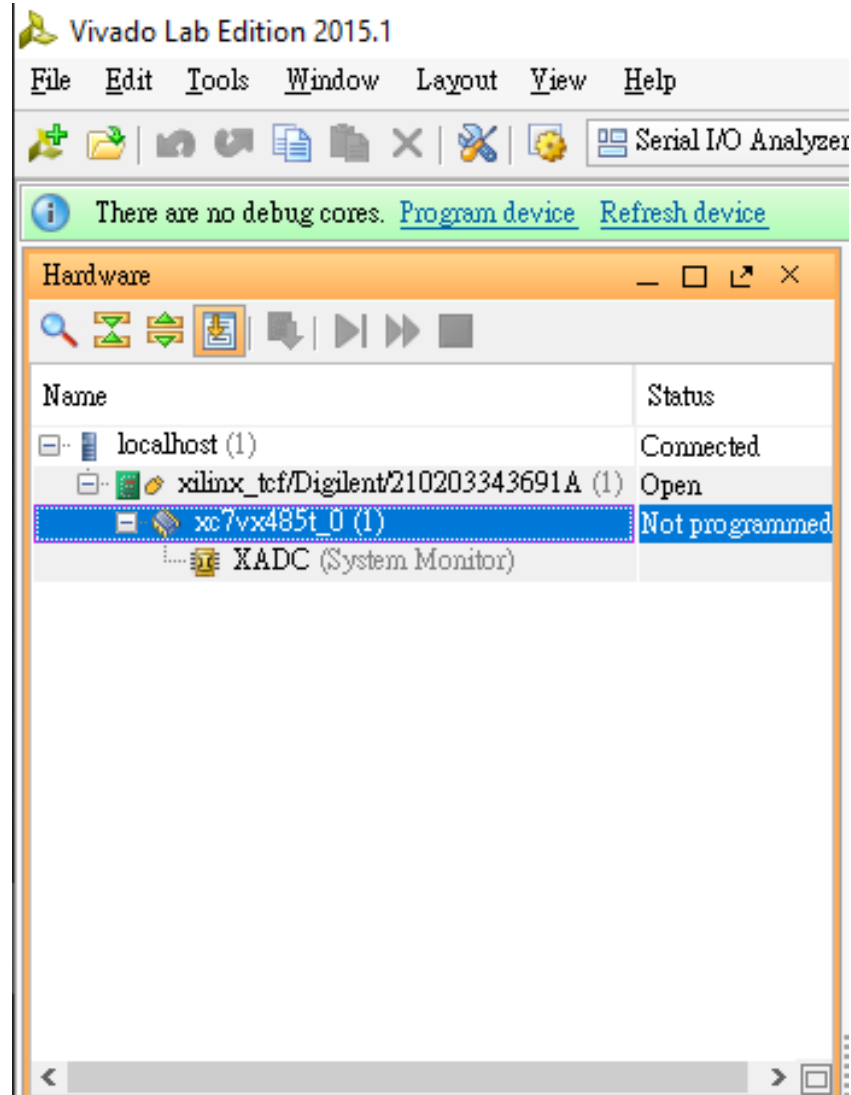
➤ Program the generated bitstream



Note: Presentation applies to the VC707

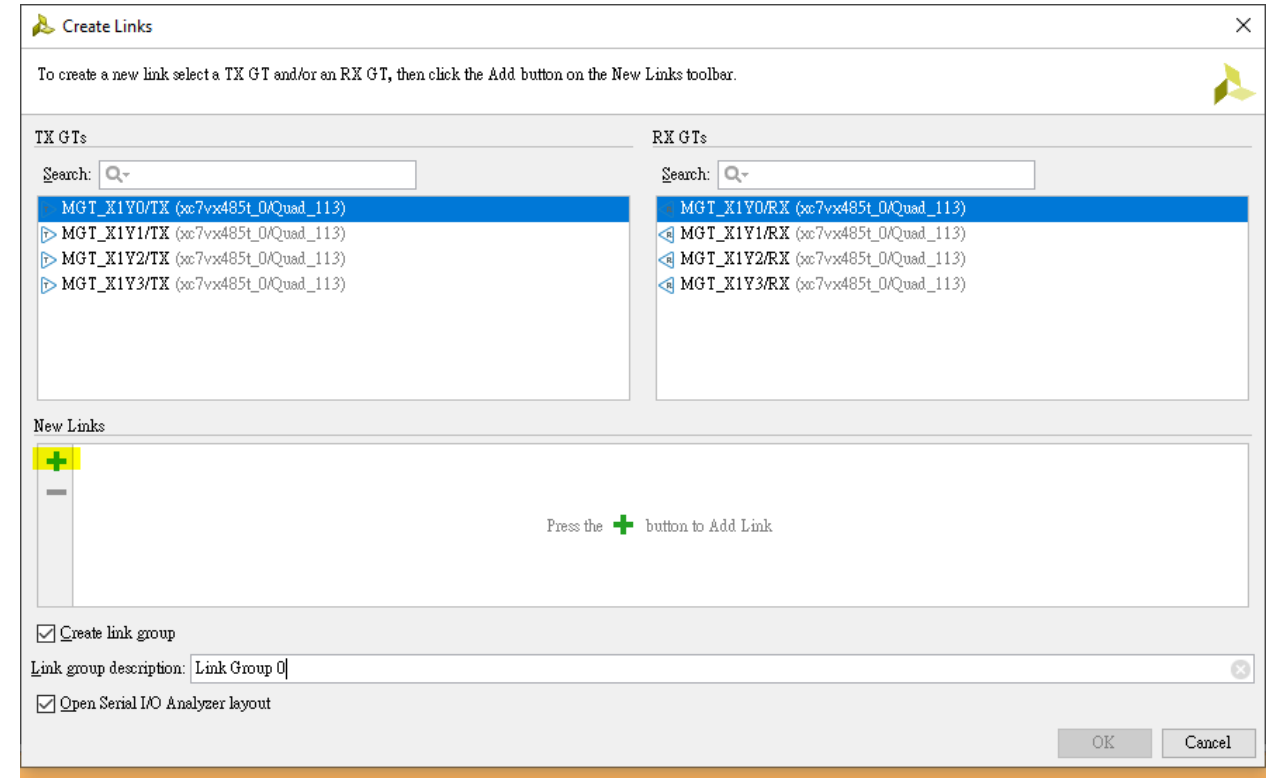
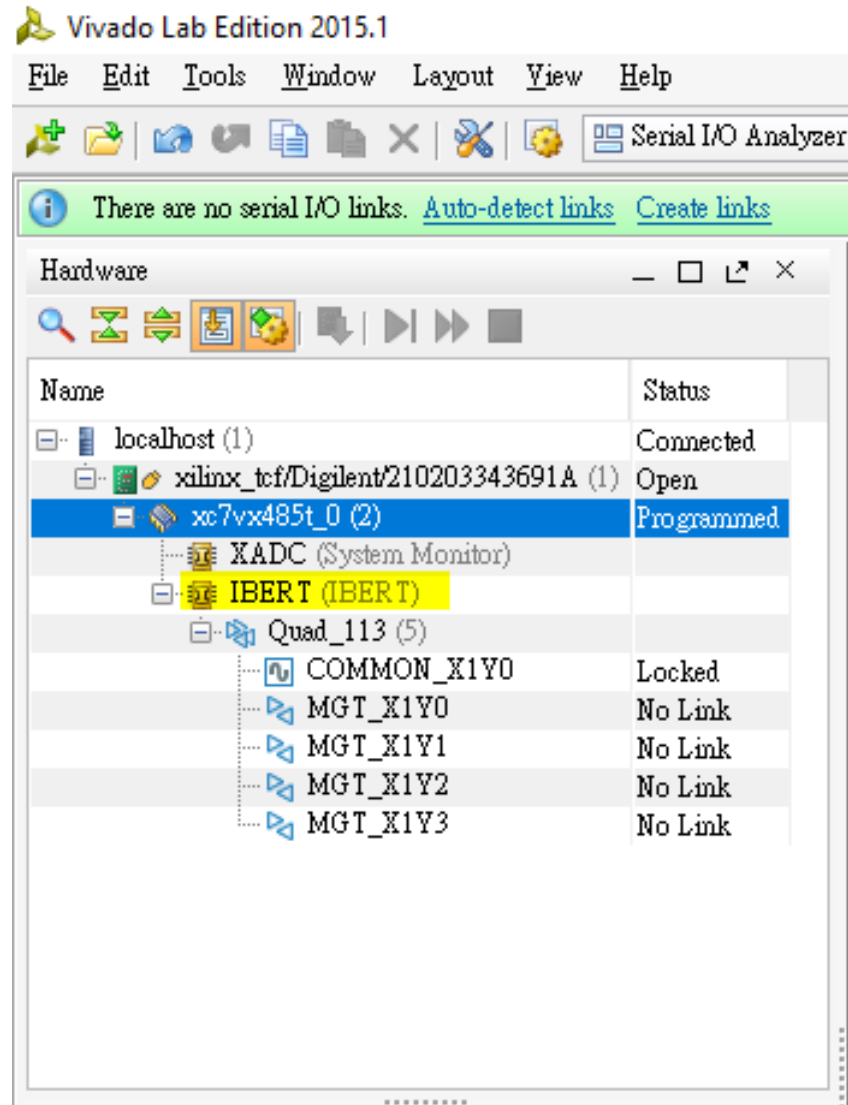
Open Hardware Manager(Vivado Lab 2015.1)

➤ Program the generated bitstream



Open Hardware Manager(Vivado Lab 2015.1)


➤ Program the generated bitstream



[Auto-detect links](#) or [create links](#) to add serial I/O links to this window.

Open Hardware Manager(Vivado Lab 2015.1)

➤ Program the generated bitstream

 **Create Links** ×

To create a new link select a TX GT and/or an RX GT, then click the Add button on the New Links toolbar.

TX GTs
Search: **TX GTs**

RX GTs
Search:

New Links

	Description	TX	RX	Internal Loopback
+	Link 0	MGT_X1Y0/TX (xc7vx485t_0/Quad_113)	MGT_X1Y0/RX (xc7vx485t_0/Quad_113)	<input checked="" type="checkbox"/>
-	Link 1	MGT_X1Y1/TX (xc7vx485t_0/Quad_113)	MGT_X1Y1/RX (xc7vx485t_0/Quad_113)	<input checked="" type="checkbox"/>
	Link 2	MGT_X1Y2/TX (xc7vx485t_0/Quad_113)	MGT_X1Y2/RX (xc7vx485t_0/Quad_113)	<input checked="" type="checkbox"/>
	Link 3	MGT_X1Y3/TX (xc7vx485t_0/Quad_113)	MGT_X1Y3/RX (xc7vx485t_0/Quad_113)	<input checked="" type="checkbox"/>

☒ Create link group
Link group description: ×
☒ Open Serial I/O Analyzer layout

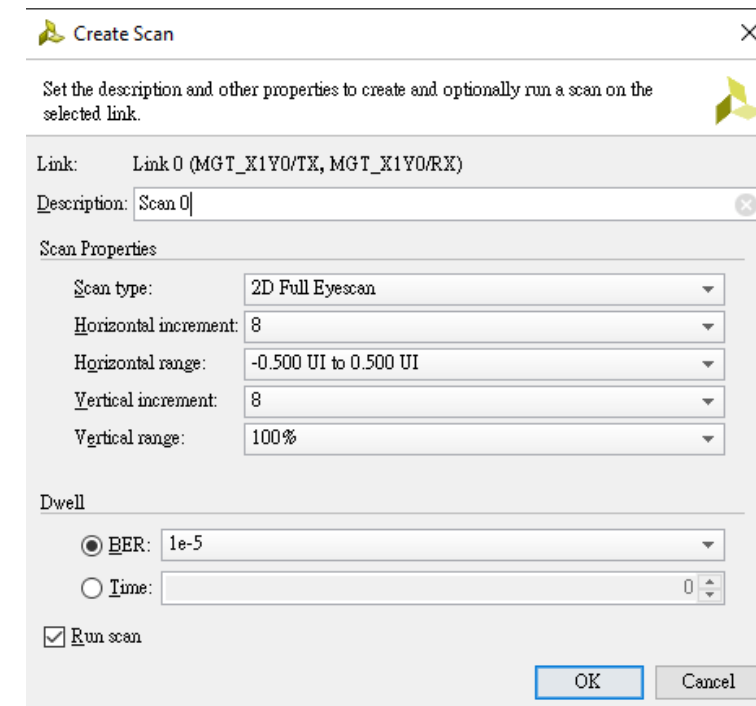
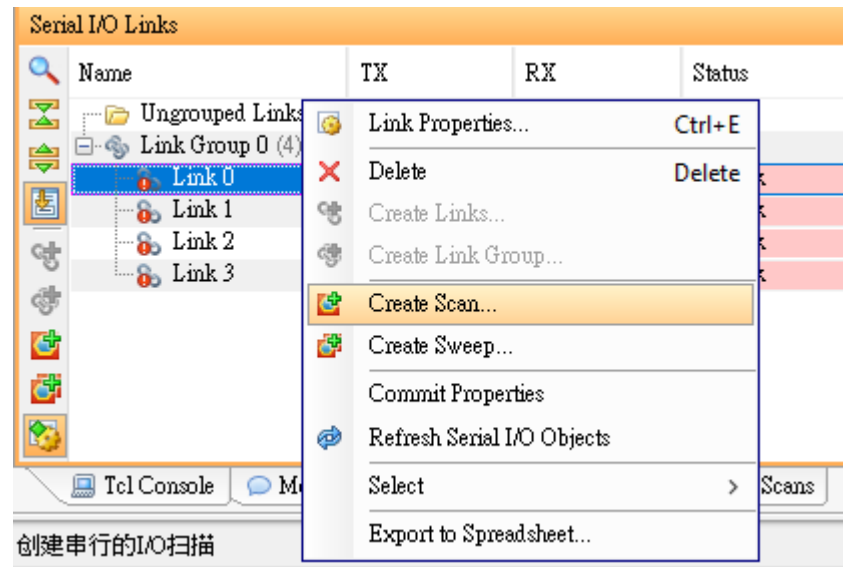
OK

Cancel

Open Hardware Manager(Vivado Lab 2015.1)

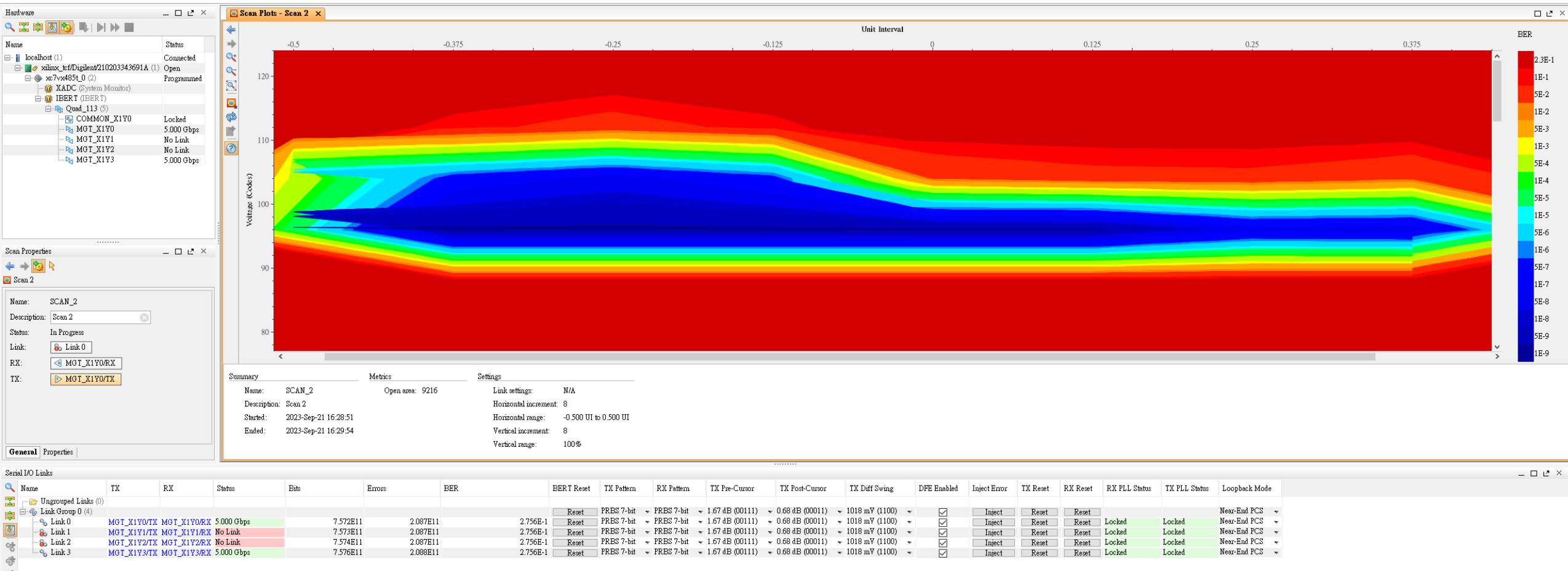
➤ Program the generated bitstream

Serial I/O Links																				
Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode	
Ungrouped Links (0)																				
Link Group 0 (4)																				
Link 0	MGT_X1Y0/TX	MGT_X1Y0/RX	5.000 Gbps	4.81E11	1.325E11	2.756E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)	<input checked="" type="checkbox"/>	Inject	Reset	Reset			Near-End PCS	
Link 1	MGT_X1Y1/TX	MGT_X1Y1/RX	5.000 Gbps	4.81E11	1.326E11	2.756E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS	
Link 2	MGT_X1Y2/TX	MGT_X1Y2/RX	No Link	4.81E11	1.326E11	2.756E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS	
Link 3	MGT_X1Y3/TX	MGT_X1Y3/RX	No Link	4.81E11	1.326E11	2.756E-1	Reset	PRBS 7-bit	PRBS 7-bit	1.67 dB (00111)	0.68 dB (00011)	1018 mV (1100)	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	Near-End PCS	



Open Hardware Manager(Vivado Lab 2015.1)

➤ Create Eye Scan





APPENDIX A: Correct IBERT Flow Following Way

1. Follow the board IBERT tutorial on Xilinx Website.



XTP499 - ZCU104 IBERT Tutorial (v4.0)

Document Type: Example Designs

Creating an Using a GTH IBERT Design with the ZCU104 board

See All Versions

Design File(s):

rdf0453-zcu104-ibert-c-2018-3.zip

2. Check the board schematic (notice the difference version cause difference pin assignment).

TITLE: Title Page SCHEM, ROHS COMPLIANT HW-Z1-ZCU104_REV1_0		ASSY P/N: 0432057 PCB P/N: 1280961 SCH P/N: 0381794 TEST P/N: TSS0189	
DATE: 01/26/2018:14:16	VER:	1.0	
SHEET SIZE: B	REV:	01	
SHEET 1 OF 58	DRAWN BY:	BP	



ZCU104 Evaluation Board

User Guide

UG1267 (v1.1) October 9, 2018

APPENDIX A: Correct IBERT Flow Following Way

3. Check the correct system clock and MGT Quad for testing.

