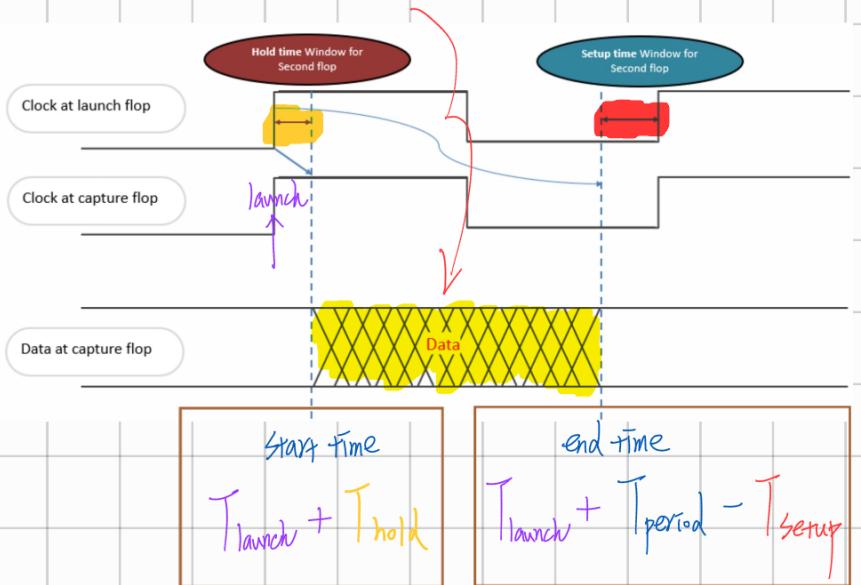


# Data Valid Window



Data Valid Window 持續時間  $\text{Clock period} - \text{Setup time} - \text{Hold time}$

計算 Setup & Hold Timing 會從 Timing Report 去剖析

Timing Summary 時序大綱

Summary					
Name	Path 2				
Slack (Hold)	0.146ns				
Source	uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg[2]C	(rising edge-triggered cell FDRE clocked by clk_out2_clk_core {rise@0.000ns fall@2.580ns period=5.161ns})			
Destination	uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg[6]D	(rising edge-triggered cell FDRE clocked by clk_out2_clk_core {rise@0.000ns fall@2.580ns period=5.161ns})			
Path Group	clk_out2_clk_core				
Path Type	Hold (Min at Fast Process Corner)				
Requirement	0.000ns (clk_out2_clk_core rise@0.000ns - clk_out2_clk_core rise@0.000ns)				
Data P... Delay	0.347ns (logic 0.125ns (35.99%) route 0.222ns (64.004%))				
Logic Levels	2 (LUT3=1 LUT5=1)				
Clock ... Skew	0.145ns				

Source Clock Path show detailed path components

Source Clock Path					
Delay Type	Incr (ns)	Path ...	Loca...	Netlist Resource(s)	
(clock clk_out2_clk_core rise edge)					
net (fo=0)	(r) 0.000	0.000		clk_pin_p	
	(r) 0.000	0.000		clk_gen_i0/clk_core_0/inst/cikin1_ibufs/DIFFINBUF_INST/DIFF_IN_P	
DIFFINBUF (Prop_DIFFINBUF_DIFF_IN_P_O)	(r) 0.098	0.098		clk_gen_i0/clk_core_0/inst/cikin1_ibufs/DIFFINBUF_INST/O	
net (fo=1, unplaced)	0.001	0.099		clk_gen_i0/clk_core_0/inst/cikin1_ibufs/IBUFCTRL_INST/I	
IBUFCTRL (Prop_IBUFCTRL_I_O)	(r) 0.000	0.099		clk_gen_i0/clk_core_0/inst/cikin1_ibufs/IBUFCTRL_INST/O	
net (fo=1, unplaced)	0.371	0.470		clk_gen_i0/clk_core_0/inst/cikin1_clk_core	
MMCME3_ADV (Prop_MMCME3_ADV_CLKIN1_CLKOUT1)	(r) -2.494	-2.024		clk_gen_i0/clk_core_0/inst/mmcme3_adv_inst/CLKOUT1	
net (fo=1, unplaced)	0.128	-1.896		clk_gen_i0/clk_core_0/inst/cikout2_clk_core	
BUFGCE (Prop_BUFGCE_I_O)	(r) 0.027	-1.869		clk_gen_i0/clk_core_0/inst/cikout2_buf0	
net (fo=149, unplaced)	1.114	-0.755		uart_tx_i0/uart_baud_gen_tx_i0/clk	
FDRE				uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg[2]C	

Data Path shows the delays and arrival time

Data Path					
Delay Type	Incr (ns)	Path ...	Loca...	Netlist Resource(s)	
FDRE (Prop_FDRE_C_Q)	(r) 0.049	-0.706		uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg[2]Q	
net (fo=7, unplaced)	0.087	-0.619		uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg_n_0[2]	
LUT3 (Prop_LUT3_I_O)	(r) 0.038	-0.581		uart_tx_i0/uart_baud_gen_tx_i0/internal_count[6]_I_2/O	
net (fo=2, unplaced)	0.123	-0.458		uart_tx_i0/uart_baud_gen_tx_i0/internal_count[6]_I_2_n_0	
LUT5 (Prop_LUT5_I_O)	(r) 0.038	-0.420		uart_tx_i0/uart_baud_gen_tx_i0/internal_count[6]_I_1/O	
net (fo=1, unplaced)	0.042	-0.400		uart_tx_i0/uart_baud_gen_tx_i0/internal_count[6]_I_1_n_0	

net (t0=1, unplaced)	0.012	-0.408	uart_tx_i0/uart_baud_gen_tx_i0/internal_count[0]
FDSE			
Arrival Time		-0.408	uart_tx_i0/uart_baud_gen_tx_i0/internal_count[0]

Destination Clock Path shows the delay's and required time

Destination Clock Path				
Delay Type	Incr (ns)	Path (ns)	Loca...	Netlist Resource(s)
(clock clk_out2_clk_core rise edge)				(r) 0.000 0.000 clk_pin_p
net (fo=0)				clk_gen_i0/clk_core_i0/inst/clkin1_ibufs/ clk_gen_i0/clk_core_i0/inst/clkin1_ibufs/DIFFINBUF_INST/0
DIFFINBUF (Prop_DIFFINBUF_DIFF_IN_P_Q)	(r) 0.280	0.280		clk_gen_i0/clk_core_i0/inst/clkin1_ibufs/DIFFINBUF_INST/0
net (fo=1, unplaced)	0.001	0.281		clk_gen_i0/clk_core_i0/inst/clkin1_ibufs/OUT
IBUFCTRL (Prop_IBUFCTRL_I_O)	(r) 0.000	0.281		clk_gen_i0/clk_core_i0/inst/clkin1_ibufs/IBUFCTRL_INST/0
net (fo=1, unplaced)	0.417	0.698		clk_gen_i0/clk_core_i0/inst/clk_in1_clk_core
MMCME3_ADV (Prop_MMCM_ADV_CLKIN1_CLKOUT1)	(r) -2.849	-2.151		clk_gen_i0/clk_core_i0/inst/mmcme3_adv_inst/CLKOUT1
net (fo=1, unplaced)	0.176	-1.975		clk_gen_i0/clk_core_i0/inst/clk_out2_clk_core
BUFGE (Prop_BUFGE_I_O)	(r) 0.031	-1.944		clk_gen_i0/clk_core_i0/inst/clkout2_buf
net (fo=149, unplaced)	1.259	-0.685		uart_tx_i0/uart_baud_gen_tx_i0/clk
FDSE				uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg[6]/D
clock pessimism	0.075	-0.610		
FDSE (Hold FDSE_C_D)	0.056	-0.554		uart_tx_i0/uart_baud_gen_tx_i0/internal_count_reg[6]

⇒ Slack is based on arrival time for required time calculation

## Setup Time Check Path Delays

Source Clock Path				
Delay Type	Incr (ns)	Path (ns)	Location	Netlist Resource(s)
FDPE				
MMCME3_ADV_CLKOUT0	(r) -5.039	-3.536	Site: SLICE_X54Y82	rst_gen_i0/reset_bridge_clk_rx_i0/rst_dst/reg/C
(clock clk_out...re rise edge)	(r) 0.000	0.000	Site: MMCME3_ADV_X1Y2	clk_gen_i0/clk_core_i0/inst/mmcme3_adv_inst/CLKOUT0
IBUFCTRL (Pr_I_HPIOB_I_O)	(r) 0.000	0.000	Site: G9	clk_gen_i0/clk_core_i0/inst/clkin1_ibufs/IBUFCTRL_INST/0
BUFGE (Prop_BUFGE_I_O)	0.638	0.638	Site: G9	clk_gen_i0/clk_core_i0/inst/clkout1_buf
DIFFINBUF (P_IFF_IN_P_Q)	(r) 0.083	-3.050	Site: BUFGE_X1Y62	clk_gen_i0/clk_core_i0/inst/clkin1_ibufs/DIFFINBUF_INST/0
net (fo=0)	0.548	0.548	Site: HPIOBDIFFINBUF_X1Y58	clk_gen_i0/clk_core_i0/inst/clkin1_ibufs/DIFFINBUF_INST/0
net (fo=1, routed)	0.000	0.000		clk_gen_i0/clk_core_i0/inst/clkin1_ibufs/OUT
net (fo=1, routed)	0.090	0.638		clk_gen_i0/clk_core_i0/inst/clk_out1_clk_core
net (fo=1, routed)	0.403	-3.133		clk_gen_i0/clk_core_i0/inst/clk_in1_clk_core
net (fo=1, routed)	0.655	1.503		rst_gen_i0/reset_bridge_clk_rx_i0/clk_dst
net (fo=258, routed)	2.714	-0.336	Clock region: ... (CLOCK_ROOT)	
Data Path				
Delay Type	Path (ns)	Incr (ns)	Location	Netlist Resource(s)
FDPE (Prop_E_SLICE_C_Q)	-0.222	(r) 0.114	Site: SLICE_X54Y82	rst_gen_i0/reset_bridge_clk_rx_i0/rst_dst/reg/Q
net (fo=248, routed)	2.755	2.977		clk_pre_i0/rst_clk_src
FDRE				clk_pre_i0/bus_samp_src/reg[11]/R
Arrival Time	2.755			Arrival time
Destination Clock Path				
Delay Type	Incr (ns)	Path(ns)	Location	Netlist Resource(s)
MMCME3_ADV_CLKOUT0	(r) 0.000	4.995	Site: G9	clk_pin_p
(clock clk_out...re rise edge)	(r) 4.999	4.999		
IBUFCTRL (Pr_I_HPIOB_I_O)	(r) 0.075	1.943	Site: BUFGE_X1Y62	clk_gen_i0/clk_core_i0/inst/clkout1_buf
DIFFINBUF (P_IFF_IN_P_Q)	(r) 0.390	5.390	Site: HPIOBDIFFINBUF_X1Y58	clk_gen_i0/clk_core_i0/inst/clkin1_ibufs/DIFFINBUF_INST/0
FDRE			Site: SLICE_X31Y151	clk_gen_i0/clk_core_i0/inst/clkin1_ibufs/OUT
FDRE (Setup_SLICE_C_R)	-0.083	4.054	Site: SLICE_X31Y151	clk_gen_i0/clk_core_i0/inst/clk_out1_clk_core
IBUFCTRL (Pr_I_HPIOB_I_O)	(r) 0.000	5.441	Site: G9	clk_gen_i0/clk_core_i0/inst/clk_in1_clk_core
MMCME3_ADV_CLKOUT0	(r) -4.696	1.523	Site: MMCME3_ADV_X1Y2	rst_gen_i0/reset_bridge_clk_rx_i0/clk_dst
Required Time	4.054			Required time

Setup slack

= Required time - Arrival time > 0

→ Destination delay starts at the next clock edge

## Hold Time Check Path Delays

Location	Delay type	Incr (ns)	Path(ns)	Netlist Resource(s)
(clock clk_pin_p rise edge)				
AD12	net (fo=0)	0.000	0.000 r	clk_pin_p
AD12	ISBUF (Prop_ibufds_I_O)	0.000	0.000 r	clk_pin_p
BUFCTRL_XOYO	net (fo=1, routed)	0.398	0.398 r	IBUFCTRL_clk_i0/0
SLICE_X10Y196	BUFQ (Prop_bufq_I_O)	1.083	1.083 r	clk_i
SLICE_X10Y196	net (fo=49, routed)	0.026	1.497 r	BUFQ_clk_rx_i0/0
SLICE_X10Y196		0.591	2.098 r	uart_rx_i0/uart_baud_gen_rx_i0/clk_rx
SLICE_X10Y196			r	uart_rx_i0/uart_baud_gen_rx_i0/internal_count_reg[2]/C
SLICE_X10Y196	FDSE (Prop_fdse_C_Q)	0.118	2.206 r	uart_rx_i0/uart_baud_gen_rx_i0/internal_count_reg[2]/Q
SLICE_X10Y196	net (fo=7, routed)	0.151	2.358 r	uart_rx_i0/uart_baud_gen_rx_i0/internal_count[2]
SLICE_X10Y196	LUT6 (Prop_lut6_I3_O)	0.028	2.386 r	uart_rx_i0/uart_baud_gen_rx_i0/internal_count_reg[6]_1/0
SLICE_X10Y196	net (fo=1, routed)	0.000	2.386 r	uart_rx_i0/uart_baud_gen_rx_i0/n/internal_count_reg[6]/D
(clock clk_pin_p rise edge)				
AD12	net (fo=0)	0.000	0.000 r	clk_pin_p
AD12	ISBUF (Prop_ibufds_I_O)	0.470	0.470 r	IBUFCTRL_clk_i0/0
BUFCTRL_XOYO	net (fo=1, routed)	1.154	1.624	clk_i
BUFCTRL_XOYO	BUFQ (Prop_bufq_I_O)	0.030	1.654 r	BUFQ_clk_rx_i0/0
SLICE_X10Y196	net (fo=49, routed)	0.792	2.446 r	uart_rx_i0/uart_baud_gen_rx_i0/clk_rx
SLICE_X10Y196	clock pessimism	-0.346	2.099 r	uart_rx_i0/uart_baud_gen_rx_i0/internal_count_reg[6]/C
SLICE_X10Y196	FDSE (Hold_fdse_C_D)	0.060	2.159 r	uart_rx_i0/uart_baud_gen_rx_i0/internal_count_reg[6]

Hold slack

= Arrival time - Required time > 0

→ Destination delay starts at the same clock edge

If there are multiple source clock and destination clock combinations, Vivado will choose the most compact timing

## Input / Output Timing Analysis

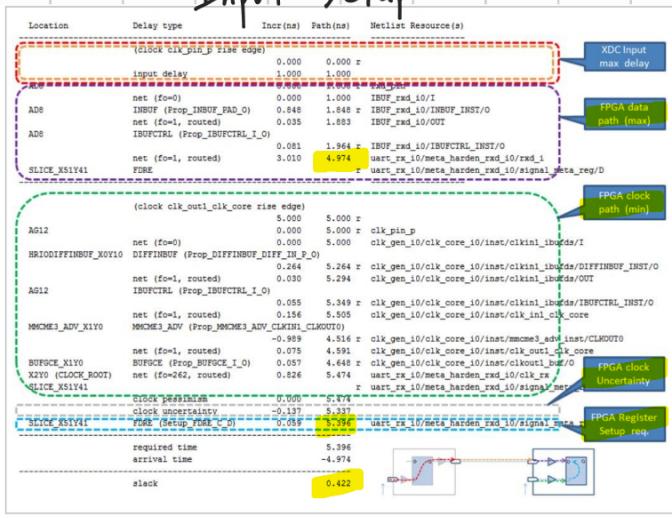
### Input Setup Timing Analysis

- Max Upstream device delay
- Max Board trace delay
- Max FPGA data path
- Min Destination (FPGA) clock path
- Setup requirement
- Clock Uncertainty

### Input Hold Timing Analysis

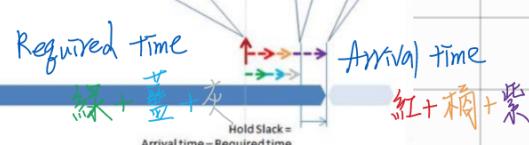
- Min Upstream device delay
- Min Board trace delay
- Min FPGA data path
- Max Destination (FPGA) clock path
- Hold requirement
- Clock Uncertainty

## Input Setup

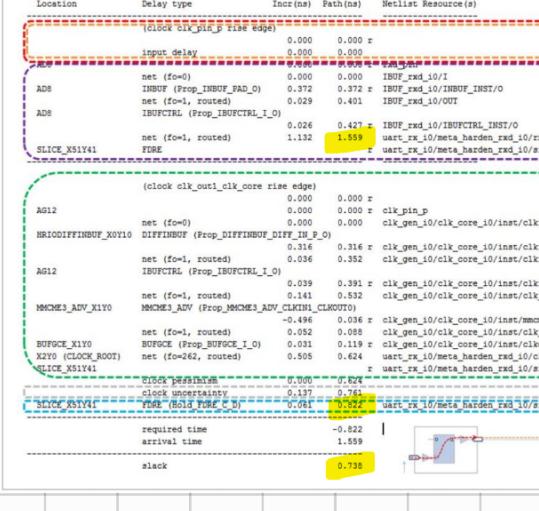


Required time 紅+藍+灰

Setup Slack = Required time - Arrival time  
綠+藍+灰



## Input Hold



### Output Setup Timing Analysis

- Max FPGA clock path delay
- Max FPGA data path
- Min Board trace delay
- Downstream Setup requirement
- Clock Uncertainty

### Output Hold Timing Analysis

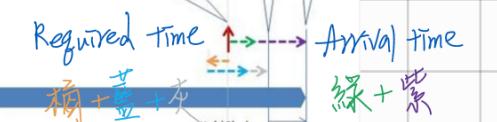
- Min FPGA clock path delay
- Min FPGA data path
- Min Board trace delay
- Downstream Hold requirement
- Clock Uncertainty

## Output Setup



Required time 紅+藍+灰

Setup Slack = Required time - Arrival time  
綠+藍+灰



## Output Hold

# 統整小結

各 Constraints Tel 下

Constraints	Description
Reg-to-reg constraints	create_clock
Input-to-reg constraints	set_input_delay
Reg-to-output constraints	set_output_delay
Input-to-output constraints	set_max_delay/set_min_delay
Timing exceptions	set_false_path, set_multicycle_path
Clock constraints	set_clock_uncertainty, jitter, set_clock_latency, set_clock_groups

## Q question

### True or False Question

When a hold value is calculated, the output delay value is subtracted from the destination delay value.

- True
- False

