



VC707 Test Pattern Generator Flow

Field Application Engineer

Adaptive and Embedded Computing Group (AECG)

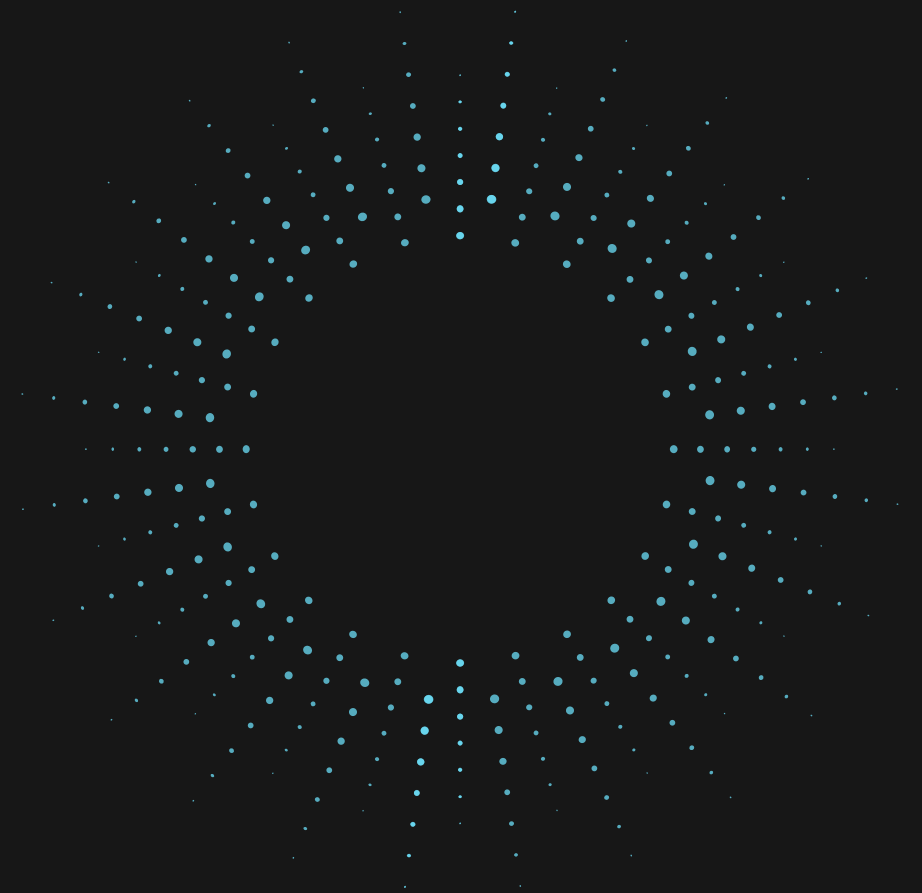
Revision History

Date	Version	Description
10/25/23	1.1	Fix block design bug on page 4, .24, 25 and add new problem on page 40.
10/24/23	1.0	Initial version for flow introduction.

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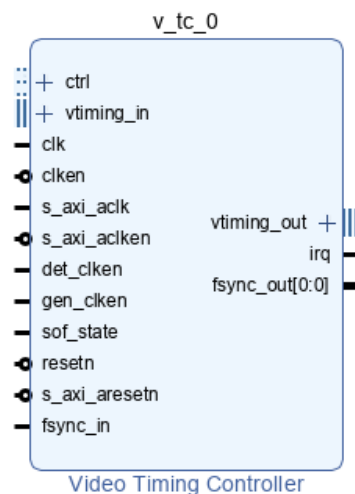
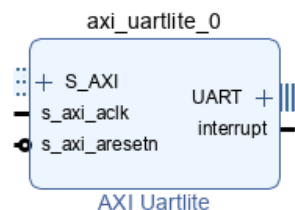
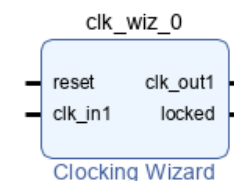
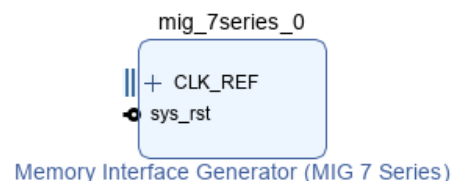
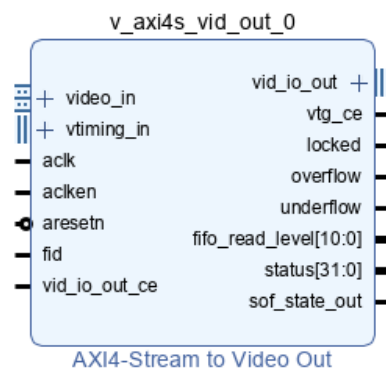
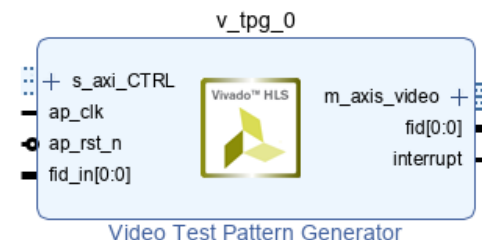
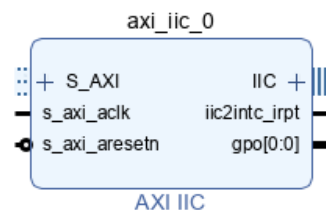
Vivado 2021.1 Part



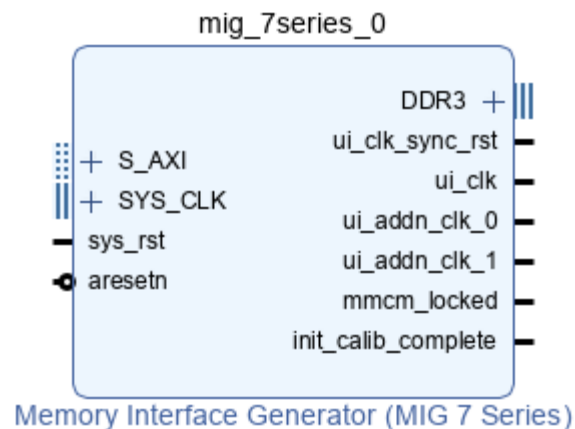
VC707 Test Pattern Generator Flow

Block Design Steps

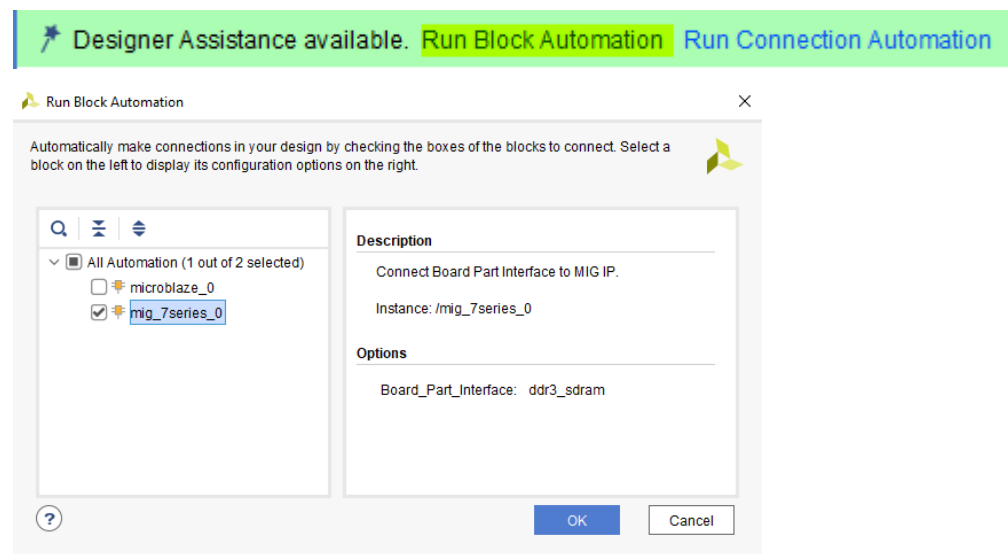
先召喚出這幾個 IP



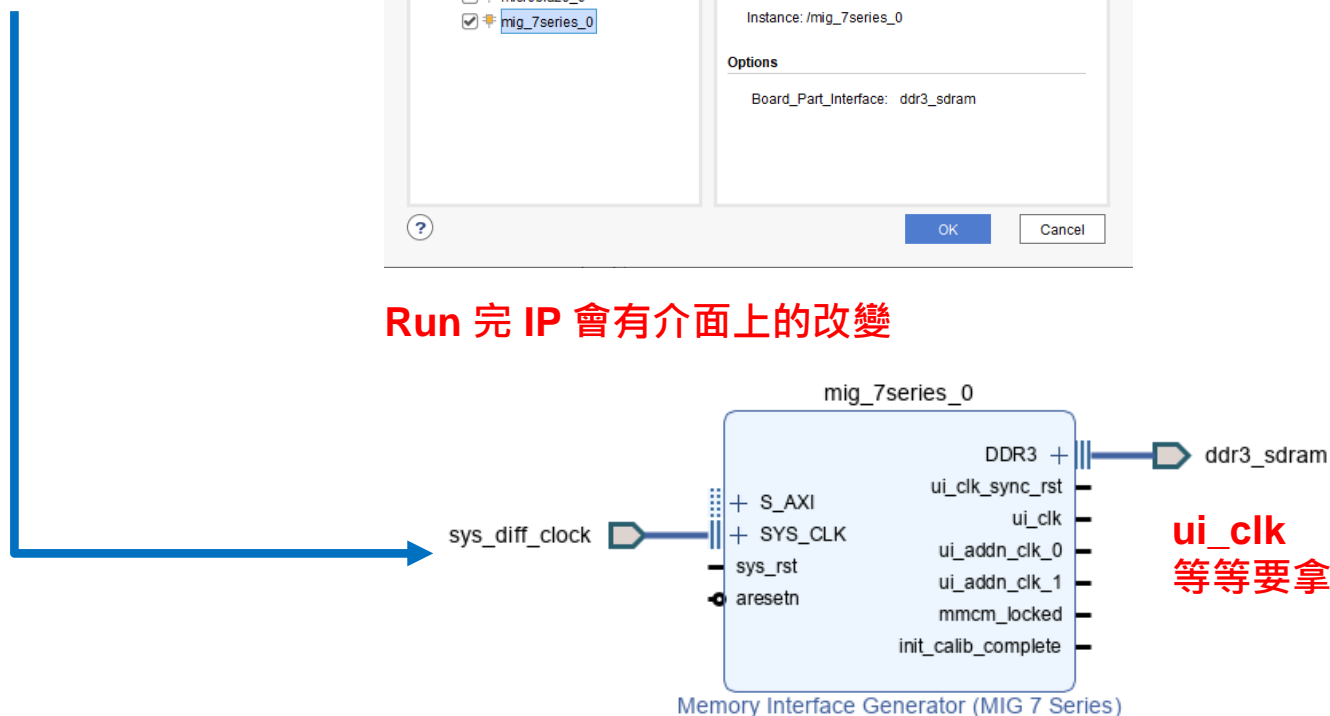
VC707 Test Pattern Generator Flow – MIG 7 Series



DDR3，影像緩存用
點選 Block Automation

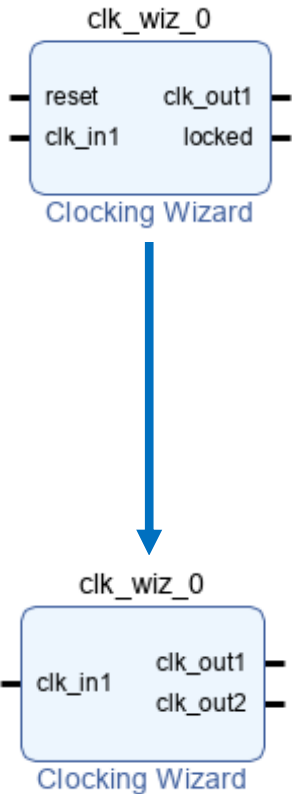


Run 完 IP 會有介面上的改變



ui_clk
等等要拿來接 clocking wizard 的 input

VC707 Test Pattern Generator Flow – clocking wizard



會分出兩個 clock 分別是 100MHz 和 148.5MHz
100MHz 給 Microblaze 吃，148.5MHz 給解析度 1080P 吃

Re-customize IP

Clocking Wizard (6.0)

Documentation IP Location

Component Name: clk_wiz_0

Board	Clocking Options	Output Clocks	MMCM Settings	Summary						
		Requested	Actual	Requested	Actual	Requested	Actual	BUFG	Fine PS	of buffer
<input checked="" type="checkbox"/>	clk_out1	100.000	100.000000	0.000	0.000	50.000	50.0	BUFG	709.723	
<input checked="" type="checkbox"/>	clk_out2	148.5	148.43750	0.000	0.000	50.000	50.0	BUFG	709.723	
<input type="checkbox"/>	clk_out3	100.000	N/A	0.000	N/A	50.000	N/A	BUFG	709.723	
<input type="checkbox"/>	clk_out4	100.000	N/A	0.000	N/A	50.000	N/A	BUFG	709.723	
<input type="checkbox"/>	clk_out5	100.000	N/A	0.000	N/A	50.000	N/A	BUFG	709.723	
<input type="checkbox"/>	clk_out6	100.000	N/A	0.000	N/A	50.000	N/A	BUFG	709.723	
<input type="checkbox"/>	clk_out7	100.000	N/A	0.000	N/A	50.000	N/A	BUFG	709.723	

WARNING: The Requested frequency value for clk_out2 can not be achieved. Please change the requested frequency or proceed with the nearest obtained frequency value of 148.43750

☐ USE CLOCK SEQUENCING

Clocking Feedback

Output Clock	Sequence Number
clk_out1	1
clk_out2	1
clk_out3	1
clk_out4	1
clk_out5	1
clk_out6	1
clk_out7	1

Source

☒ Automatic Control On-Chip
☐ Automatic Control Off-Chip
☐ User-Controlled On-Chip
☐ User-Controlled Off-Chip

Signaling

☒ Single-ended
☐ Differential

Enable Optional Inputs / Outputs for MMCM/PLL

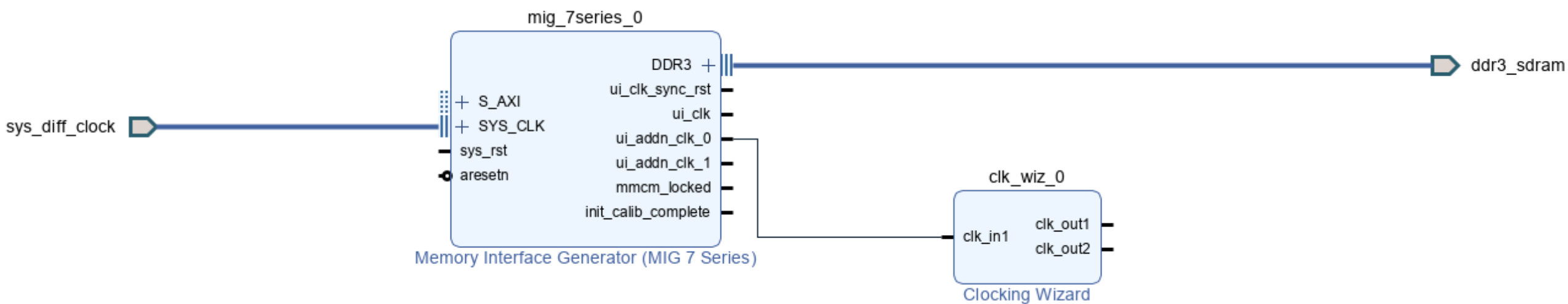
☒ reset ☐ power_down ☐ input_clk_stopped
☒ locked ☐ clkfbstopped

Reset Type

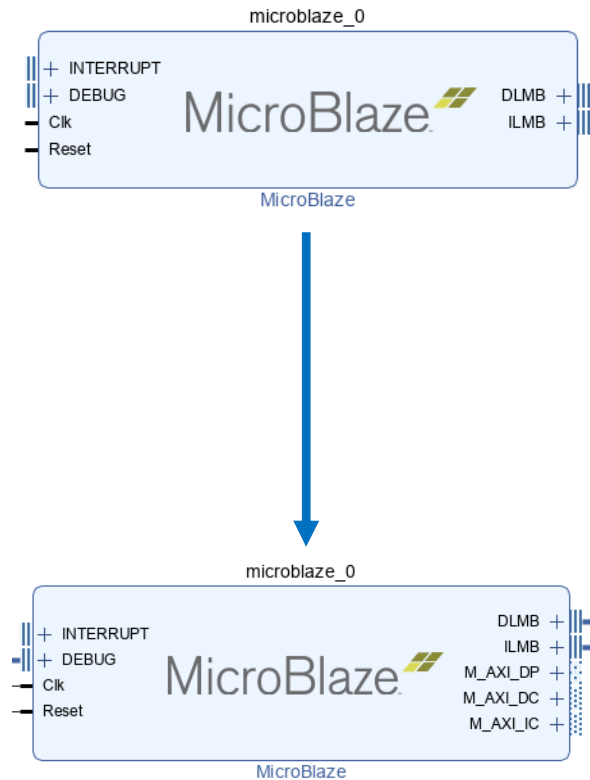
☒ Active High ☐ Active Low

OK Cancel

VC707 Test Pattern Generator Flow



VC707 Test Pattern Generator Flow – Microblaze



點選 Block Automation

Run Block Automation

Automatically make connections in your design by checking the boxes of the blocks to connect. Select a block on the left to display its configuration options on the right.

Description

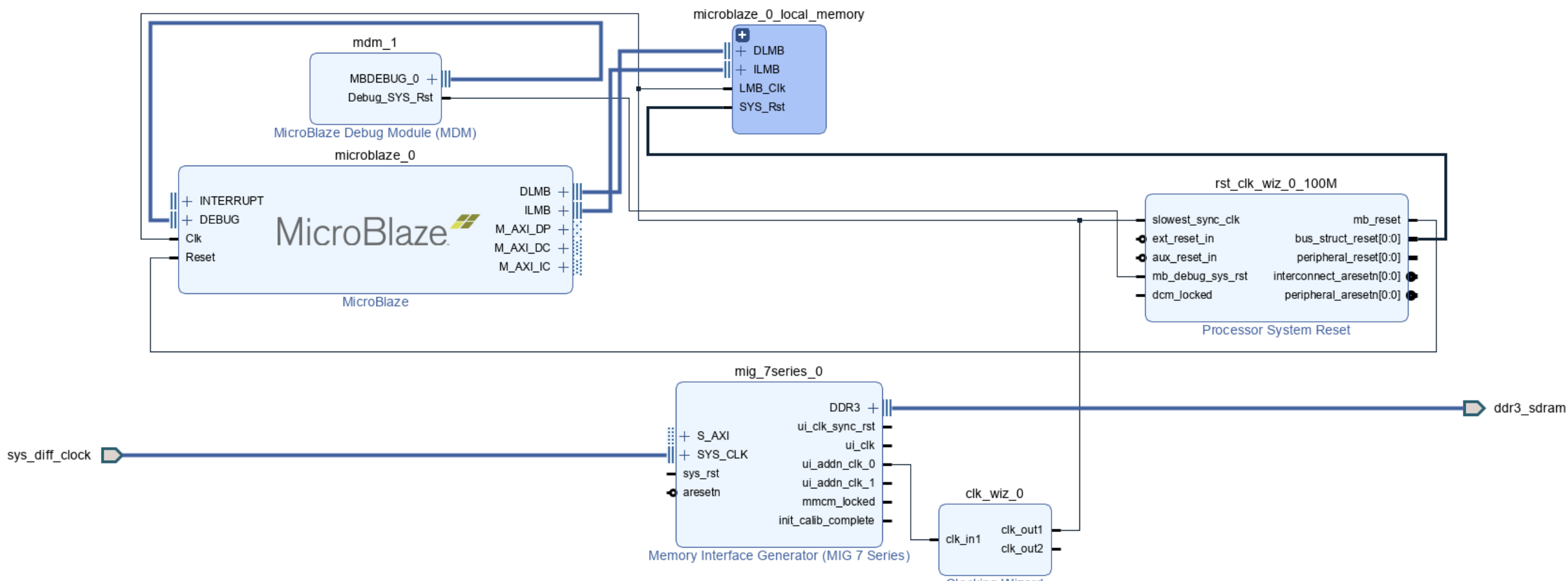
MicroBlaze connection automation generates local memory of selected size, and caches can be configured. MicroBlaze Debug Module, Peripheral AXI Interconnect, Interrupt Controller, a clock source, Processor System Reset are added and connected as needed. A preset MicroBlaze configuration can also be selected. Information about the options can be found in the tooltips.

Options

Preset	None
Local Memory	128KB
Local Memory ECC	None
Cache Configuration	64KB
Debug Module	Debug Only
Peripheral AXI Port	Enabled
<input type="checkbox"/> Interrupt Controller	
Clock Connection	/clk_wiz_0/clk_out1 (100 MHz)

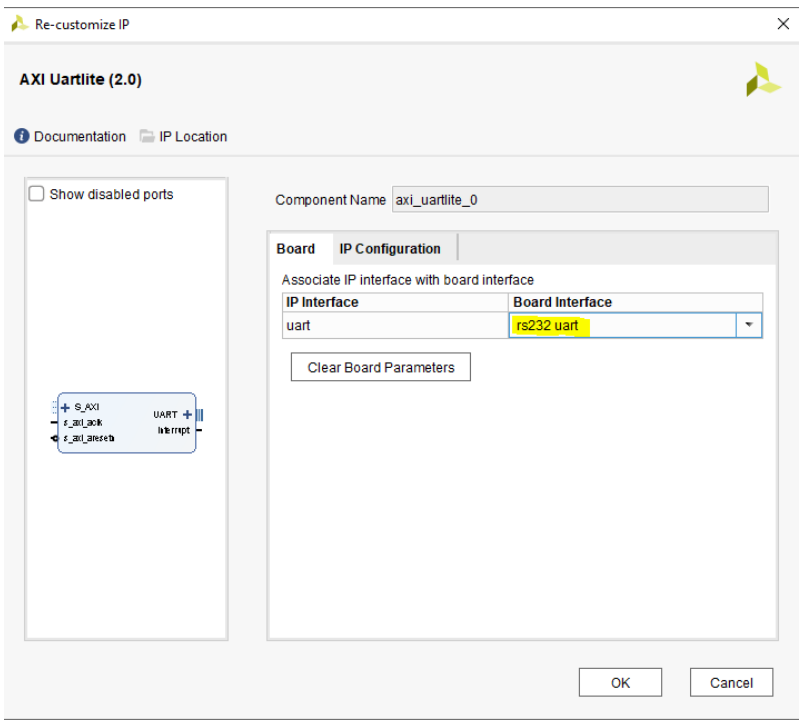
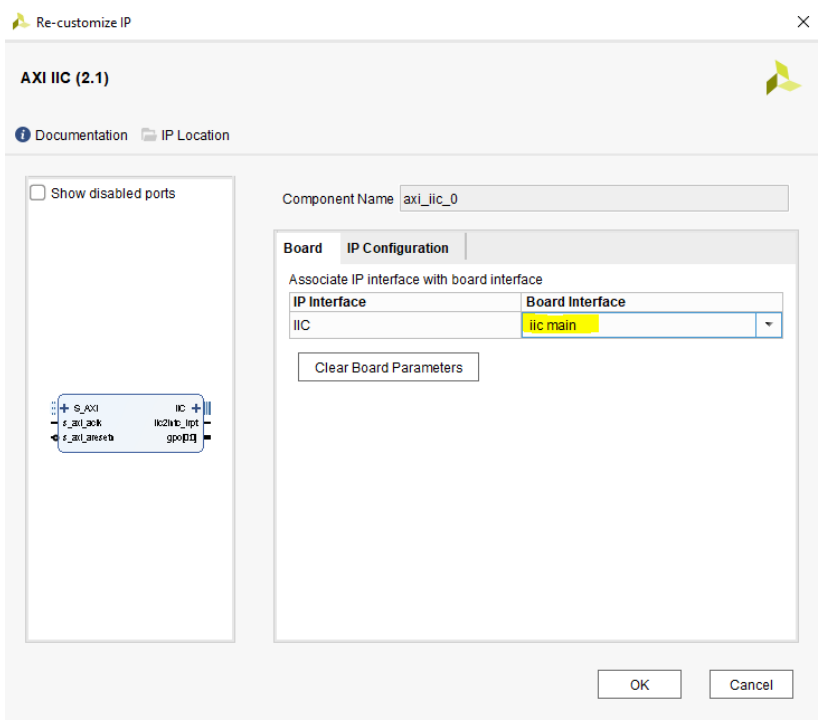
OK Cancel

VC707 Test Pattern Generator Flow



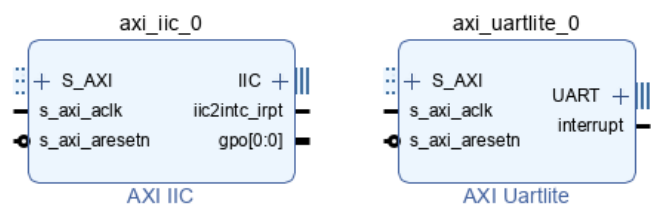
VC707 Test Pattern Generator Flow – UART & IIC

雙擊 IP 進行設定



沒變

VC707 Test Pattern Generator Flow – UART & IIC



沒變

Designer Assistance available. [Run Connection Automation](#)

Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

Q

≡

⚙

▼ All Automation (4 out of 7 selected)

☒ axi_iic_0

☒ IIC

☒ S_AXI

☒ axi_uartlite_0

☒ S_AXI

☒ UART

☐ mig_7series_0

☐ S_AXI

☐ sys_rst

☐ rst_clk_wiz_0_100M

☐ ext_reset_in

Description

Connect Slave interface (/axi_iic_0/S_AXI) to a selected Master address space.

Options

Master interface

/microblaze_0 (Periph)

Bridge IP

New AXI Interconnect

Clock source for driving Bridge IP

/clk_wiz_0/clk_out2 (148 MHz)

Clock source for Slave interface

/clk_wiz_0/clk_out2 (148 MHz)

Clock source for Master interface

/clk_wiz_0/clk_out1 (100 MHz)

Run Connection Automation

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

Q

≡

⚙

▼ All Automation (4 out of 7 selected)

☒ axi_iic_0

☒ IIC

☒ S_AXI

☒ axi_uartlite_0

☒ S_AXI

☒ UART

☐ mig_7series_0

☐ S_AXI

☐ sys_rst

☐ rst_clk_wiz_0_100M

☐ ext_reset_in

Description

Connect Slave interface (/axi_uartlite_0/S_AXI) to a selected Master address space.

Options

Master interface

/microblaze_0 (Periph)

Bridge IP

New AXI Interconnect

Clock source for driving Bridge IP

/clk_wiz_0/clk_out2 (148 MHz)

Clock source for Slave interface

/clk_wiz_0/clk_out2 (148 MHz)

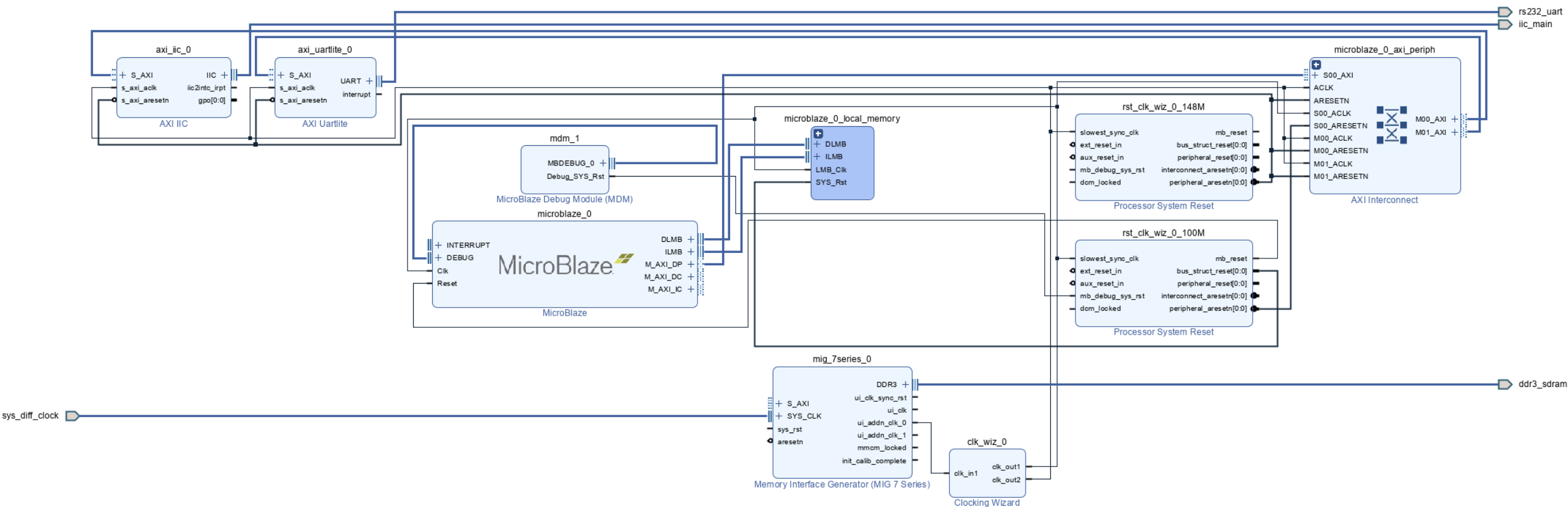
Clock source for Master interface

/clk_wiz_0/clk_out1 (100 MHz)

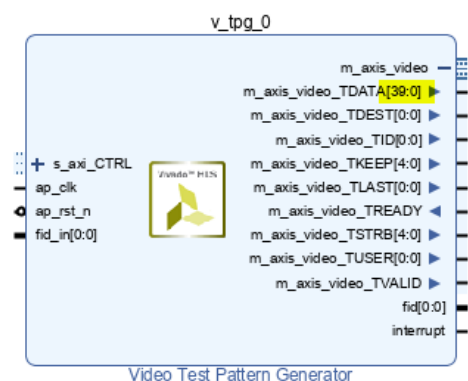
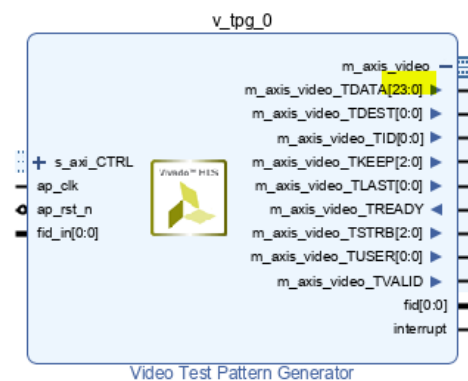
OK

Cancel

VC707 Test Pattern Generator Flow



VC707 Test Pattern Generator Flow – Test Pattern Generator



雙擊 IP 進行設定

Re-customize IP

Video Test Pattern Generator (8.1)

Documentation IP Location

☐ Show disabled ports

Component Name: v_tpg_0

Samples per Clock: 1

Maximum Data Width: 12

Maximum Number of Columns: 4096 [64 - 10328]

Maximum Number of Rows: 2160 [64 - 7760]

☐ HAS AXI4S SLAVE

☐ HAS AXI4 YUV422 YUV420

Background Patterns

☒ SOLID COLOR ☒ RAMP ☒ COLOR BAR

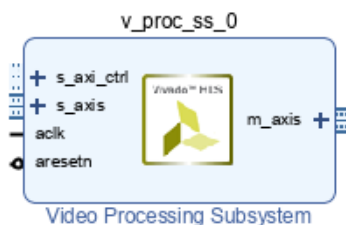
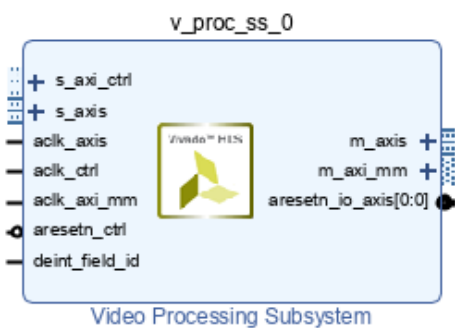
☒ DISPLAY PORT ☒ COLOR SWEEP ☒ ZONE PLATE

Foreground Patterns

☒ FOREGROUND

OK Cancel

VC707 Test Pattern Generator Flow – Video Processing Subsystem



雙擊 IP 進行設定

The 'Re-customize IP' dialog for the Video Processing Subsystem (2.3) is shown. The component name is v_proc_ss_0. The 'Top Level' tab is selected, showing the 'Color Matrix' configuration. The 'Color Space Support' section is expanded, and 'RGB | YUV 4:4:4' is selected.

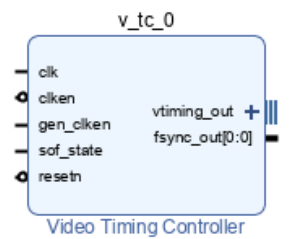
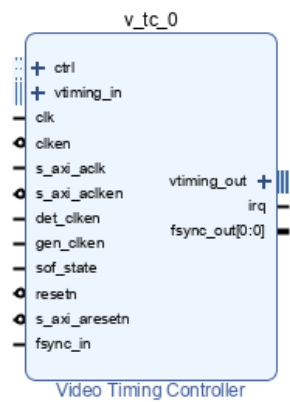
Component Name: v_proc_ss_0

Top Level Configuration Options

Color Space Support

- ☐ RGB | YUV 4:4:4 | YUV 4:2:2 | YUV 4:2:0
- ☐ RGB | YUV 4:4:4 | YUV 4:2:2
- ☒ RGB | YUV 4:4:4

VC707 Test Pattern Generator Flow – Video Timing Controller



雙擊 IP 進行設定

Re-customize IP

Video Timing Controller (6.2)

Documentation IP Location

Component Name v_tc_0

Detection/Generation Default/Constant Frame Sync Position

Optional Features

- ☒ Include AXI4-Lite Interface
- ☐ Include INTC Interface
- ☐ Interlaced Video Support
- ☐ Synchronize Generator to Detector or to fsync_in

Max Clocks Per Line 4096 Max Lines Per Frame 4096

Frame Syncs 1

☒ Enable Generation ☒ Enable Detection

Generation Options

- ☐ Field ID Generation
- ☒ Vertical Blank Generation
- ☒ Horizontal Blank Generation
- ☒ Vertical Sync Generation
- ☒ Horizontal Sync Generation
- ☒ Active Video Generation
- ☐ Active Chroma Generation
- ☐ Auto Generation Mode

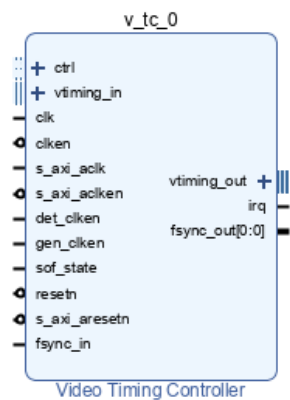
Detection Options

- ☐ Field ID Detection
- ☒ Vertical Blank Detection
- ☒ Horizontal Blank Detection
- ☒ Vertical Sync Detection
- ☒ Horizontal Sync Detection
- ☒ Active Video Detection
- ☐ Active Chroma Detection

clk clken gen_clken sof_state resetn vtiming_out fsync_out[0:0]

OK Cancel

VC707 Test Pattern Generator Flow – Video Timing Controller



雙擊 IP 進行設定

Re-customize IP

Video Timing Controller (6.2)

Documentation IP Location

☐ Show disabled ports

Component Name: v_tc_0

Detection/Generation | **Default/Constant** | **Frame Sync Position**

Video Format

Video Mode: 1080p

Horizontal Settings

Active Size	1920	[0 - 4095]
Frame Size	2200	[0 - 4095]
Sync Start	2008	[0 - 4095]
Sync End	2052	[0 - 4095]

Frame/Field 0 Vertical Settings

Active Size	1080	[0 - 4095]
Frame Size	1125	[0 - 4095]
Sync Start	1083	[0 - 4095]
Sync End	1088	[0 - 4095]

Field 1 Vertical Settings

☐ Interlaced

Frame Size	1125	[0 - 4095]
Sync Start	1083	[0 - 4095]
Sync End	1088	[0 - 4095]

Active Polarity

Field ID	High
Vblank	High
Hblank	High
Vsync	High
Hsync	High
Active Video	High
Active Chroma	High

Frame/Field 0 Horizontal Fine Adjustment

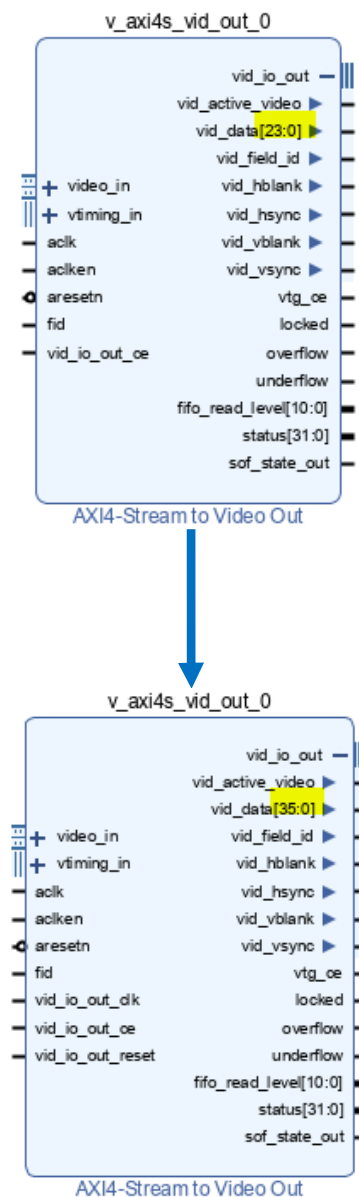
Vblank Start	960	[0 - 4095]
Vblank End	960	[0 - 4095]
VSyc Start	1004	[0 - 4095]
VSyc End	1004	[0 - 4095]

Field 1 Horizontal Fine Adjustment

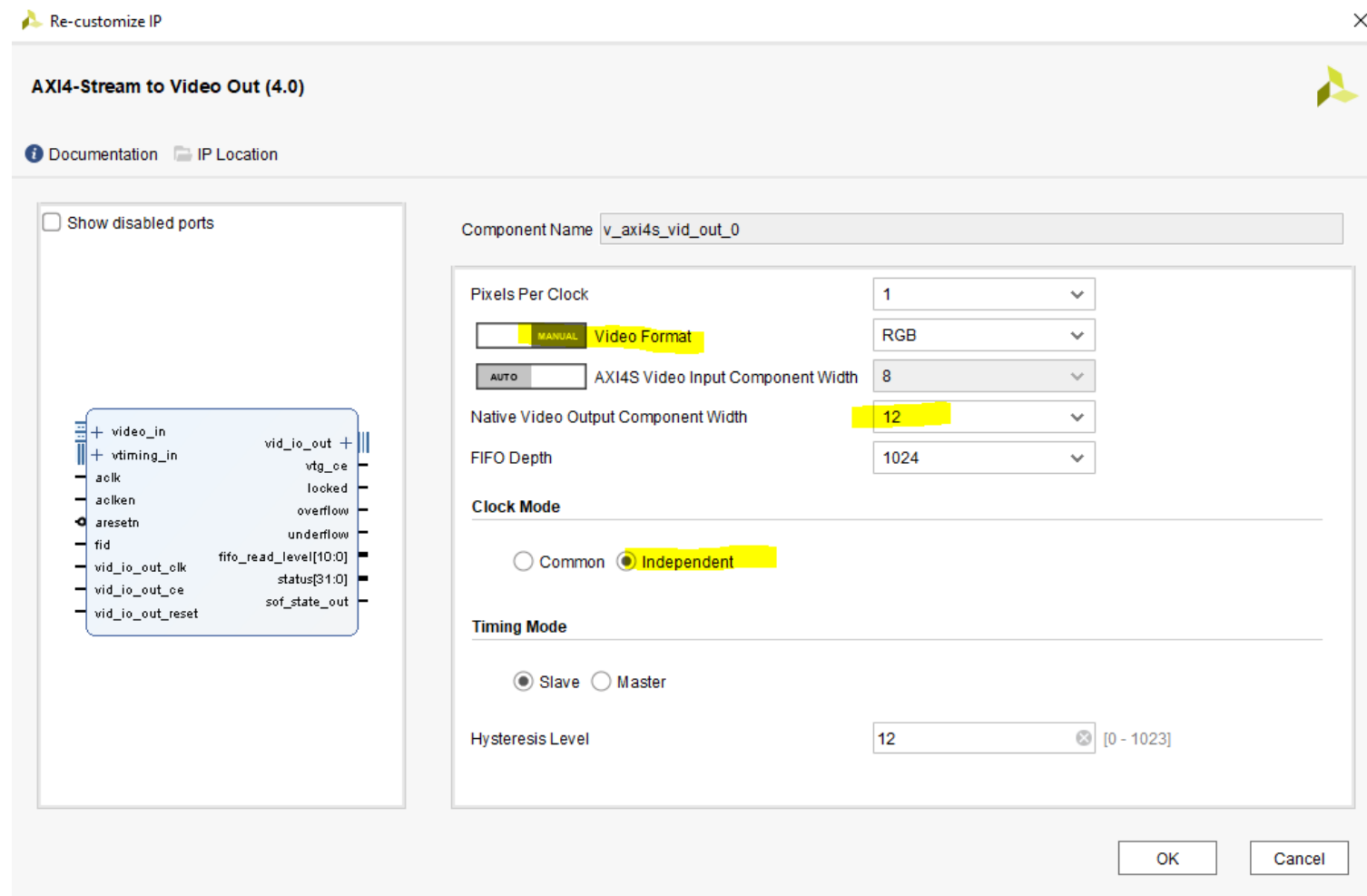
Vblank Start	960	[0 - 4095]
Vblank End	960	[0 - 4095]
VSyc Start	1004	[0 - 4095]
VSyc End	1004	[0 - 4095]

OK Cancel

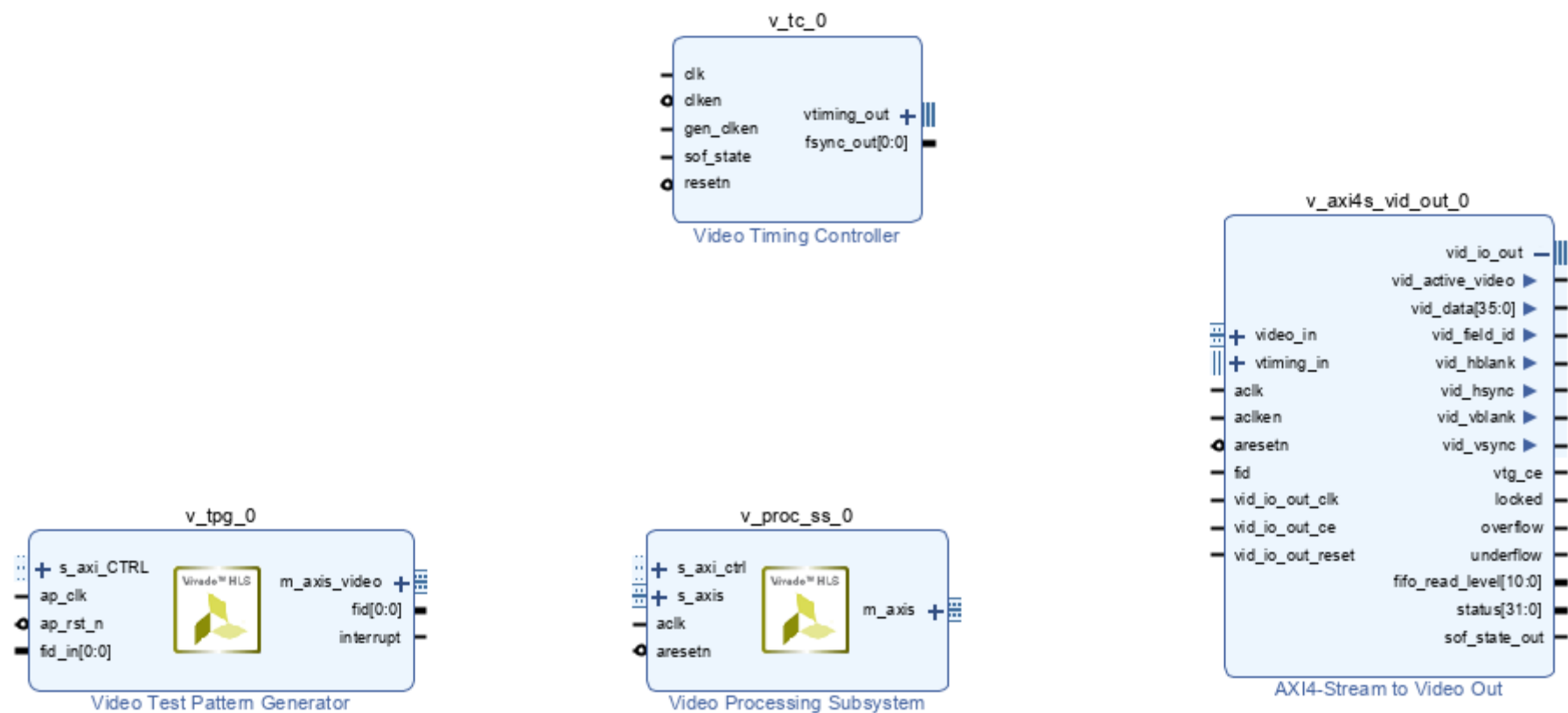
VC707 Test Pattern Generator Flow – AXI4-Stream to Video Out



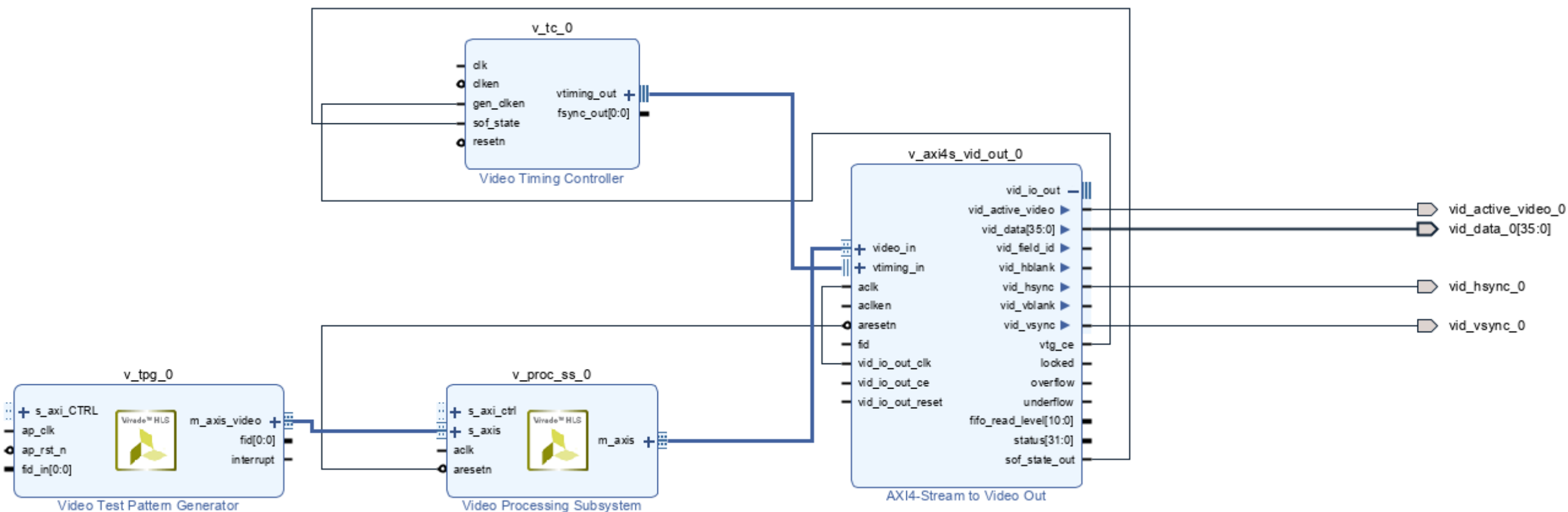
雙擊 IP 進行設定




VC707 Test Pattern Generator Flow






VC707 Test Pattern Generator Flow



VC707 Test Pattern Generator Flow

 Run Connection Automation ✕

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

▼ ☒ All Automation (2 out of 9 selected)

▼ ☐ microblaze_0

- ☐ M_AXI_DC
- ☐ M_AXI_IC

▼ ☒ mig_7series_0

- ☒ S_AXI
- ☒ sys_rst

▼ ☐ rst_clk_wiz_0_100M

- ☐ ext_reset_in

▼ ☐ rst_clk_wiz_0_148M

- ☐ ext_reset_in

▼ ☐ v_axi4s_vid_out_0

- ☐ aclk

▼ ☐ v_tc_0

- ☐ clk

▼ ☐ v_tpg_0

- ☐ s_axi_CTRL

Description

Connect Slave interface (/mig_7series_0/S_AXI) to a selected Master address space.

Options

Master interface

/microblaze_0 (Cached) ▼

Bridge IP

New AXI SmartConnect ▼

Clock source for driving Bridge IP


/mig_7series_0/ui_clk (200 MHz) ▼

Clock source for Slave interface

/mig_7series_0/ui_clk (200 MHz) ▼

Clock source for Master interface

/clk_wiz_0/clk_out1 (100 MHz) ▼

 OK Cancel

VC707 Test Pattern Generator Flow

Run Connection Automation

×

Automatically make connections in your design by checking the boxes of the interfaces to connect. Select an interface on the left to display its configuration options on the right.

?

⌕

⌵

⌶

▼ ☒ All Automation (2 out of 9 selected)

▼ ☐ microblaze_0

☐ M_AXI_DC

☐ M_AXI_IC

▼ ☒ mig_7series_0

☒ S_AXI

☒ sys_rst

▼ ☐ rst_clk_wiz_0_100M

☐ ext_reset_in

▼ ☐ rst_clk_wiz_0_148M

☐ ext_reset_in

▼ ☐ v_axi4s_vid_out_0

☐ aclk

▼ ☐ v_tc_0

☐ clk

▼ ☐ v_tpg_0

☐ s_axi_CTRL

Description

Connect Board Part Interface to IP interface.

Interface: /mig_7series_0/sys_rst

Options

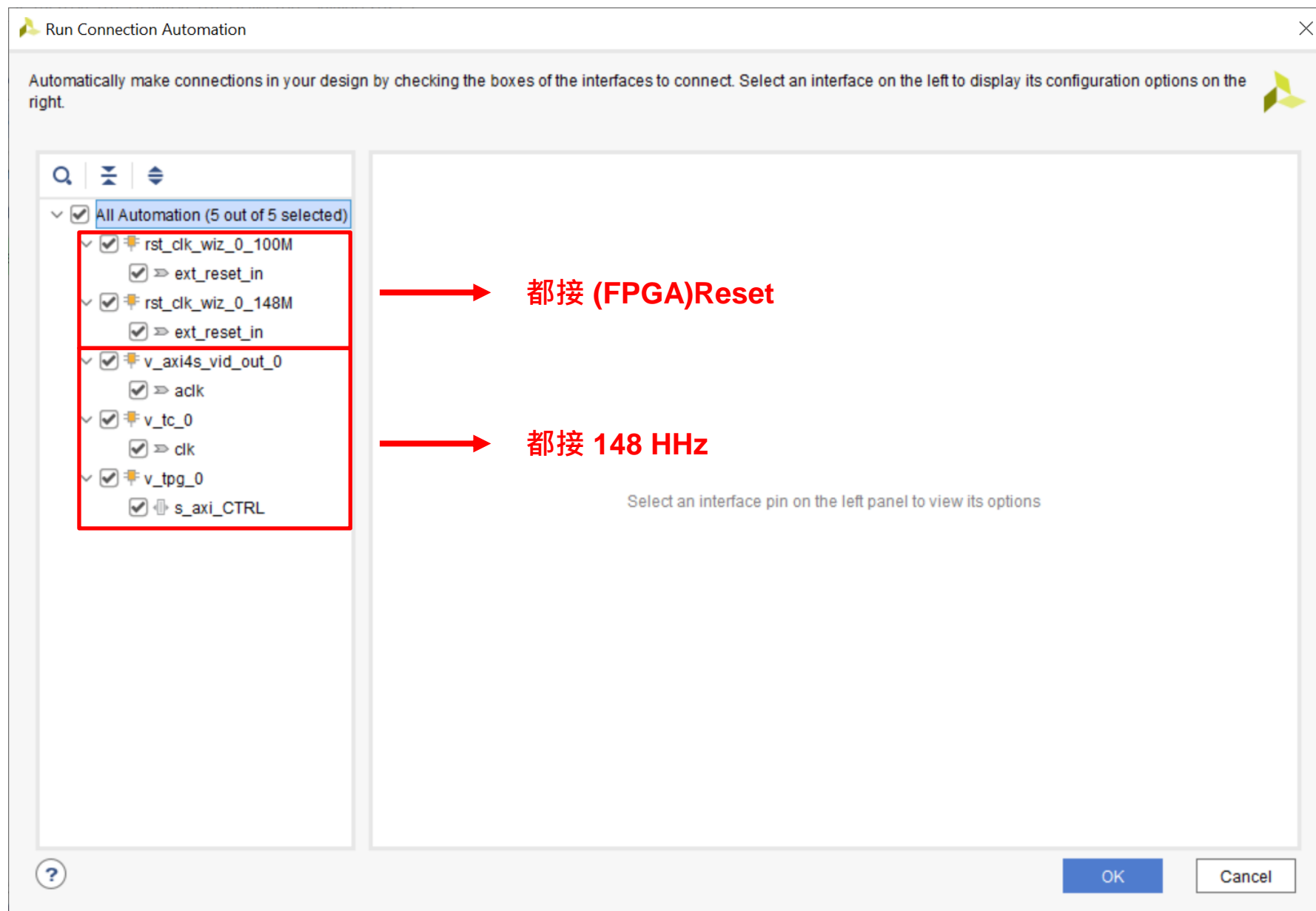
Select Board Part Interface reset (FPGA Reset) ▼

?

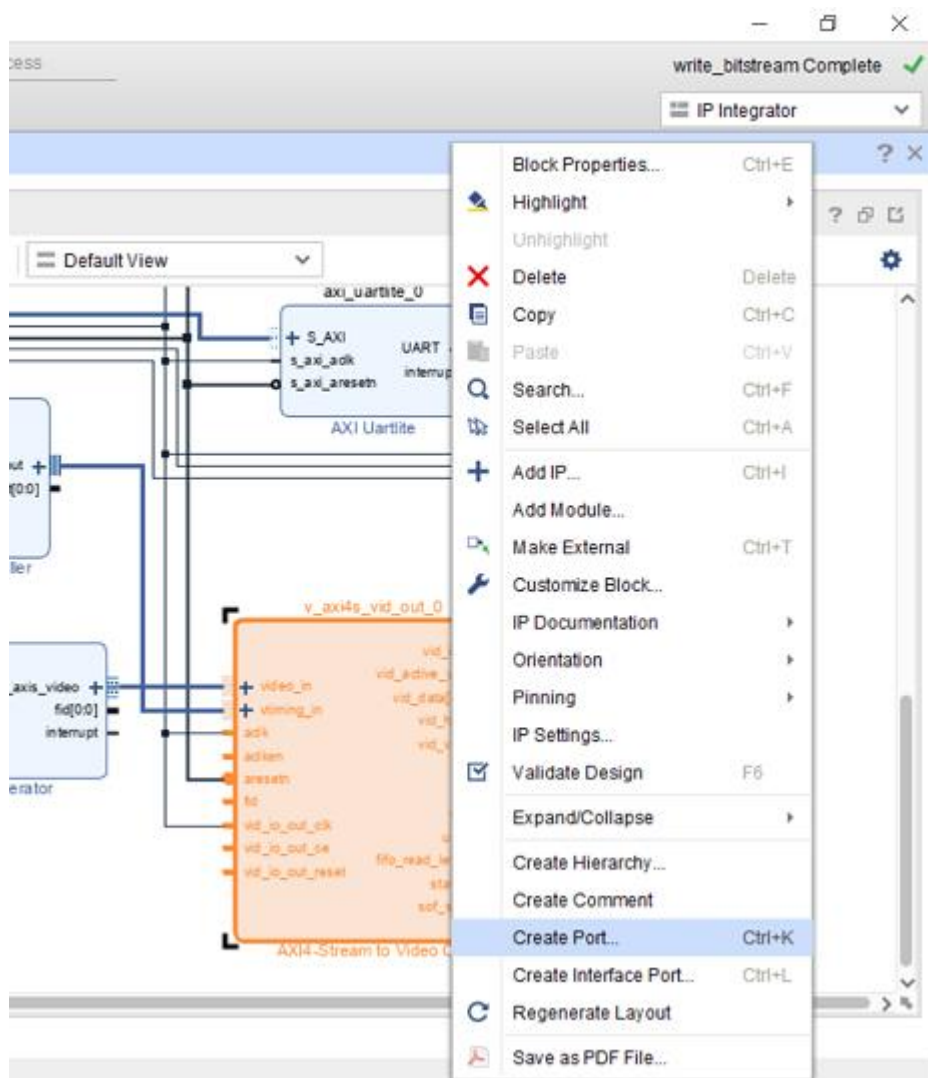
OK

Cancel

VC707 Test Pattern Generator Flow



VC707 Test Pattern Generator Flow



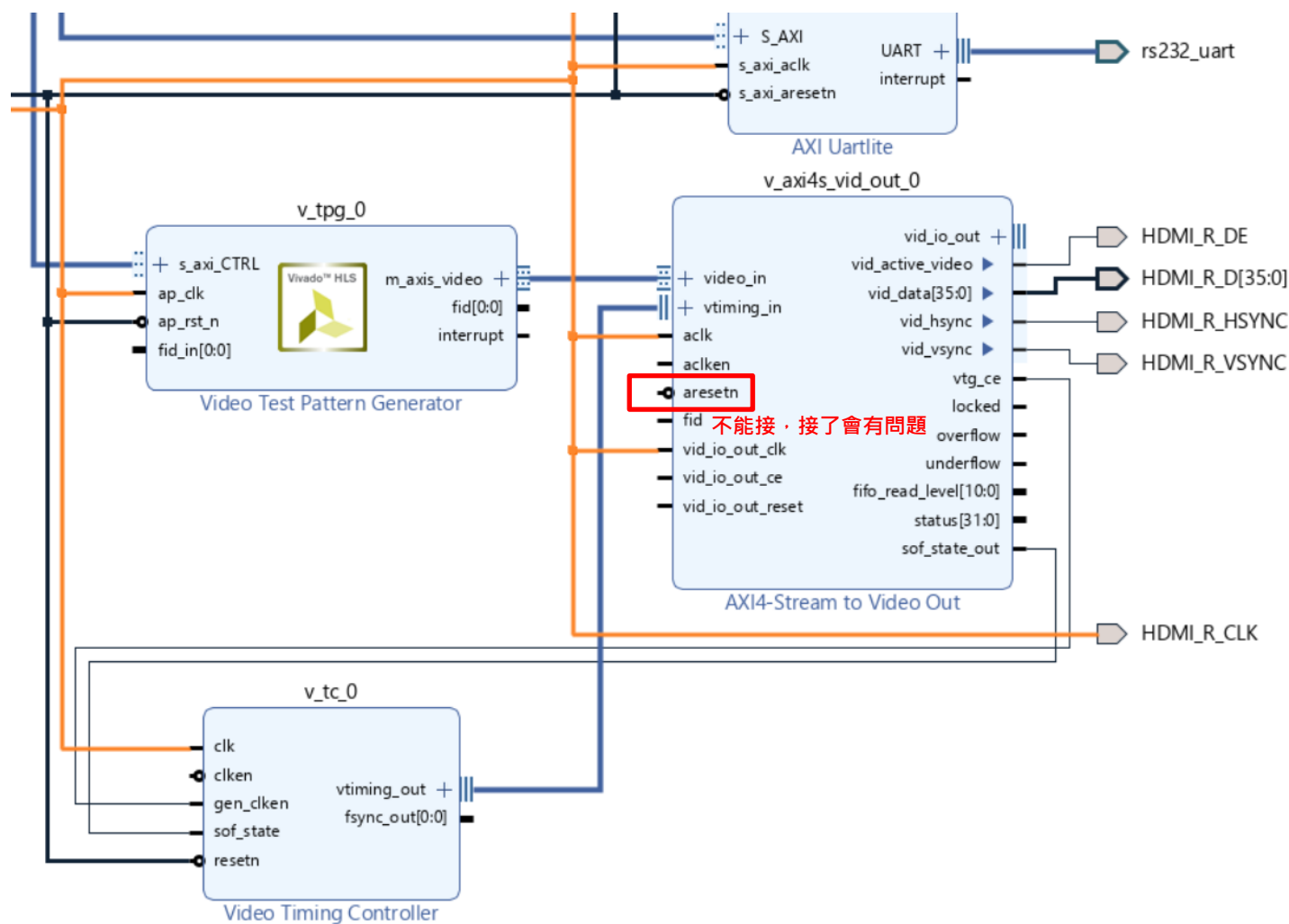
在 AXI4-Stream to Video Out 右鍵點選 **Create Port** 並輸入下圖資訊：

The 'Create Port' dialog box is shown, titled 'Create port and connect it to selected pins and ports'. It contains the following fields and options:

- Port name:** A text field containing 'hdmi_clk'.
- Direction:** A dropdown menu set to 'Output'.
- Type:** A dropdown menu set to 'Clock'.
- Create vector:** An unchecked checkbox. If checked, it would specify a range from 31 to 0.
- Frequency (MHz):** An empty text field.
- Interrupt type:** Two radio buttons, 'Level' (selected) and 'Edge'.
- Sensitivity:** Two radio buttons, 'Active High' (selected) and 'Active Low'.
- Connect to matching selected ports:** An unchecked checkbox.
- Buttons:** 'OK' and 'Cancel' buttons at the bottom right.

VC707 Test Pattern Generator Flow

連接 HDMI Clk 到 VTC clk

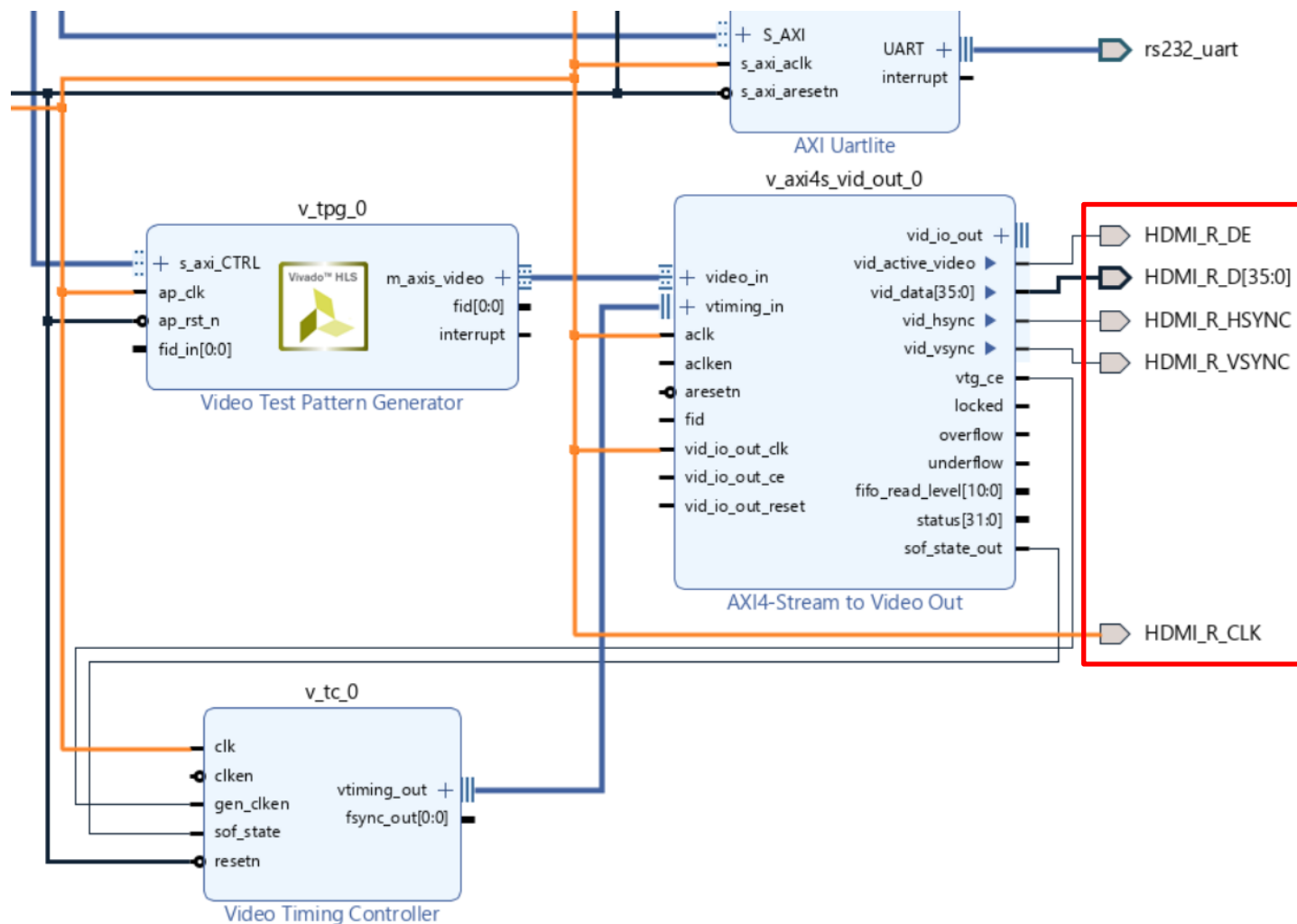


VC707 Test Pattern Generator Flow

撰寫 HDMI XDC，可以在以下網址找到寫好的作參考

[VC707 XDC Constraints File: Sorted · GitHub](#)

記得改成相對應的名字



VC707 Test Pattern Generator Flow

撰寫 HDMI XDC，可以在以下網址找到寫好的作參考

[VC707 XDC Constraints File: Sorted - GitHub](#)

記得改成相對應的名字，自己複製對照

```
set_property PACKAGE_PIN AM22 [get_ports HDMI_R_D[0]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[0]]
set_property PACKAGE_PIN AL22 [get_ports HDMI_R_D[1]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[1]]
set_property PACKAGE_PIN AJ20 [get_ports HDMI_R_D[2]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[2]]
set_property PACKAGE_PIN AJ21 [get_ports HDMI_R_D[3]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[3]]
set_property PACKAGE_PIN AM21 [get_ports HDMI_R_D[4]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[4]]
set_property PACKAGE_PIN AL21 [get_ports HDMI_R_D[5]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[5]]
set_property PACKAGE_PIN AK22 [get_ports HDMI_R_D[6]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[6]]
set_property PACKAGE_PIN AJ22 [get_ports HDMI_R_D[7]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[7]]
set_property PACKAGE_PIN AL20 [get_ports HDMI_R_D[8]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[8]]
set_property PACKAGE_PIN AK20 [get_ports HDMI_R_D[9]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[9]]
set_property PACKAGE_PIN AK23 [get_ports HDMI_R_D[10]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[10]]
set_property PACKAGE_PIN AJ23 [get_ports HDMI_R_D[11]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[11]]
set_property PACKAGE_PIN AN21 [get_ports HDMI_R_D[12]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[12]]
set_property PACKAGE_PIN AP22 [get_ports HDMI_R_D[13]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[13]]
set_property PACKAGE_PIN AP23 [get_ports HDMI_R_D[14]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[14]]
set_property PACKAGE_PIN AN23 [get_ports HDMI_R_D[15]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[15]]
set_property PACKAGE_PIN AM23 [get_ports HDMI_R_D[16]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[16]]
set_property PACKAGE_PIN AN24 [get_ports HDMI_R_D[17]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[17]]
set_property PACKAGE_PIN AY24 [get_ports HDMI_R_D[18]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[18]]
set_property PACKAGE_PIN BB22 [get_ports HDMI_R_D[19]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[19]]
set_property PACKAGE_PIN BA22 [get_ports HDMI_R_D[20]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[20]]
set_property PACKAGE_PIN BA25 [get_ports HDMI_R_D[21]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[21]]
set_property PACKAGE_PIN AY25 [get_ports HDMI_R_D[22]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[22]]
set_property PACKAGE_PIN AY22 [get_ports HDMI_R_D[23]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[23]]
```

```
set_property PACKAGE_PIN AY23 [get_ports HDMI_R_D[24]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[24]]
set_property PACKAGE_PIN AV24 [get_ports HDMI_R_D[25]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[25]]
set_property PACKAGE_PIN AU24 [get_ports HDMI_R_D[26]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[26]]
set_property PACKAGE_PIN AW21 [get_ports HDMI_R_D[27]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[27]]
set_property PACKAGE_PIN AV21 [get_ports HDMI_R_D[28]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[28]]
set_property PACKAGE_PIN AT24 [get_ports HDMI_R_D[29]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[29]]
set_property PACKAGE_PIN AR24 [get_ports HDMI_R_D[30]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[30]]
set_property PACKAGE_PIN AU21 [get_ports HDMI_R_D[31]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[31]]
set_property PACKAGE_PIN AT21 [get_ports HDMI_R_D[32]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[32]]
set_property PACKAGE_PIN AW22 [get_ports HDMI_R_D[33]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[33]]
set_property PACKAGE_PIN AW23 [get_ports HDMI_R_D[34]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[34]]
set_property PACKAGE_PIN AV23 [get_ports HDMI_R_D[35]]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_D[35]]
```

```
set_property PACKAGE_PIN AU23 [get_ports HDMI_R_CLK]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_CLK]
set_property PACKAGE_PIN AP21 [get_ports HDMI_R_DE]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_DE]
set_property PACKAGE_PIN AT22 [get_ports HDMI_R_VSYNC]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_VSYNC]
set_property PACKAGE_PIN AU22 [get_ports HDMI_R_HSYNC]
set_property IOSTANDARD LVCMOS18 [get_ports HDMI_R_HSYNC]
```

VC707 Test Pattern Generator Flow

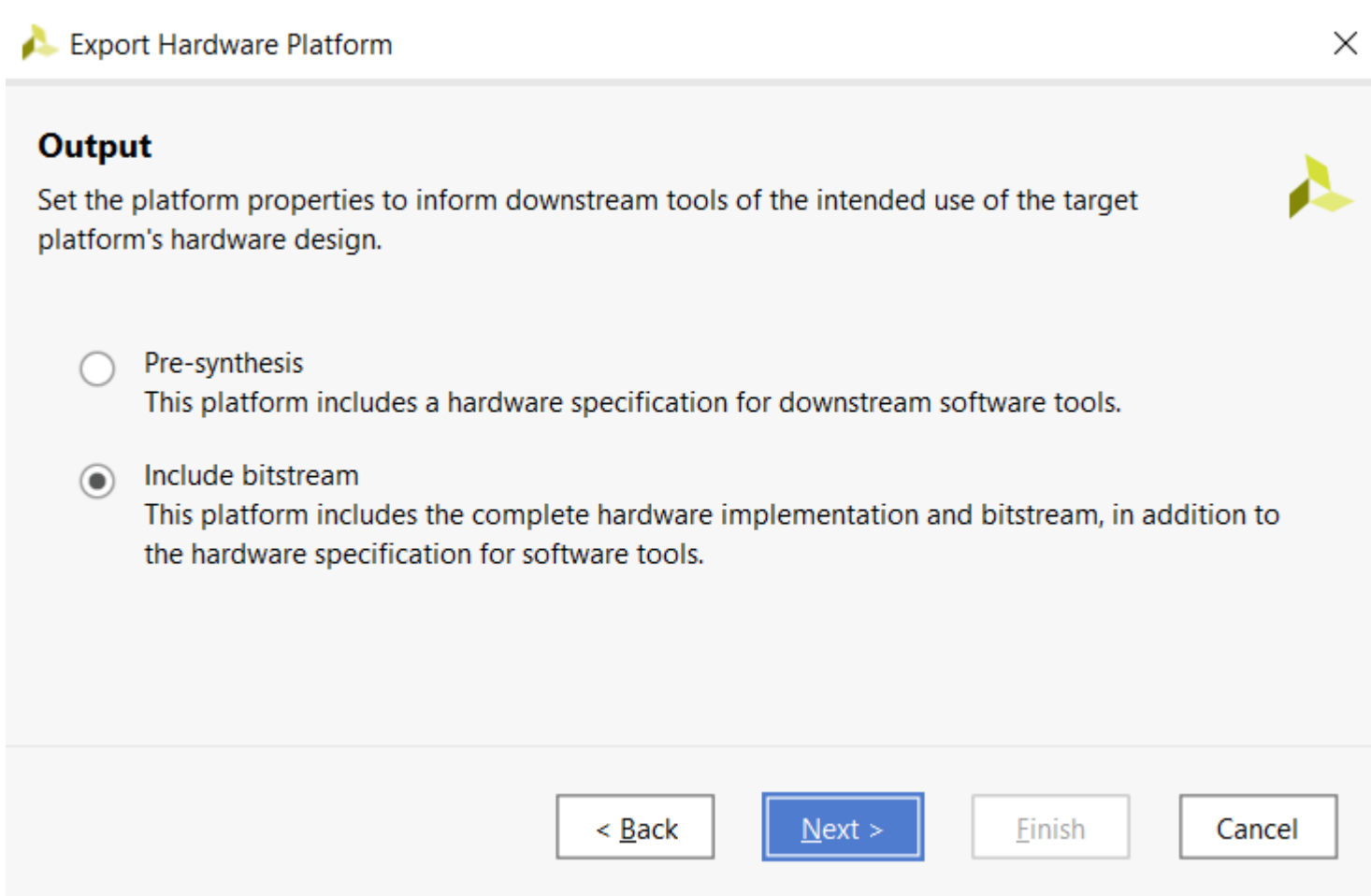
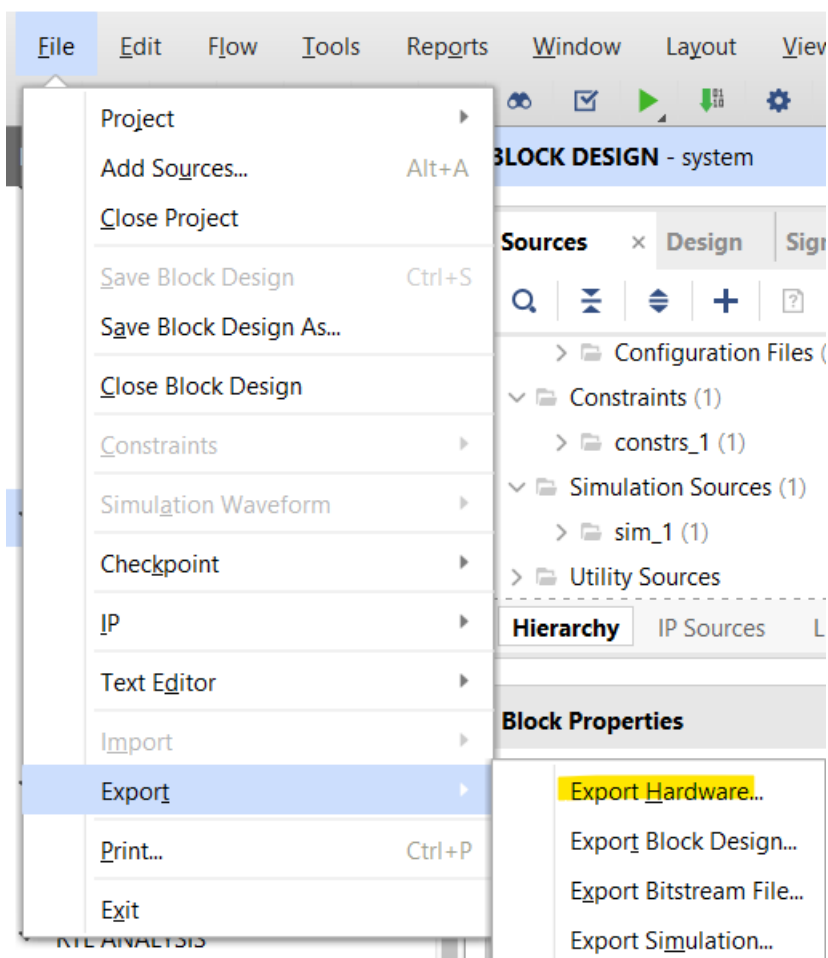
Block Design Steps

The screenshot illustrates the initial steps of the VC707 Test Pattern Generator flow. The 'Sources' window shows the project structure, including 'Design Sources (1)' with 'design_1 (design_1.bd)', 'Constraints (1)' with 'constrs_1 (1)' and 'ZC702.xdc', 'Simulation Sources (1)' with 'sim_1 (1)', and 'Utility Sources'. A context menu is open for 'design_1 (design_1.bd)', with 'Generate Output Products...' selected. The 'IMPLEMENTATION' section in the bottom toolbar shows 'Run Implementation' and 'Open Implemented Design'. The 'PROGRAM AND DEBUG' section shows 'Generate Bitstream' (highlighted) and 'Open Hardware Manager'. A 'No Implementation Results Available' dialog box is displayed, asking if the user wants to launch synthesis and implementation. The 'Yes' button is highlighted. The command prompt at the bottom shows the command: `add_files -fileset constrs_1 -norecurse C:/BIST/XVES_0019/src/constr/ZC702.xdc`.

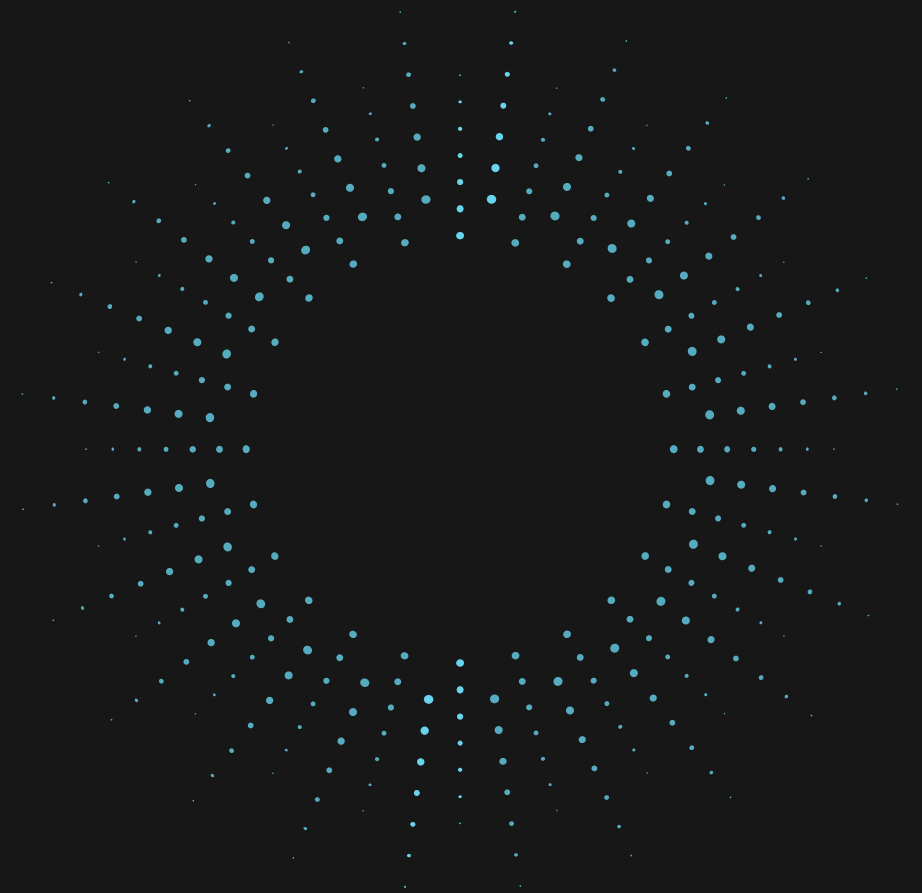


**THIRTY-SEVEN
MINUTES
LATER...**

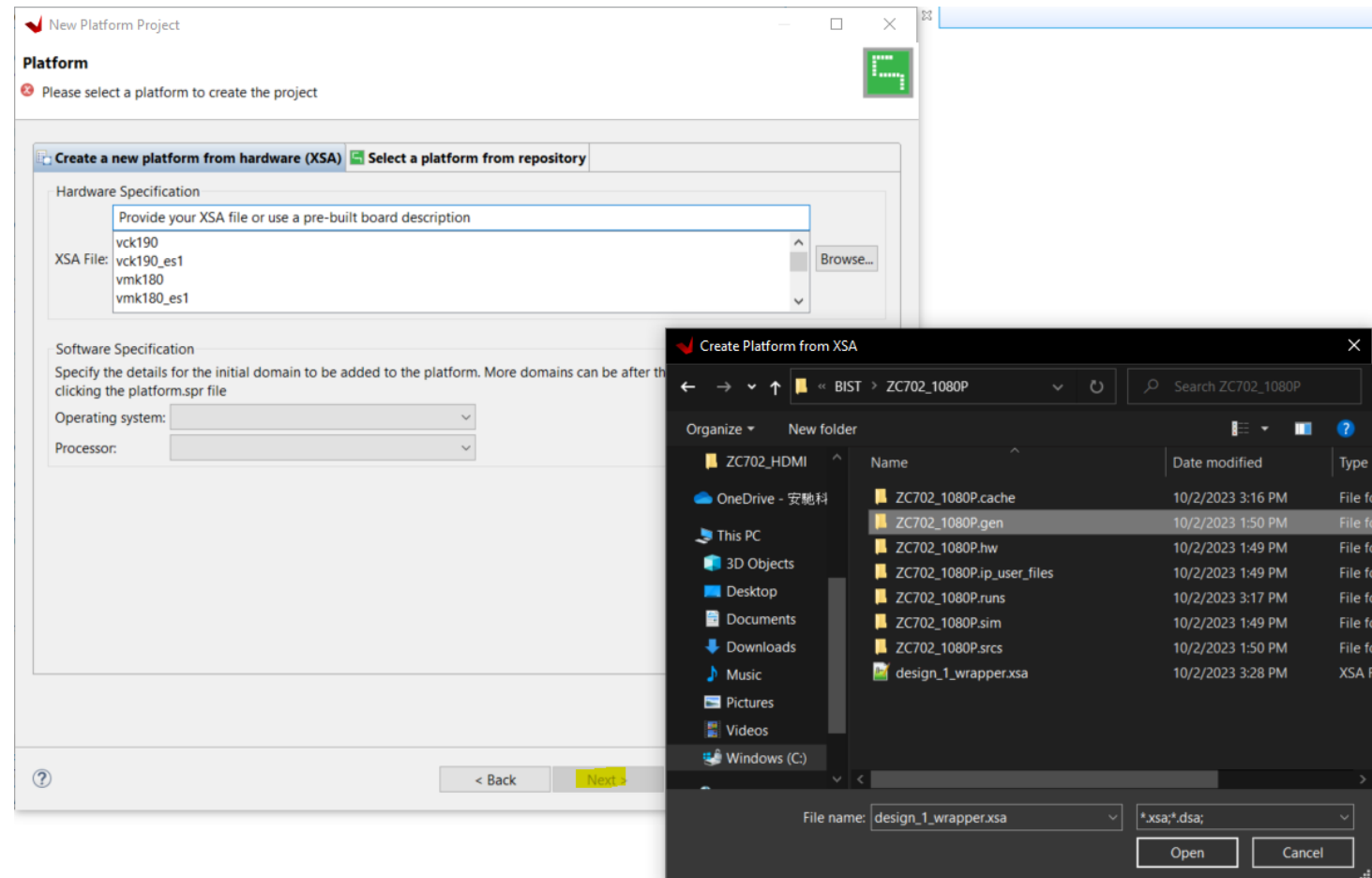
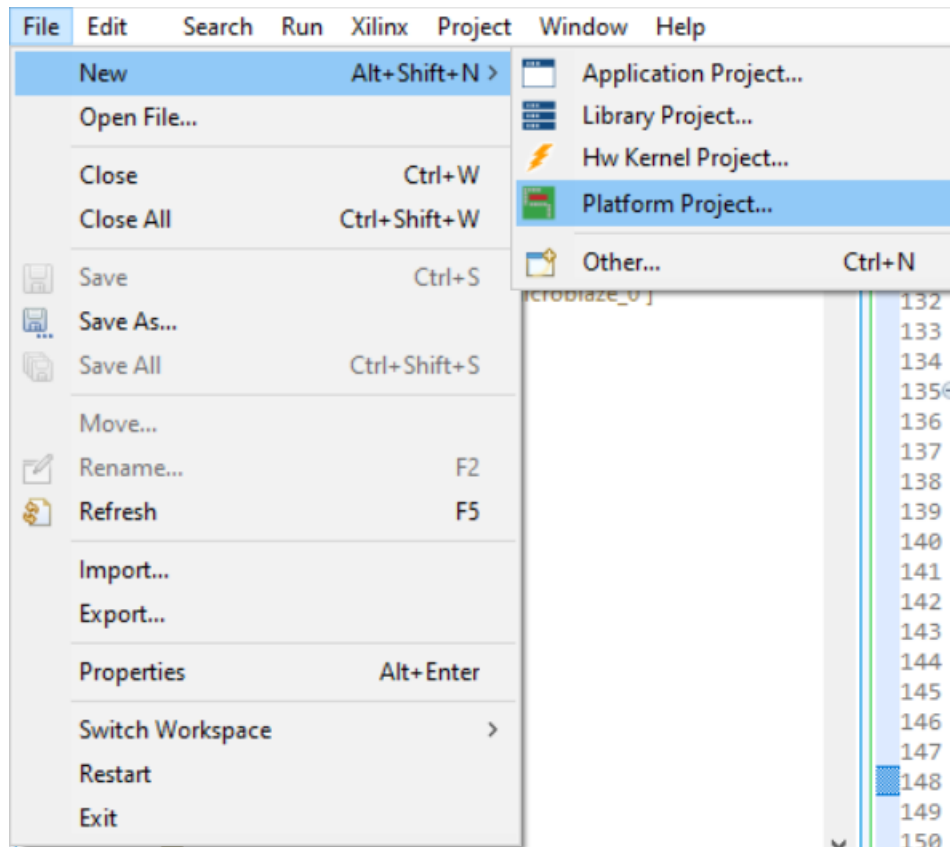
VC707 Test Pattern Generator Flow



Vitis 2021.1 Part

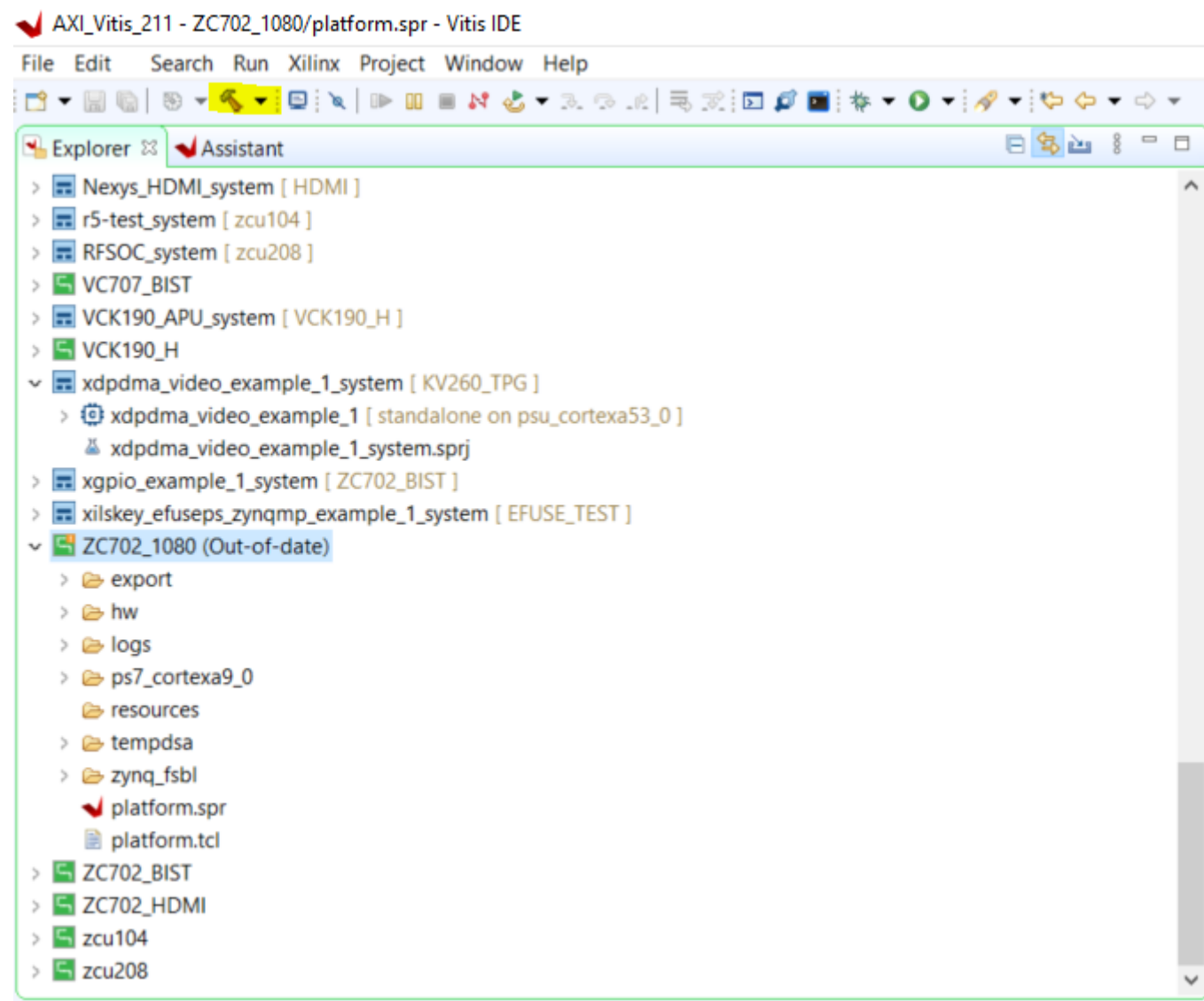


VC707 Test Pattern Generator Flow

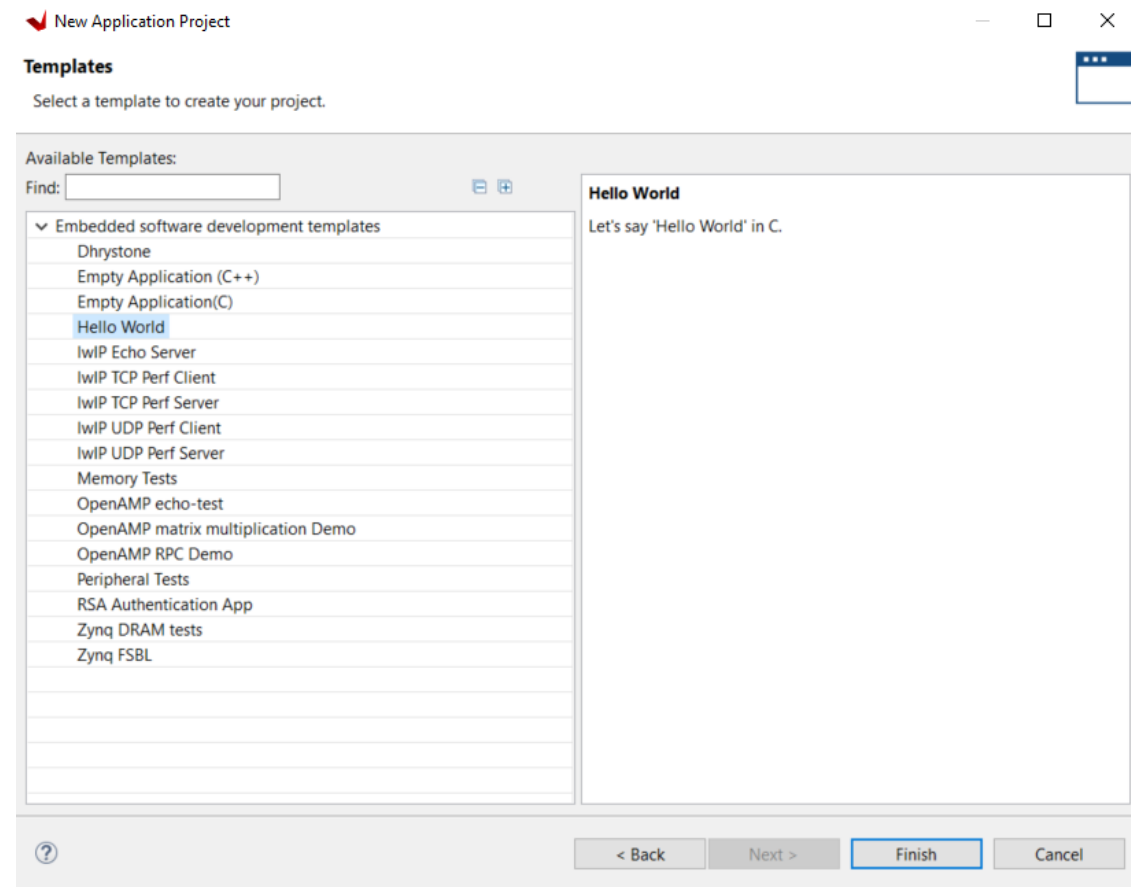
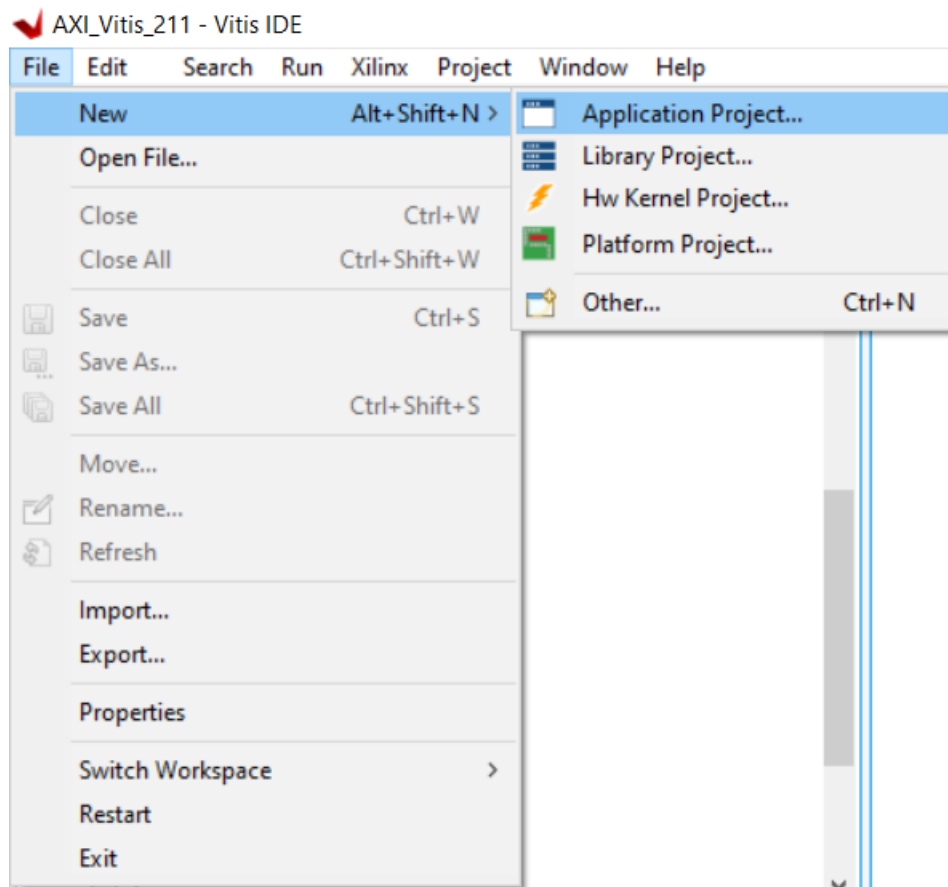


*** 實際檔案請按照自己設定的位置與名稱去開啟

VC707 Test Pattern Generator Flow

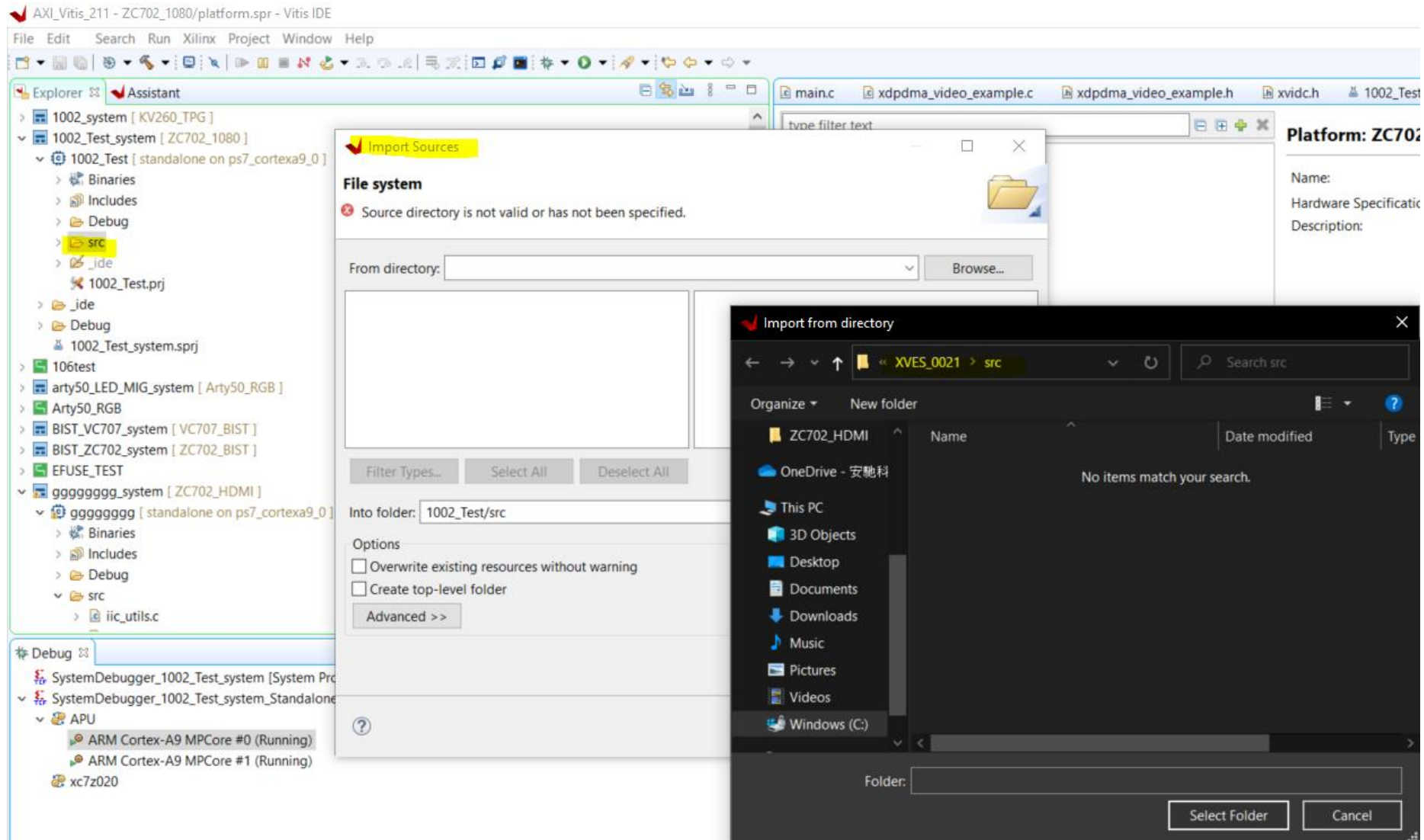


VC707 Test Pattern Generator Flow



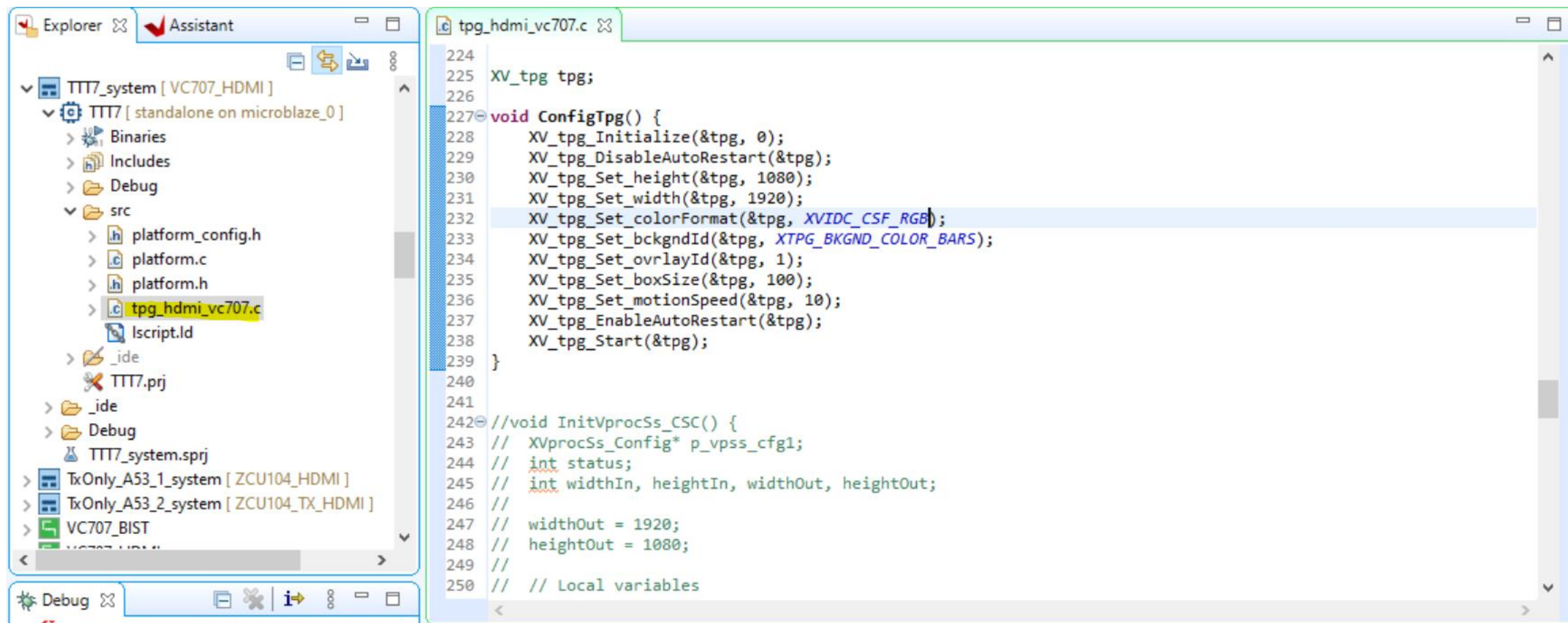
VC707 Test Pattern Generator Flow

helloworld.c 刪掉，然後新增一個文件 .c 檔，把以下 tpg_hdmi_vc707.c import 進去，日後再更新 code 內每個 function 功能

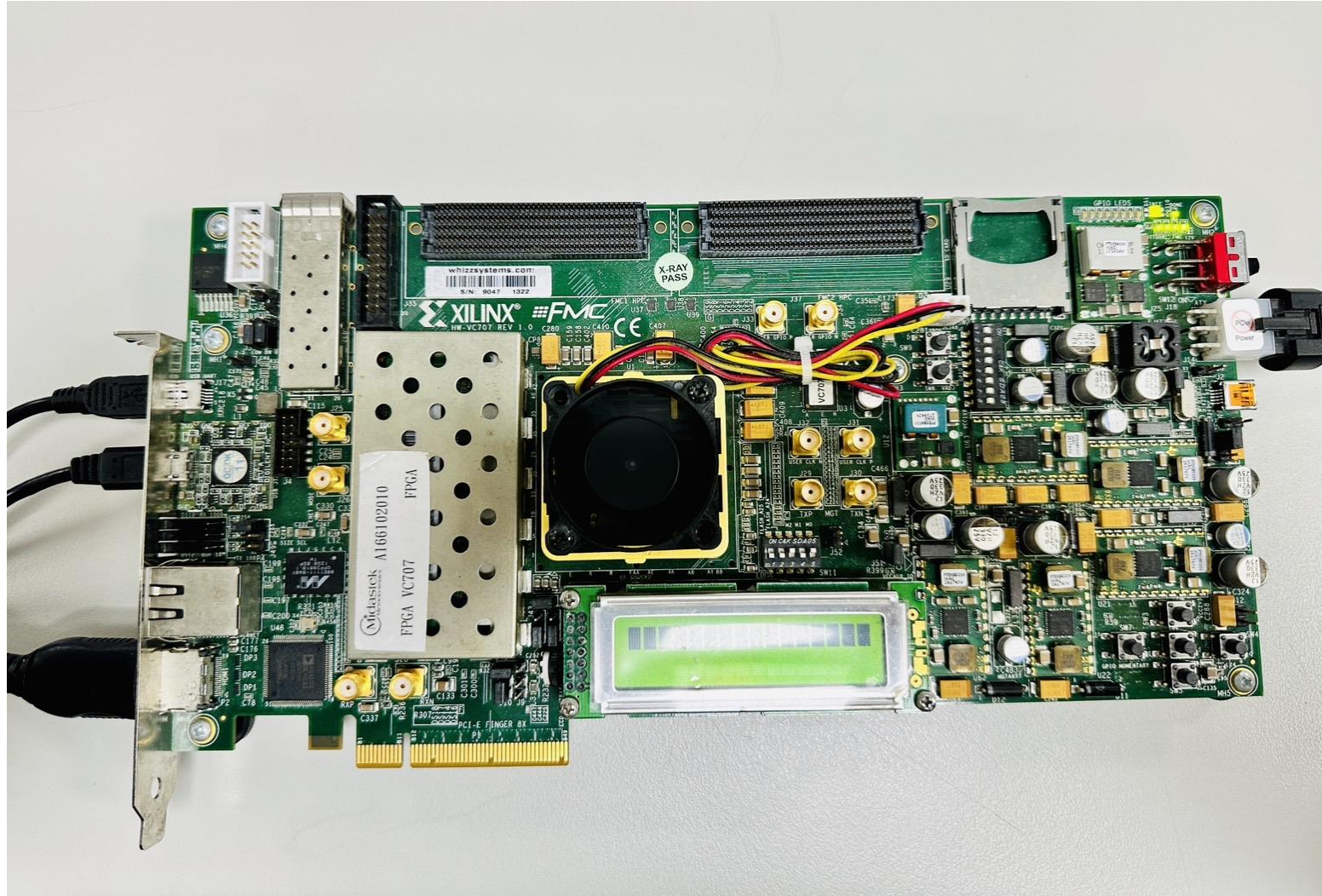


VC707 Test Pattern Generator Flow

helloworld.c 刪掉，然後新增一個文件 .c 檔，把以下 tpg_hdmi_vc707.c import 進去，日後再更新 code 內每個 function 功能



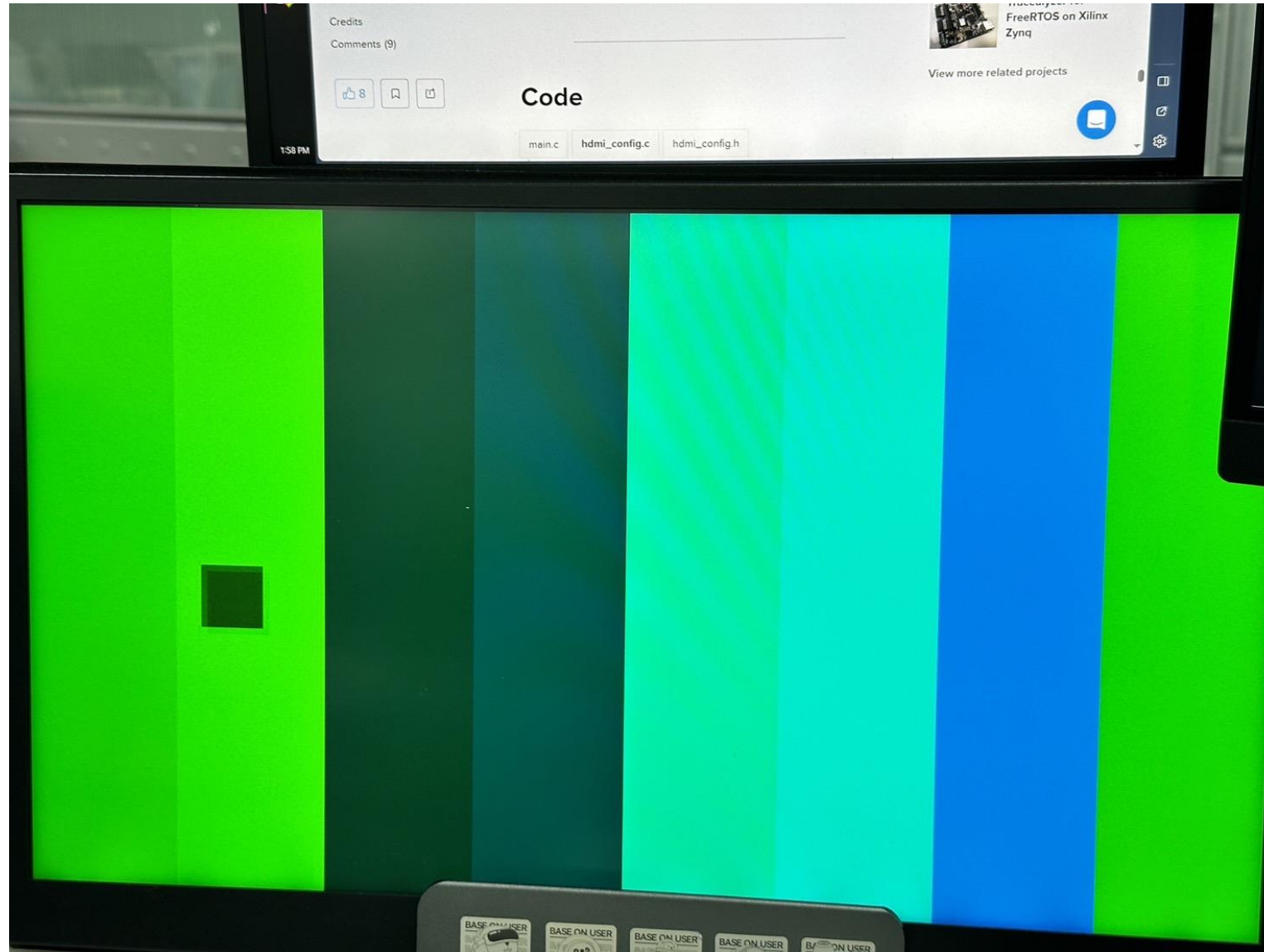
VC707 Hardware Setting



VC707 Test Pattern Generator Output Demo

```
Hello World  
Successfully ran Hello World application  
After XIic_DynInit  
ADV7511 IIC programming PASSED  
-----  
ADV7511 HDMI Output Demo  
-----  
  
TPG Configuration
```

VC707 Test Pattern Generator Output Demo



VC707 Test Pattern Generator Output Demo



VC707 Test Pattern Generator Output Demo Problem

1. **Color Space** 是錯誤的，顯示不出正確的彩條
2. 燒錄 VC707 有時候會出現 **Microblaze instruction insert overrun**，我也不知道為何
3. **AXI4-Stream to Video Out** 的 **aresetn** 不能接，感覺跟 **Vitis C Code** 設定有關係
4. 一定先讓 **MIG** 做 **Block Automation** 後產出 **sys_diff_clock**，再讓 **MicroBlaze** 做 **Block Automation**

Reference

1. [Xilinx FPGA-HDMI1.4: You Must Know First ! - Hackster.io](#)
2. <https://www.hackster.io/adam-taylor/ac701-hdmi-test-pattern-generation-9aa148>

