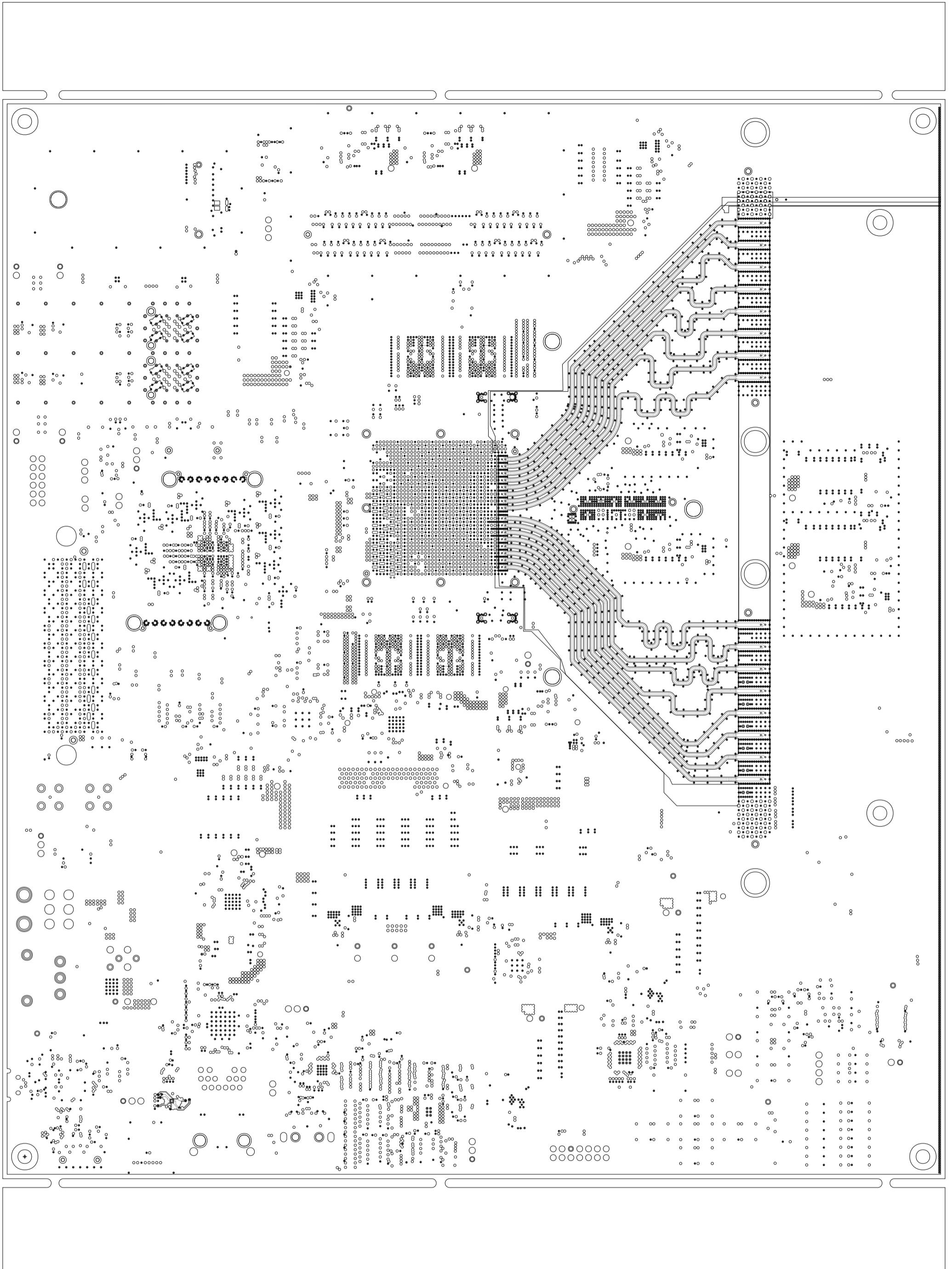
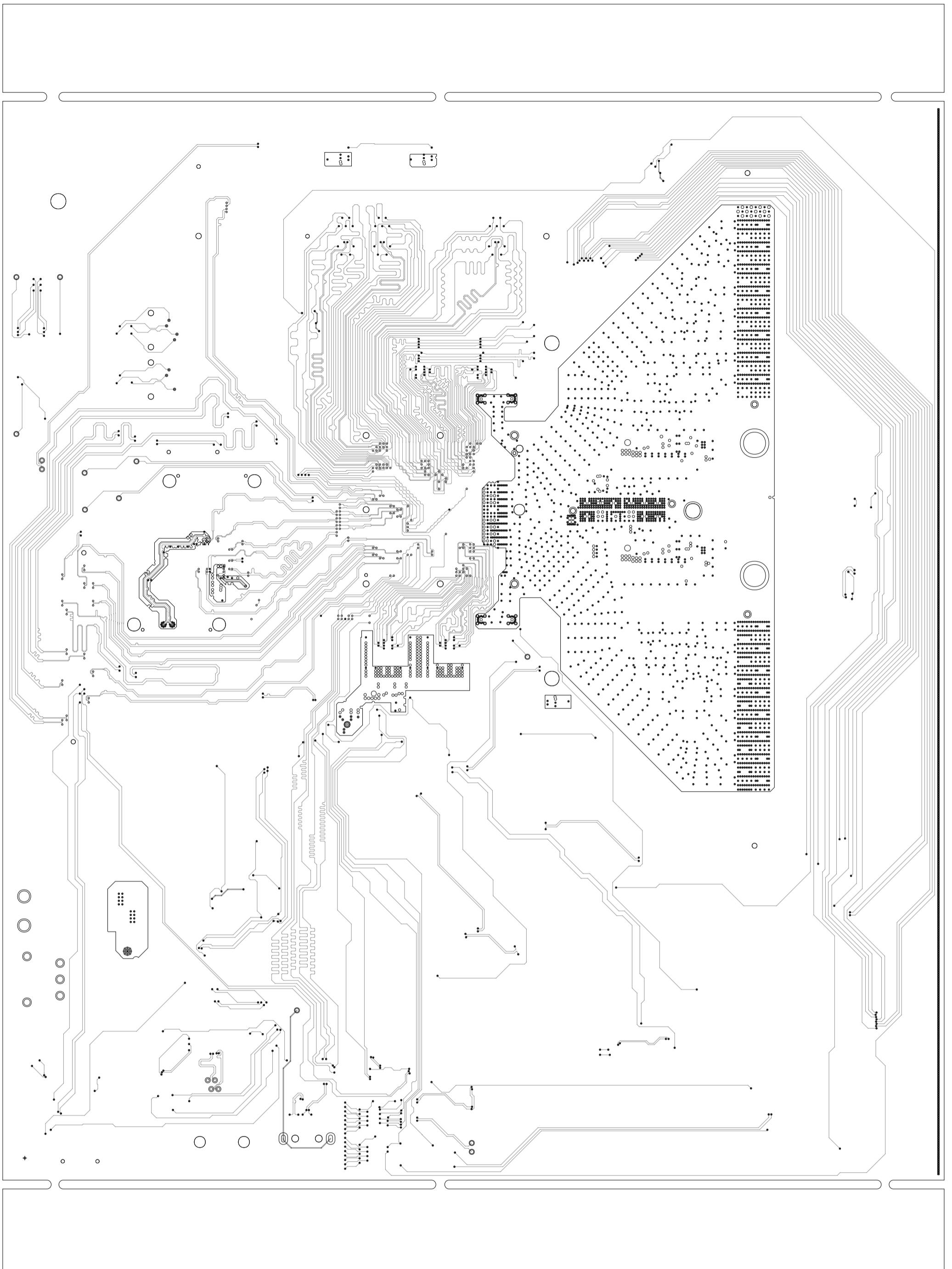


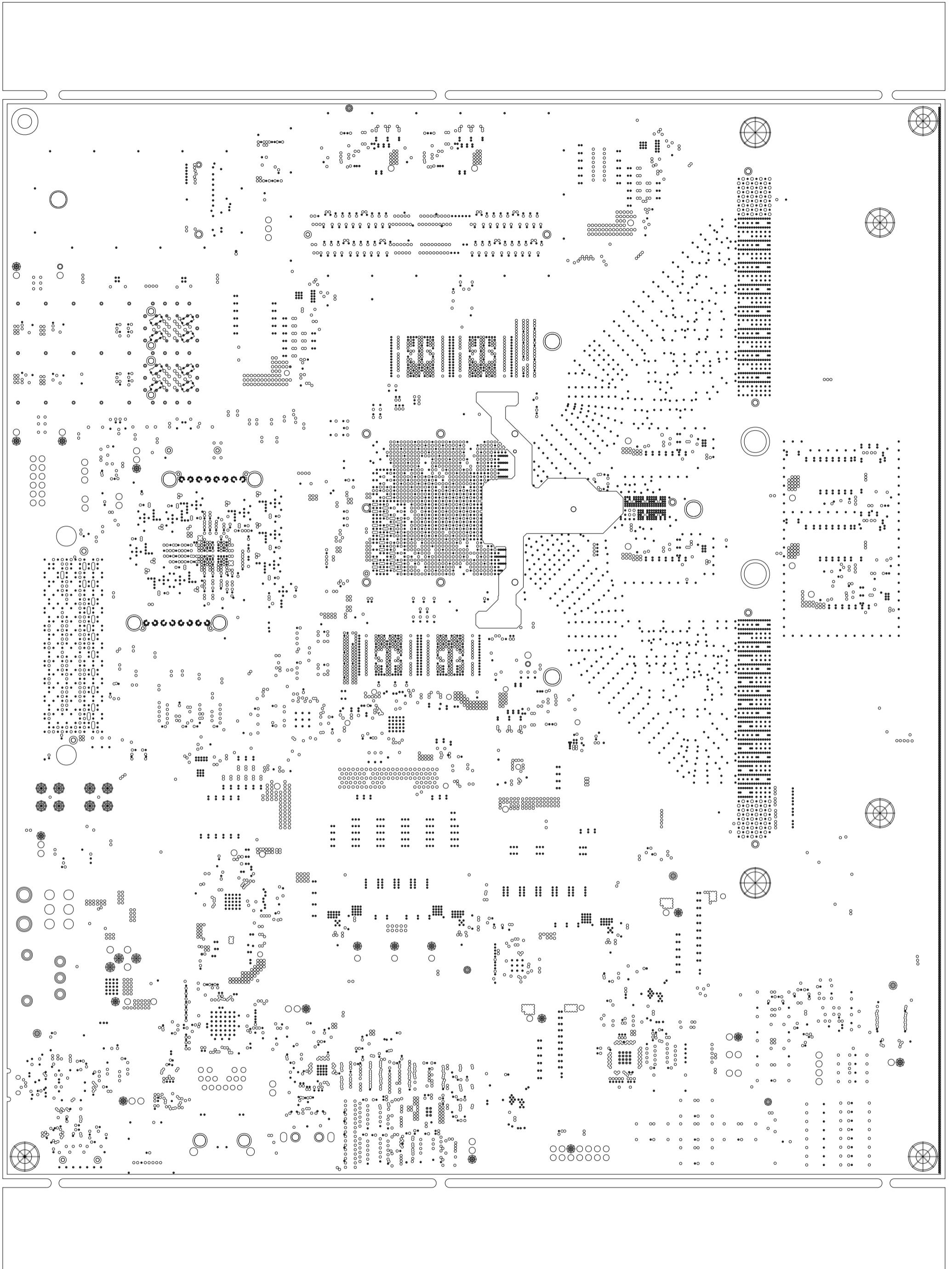
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB # 128-05023-01	LAYER: L1_TOP
Designed by Xilinx	DATE: 12/12/2019
BOARD designer: NHANO	PHONE: 408-879-4993
1	XILINX DOC USE ONLY REVISION:A01 Version b0



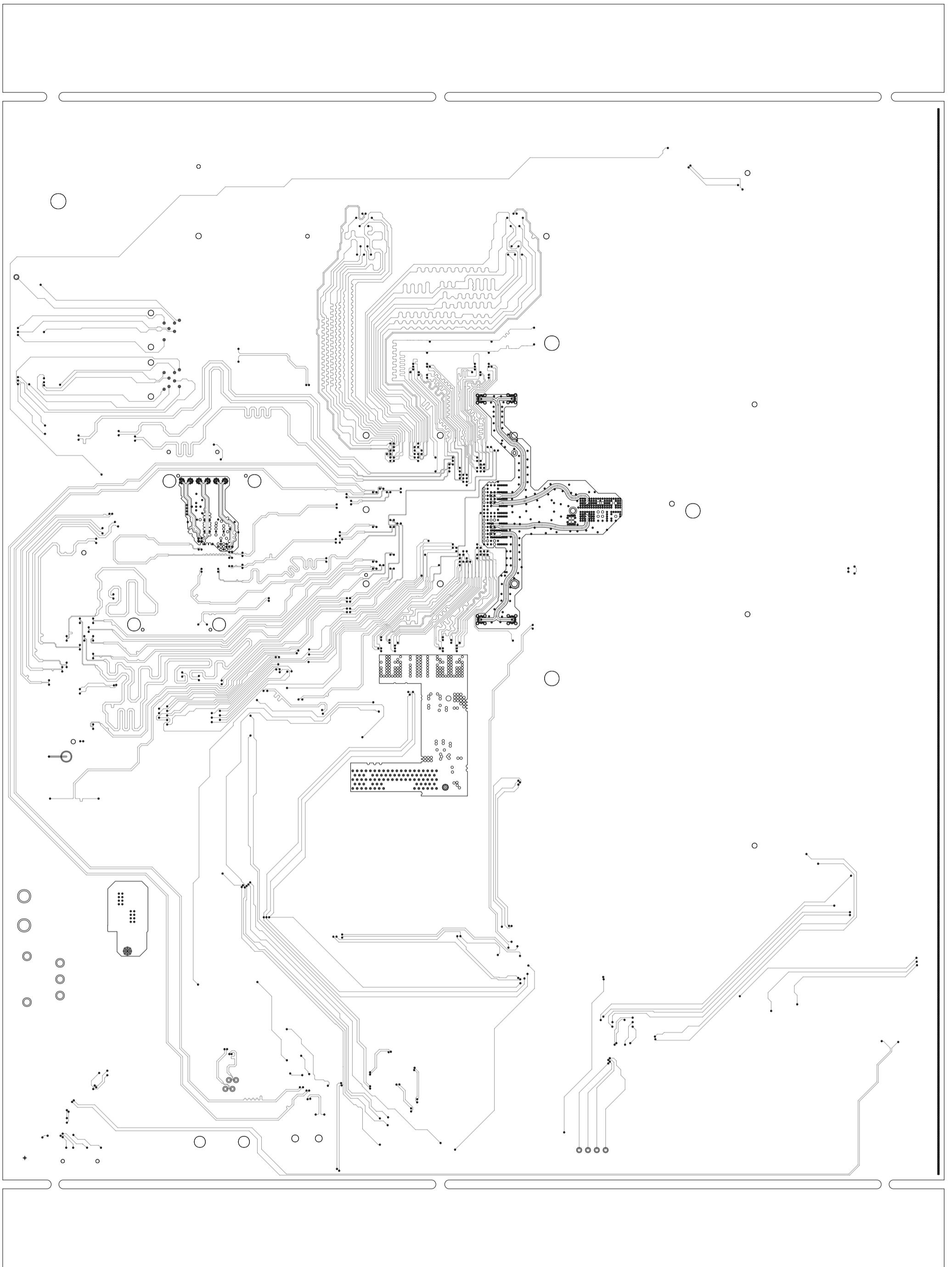
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PCB #	128-05023-01
Designed by	Xilinx
BOARD designer:	NHANO
	LAYER: L2_GND_RF_SIG
DATE:	12/12/2019
PHONE:	408-879-4993
2	XILINX DOC USE ONLY REVISION:A01 Version ba



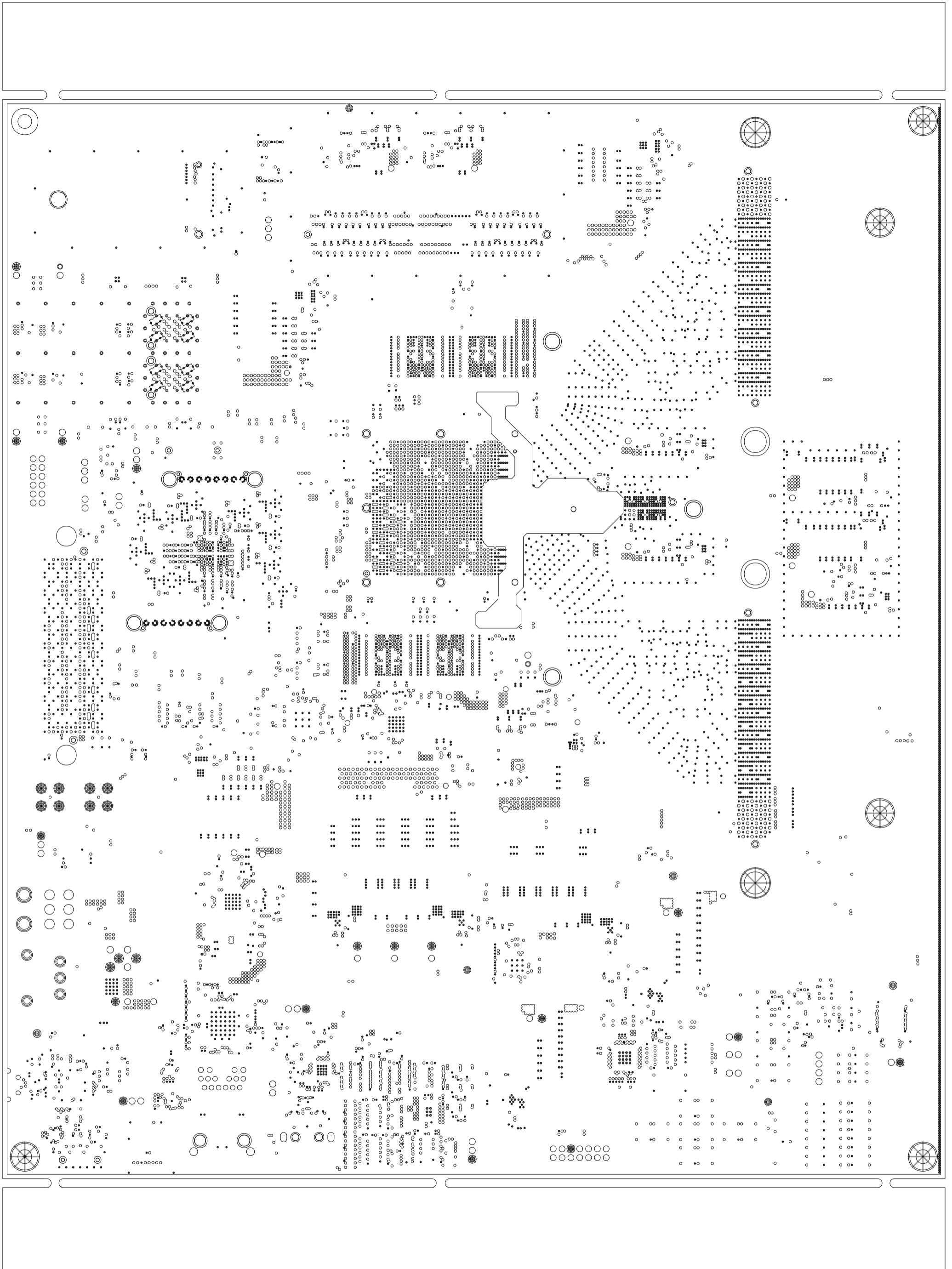
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PCB #	128-05023-01
Designed by	Xilinx
BOARD designer:	NHANO
	LAYER: L3_SIG_RF_GND
	DATE: 12/12/2019
	PHONE: 408-879-4993
3	XILINX DOC USE ONLY
	REVISION:A01 Version b0



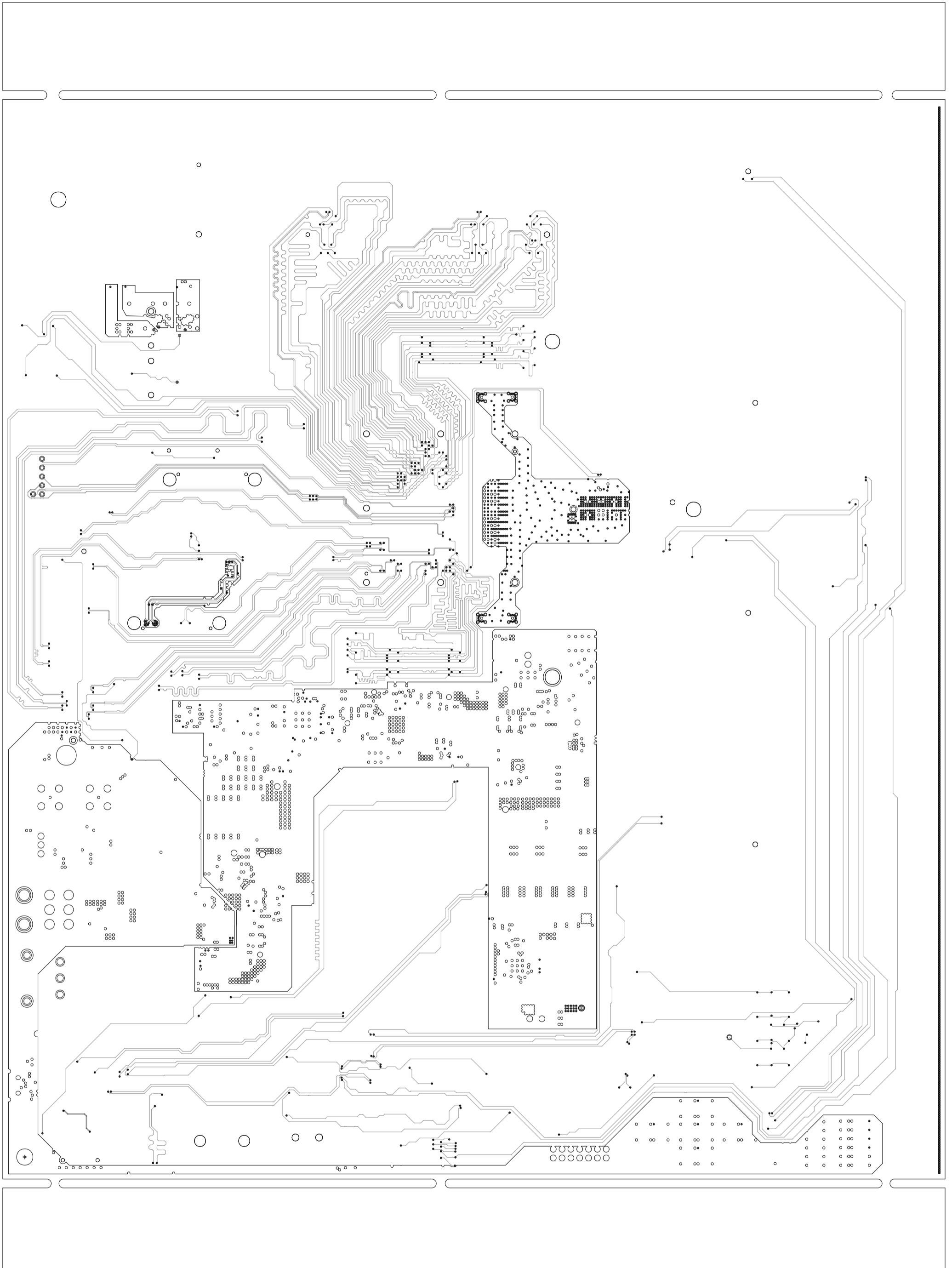
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PCB #	128-05023-01
Designed by	Xilinx
BOARD designer:	NHANO
	LAYER: L4_GND_RF_SIG
DATE:	12/12/2019
PHONE:	408-879-4993
4	XILINX DOC USE ONLY REVISION:A01 Version ba



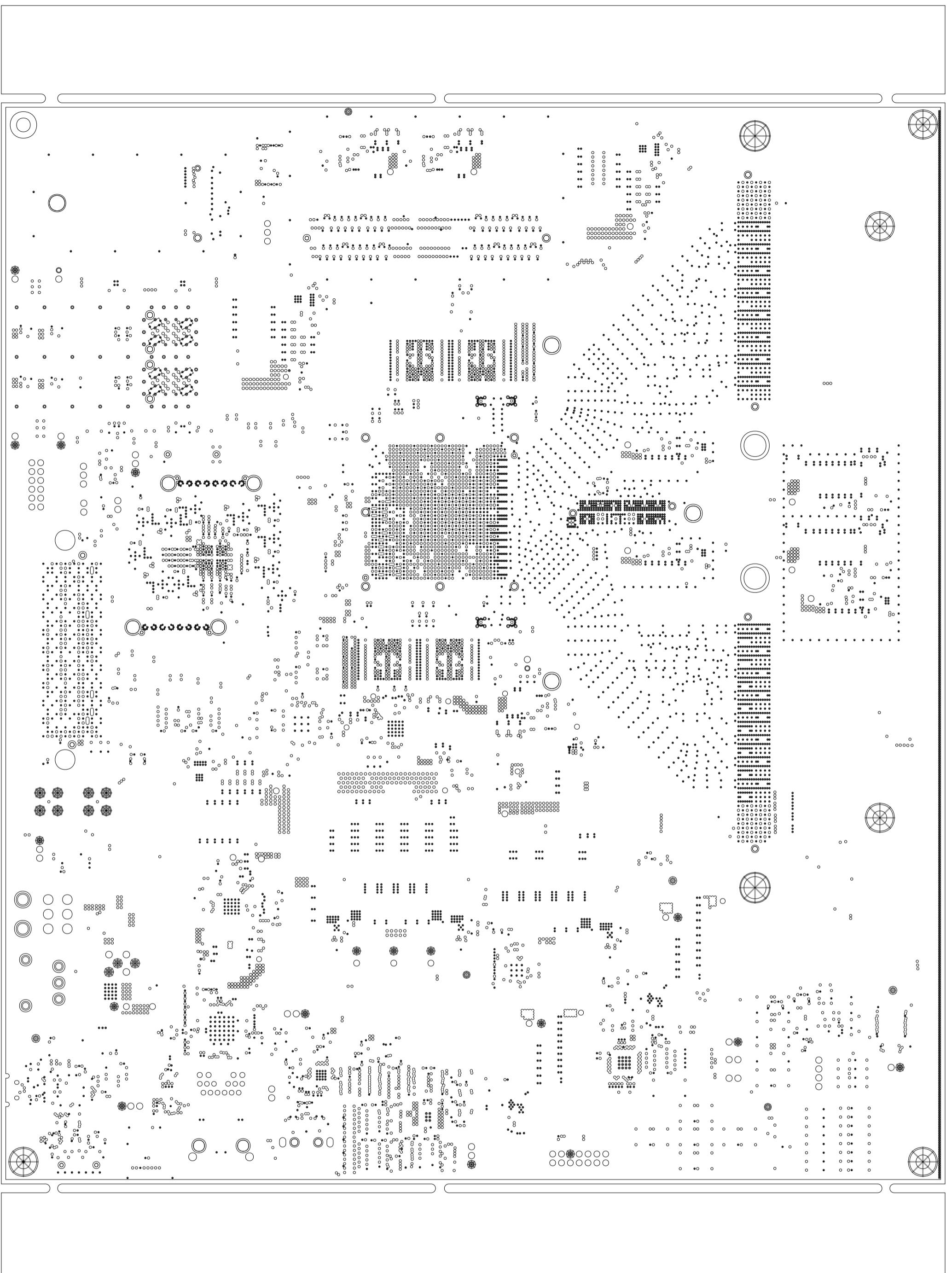
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PCB #	128-05023-01
Designed by	Xilinx
BOARD designer:	NHANO
5	XILINX DOC USE ONLY REVISION:A01 Version ba



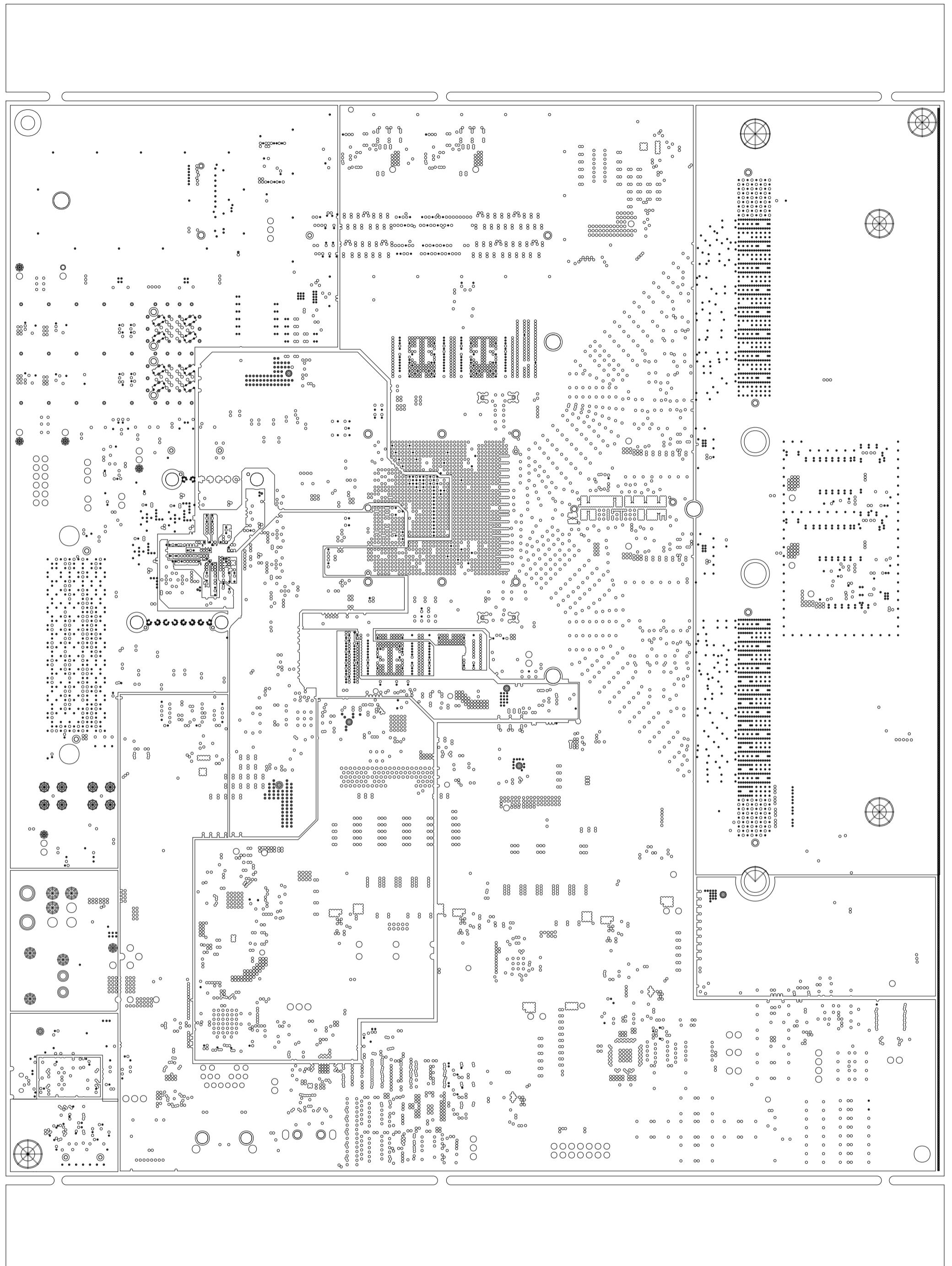
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB #	128-05023-01
Designed by	Xilinx
BOARD designer:	NHANO
	LAYER: L6_GND_RF_SIG
DATE:	12/12/2019
PHONE:	408-879-4993
6	XILINX DOC USE ONLY REVISION:A01 Version ba



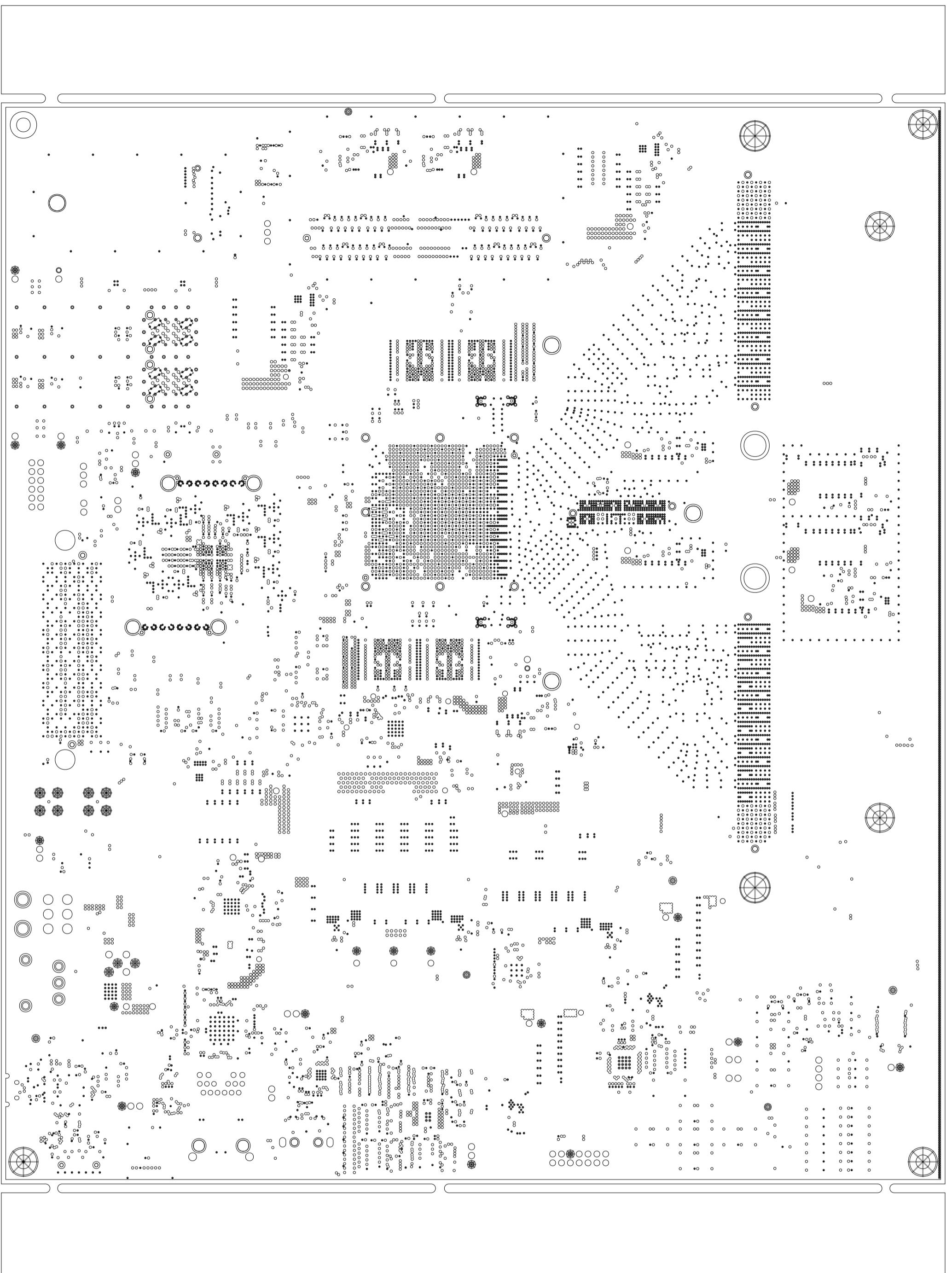
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB #	128-05023-01
Designed by Xilinx	LAYER: L7_SIG_RF_GND
BOARD designer:	DATE: 12/12/2019
NHANO	PHONE: 408-879-4993
7	XILINX DOC USE ONLY
	REVISION:A01 Version ba



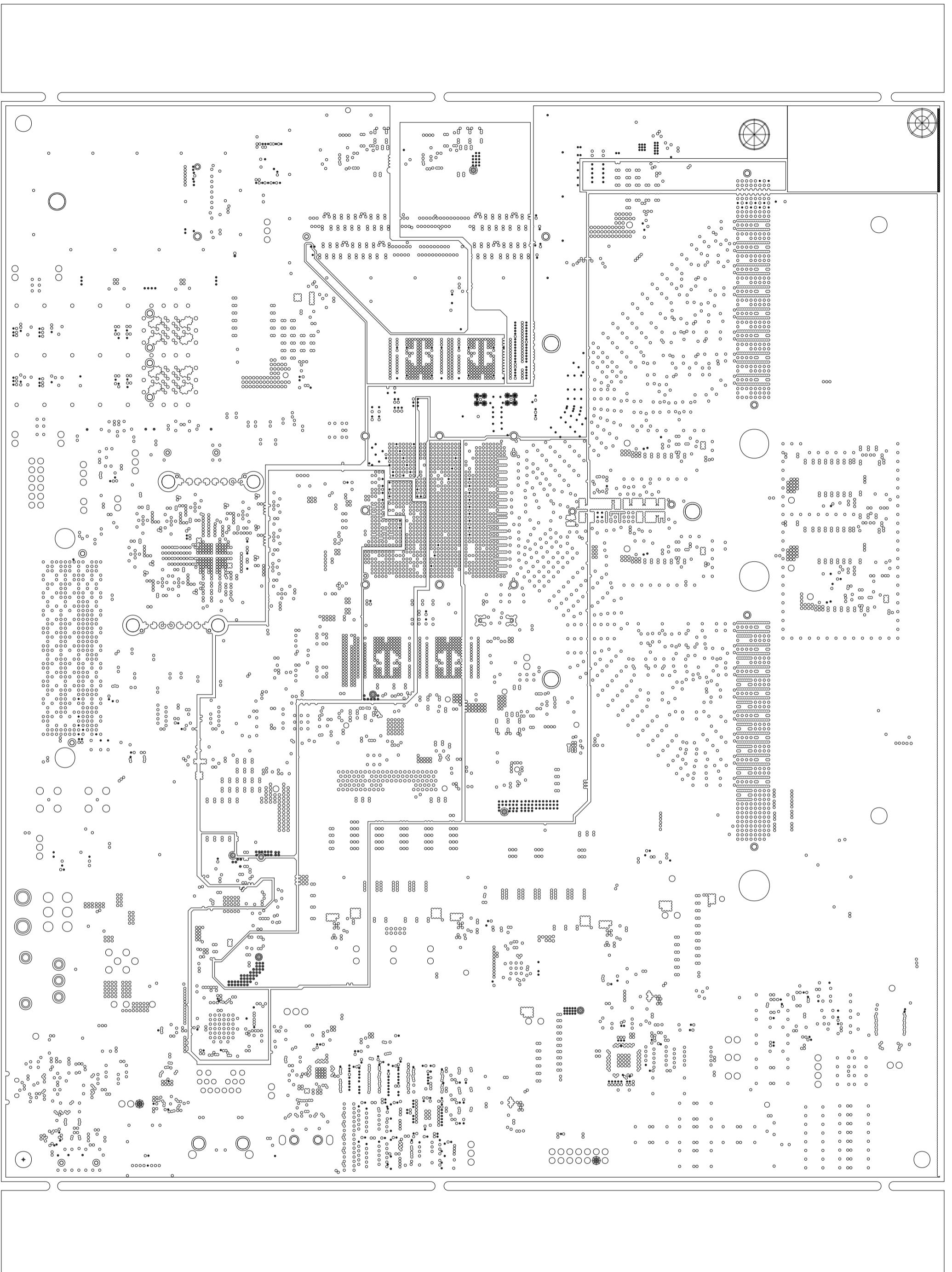
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB #	128-05023-01
Designed by Xilinx	LAYER: L8_GND
BOARD designer:	DATE: 12/12/2019
NHANO	PHONE: 408-879-4993
8	XILINX DOC USE ONLY
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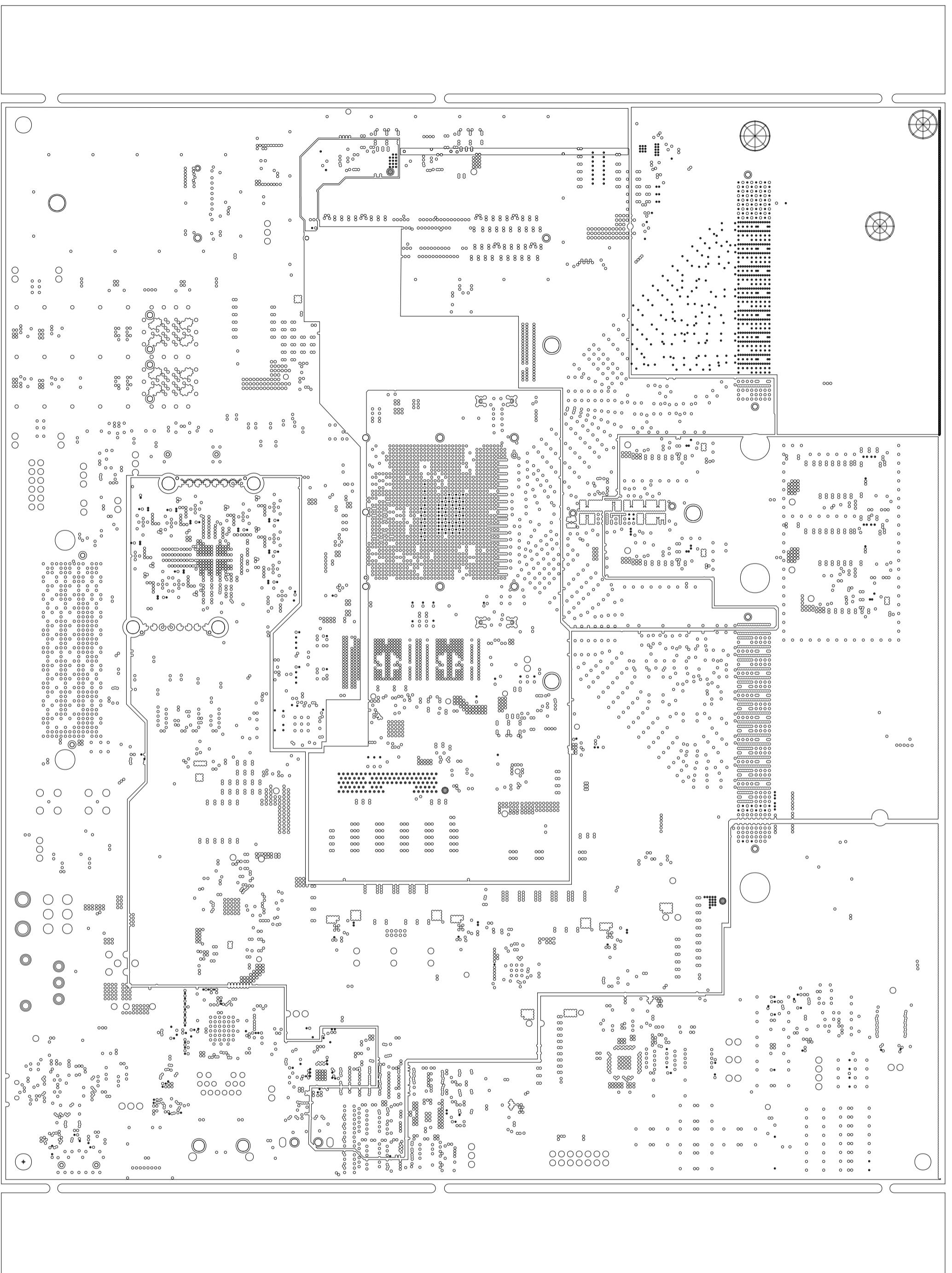
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB #	128-05023-01
Designed by Xilinx	LAYER: L9_PWR
BOARD designer:	NHANO
	DATE: 12/12/2019
	PHONE: 408-879-4993
9	XILINX DOC USE ONLY
	REVISION:A01 Version ba



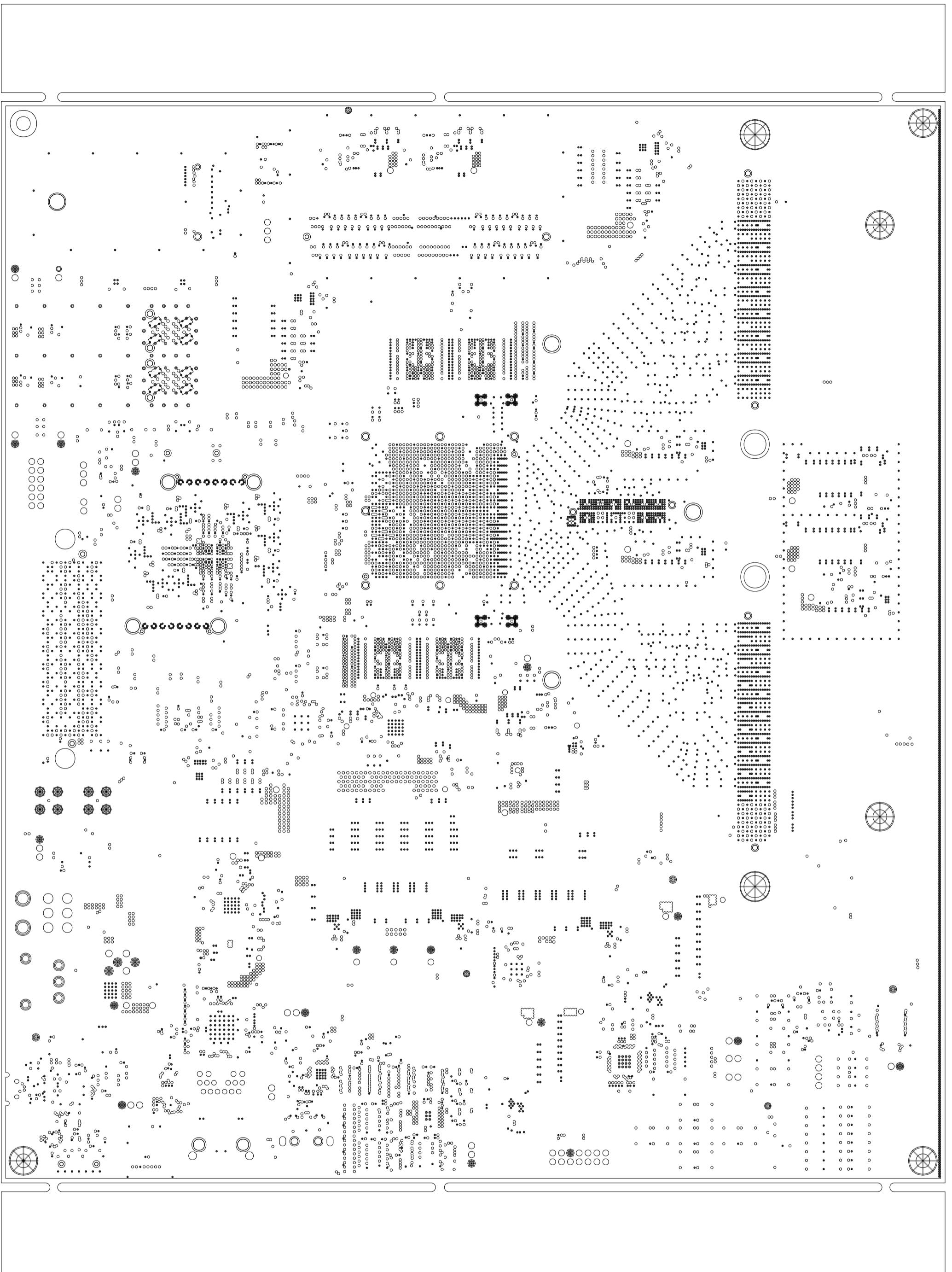
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB #	128-05023-01
Designed by	Xilinx
BOARD designer:	NHANO
10	XILINX DOC USE ONLY REVISION:A01 Version ba



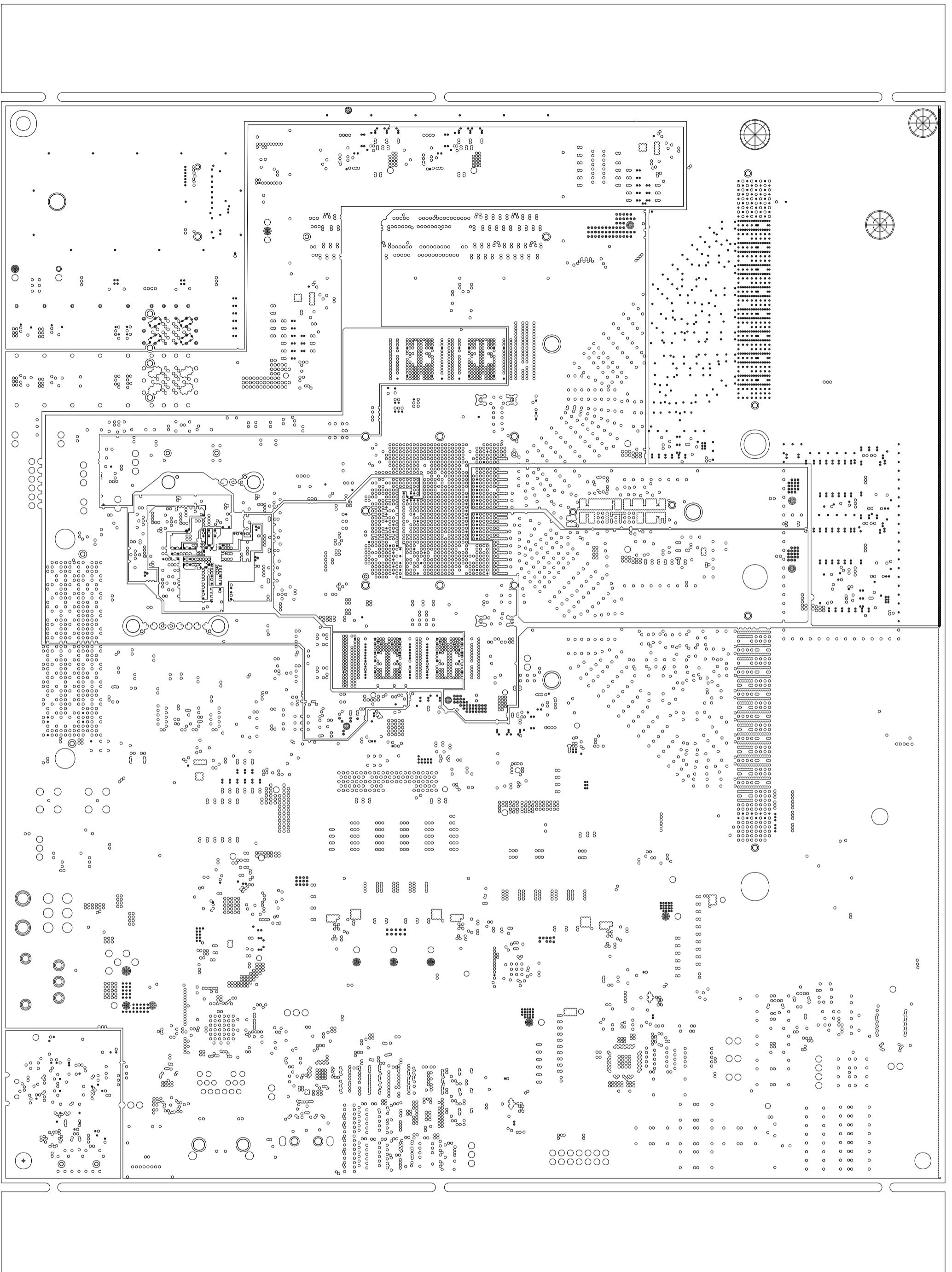
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB # 128-05023-01	LAYER: L11_PWR
Designed by Xilinx	DATE: 12/12/2019
BOARD designer: NHANO	PHONE: 408-879-4993
11	XILINX DOC USE ONLY REVISION:A01 Version ba



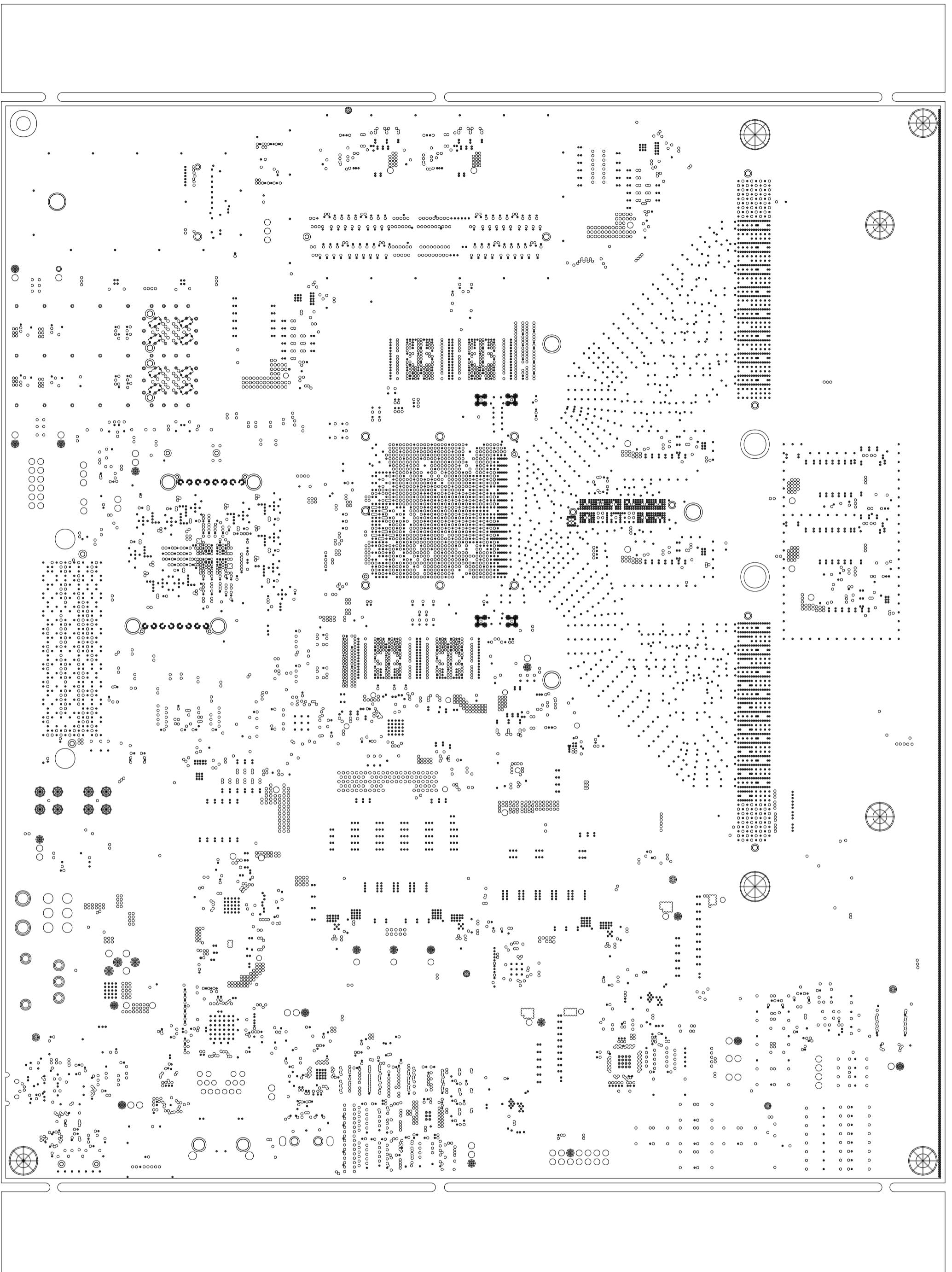
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB #	128-05023-01
Designed by	Xilinx
BOARD designer:	NHANO
12	XILINX DOC USE ONLY REVISION:A01 Version ba



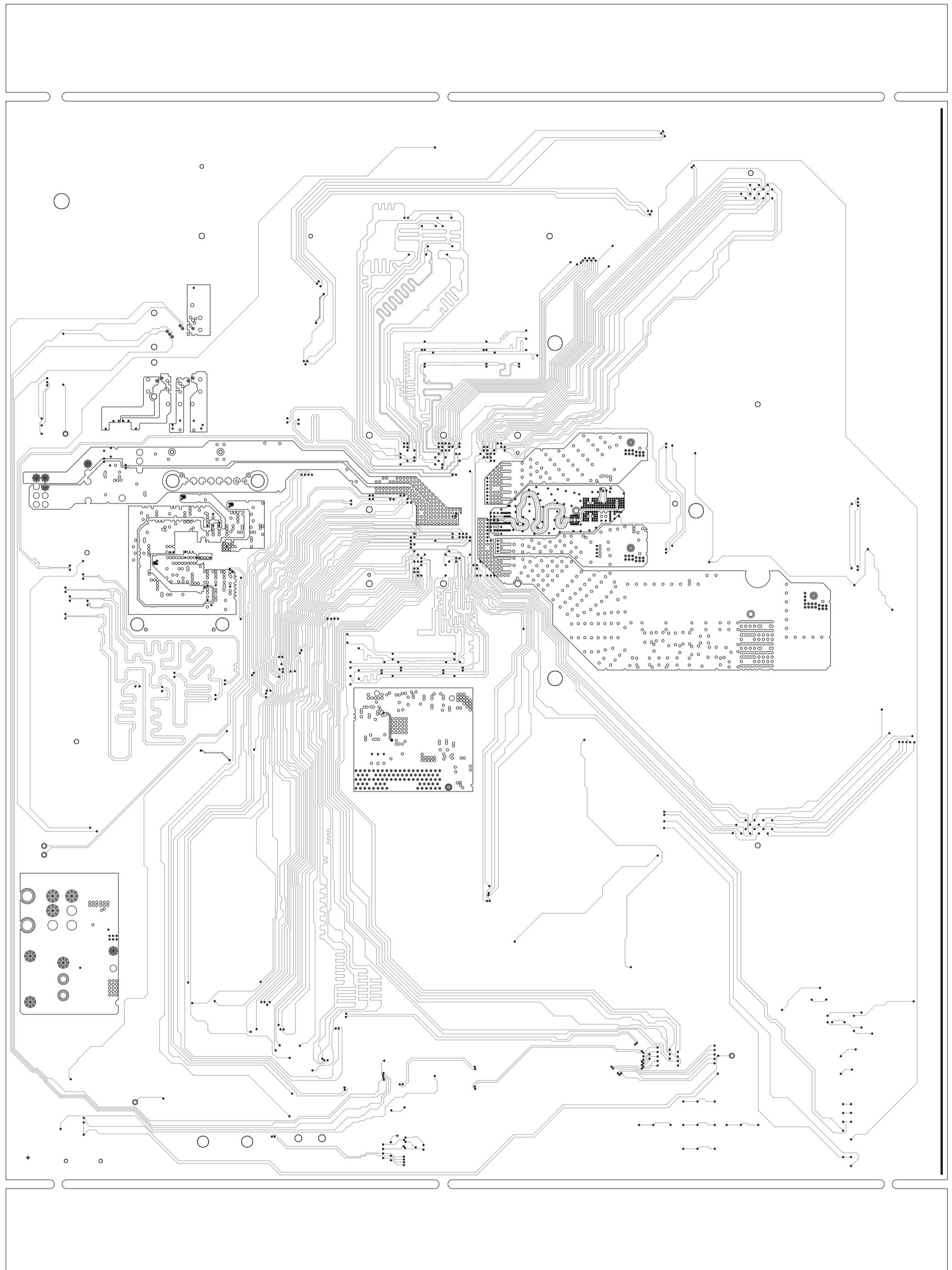
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PCB # 128-05023-01	LAYER: L13_GND
Designed by Xilinx	DATE: 12/12/2019
BOARD designer: NHANO	PHONE: 408-879-4993
13	XILINX DOC USE ONLY REVISION:A01 Version ba



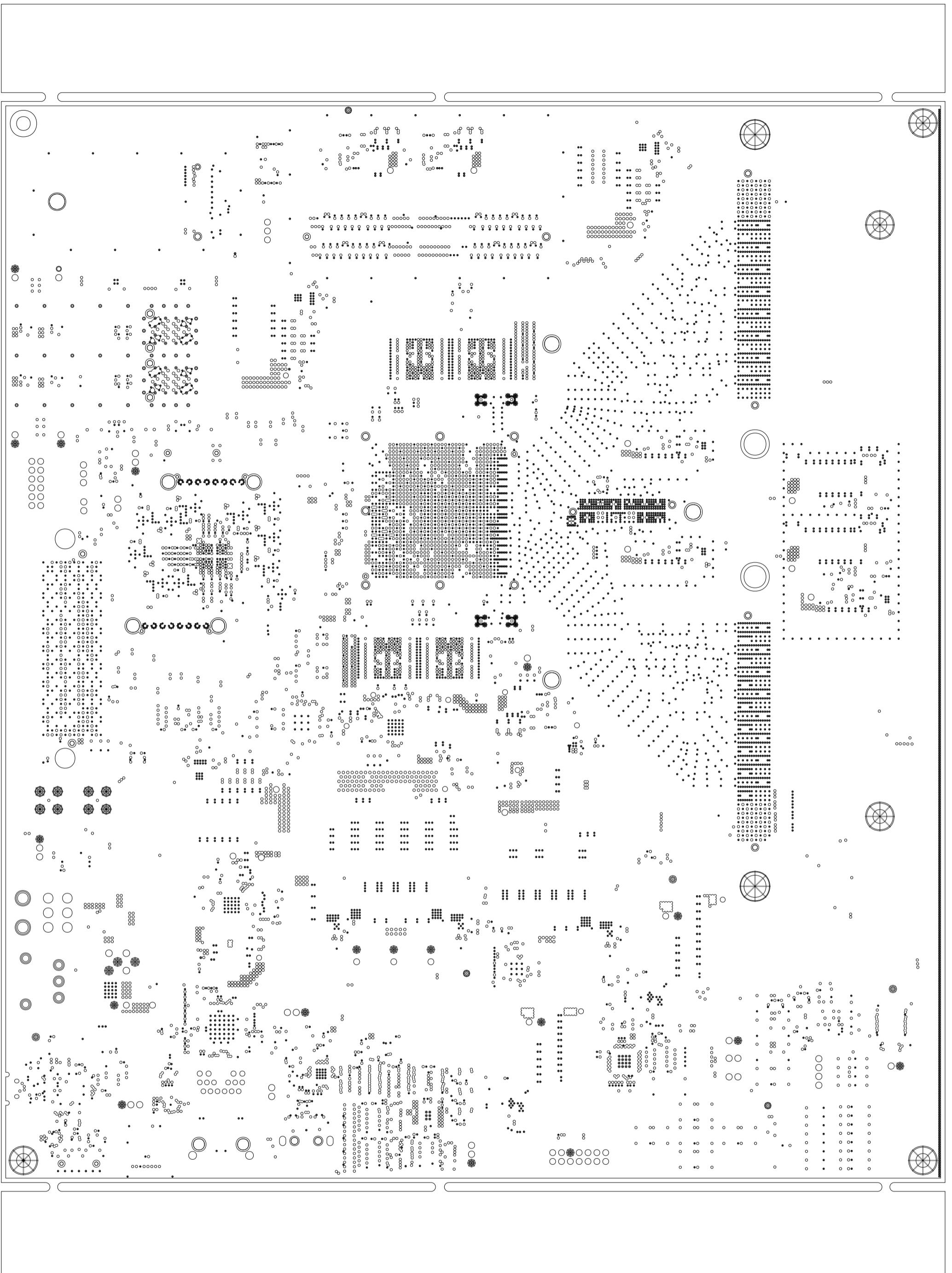
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PCB #	128-05023-01
Designed by Xilinx	LAYER: L14_PWR
BOARD designer:	DATE: 12/12/2019
NHANO	PHONE: 408-879-4993
14	XILINX DOC USE ONLY
	REVISION:A01 Version ba



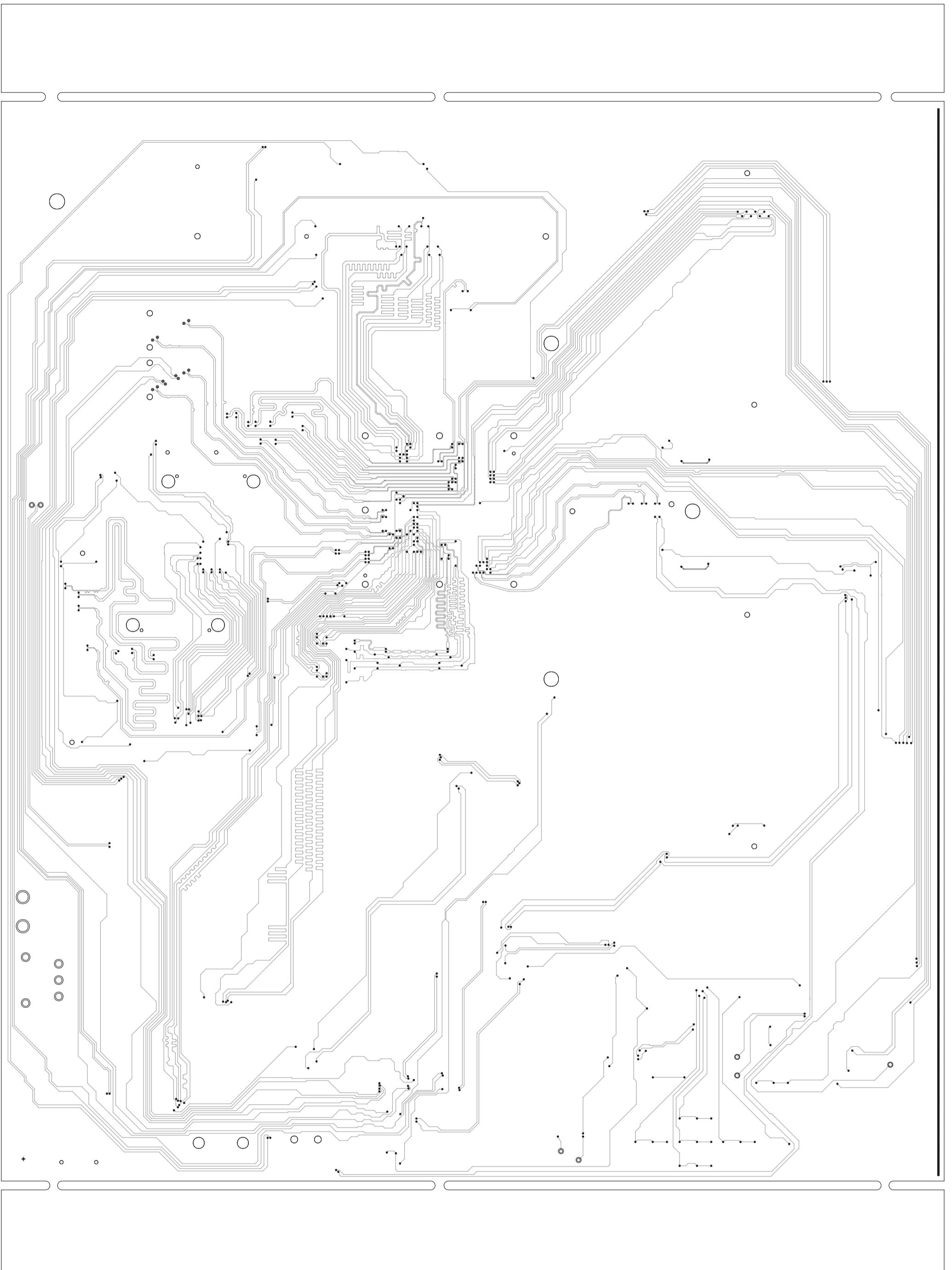
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PCB # 128-05023-01	LAYER: L15_GND
Designed by Xilinx	DATE: 12/12/2019
BOARD designer: NHANO	PHONE: 408-879-4993
15	XILINX DOC USE ONLY REVISION:A01 Version ba



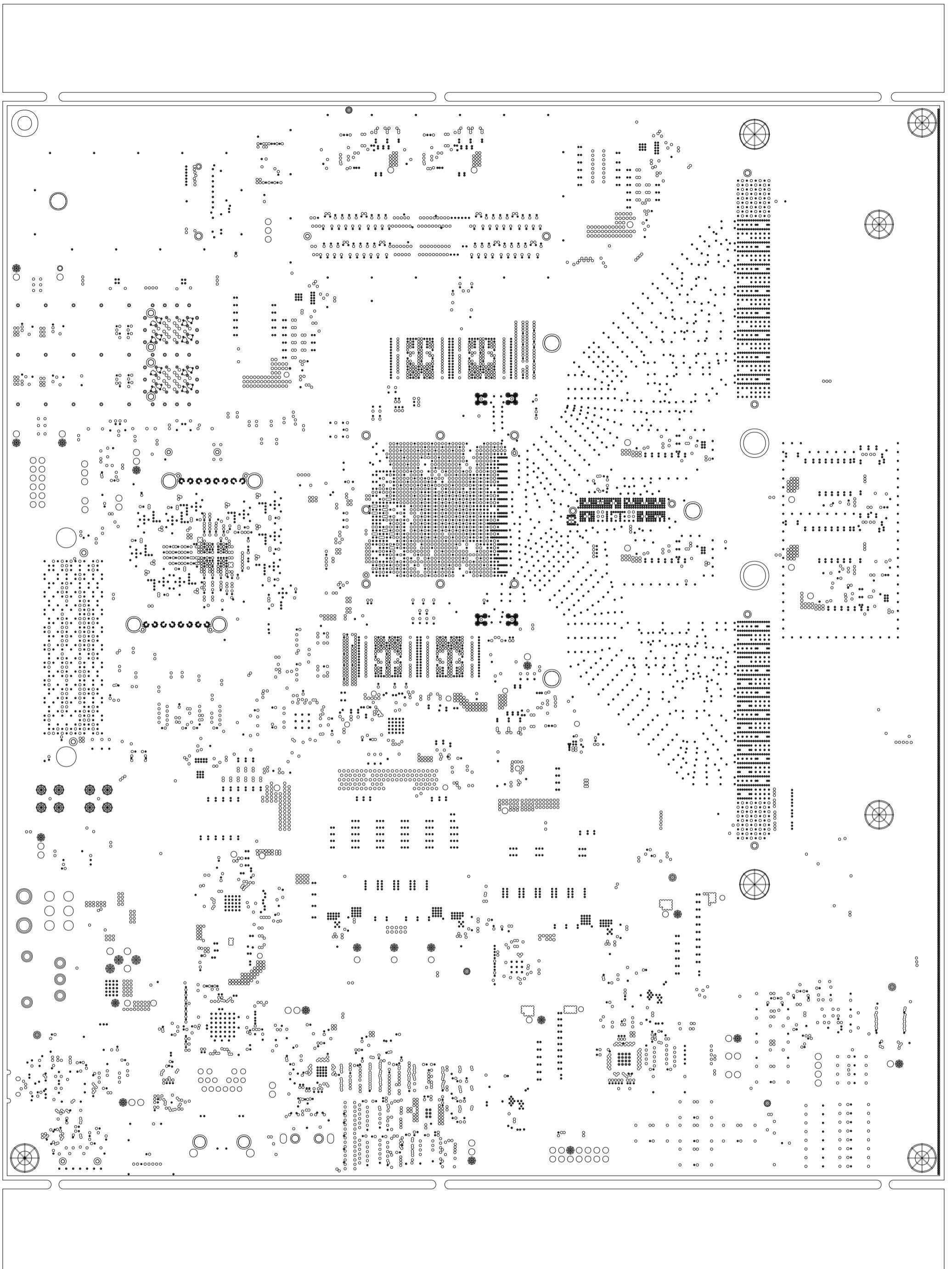
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB #	128-05023-01
Designed by	Xilinx
BOARD designer:	NHANO
16	XILINX DOC USE ONLY REVISION:A01 Version ba



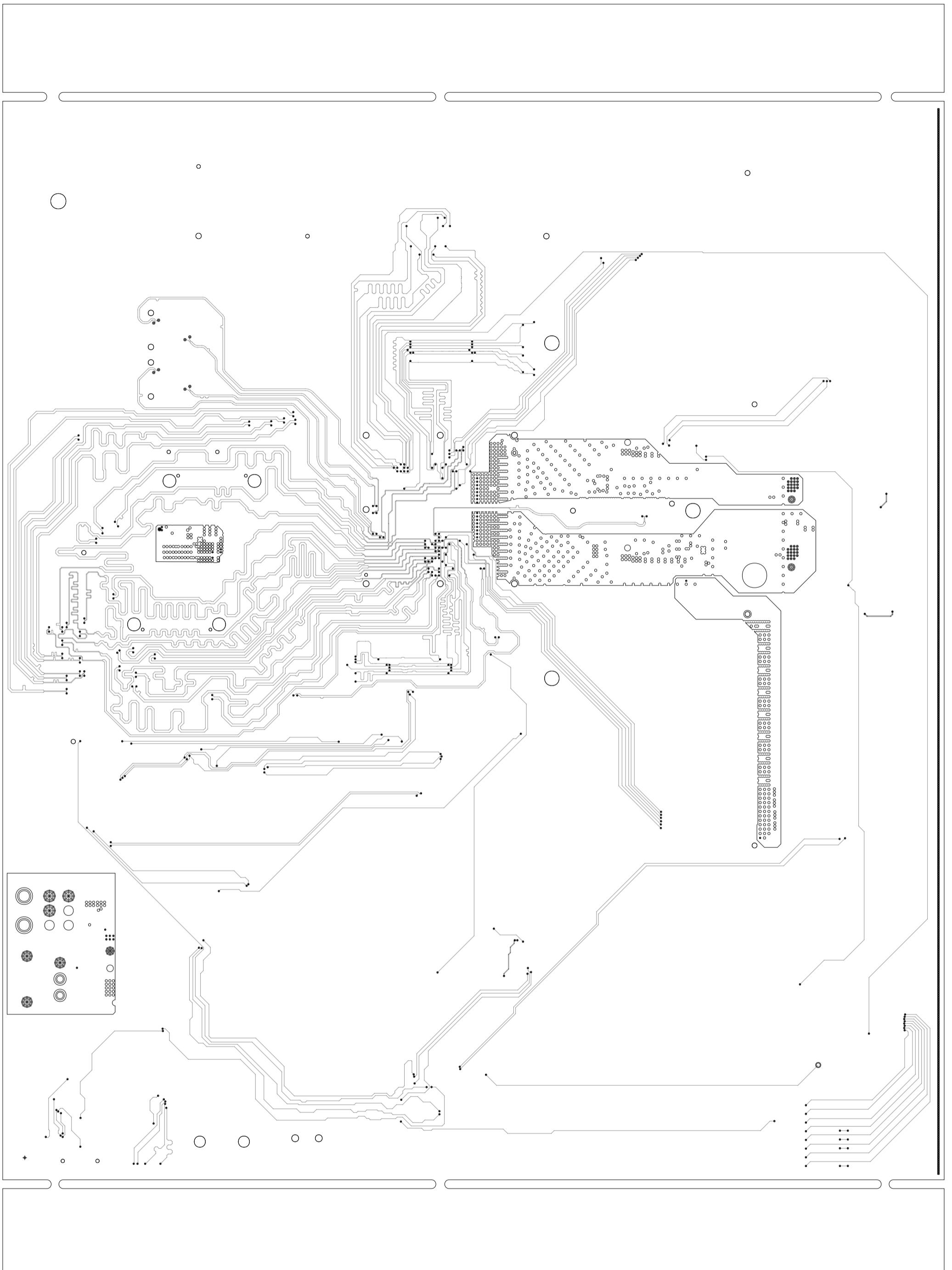
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB # 128-05023-01	LAYER: L17_GND
Designed by Xilinx	DATE: 12/12/2019
BOARD designer: NHANO	PHONE: 408-879-4993
17	XILINX DOC USE ONLY REVISION:A01 Version ba



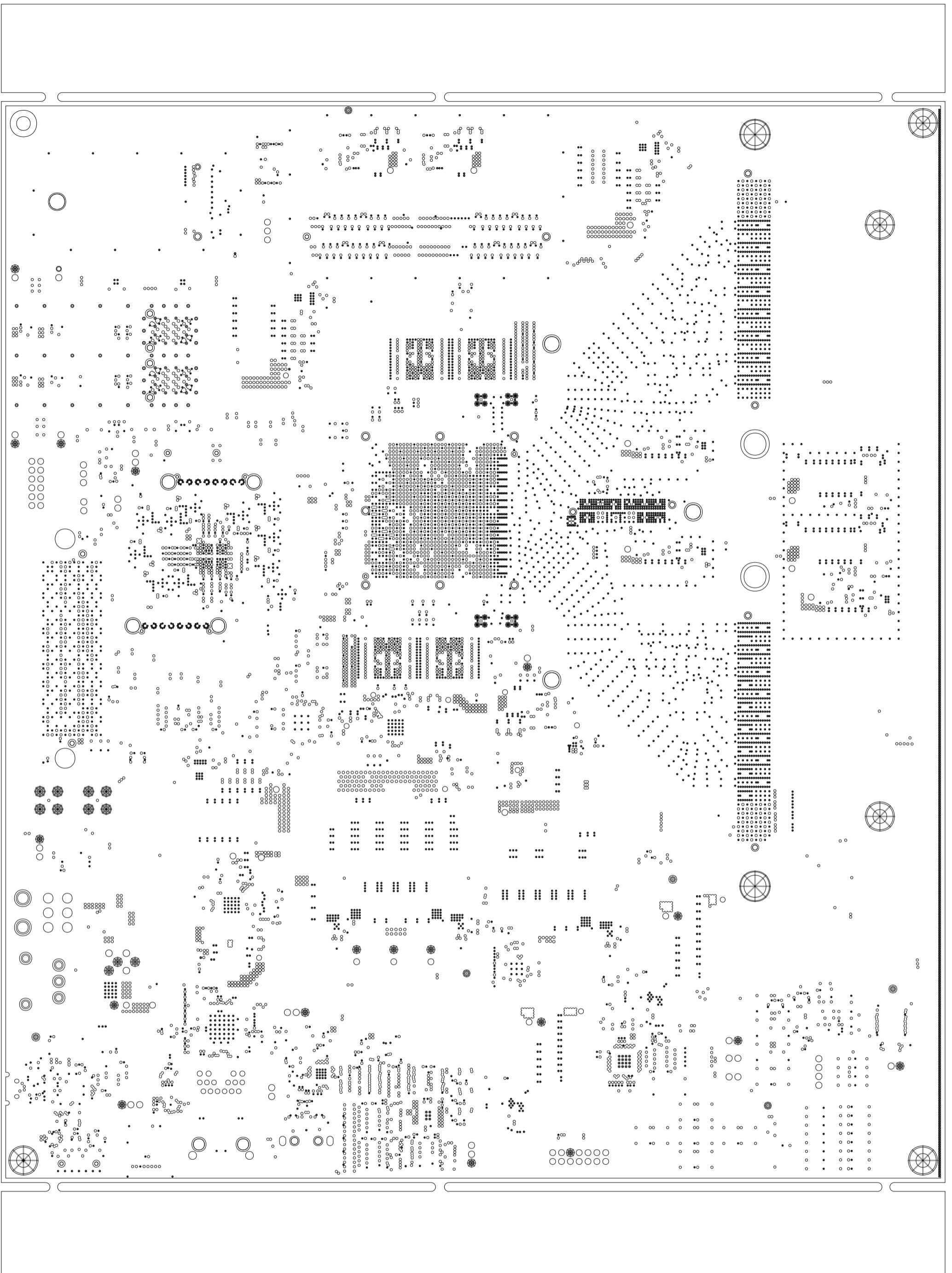
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB #	128-05023-01
Designed by	Xilinx
BOARD designer:	NHANO
LAYER:	L18_SIG
DATE:	12/12/2019
PHONE:	408-879-4993
18	XILINX DOC USE ONLY REVISION:A01 Version ba



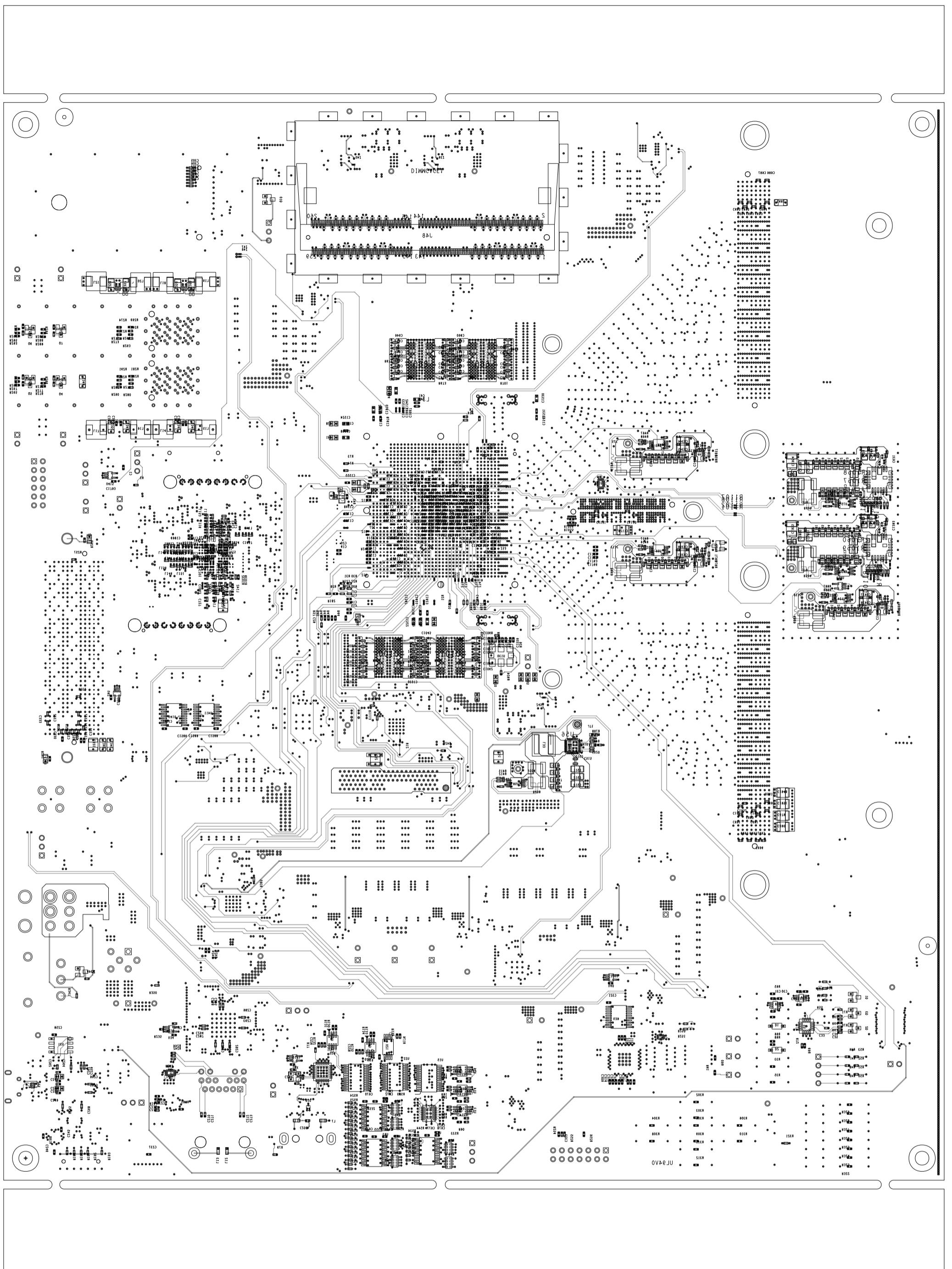
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB # 128-05023-01	LAYER: L19_GND
Designed by Xilinx	DATE: 12/12/2019
BOARD designer: NHANO	PHONE: 408-879-4993
19	XILINX DOC USE ONLY REVISION:A01 Version ba



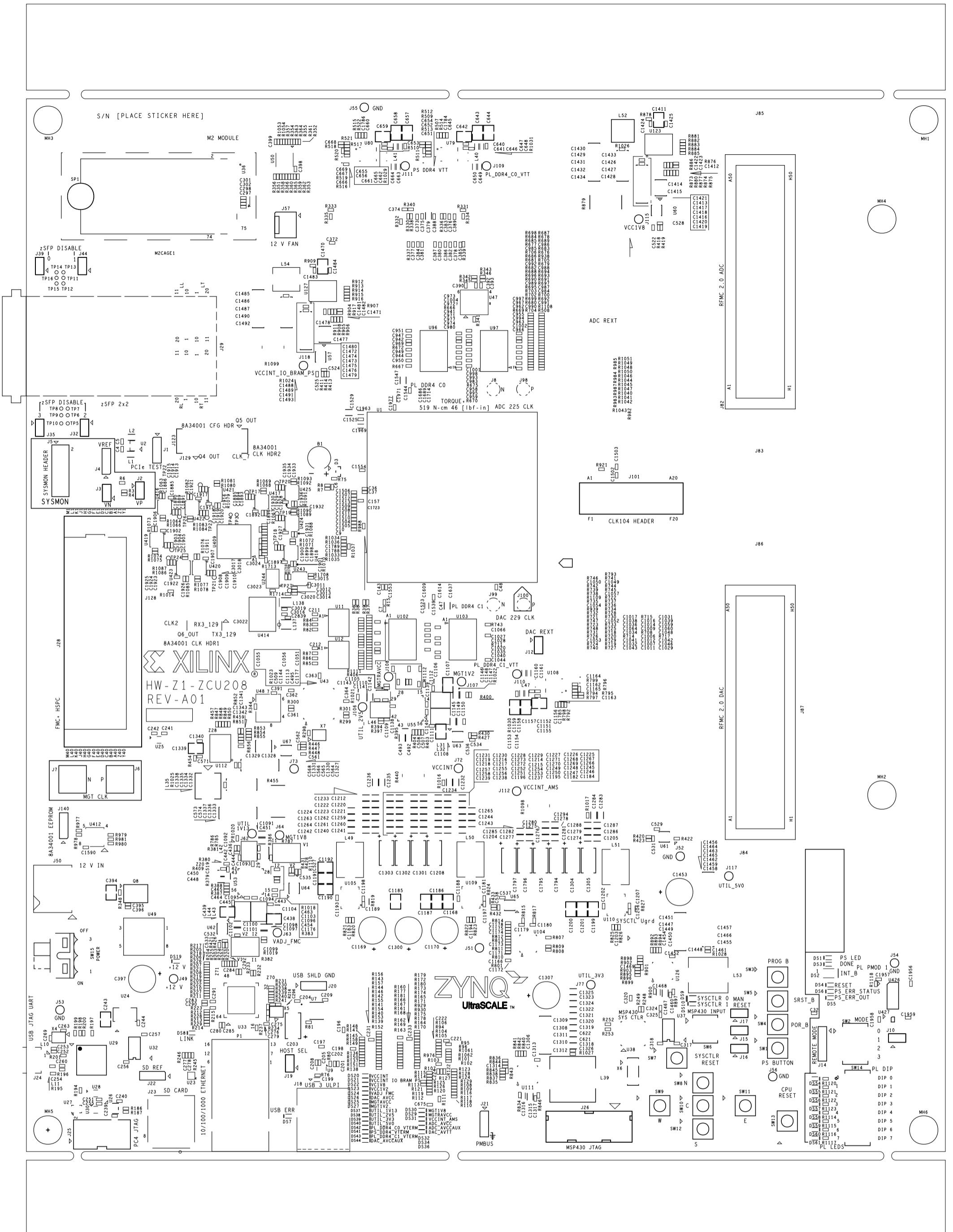
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB #	128-05023-01
Designed by	Xilinx
BOARD designer:	NHANO
20	XILINX DOC USE ONLY REVISION:A01 Version ba

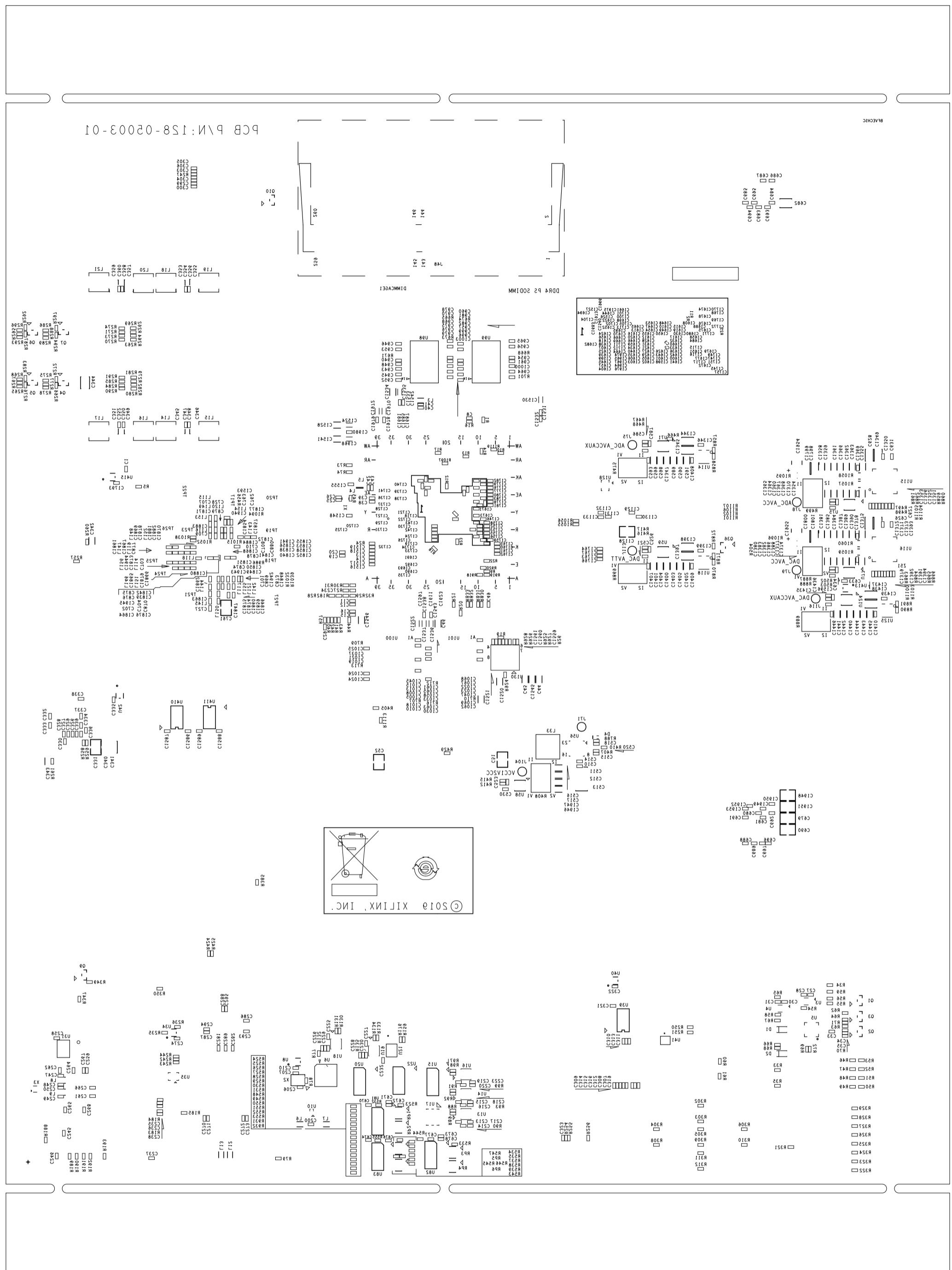


ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB # 128-05023-01	LAYER: L21_GND
Designed by Xilinx	DATE: 12/12/2019
BOARD designer: NHANO	PHONE: 408-879-4993
21	XILINX DOC USE ONLY REVISION:A01 Version ba

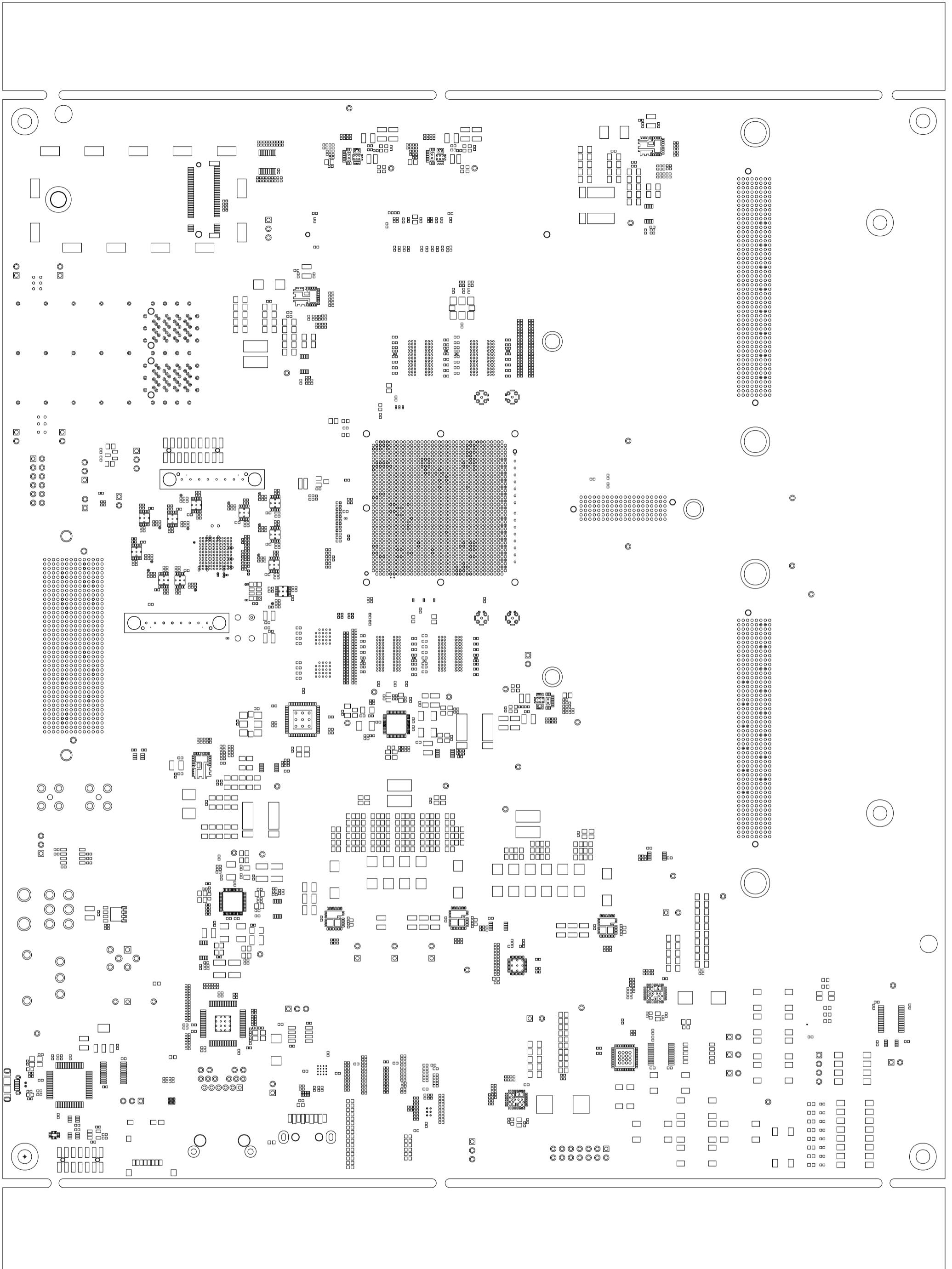


ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB # 128-05023-01	LAYER: L22_BOTTOM
Designed by Xilinx	DATE: 12/12/2019
BOARD designer: NHANO	PHONE: 408-879-4993
	XILINX DOC USE ONLY
22	REVISION:A01 Version ba

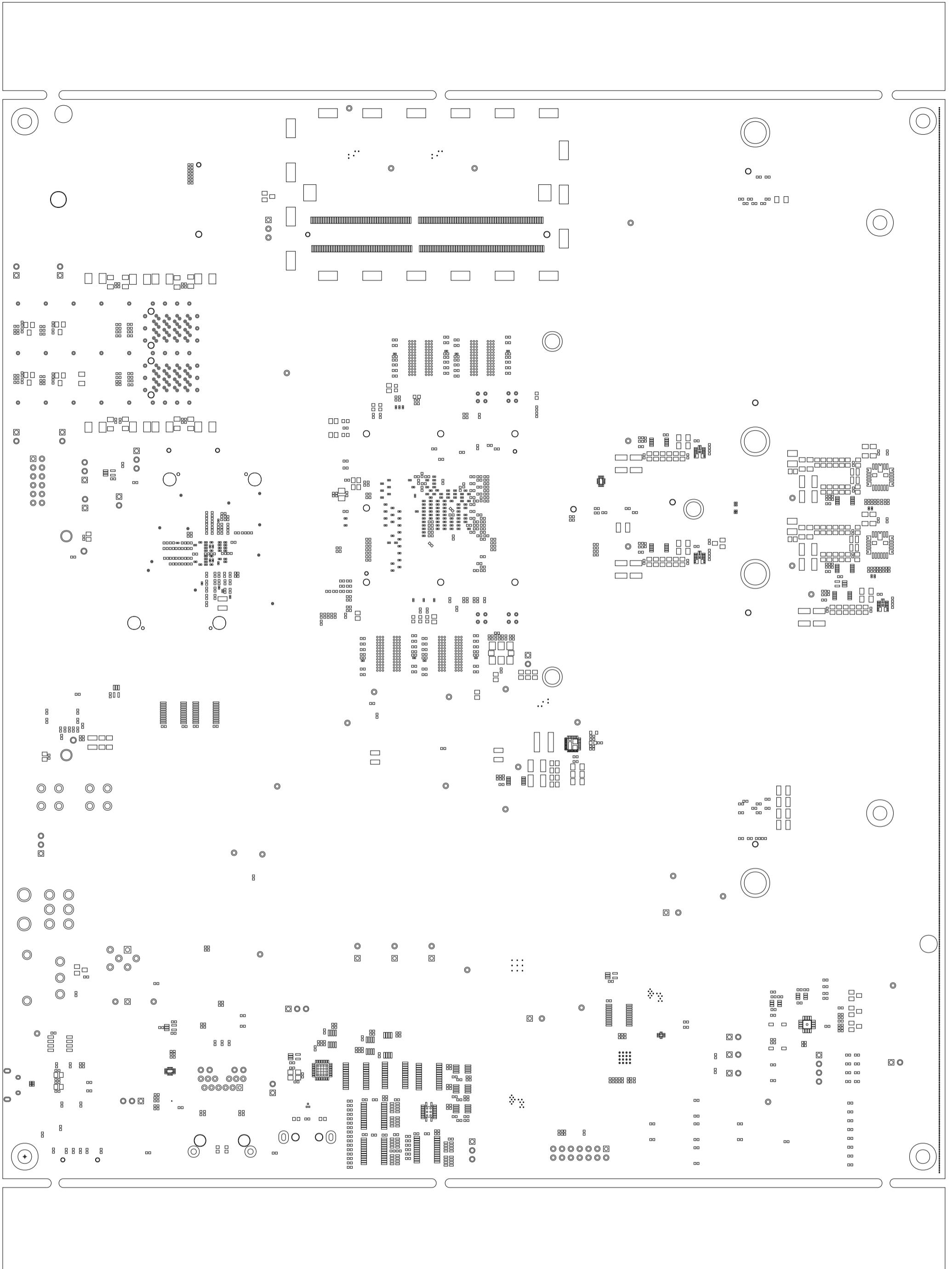




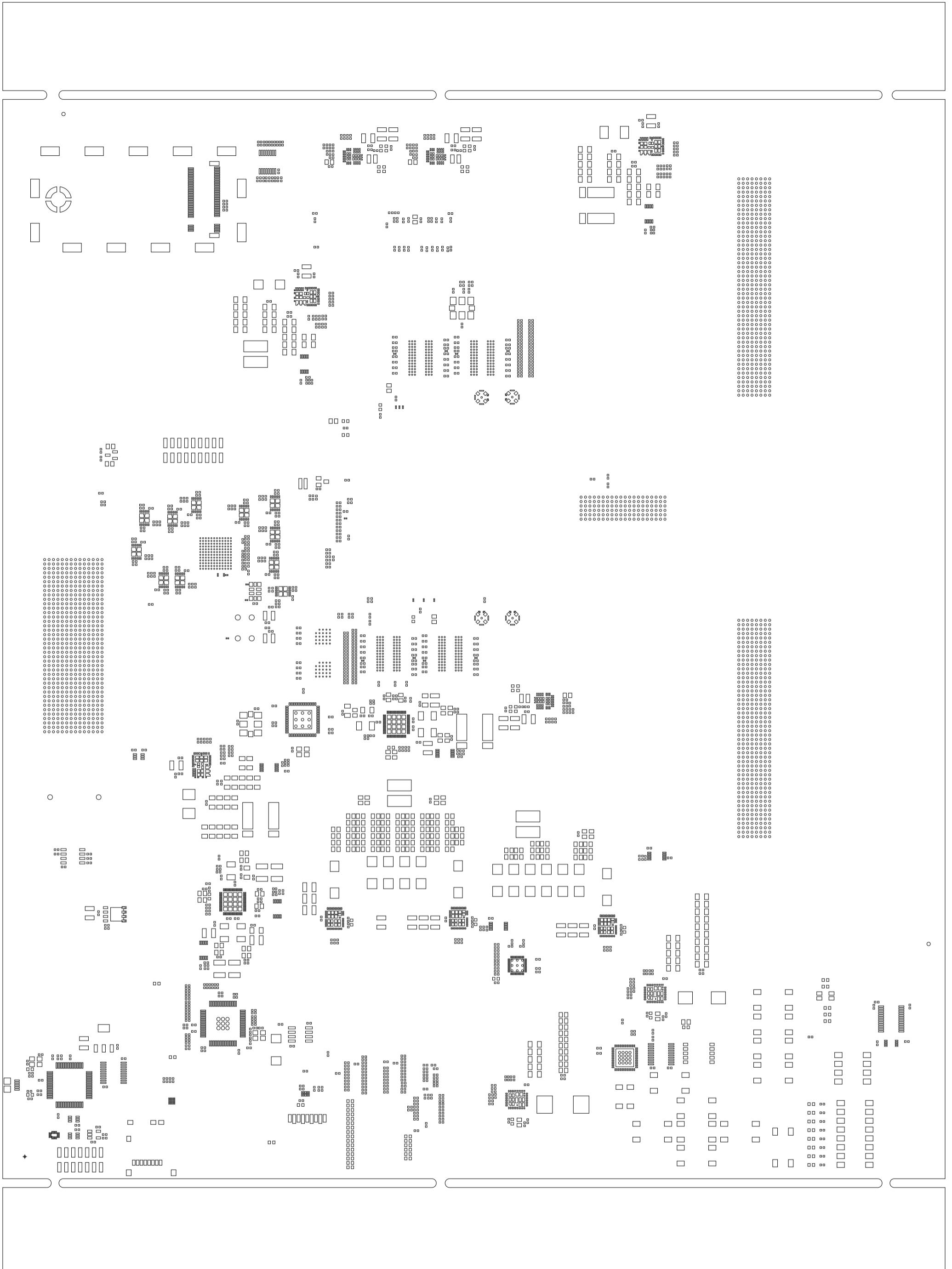
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB #	128-05023-01
Designed by Xilinx	LAYER: SILKSCREEN BOTTOM
BOARD designer:	DATE: 12/12/2019
NHANO	PHONE: 408-879-4993
24	XILINX DOC USE ONLY
	REVISION:A01 Version b0



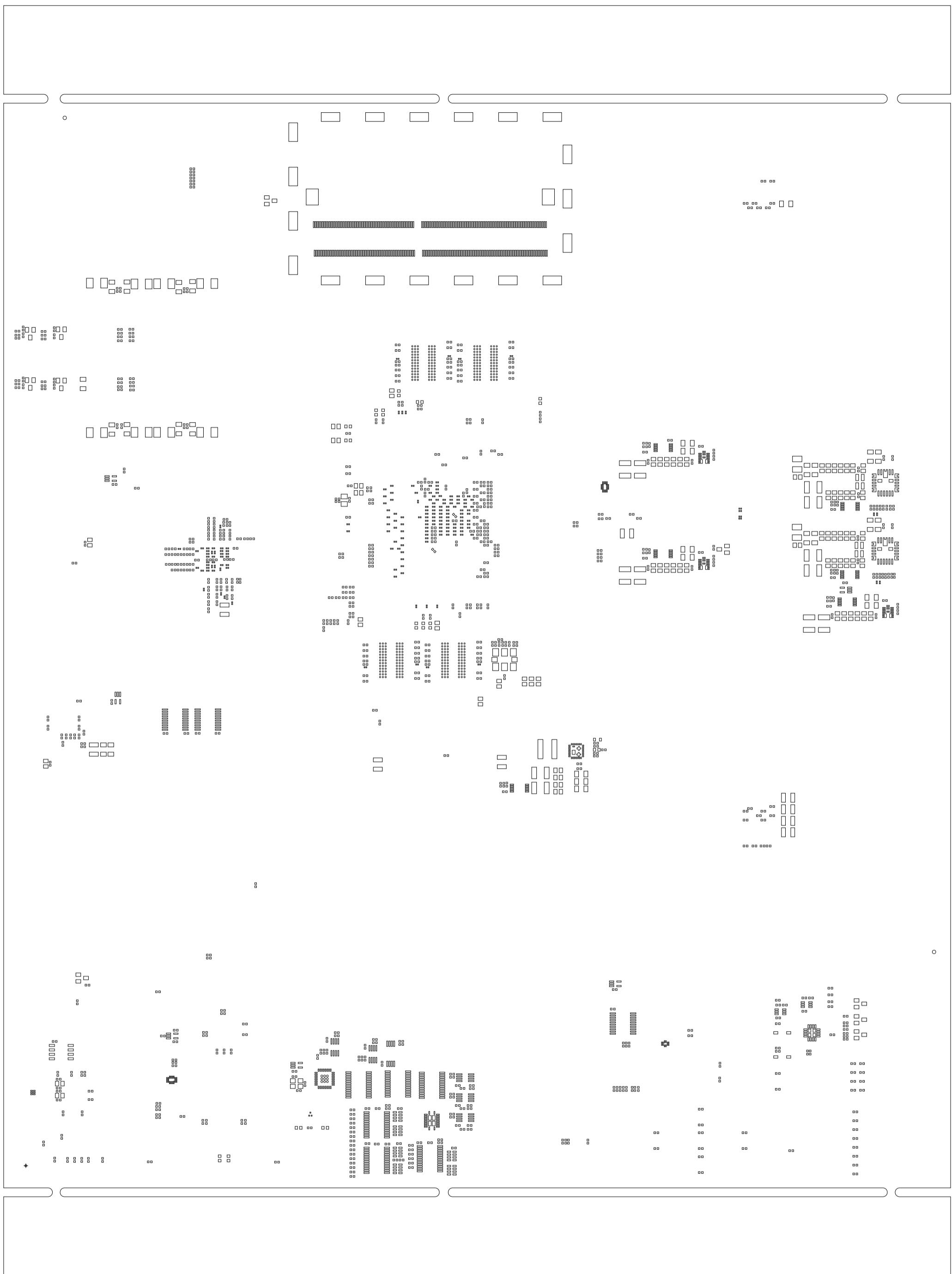
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB # 128-05023-01	LAYER: MASK_TOP
Designed by Xilinx	DATE: 12/12/2019
BOARD designer: NHANO	PHONE: 408-879-4993
	XILINX DOC USE ONLY
25	REVISION:A01 Version ba



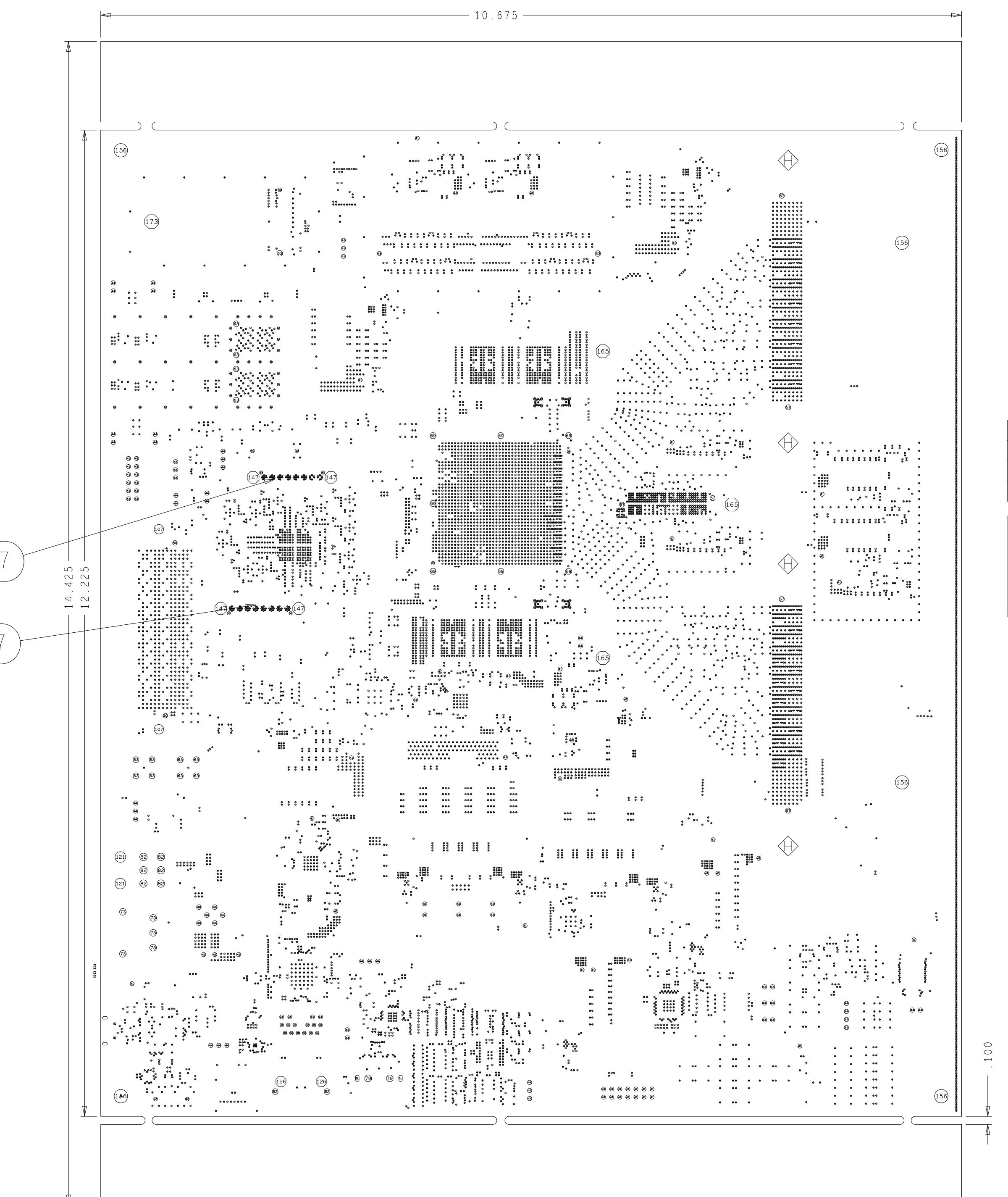
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB # 128-05023-01	LAYER: MASK_BOTTOM
Designed by Xilinx	DATE: 12/12/2019
BOARD designer: NHANO	PHONE: 408-879-4993
	XILINX DOC USE ONLY
26	REVISION:A01 Version ba



ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB # 128-05023-01	LAYER: PASTE_TOP
Designed by Xilinx	DATE: 12/12/2019
BOARD designer: NHANO	PHONE: 408-879-4993
	XILINX DOC USE ONLY
27	REVISION:A01 Version ba



ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU208	
PCB #	128-05023-01
Designed by	Xilinx
BOARD designer:	NHANO
	XILINX DOC USE ONLY
28	REVISION:A01 Version b0



BACKDRILL: BOTTOM to L06_GND_RF_SIG				
ALL UNITS ARE IN MILS				
FIGURE	BD_SIZE	MNC_LAYER	MAX_DEPTH	MFG_STUB QTY
.	9.8	L05 SIG RF GND	90.5	8.0 96

NOTES:  
 - MNC\_LAYER: MUST-NOT-CUT-LAYER  
 - MAX\_DEPTH: DEPTH FROM START LAYER TO THE SURFACE OF MUST-NOT-CUT-LAYER  
 - MFG\_STUB : MANUFACTURING STUB LENGTH

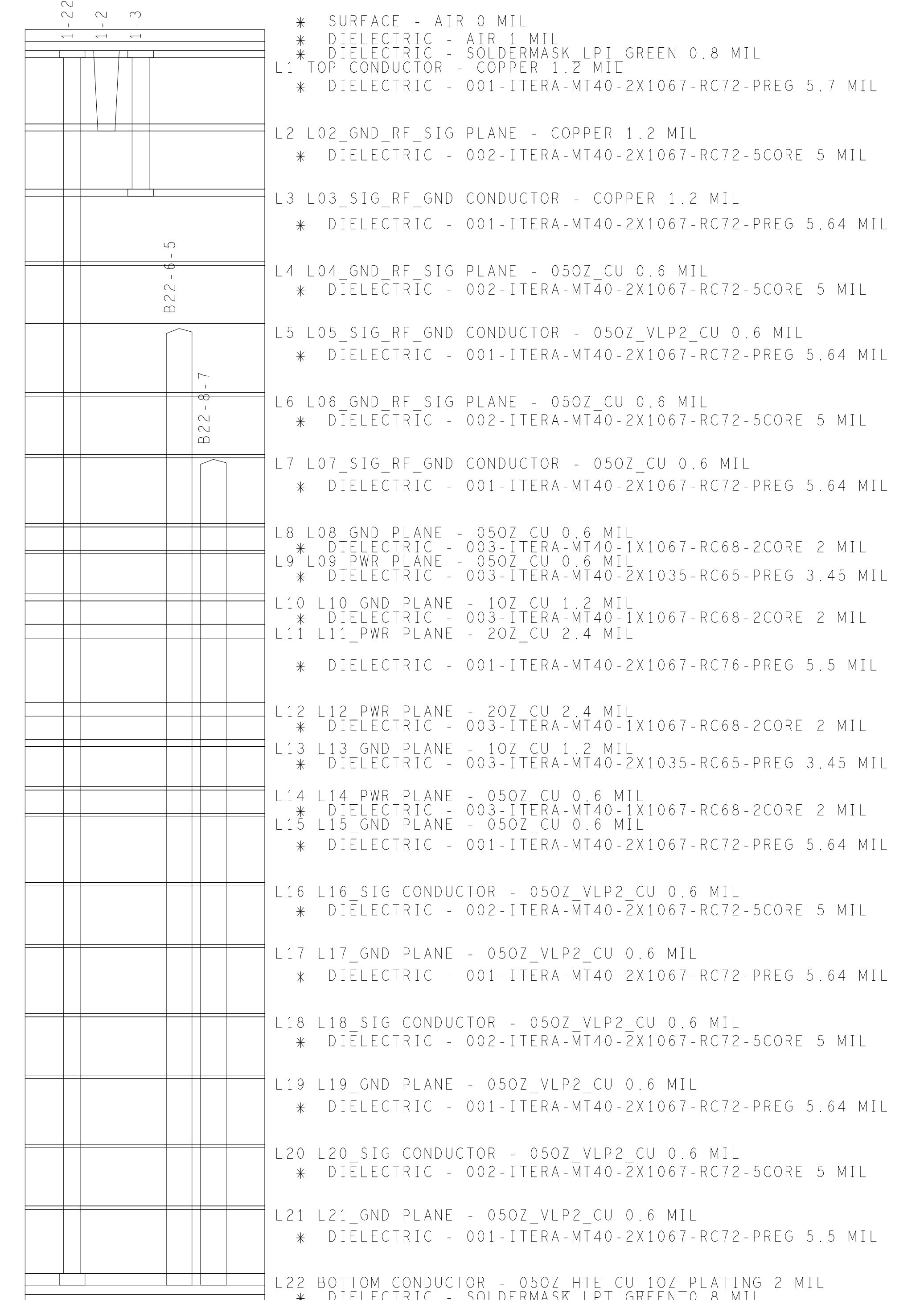
BACKDRILL: BOTTOM to L08_GND				
ALL UNITS ARE IN MILS				
FIGURE	BD_SIZE	MNC_LAYER	MAX_DEPTH	MFG_STUB QTY
.	9.8	L07 SIG RF GND	78.66	8.0 42

NOTES:  
 - MNC\_LAYER: MUST-NOT-CUT-LAYER  
 - MAX\_DEPTH: DEPTH FROM START LAYER TO THE SURFACE OF MUST-NOT-CUT-LAYER  
 - MFG\_STUB : MANUFACTURING STUB LENGTH

DRILL CHART: TOP to L03_SIG_RF_GND				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
.	9.8	+0.0/-9.8	PLATED	212

DRILL CHART: TOP to L02_GND_RF_SIG				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
.	6.0	+0.0/-6.0	PLATED	8
.	6.0	+0.0/-6.0	PLATED	78

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
.	7.9	+0.0/-7.9	PLATED	1
.	9.8	+0.0/-9.8	PLATED	10649
.	12.0	+0.0/-12.0	PLATED	516
.	14.0	+2.0/-2.0	PLATED	80
.	22.0	+2.0/-2.0	PLATED	39
.	23.0	+3.0/-3.0	PLATED	16
.	35.0	+3.0/-3.0	PLATED	2
.	36.0	+3.0/-3.0	PLATED	12
.	40.0	+3.0/-3.0	PLATED	71
.	41.0	+3.0/-3.0	PLATED	4
.	44.0	+3.0/-3.0	PLATED	46
.	48.0	+3.0/-3.0	PLATED	6
.	62.0	+3.0/-3.0	PLATED	2
.	63.0	+3.0/-3.0	PLATED	8
.	73.0	+3.0/-3.0	PLATED	5
.	82.0	+3.0/-3.0	PLATED	6
.	107.0	+3.0/-3.0	PLATED	2
.	121.0	+3.0/-3.0	PLATED	2
.	156.0	+3.0/-3.0	PLATED	6
.	250.0	+3.0/-3.0	PLATED	4
.	32.992	+2.0/-2.0	NON-PLATED	4
.	40.0	+2.0/-2.0	NON-PLATED	4
.	43.0	+2.0/-2.0	NON-PLATED	1
.	43.0	+2.0/-2.0	NON-PLATED	1
.	50.0	+2.0/-2.0	NON-PLATED	2
.	57.0	+2.0/-2.0	NON-PLATED	6
.	63.0	+2.0/-2.0	NON-PLATED	6
.	69.0	+3.0/-3.0	NON-PLATED	7
.	79.0	+2.0/-2.0	NON-PLATED	2
.	126.0	+2.0/-2.0	NON-PLATED	2
.	147.008	+2.0/-2.0	NON-PLATED	4
.	166.0	+3.0/-0.0	NON-PLATED	3
.	173.0	+2.0/-2.0	NON-PLATED	1
.	33.0x26.0	+3.0/-3.0	PLATED	2
.	59.0x33.0	+3.0/-3.0	PLATED	2
.	79.0x44.0	+3.0/-3.0	PLATED	2



DESIGN CROSS SECTION CHART  
TOTAL THICKNESS 120.24 MIL

REVISIONS			
VER	DESCRIPTION	DATE	APPROVED
A01	FIRST RELEASE	12/16/19	NH

- FABRICATE TO IPC-6012 CLASS 2,CURRENT REVISION.
- BOARD SHALL MEET THE INSPECTION CRITERIA OF IPC-A-600,CLASS 2,CURRENT REVISION.
- MATERIAL: ISPEED LOW DK VLP2 COPPER. SEE STACK UP FOR MORE INFO.
- WEIGHT OF ALL COPPER LAYERS SHALL NOT BE LESS 0.5 OZ. PER SQUARE FOOT.
- ZUM SMOOTHNESS IS REQUIRED FOR ALL VLP2 COPPER USED ON THE INTERNAL LAYERS.
- IMPEDANCE TOLERANCE +/- 10%
- SOLDERMASK BOTH SIDES USING TAIYO PSSR-LDI COLOR GREEN. FINISH - GOLD IMMERSION 2-10 MICRO INCHES OVER 200 MICRO INCHES MINIMUM OF NICKEL. SELECTIVE HARD GOLD PLATE 30 MICRO INCHES IN AREAS SHOWN FOR J128 and J129
- SILKSCREEN TOP SIDE/BOTH SIDES WITH NON-CONDUCTIVE EPOXY BASED INK. COLOR SHALL BE WHITE A CONTRASTING INK WITH RESPECT TO SOLDER MASK COLOR. DISTORTION OF SILKSCREEN IS ACCEPTABLE OVER TRACES. EPOXY INK ON PLATED LANDS IS NOT ACCEPTABLE.
- VENDOR LOGO AND DATE CODE TO BE MARKED FAR SIDE SILKSCREEN MAXIMUM HEIGHT .12 INCHES.
- 100% ELECTRICAL TEST REQUIRED FOR CONTINUITY. BOARD SHALL HAVE A UL RATING OF 94V-O. UL SYMBOL AND RATING SHALL BE MARKED FAR SIDE SILKSCREEN
- REMOVE ALL UNUSED PADS FROM INTERNAL LAYERS.
- SOLDER MASK REGISTRATION TO BE WITHIN DIAMETRICAL TRUE POSITION OF +/- 0.002 WITH APPLICABLE HOLE / PAD.
- 274X GERBERS/ODB+. USED FOR FAB MUST BE VERIFIED AGAINST THE PROVIDED IPC356 NETLIST. INTENTIONAL SHORTS LIST SUPPLIED.
- USE ARTMASTER # 12805023-01 REV-1.0 VERSION 6.0.
- THIEVING: DO NOT ADD COPPER THIEVING ON TOP LAYER IN THE FBGA AREA, NO THIEVING ALLOWED UNDER TEXT. THIEVING PATTERN IS TO BE 30 MILS SQUARE PADS, 50 MILS SPACING, MAINTAIN 150 MIL CLEARANCE TO COPPER FEATURES.
- ALL VIA-IN-PADS (5.0 THROUGH 12.0 DRILLS) TO BE COMPLETELY FILLED. PLANARIZED SMOOTH AND PLATED OVER ON SURFACE. USE SanEi NON-CONDUCTIVE EPOXY OR EQUIVALENT FILL MATERIALS MINIMUM OF .0007 TO BE PLATED ON SURFACE. VIA-IN-PAD MUST INCLUDE WRAP REQUIREMENTS PER IPC 6012B.
- DRILL SIZES LISTED IN LEGEND ARE CONSIDERED FINISHED.
- VENDOR IS REQUIRED TO SELECT TOOLING FOR OVERDRILLING.
- LEGEND DOES NOT SPECIFY DEPTH INTO ADJACENT DIELECTRIC LAYER.
- BAKE AT 225 DEGREES FOR 4 HOURS TO REMOVE ANY MOISTURE AFTER FABRICATION.
- THERE SHOULD BE NO OPEN NETS ON THIS DESIGN.

	50 OHM SE	100 OHM DIFF	88 OHM DIFF
TOP & BOTTOM	7.60 MILS	6.78 MILS / 15 MILS	
LAYER 2		5.8 MILS / 15 MILS	
LAYER 5	5.75 MILS	5.8 MILS / 15 MILS 8.0 MILS / 5.08 MILS	6.3 MILS / 6.2
LAYERS 3,7,16,18 & 20	5.75 MILS	5.625 MILS / 15 MILS	6.3 MILS / 6.2

#### LINE WIDTH and IMPEDANCE :

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE	XILINX® 2100 LOGIC DR. SAN JOSE, CA 95124 HWCP - HARDWARE & CONFIGURATION PLATFORMS		
DIMENSIONS ARE IN INCHES TOLERANCES ON: 2 PL DECIMALS +/- .010 3 PL DECIMALS +/- .005 ANGLES + FRACTIONS +	DRAWN CHECKED ENGRC ISSUED	12/12/19	FABRICATION DRAWING PCB, ROHS COMPLIANT HW_Z1_ZCU208		
			SIZE D	FSCM NO	DWG NO 128-05023-01
			SCALE NONE		REV A01 Version aa
					SHEET 1 OF 1