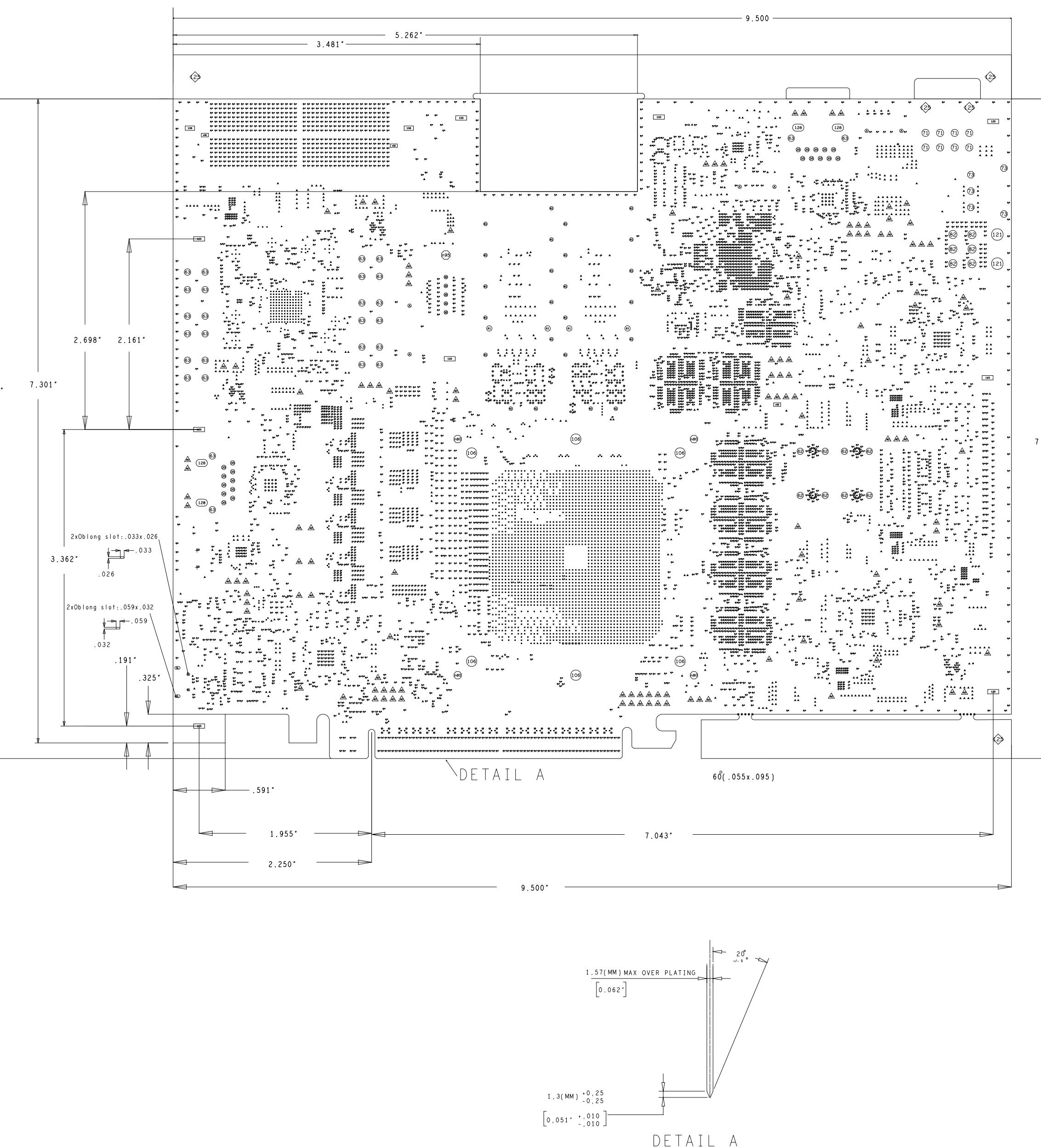


- FABRICATE TO IPC-6012 CLASS 2, CURRENT REVISION.
- BOARD SHALL MEET THE INSPECTION CRITERIA OF IPC-A-600, CLASS 2, CURRENT REVISION.
- MATERIAL: SEE STACK UP FOR MORE INFO.
- WEIGHT OF ALL COPPER LAYERS SHALL NOT BE LESS THAN 0.5 OZ. PER SQUARE FOOT.
- SOLDERMASK BOTH SIDES, USING TAIYO PSSR-LDI COLOR GREEN.
- FINISH - PLATE SELECTIVE HARD GOLD FLASH OF 2-10 MICRO INCHES OVER BOTH SURFACES OF FAB WITH OVER 200 MICRO INCHES MINIMUM OF NICKEL. SELECTIVE HARD GOLD PLATE 30 MICRO INCHES IN THE PADS FOR U1.
- SILKSCREEN TOP SIDE/BOTH SIDES WITH NON-CONDUCTIVE EPOXY BASED INK. COLOR SHALL BE WHITE A CONTRASTING INK WITH RESPECT TO SOLDER MASK COLOR. DISTORTION OF SILKSCREEN IS ACCEPTABLE OVER TRACES. EPOXY INK ON PLATED LANDS IS NOT ACCEPTABLE.
- VENDOR LOGO AND DATE CODE TO BE MARKED FAR SIDE MAXIMUM HEIGHT .12 INCHES.
- 100% ELECTRICAL TEST REQUIRED FOR CONTINUITY. BOARD SHALL HAVE A UL RATING OF 94V-0. UL SYMBOL AND RATING SHALL BE MARKED FAR SIDE.
- REMOVE ALL UNUSED PADS FROM INTERNAL LAYERS.
- PRE-SOLDERMASK OPERATION: ALL VIAS ON SECONDARY SIDE (BOT) ENCROACHED AND PLUGGED FROM BGA ATTACHMENT SIDE (DEFAULT TOP). ENSURE THESE VIAS ARE PLUGGED LEAVING NO ASSOCIATED METAL EXPOSED.
- SOLDER MASK REGISTRATION TO BE WITHIN DIAMETRICAL TRUE POSITION OF + / - 0.002" WITH APPLICABLE HOLE / PAD.
- 274X GERBERS/ODB++ USED FOR FAB MUST BE VERIFIED AGAINST THE PROVIDED IPC356 NETLIST.

22. INTENTIONAL SHORTS:
PLEASE REFER TO INTENTIONAL SHORTS LIST PROVIDED.
REPORT ANY OTHER SHORTS OR OPENS NOT ON THIS LIST.

- USE ARTMASTER # 128-05072-01-REV_B01.
- THIEVING: DO NOT ADD COPPER THIEVING ON TOP LAYER IN THE FBGA AREA. NO THIEVING ALLOWED UNDER TEXT. THIEVING PATTERN IS TO BE 30 MILS SQUARE PADS, 50 MILS SPACING. THIEVING TO BE ADDED ON INTERNAL LAYERS TO ACHIEVE BALANCED COPPER DENSITY, MAINTAIN 150 MIL CLEARENCE TO COPPER FEATURES.
- ALL VIA-IN-PADS (12.0 AND UNDER DRILLS) TO BE COMPLETELY FILLED. PLANARIZED SMOOTH AND PLATED OVER ON SURFACE. USE Sanei NON-CONDUCTIVE EPOXY OR EQUIVALENT FILL MATERIALS MINIMUM OF .0007 TO BE PLATED ON SURFACE. VIA-IN-PAD MUST INCLUDE WRAP REQUIREMENTS PER IPC 6012B.
- DRILL SIZES LISTED IN LEGEND ARE CONSIDERED FINISHED.
- VENDOR IS REQUIRED TO SELECT TOOLING FOR OVERRILLING.
- LEGEND DOES NOT SPECIFY DEPTH INTO ADJACENT DIELECTRIC LAYER.
- BAKE AT 225 DEGREES FOR 4 HOURS TO REMOVE ANY MOISTURE AFTER FABRICATION.
- HARD GOLD ON FINGERS , 30-50 MICRO INCHES OF GOLD OVER 150-200 MICRO INCHES OF NICKEL MINIMUM.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A01	PROTOTYPE	01/19/21	
B01	MISC UPDATES	08/26/21	



LAYER	IMPEDANCES	DIFF LINE WIDTH	DIFF LINE SPACE
L3,L5,L7,L12,L14,L16	76 OHM	4.15 MILS	5.85 MILS
L3,L5,L7,L12,L14,L16	82 OHM	3.4 MILS	3.4 MILS
L3,L5,L7,L12,L14,L16	85 OHM	3.4 MILS	4.6 MILS
L3,L5,L7,L12,L14,L16	100 OHM	3.0 MILS	4.0 MILS

LAYERS	SINGLE ENDED			DIFFERENTIAL PAIRS									
	40 OHM LINE WIDTH	45 OHM LINE WIDTH	50 OHM LINE WIDTH	76 OHM LINE WIDTH	82 OHM LINE WIDTH	85 OHM LINE WIDTH	90 OHM LINE WIDTH	100 OHM LINE WIDTH	SPACE				
L1	8.0 MILS	6.4 MILS	5.1 MILS	6.8 MILS	5.7 MILS	5.2 MILS	4.8 MILS	5.0 MILS	5.2 MILS	4.5 MILS	5.5 MILS	3.9 MILS	7.1 MILS
L3	4.5 MILS	3.6 MILS	3.0 MILS	4.8 MILS	7.7 MILS	4.15 MILS	5.85 MILS	3.9 MILS	6.1 MILS	3.5 MILS	6.5 MILS	3.0 MILS	9.0 MILS
L5	4.5 MILS	3.6 MILS	3.0 MILS	4.8 MILS	7.7 MILS	4.15 MILS	5.85 MILS	3.9 MILS	6.1 MILS	3.5 MILS	6.5 MILS	3.0 MILS	9.0 MILS
L7	4.5 MILS	3.6 MILS	3.0 MILS	4.8 MILS	7.7 MILS	4.15 MILS	5.85 MILS	3.9 MILS	6.1 MILS	3.5 MILS	6.5 MILS	3.0 MILS	9.0 MILS
L12	4.5 MILS	3.6 MILS	3.0 MILS	4.8 MILS	7.7 MILS	4.15 MILS	5.85 MILS	3.9 MILS	6.1 MILS	3.5 MILS	6.5 MILS	3.0 MILS	9.0 MILS
L14	4.5 MILS	3.6 MILS	3.0 MILS	4.8 MILS	7.7 MILS	4.15 MILS	5.85 MILS	3.9 MILS	6.1 MILS	3.5 MILS	6.5 MILS	3.0 MILS	9.0 MILS
L15	4.5 MILS	3.6 MILS	3.0 MILS	4.8 MILS	7.7 MILS	4.15 MILS	5.85 MILS	3.9 MILS	6.1 MILS	3.5 MILS	6.5 MILS	3.0 MILS	9.0 MILS
L16	4.5 MILS	3.6 MILS	3.0 MILS	4.8 MILS	7.7 MILS	4.15 MILS	5.85 MILS	3.9 MILS	6.1 MILS	3.5 MILS	6.5 MILS	3.0 MILS	9.0 MILS
L17	4.5 MILS	3.6 MILS	3.0 MILS	4.8 MILS	7.7 MILS	4.15 MILS	5.85 MILS	3.9 MILS	6.1 MILS	3.5 MILS	6.5 MILS	3.0 MILS	9.0 MILS
L18	8.0 MILS	6.4 MILS	5.1 MILS	6.8 MILS	5.7 MILS	5.2 MILS	4.8 MILS	5.0 MILS	5.2 MILS	4.5 MILS	5.5 MILS	3.0 MILS	9.0 MILS

LINE WIDTH IMPEDANCE CHART FOR REFERENCE

DRILL CHART: TOP to L3_SIG1						
ALL UNITS ARE IN MILS						
FIGURE	FINISHED_SIZE	TOOL_SIZE	TOLERANCE_DRILL	TOLERANCE_TRAVEL	PLATED	NONSTANDARD
.	8.0		+2.0/-2.0	-	PLATED	LASER
.	9.8		+2.0/-2.0	-	PLATED	LASER

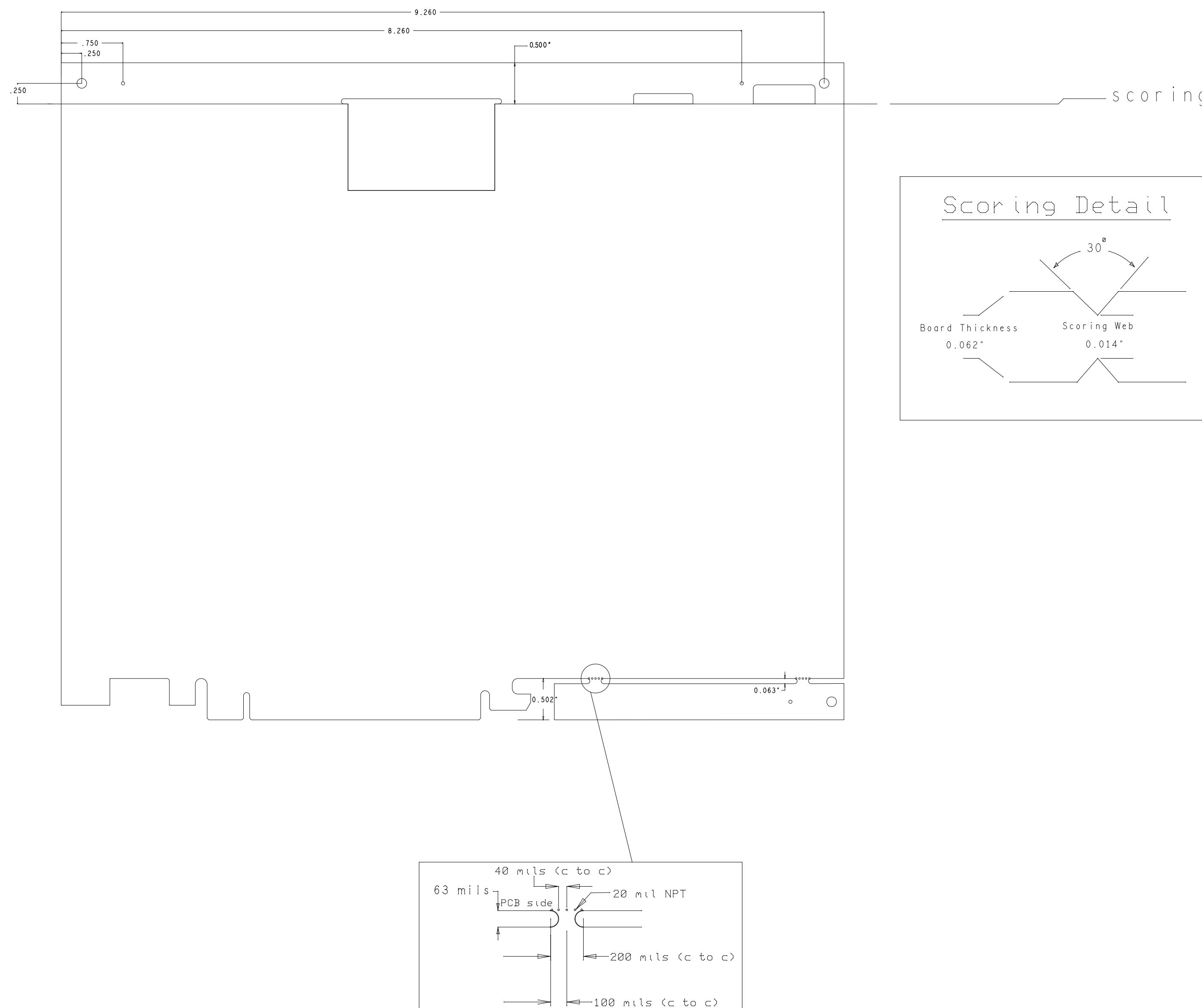
DRILL CHART: TOP to L2_GND1						
ALL UNITS ARE IN MILS						
FIGURE	FINISHED_SIZE	TOOL_SIZE	TOLERANCE_DRILL	TOLERANCE_TRAVEL	PLATED	NONSTANDARD
.	5.0		+2.0/-2.0	-	PLATED	LASER
.	8.0		+2.0/-2.0	-	PLATED	LASER

DRILL CHART: TOP to BOTTOM						
ALL UNITS ARE IN MILS						
FIGURE	FINISHED_SIZE	TOOL_SIZE	TOLERANCE_DRILL	TOLERANCE_TRAVEL	PLATED	NONSTANDARD
.	7.8	7.8	+2.0/-2.0	-	PLATED	-
.	8.0		+2.0/-2.0	-	PLATED	-
.	9.8		+2.0/-2.0	-	PLATED	-
.	10.0		+2.0/-2.0	-	PLATED	-
.	11.81		+2.0/-2.0	-	PLATED	-
.	12.0		+2.0/-2.0	-	PLATED	-
.	32.0		+3.0/-3.0	-	PLATED	-
.	35.0		+3.0/-3.0	-	PLATED	-
.	40.0		+3.0/-3.0	-	PLATED	-
.	41.339		+2.0/-2.0	-	PLATED	-
.	61.024		+3.0/-3.0	-	PLATED	-
.	62.0		+3.0/-3.0	-	PLATED	-
.	63.0		+3.0/-3.0	-	PLATED	-
.	71.0		+2.0/-2.0	-	PLATED	-
.	73.0		+3.0/-3.0	-	PLATED	-
.	82.0		+3.0/-3.0	-	PLATED	-
.	106.0		+3.0/-3.0	-	PLATED	-
.	121.0		+3.0/-3.0	-	PLATED	-
.	125.0		+3.0/-3.0	-	PLATED	-
.	20.0		+2.0/-2.0	-	NON-PLATED	-
.	39.3701		+2.0/-2.0	-	NON-PLATED	-
.	50.0		+2.0/-2.0	-	NON-PLATED	-
.	59.055		+2.0/-2.0	-	NON-PLATED	-
.	80.0		+2.0/-2.0	-	NON-PLATED	-
.	95.0		+2.0/-2.0	-	NON-PLATED	-
.	106.0		+3.0/-3.0	-	NON-PLATED	-
.	118.0		+2.0/-2.0	-	NON-PLATED	-
.	127.9528		+2.0/-2.0	-	NON-PLATED	-
.	33.0x26.0		+5.0/-5.0	+5.0/-5.0	PLATED	-
.	59.0x32.0		+5.0/-5.0	+5.0/-5.0	PLATED	-

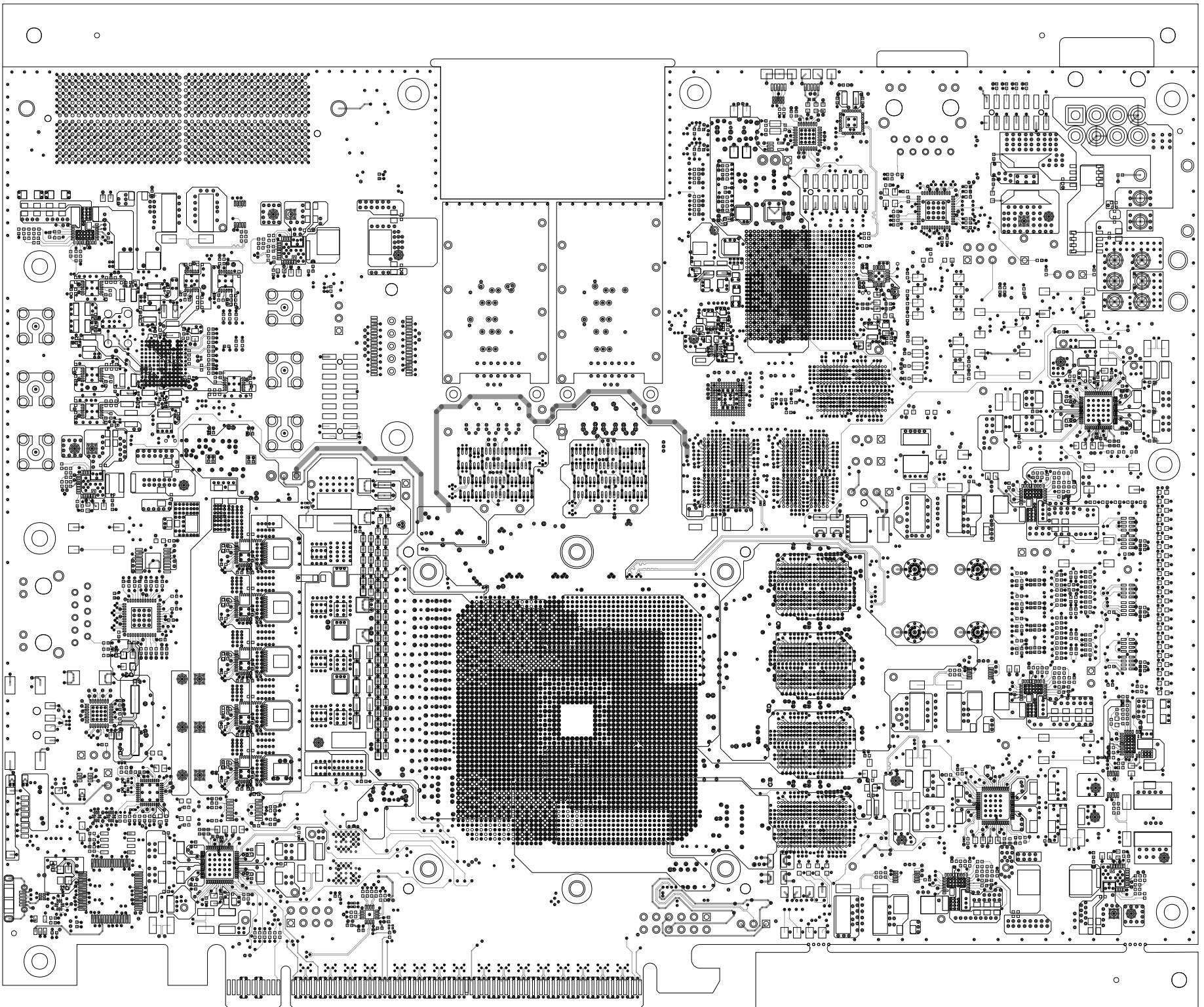
***. 41.339 HOLES ARE FOR PRESSFIT PINS.

SEE SEPARATE BACKDRILL PAGE FOR BACK DRILL DETAIL.

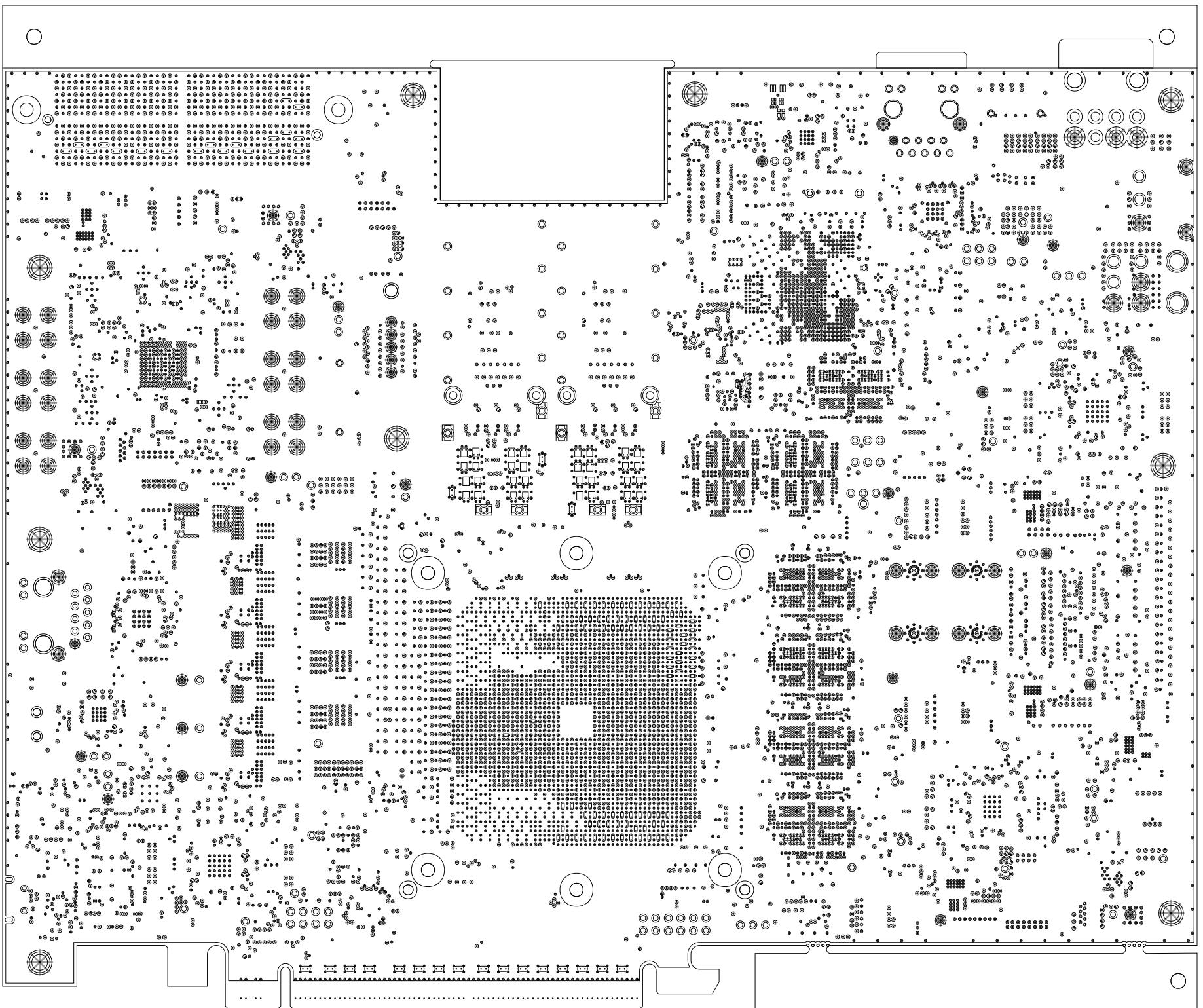
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A01	PROTOTYPE	01/19/21	
B01	MISC UPDATES	08/26/21	



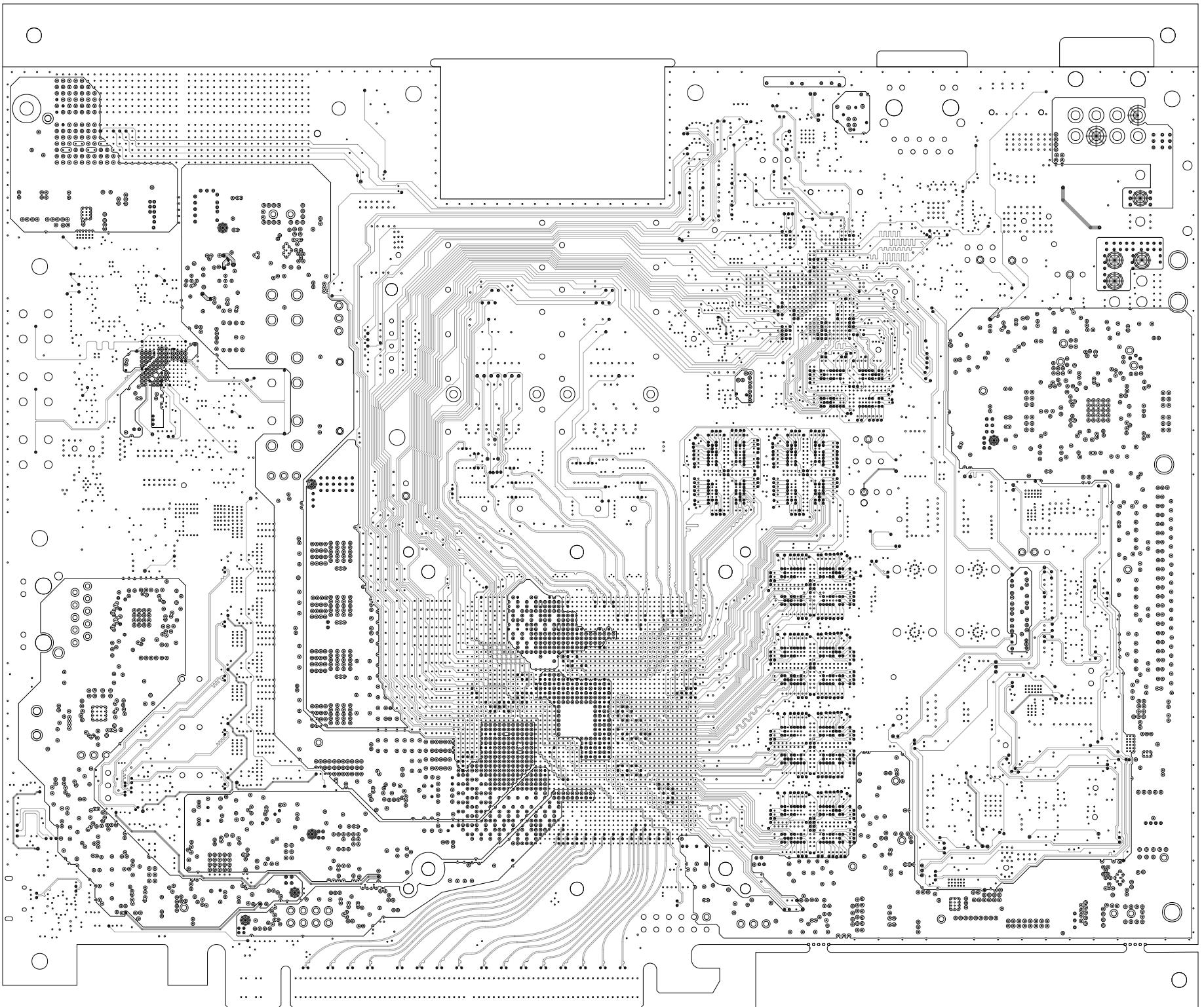
UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE	XILINX® 2100 LOGIC DR. SAN JOSE, CA 95124 FABRICATION DRAWING PCB, ROHS COMPLIANT VPK120			
DIMENSIONS ARE IN INCHES	DRAWN FAWAD MUNAWAR	01/19/21				
TOLERANCES ON: +/- .005	CHECKED					
ANGLES + FRACTIONS +	ENGRG BRIAN	01/19/21				
	ISSUED					
SIZE	FSCM NO	DWG NO	128-05072-01 B01 b a			
D						
SCALE	NONE		SHEET 2 of 2			



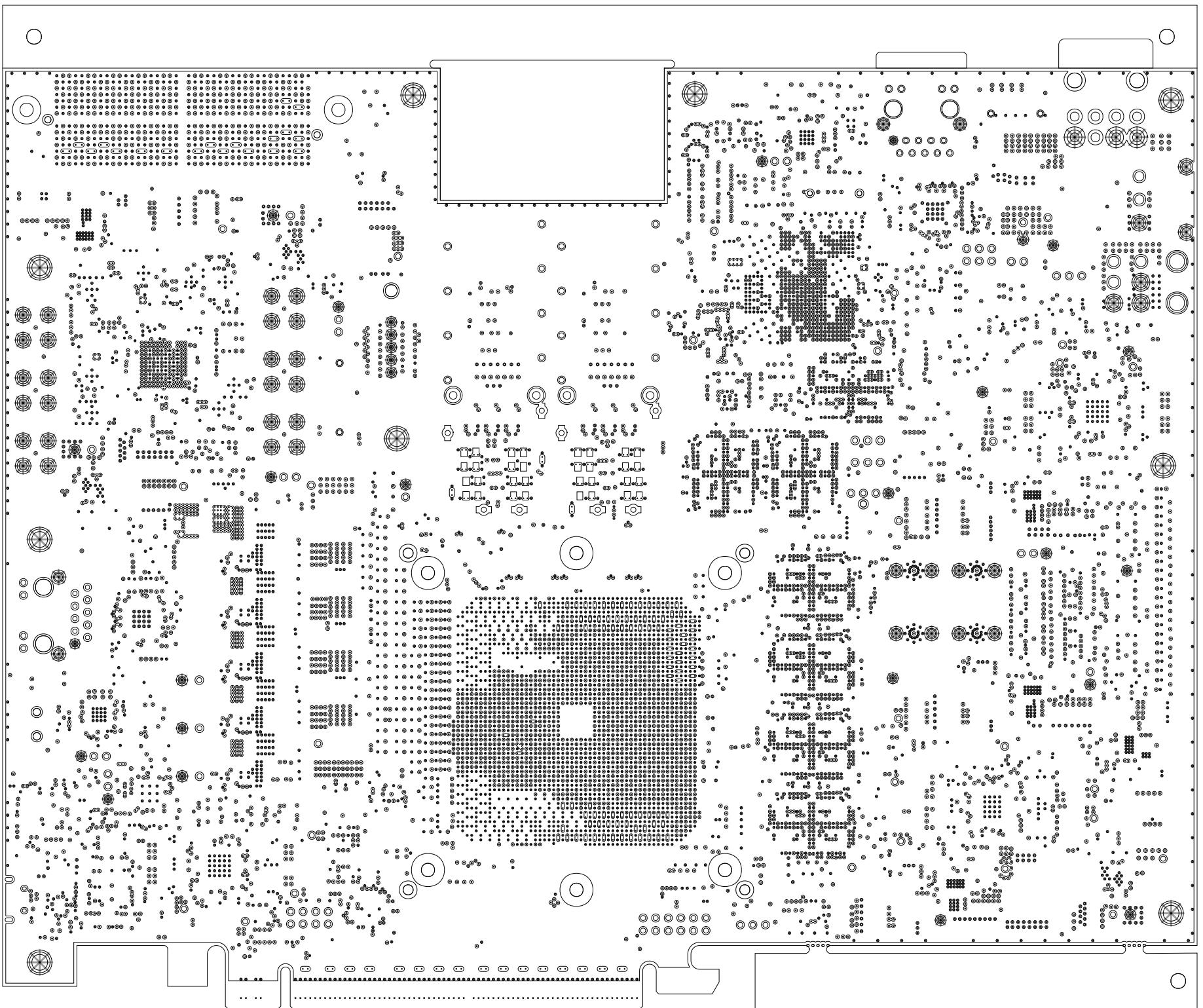
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PCB # 128-05072-01	
Designed by Xilinx	DATE: 08/26/2021
SCHEM: BRIAN; LAYOUT:CAROL	PHONE: 720-652-3759
LAYER: L01_TOP	XILINX DOC USE ONLY REVISION:B01



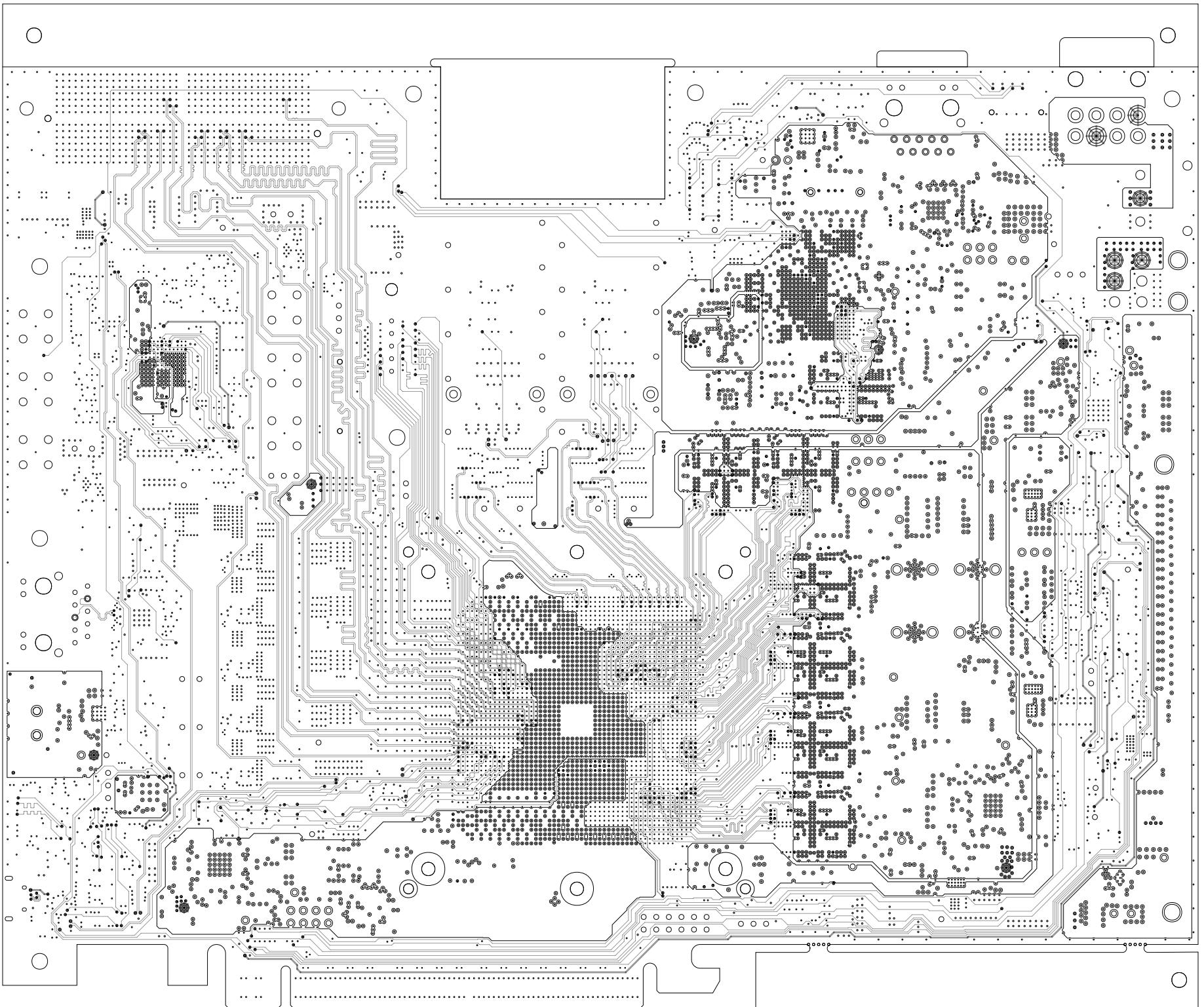
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Designed by Xilinx	DATE: 08/26/2021
SCHEM: BRIAN; LAYOUT:CAROL	PHONE: 720-652-3759
LAYER: L02_GND1	XILINX DOC USE ONLY REVISION:B01



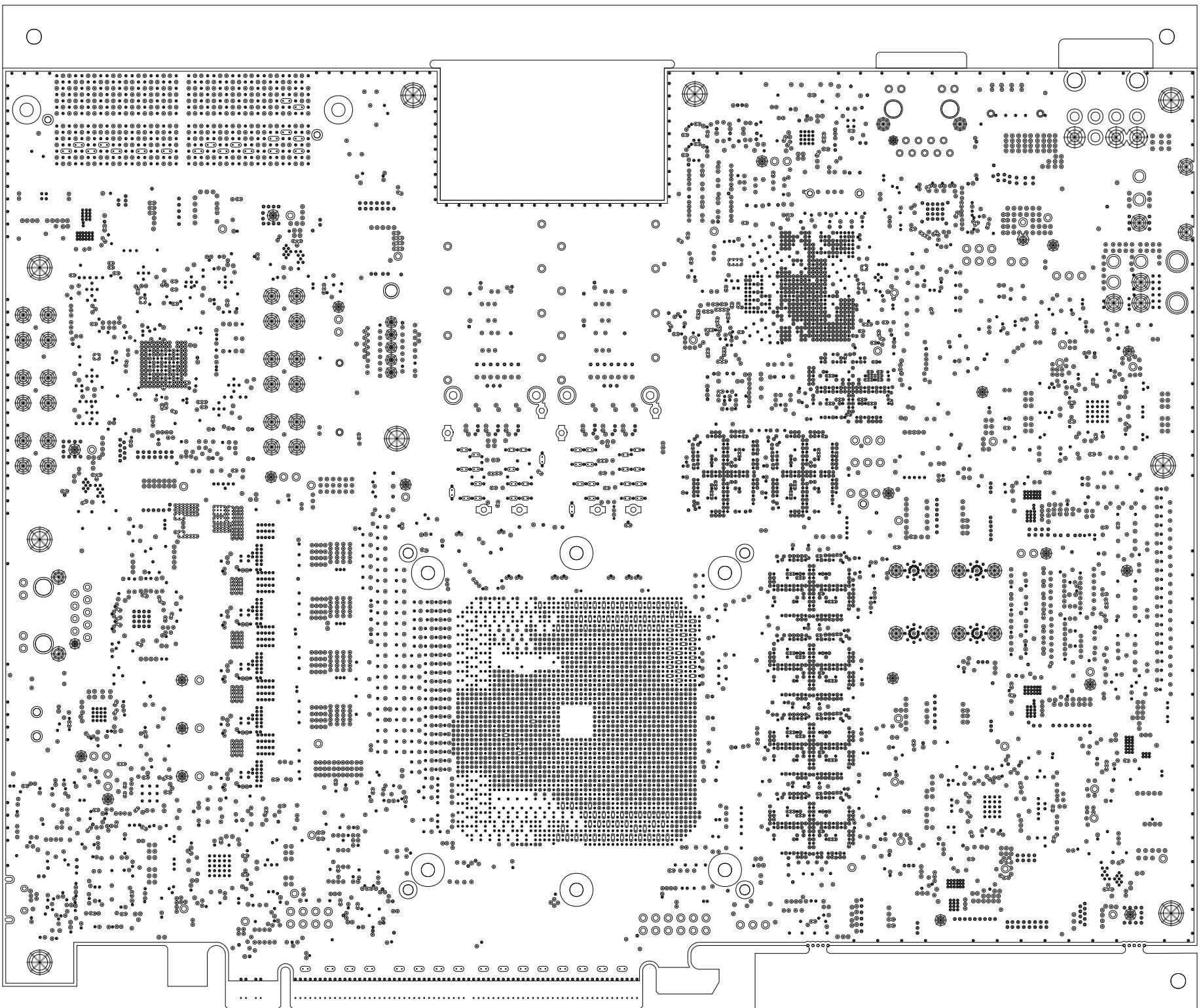
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LAYER: L03_SIG1	XILINX DOC USE ONLY REVISION:B01



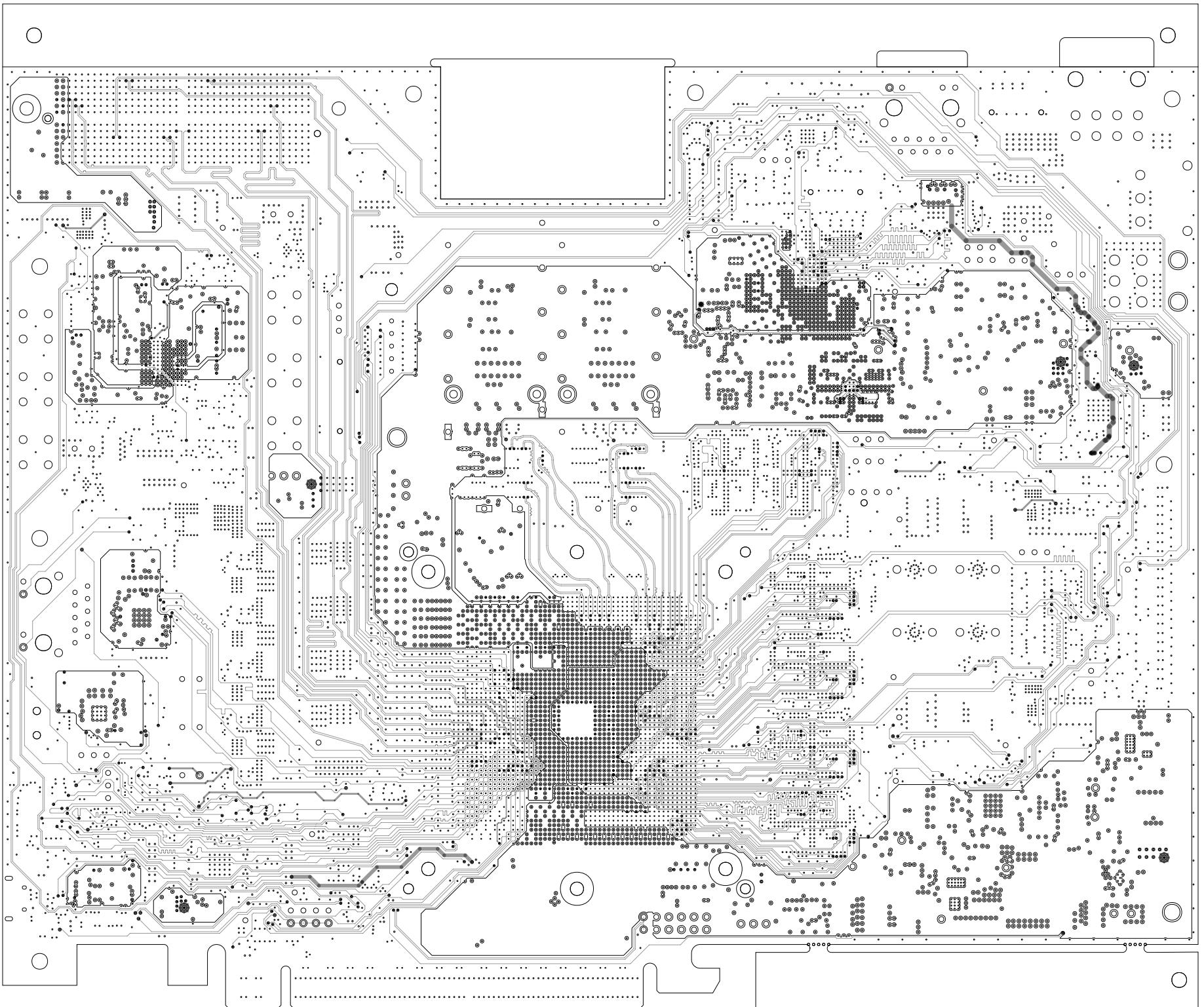
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LAYER: L04_GND2	XILINX DOC USE ONLY REVISION:B01



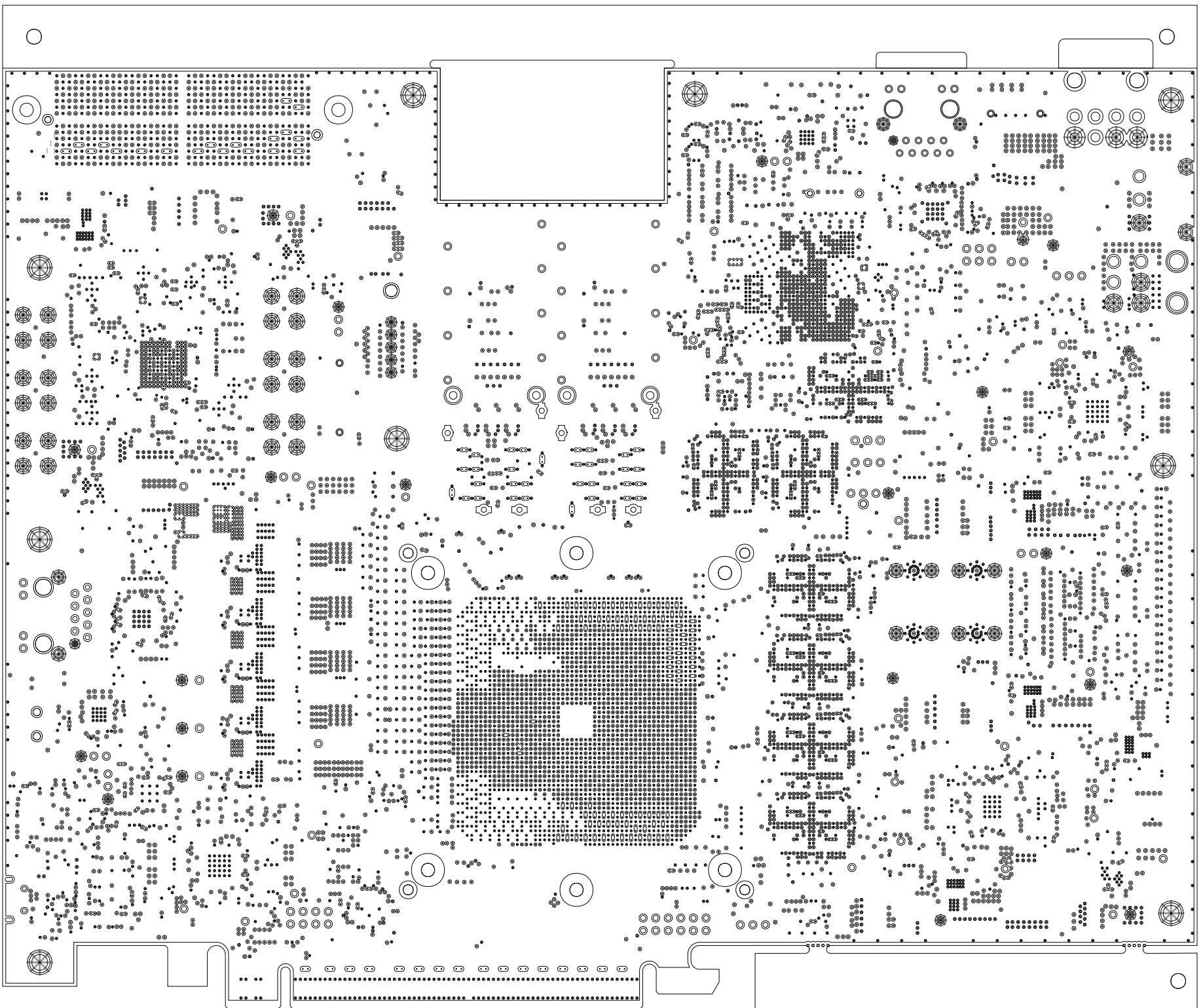
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LAYER: L05_SIG2	XILINX DOC USE ONLY REVISION:B01



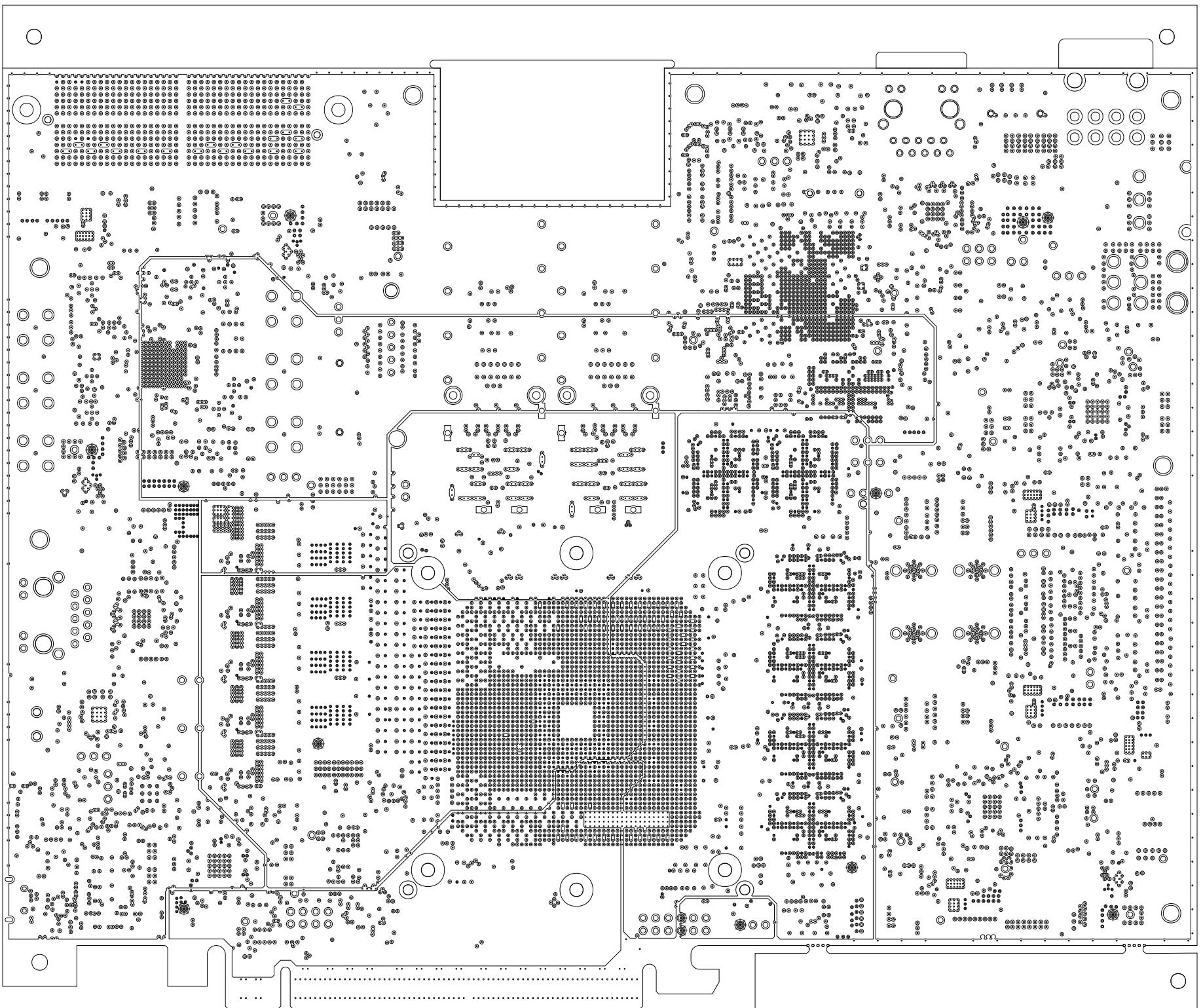
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PCB # 128-05072-01	
Designed by Xilinx	DATE: 08/26/2021
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LAYER: L06_GND3	XILINX DOC USE ONLY REVISION:B01



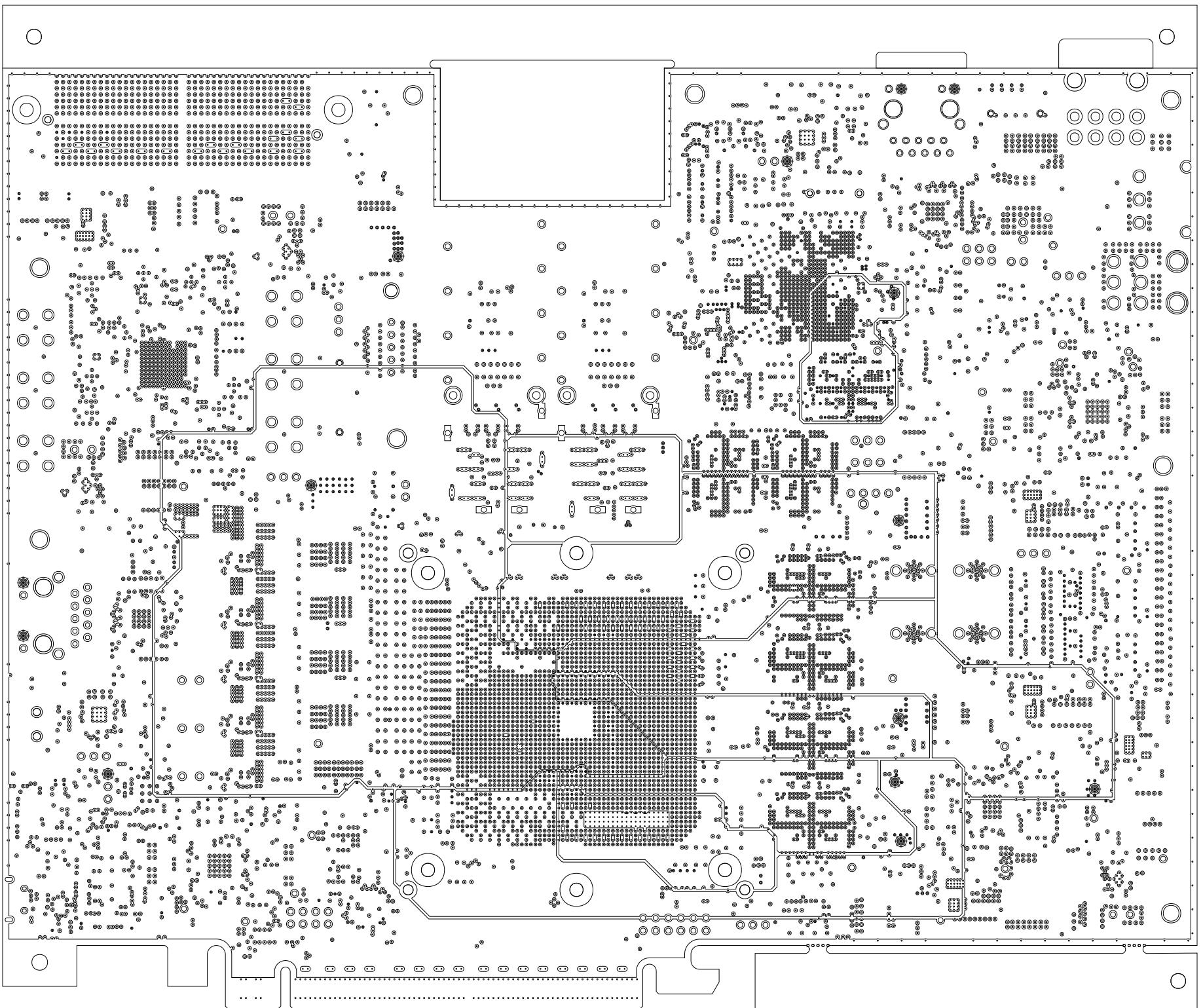
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LAYER: L07_SIG3	XILINX DOC USE ONLY REVISION:B01



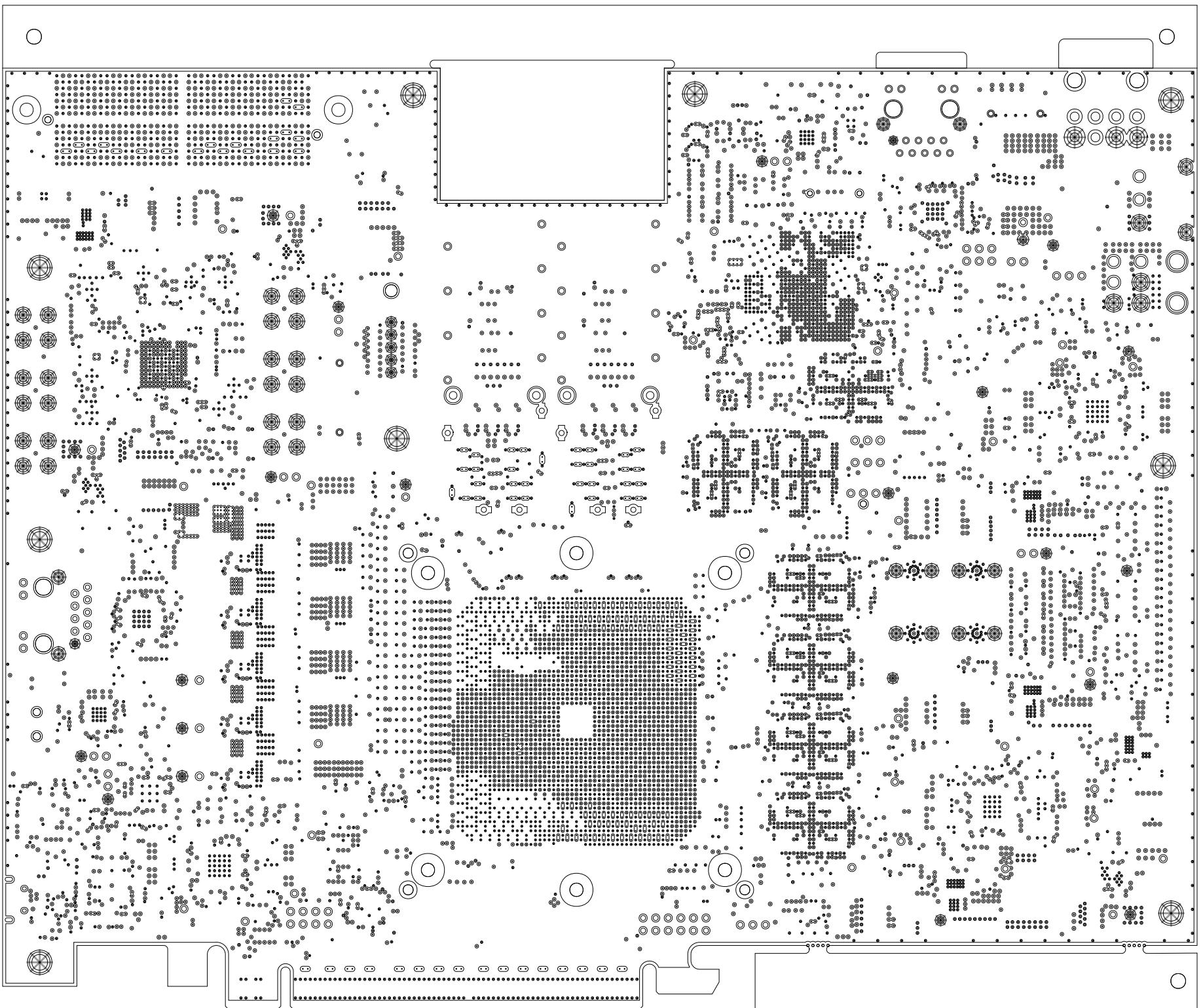
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LAYER: L08_GND4	XILINX DOC USE ONLY REVISION:B01



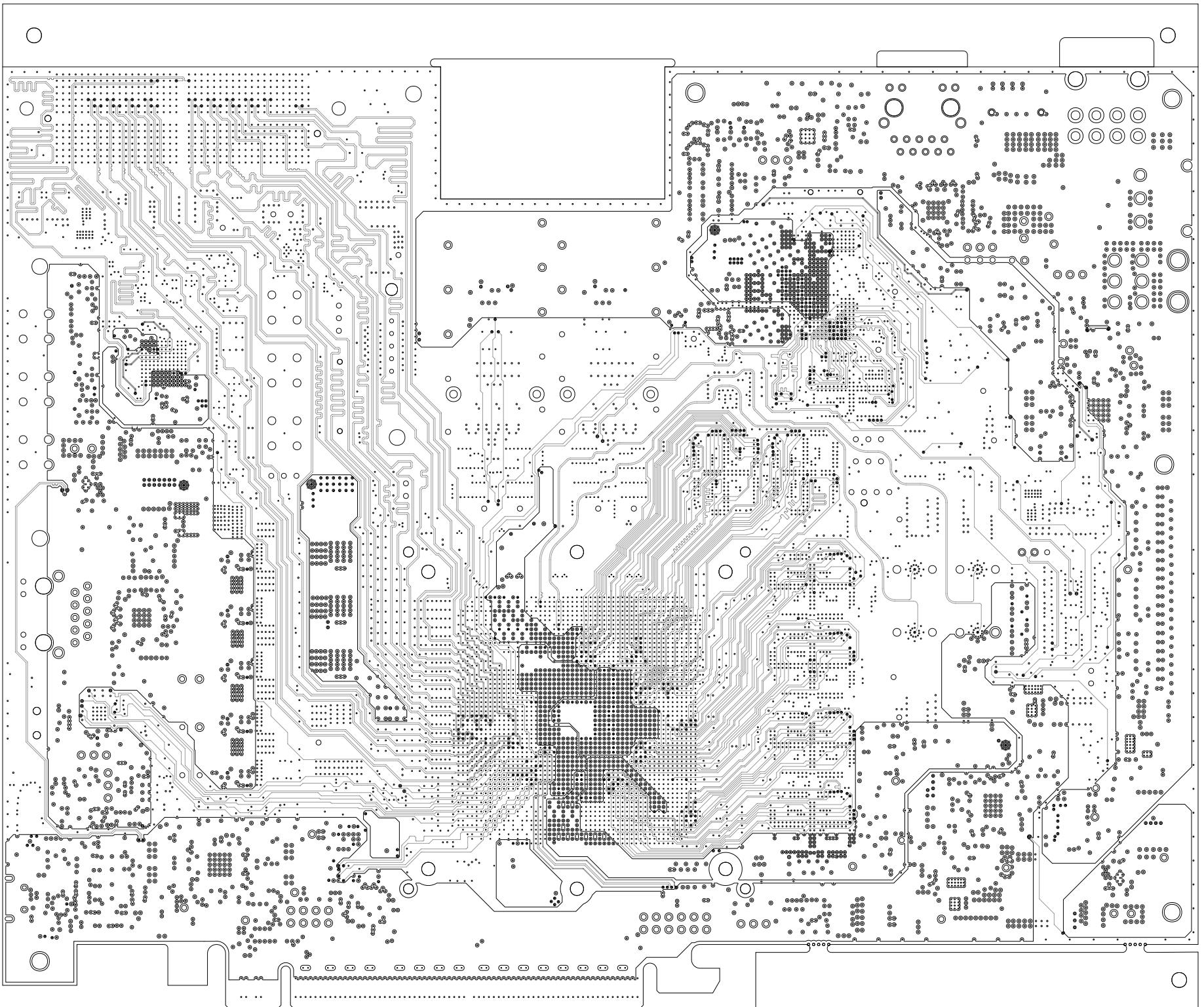
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LAYER: L09_PWR1	XILINX DOC USE ONLY REVISION:B01



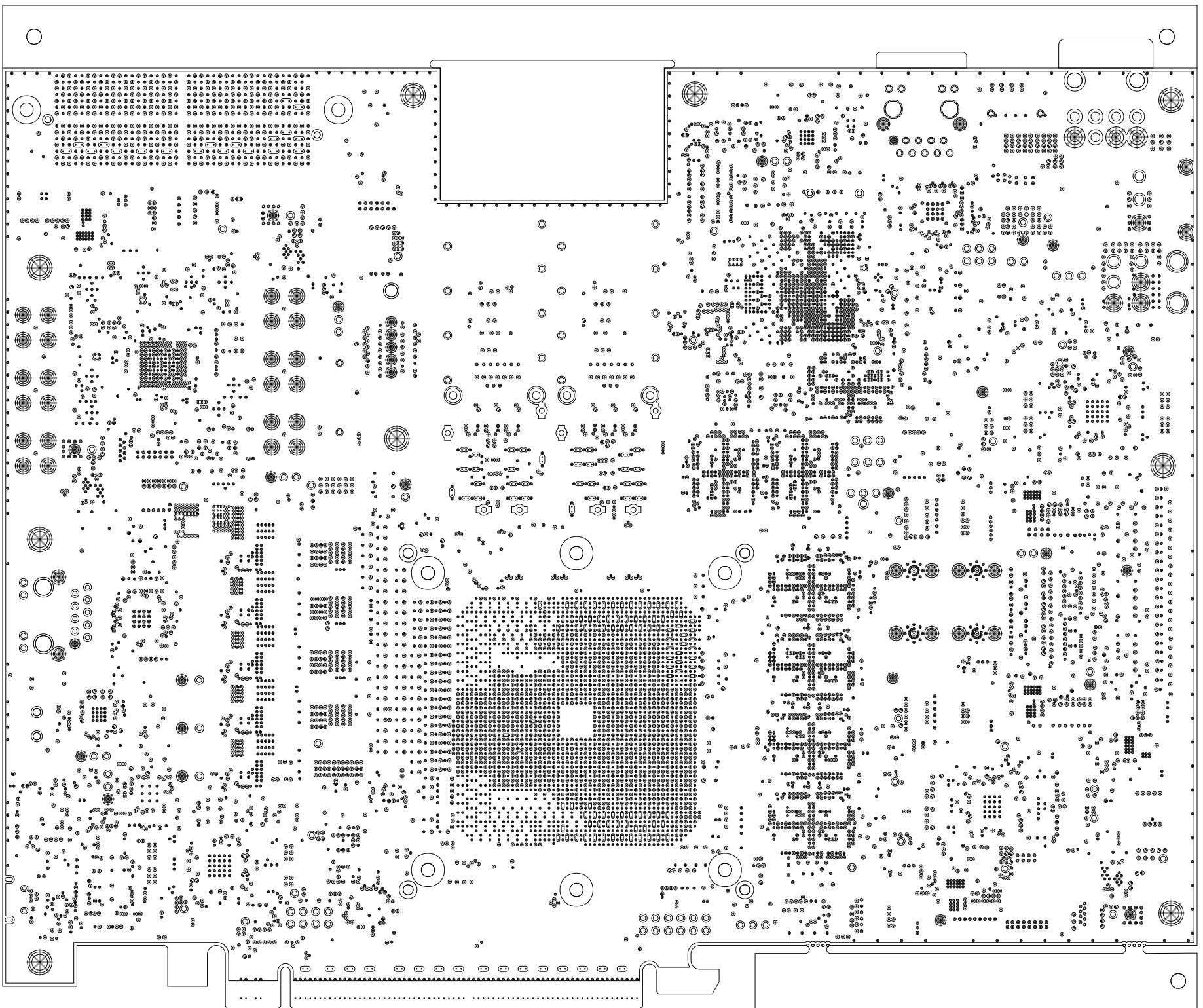
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LAYER: L10_PWR2	XILINX DOC USE ONLY REVISION:B01



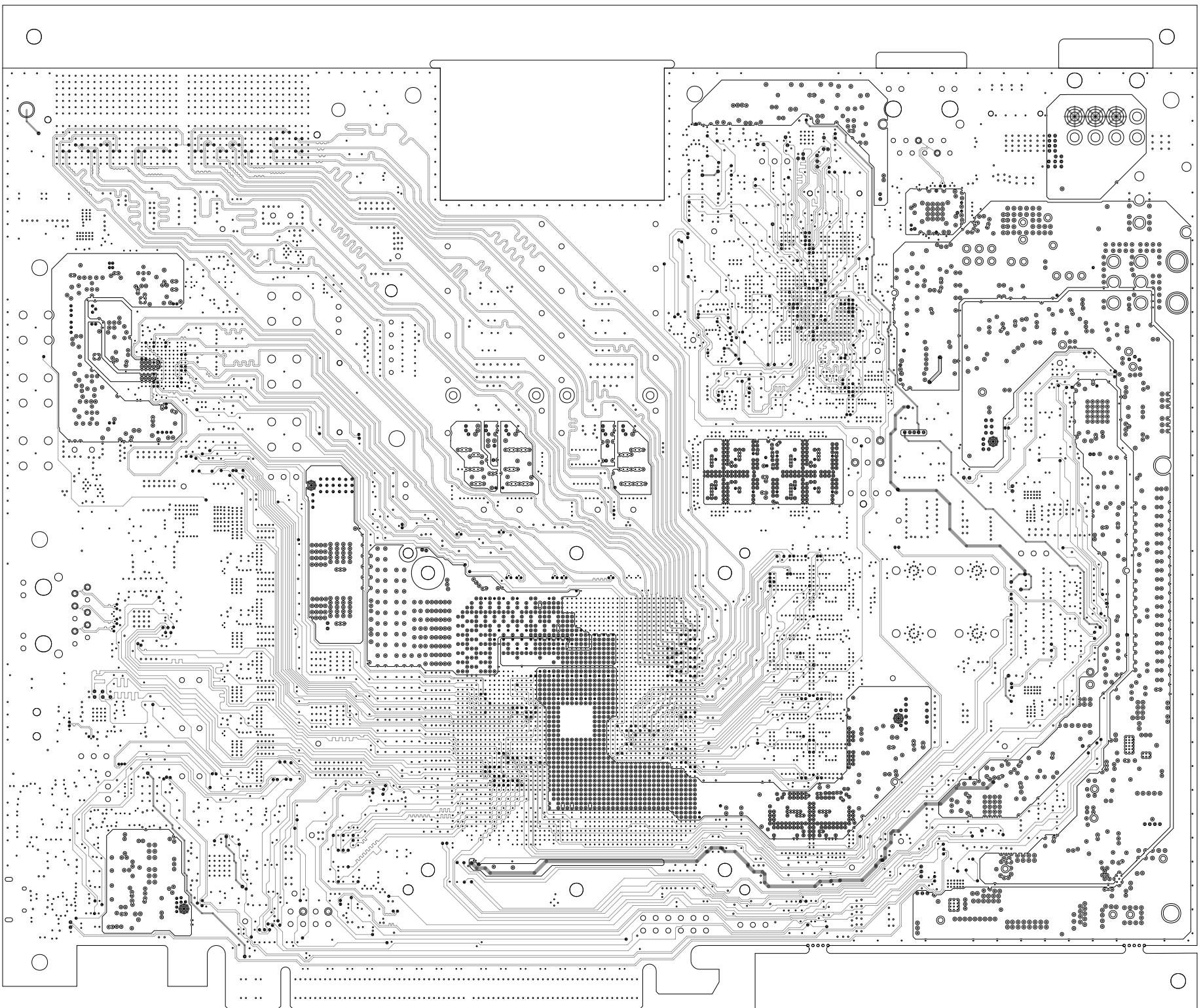
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Designed by Xilinx	DATE: 08/26/2021
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LAYER: L11_GND5	XILINX DOC USE ONLY REVISION:B01



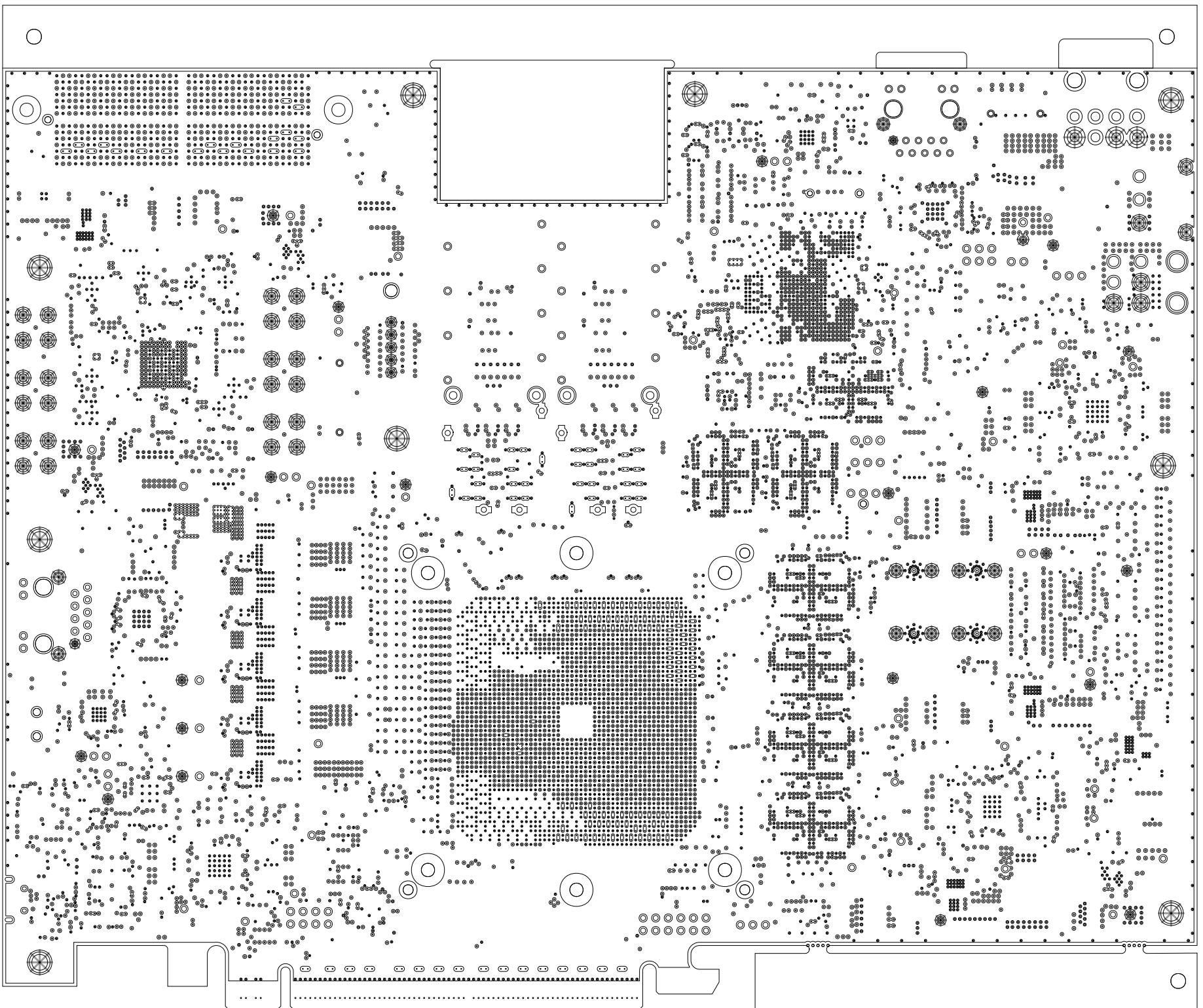
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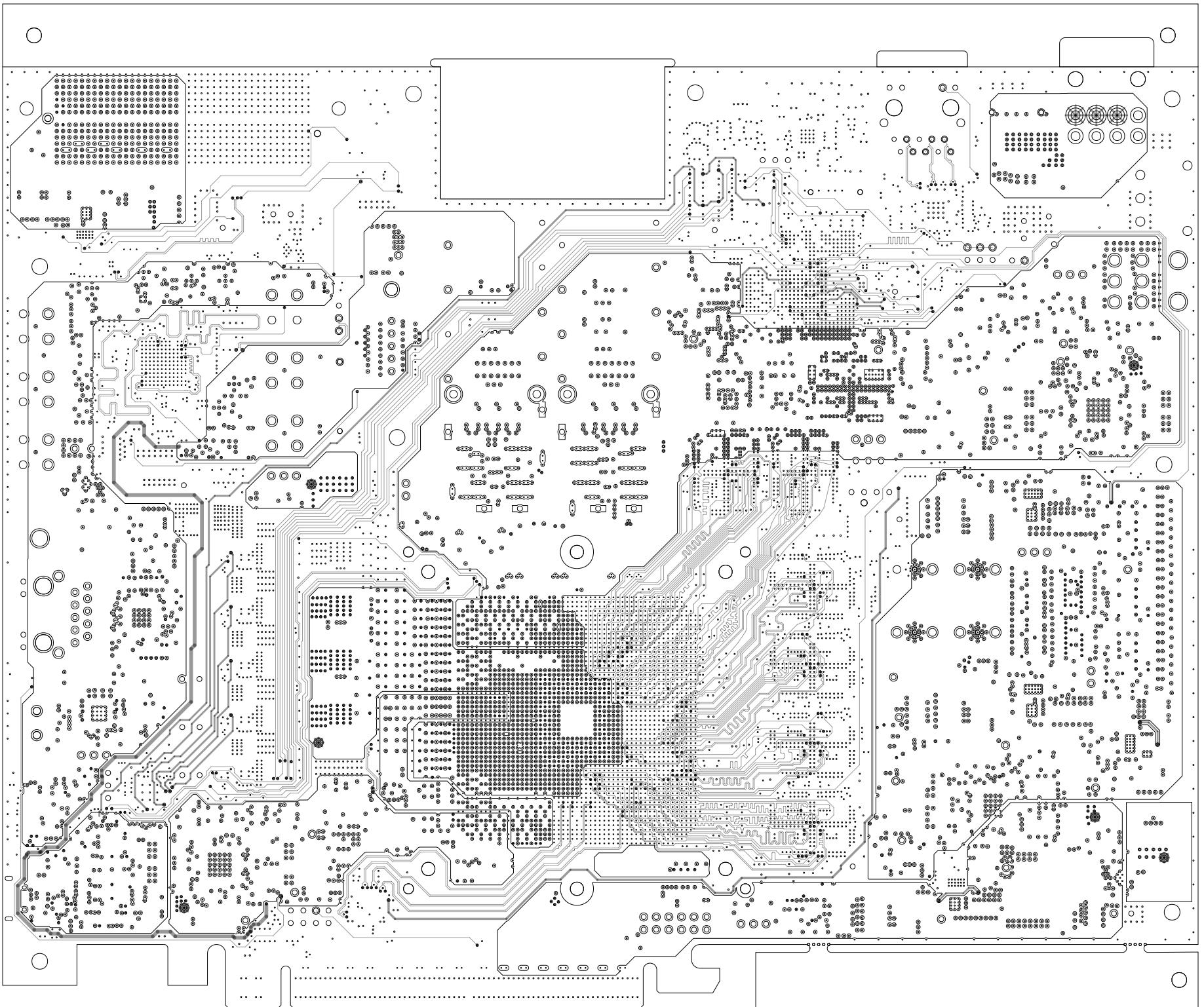
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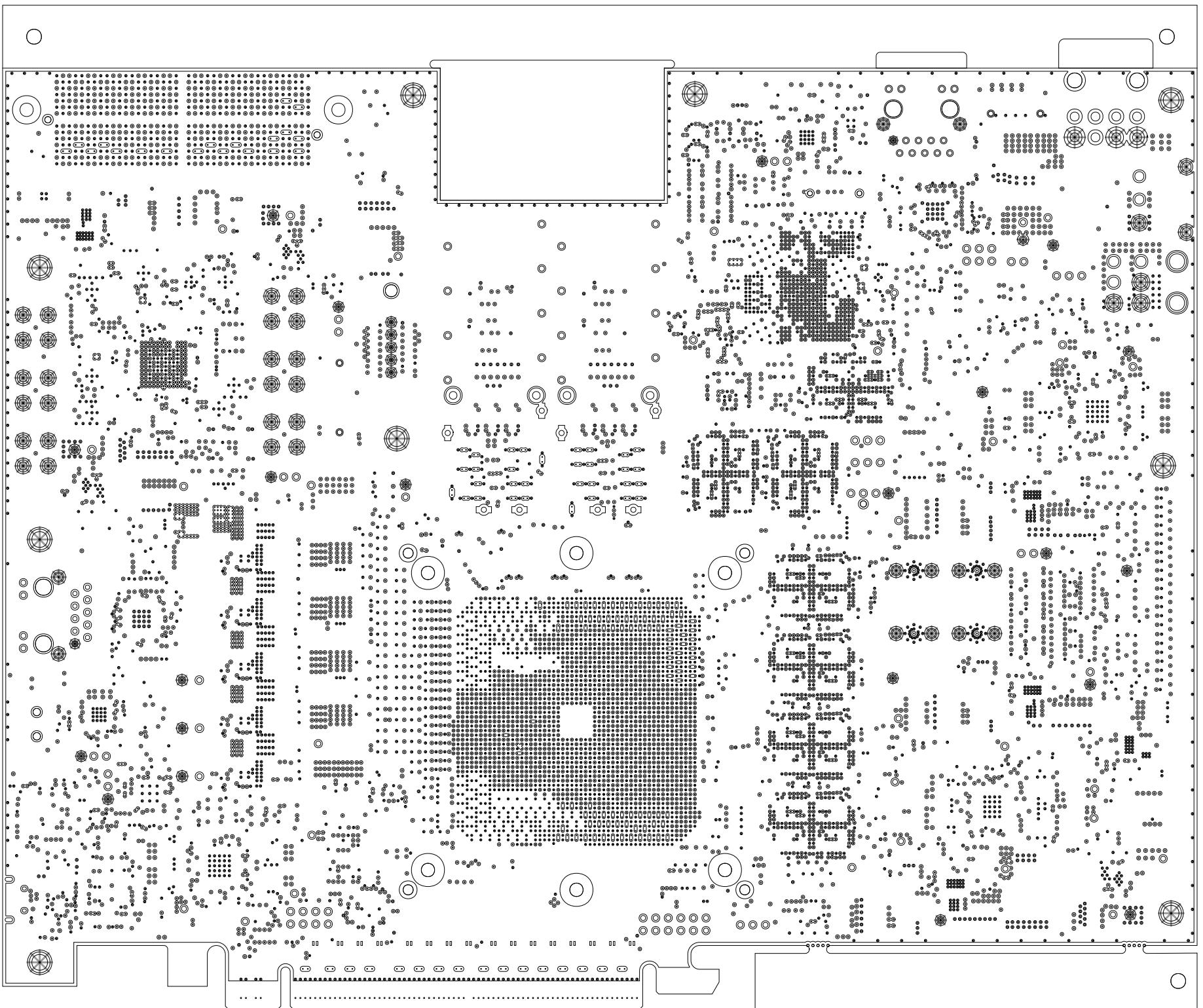
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LAYER: L14_SIG5	XILINX DOC USE ONLY REVISION:B01



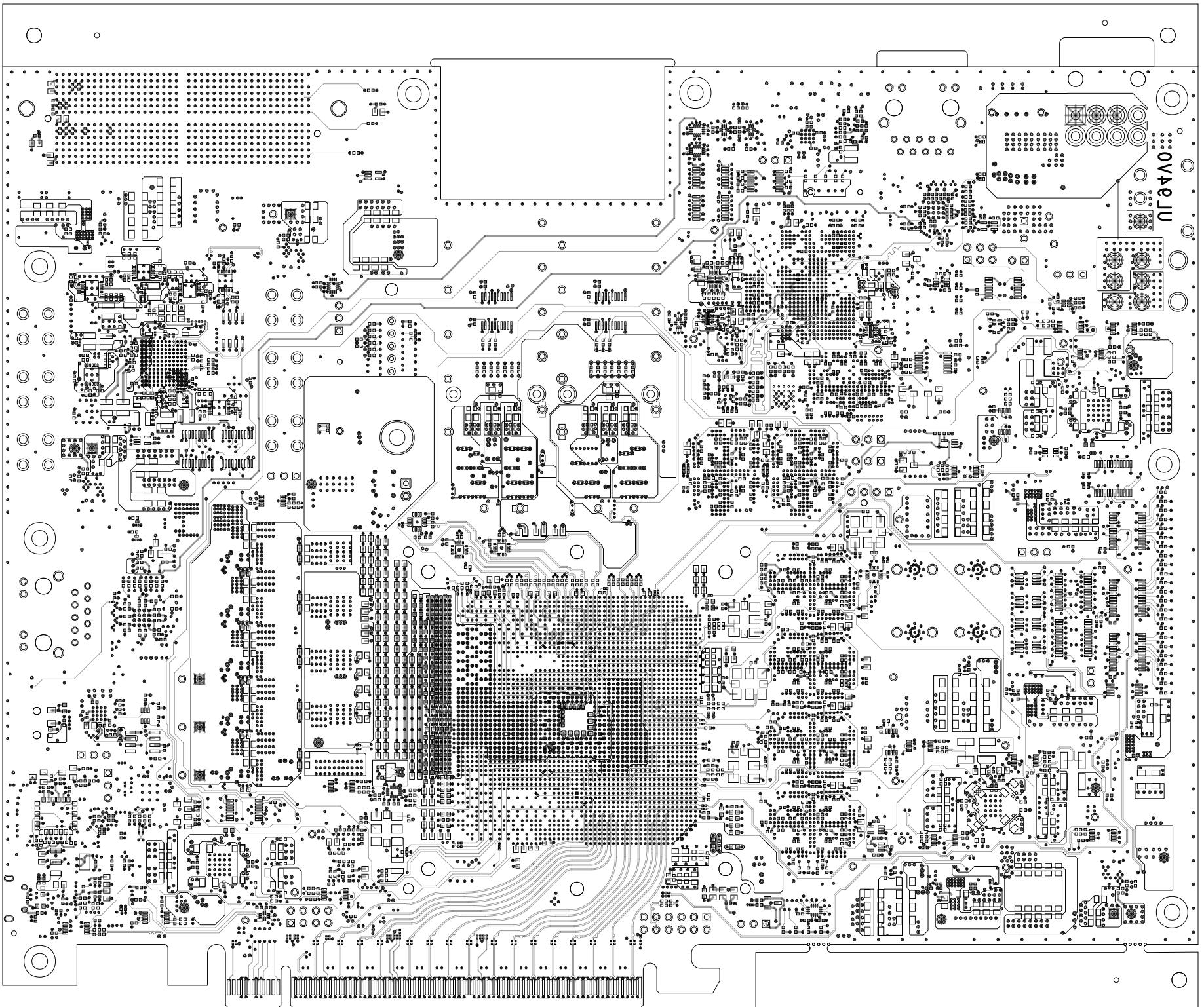
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Designed by Xilinx	DATE: 08/26/2021
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LAYER: L15_GND7	XILINX DOC USE ONLY REVISION:B01



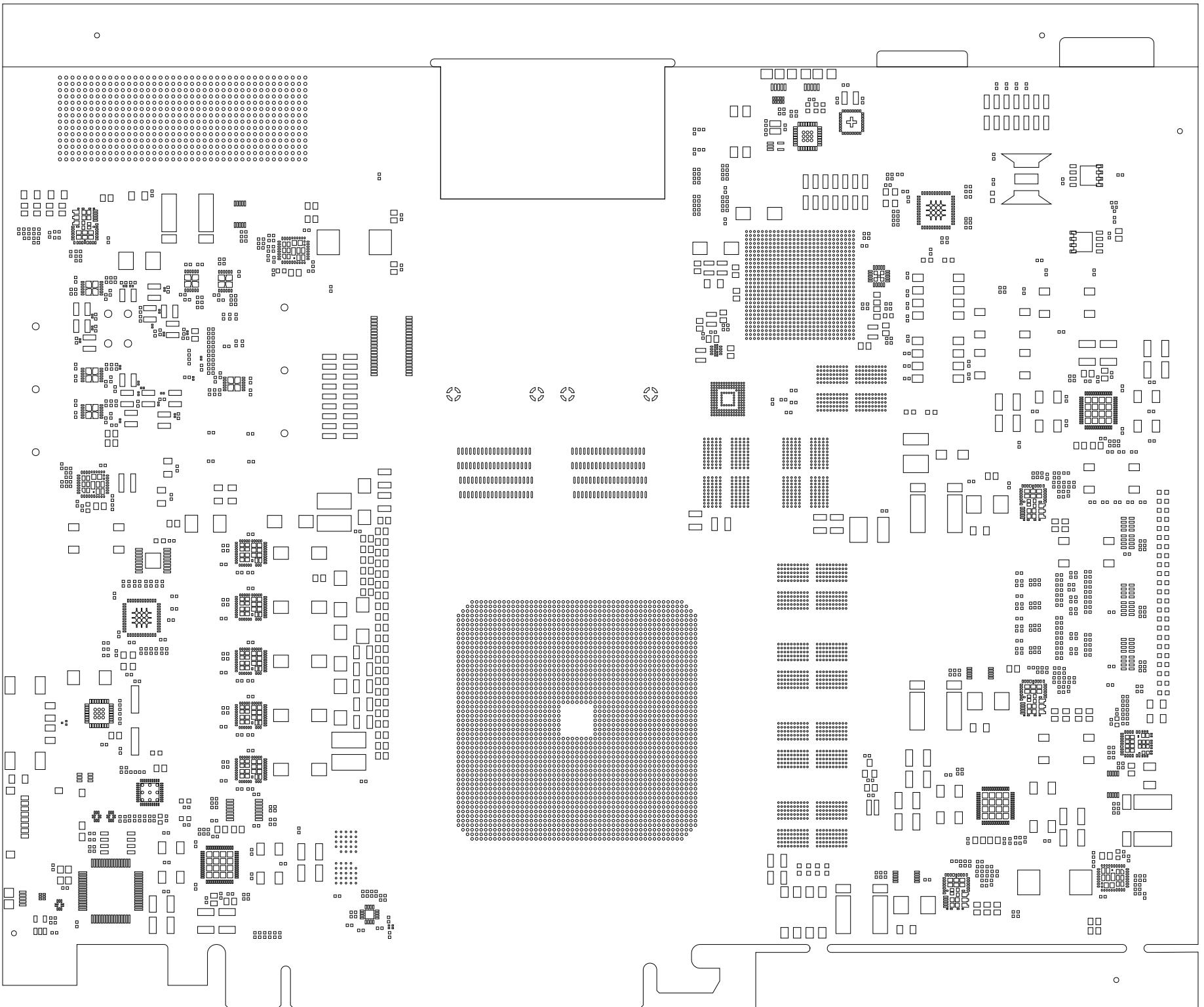
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LAYER: L16_SIG6	XILINX DOC USE ONLY REVISION:B01



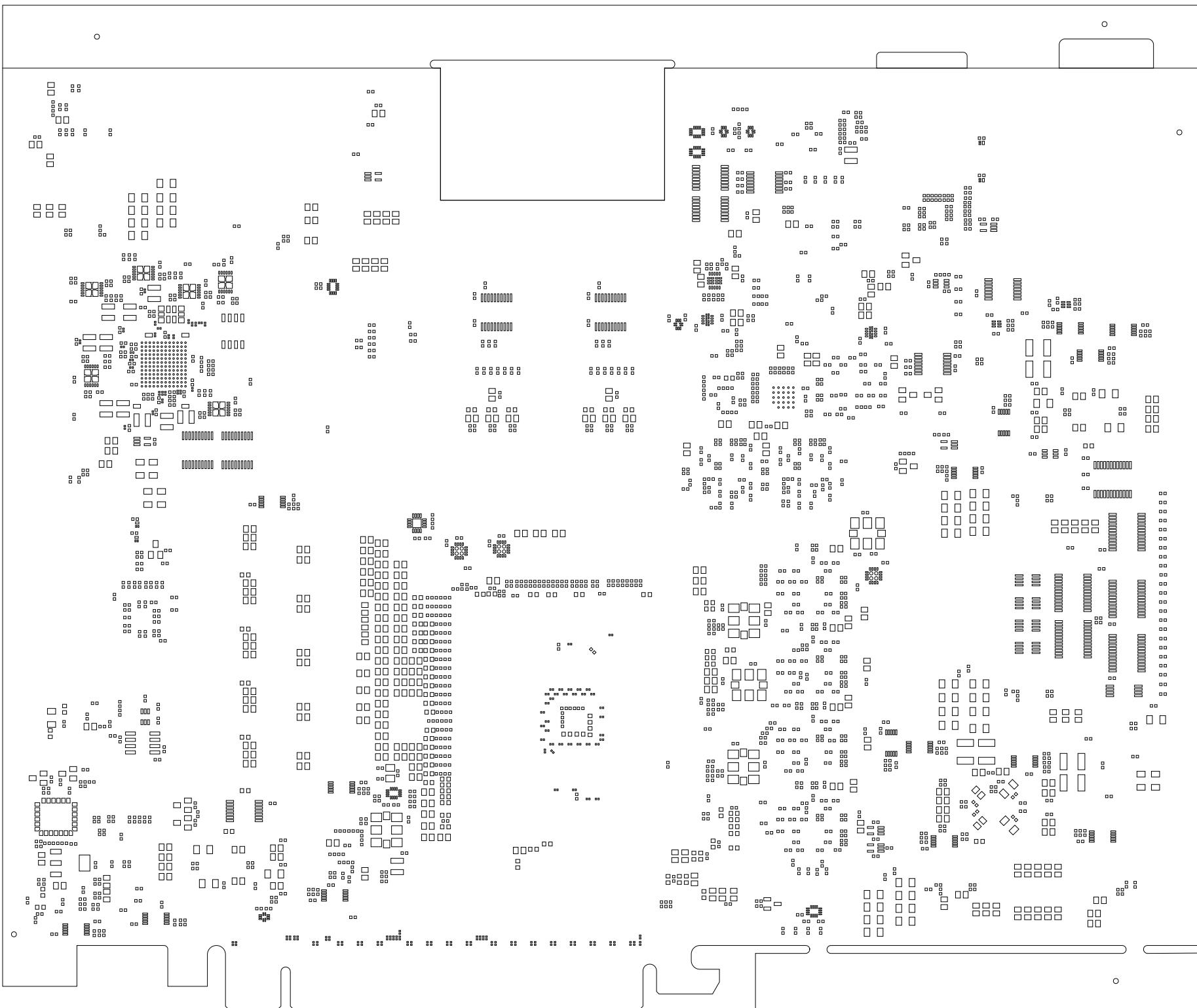
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PCB #	128-05072-01
Designed by Xilinx	DATE: 08/26/2021
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LAYER: L17_GND8	XILINX DOC USE ONLY REVISION:B01



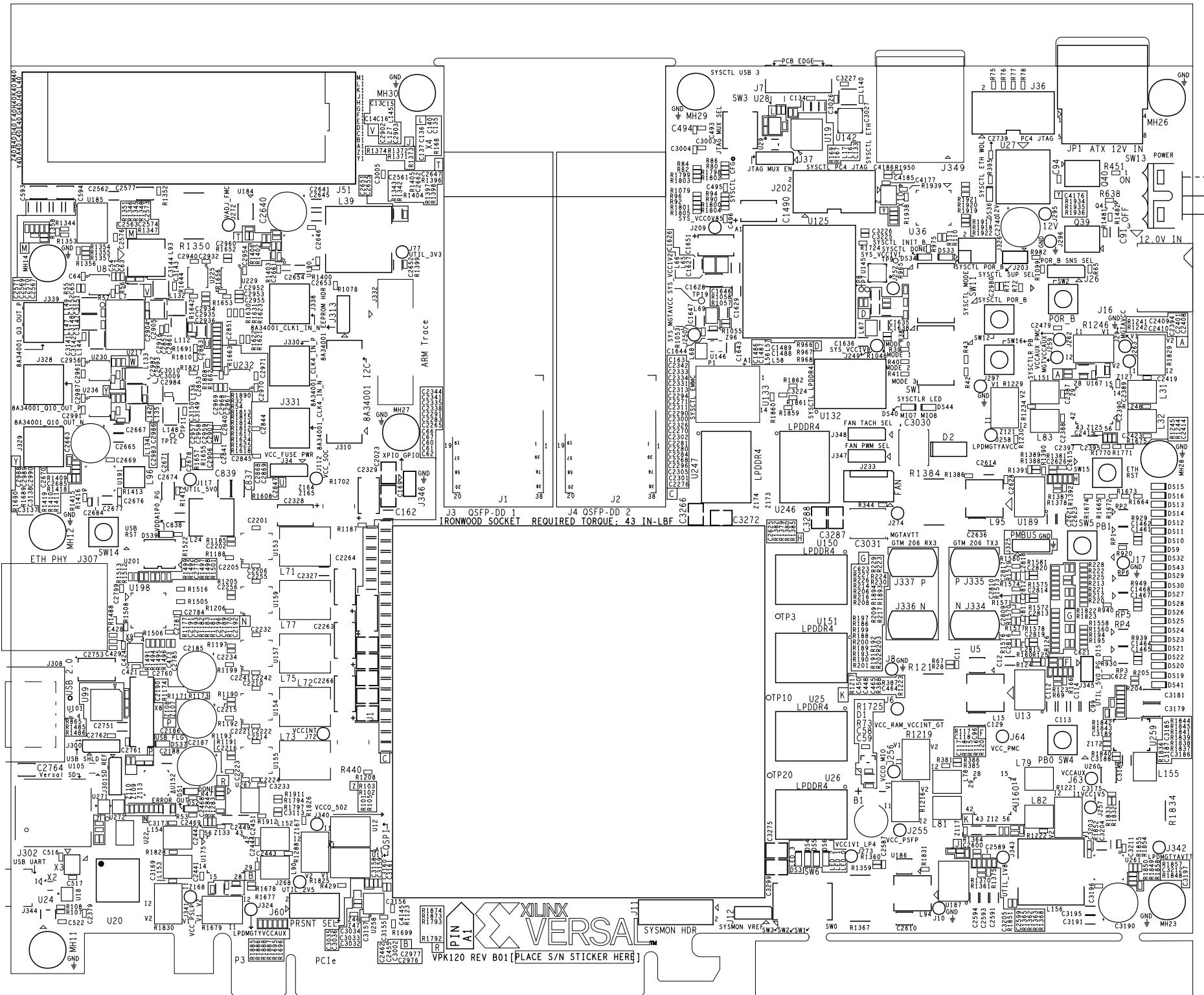
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Designed by Xilinx	DATE: 08/26/2021
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LAYER: L18_BOT	XILINX DOC USE ONLY REVISION:B01



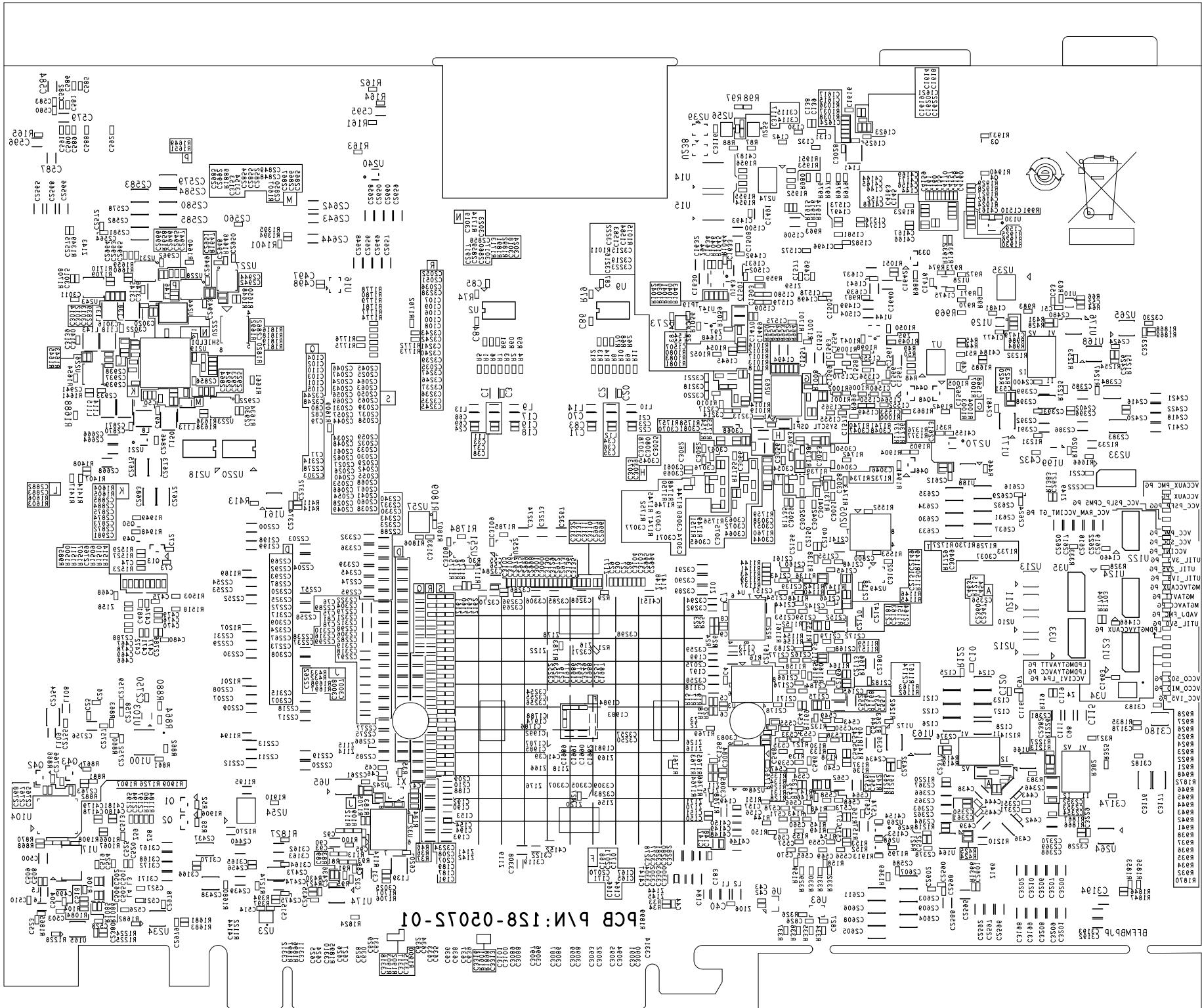
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PCB #	128-05072-01
Designed by Xilinx	DATE: 08/26/2021
SCHEM: BRIAN; LAYOUT:CAROL	PHONE: 720-652-3759
LAYER: PASTEMASK TOP	XILINX DOC USE ONLY REVISION:B01



ARTWORK, ROHS COMPLIANT, VPK120	
PCB #	128-05072-01
Designed by Xilinx	DATE: 08/26/2021
SCHEM: BRIAN; LAYOUT:CAROL	PHONE: 720-652-3759
LAYER: PASTEMASK BOTTOM	XILINX DOC USE ONLY REVISION:B01

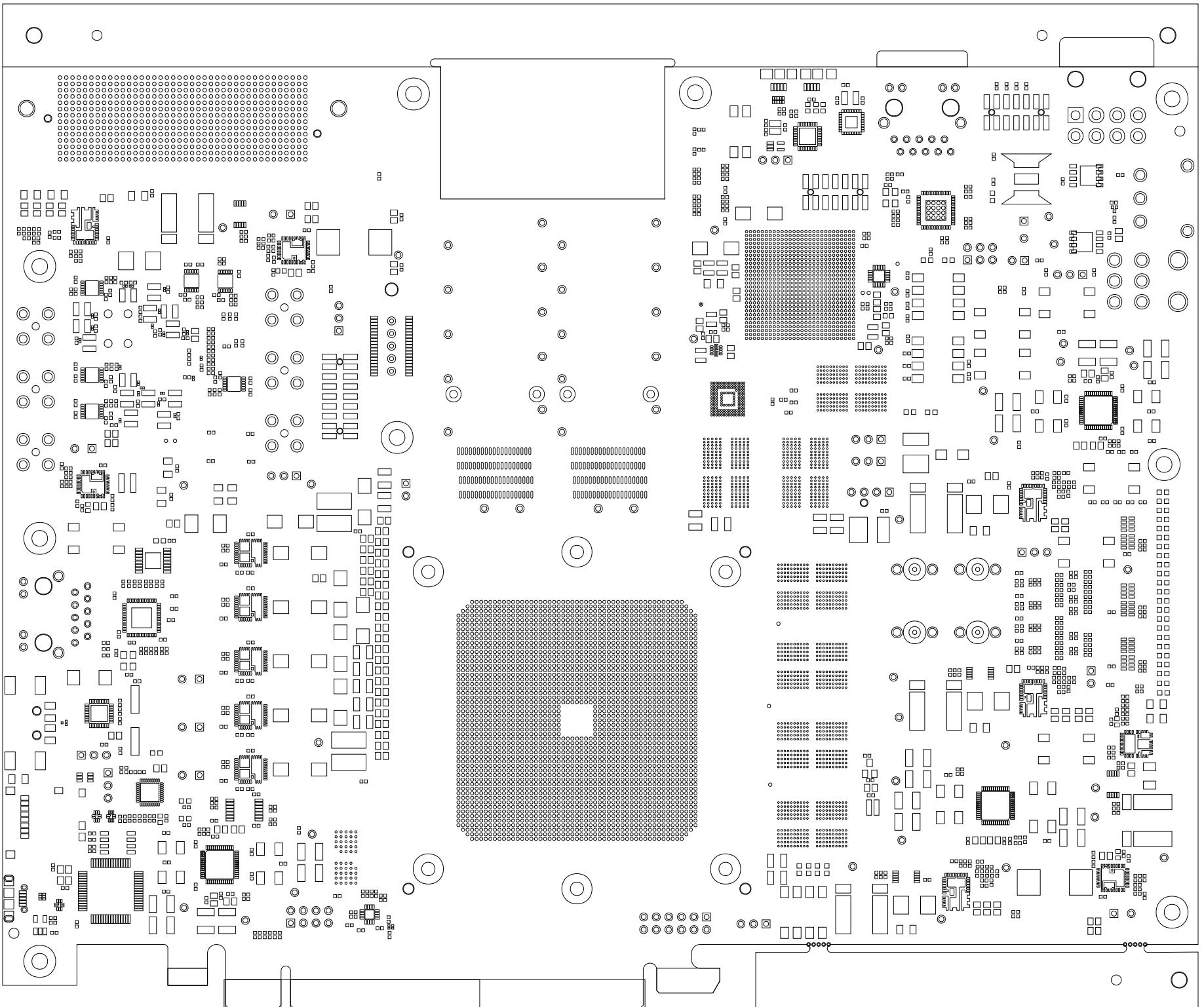


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PCB # 128-05072-01	
Designed by Xilinx	DATE : 08/26/2021
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LAYER:	XILINX DOC USE ONLY REVISION : B01
SILKSCREEN TOP	

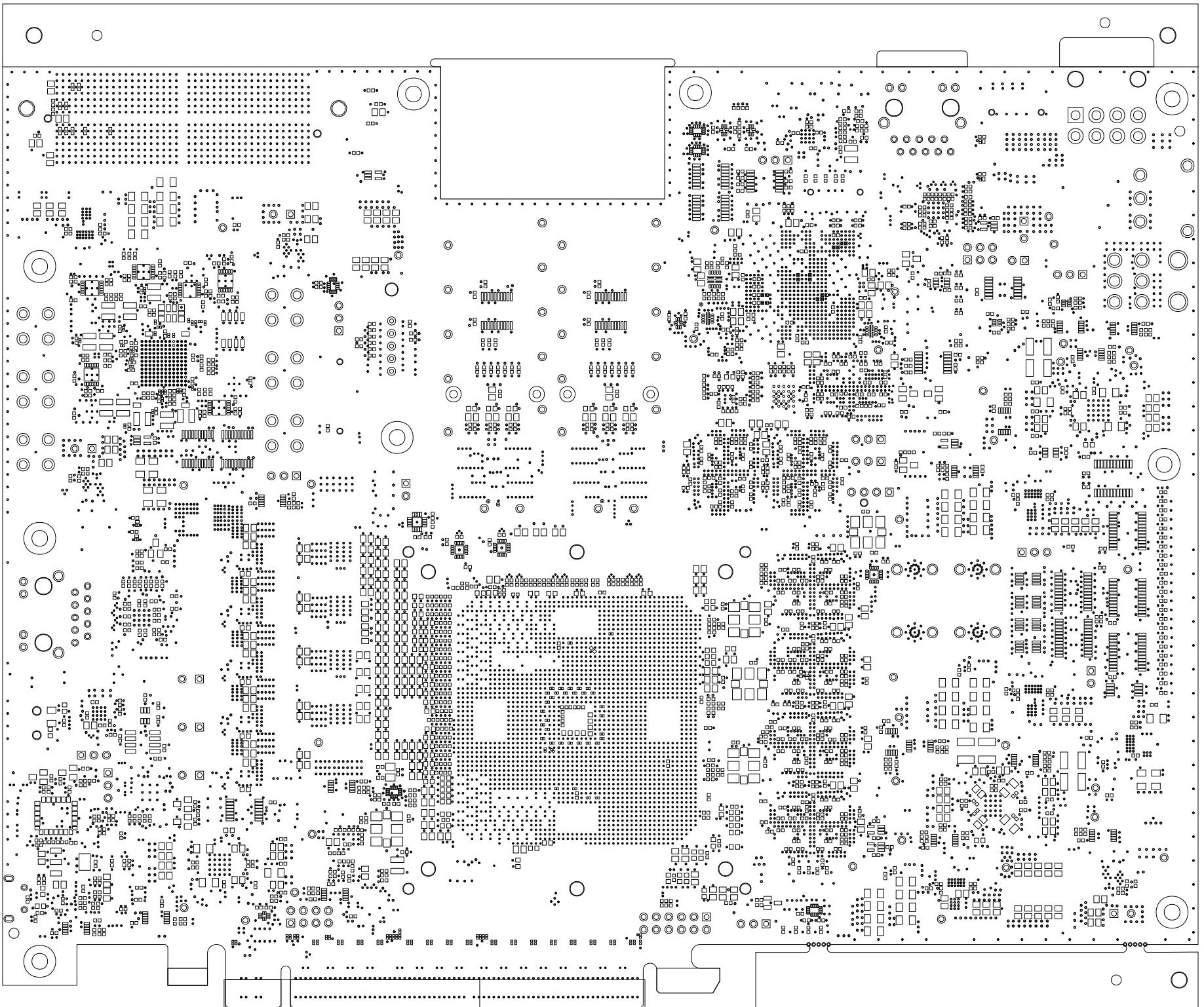


10 - 3

ARTWORK, ROHS COMPLIANT, VPK120	
PCB #	128-05072-01
Designed by Xilinx	DATE: 08/26/2021
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LAYER: SILKSCREEN BOTTOM	XILINX DOC USE ONLY REVISION:B01

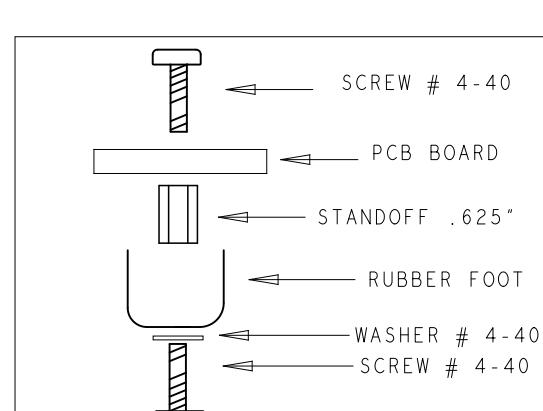
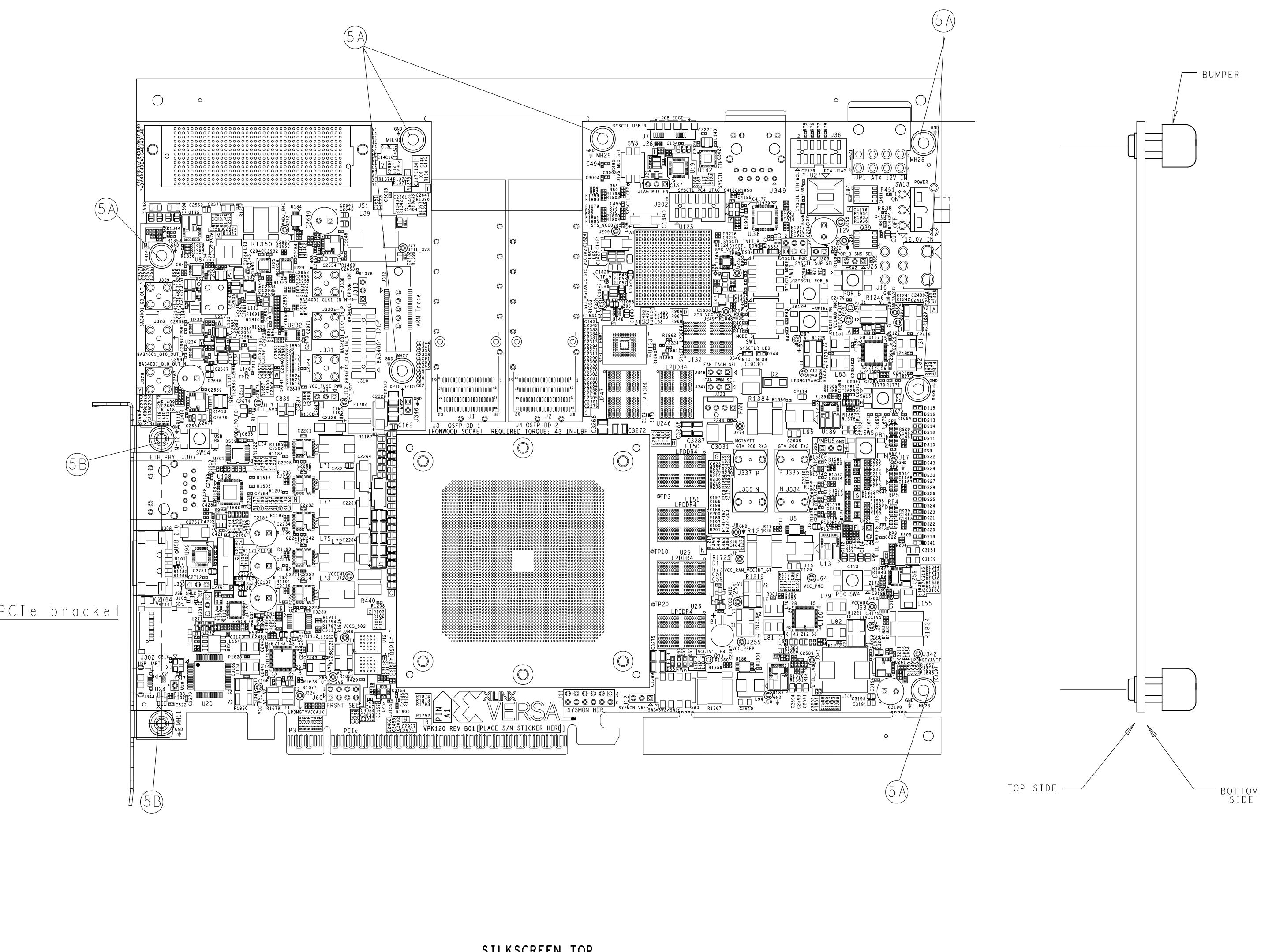


ARTWORK, ROHS COMPLIANT, VPK120	
PCB #	128-05072-01
Designed by Xilinx	DATE: 08/26/2021
SCHEM: BRIAN; LAYOUT:CAROL	PHONE: 720-652-3759
LAYER: SOLDERMASK TOP	XILINX DOC USE ONLY REVISION:B01



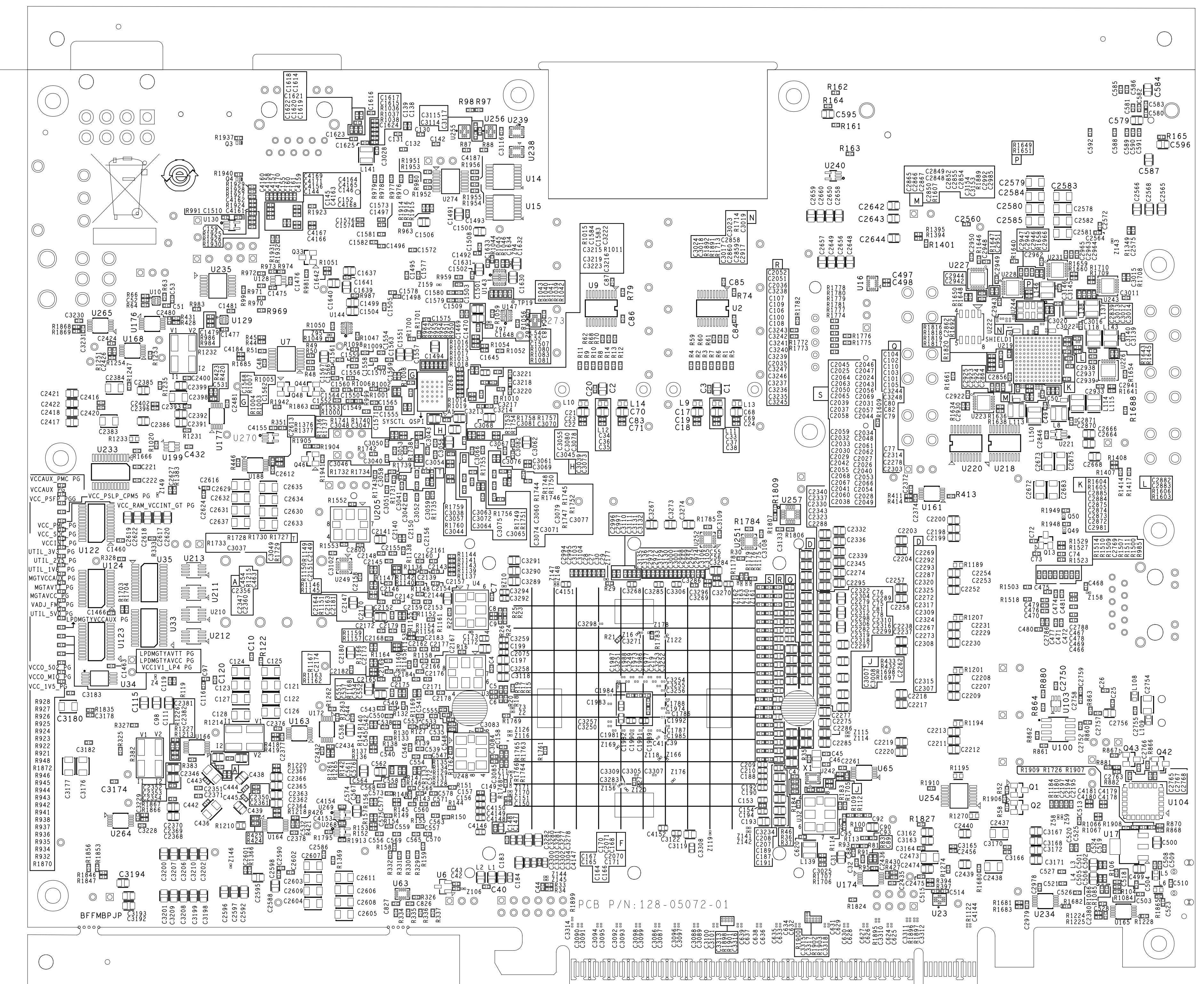
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PCB # 128-05072-01	
Designed by Xilinx	DATE: 08/26/2021
SCHEM: BRIAN; LAYOUT:CAROL	PHONE: 720-652-3759
LAYER: SOLDERMASK BOTTOM	XILINX DOC USE ONLY REVISION:B01

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
01	PROTOTYPE	01/19/21	
01	MISC UPDATES	08/26/21	



UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE					
DIMENSIONS ARE IN INCHES	DRAWN FAWAD MUNAWAR	01/19/21	 XILINX® 2100 LOGIC DR. SAN JOSE, CA 95124 ASSY, ROHS COMPLIANT VPK120				
	CHECKED						
TOLERANCES ON: + / - .005 ANGLES + FRACTIONS +	ENRG BRIAN	01/19/21					
	ISSUED						
			SIZE	FSCM NO	DWG NO	REVISION	DRV
			D		043-05072-01	B01	a a
			SCALE	NONE		SHEET	1 of 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
01	PROTOTYPE	01/19/21	
01	MISC UPDATES	08/26/21	



SECONDARY SIDE

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE	 XILINX® 2100 LOGIC DR. SAN JOSE, CA 95124					
DIMENSIONS ARE IN INCHES	DRAWN FAWAD MUNAWAR	01/19/21						
	CHECKED							
TOLERANCES ON: + / - .005 ANGLES + FRACTIONS +	ENGRG BRIAN	01/19/21	ASSY, ROHS COMPLIANT VPK120					
	ISSUED							
			SIZE	FSCM NO	DWG NO	REVISION		DRV
			D		043-05072-01	B01		a a
			SCALE	NONE			SHEET 2 of 2	

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
A01	PROTOTYPE	01/19/21	
B01	MISC UPDATES	08/26/21	

BACKDRILL: BOTTOM to L4_GND2					
ALL UNITS ARE IN MILS					
FIGURE	BD_SIZE	MNC_LAYER	MAX_DEPTH	MFG_STUB	QTY
.	13.8	L3_SIG1	53.03	12.0	108

NOTES:
- MNC_LAYER: MUST-NOT-CUT-LAYER
- MAX_DEPTH: DEPTH FROM START LAYER TO THE SURFACE OF MUST-NOT-CUT-LAYER
- MFG_STUB : MANUFACTURING STUB LENGTH

BACKDRILL: BOTTOM to L6_GND3					
ALL UNITS ARE IN MILS					
FIGURE	BD_SIZE	MNC_LAYER	MAX_DEPTH	MFG_STUB	QTY
.	13.8	L5_SIG2	46.26	12.0	40

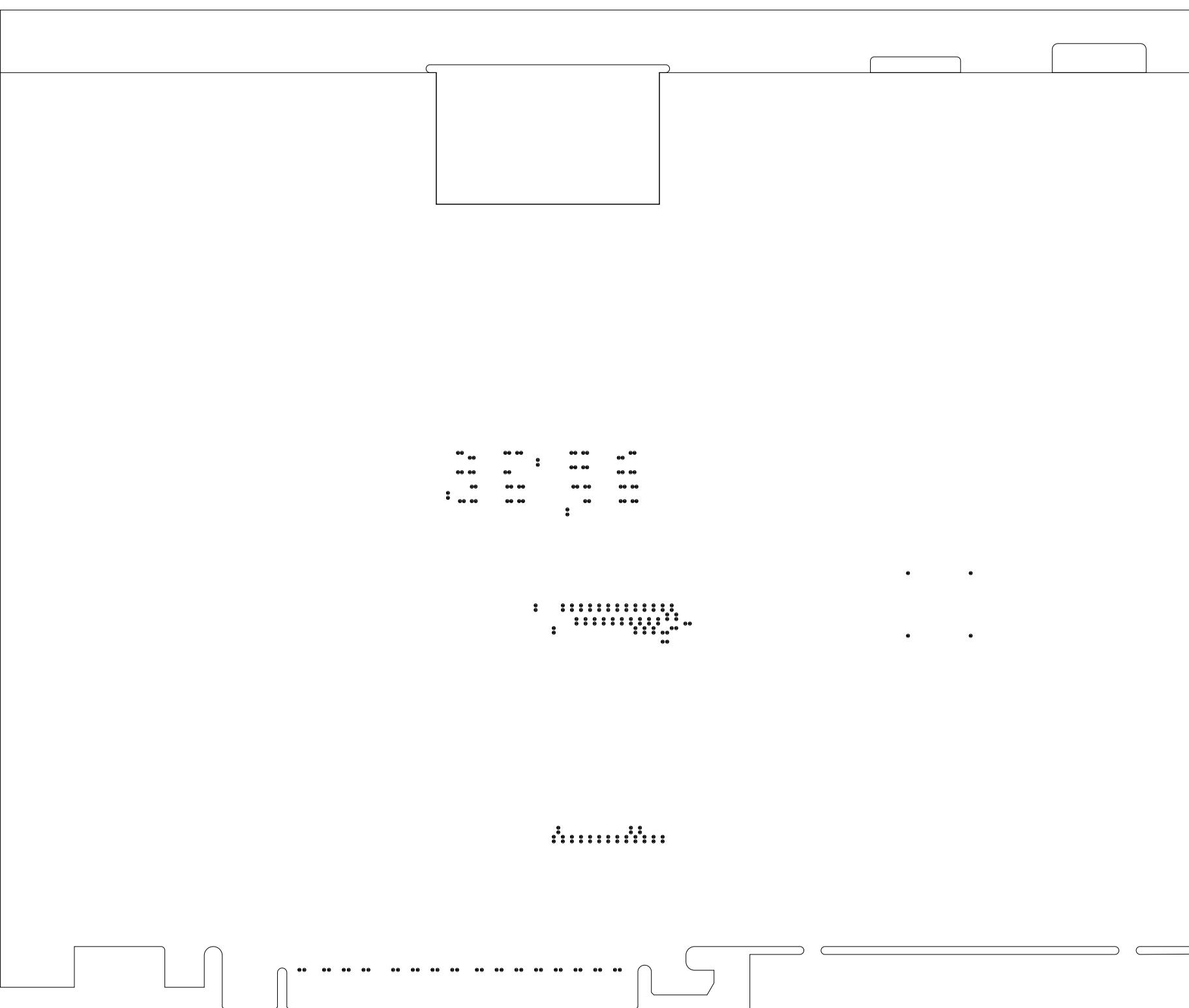
NOTES:
- MNC_LAYER: MUST-NOT-CUT-LAYER
- MAX_DEPTH: DEPTH FROM START LAYER TO THE SURFACE OF MUST-NOT-CUT-LAYER
- MFG_STUB : MANUFACTURING STUB LENGTH

BACKDRILL: BOTTOM to L8_GND4					
ALL UNITS ARE IN MILS					
FIGURE	BD_SIZE	MNC_LAYER	MAX_DEPTH	MFG_STUB	QTY
.	13.8	L7_SIG3	39.49	12.0	44

NOTES:
- MNC_LAYER: MUST-NOT-CUT-LAYER
- MAX_DEPTH: DEPTH FROM START LAYER TO THE SURFACE OF MUST-NOT-CUT-LAYER
- MFG_STUB : MANUFACTURING STUB LENGTH

BACKDRILL: BOTTOM to L13_GND6					
ALL UNITS ARE IN MILS					
FIGURE	BD_SIZE	MNC_LAYER	MAX_DEPTH	MFG_STUB	QTY
.	13.8	L12_SIG4	22.25	12.0	8

NOTES:
- MNC_LAYER: MUST-NOT-CUT-LAYER
- MAX_DEPTH: DEPTH FROM START LAYER TO THE SURFACE OF MUST-NOT-CUT-LAYER
- MFG_STUB : MANUFACTURING STUB LENGTH



UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE	XILINX® 2100 LOGIC DR. SAN JOSE, CA 95124			
DIMENSIONS ARE IN INCHES	DRAWN FAWAD MUNAWAR	01/19/21				
TOLERANCES ON: +/- .005	CHECKED		ASSY, ROHS COMPLIANT VPK120			
ANGLES + FRACTIONS +	ENGRG BRIAN	01/19/21				
ISSUED			SIZE FSCM NO DWG NO D 128-05072-01 B01 DRV SCALE NONE SHEET 1 of 1			