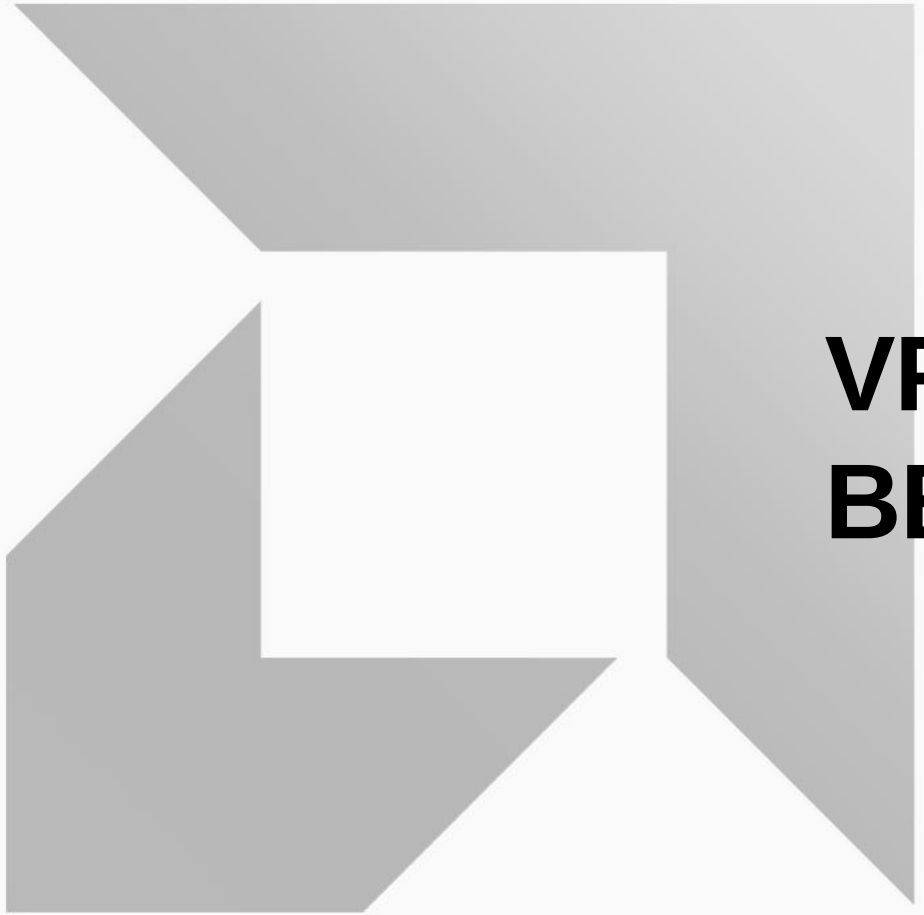


VPK120
BEAM & System Controller

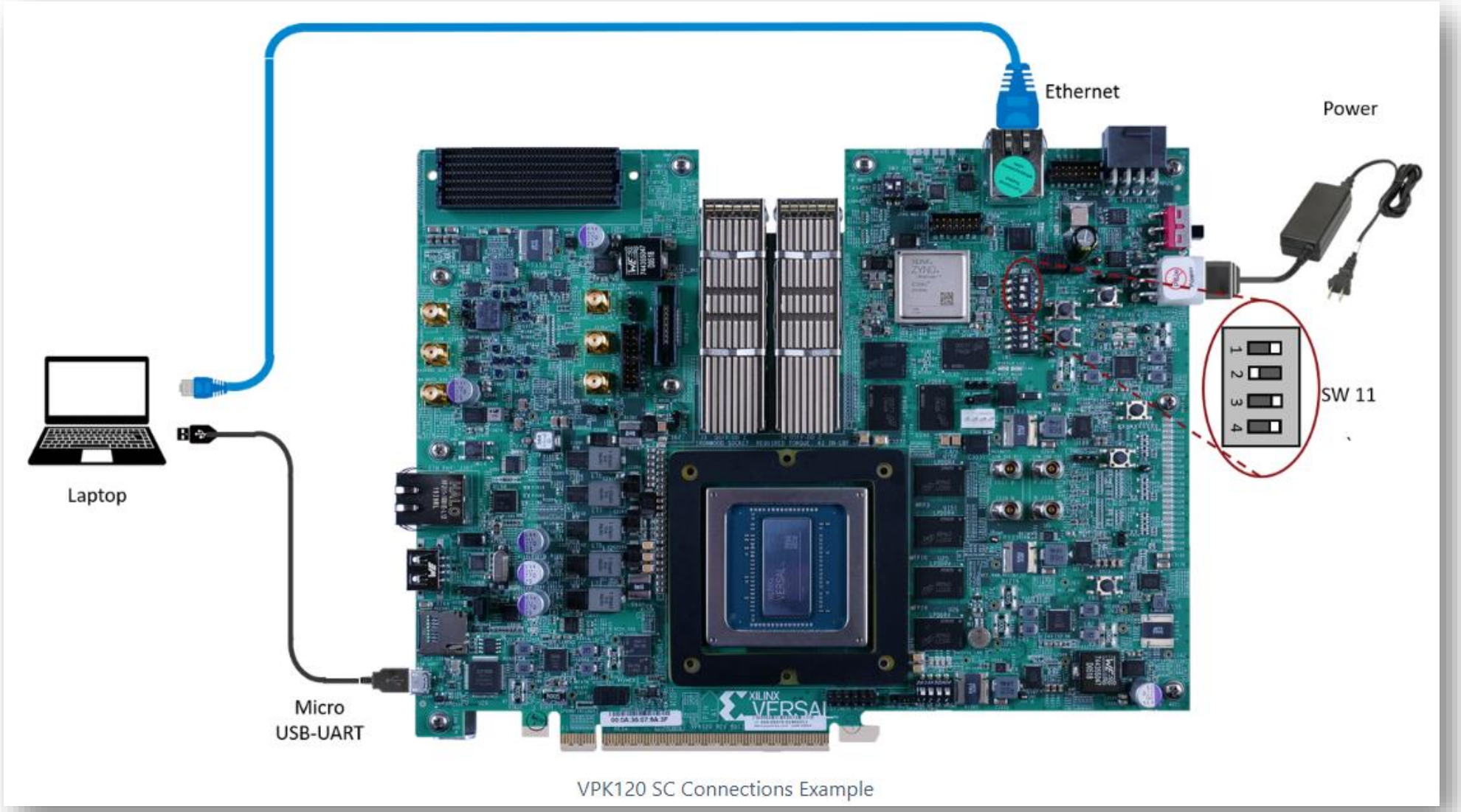
AMD
together we advance_

BEAM

BEAM

BEAM is a web based GUI application to monitor and modify parameters of the evaluation board. The BEAM web page connects to a web server running on the system controller and provides a home screen which provides navigation to board specific test interfaces and related product pages.

Board setup and Connections



VPK120 SC Connections Example

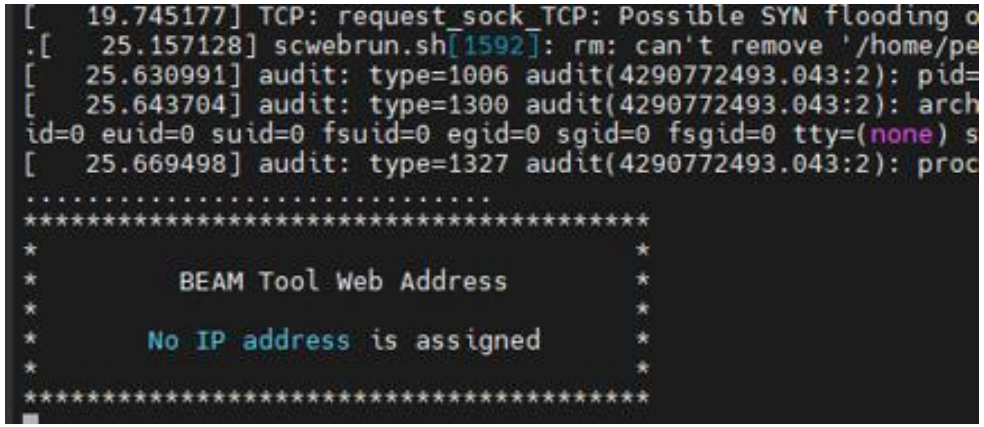
Board setup and Connections

1.Of the three COM ports that are assigned when connecting a cable to the debug port, connect your terminal program to the highest com port. Configure the port with 115200,8,n,1.

2.The board and Windows PC with Ethernet can be connected directly. Alternatively, the board can be in a network with a DHCP server running to provide the address.

3.Login to the system controller using the serial terminal using the username ***petalinux*** and if prompted for a password, enter the password that you set up for the first time login.

4.For the first time login, there will be a prompt to set a password. Set a password that you can remember for the next login.



Board setup and Connections

For some boards shipping from the factory, a login for the system controller console session will not appear, but instead the following banner appears in the console output:

```
**********************************************************
*  Enter these key-sequence to exit Board Framework  *
*                                                        *
*               EXT<Enter key><Tab key>                  *
**********************************************************
```

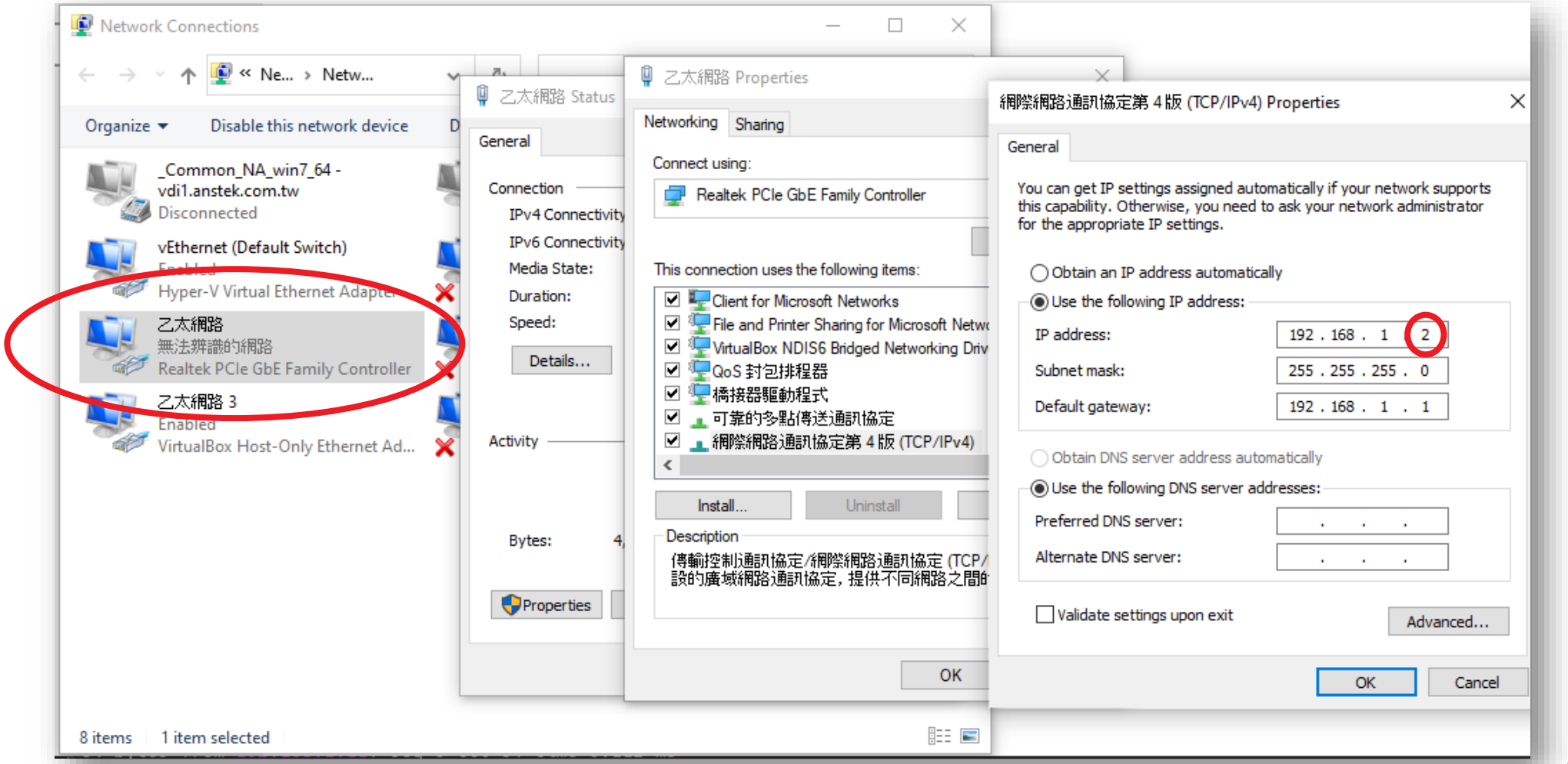
Enter the keyboard sequence as indicated EXT<Enter key><Tab key> to gain access to the command prompt.

```
**********************************************************
*  Enter these key-sequence to exit Board Framework  *
*                                                        *
*               EXT<Enter key><Tab key>                  *
**********************************************************
[   54.108846] TCP: request_sock_TCP: Possible SYN flooding on port 2542. Sending cookies.  Check SNMP counters.
Connect to this XSDB server use host xilinx-versal-system-controller-2021_2 and port 54321
[ 54.62 ]       DONE
Starting tcf-agent: OK

root@xilinx-versal-system-controller-2021_2:~#
```

Windows PC IP Settings

Make sure that the last digit of the IP Address on the Windows PC is different to what is being set on the Board.



Board IP Setting

enter the below command to override the IP address configured through the DHCP and to set the required static IP in the target board. use the below command to set the IP:

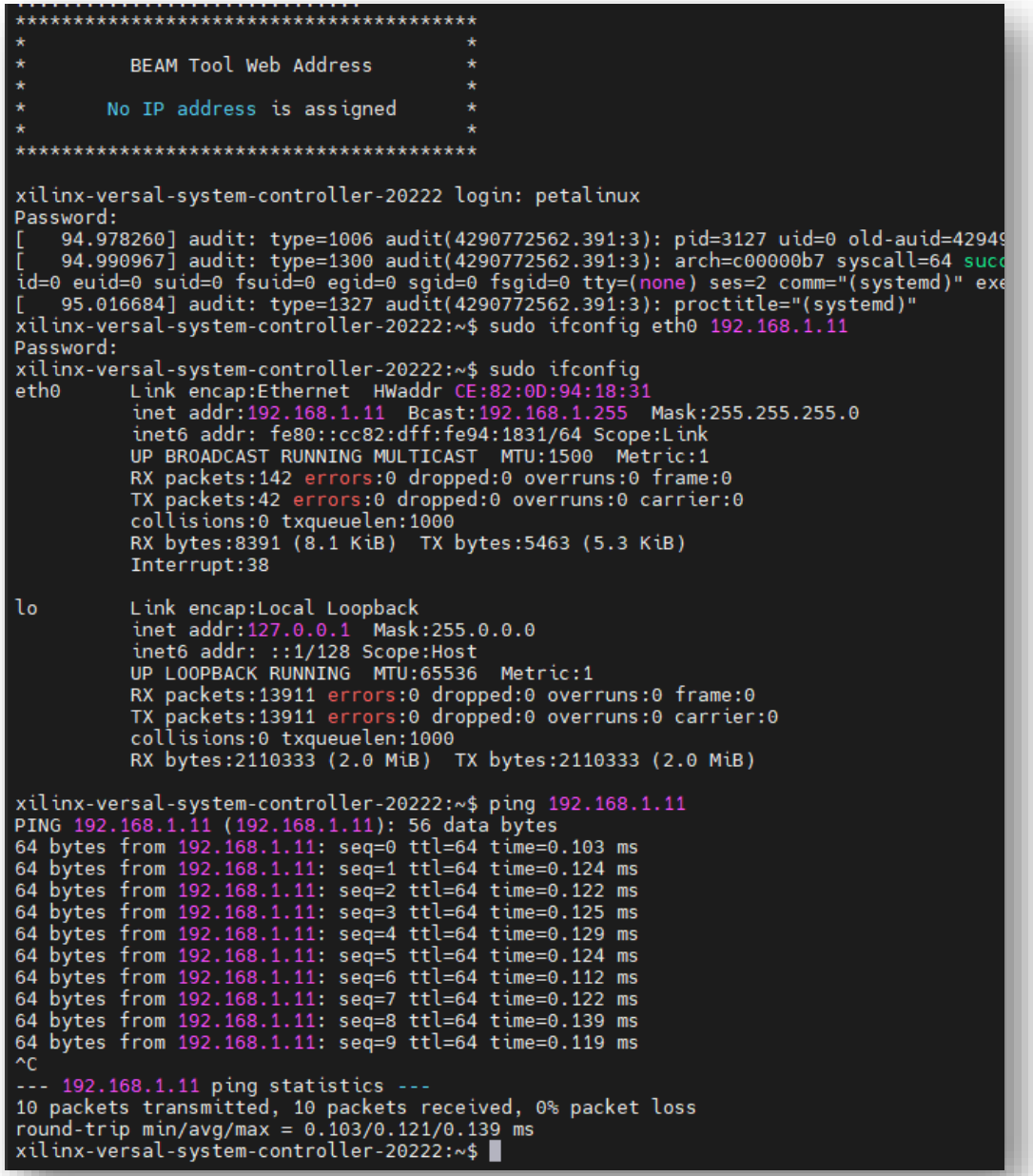
sudo ifconfig eth0 192.168.1.11

Verify/check the IP address of the board on the session.
sudo ifconfig

Ping the Windows PC with the below command via the session. Press Ctrl + C to stop ping on session.

ping <host_ip>

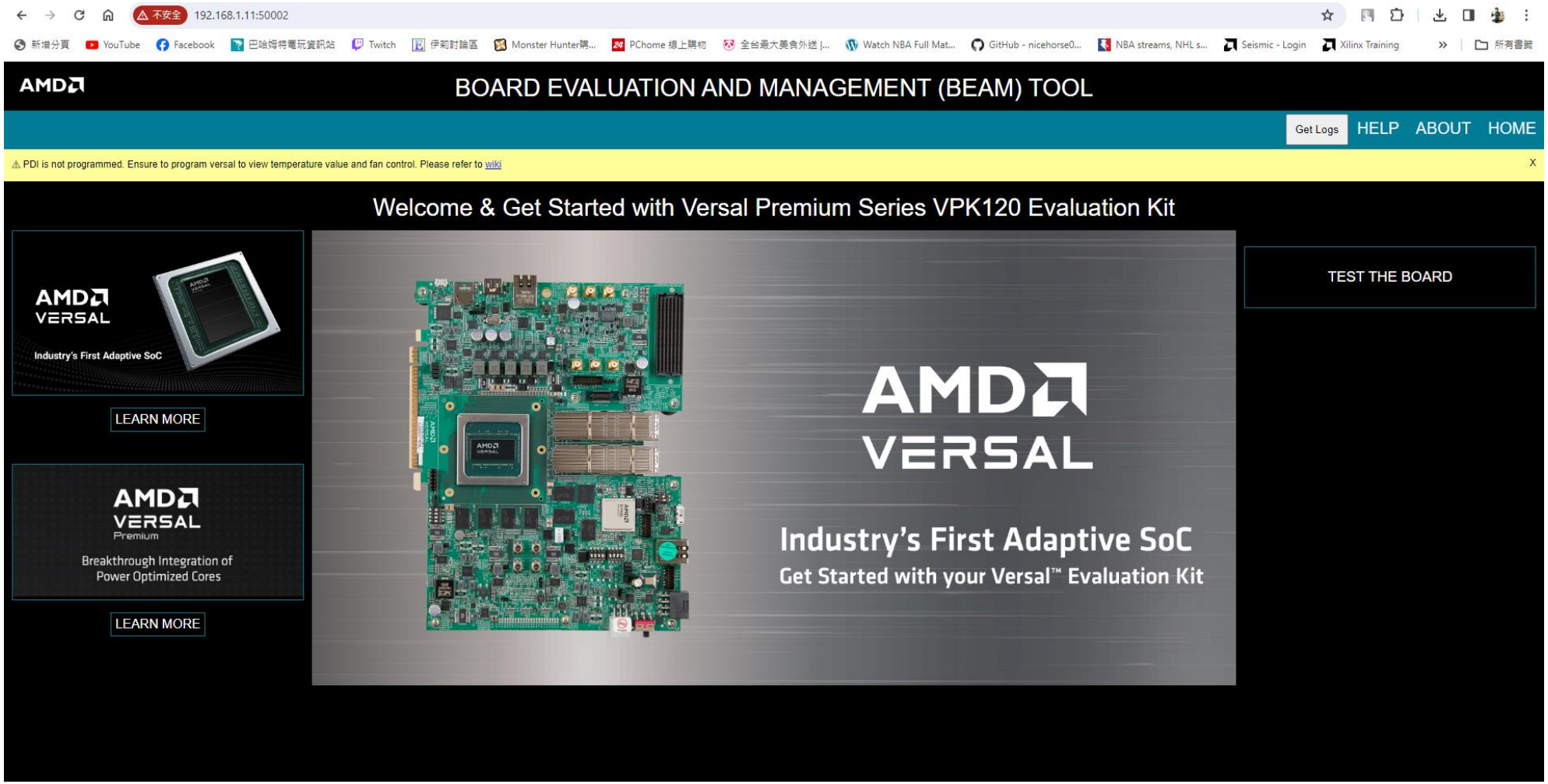
Ex: ping 192.168.1.11



Launching the GUI

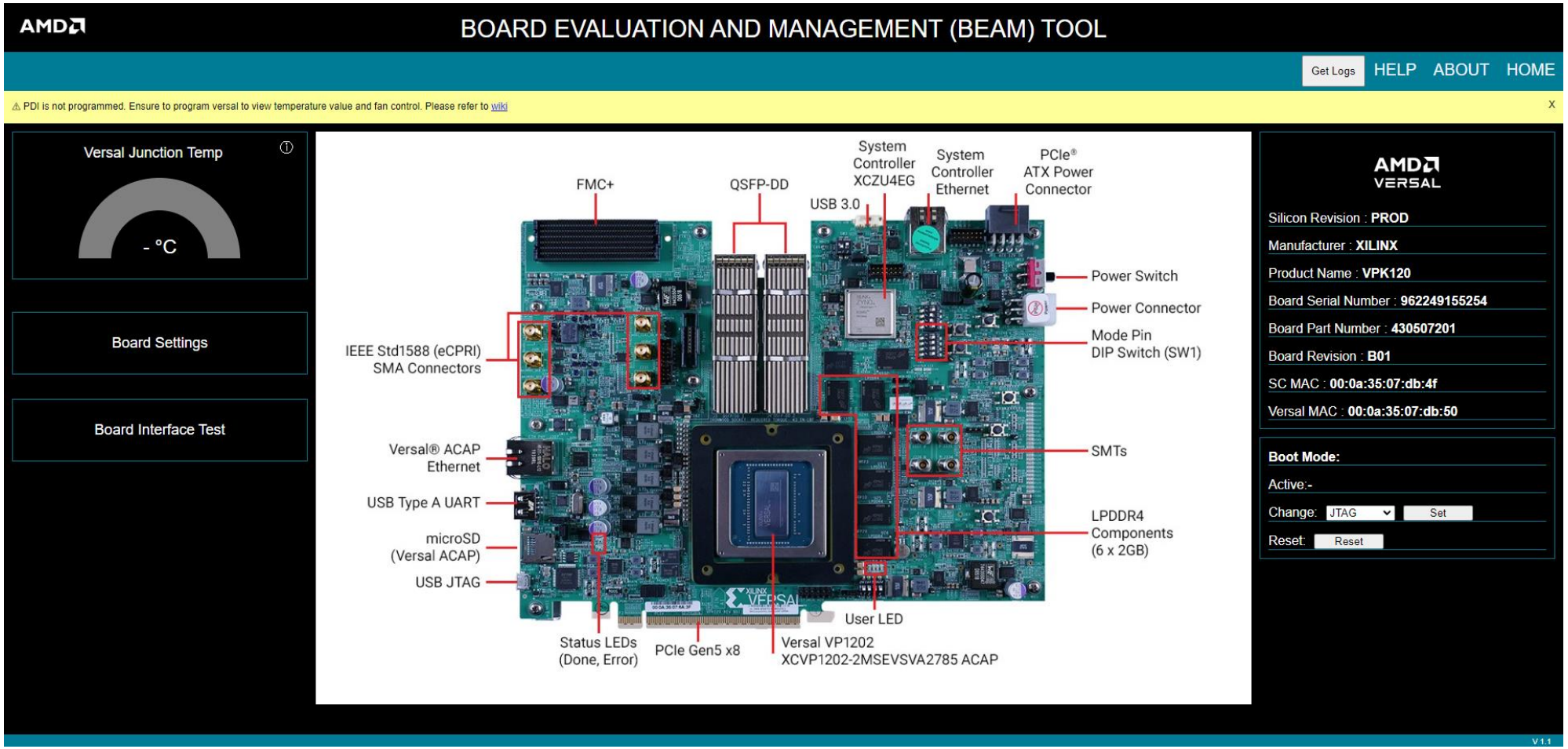
On the Windows PC, Open the Chrome web browser.

Enter <ip of system_controller>:50002 in the address bar of the web browser. (Ex:192.168.1.11:50002)



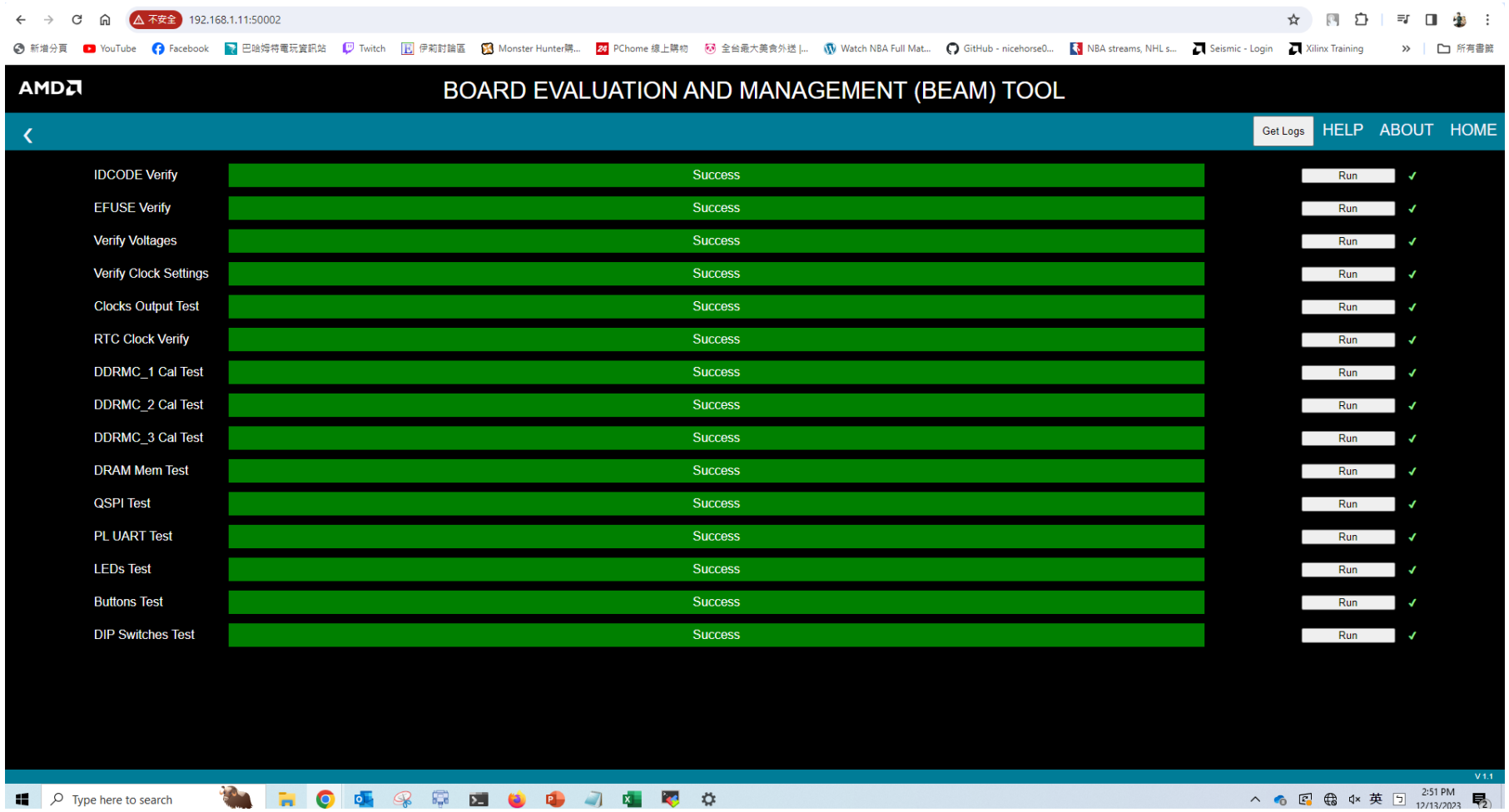
Test the Board

The “Test the board” screen contains board image, device details, and boot mode.
It contains navigation options to Board settings and Board interface test screens.



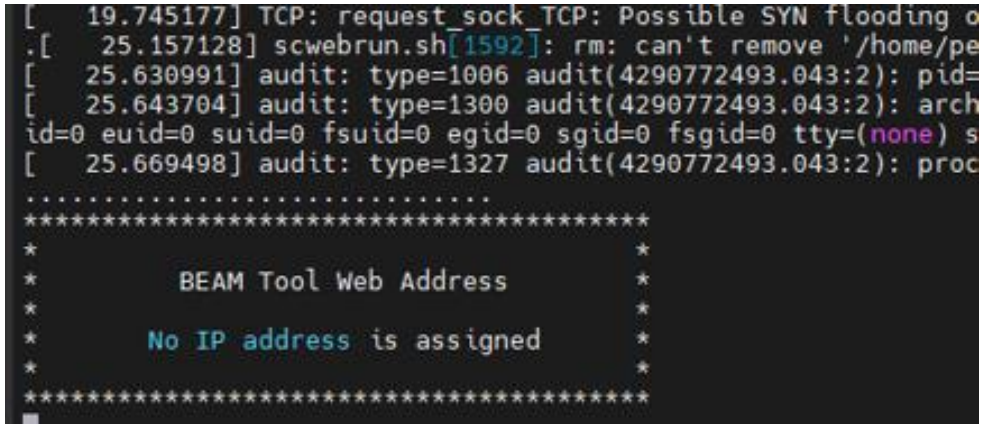
Board Interface Test

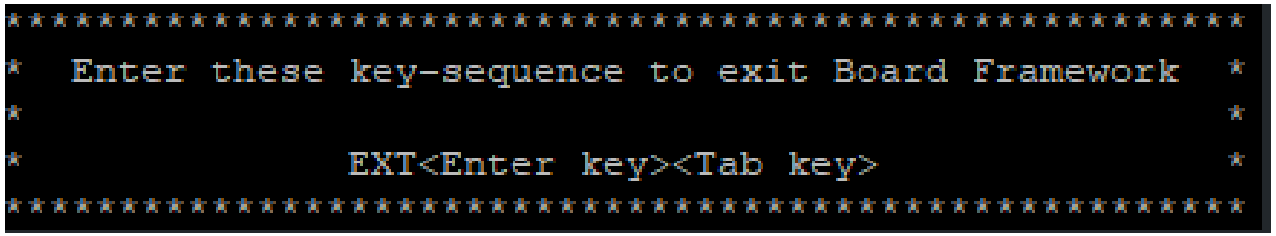
From the Home screen, click on the “Test The Board” panel and then click the “Board Interface Test” button to display the Board Interface Test (BIT) section.



Linux Image Updates

- If the displayed screen during boot differs from the demonstrated image, you may need to update the Linux image.

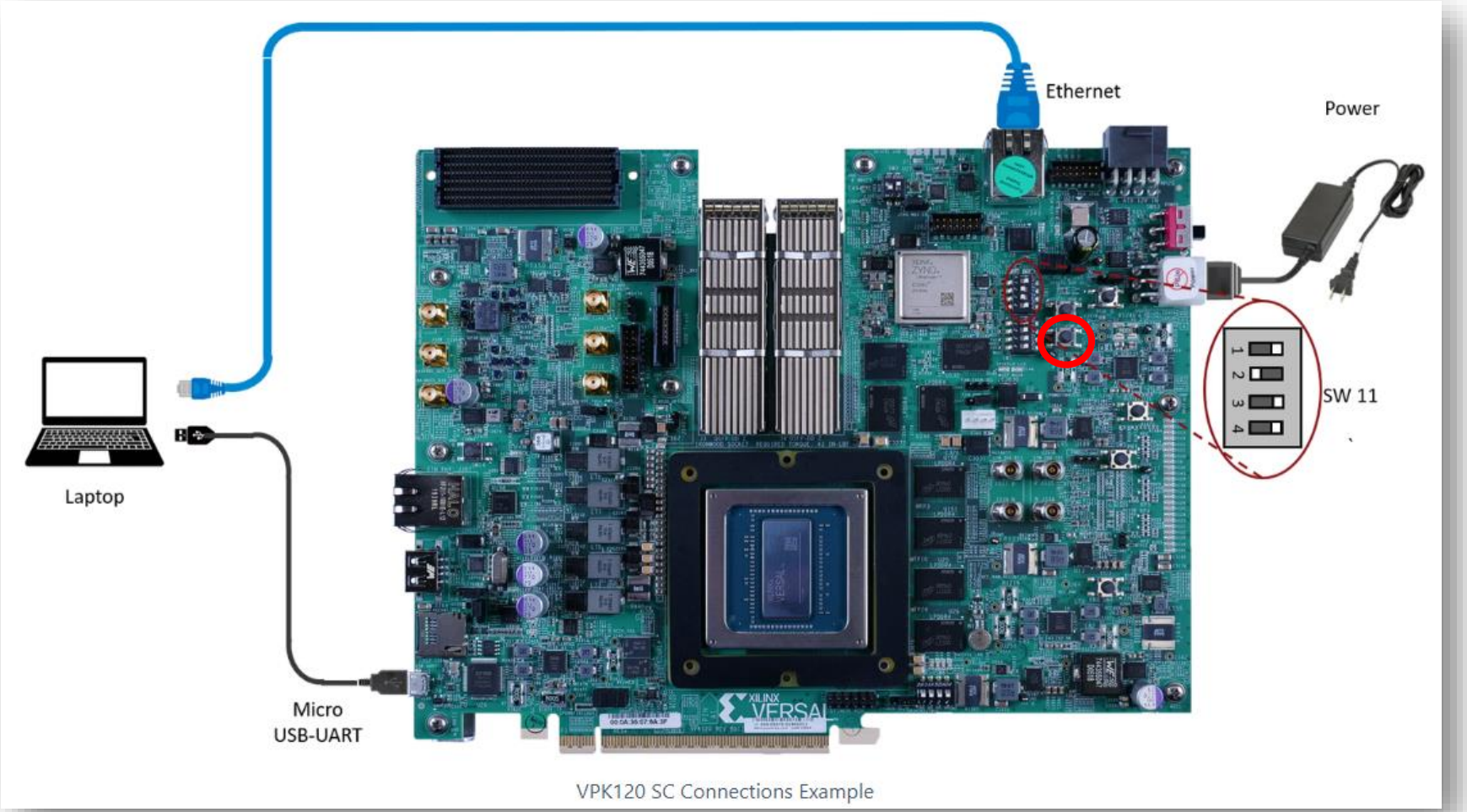




SC Linux Image	Description & Updates	Board Supported	Download Link
SC Update 0 (2021.2 base)	Early Access BEAM release	VPK120ES	None - Factory deployed only
SC Update 1 (2022.1 base)	Initial BEAM production release	VPK120ES, VPK120, VPK180ES	Xilinx Download
SC Update 2 (2022.2 base)	BEAM based active fan control	VPK120ES, VPK120, VPK180ES, VPK180, VHK158ES	Xilinx Download
SC Update 3 (2022.2 base)	BEAM, SC fan control, bug fixes & feature enhancements	VPK120ES, VPK120, VPK180ES, VPK180, VHK158ES, VHK158, VEK280ES	Xilinx Download
SC Update 4 (2022.2 base)	BEAM, SC fan Control, various bug fixes & feature enhancements	VPK120ES, VPK120, VPK180ES, VPK180, VHK158ES, VHK158, VEK280ES	Xilinx Download
SC Update 5 (2022.2 base)	Add support for VEK280, bug fix release	VPK120ES, VPK120, VPK180ES, VPK180, VHK158ES, VHK158, VEK280ES, VEK280	Xilinx Download

Board setup and Connections

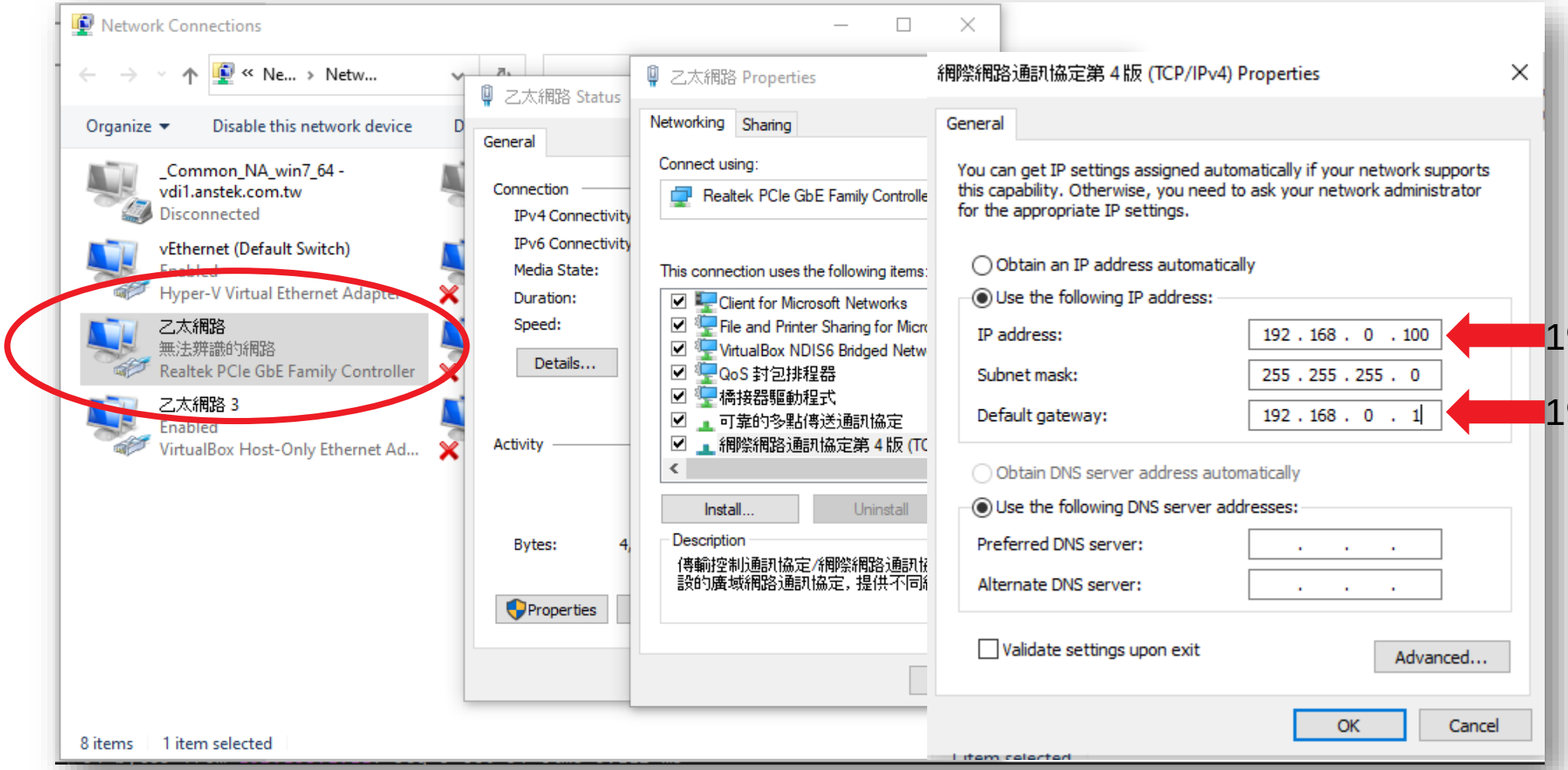
No changes are required in the development board configuration.
The tool is launched by holding the SC FWUEN pushbutton during a power-on of the evaluation board.



VPK120 SC Connections Example

Windows PC IP Settings

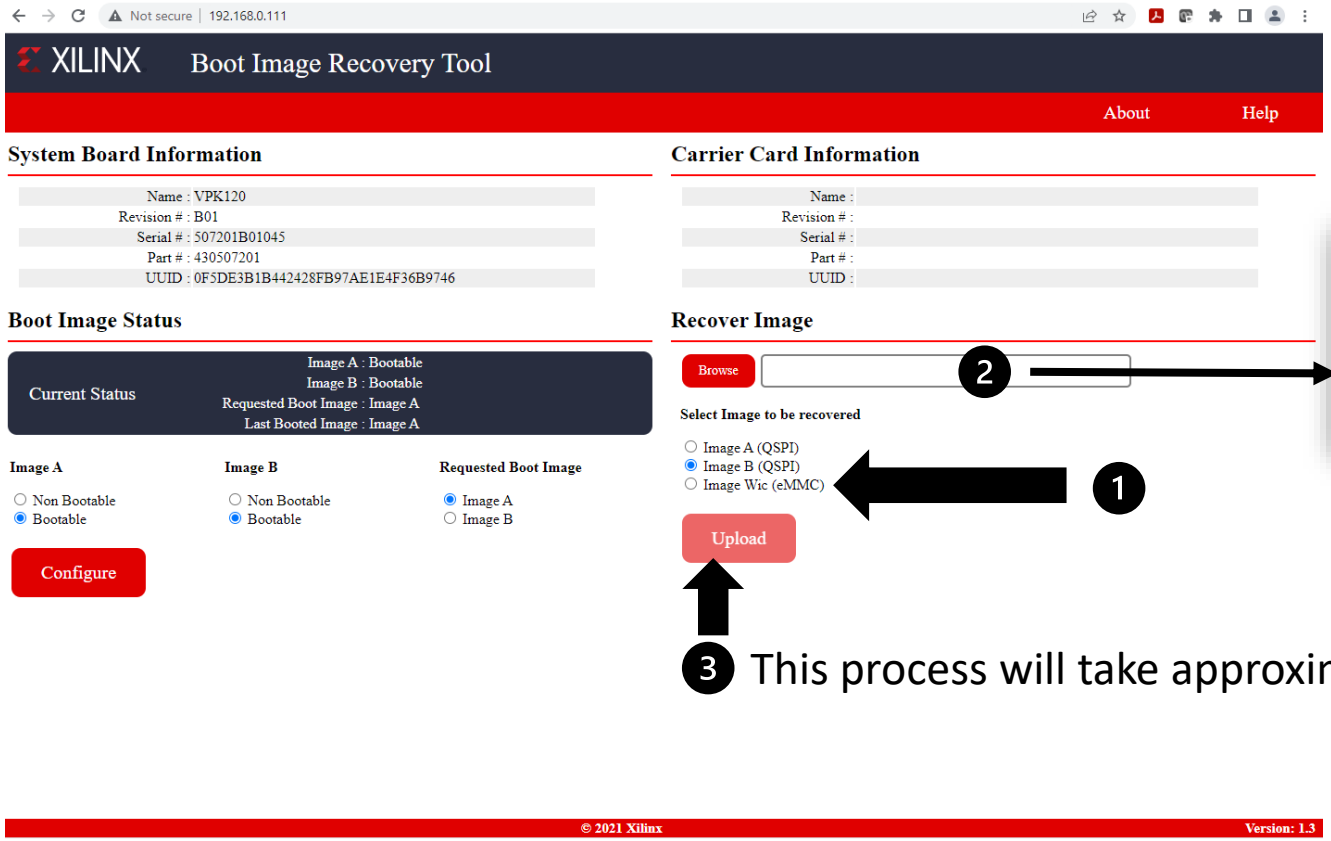
Make sure that the last digit of the IP Address on the Windows PC is different to what is being set on the Board.

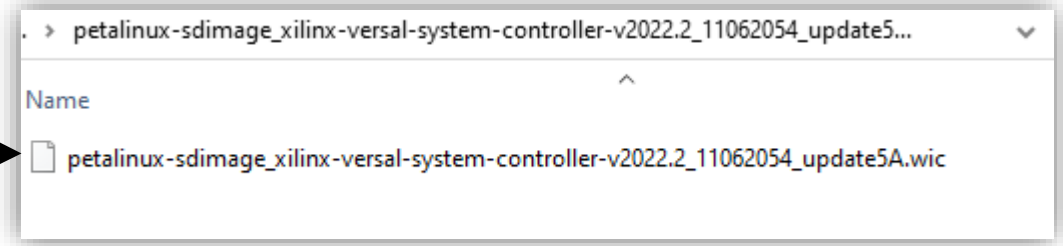


Board setup and Connections

update the Linux image download the desired SC Linux image and use the Image Recovery applicatoin “Image Wic (eMMC)” radial selection and the “Browse” button to select the downloaded <linux-image-name>.wic.

If the file downloaded was in a compressed format (e.g. .xz) then use a compression tool (e.g. 7Zip) on your Host PC to first decompress the file to a native *.wic format prior to using the Image Recovery Tool.



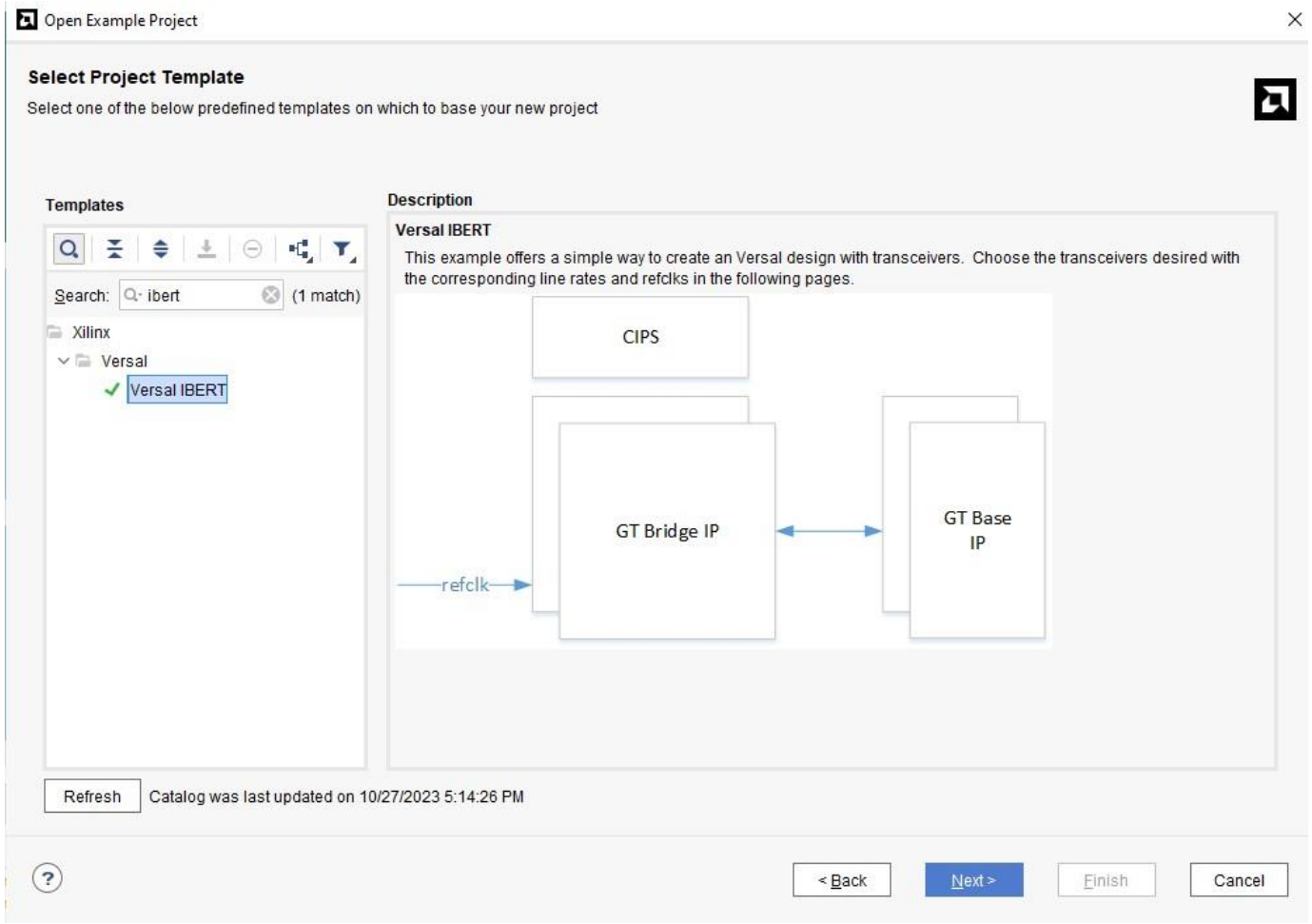


This process will take approximately 40 to 50 minutes.

Versal IBERT

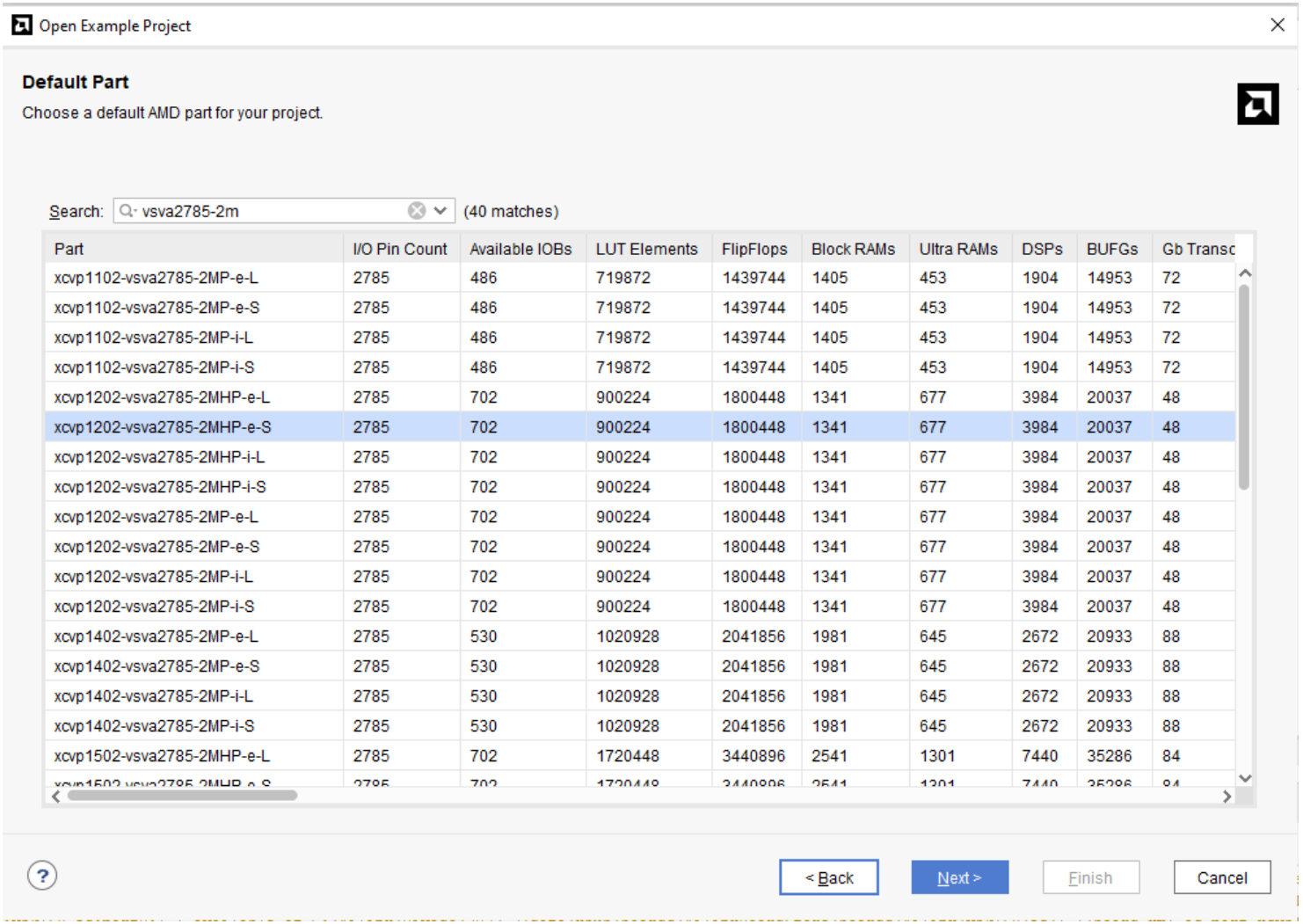
Versal IBERT Example Design

The design consists of a specific flow that will ensure success and repeatability by leveraging built in Vivado example designs and flows. This same flow can be used with deviations later, in order to test different bandwidths, GTs or other board capabilities. The design can be simply explained with the following block diagram



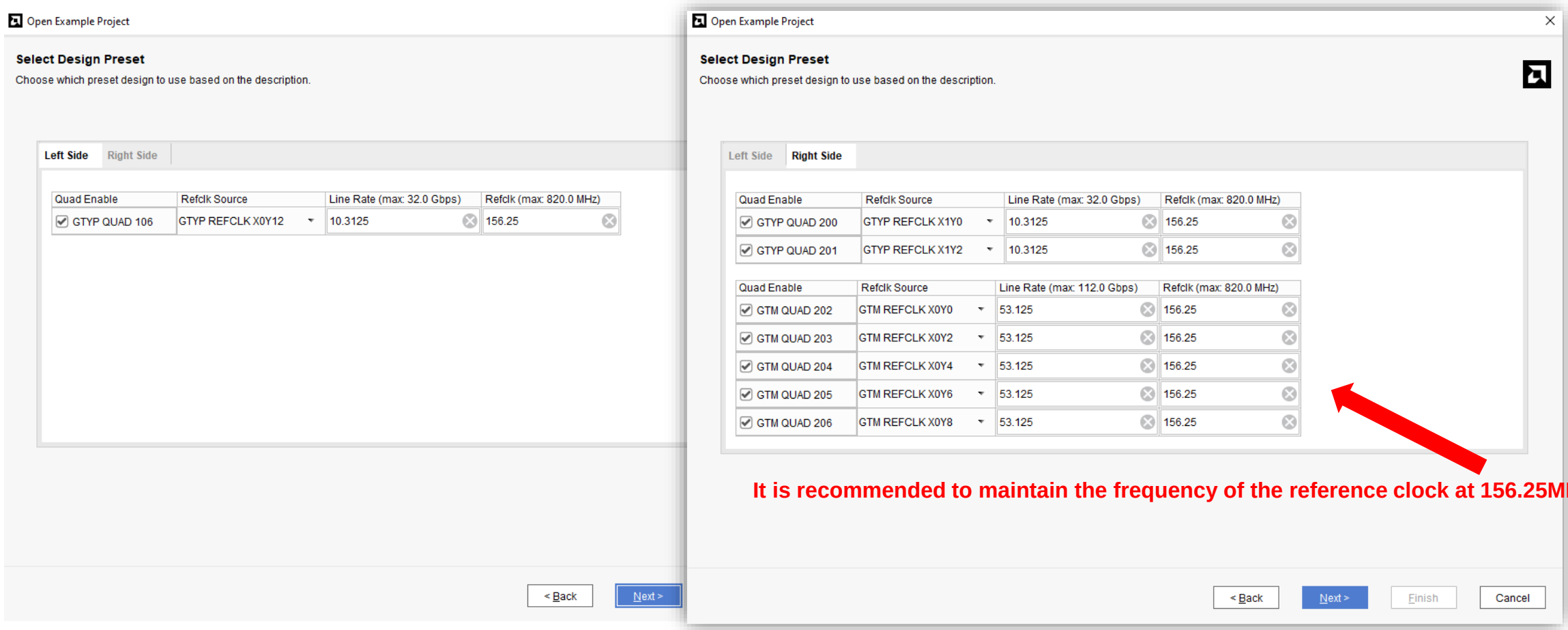
Versal IBERT Example Design

In the Default Part selection, click on the Part column header, which will sort the parts repeatably13. Scroll nearly 5/6 of the way down and select xcvp1202-vsva2785-2MP(or2MHP)-e-S



Versal IBERT Example Design

Here we can select the GTYP/GTM for our IBERT design.
The GTs are broken up into a left and right side well as broken into QUADs



Versal Transceiver Mapping

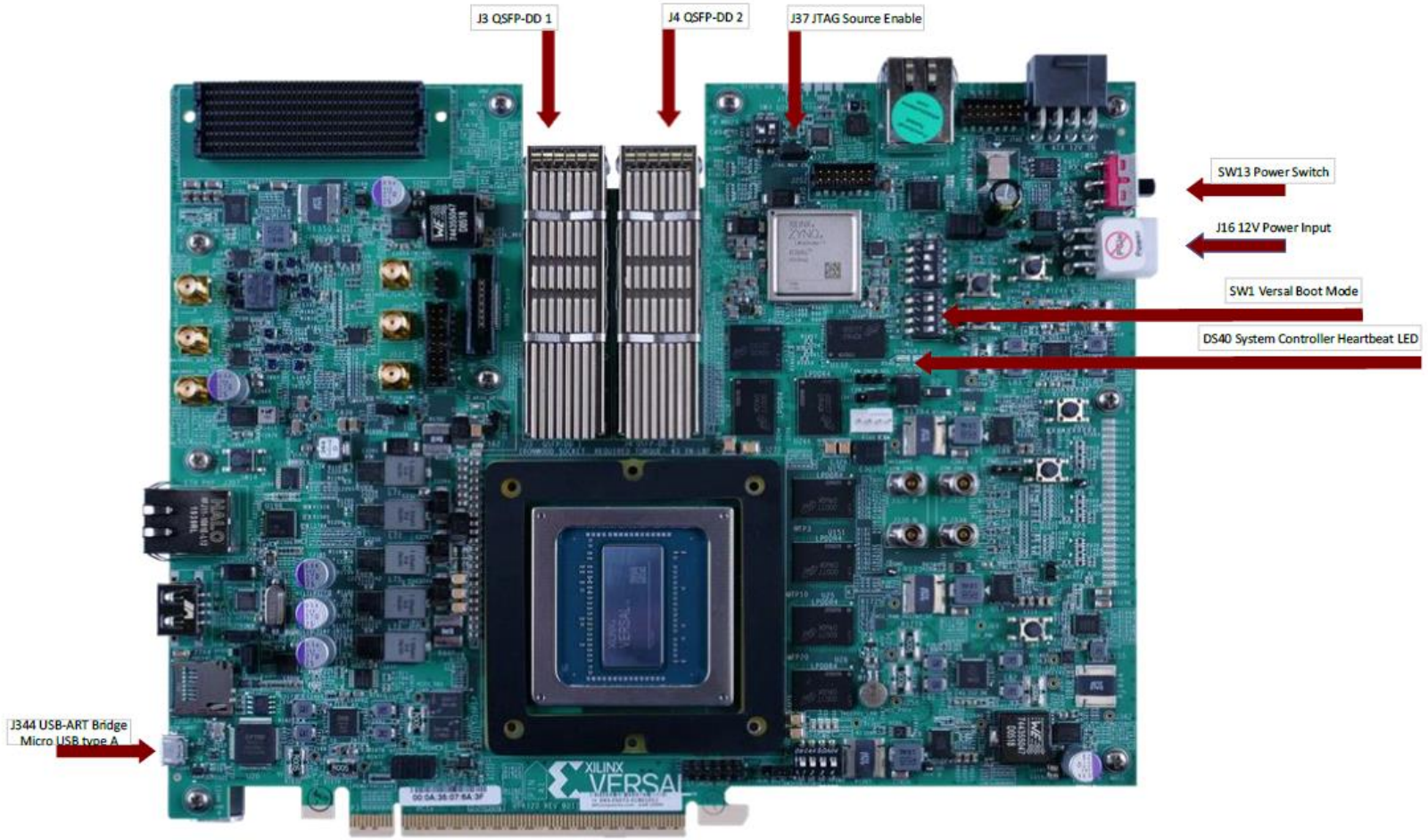
- In the User Guide, the Transceiver Mapping table has more detail as the included hardened IP blocks associated with specific transceiver quads are mapped out including which clocks are associated with each quad
- This might be used if testing and tuning specific QUADs to be used with specific hardened IP is necessary for future designs
- The default value of 156.25 MHz has already been programmed at the factory for the clock source. This mean the 8A34001 (U219).
- If a different frequency is desired, refer to the BoardUI programming tool as well as Renesas programming instructions.

Table: Transceiver Mapping

VPK120 XCVP1202 VSVA2785 GTY/GTM Mapping								
[Unused]	ch3	GTYP Quad 106 X0Y6	PCIe X0Y1			MRMAC X0Y1	GTM Quad 206 X0Y4	ch3	GTM SMA
[Unused]	ch2							ch2	8A34001 1PPS Clocks
[Unused]	ch1							ch1	[Unused]
[Unused]	ch0							ch0	[Unused]
[Unused]	refclk1							refclk1	8A34001 CLK6 IN
[Unused]	refclk0							refclk0	8A34001 Q7 OUT
PCIe Lane 0	ch3	GTYP Quad 105 X0Y5	CPM5			DCMAC X0Y0	GTM Quad 205 X0Y3	ch3	QSFPDD1 Lane 1
PCIe Lane 1	ch2							ch2	QSFPDD1 Lane 5
PCIe Lane 2	ch1							ch1	QSFPDD1 Lane 2
PCIe Lane 3	ch0							ch0	QSFPDD1 Lane 6
[Unused]	refclk1							refclk1	[Unused]
PCIe Edge Clock 0	refclk0							refclk0	8A34001 Q8 BUF0
PCIe Lane 4	ch3	GTYP Quad 104 X0Y4	CPM5 (HSDP)				GTM Quad 204 X0Y2	ch3	QSFPDD1 Lane 3
PCIe Lane 5	ch2							ch2	QSFPDD1 Lane 7
PCIe Lane 6	ch1							ch1	QSFPDD1 Lane 4
PCIe Lane 7	ch0							ch0	QSFPDD1 Lane 8
[Unused]	refclk1							refclk1	8A34001 CLK5 IN MUX1
PCIe Edge Clock 1	refclk0							refclk0	8A34001 Q8 BUF1

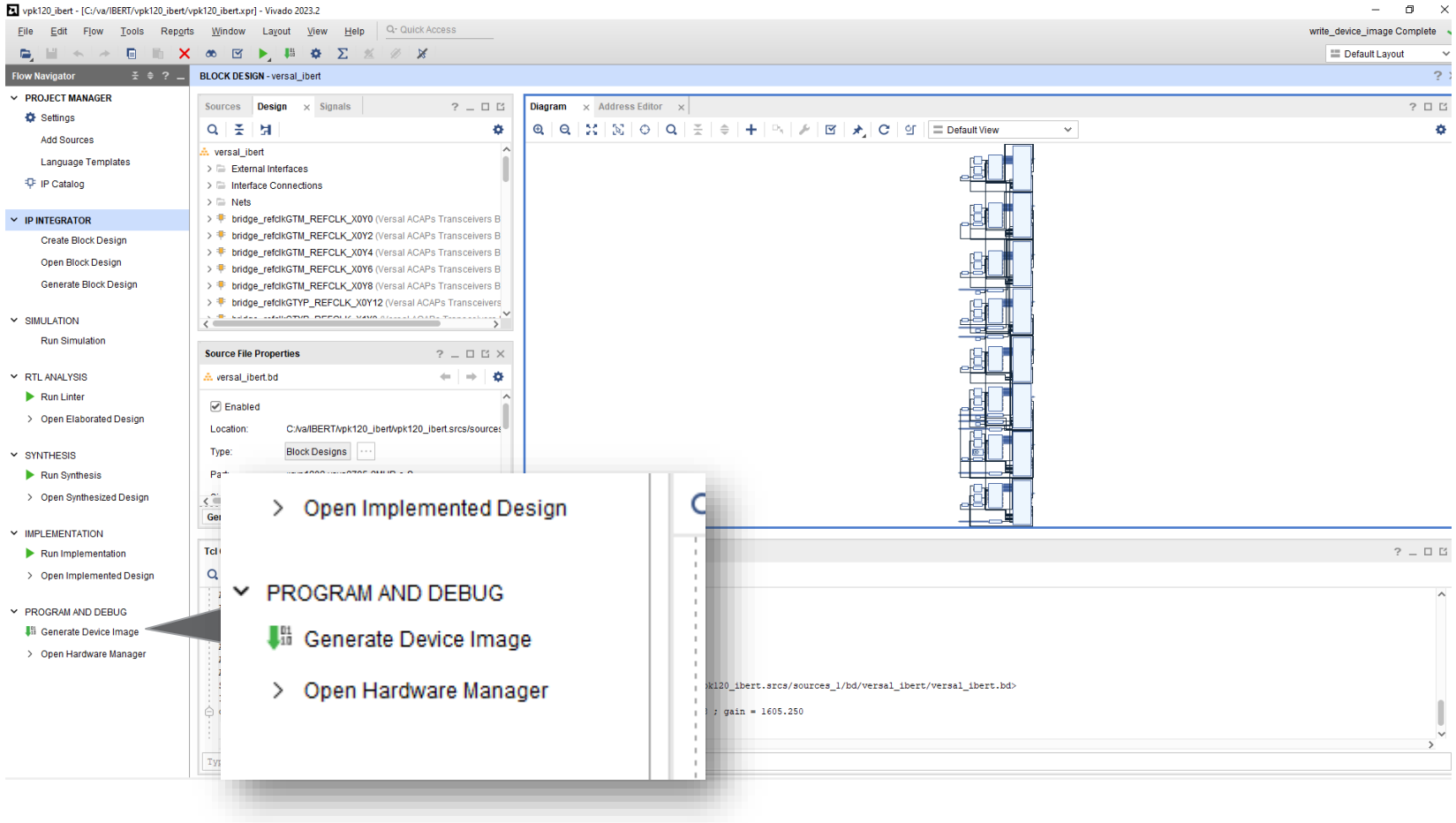
Board Component Location

Ensure the included loopback adapter (Multilane ML4062-LB-112) is inserted and FULLY seated in the QSFPDD-1 (J3) cage / connector(If you are using the official PDI file provided in RDF0636,)



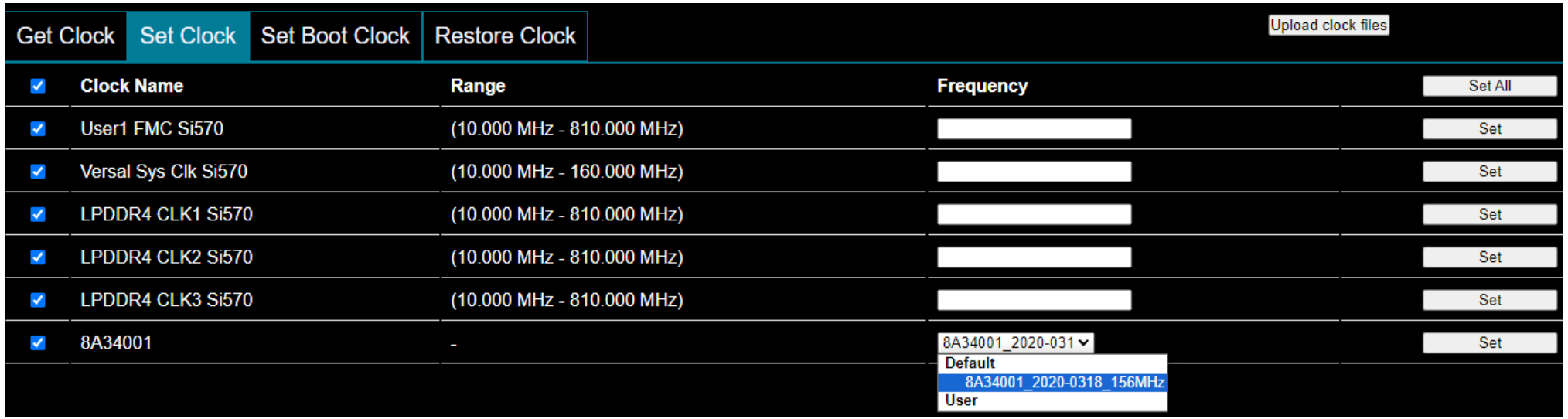
Generate Device Image

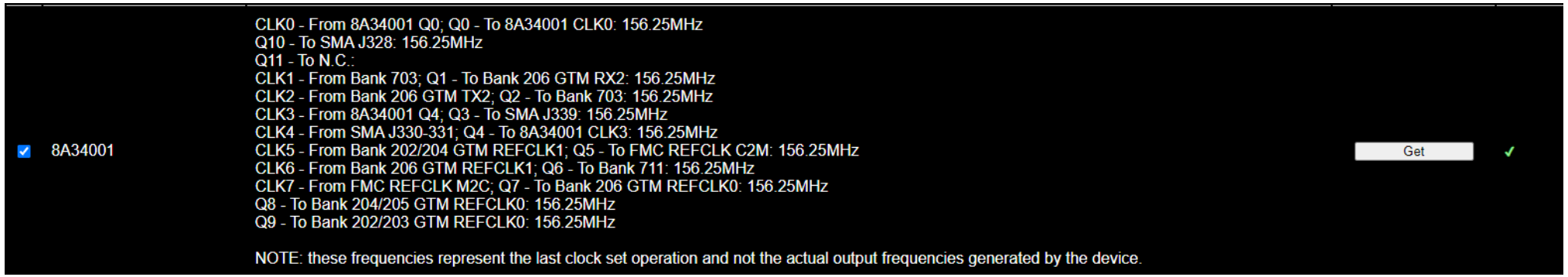
Once the project is initialized, as mentioned in the beginning overview, now is the time to review settings, by opening the Block Design and then opening the details of the various IP generated for you
Once satisfied, or if you do not wish to review, select Generate Device Image from the Flow Navigator



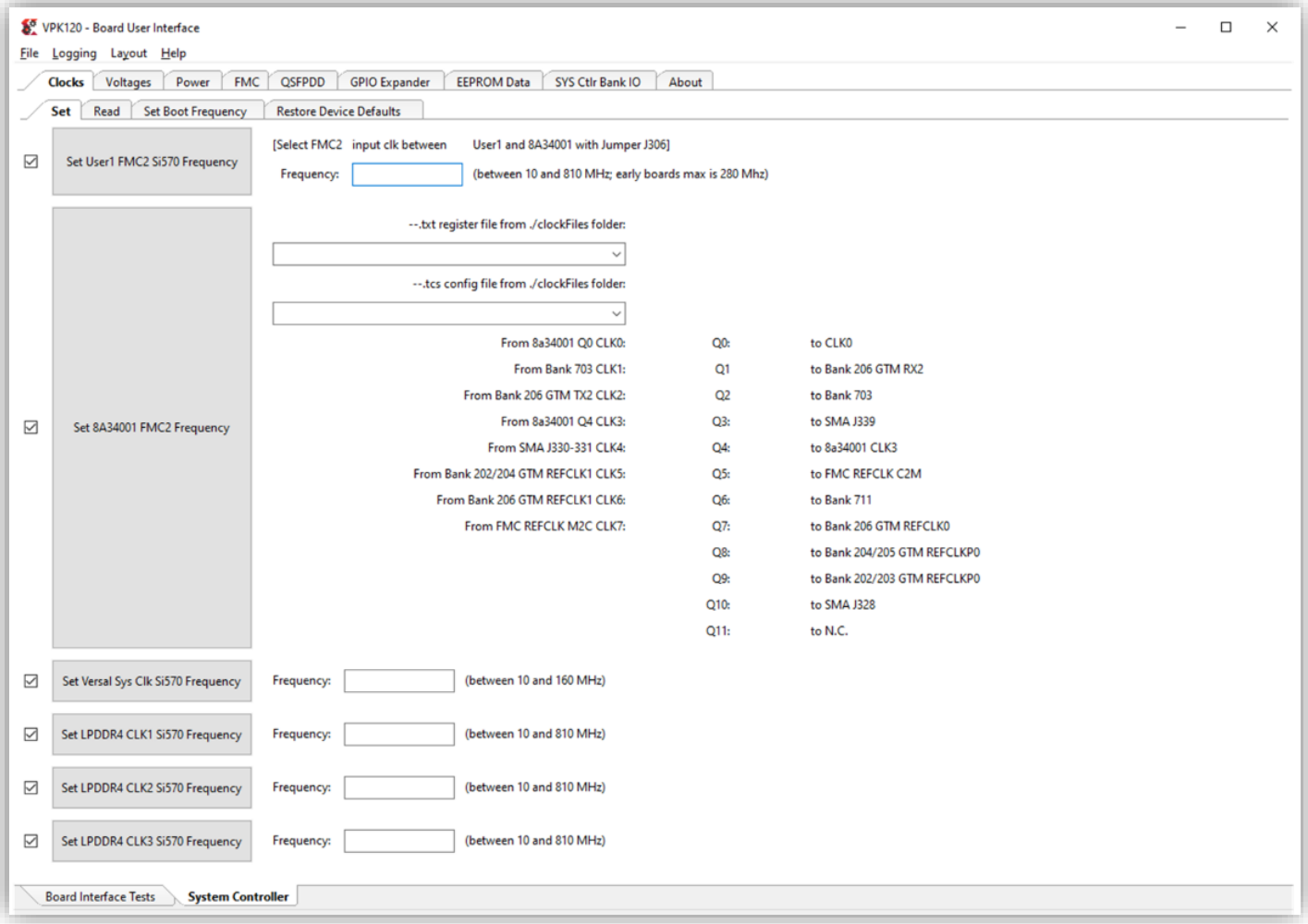
Modify Refclk Frequency

Before programming, it is necessary to adjust the frequency of 8A34001 to 156.25.
You can use either BoardUI or BEAM to utilize the System Controller for adjustment.





Modify Refclk Frequency



A brief summary is provided here.

1. Ensure the Skyworks/Silicon Labs VCP USB-UART drivers are installed. See the *Silicon Labs CP210x USB-to-UART Installation Guide* (UG1033).

2. Download the board user interface host PC application from the VPK120 Evaluation Board website.

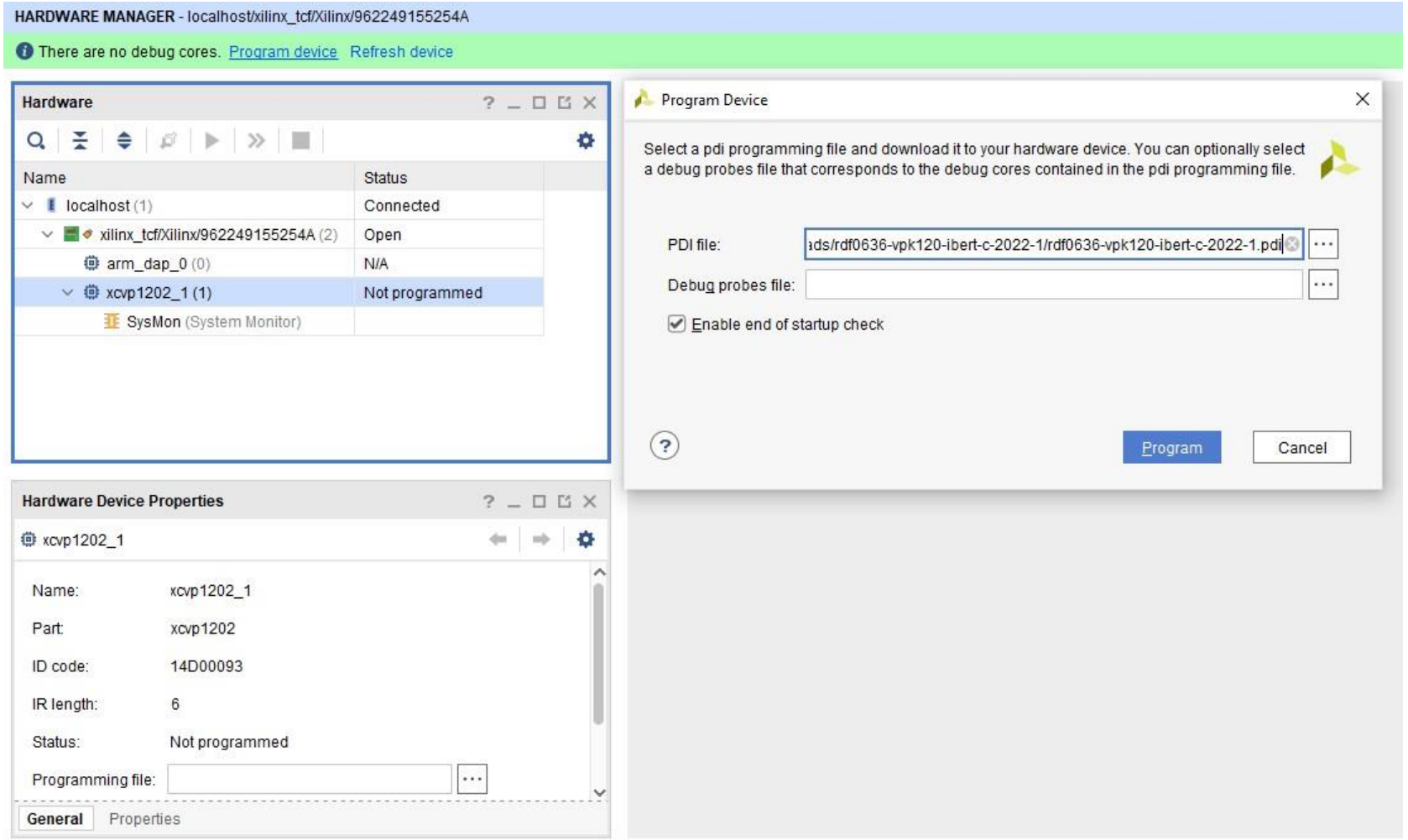
3. Connect a USB cable to VPK120 USB-UART USB-A connector (J344).

4. Power-cycle the VPK120.

5. Launch the board user interface application.

Program Device

If you are programming the prebuilt PDI, select the file here and program.
Once completed, the IBERT Real-Time Scan Plots are opened

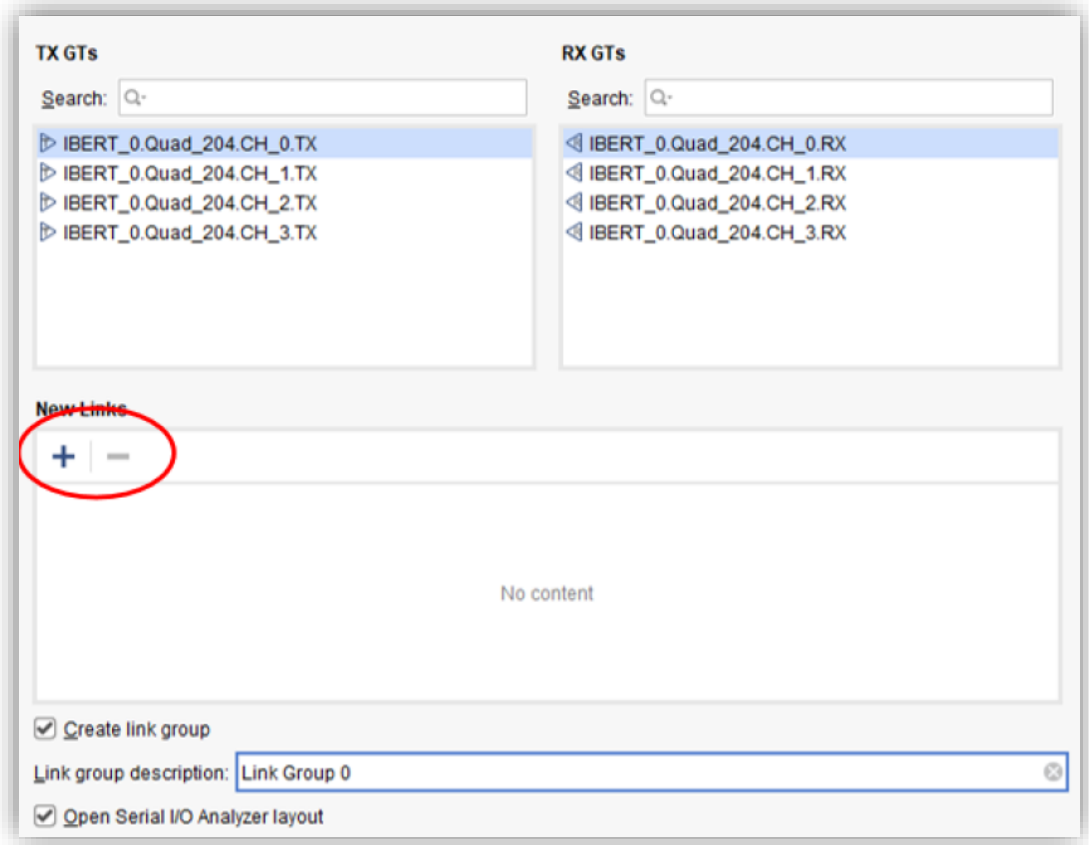


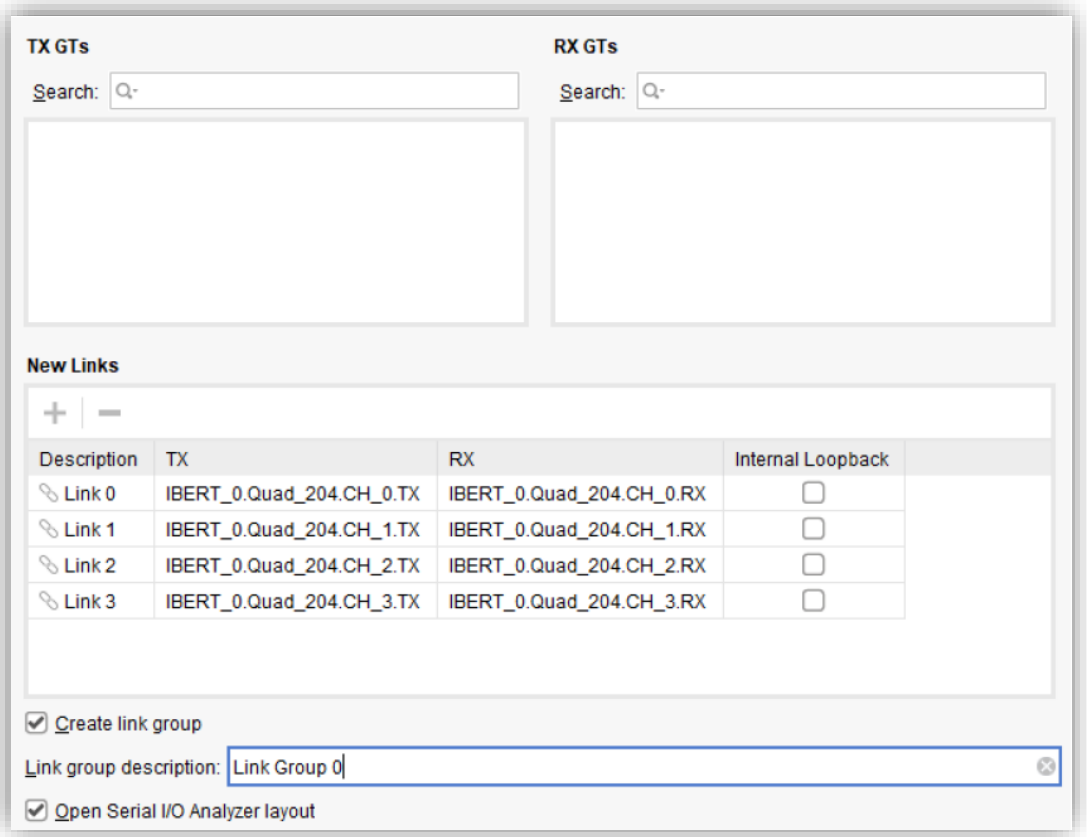
Create Links

In the Serial I/O Links tab, select Create Links.

Note: Depending on configuration, it can be prohibitively long to run “Auto-detect links”

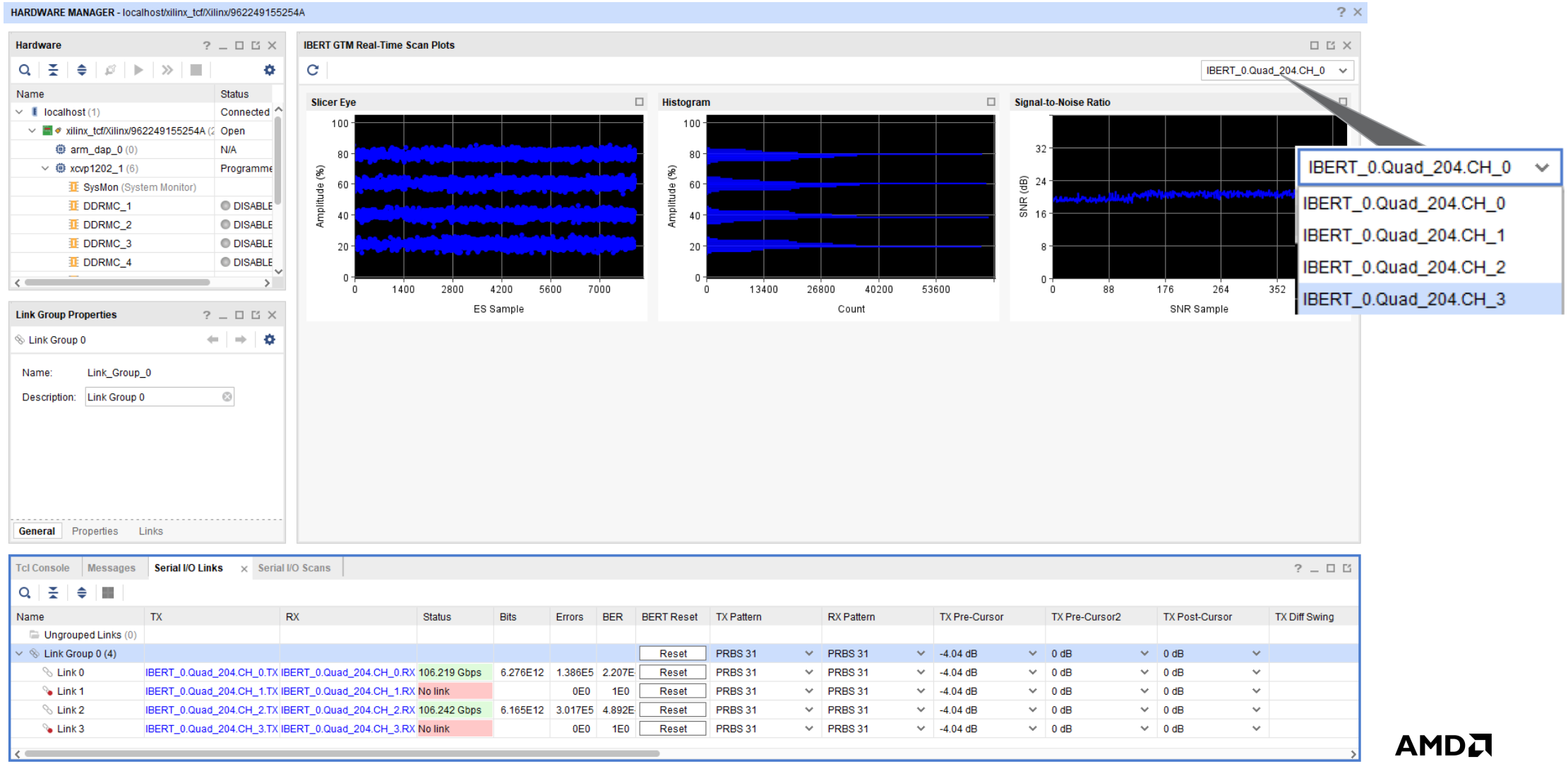
- In the following pop-up dialog, select a 1:1 for each channel such that the New Links area is populated as shown. This is done by clicking the large + while you have two channels selected





Versal IBERT View

Using this, you can view each individual channel's plots.



PLL Status

- Verify is that the PLLS are locked. Scroll the tab to the right and locate the PLL columns

- If the PLL does not show lock, please review whether the refclk is set correctly.

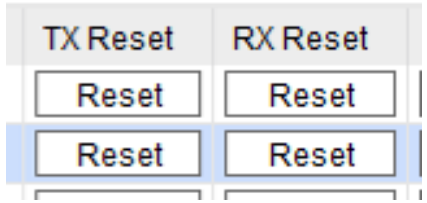
RX PLL Status	TX PLL Status
Locked	Locked
Locked	Locked
Locked	Locked
Locked	Locked

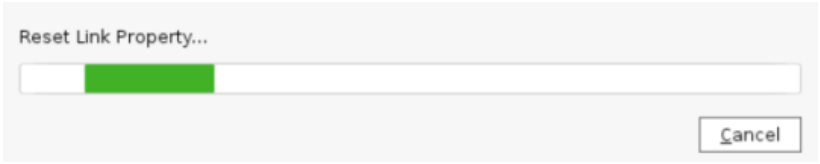
Parameter adjustment.

For the VPK120, example performance tuning has been completed and it is suggested to change the TX Pre-Cursor, TX Pre-Cursor2, TX Post-Cursor and TX Main-Cursor for Link 0 as suggested in the following image

TX Pre-Cursor	TX Pre-Cursor2	TX Post-Cursor	TX Main-Cursor
Multiple	Multiple	Multiple	Multiple
-4.04 dB	0 dB	0 dB	0.998 Vdd
User Design	User Design	User Design	User Design
User Design	User Design	User Design	User Design
User Design	User Design	User Design	User Design

As these are critical tunes, we will now need to reset the link





Appendix

Appendix

Versal Evaluation Board - System Controller

https://xilinx-wiki.atlassian.net/wiki/spaces/A/pages/2273738753/Versal+Evaluation+Board+-+System+Controller

VPK120 Evaluation Board User Guide (UG1568)

https://docs.xilinx.com/r/en-US/ug1568-vpk120-eval-bd/Additional-Resources-and-Legal-Notices

RDF0636 - VPK120 IBERT Example Design

https://www.xilinx.com/products/boards-and-kits/vpk120.html#resources