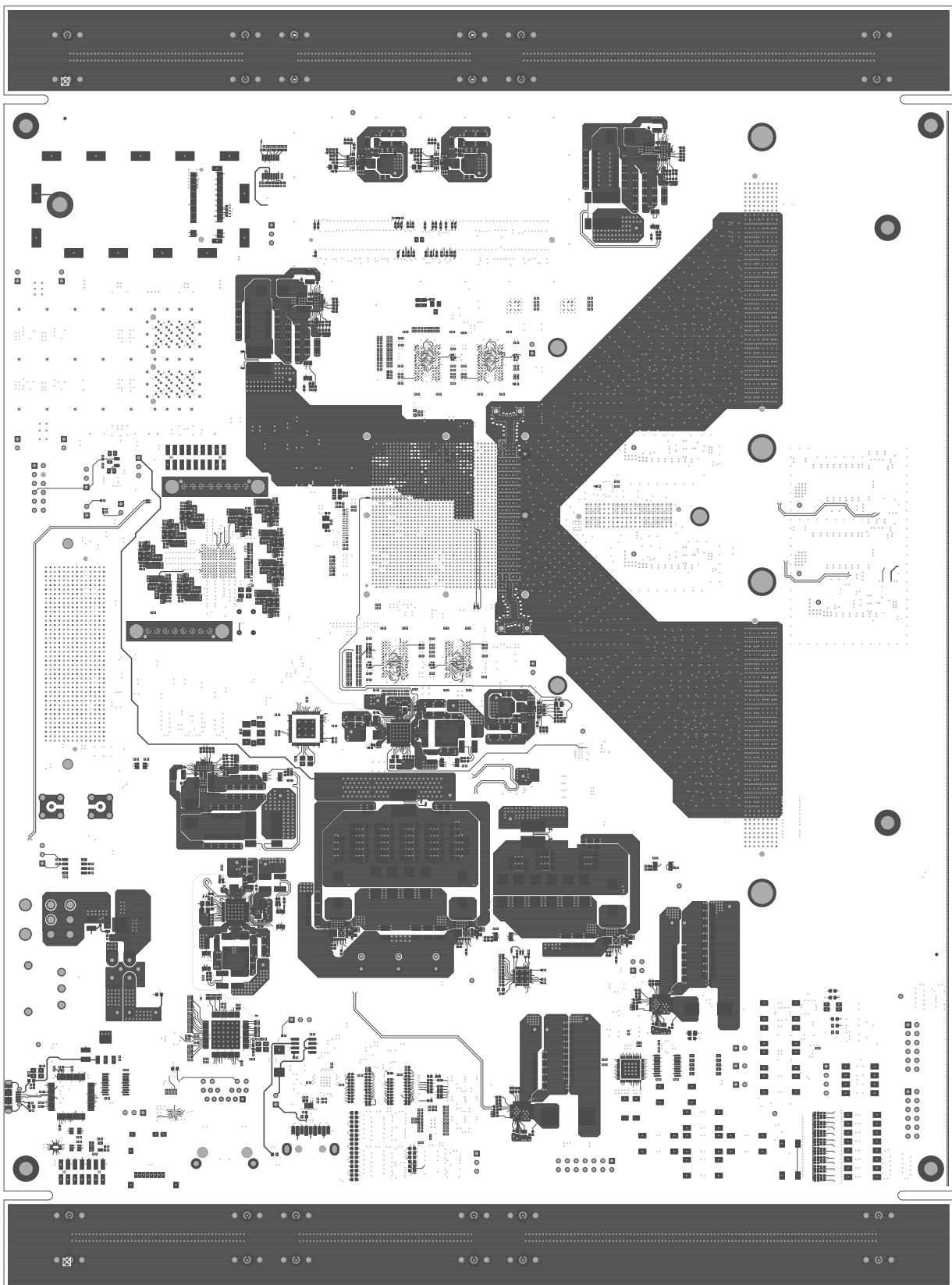
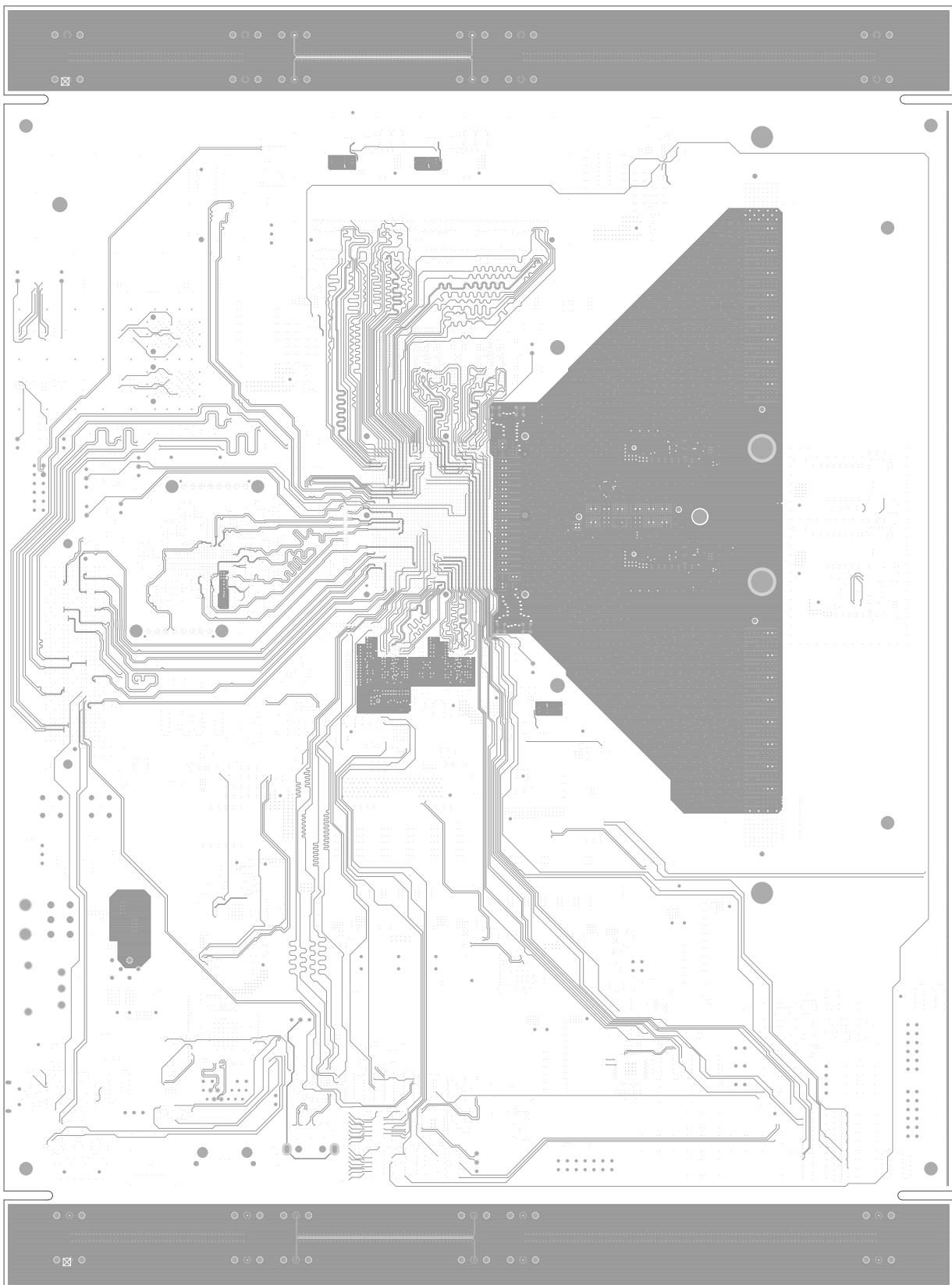


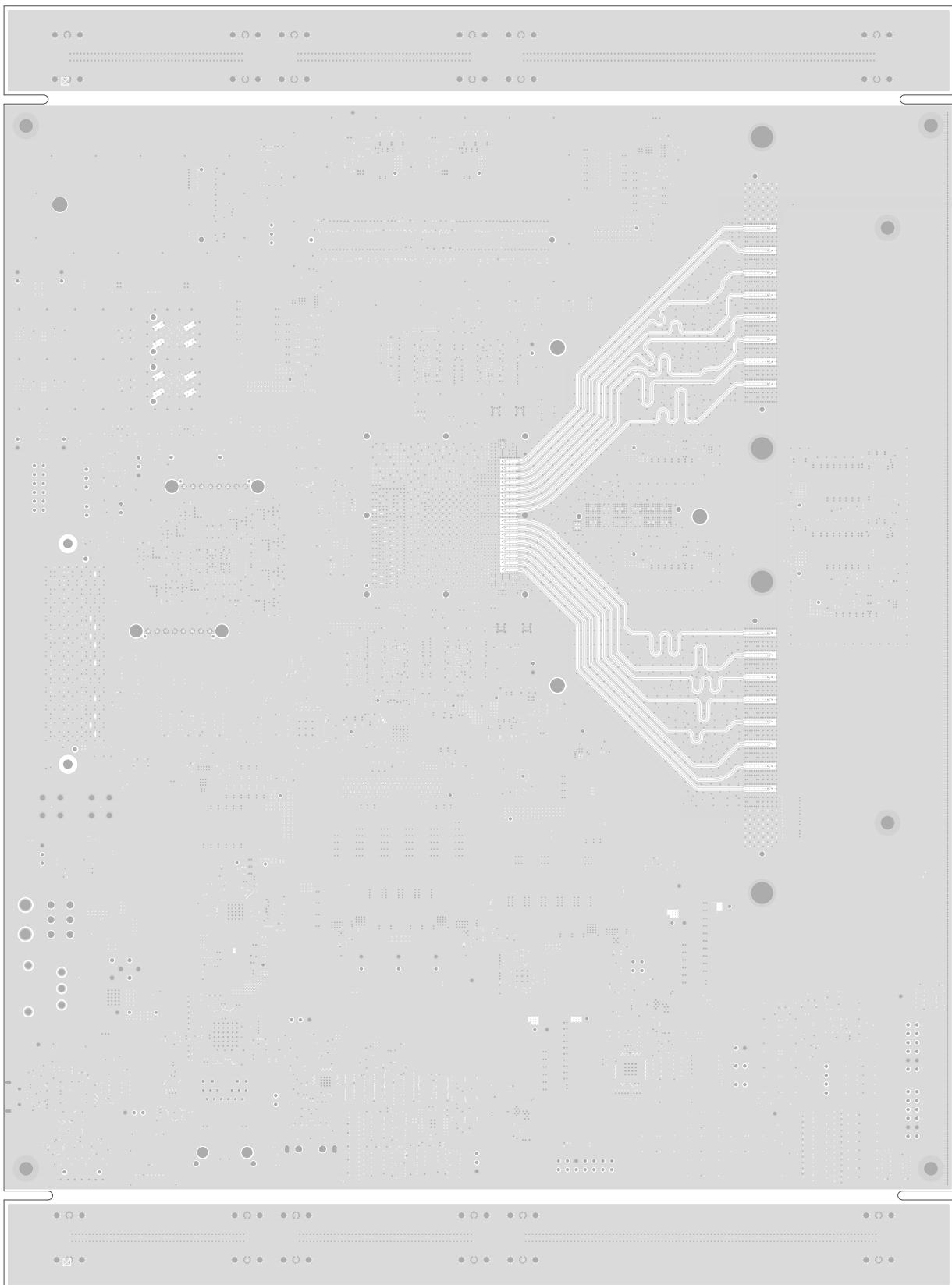
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB # 128-05003-01	LAYER: L2_GND_RF_SIG
Designed by Xilinx	DATE: 10/18/2019
BOARD designer: CAROL	PHONE: 408-879-4993
Z	XILINX DOC USE ONLY REVISION-A02 Version aa



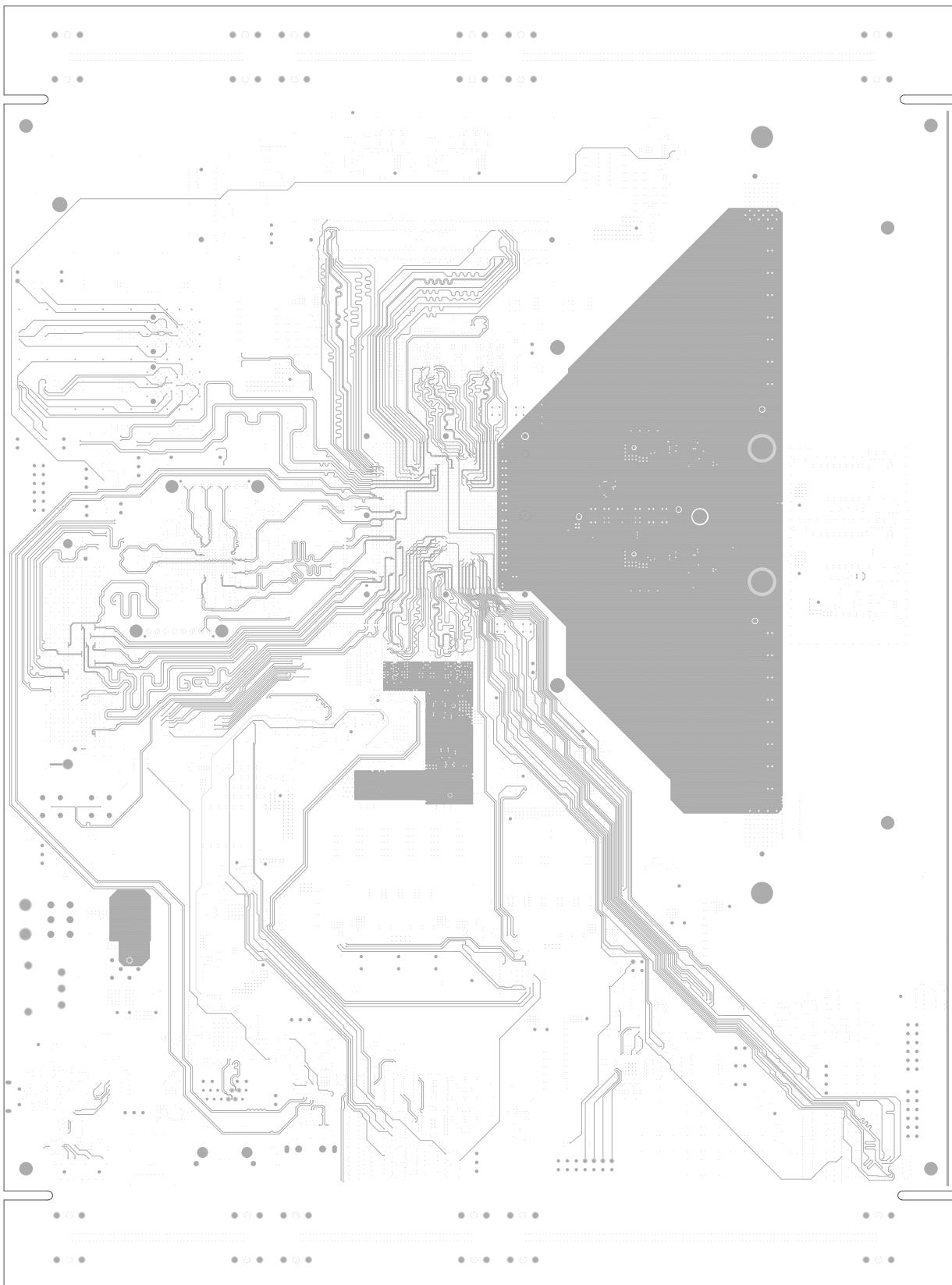
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB # 128-05003-01	LAYER: L1_TOP
Designed by Xilinx	DATE: 10/18/2019
BOARD designer: CAROL	PHONE: 408-879-4993
XILINX DOC USE ONLY	
REVISION-A02 Version aa	



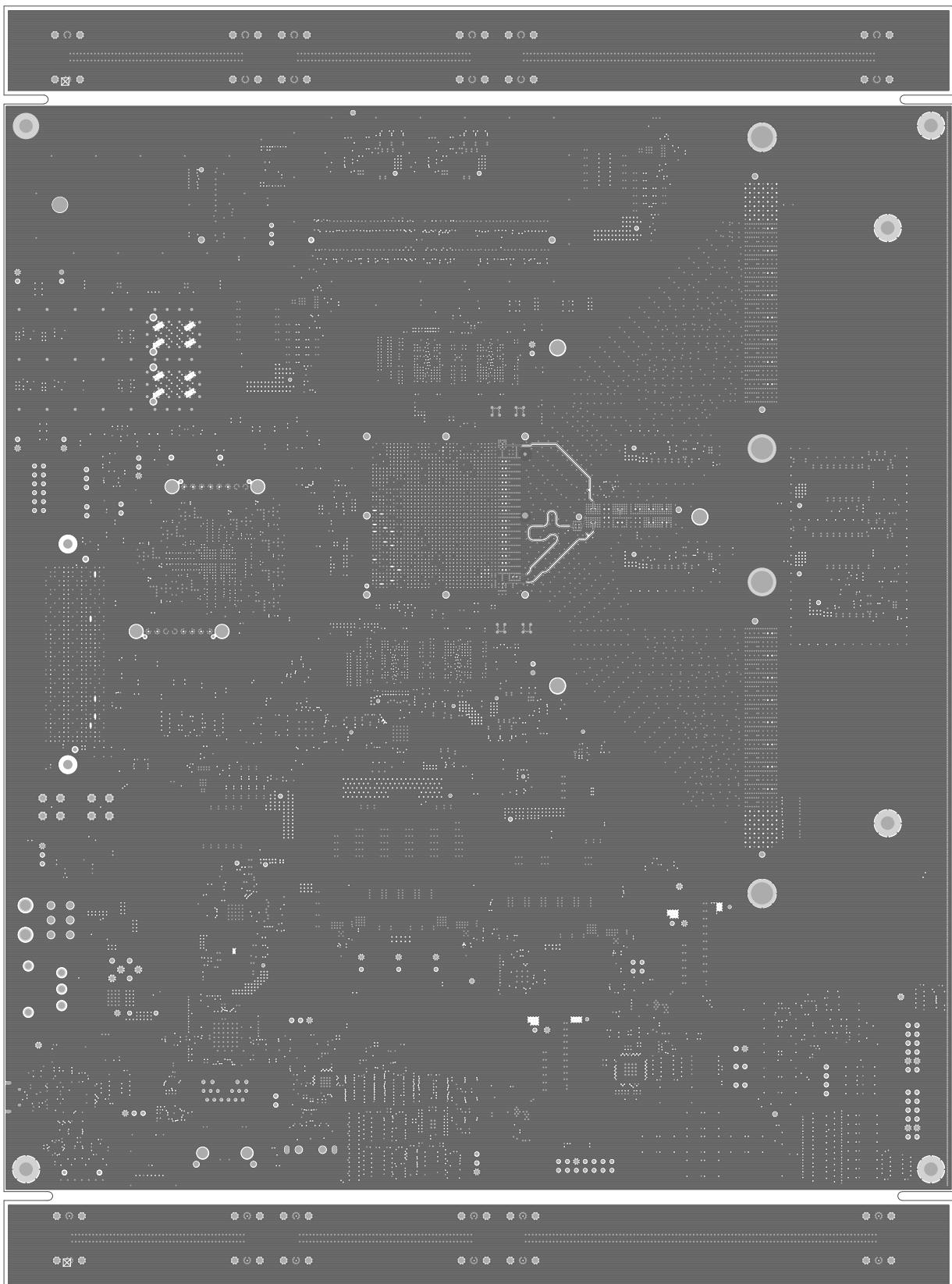
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PCB # 128-05003-01	LAYER: L3_SIG_RF_GND
Designed by Xilinx	DATE: 10/18/2019
BOARD designer: CAROL	PHONE: 408-879-4993
	XILINX DOC USE ONLY
3	REVISION-A02 Version aa



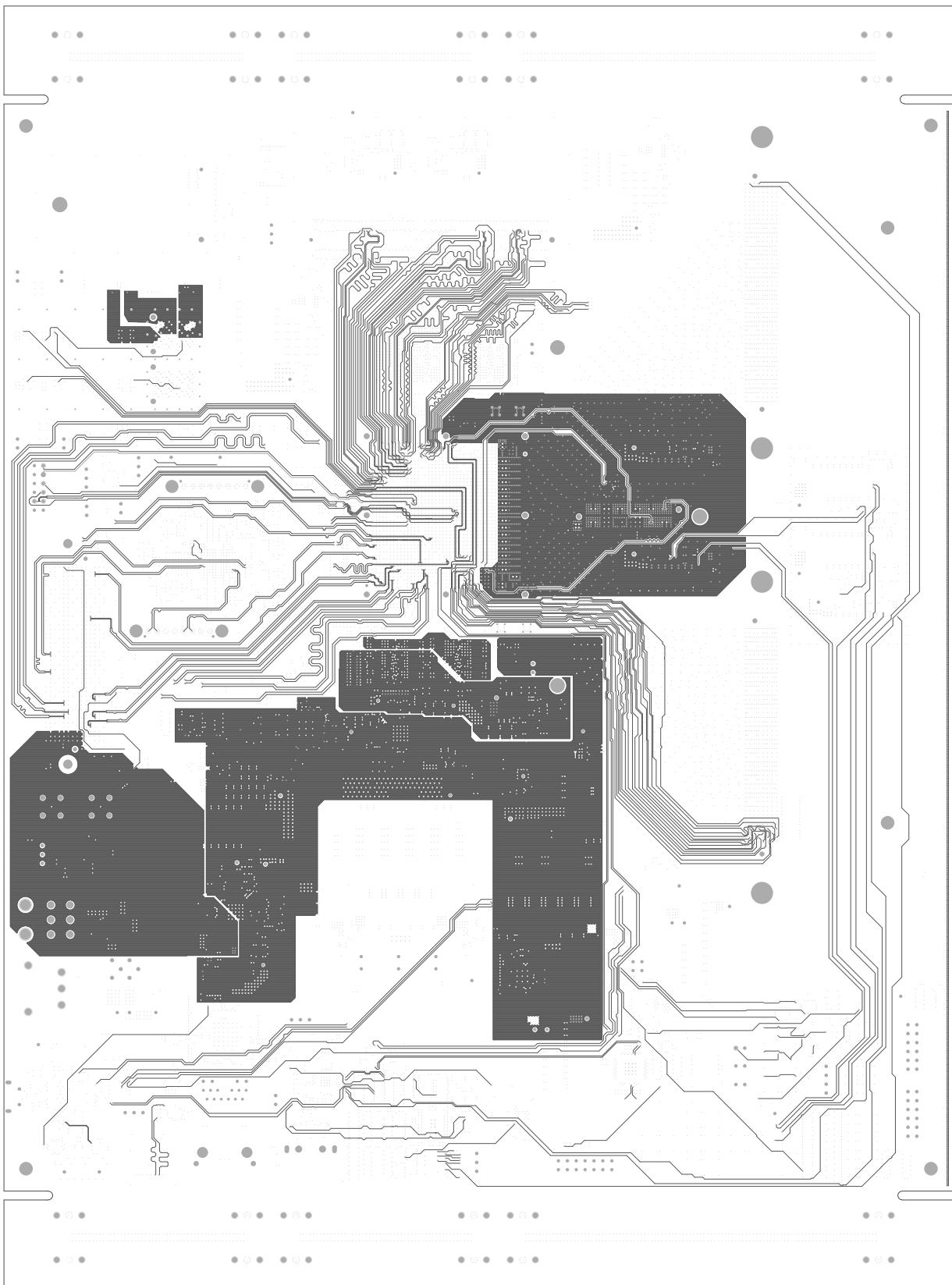
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PCB # 128-05003-01	LAYER: L4_GND_RF_SIG
Designed by Xilinx	DATE: 10/18/2019
BOARD designer: CAROL	PHONE: 408-879-4993
4	XILINX DOC USE ONLY REVISION-A02 Version aa



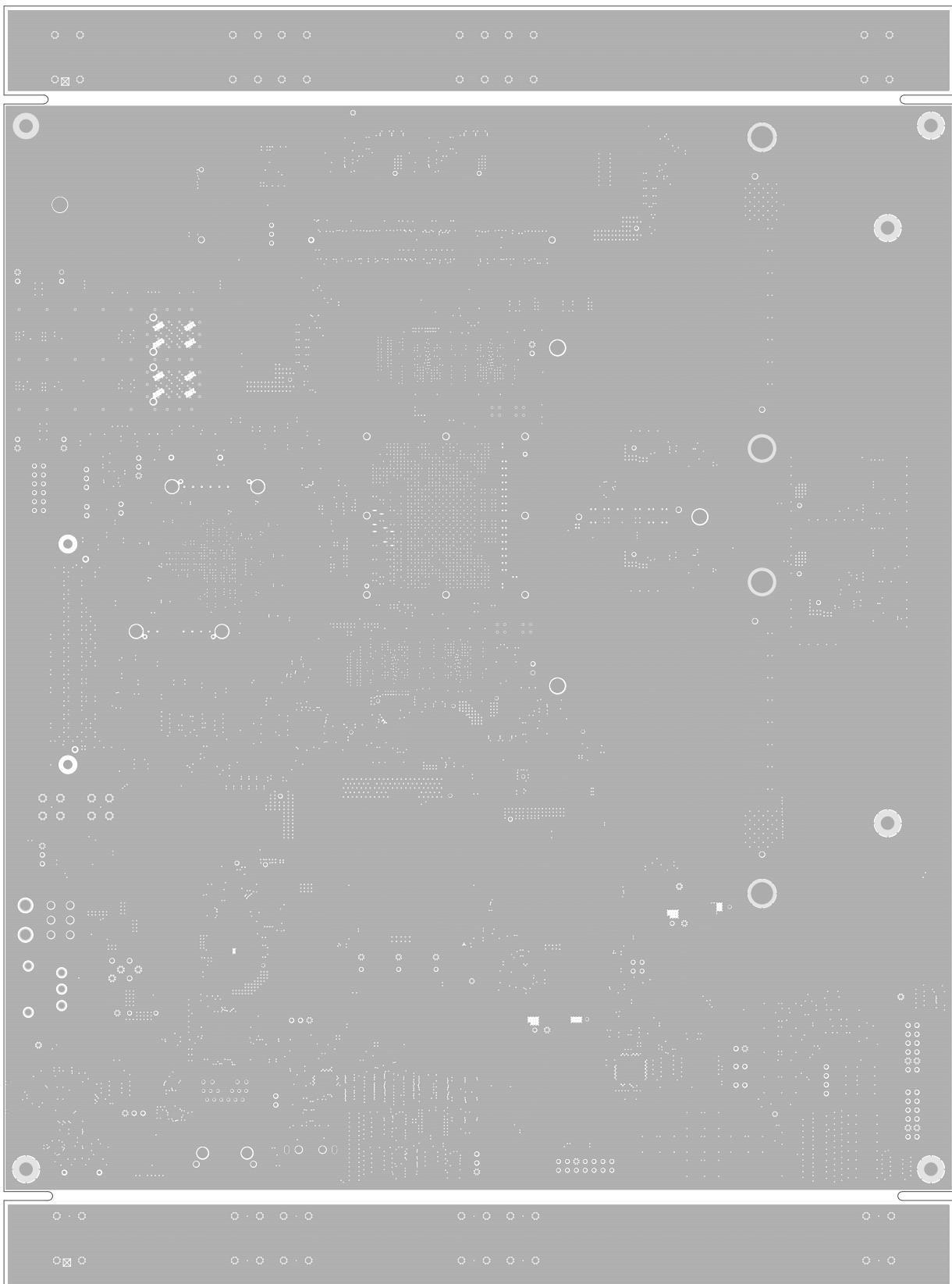
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB #	128-05003-01
Designed by	Xilinx
BOARD designer:	CAROL
5	XILINX DOC USE ONLY REVISION-A02 Version aa
LAYER:	L5_S1G_RF_GND
DATE:	10/18/2019
PHONE:	408-879-4993



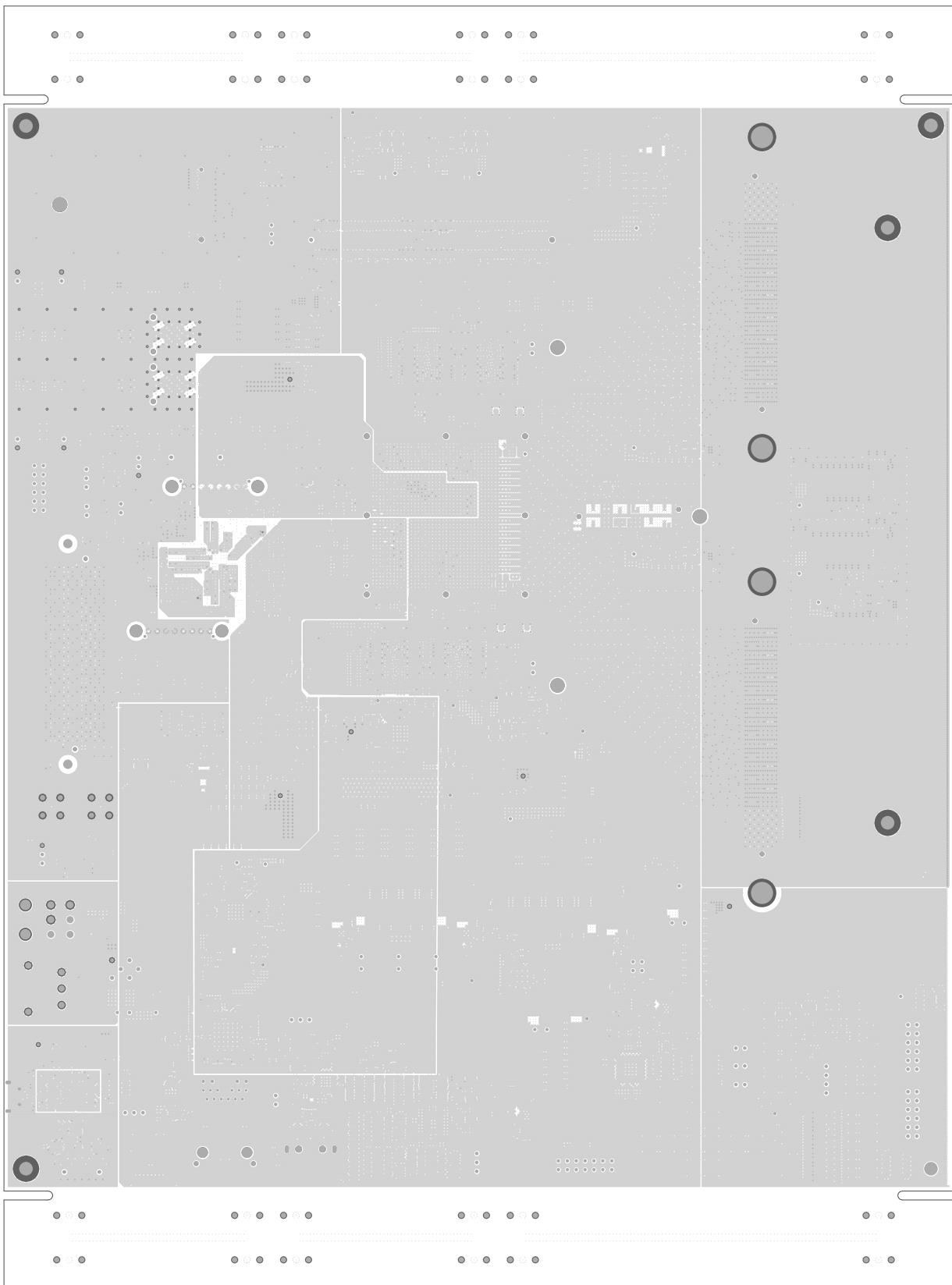
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB #	128-05003-01
LAYER:	L6_GND_RF_SIG
Designed by	Xilinx
DATE:	10/18/2019
BOARD designer:	CAROL
PHONE:	408-879-4993
	XILINX DOC USE ONLY
6	REVISION-A02 Version aa



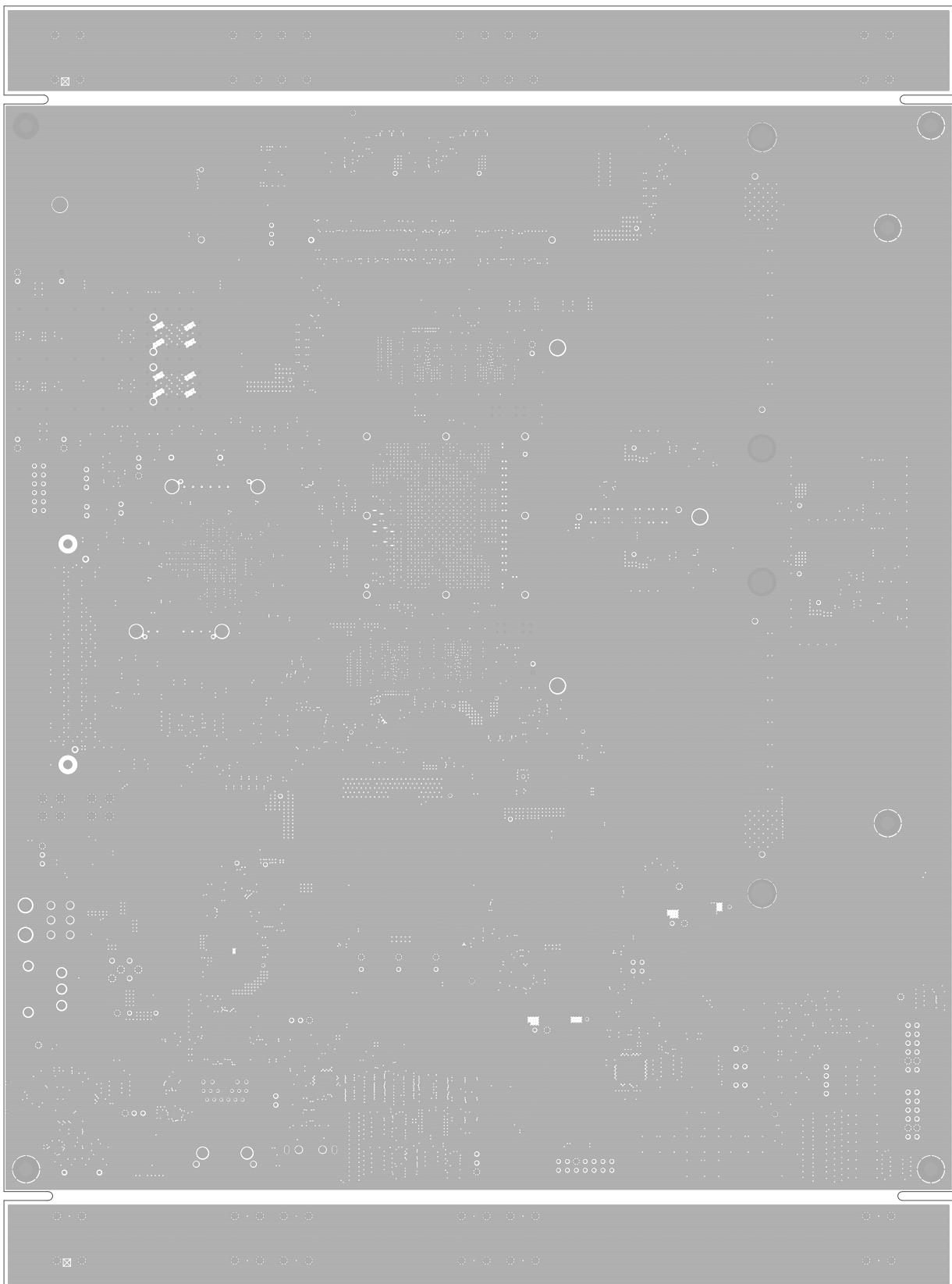
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB #	128-05003-01
Designed by	Xilinx
BOARD designer:	CAROL
DATE:	10/18/2019
PHONE:	408-879-4993
LAYER:	L7_SIG_RF_GND
7	XILINX DOC USE ONLY
REVISION-A02 Version aa	



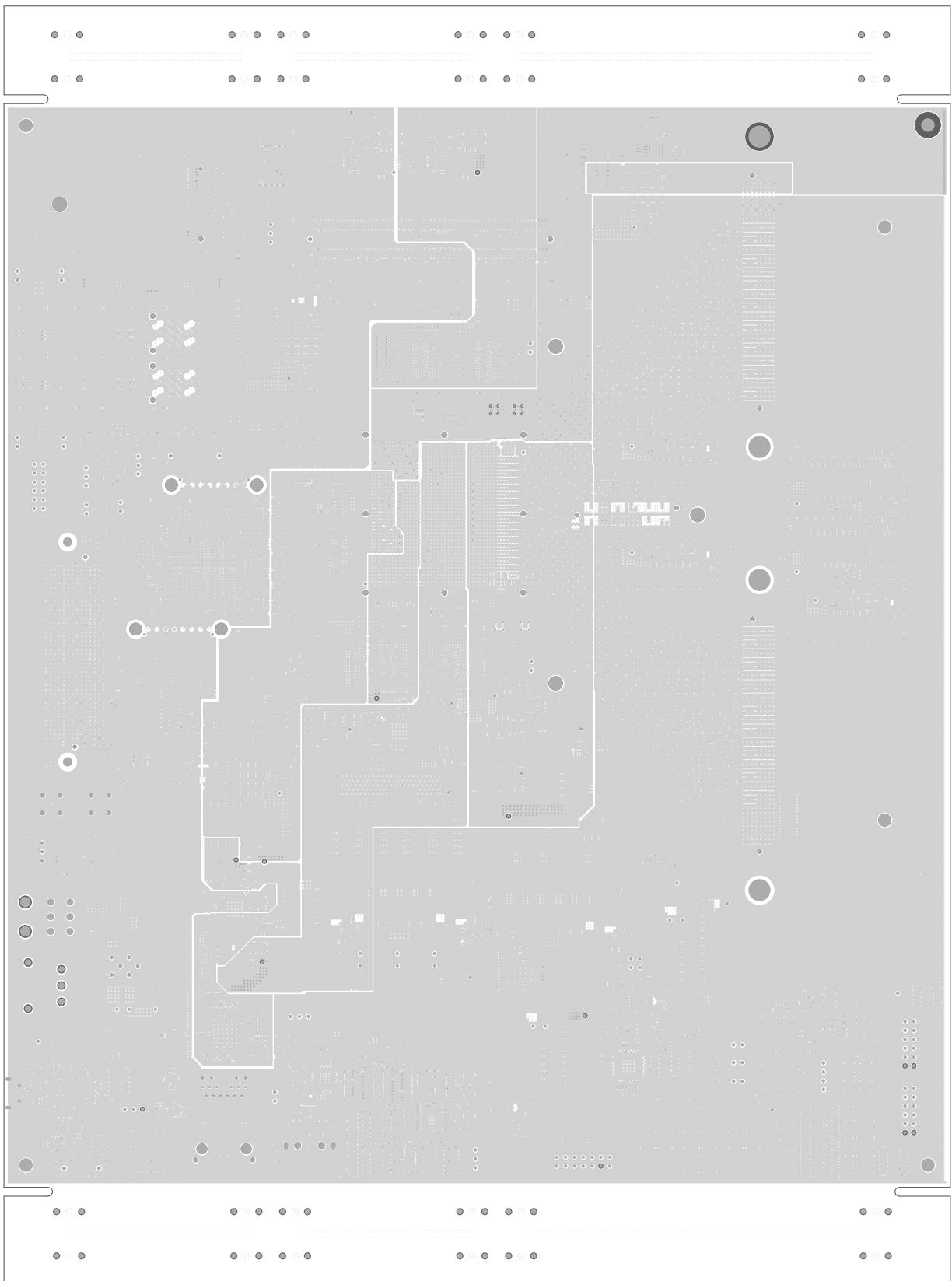
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB #	128-05003-01
LAYER:	L8_GND
Designed by	Xilinx
DATE:	10/18/2019
BOARD designer:	CAROL
PHONE:	408-879-4993
8	XILINX DOC USE ONLY
	REVISION-A02 Version aa



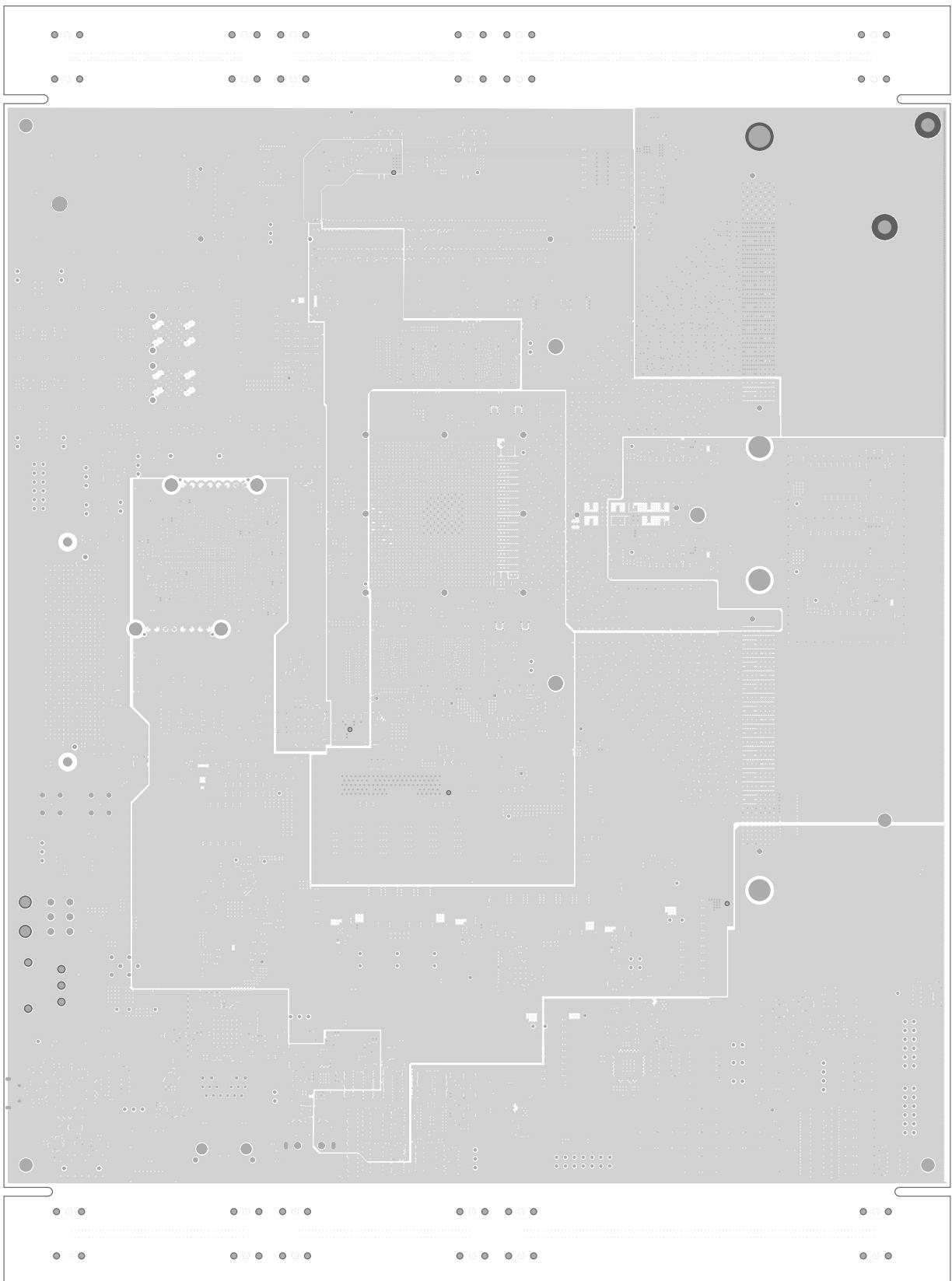
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PCB #	128-05003-01
Designed by	Xilinx
BOARD designer:	CAROL
DATE:	10/18/2019
PHONE:	408-879-4993
XILINX DOC USE ONLY	
REVISION-A02 Version aa	



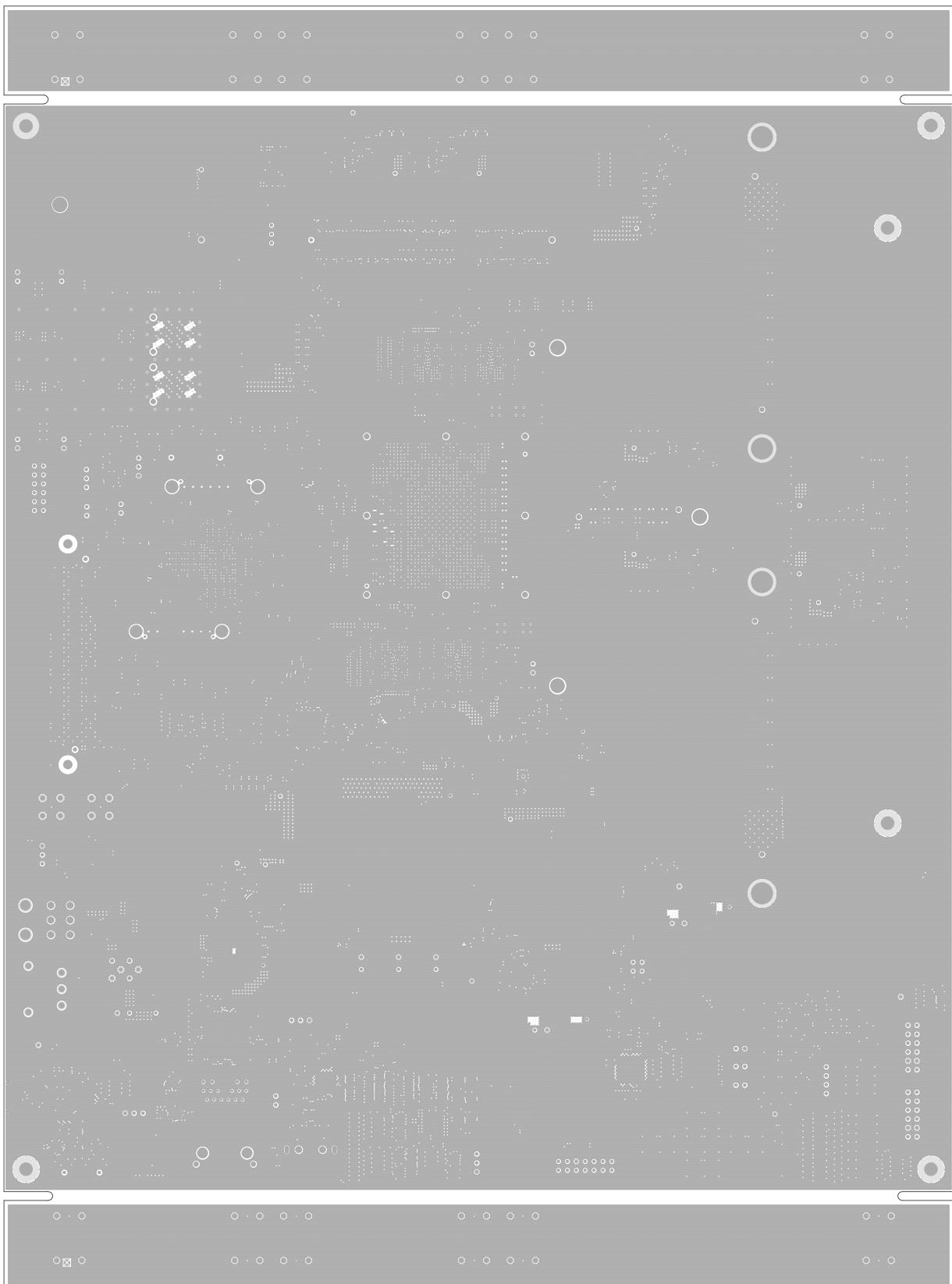
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PCB #	128-05003-01
LAYER:	L10_GND
Designed by	Xilinx
DATE:	10/18/2019
BOARD designer:	CAROL
PHONE:	408-879-4993
10	XILINX DOC USE ONLY
	REVISION-A02 Version aa



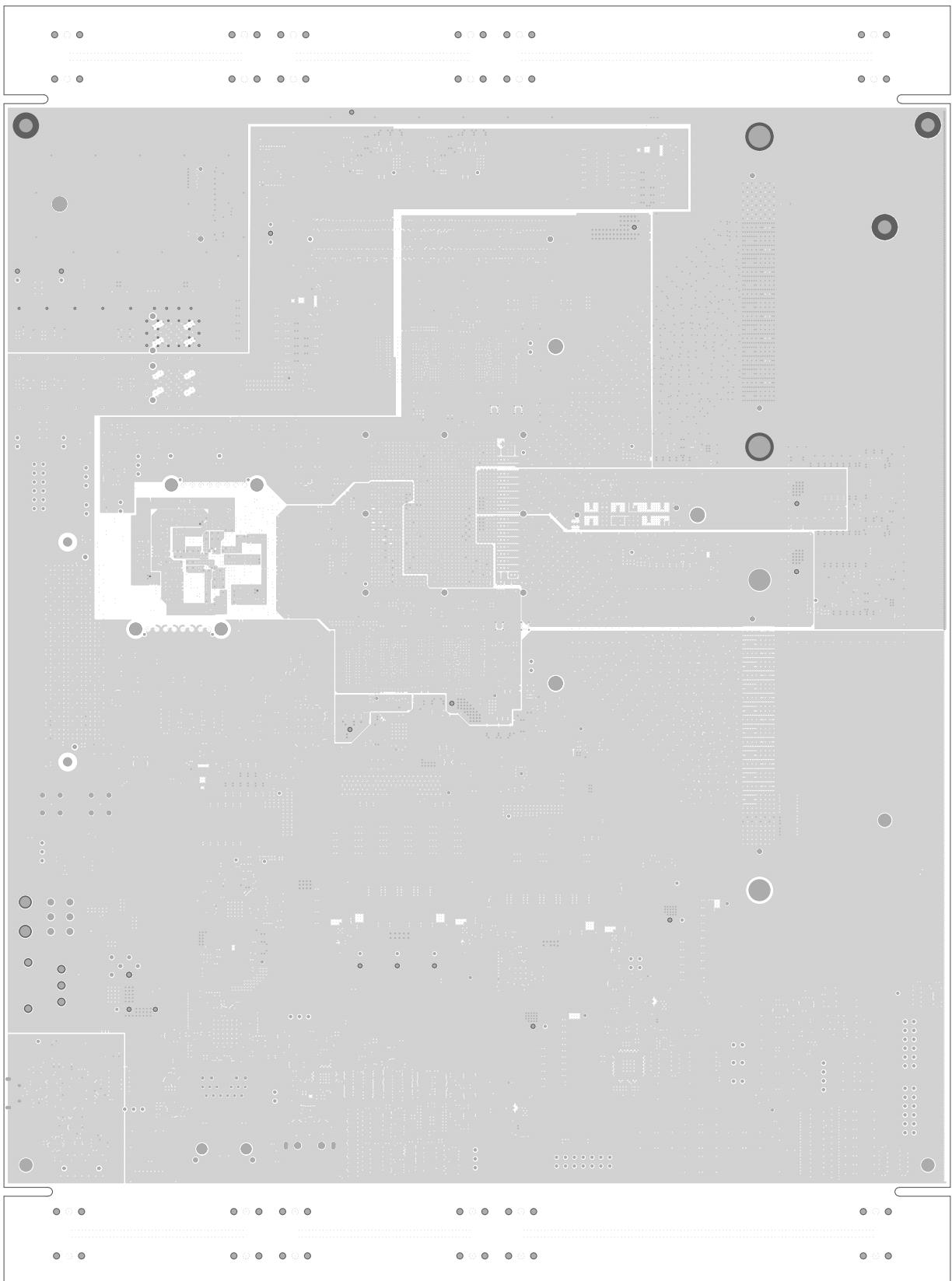
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Designed by	Xilinx
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DATE:	10/18/2019
PHONE:	408-879-4993
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REVISION-A02 Version aa	



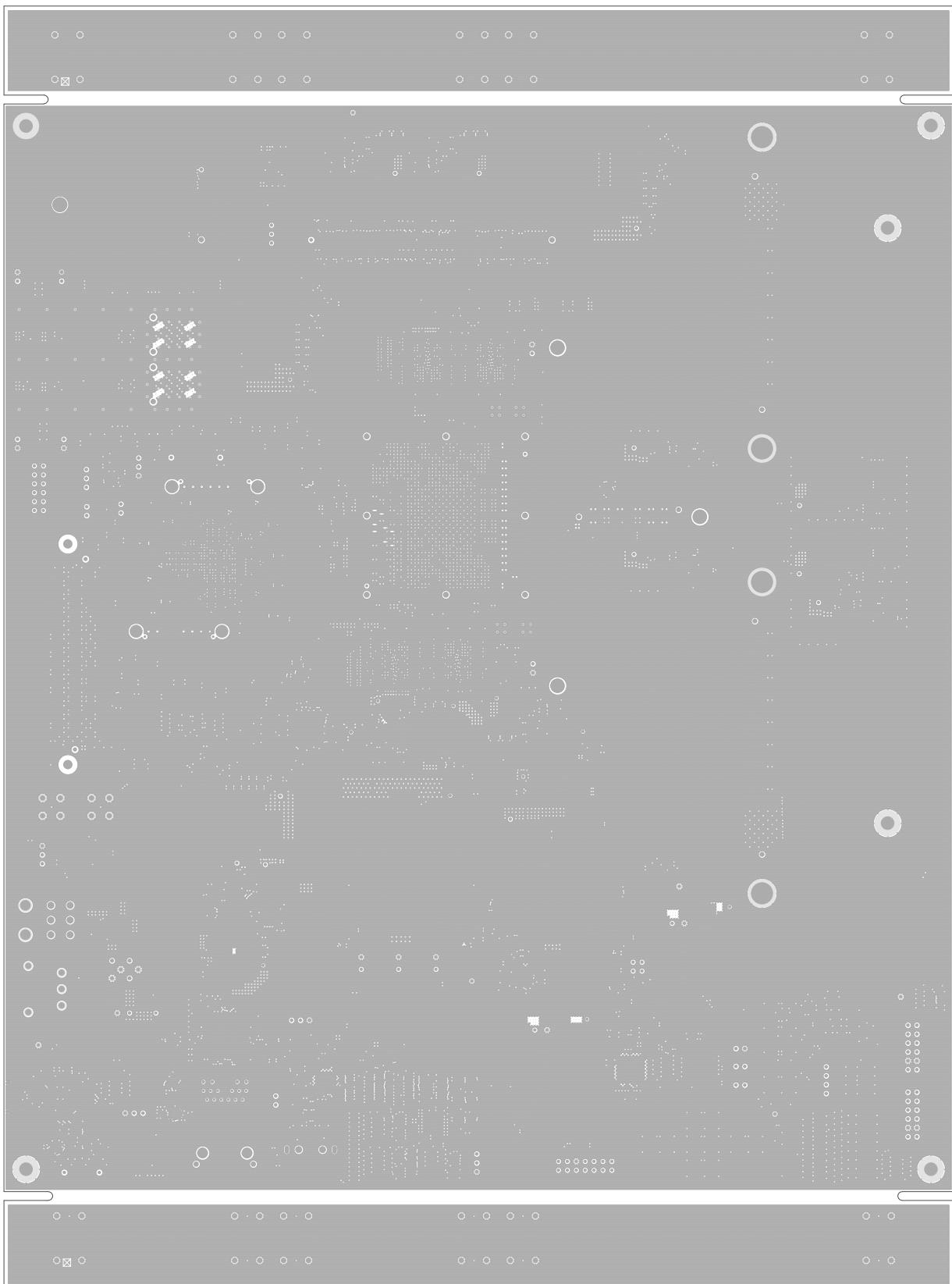
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PCB #	128-05003-01
Designed by	Xilinx
BOARD designer:	CAROL
DATE:	10/18/2019
PHONE:	408-879-4993
12	XILINX DOC USE ONLY
	REVISION-A02 Version aa



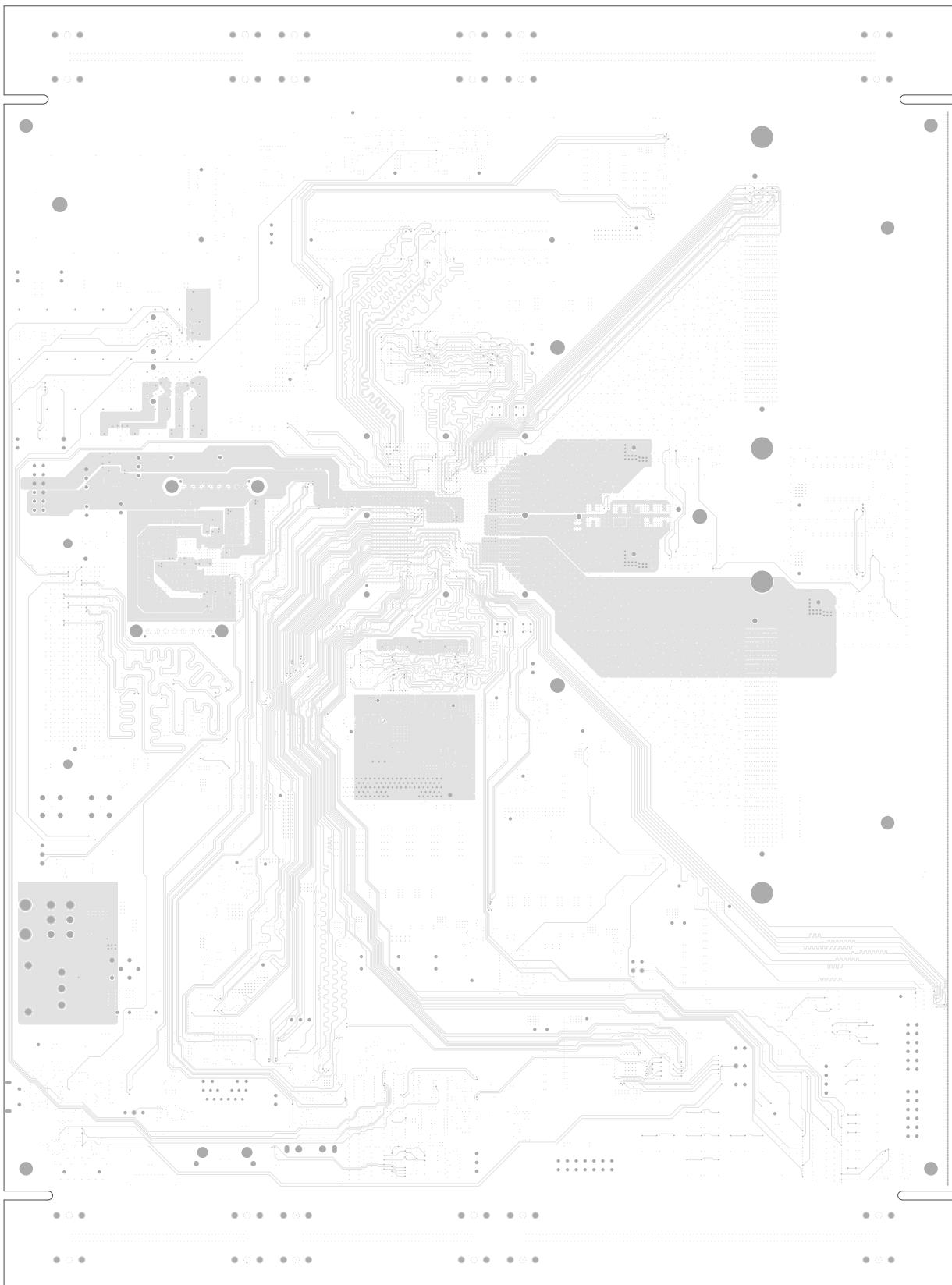
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB #	128-05003-01
LAYER:	L13_GND
Designed by	Xilinx
DATE:	10/18/2019
BOARD designer:	CAROL
PHONE:	408-879-4993
13	XILINX DOC USE ONLY REVISION-A02 Version aa



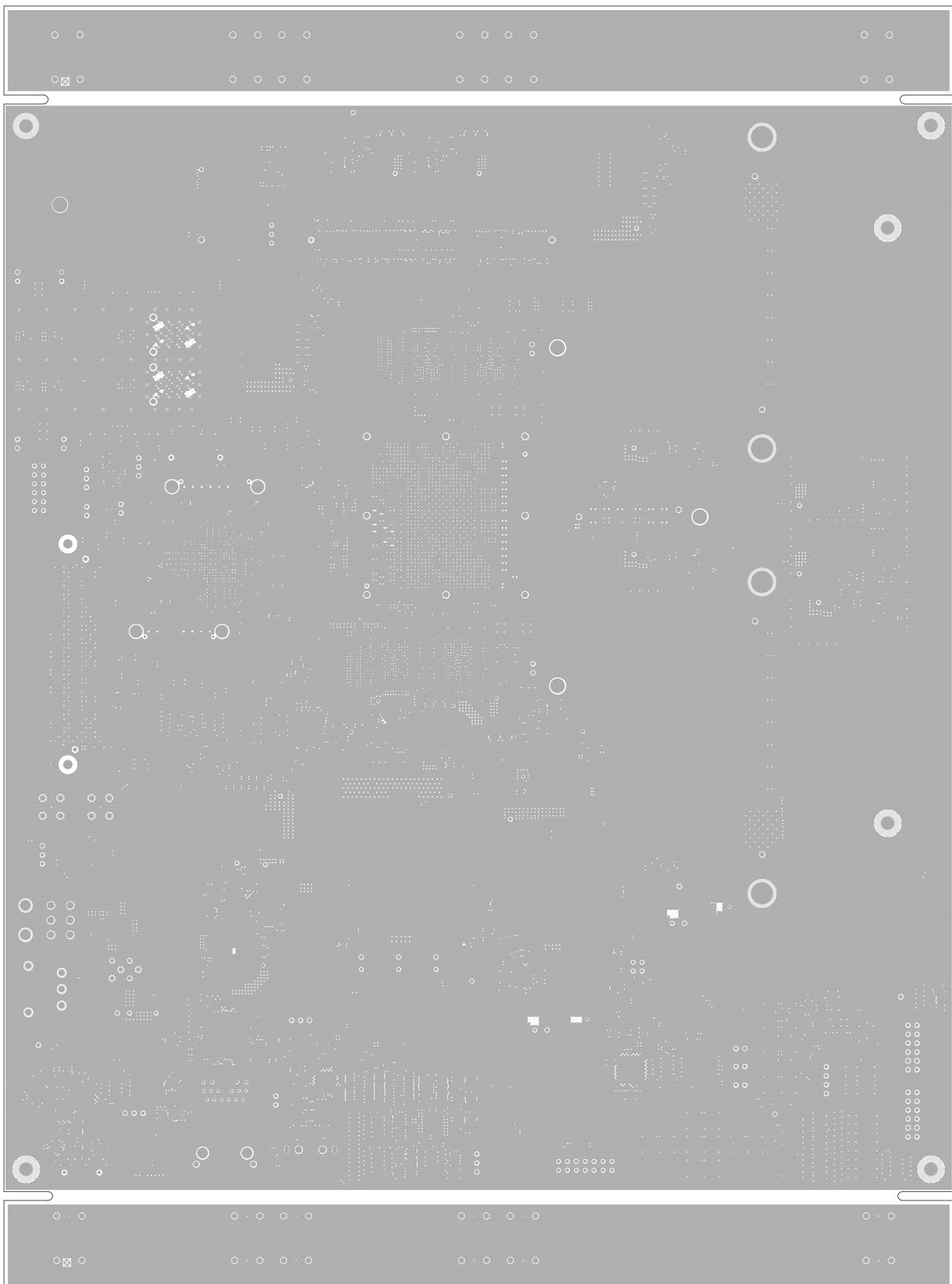
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB #	128-05003-01
Designed by	Xilinx
BOARD designer:	CAROL
DATE:	10/18/2019
PHONE:	408-879-4993
14	XILINX DOC USE ONLY REVISION-A02 Version aa



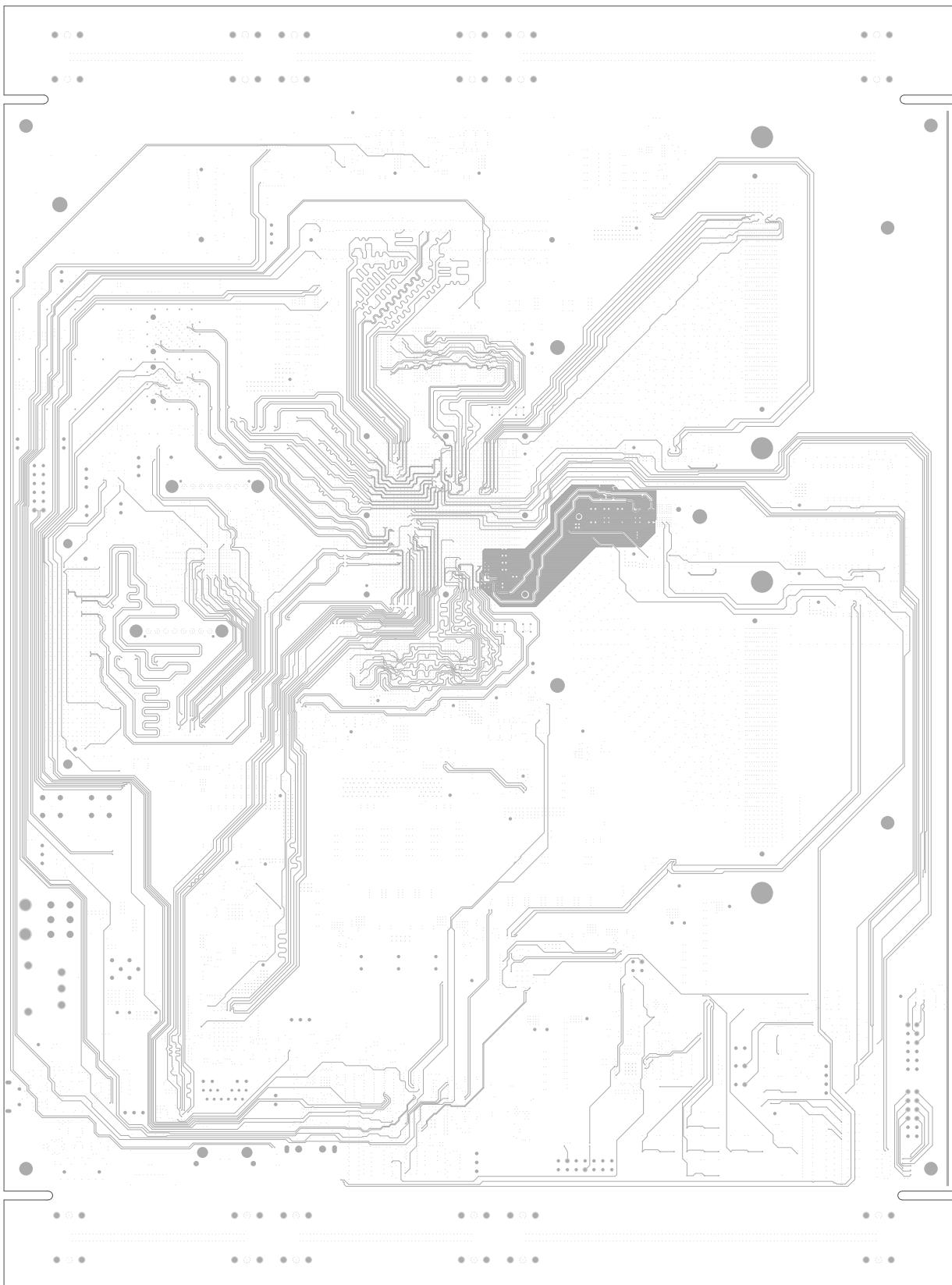
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PCB #	128-05003-01	LAYER:	L15_GND
Designed by	Xilinx	DATE:	10/18/2019
BOARD designer:	CAROL	PHONE:	408-879-4993
15		XILINX DOC USE ONLY REVISION-A02 Version aa	



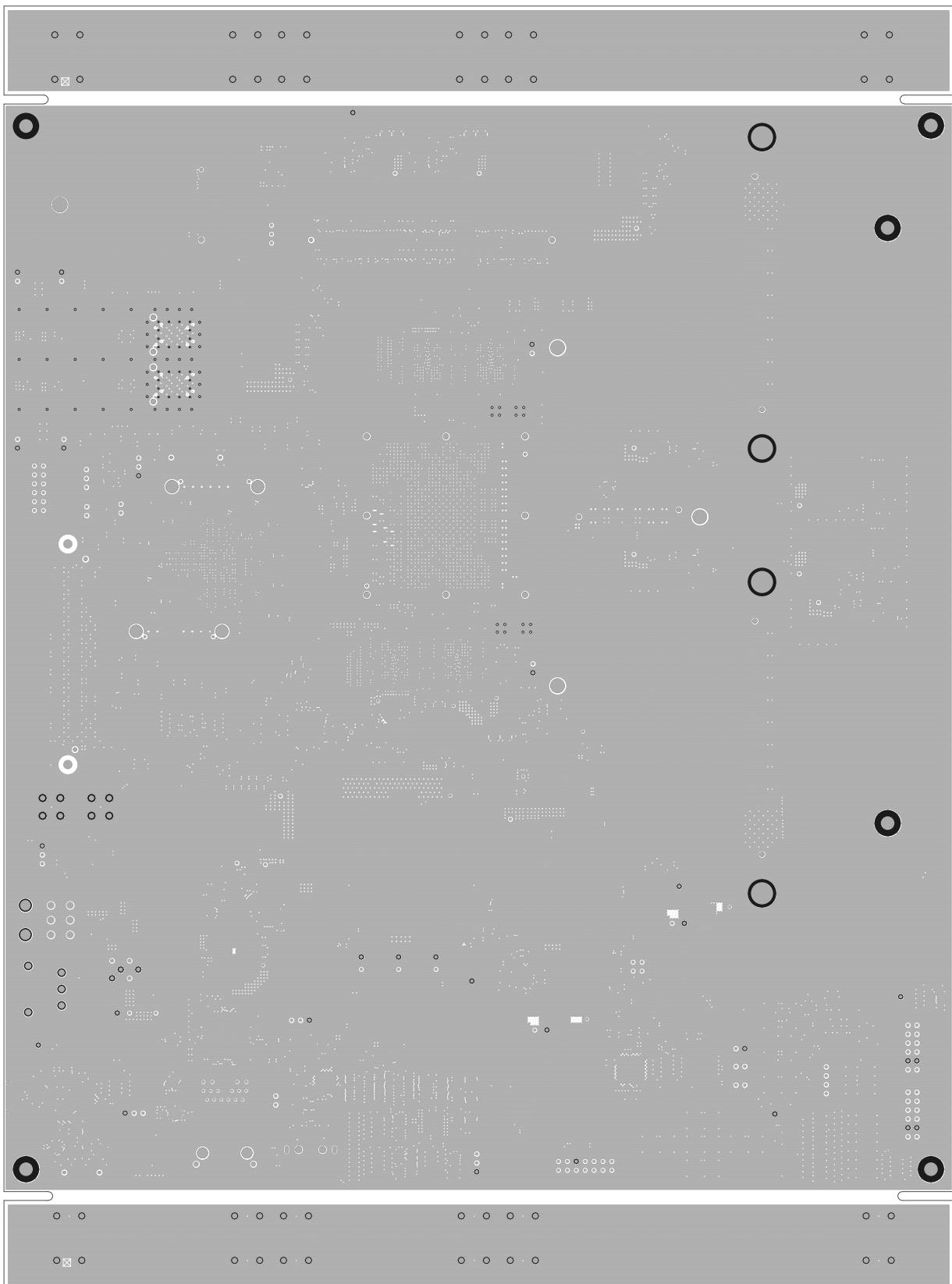
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PCB # 128-05003-01	LAYER: L16.SIG
Designed by Xilinx	DATE: 10/18/2019
BOARD designer: CAROL	PHONE: 408-879-4993
16	XILINX DOC USE ONLY
	REVISION-A02 Version aa



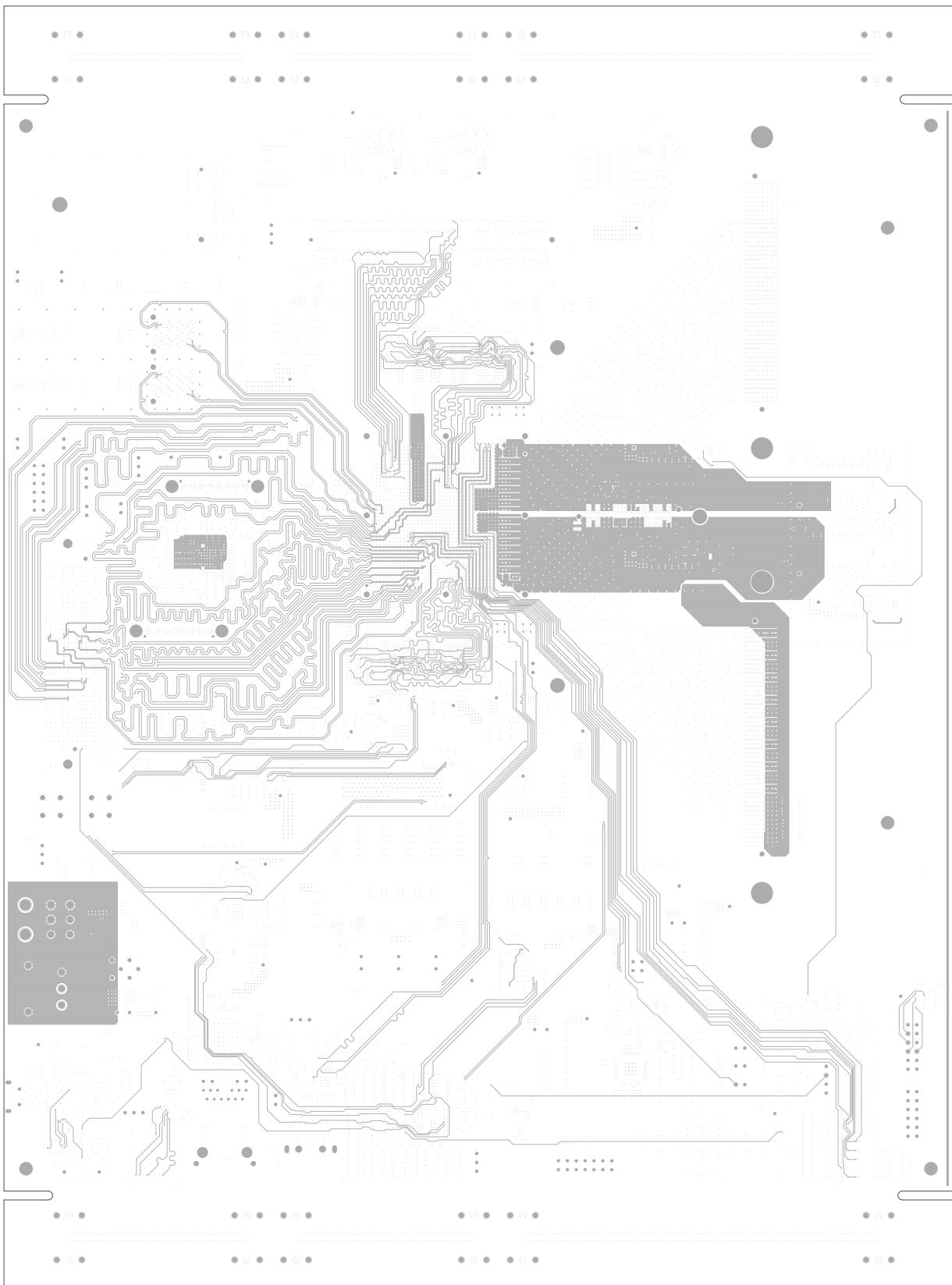
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB #	128-05003-01
Designed by	Xilinx
BOARD designer:	CAROL
DATE:	10/18/2019
PHONE:	408-879-4993
LAYER:	L17_GND
17	XILINX DOC USE ONLY REVISION-A02 Version aa



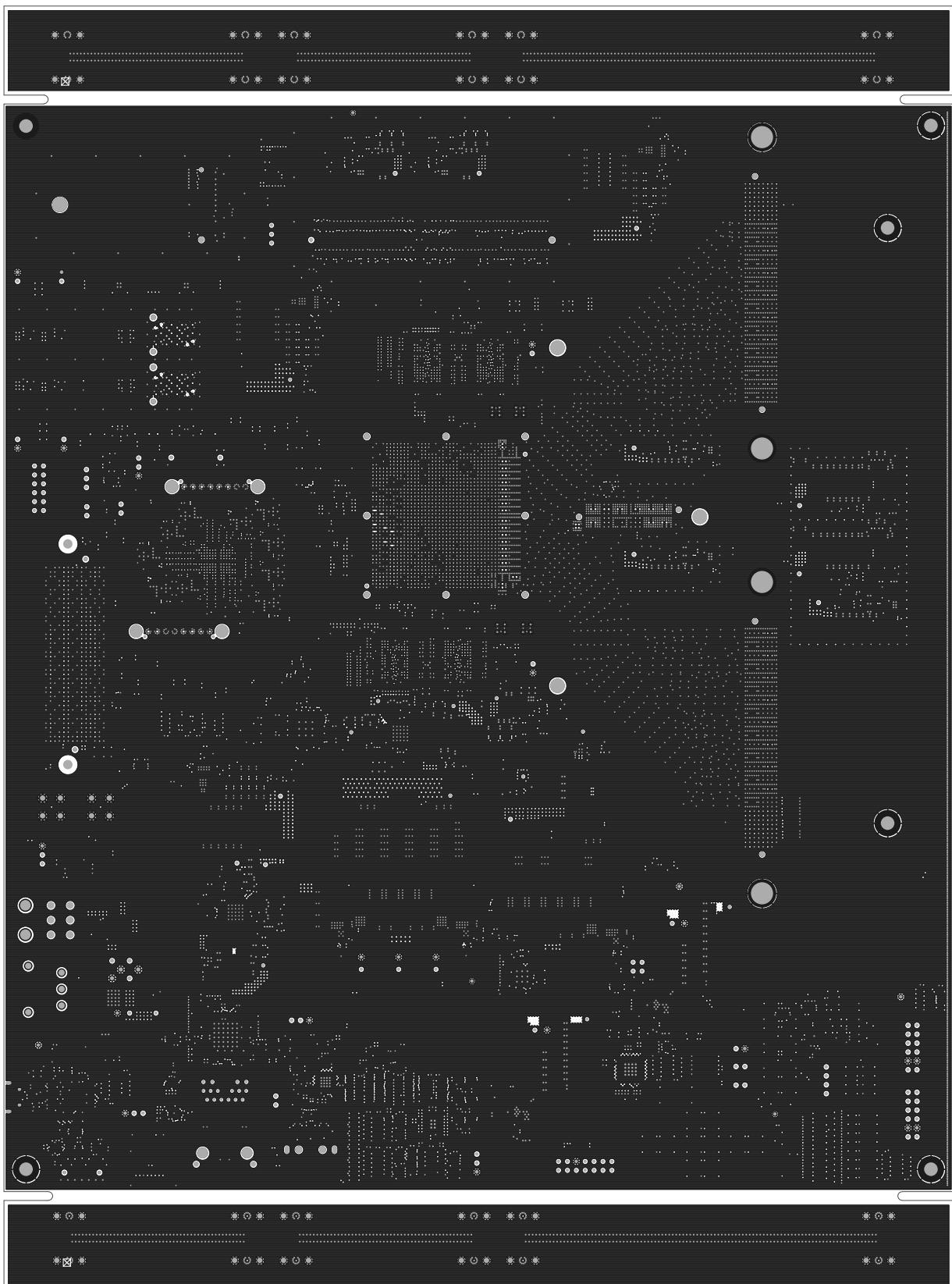
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PCB # 128-05003-01	LAYER: L18_SIG
Designed by Xilinx	DATE: 10/18/2019
BOARD designer: CAROL	PHONE: 408-879-4993
18	XILINX DOC USE ONLY
REVISION-A02 Version aa	



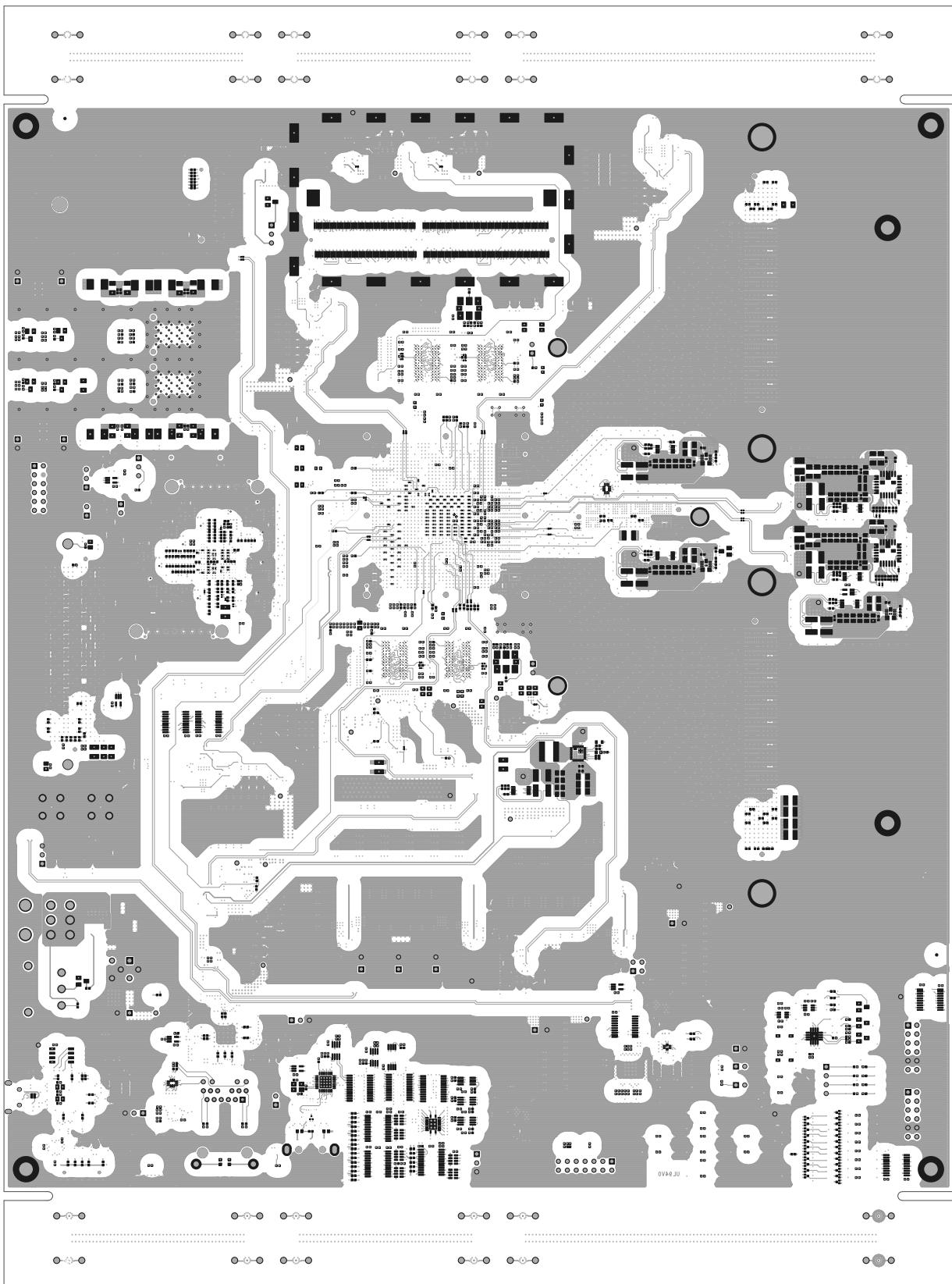
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB #	128-05003-01
Designed by	Xilinx
BOARD designer:	CAROL
DATE:	10/18/2019
PHONE:	408-879-4993
XILINX DOC USE ONLY	
19	REVISION-A02 Version aa



ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB #	128-05003-01
Designed by	Xilinx
BOARD designer:	CAROL
DATE:	10/18/2019
PHONE:	408-879-4993
20	XILINX DOC USE ONLY
	REVISION-A02 Version aa



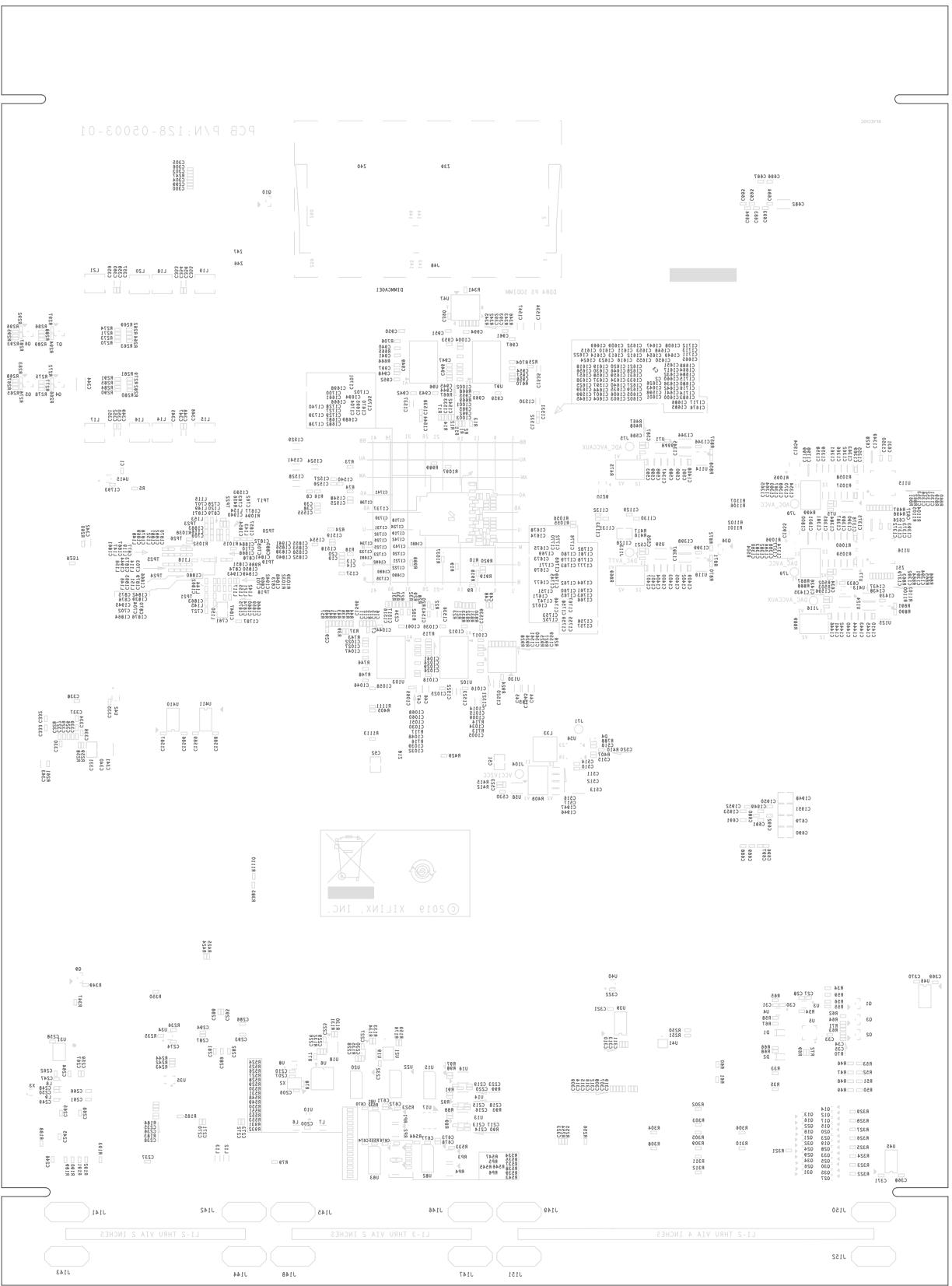
ARTWORK, ROHS COMPLIANT, HW-71-ZCU216	
PCB #	128-05003-01
LAYER:	L21_GND
Designed by	Xilinx
DATE:	10/18/2019
BOARD designer:	CAROL
PHONE:	408-879-4993
21	XILINX DOC USE ONLY
	REVISION-A02 Version aa

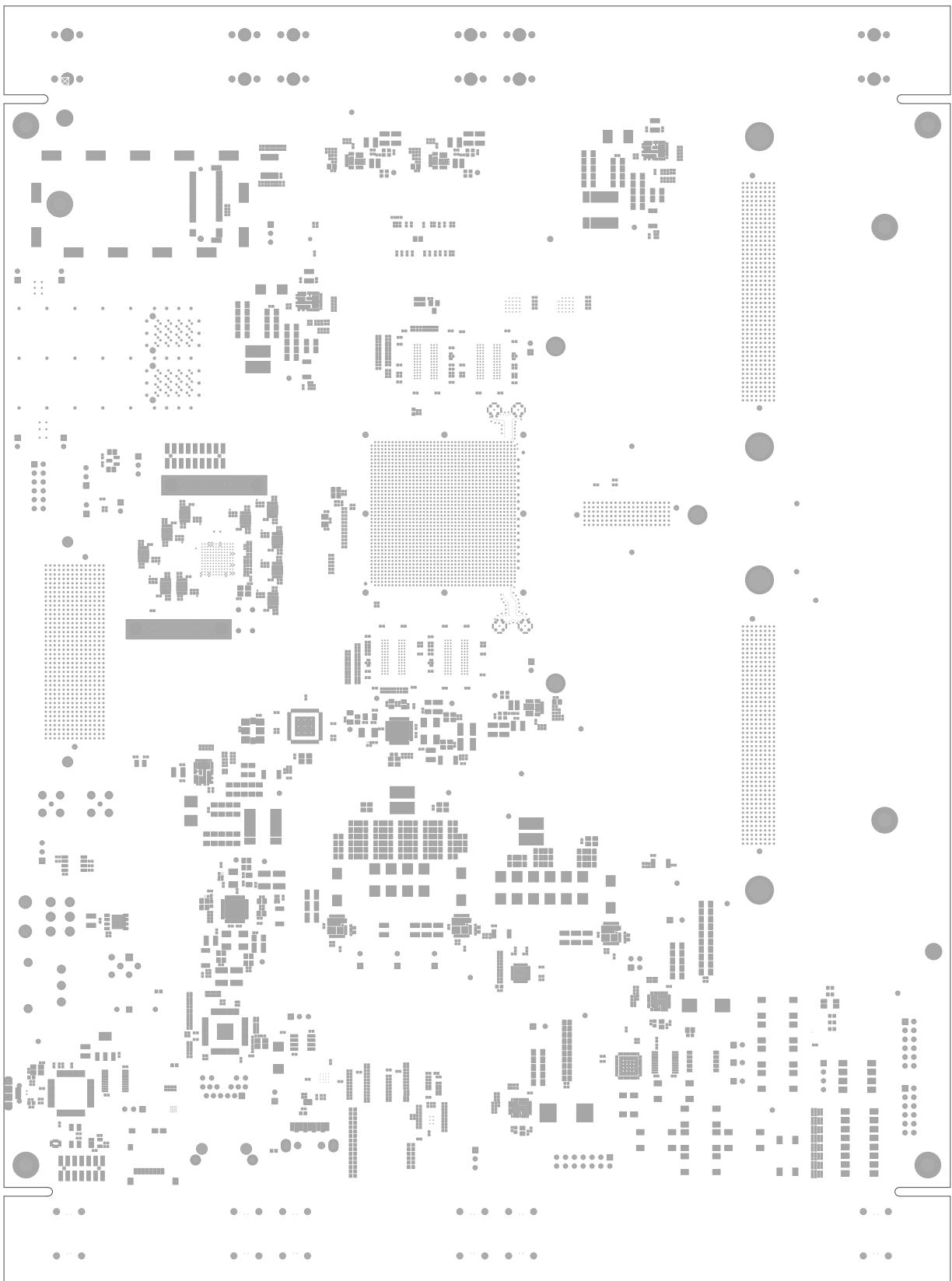


ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB # 128-05003-01	LAYER: L22_BOTTOM
Designed by Xilinx	DATE: 10/18/2019
BOARD designer: CAROL	PHONE: 408-879-4993
	XILINX DOC USE ONLY
22	REVISION-A02 Version aa

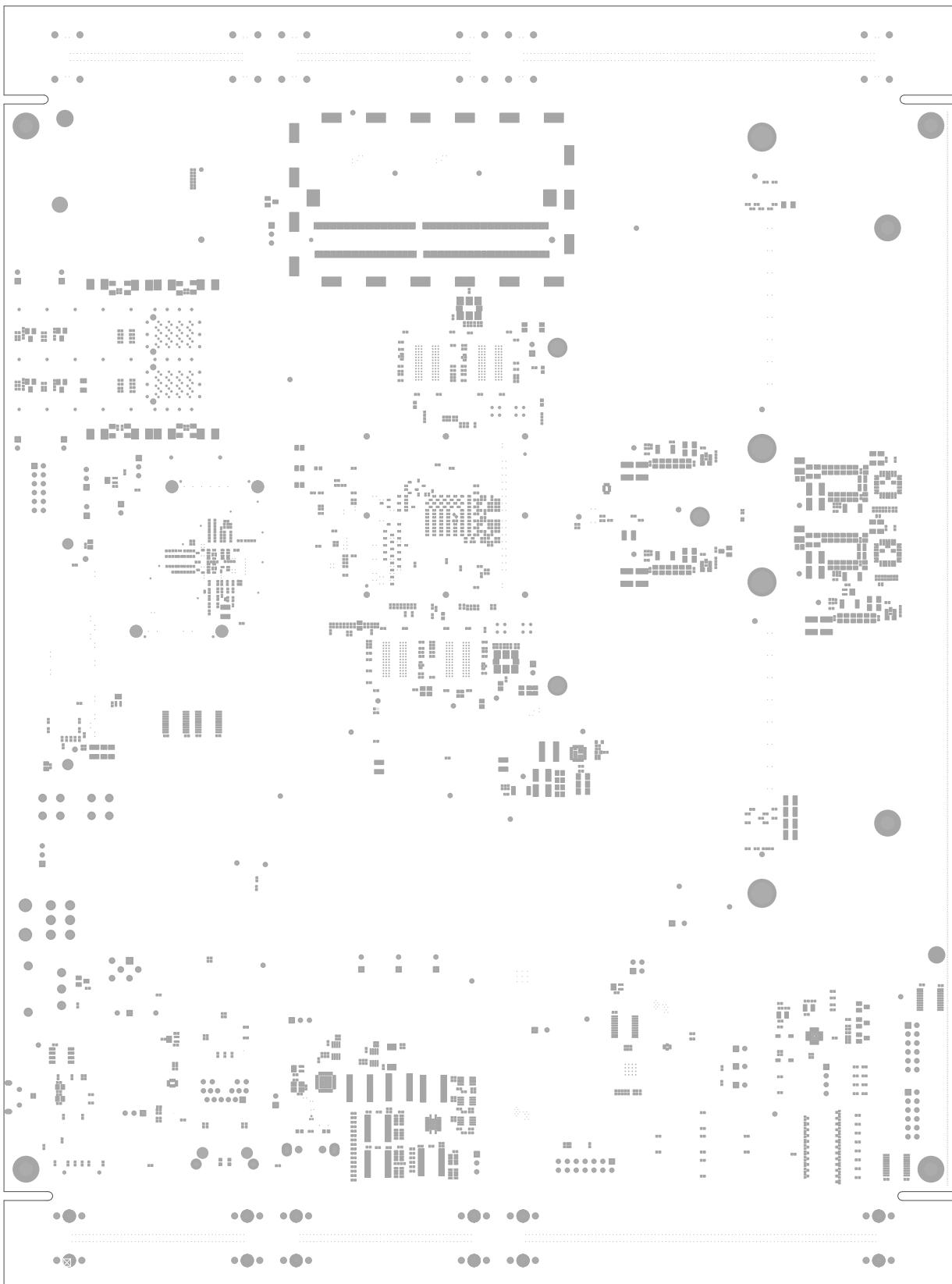


ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB # 128-05003-01	LAYER: SILKSCREEN TOP
Designed by Xilinx	DATE: 10/18/2019
BOARD designer: CAROL	PHONE: 408-879-4993
XILINX DOC USE ONLY	
REVISION-A02 Version aa	





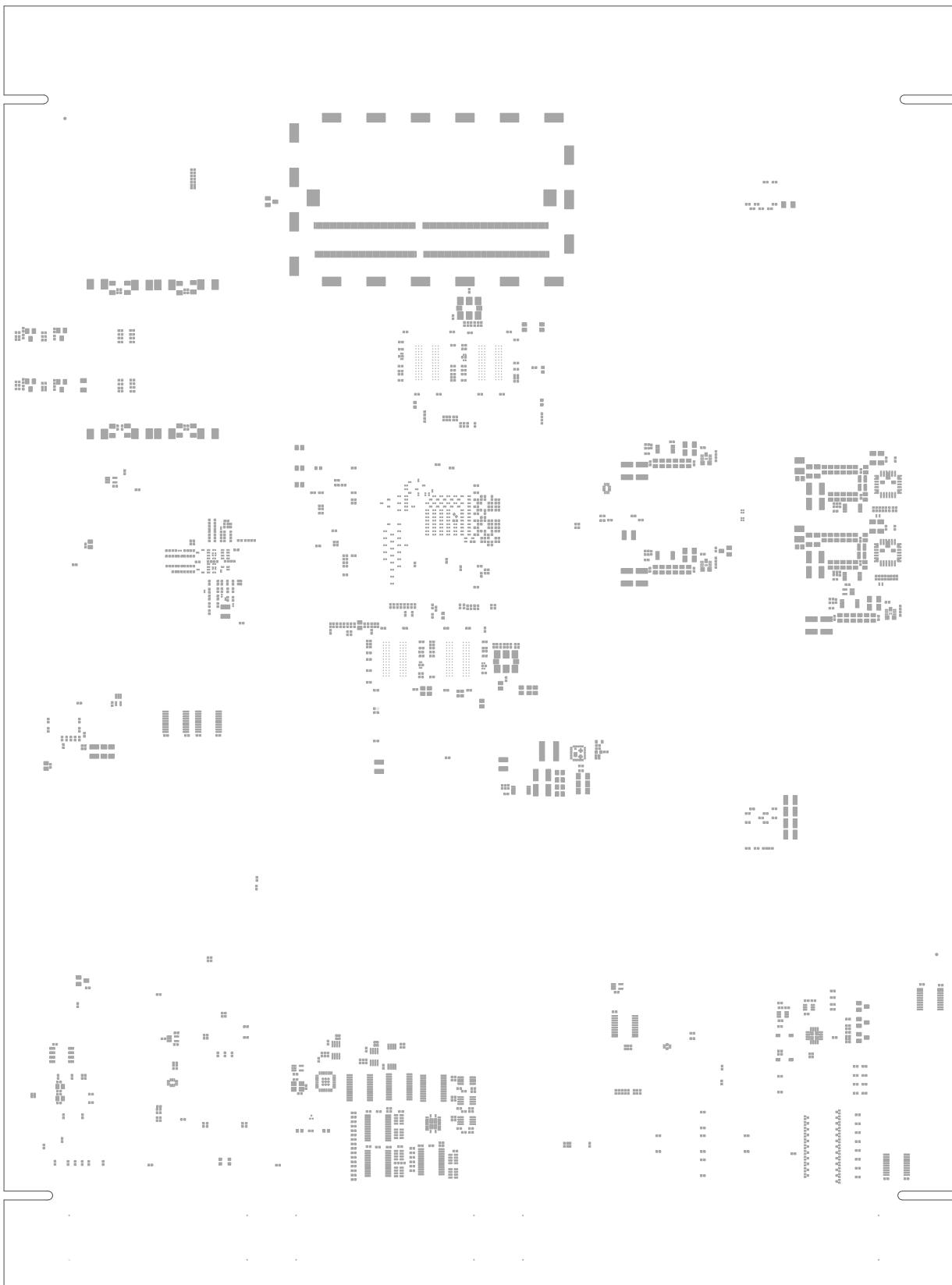
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB #	128-05003-01
LAYER:	MASK_TOP
Designed by	Xilinx
DATE:	10/18/2019
BOARD designer:	CAROL
PHONE:	408-879-4993
25	XILINX DOC USE ONLY
	REVISION-A02 Version aa



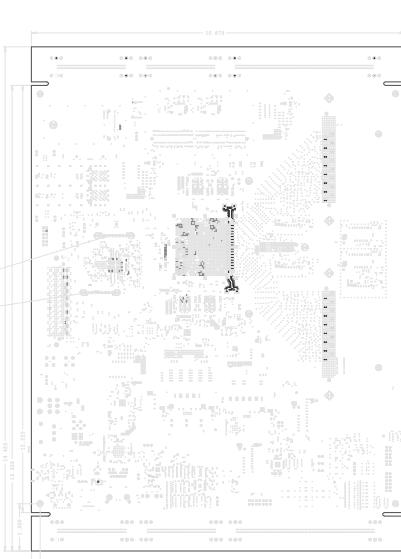
ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB #	128-05003-01
LAYER:	MASK_BOTTOM
Designed by	Xilinx
DATE:	10/18/2019
BOARD designer:	CAROL
PHONE:	408-879-4993
26	XILINX DOC USE ONLY
	REVISION-A02 Version aa



ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB # 128-05003-01	LAYER: PASTE_TOP
Designed by Xilinx	DATE: 10/18/2019
BOARD designer: CAROL	PHONE: 408-879-4993
	XILINX DOC USE ONLY
27	REVISION-A02 Version aa



ARTWORK, ROHS COMPLIANT, HW-Z1-ZCU216	
PCB # 128-05003-01	LAYER: PASTE_BOT
Designed by Xilinx	DATE: 10/18/2019
BOARD designer: CAROL	PHONE: 408-879-4993
	XILINX DOC USE ONLY
28	REVISION-A02 Version aa



BACKDRILL: BOTTOM to L07_SIG_RF_GND
ALL UNITS ARE IN MILS MFG STUB QTY
FIGURE BD_SIZE MNC LAYER MFG STUB QTY
• 11.6 L05_GND_RF_SIG 8.0 8

BACKDRILL: BOTTOM to L06_GND_RF_SIG
ALL UNITS ARE IN MILS MFG STUB QTY
FIGURE BD_SIZE MNC LAYER MFG STUB QTY
• 11.6 L05_SIG_RF_GND 8.0 16

BACKDRILL: BOTTOM to L08_GND
ALL UNITS ARE IN MILS MFG STUB QTY
FIGURE BD_SIZE MNC LAYER MFG STUB QTY
• 11.6 L07_SIG_RF_GND 8.0 40

DRILL CHART: TOP to L03_SIG_RF_GND
ALL UNITS ARE IN MILS DRILL TOLERANCE PLATED QTY COMMENT

FIGURE FMS FMS TOLERANCE DRILL SIZE DRILL TOLERANCE PLATED QTY COMMENT

• 9.8 +0.0/-0.8 9.8 PLATED 239

DRILL CHART: TOP to L02_GND_RF_SIG

ALL UNITS ARE IN MILS DRILL TOLERANCE PLATED QTY COMMENT

FIGURE FMS FMS TOLERANCE DRILL SIZE DRILL TOLERANCE PLATED QTY COMMENT

• 6.0 +0.0/-0.0 6 PLATED 151

DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

FIGURE FMS FMS TOLERANCE DRILL SIZE DRILL TOLERANCE PLATED QTY COMMENT

• 9.8 +0.0/-0.8 9.8 PLATED 11617

• 9.8 +0.0/-0.8 9.8 PLATED 11617

• 9.8 +0.0/-0.8 9.8 PLATED 11644

• 12.0 +0.0/-0.0 12.0 PLATED 37

• 12.0 +0.0/-0.0 12.0 PLATED 37

• 14.0 +0.0/-0.0 14.0 PLATED 80

• 22.0 +0.0/-0.0 22.0 PLATED 29

• 22.0 +0.0/-0.0 22.0 PLATED 29

• 33.0 +0.0/-0.0 33.0 PLATED 2

• 33.0 +0.0/-0.0 33.0 PLATED 2

• 45.0 +0.0/-0.0 45.0 PLATED 15

• 45.0 +0.0/-0.0 45.0 PLATED 4

• 45.0 +0.0/-0.0 45.0 PLATED 4

• 48.0 +0.0/-0.0 48.0 PLATED 8

• 62.0 +0.0/-0.0 62.0 PLATED 40

• 62.0 +0.0/-0.0 62.0 PLATED 40

• 63.0 +0.0/-0.0 63.0 PLATED 8

• 73.0 +0.0/-0.0 73.0 PLATED 5

• 82.0 +0.0/-0.0 82.0 PLATED 4

• 121.0 +0.0/-0.0 121.0 PLATED 2

• 136.0 +0.0/-0.0 136.0 PLATED 2

• 136.0 +0.0/-0.0 136.0 PLATED 2

• 33.0 +0.0/-0.0 33.0 NON-PLATED 4

• 33.0 +0.0/-0.0 33.0 NON-PLATED 4

• 43.0 +0.0/-0.0 43.0 NON-PLATED 1

• 43.0 +0.0/-0.0 43.0 NON-PLATED 1

• 57.0 +0.0/-0.0 57.0 NON-PLATED 6

• 78.0 +0.0/-0.0 78.0 NON-PLATED 2

• 126.0 +0.0/-0.0 126.0 NON-PLATED 2

• 146.0 +0.0/-0.0 146.0 NON-PLATED 3

• 146.0 +0.0/-0.0 146.0 NON-PLATED 3

• 175.0 +0.0/-0.0 175.0 NON-PLATED 1

• 33.0 +0.0/-0.0 33.0 PLATED 2

• 56.043.0 +0.0/-0.0 56.043.0 PLATED 2

• 78.044.0 +0.0/-0.0 78.044.0 PLATED 2

DESIGN CROSS SECTION CHART
TOTAL THICKNESS 119.94 MIL

REV		DESCRIPTION		DATE	APPROVED
VER	1	FIRST RELEASE		07/24/19	CH
VER	2	MINI UPDATES		07/24/19	CH

SURFACE : AIR
DIELECTRIC : AIR
L1 TOP CONDUCTOR - 0502_HTE_M2_OZ_PLATING
DIELECTRIC - 001-ITERA-MT40-2X1067-RCT2-PREG
L2 L02_GND_RF_S10 PLANE - 0502_VLP2_CU
DIELECTRIC - 002-ITERA-MT40-2X1067-RCT2-SCORE
L3 L03_SIG_RF_GND CONDUCTOR - 0502_VLP2_CU
DIELECTRIC - 001-ITERA-MT40-2X1067-RCT2-PREG
L4 L04_GND_RF_S10 PLANE - 0502_VLP2_CU
DIELECTRIC - 002-ITERA-MT40-2X1067-RCT2-SCORE
L5 L05_GND_RF_GND CONDUCTOR - 0502_VLP2_CU
DIELECTRIC - 001-ITERA-MT40-2X1067-RCT2-PREG
L6 L06_GND_RF_S10 PLANE - 0502_VLP2_CU
DIELECTRIC - 002-ITERA-MT40-2X1067-RCT2-SCORE
L7 L07_SIG_RF_GND CONDUCTOR - 0502_VLP2_CU
DIELECTRIC - 001-ITERA-MT40-2X1067-RCT2-PREG
L8 L08_GND PLANE - 0502_CU
DIELECTRIC - 003-ITERA-MT40-1X1067-RC68-2CORE
L9 L09_GND PLANE - 0502_CU
DIELECTRIC - 003-ITERA-MT40-2X1035_RC65-PREG
L10 L10_GND PLANE - 0502_CU
DIELECTRIC - 001-ITERA-MT40-1X1067-RC68-2CORE
L11 L11_PWR PLANE - 0502_CU
DIELECTRIC - 001-ITERA-MT40-2X1067-RCT2-PREG
L12 L12_PWR PLANE - 0502_CU
DIELECTRIC - 003-ITERA-MT40-1X1067-RC68-2CORE
L13 L13_PWR PLANE - 0502_CU
DIELECTRIC - 003-ITERA-MT40-2X1035_RC65-PREG
L14 L14_PWR PLANE - 0502_CU
DIELECTRIC - 001-ITERA-MT40-1X1067-RC68-2CORE
L15 L15_GND PLANE - 0502_CU
DIELECTRIC - 001-ITERA-MT40-2X1067-RCT2-PREG
L16 L16_S10 CONDUCTOR - 0502_VLP2_CU
DIELECTRIC - 002-ITERA-MT40-2X1067-RCT2-SCORE
L17 L17_GND PLANE - 0502_VLP2_CU
DIELECTRIC - 001-ITERA-MT40-2X1067-RCT2-PREG
L18 L18_S10 CONDUCTOR - 0502_VLP2_CU
DIELECTRIC - 002-ITERA-MT40-2X1067-RCT2-SCORE
L19 L19_GND PLANE - 0502_VLP2_CU
DIELECTRIC - 001-ITERA-MT40-2X1067-RCT2-PREG
L20 L20_S10 CONDUCTOR - 0502_VLP2_CU
DIELECTRIC - 002-ITERA-MT40-2X1067-RCT2-SCORE
L21 L21_GND PLANE - 0502_VLP2_CU
DIELECTRIC - 001-ITERA-MT40-2X1067-RCT2-PREG
L22 BOTTOM CONDUCTOR - 0502_HTE_M2_OZ_PLATING
SURFACE : 0502_HTE_M2_OZ_PLATING
DIELECTRIC - 0502_HTE_M2_OZ_PLATING
SURFACE : AIR

UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE
DIMENSIONS ARE IN INCHES	DRANN, CAROL H.	07/24/19
INCHES = 25.4MM		
± P. DECIMALS +/- .010	CHECKED	
± P. DECIMALS +/- .005	ENGRC, BRIAN FORSSE	07/24/19
FRACTIONS +	ISSUED	

XILINX.
2100 LOGIC DR
SAN JOSE, CA 95124
HMC - HARDWARE & CONFIGURATION PLATFORMS

FABRICATION DRAWING
PCB: FABRICATED
HW-01_ZCU216

SIZE FSCM NO Dwg No REV
D 128-05003-01 A02
SCALE NONE SHEET
Version Aa