

RFSoC UltraScale+ Evaluation Board

HW-Z1-ZCU216

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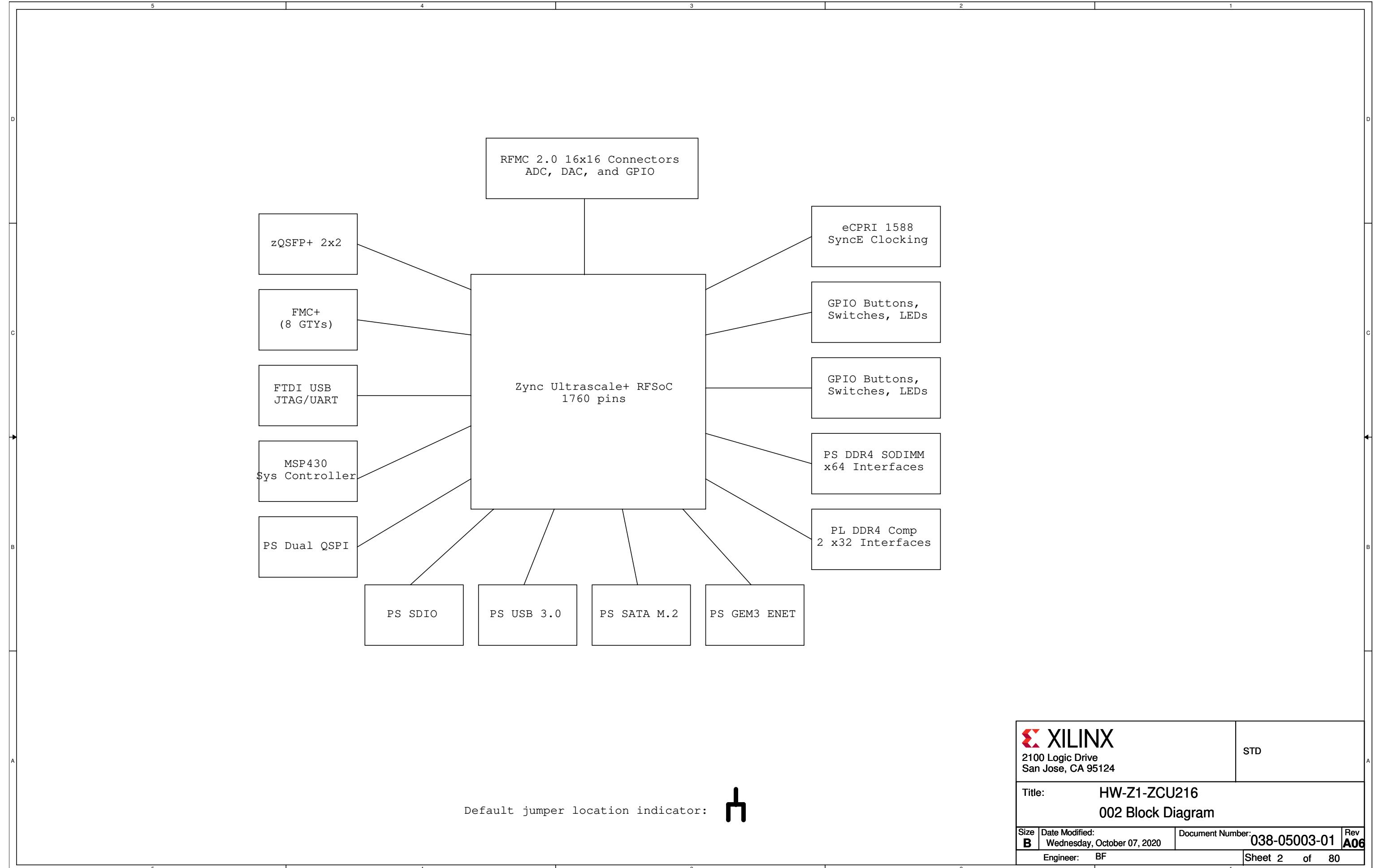
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Title: HW-Z1-ZCU216 001 Title Page		
Size: B	Date Modified: Wednesday, October 07, 2020	Document Number: 038-05003-01 Rev A06
Engineer: BF	Sheet 1 of 80	



Default jumper location indicator:



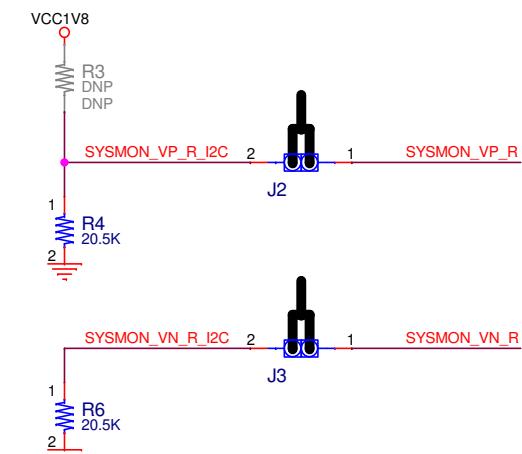
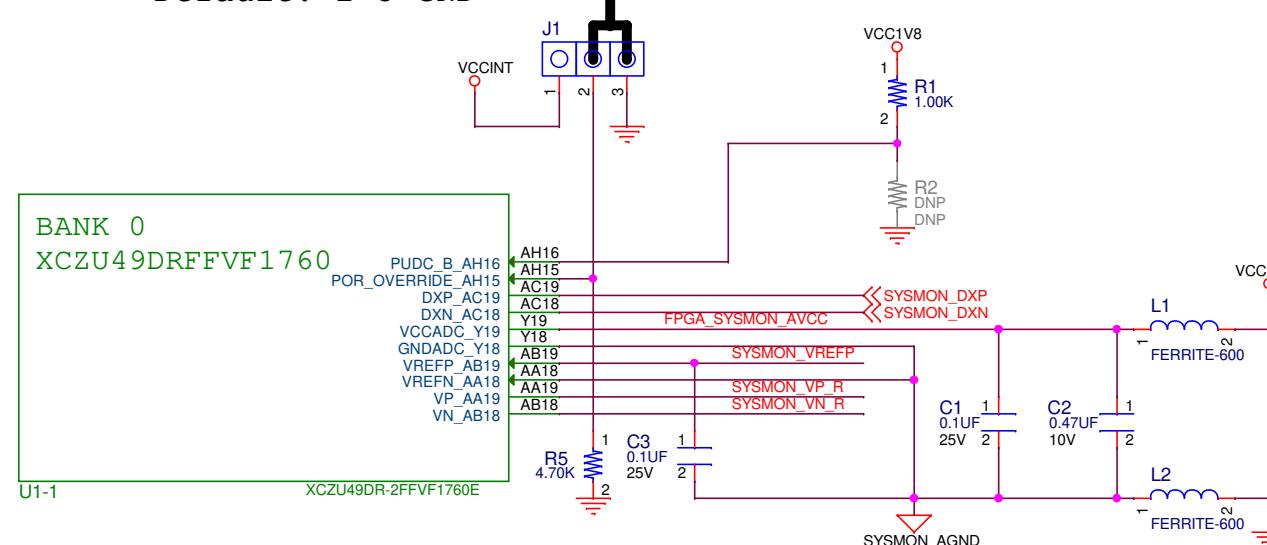
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San Jose, CA 95124

STD

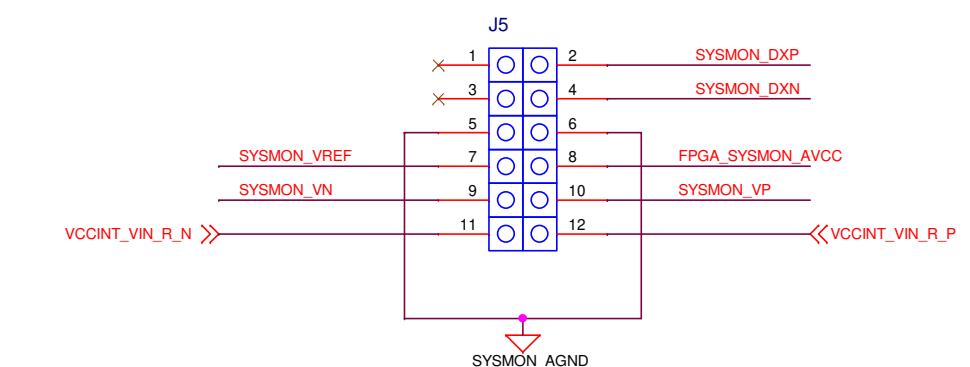
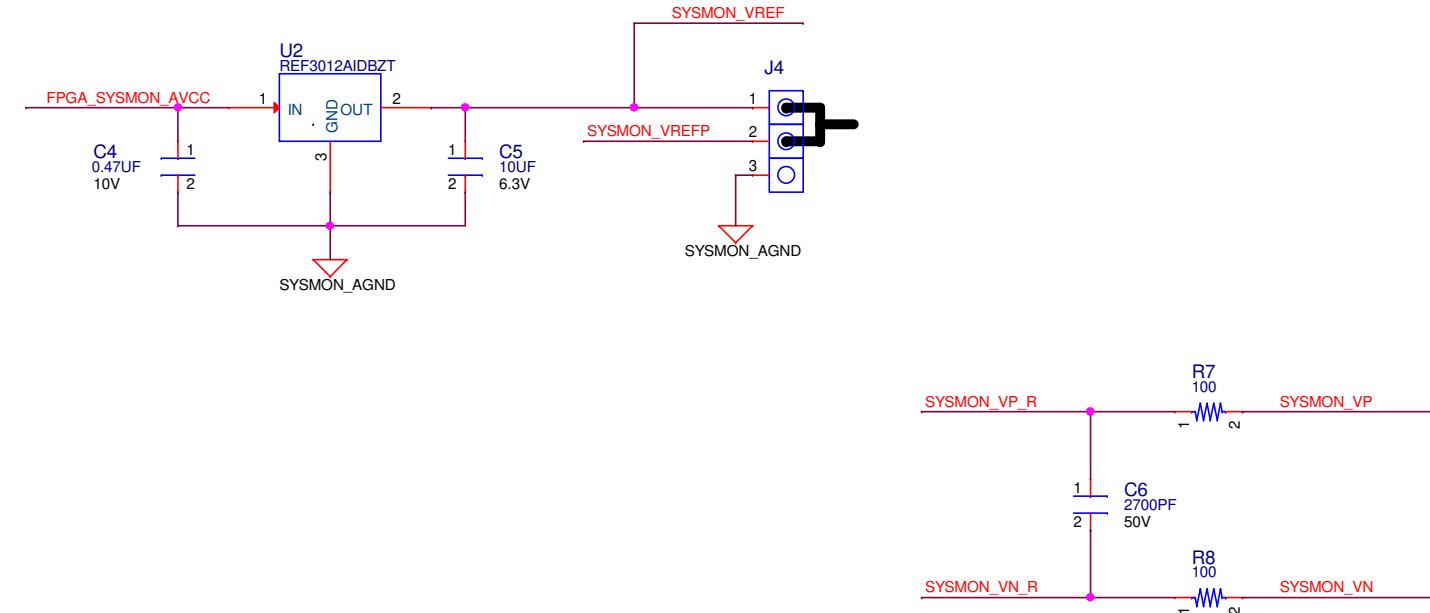
Title: **HW-Z1-ZCU216**
002 Block Diagram

Size	Date Modified:	Document Number:	Rev
B	Wednesday, October 07, 2020	038-05003-01	A06
Engineer: BF	Sheet 2 of 80		

POR_OVERRIDE select
Default: 2-3 GND



SYSMON I2C Address jumpers



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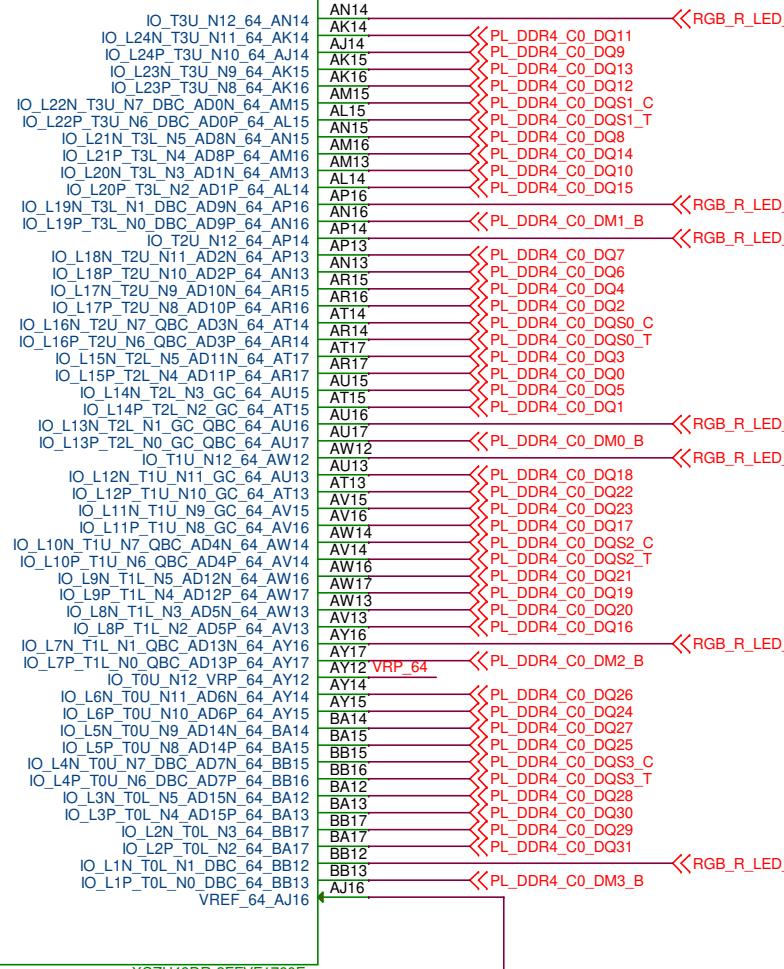
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STD

Title: HW-Z1-ZCU216
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Size	Date Modified:	Document Number:	Rev
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Engineer: BF	Sheet 3 of 80		

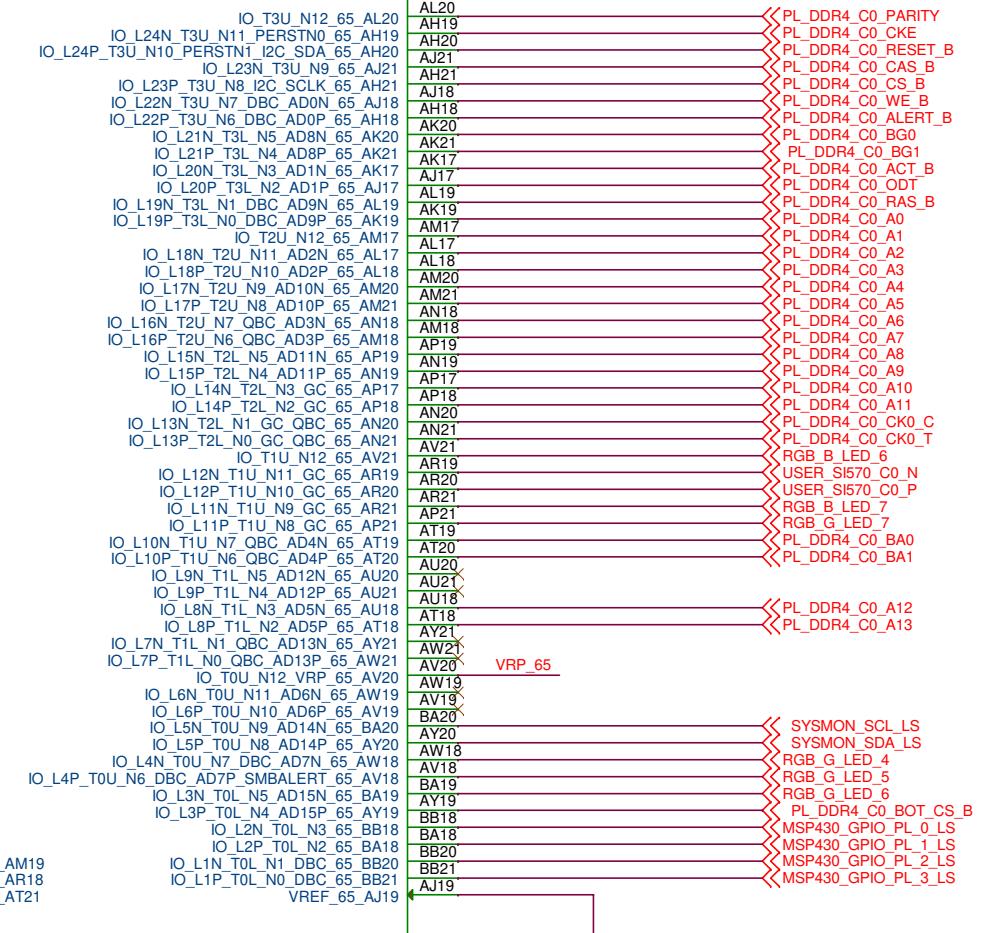
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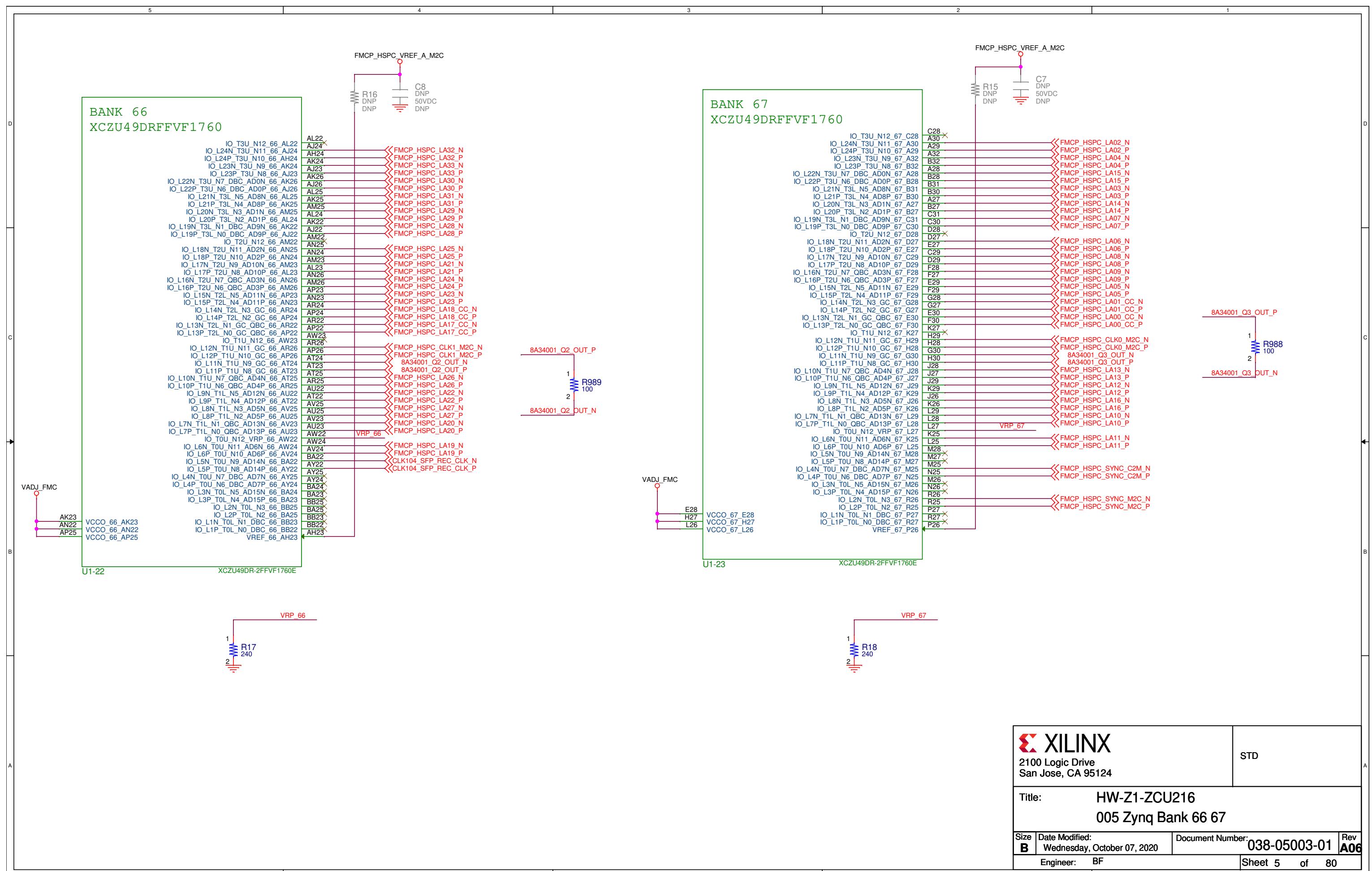
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Title: HW-Z1-ZCU216
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Size	Date Modified:	Document Number:	Rev
B	Wednesday, October 07, 2020	038-05003-01	A06
Engineer: BF	Sheet 4 of 80		



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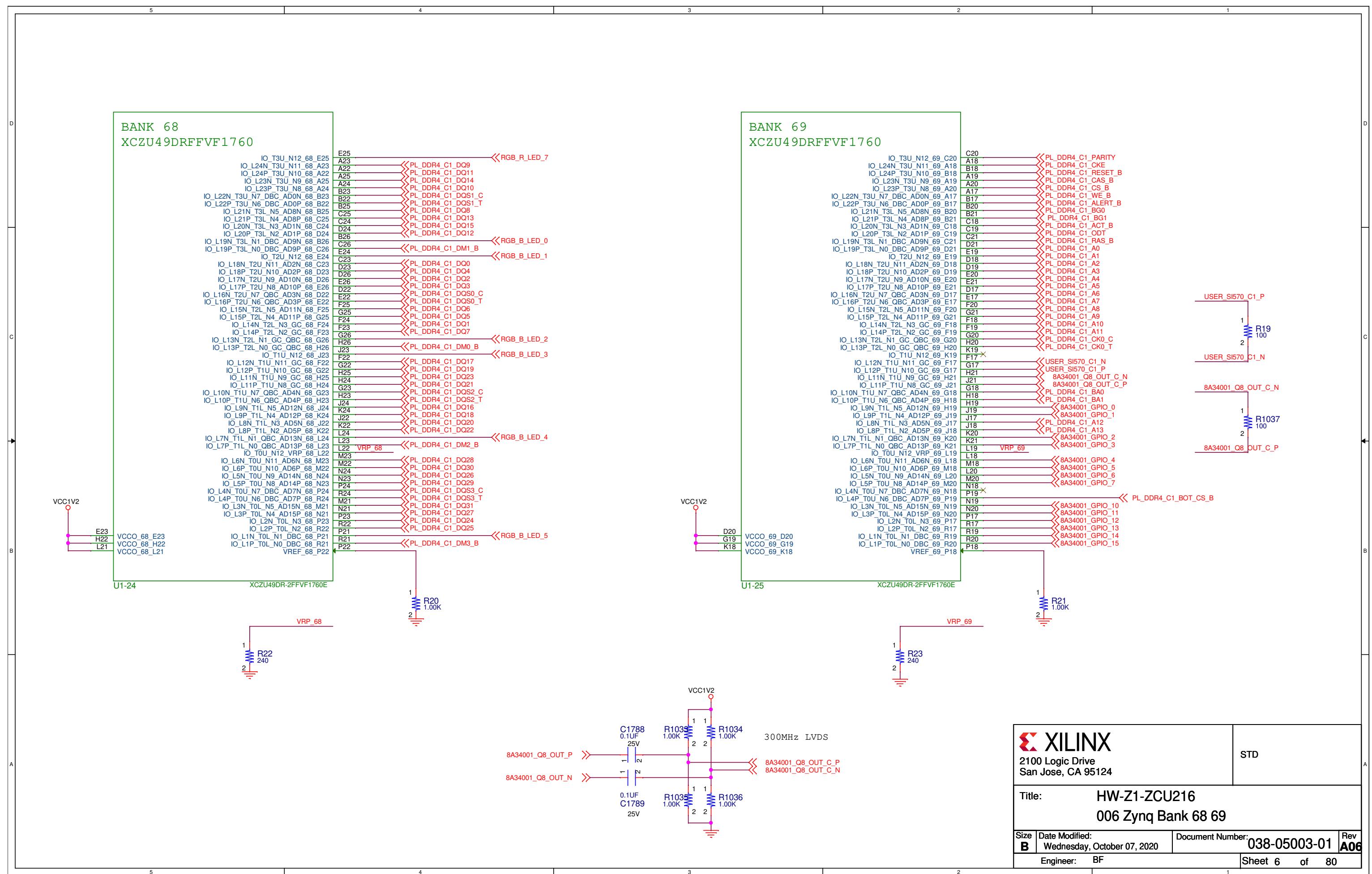
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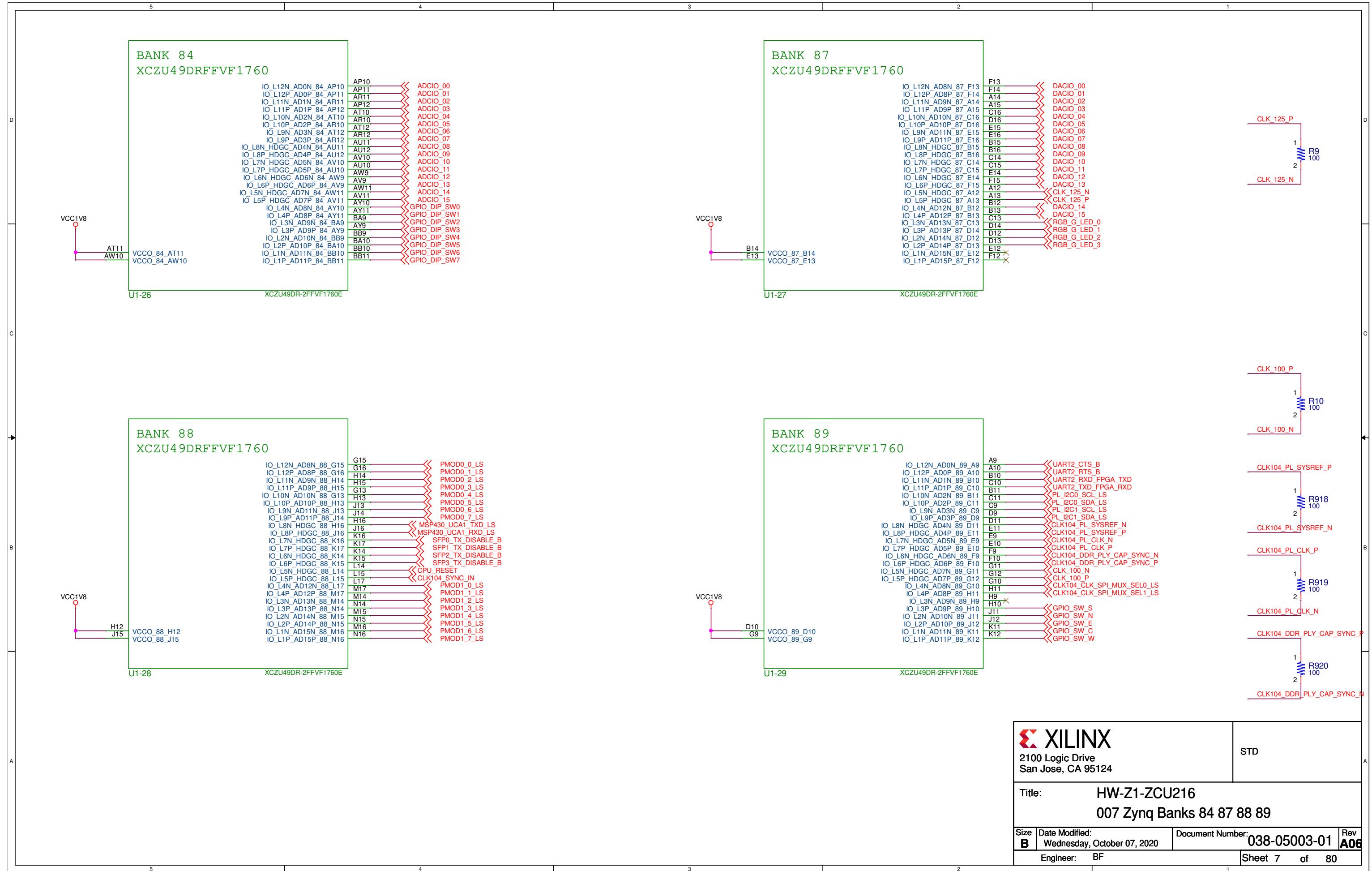
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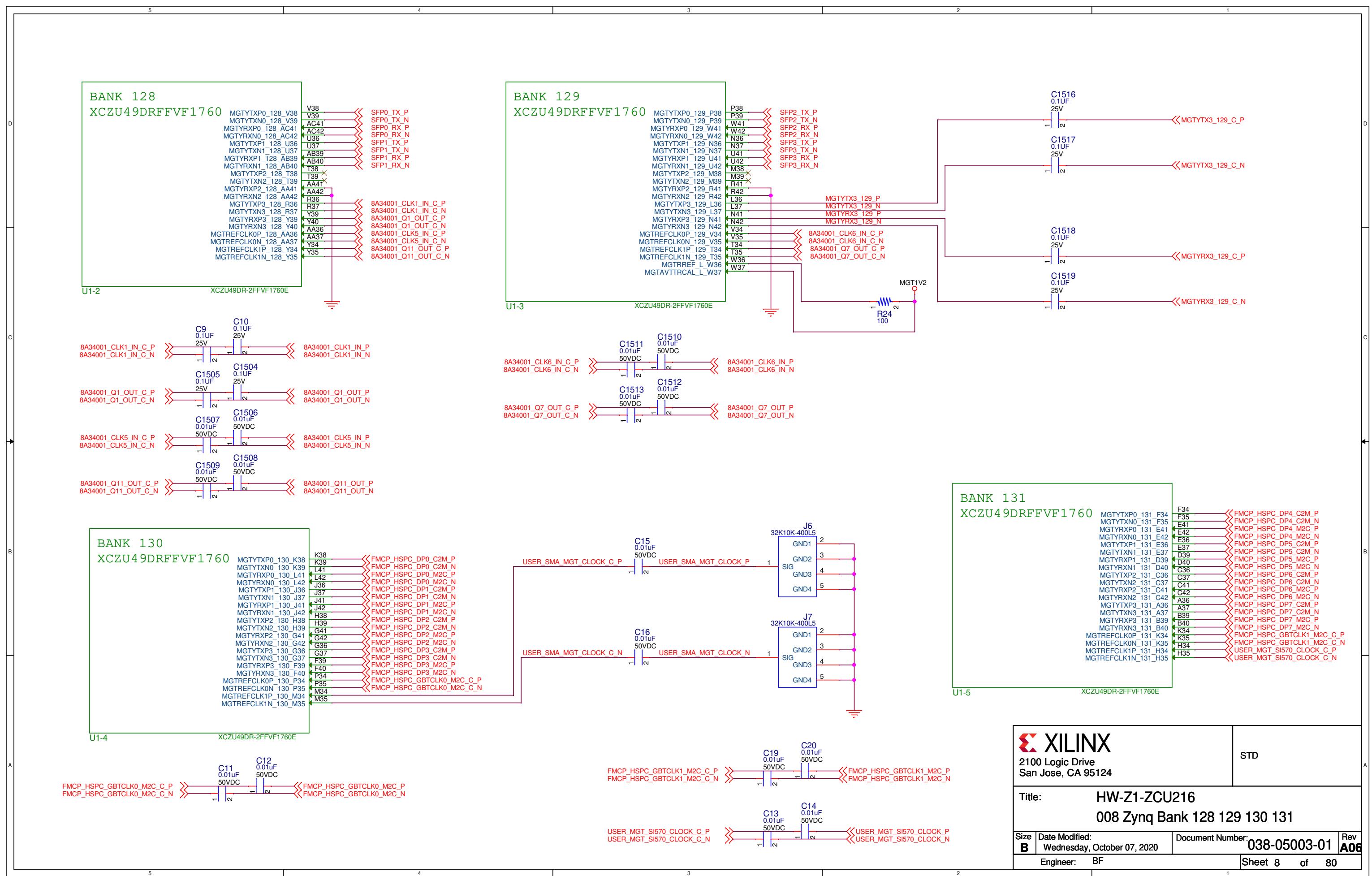
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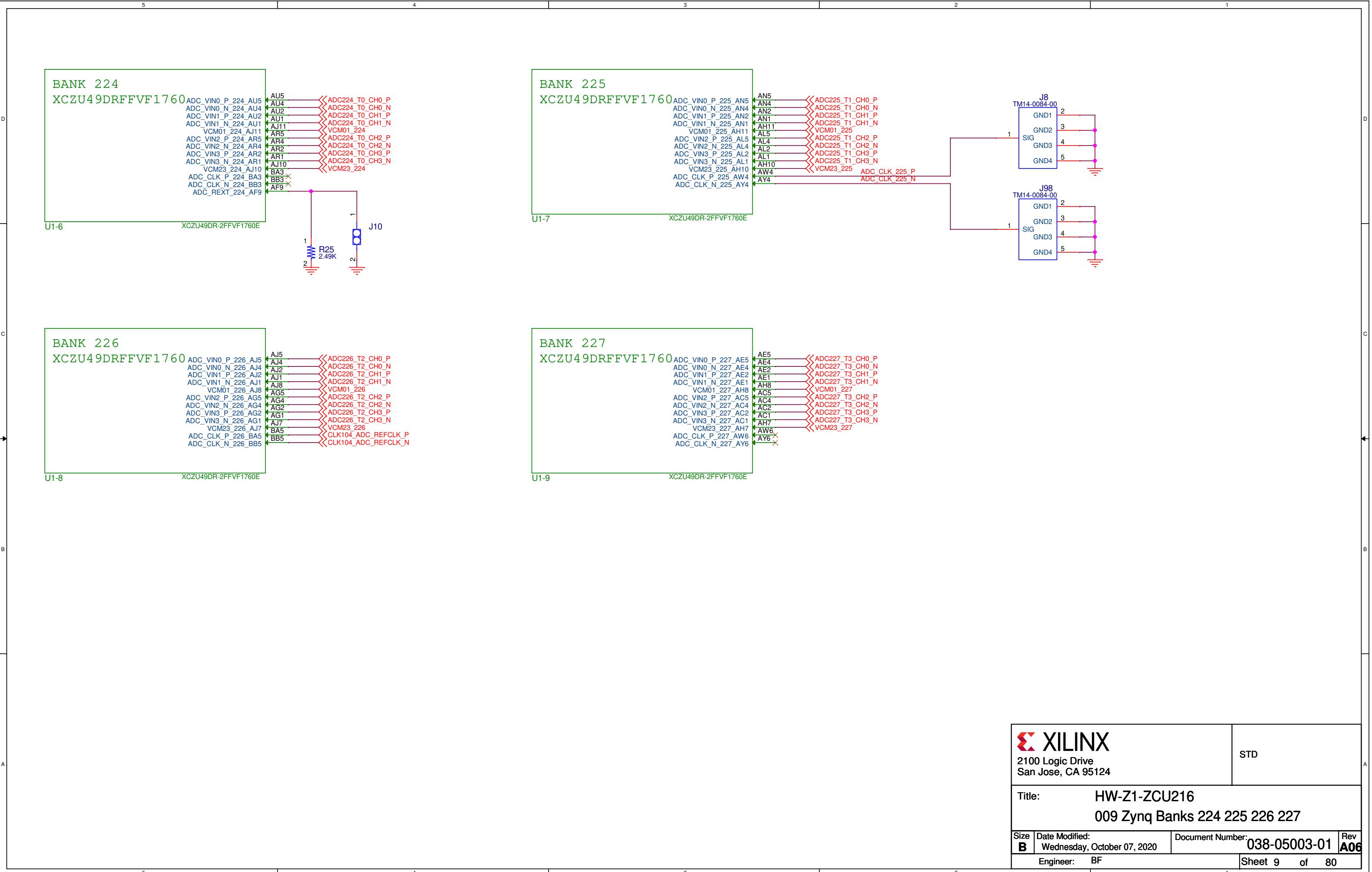
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B	Wednesday, October 07, 2020	038-05003-01
Engineer:	BF	Rev A06

Sheet 5 of 80





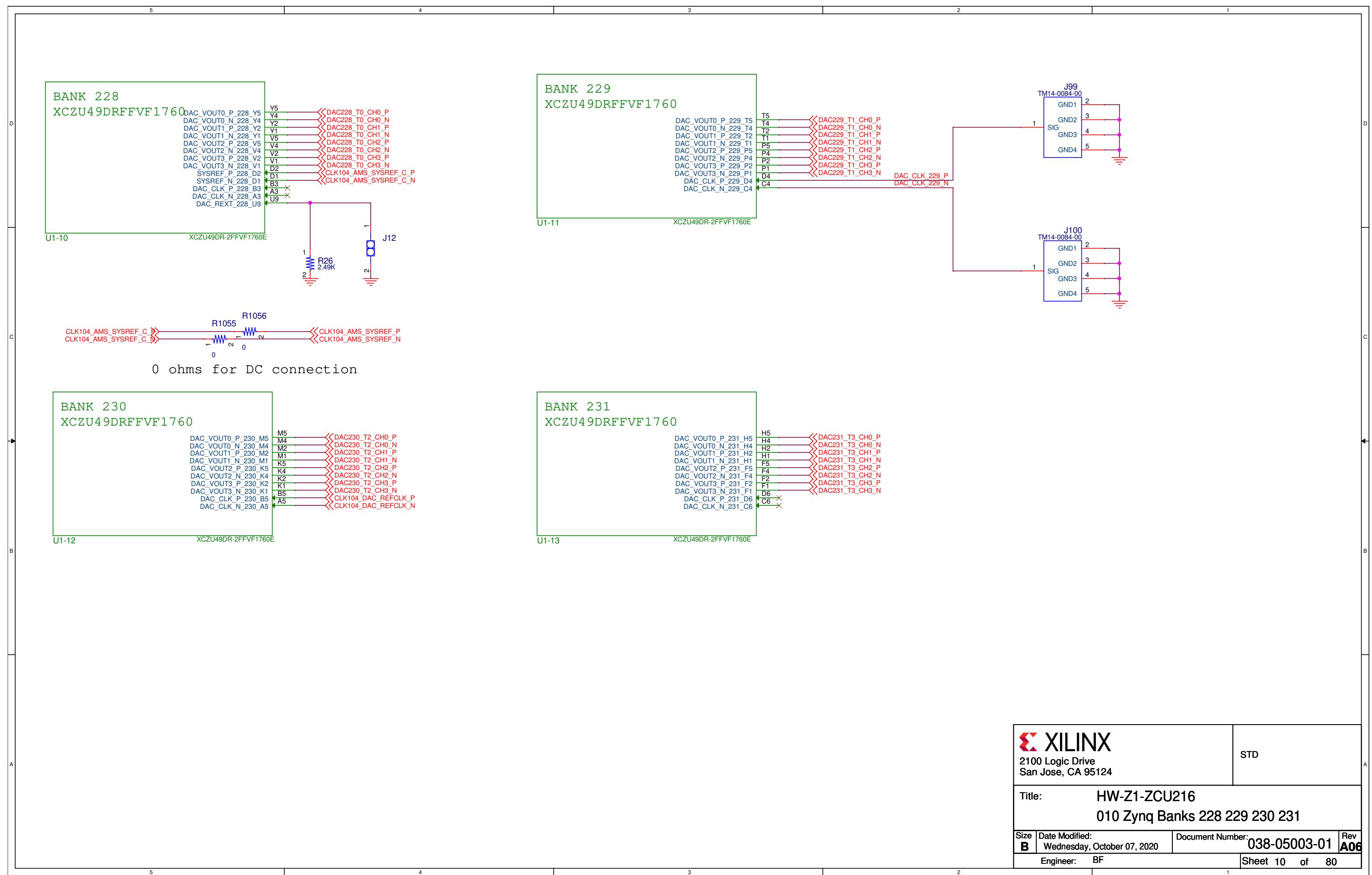


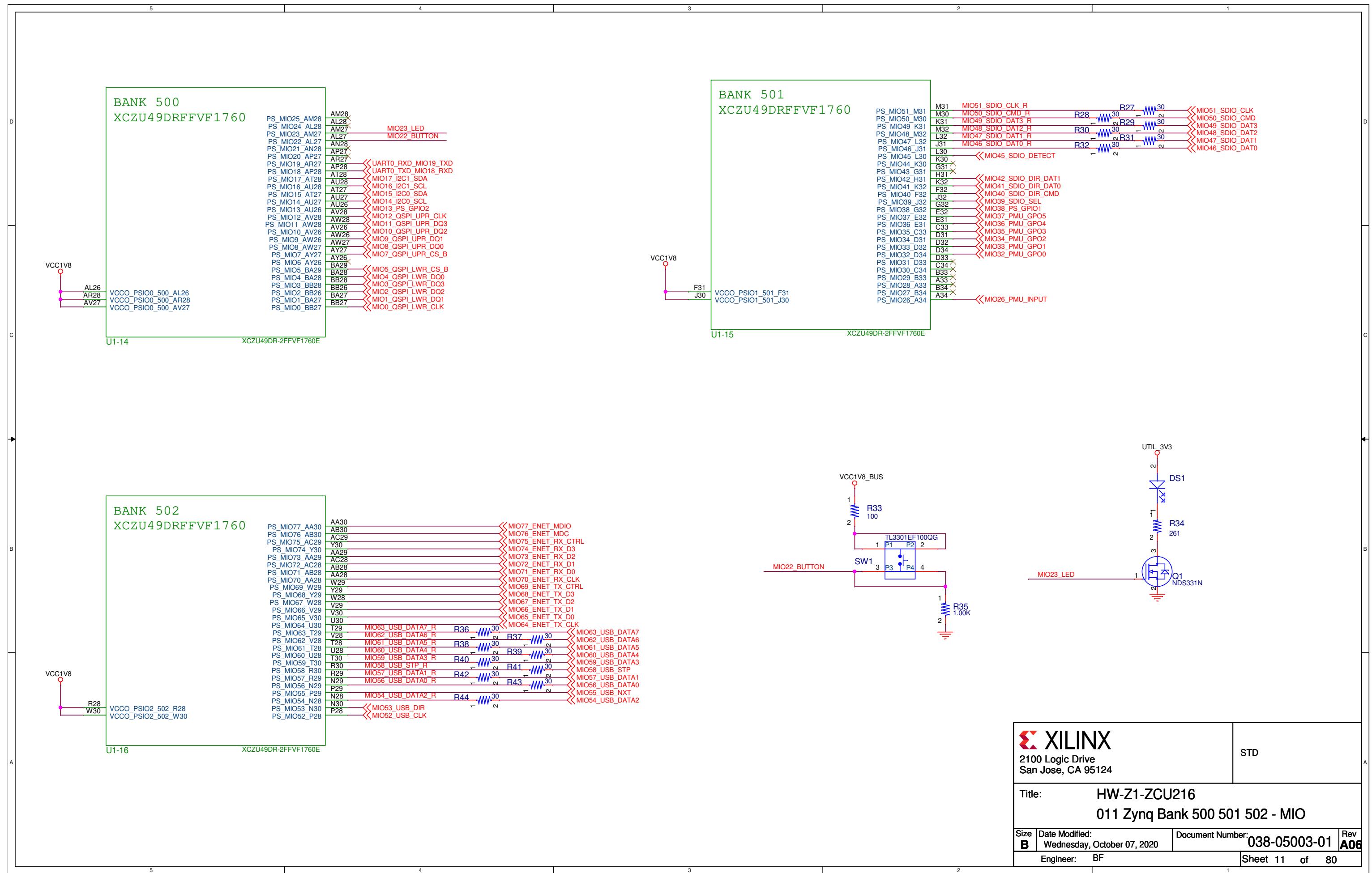


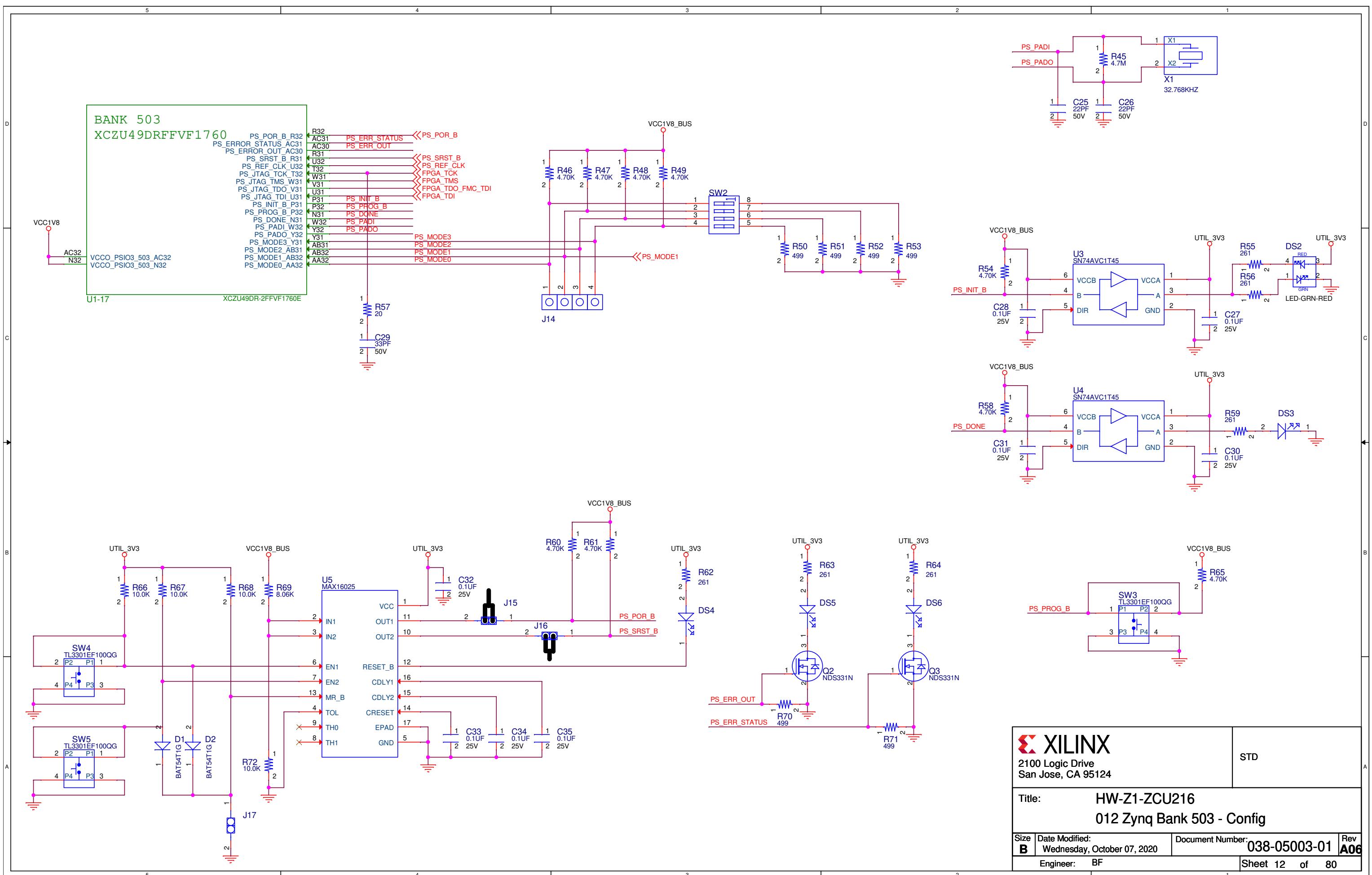
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009 Zynq Banks 224 225 226 227

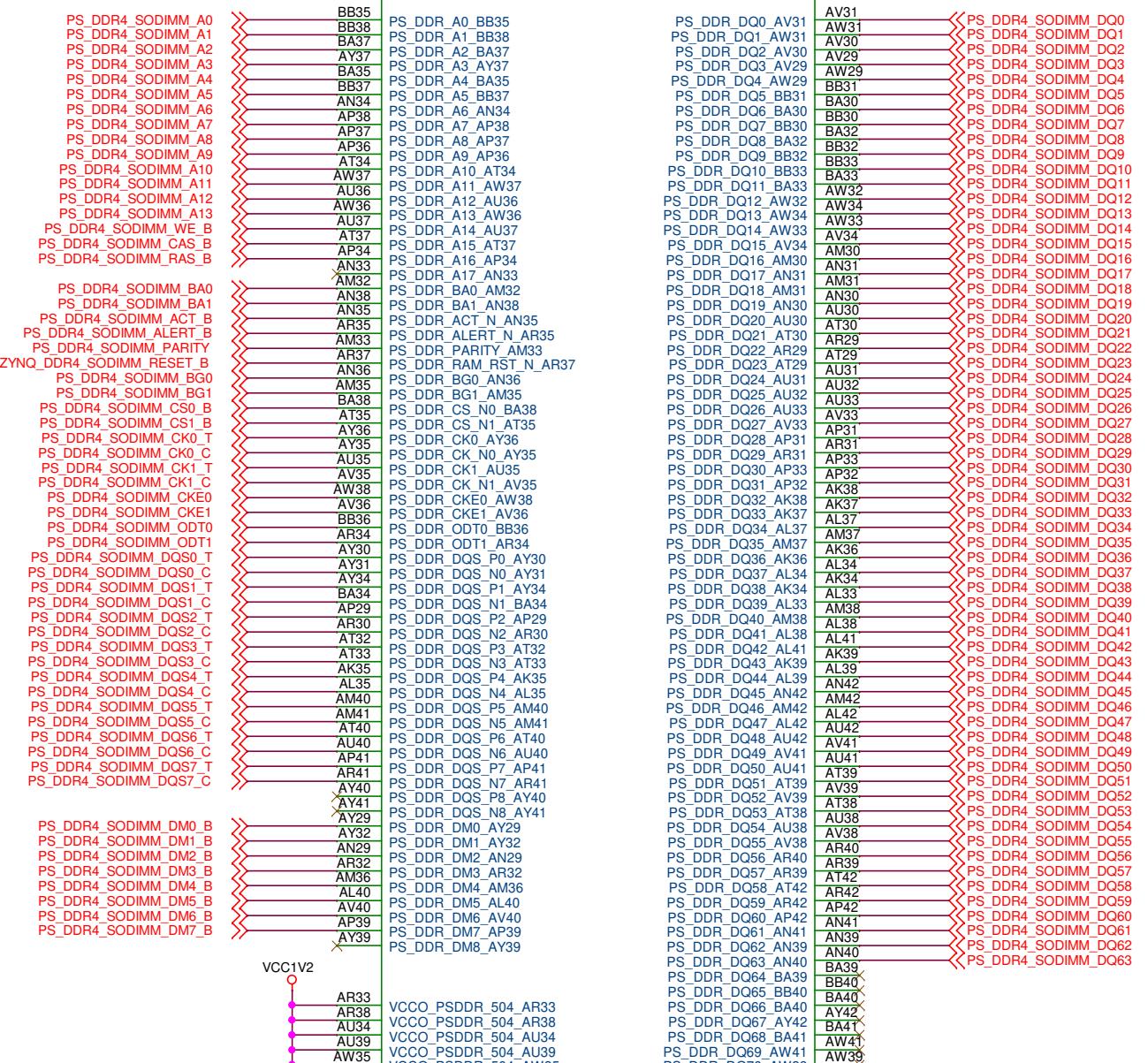
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Engineer: BF	Sheet 9 of 80		







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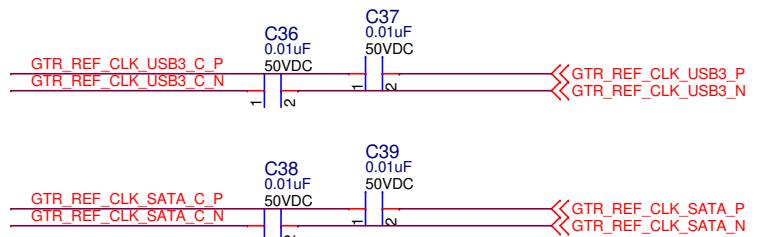


BANK 505
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 PS_MGTRXP0_505_AJ41
 PS_MGTRRXN0_505_AJ42
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 PS_MGTRTXN1_505_AG38
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 PS_MGTRRN1_505_AH40
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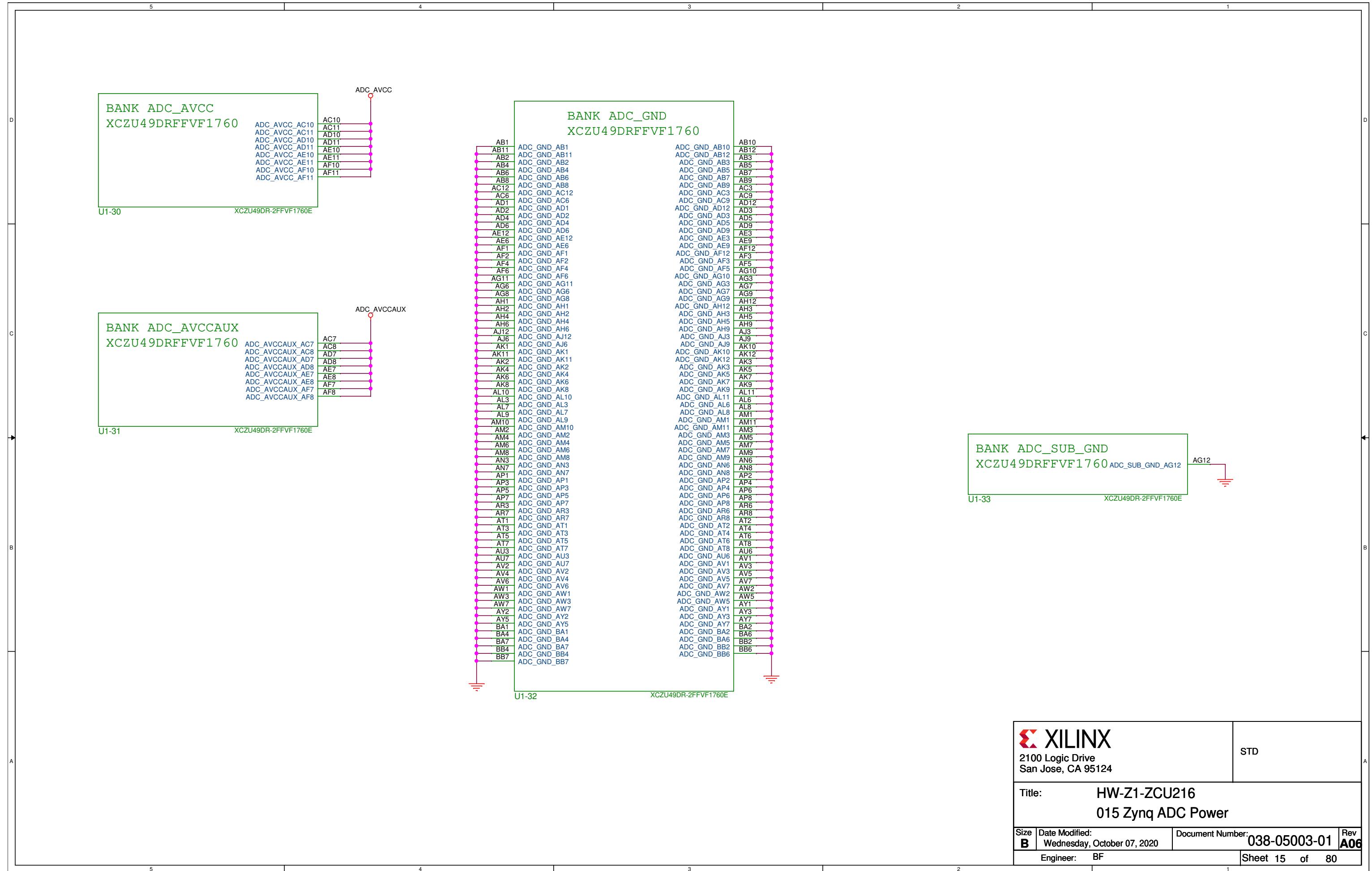
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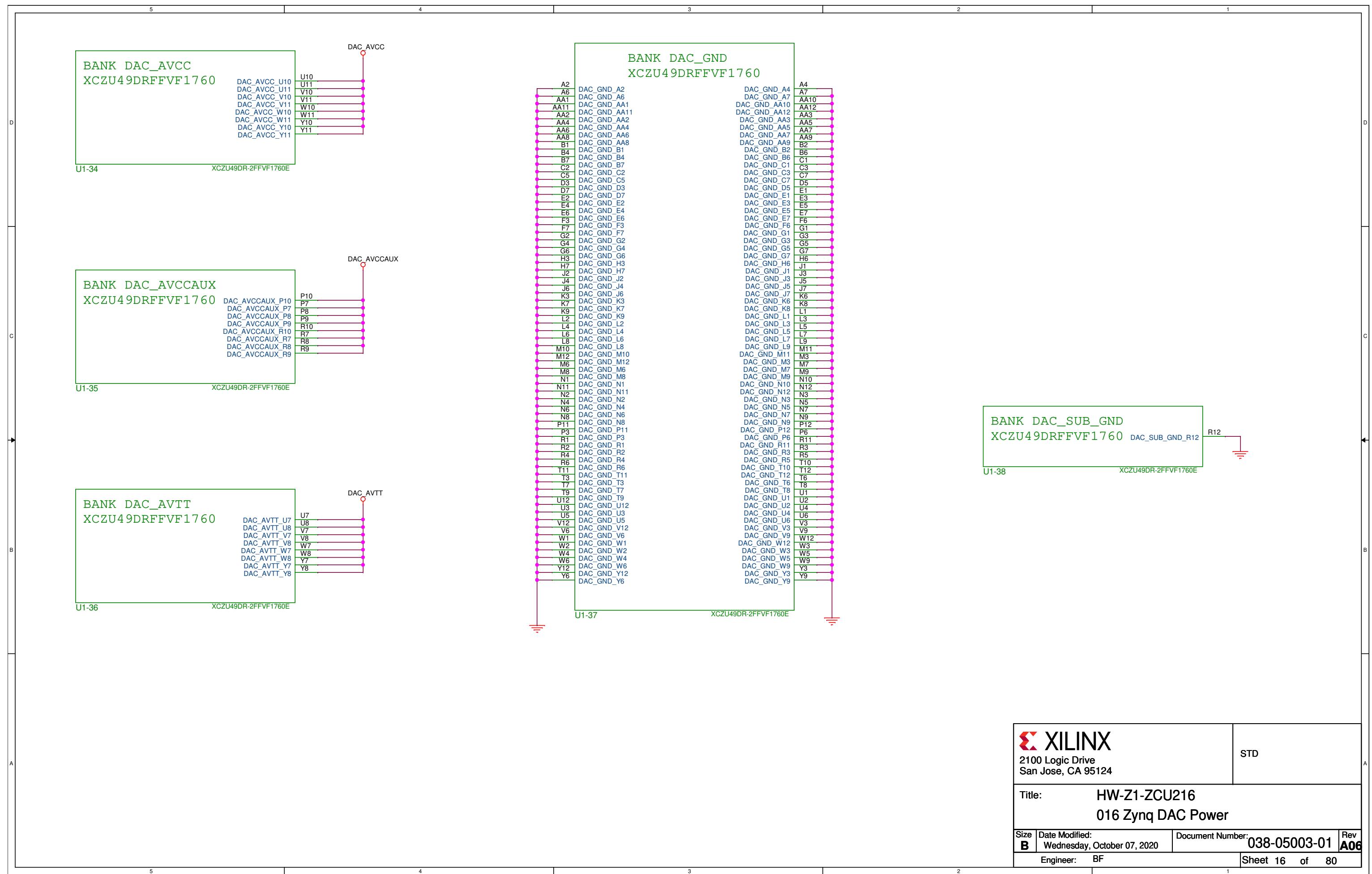


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Title: HW-Z1-ZCU216
014 Zynq Bank 505 - GTR

Size	Date Modified:	Document Number:
B	Wednesday, October 07, 2020	038-05003-01 Rev A06
Engineer: BF		Sheet 14 of 80



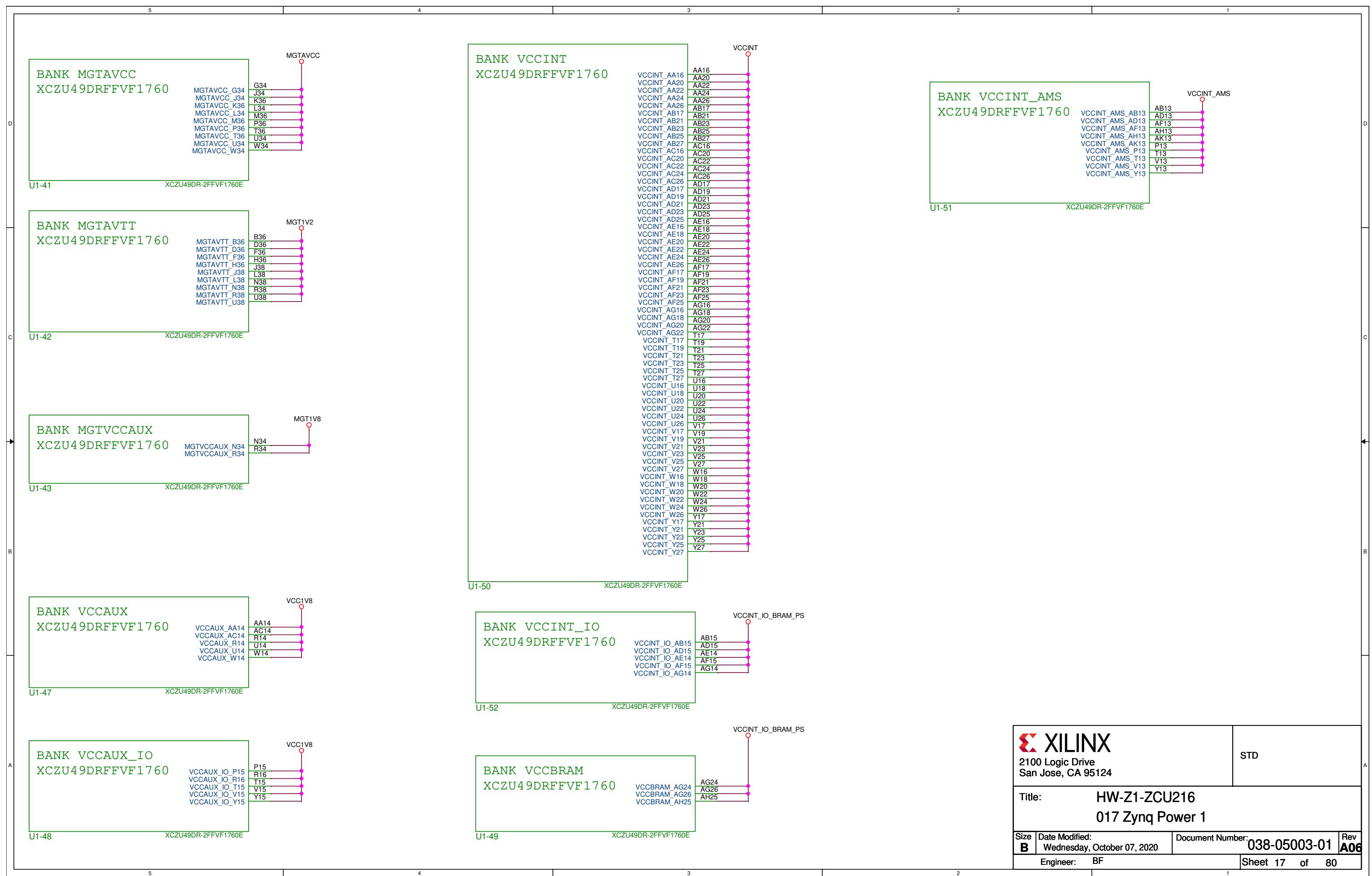


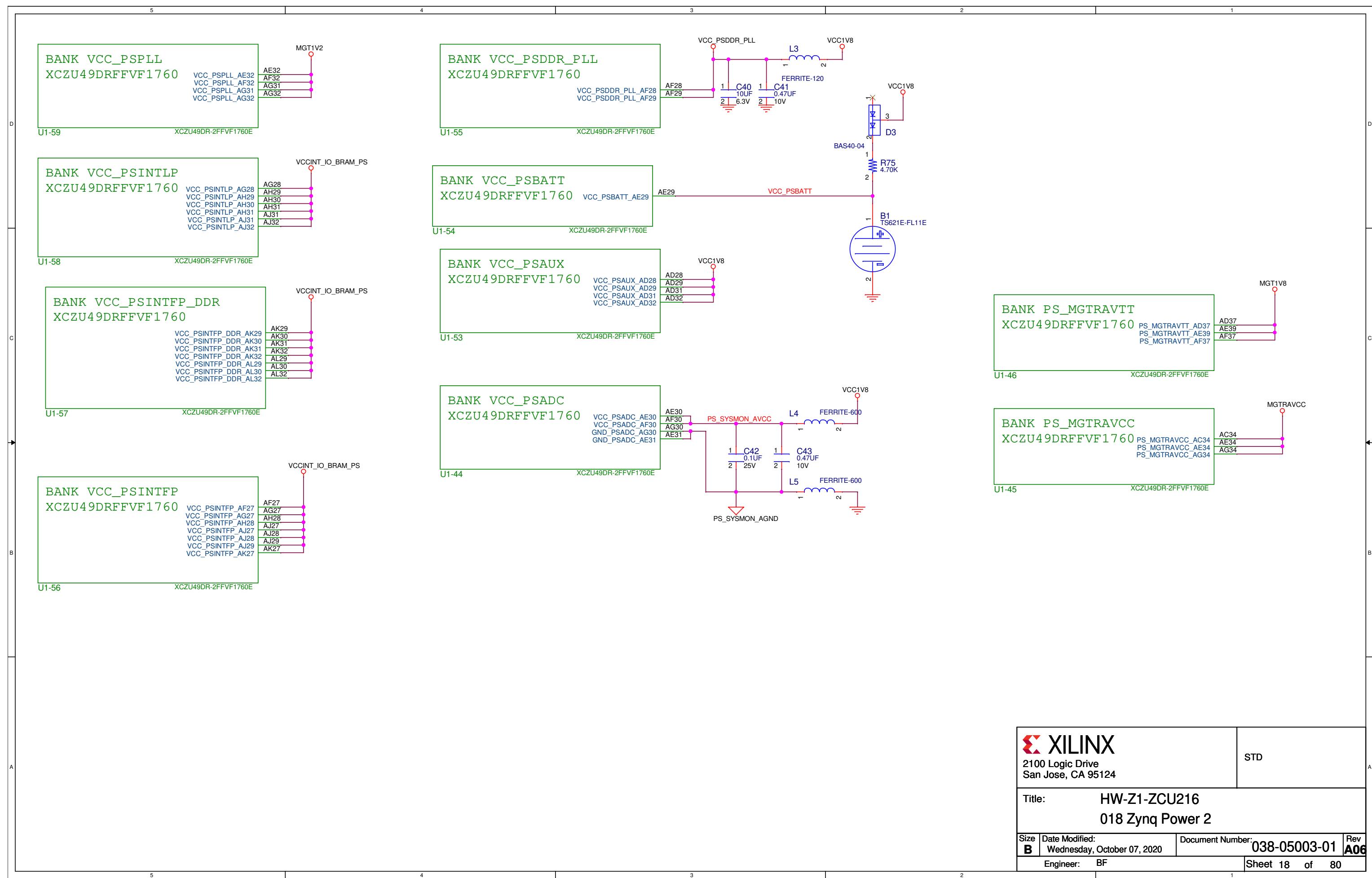
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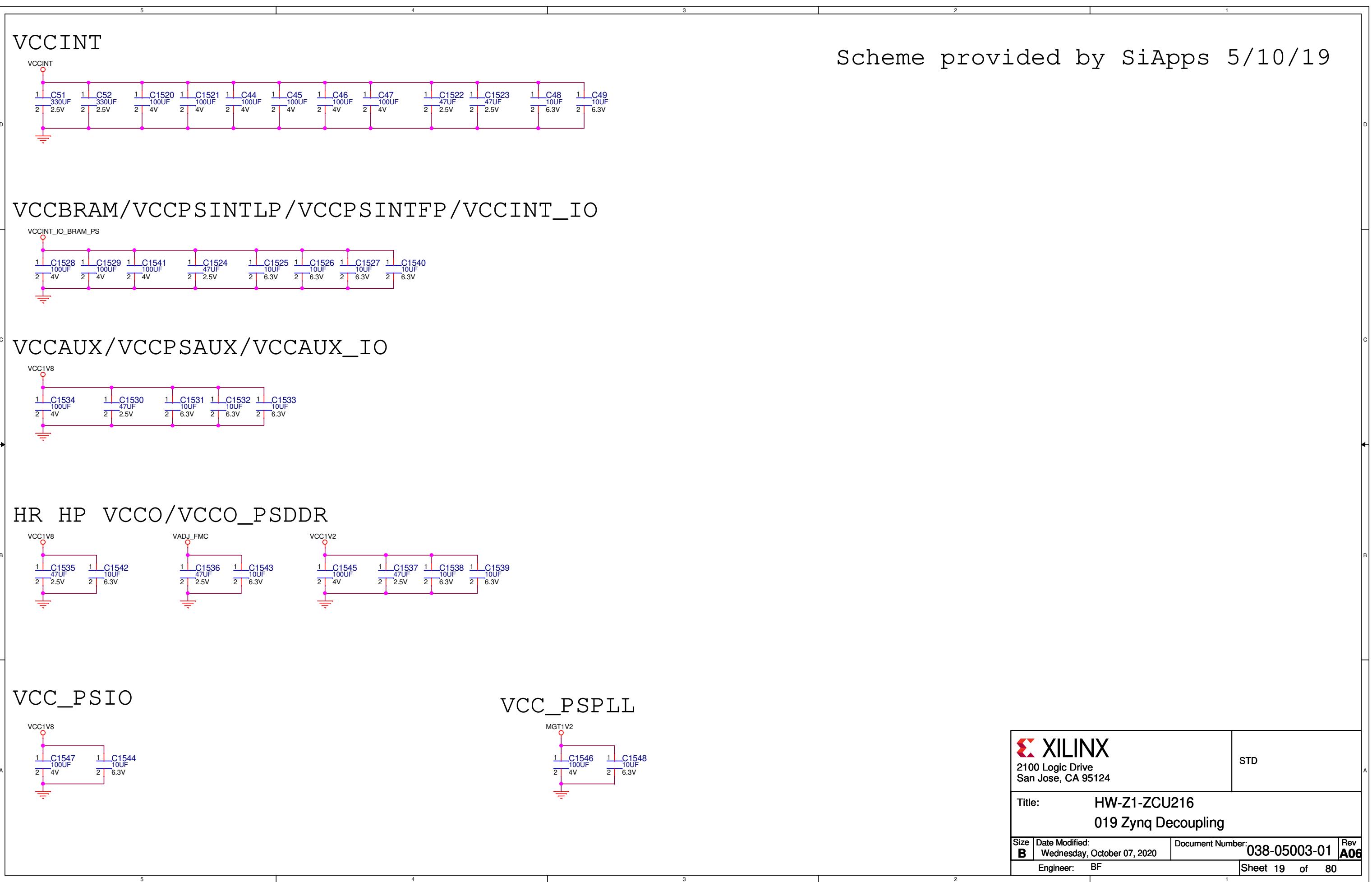
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Size	Date Modified:	Document Number:
B	Wednesday, October 07, 2020	038-05003-01
Engineer: BF	Rev A06	

Sheet 16 of 80

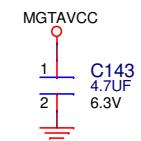




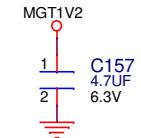


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Engineer: BF	Sheet 19 of 80	

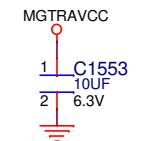
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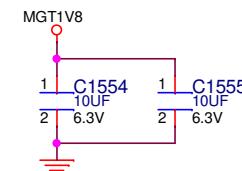
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MGTRAVCC

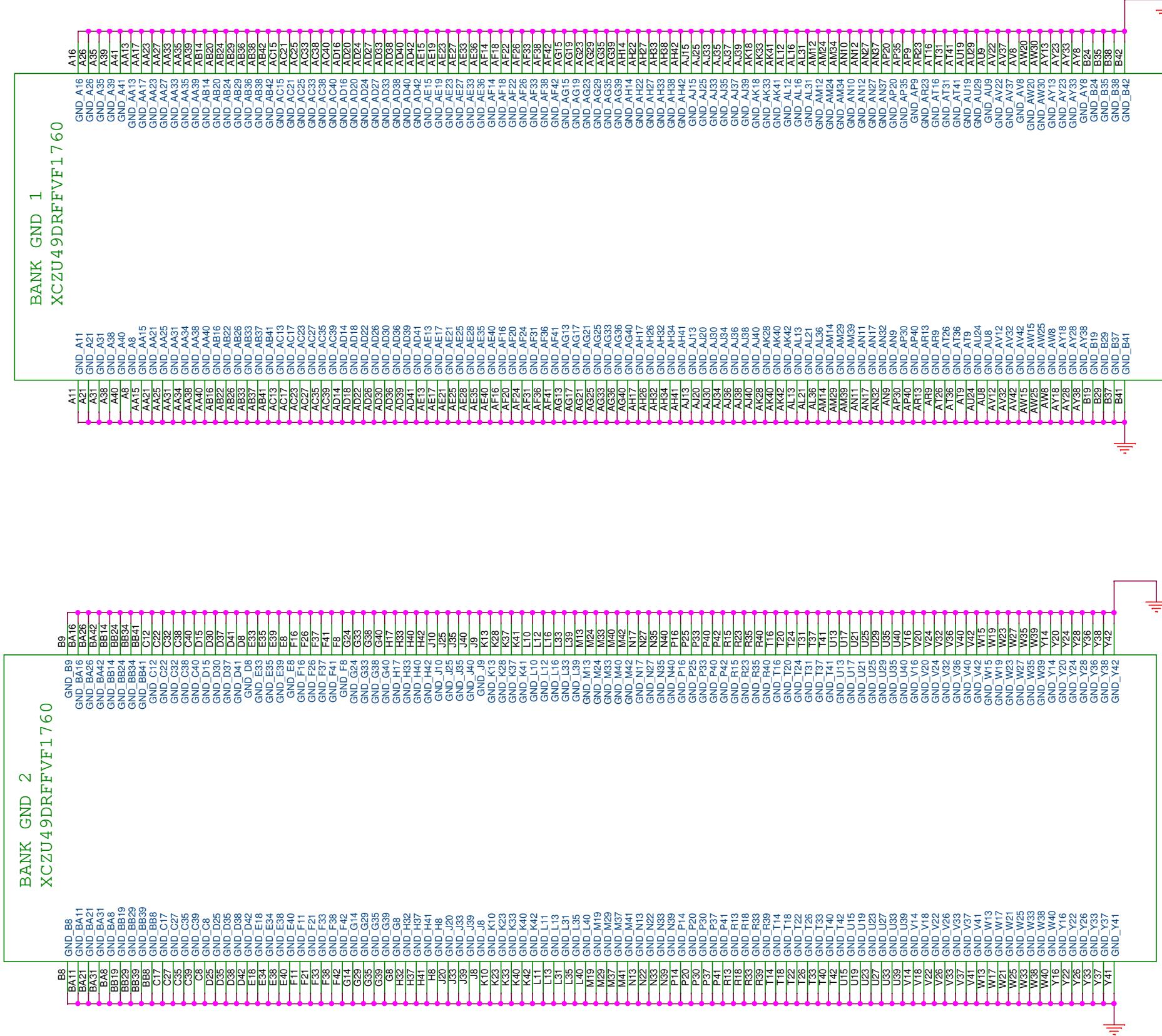


MGTVCCAUX/MGTRAVTT



AMS Scheme from UG583 1.15
GTY scheme from UG567 1.3
GTR scheme from Si Apps 5/10/19

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Engineer: BF	Sheet 20 of 80	

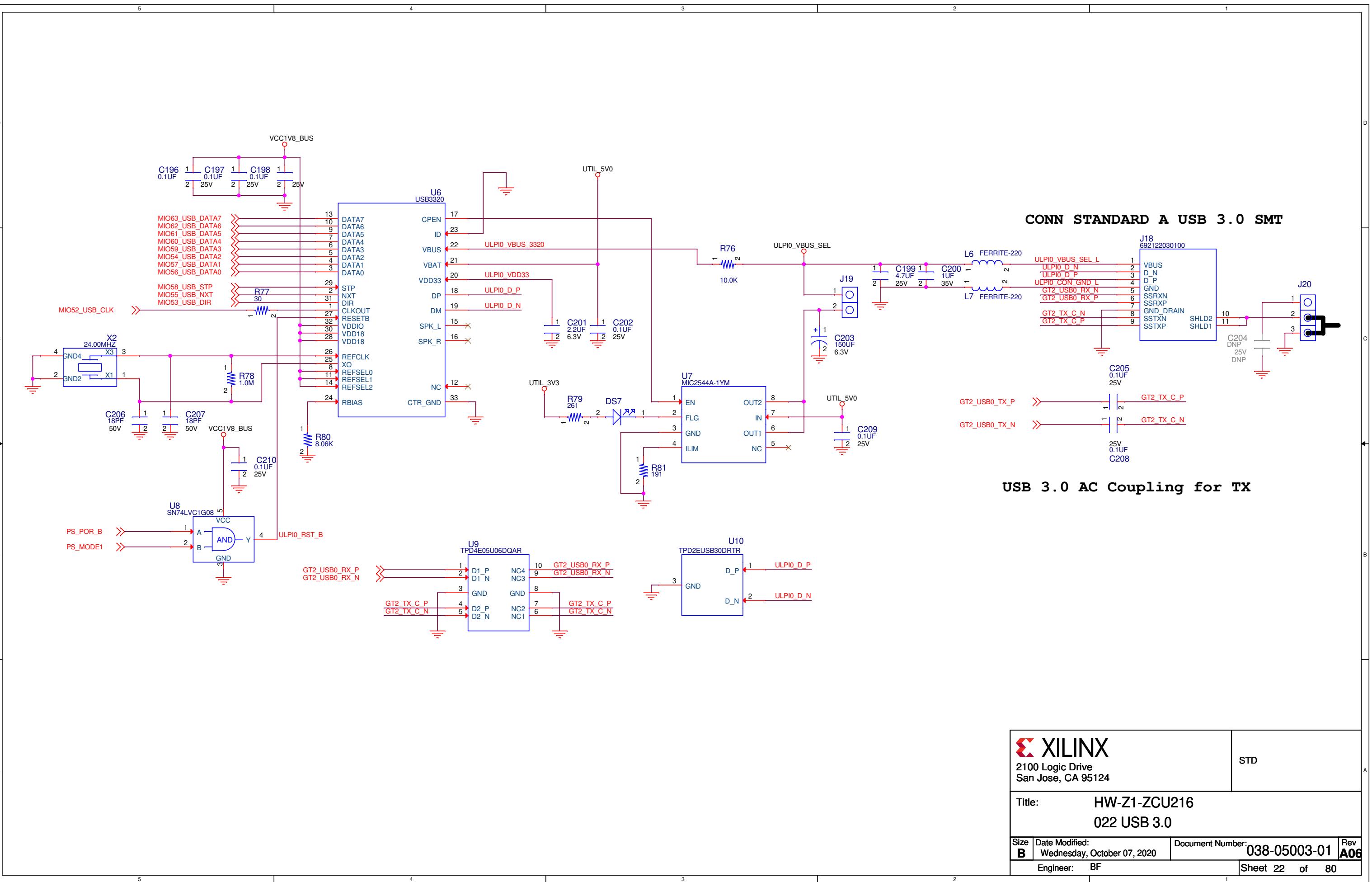


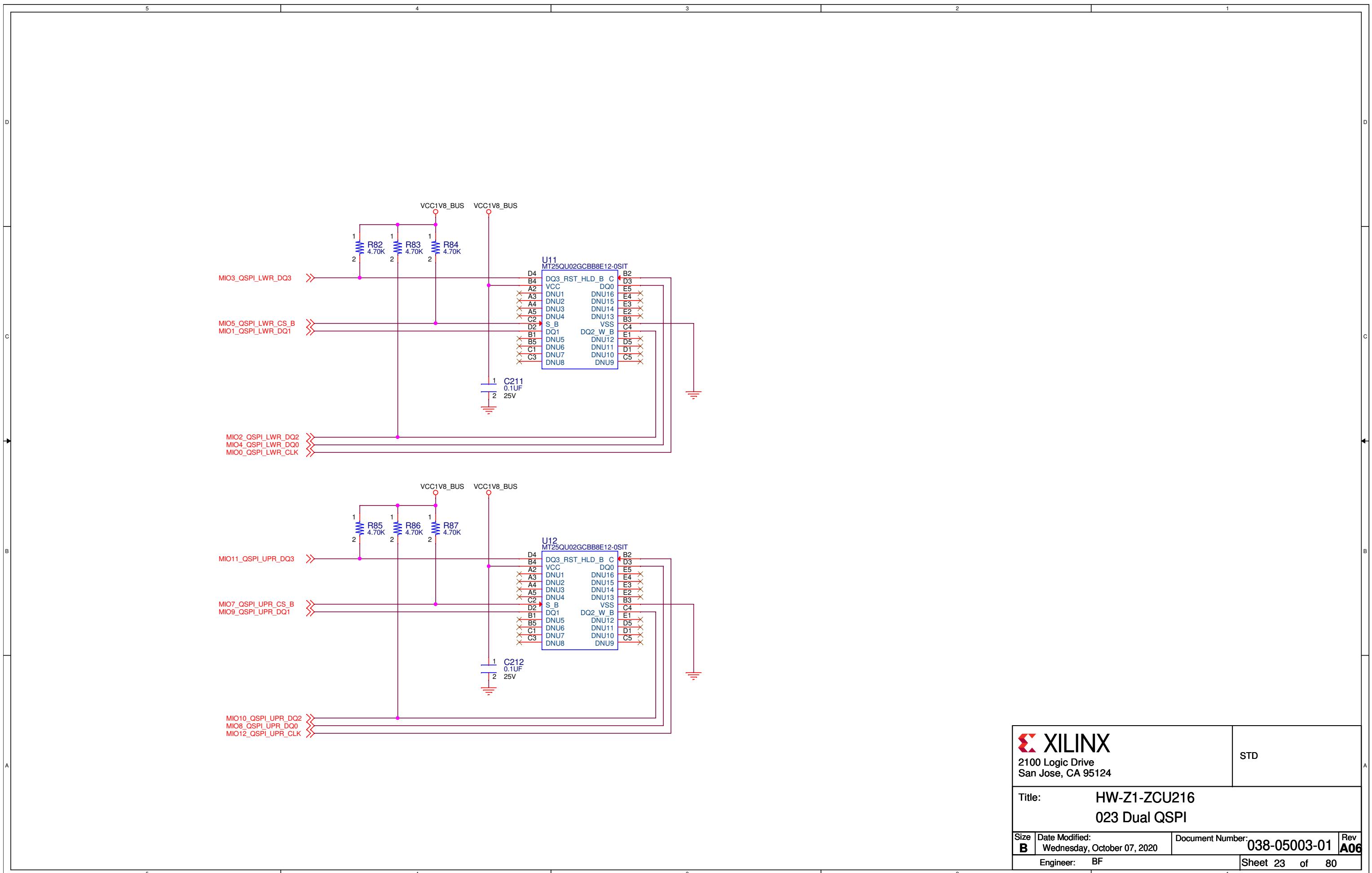
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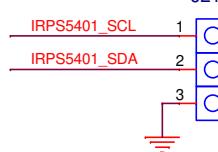
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Engineer:	BF	Sheet 21	of 80



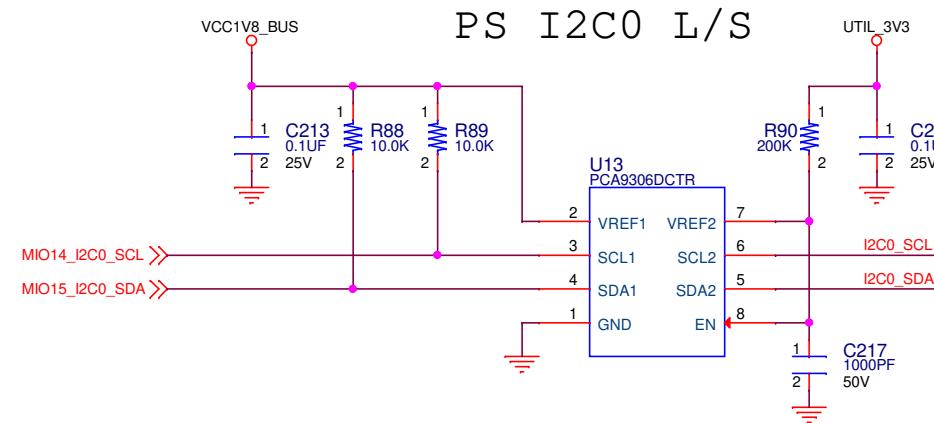


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Document Number: 038-05003-01	Rev: A06
Engineer: BF	Sheet 23 of 80

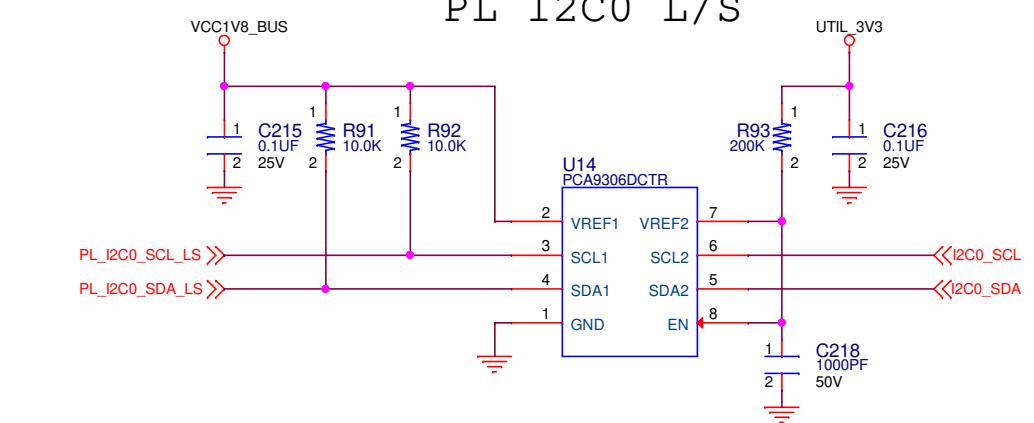
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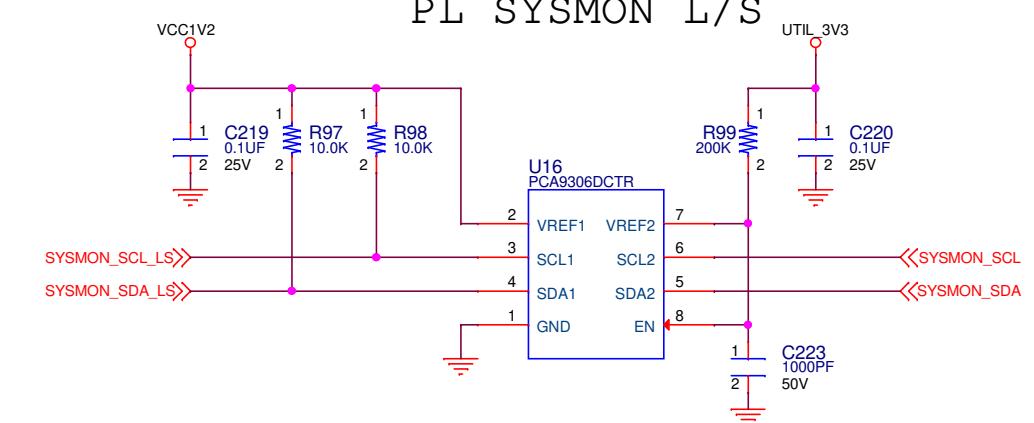
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PL I₂C0 L/S



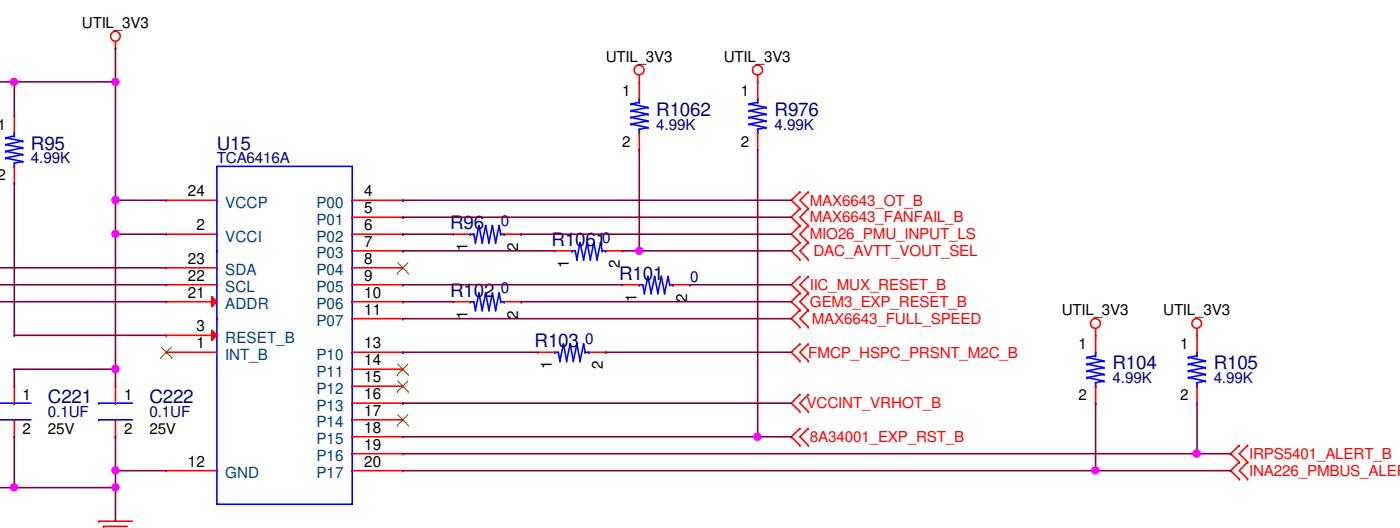
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UTIL_3V3

UTIL_3V3

UTIL_3V3



UTIL_3V3

R107

4.99K

R115

4.99K

C224

0.1uF

25V

R108

4.99K

R109

4.99K

R110

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R111

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R112

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R113

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R114

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R115

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R116

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R124

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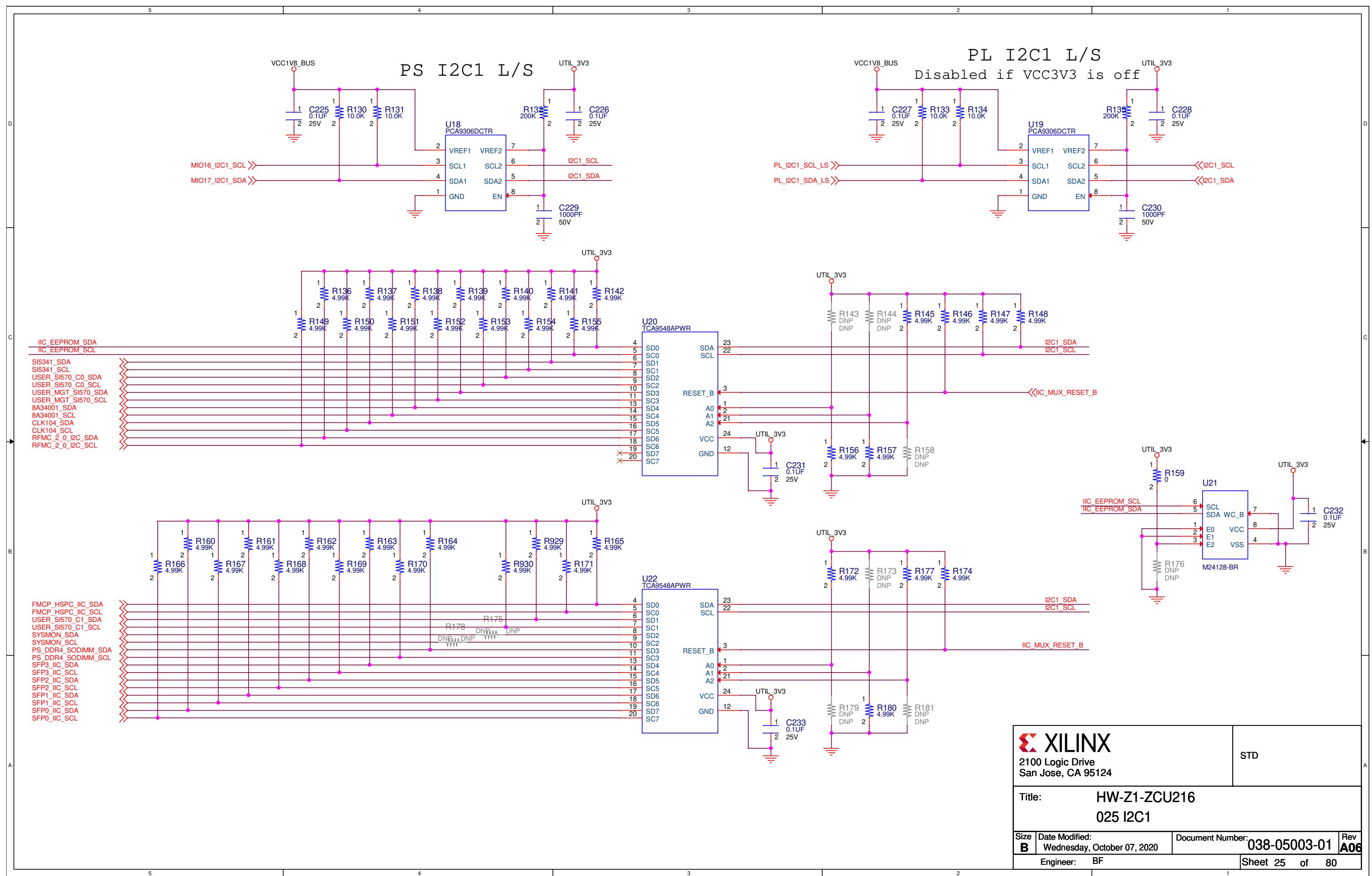
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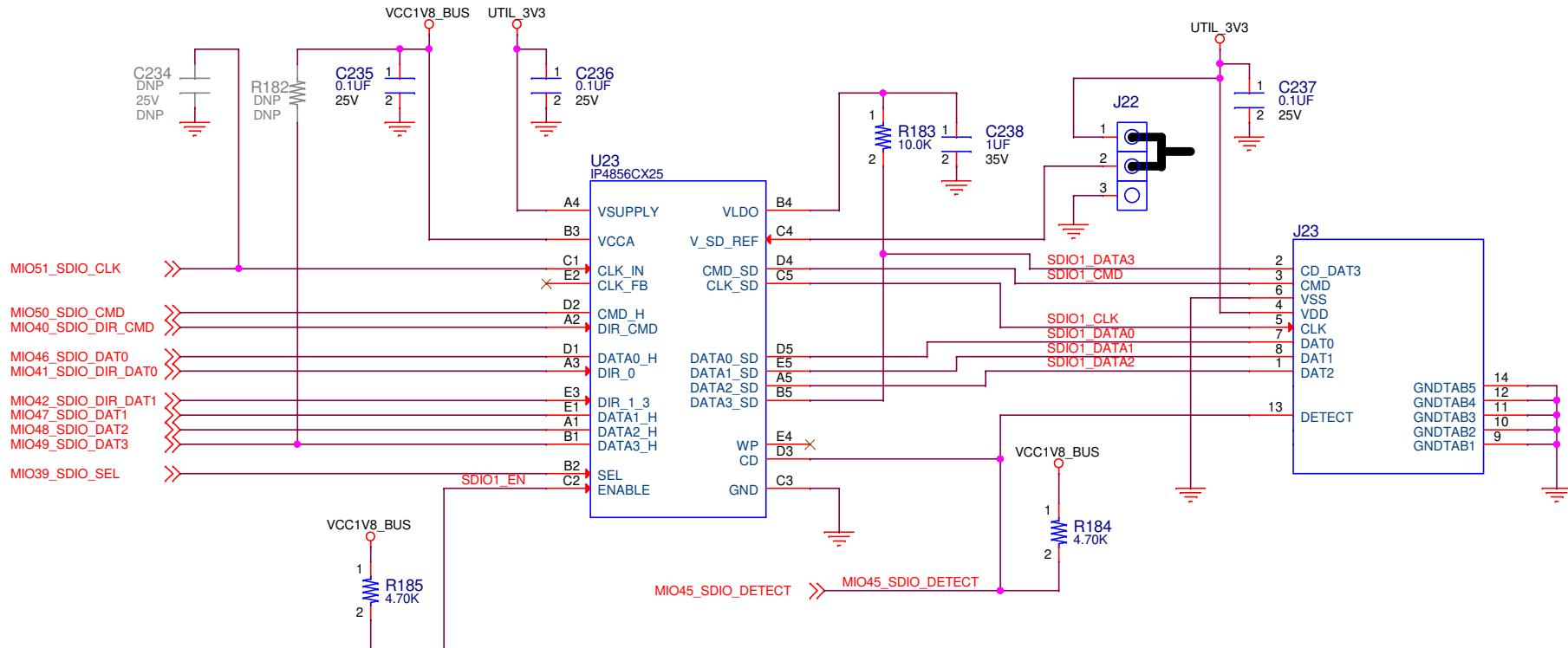
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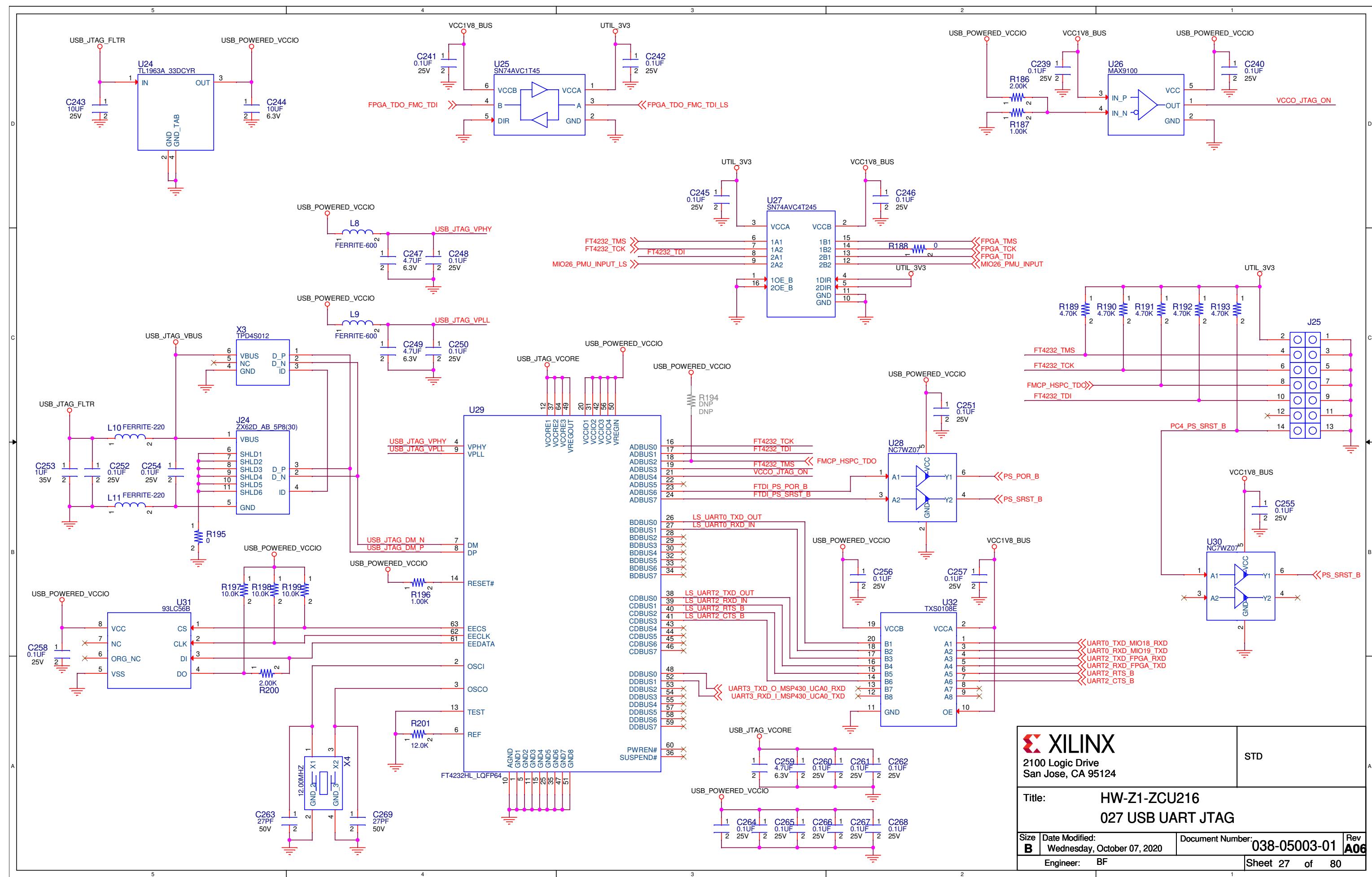
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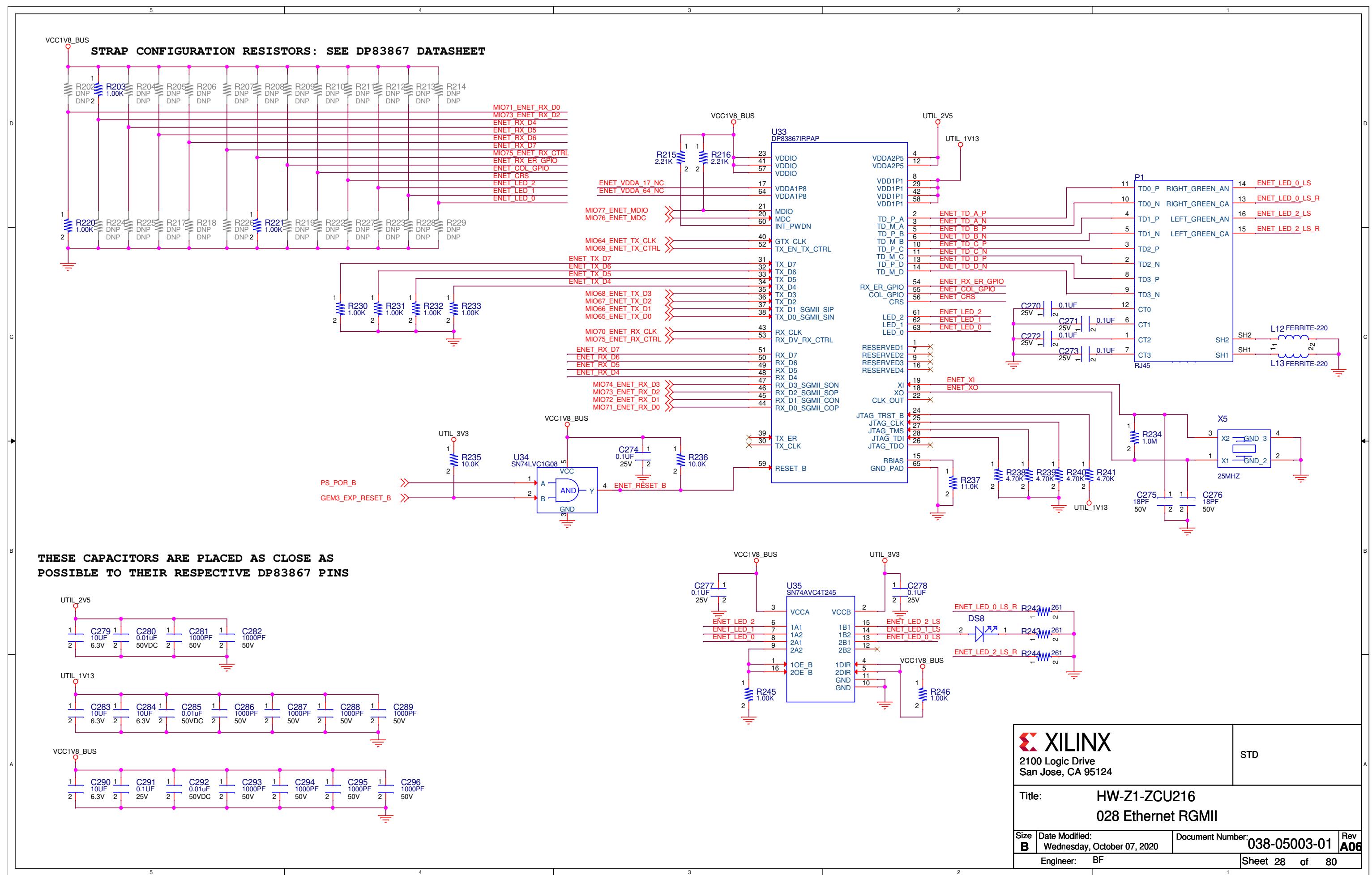
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B Wednesday, October 07, 2020 038-05003-01 **A06**

Engineer: BF Sheet 25 of 80







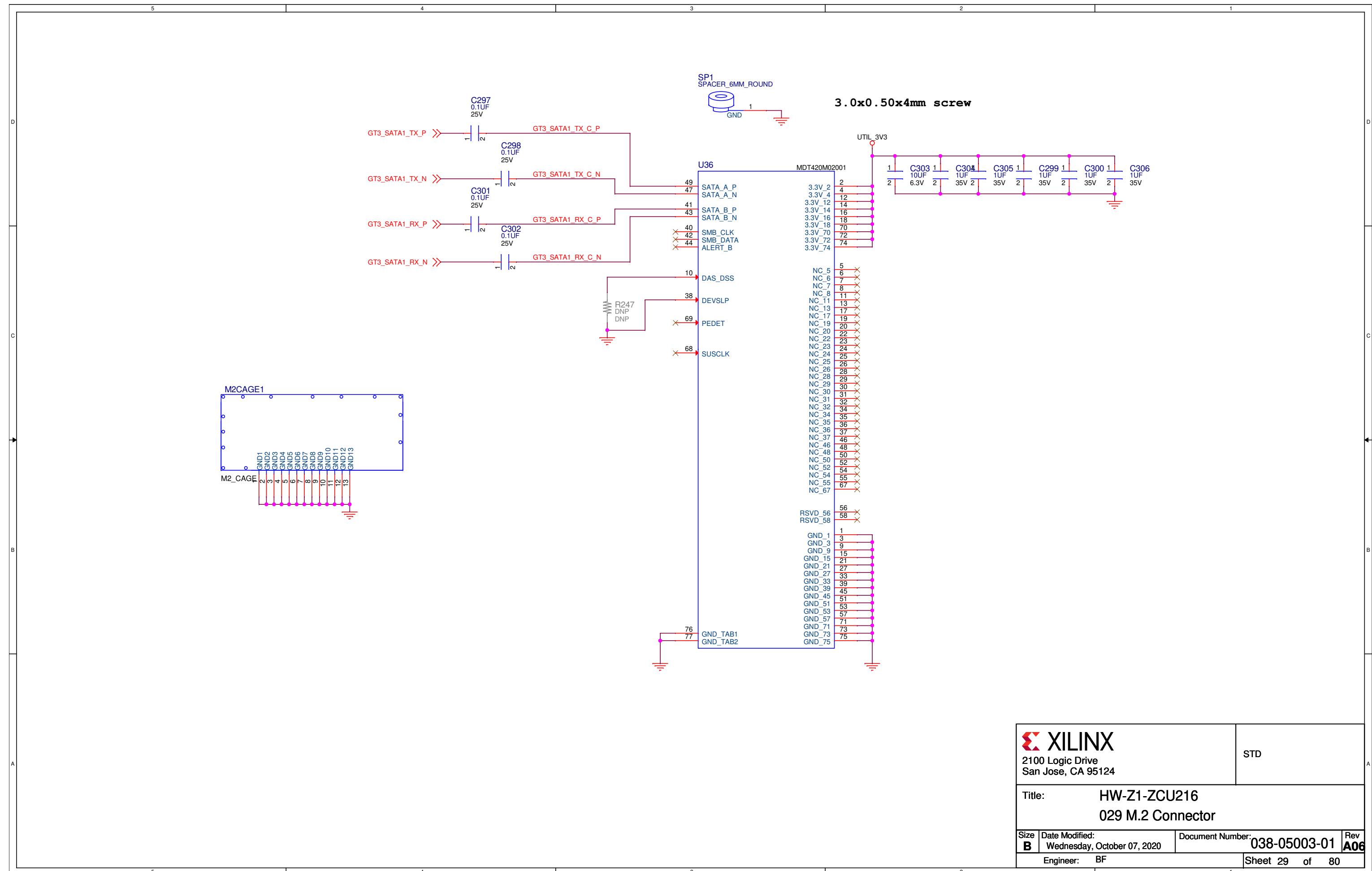
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B	Wednesday, October 07, 2020	038-05003-01 Rev A06
Engineer:	BF	Sheet 28 of 80



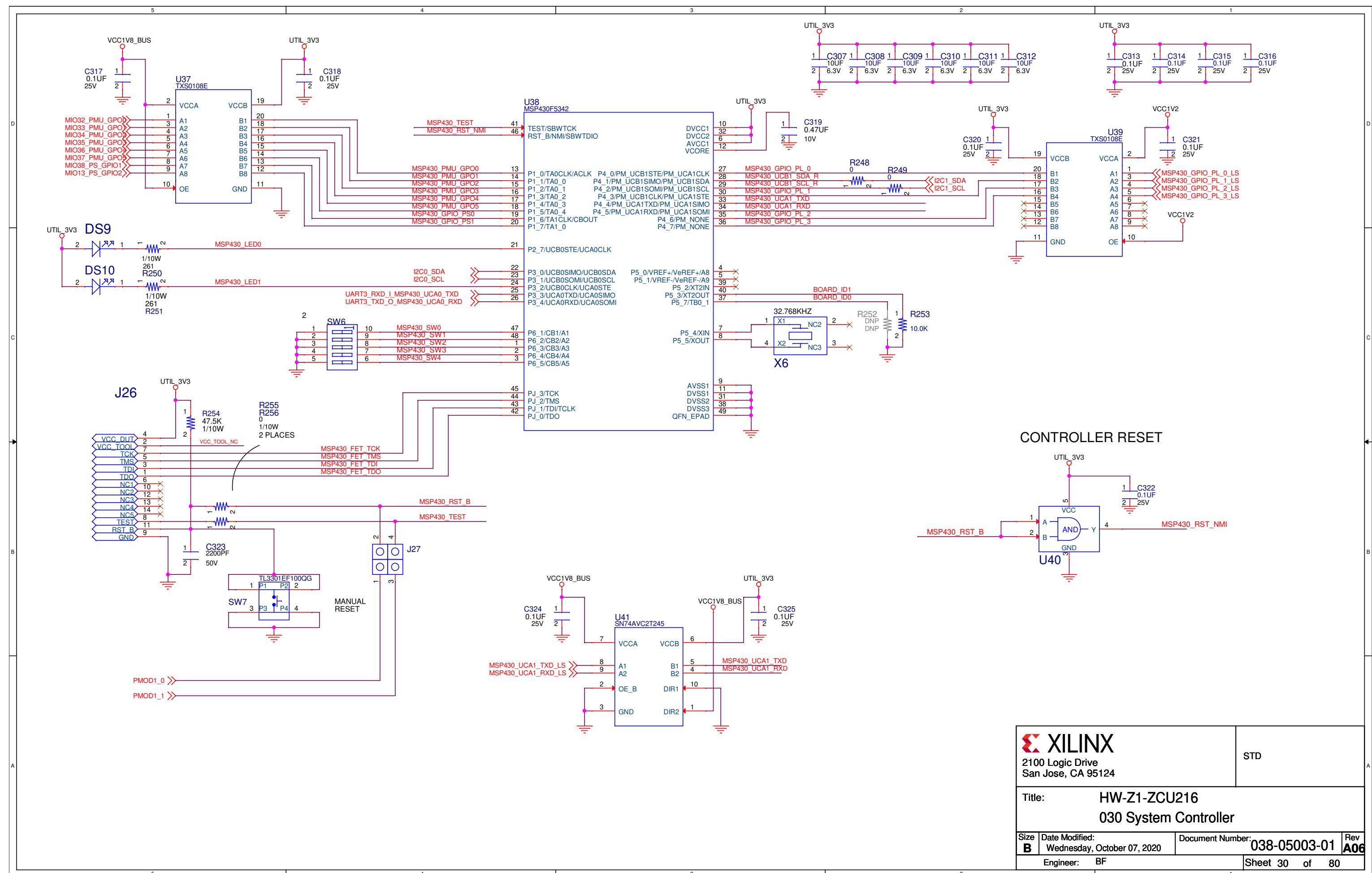
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Size	Date Modified:	Document Number:	Rev
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Engineer: BF	Sheet 29 of 80		



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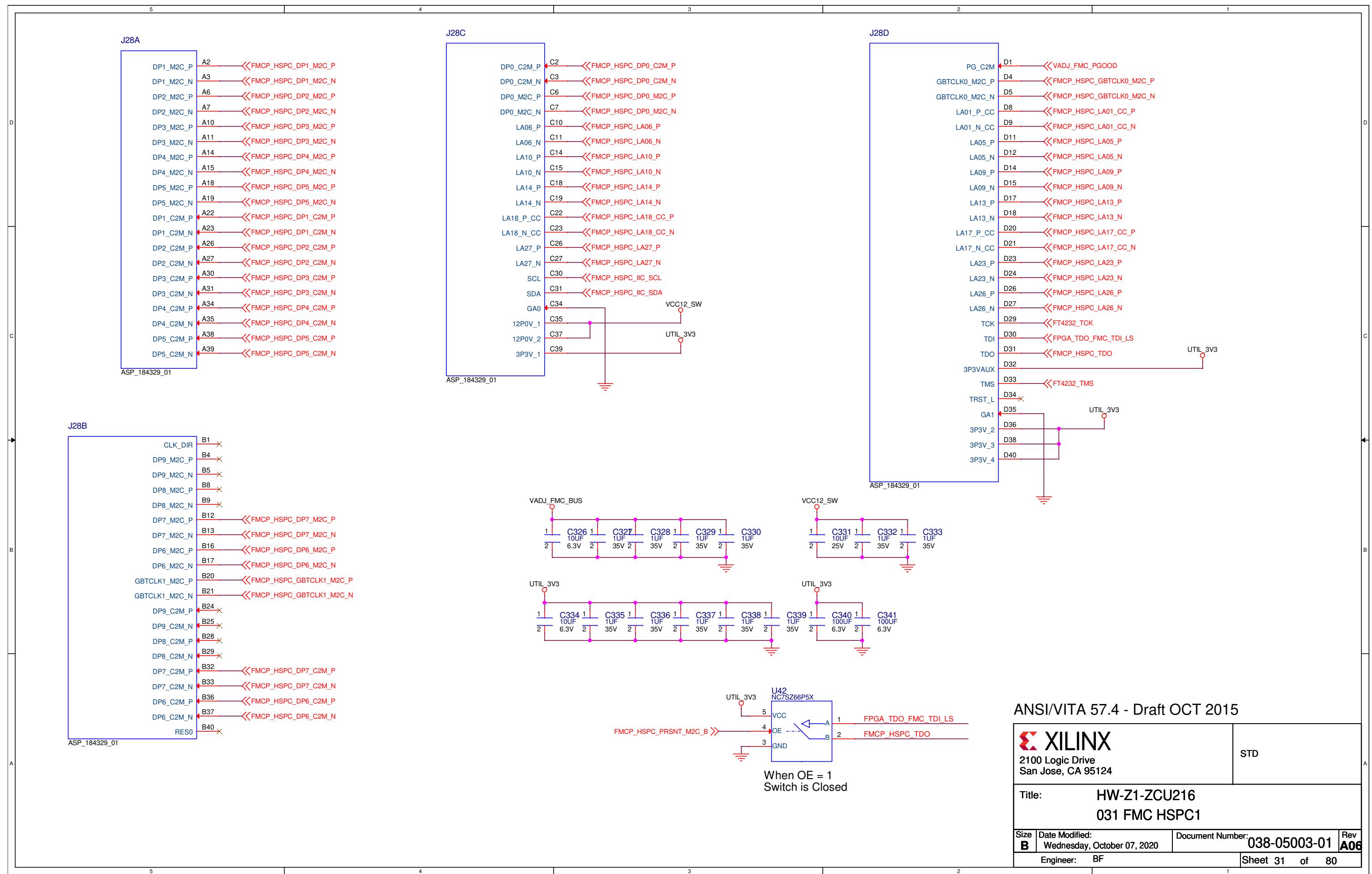
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030 System Controller

Size	Date Modified:	Document Number:
B	Wednesday, October 07, 2020	038-05003-01
		Rev A06

Engineer: BF

Sheet 30 of 80



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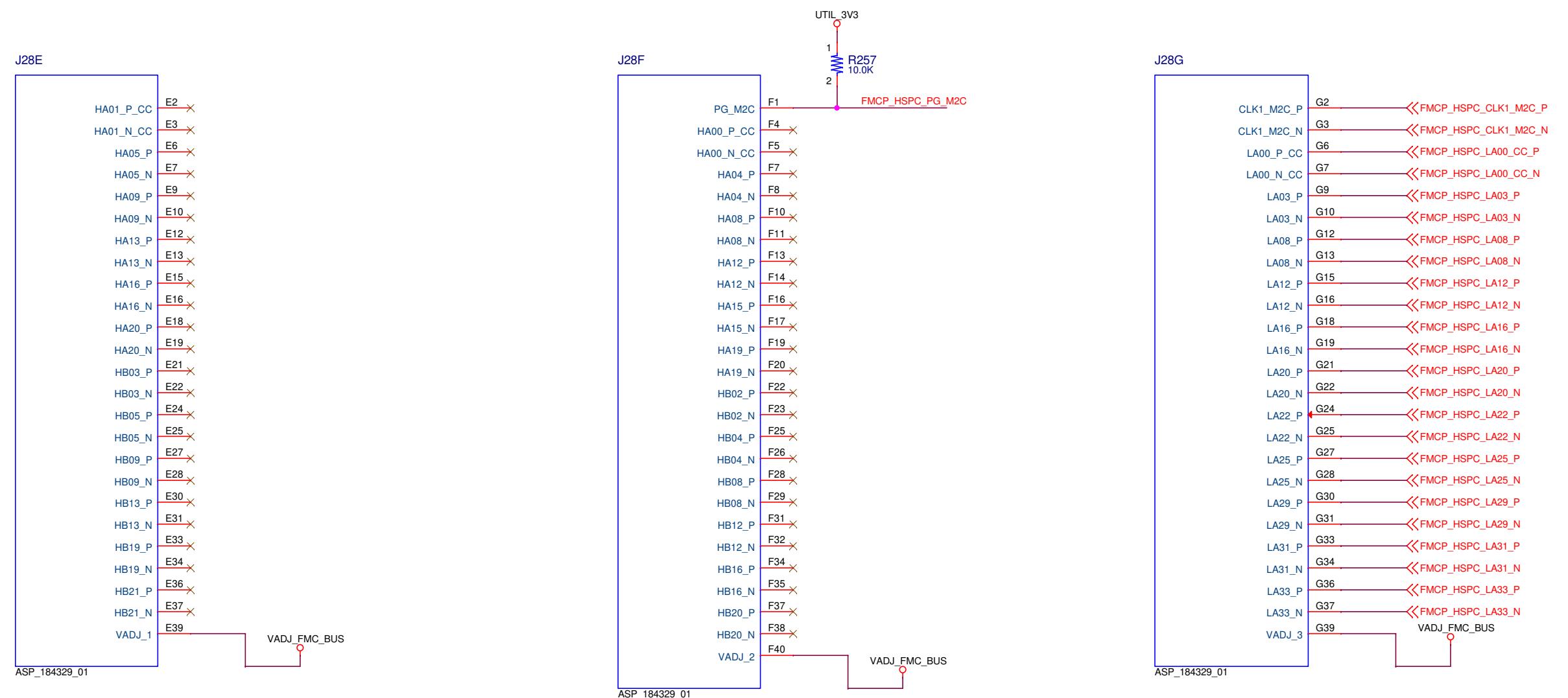


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Size	Date Modified:	Document Number:	Rev
B	Wednesday, October 07, 2020	038-05003-01	A06
Engineer: BF	Sheet 31 of 80		



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STD

Title: HW-Z1-ZCU216
032 FMC HSPC2

Size	Date Modified:	Document Number:
B	Wednesday, October 07, 2020	038-05003-01 Rev A06
Engineer:	BF	

Sheet 32 of 80



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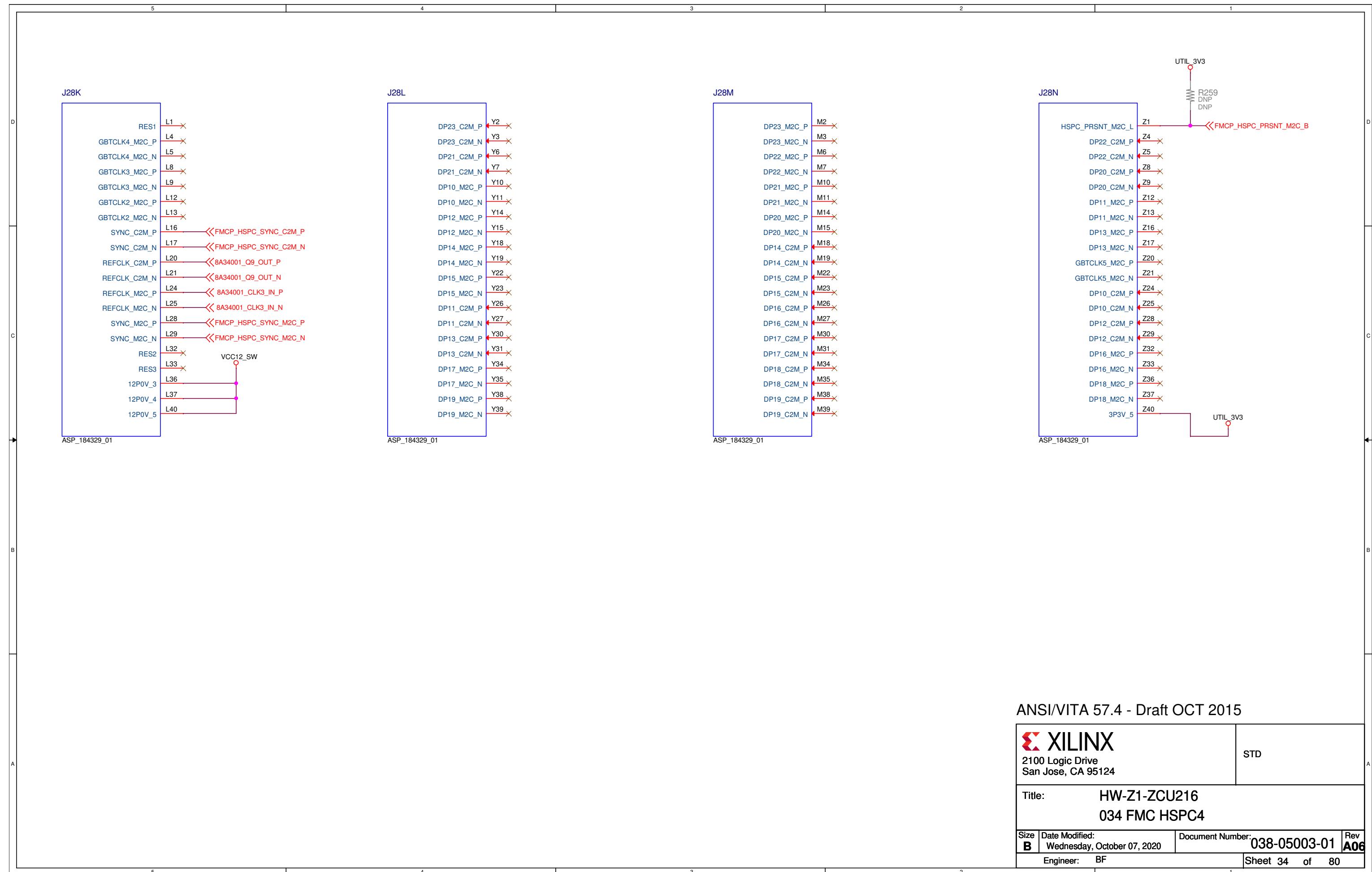


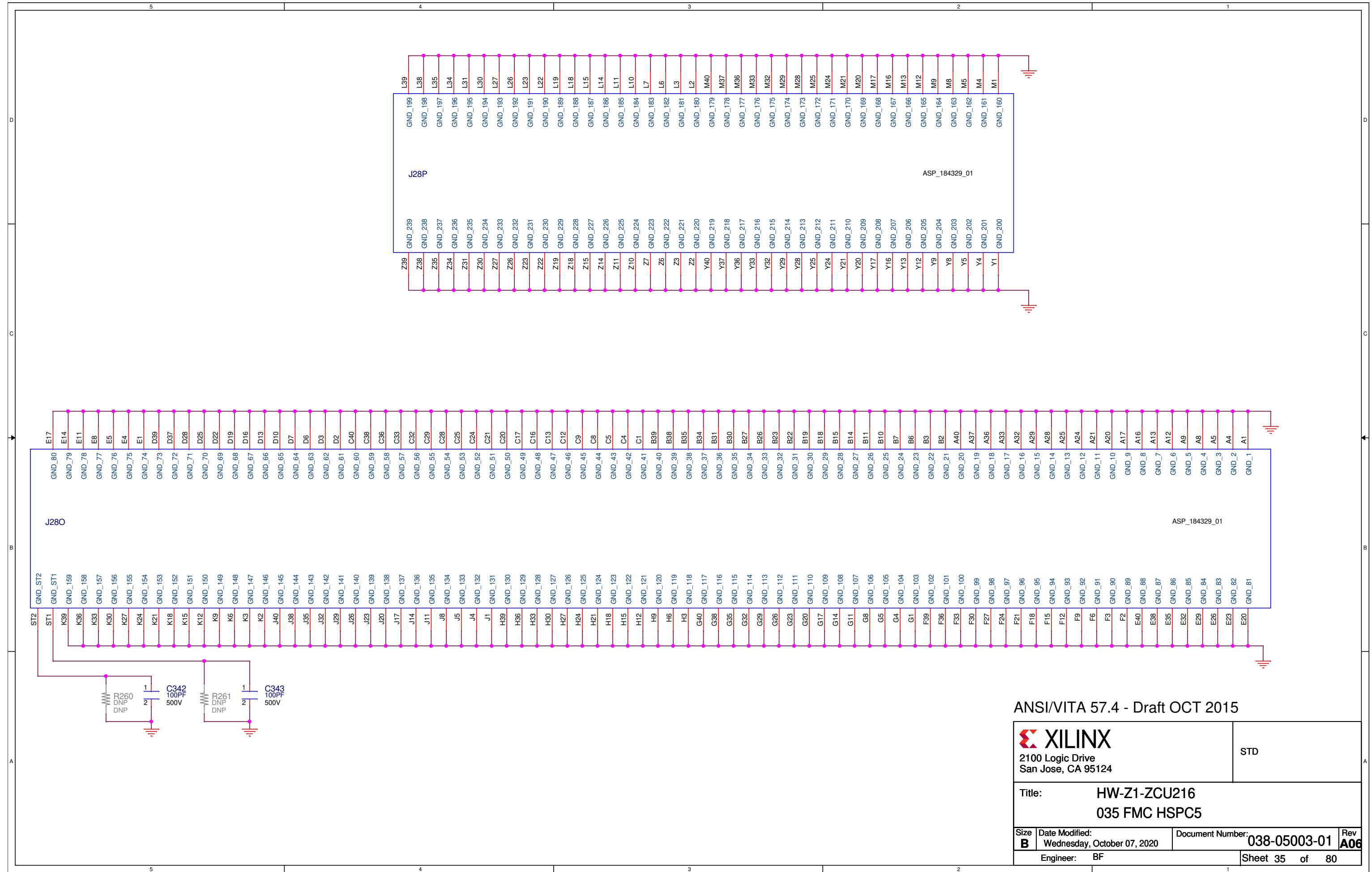
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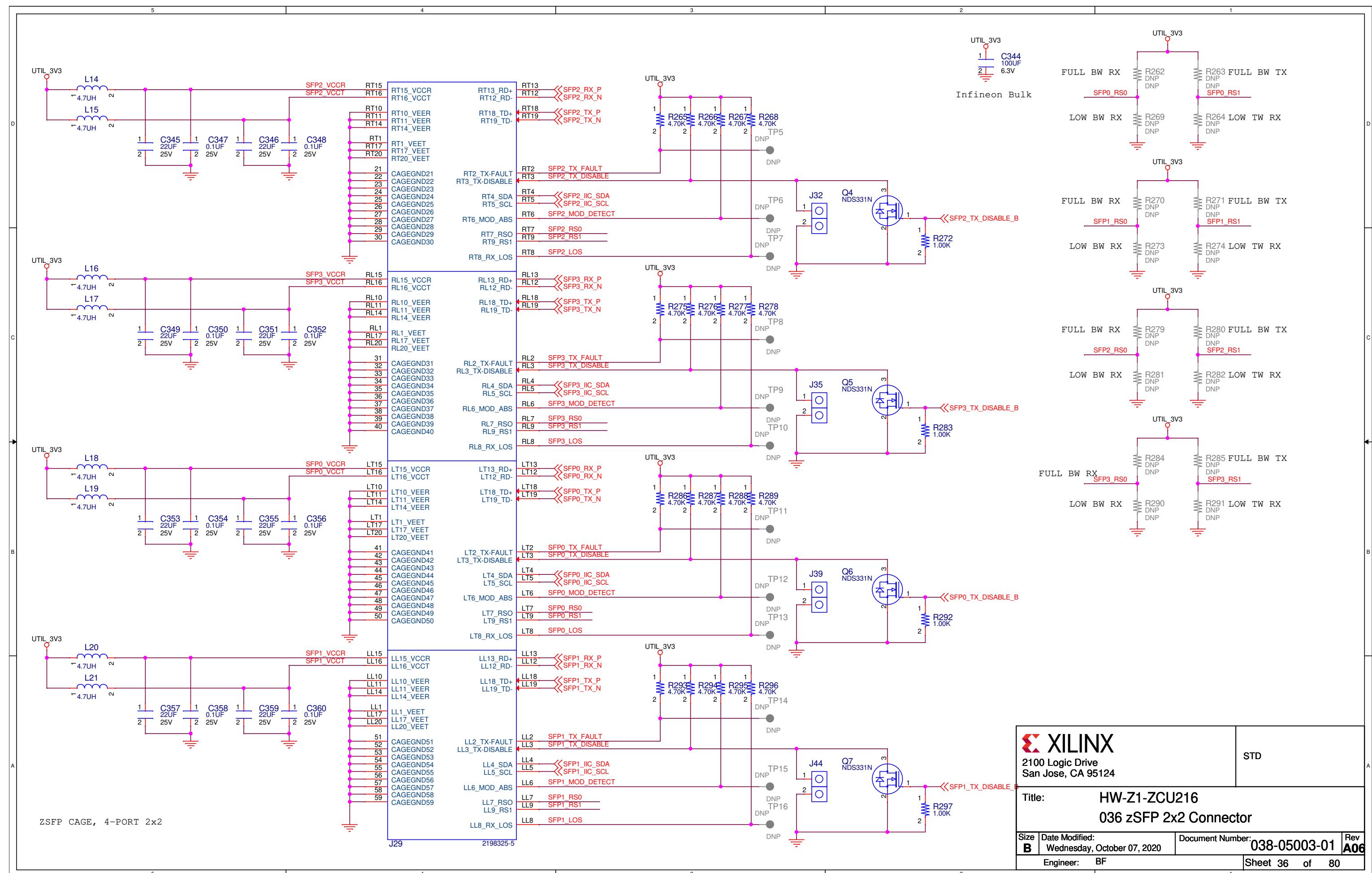
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Size	Date Modified:	Document Number:
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Engineer: BF		Sheet 33 of 80







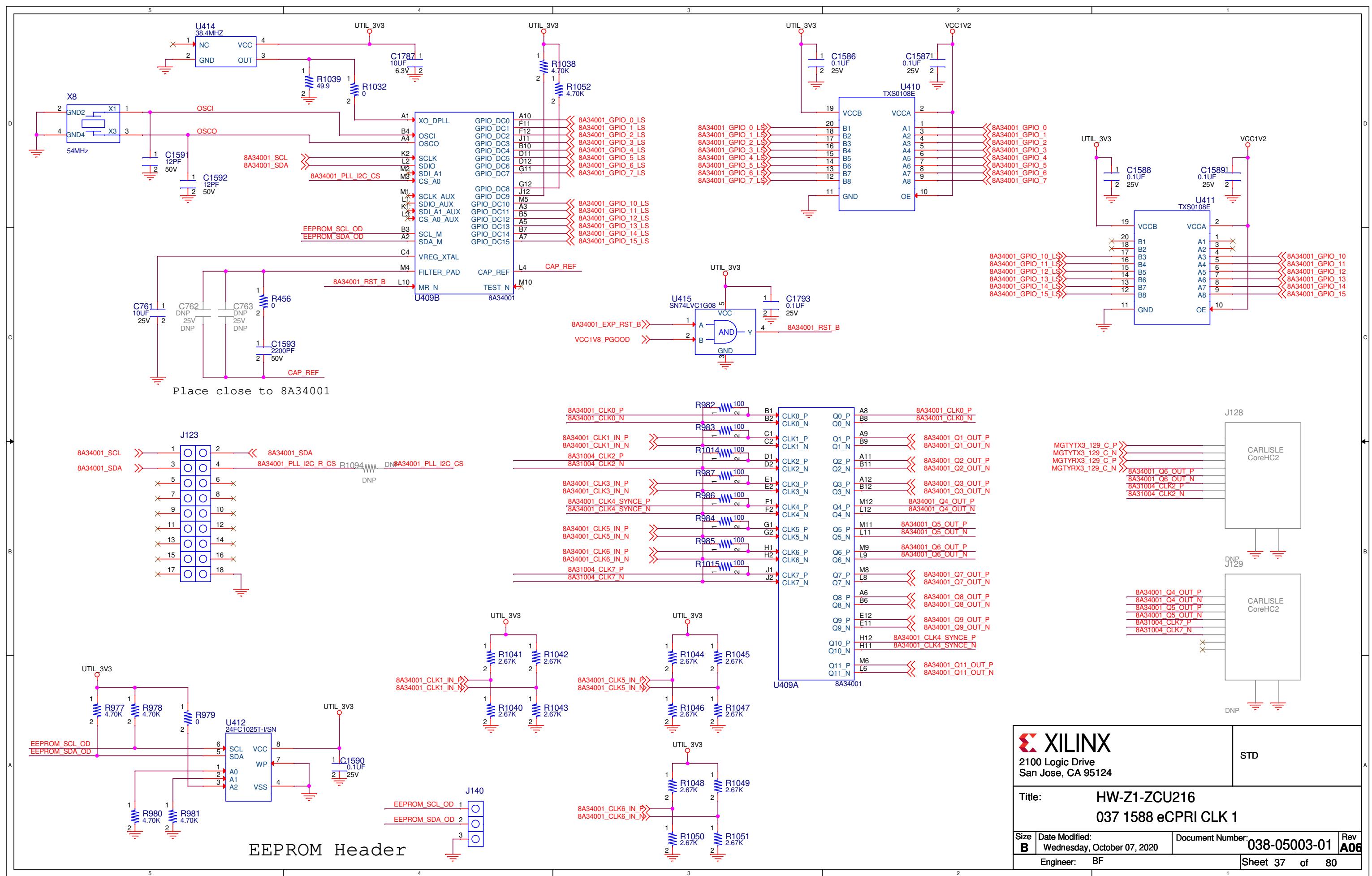
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Size	Date Modified:	Document Number:	Rev
B	Wednesday, October 07, 2020	038-05003-01	A06
		Engineer: BF	Sheet 36 of 80



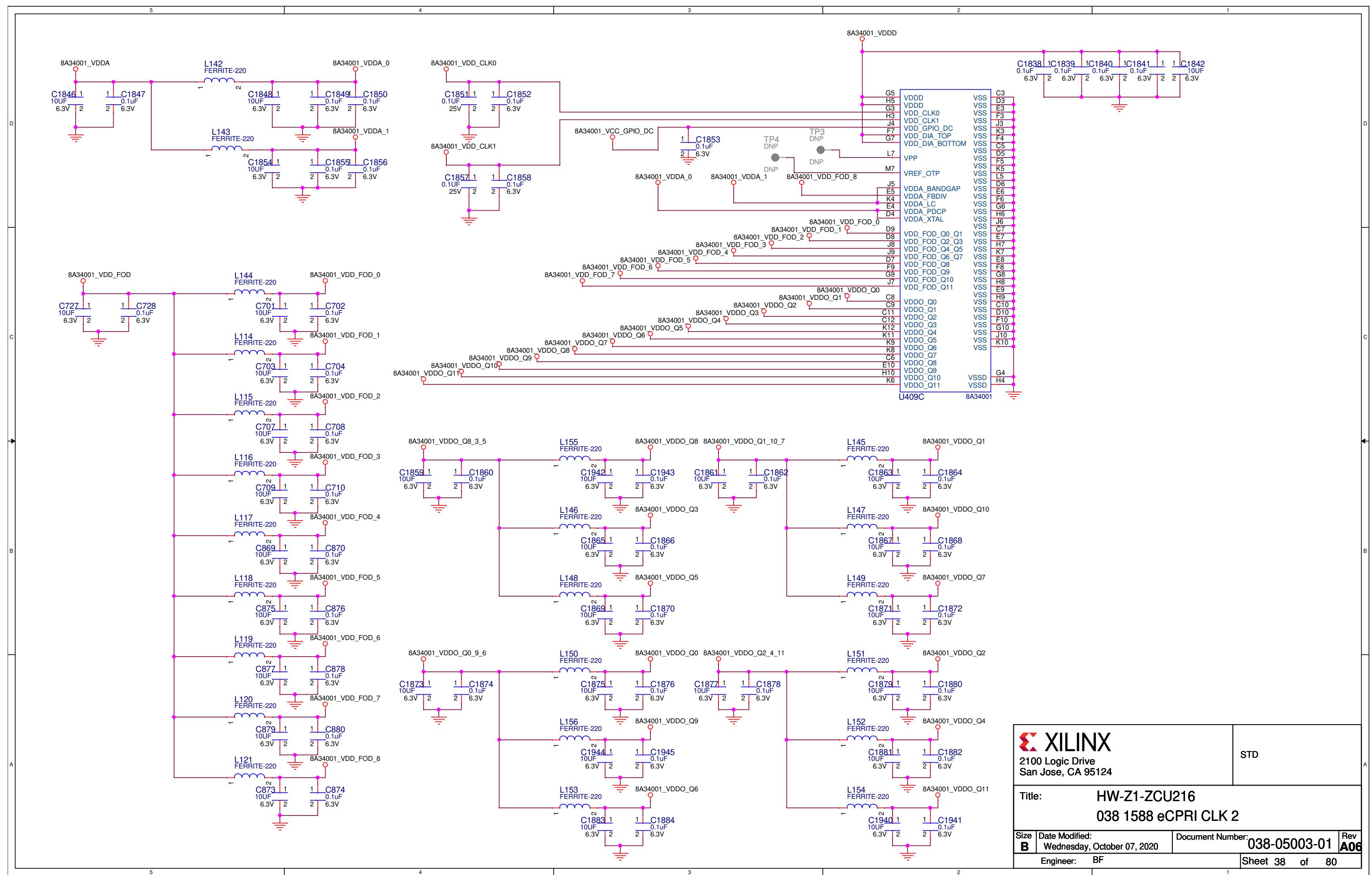
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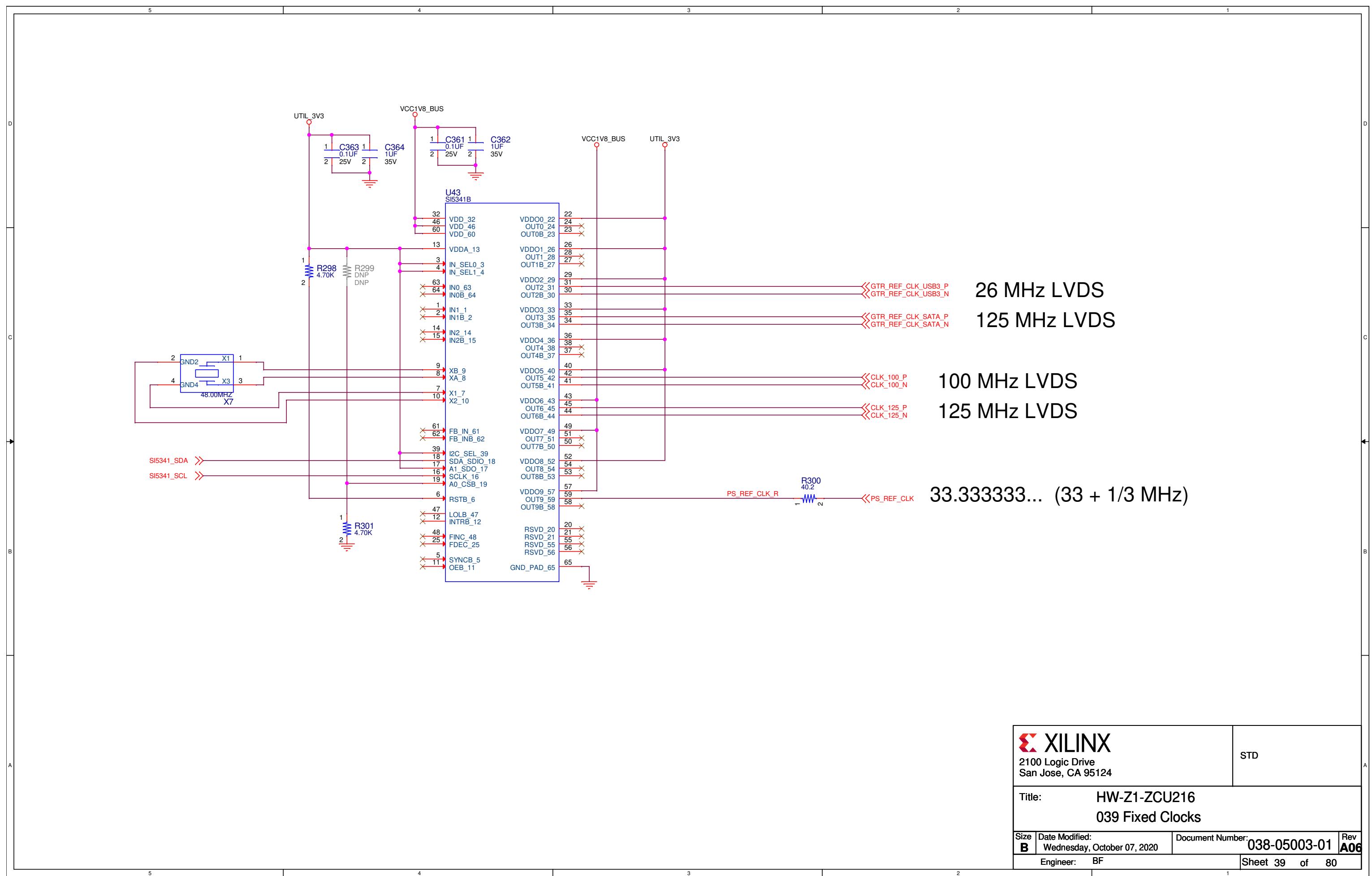
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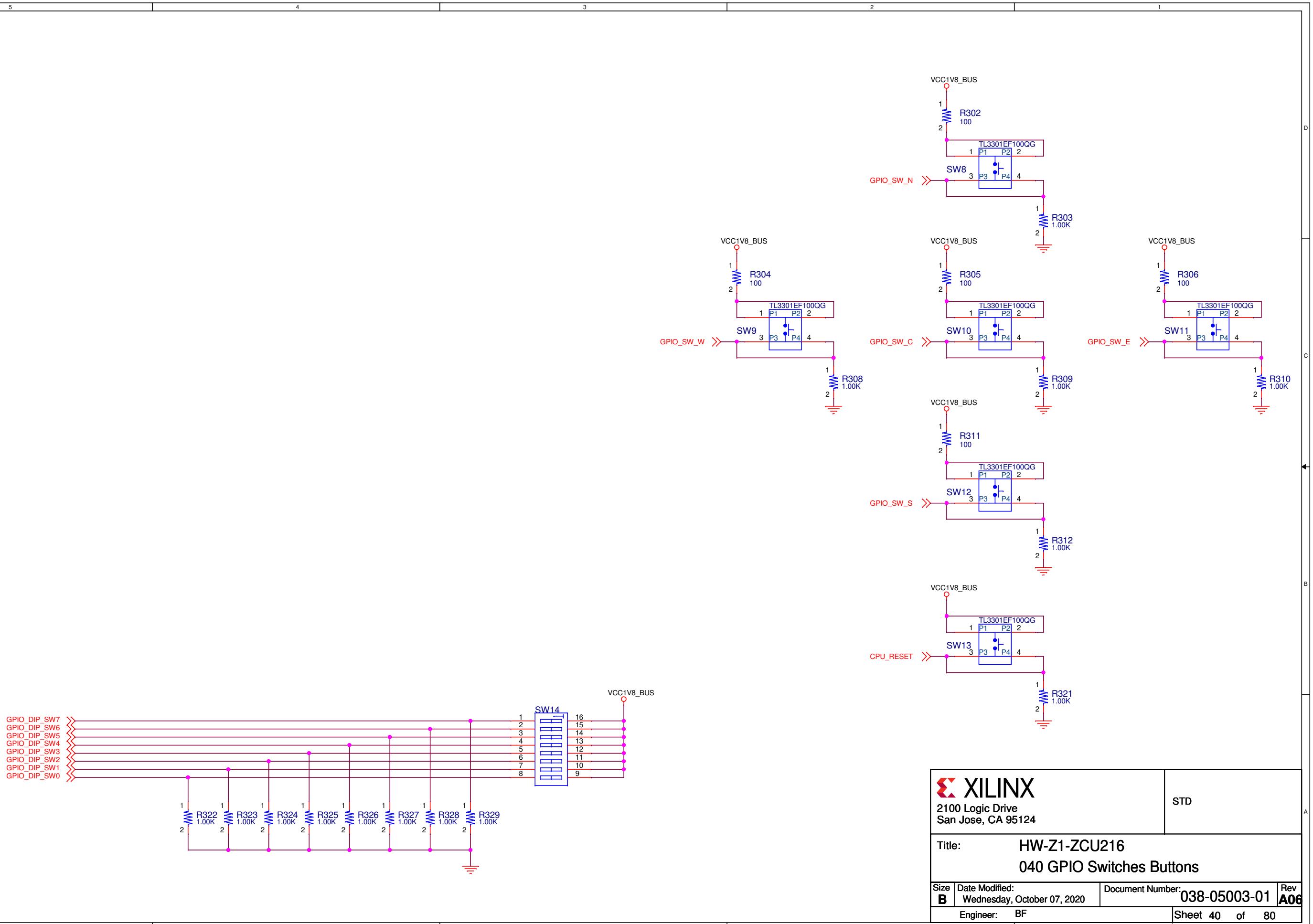
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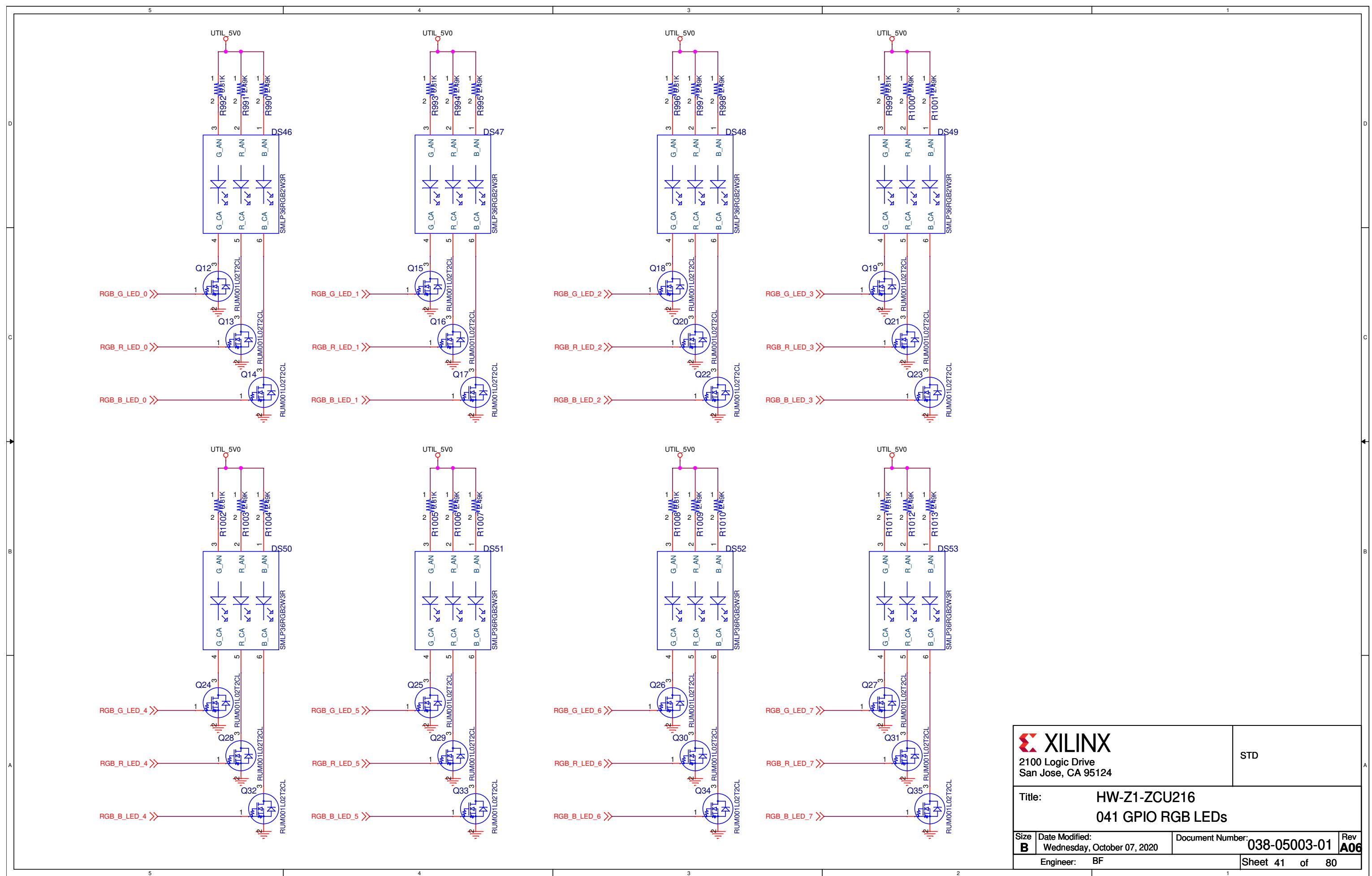
Engineer: BF Sheet 37 of 80

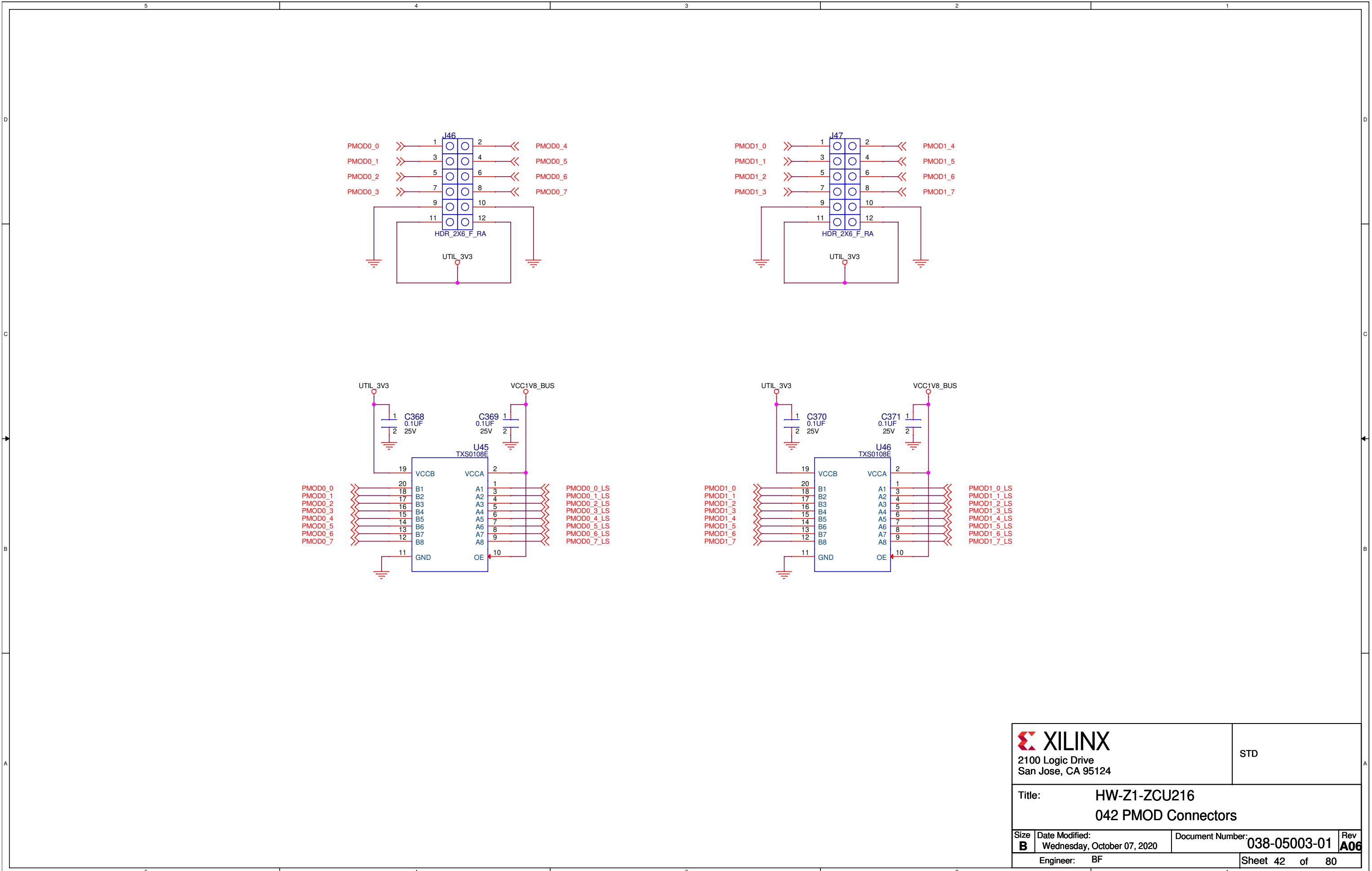




XILINX 2100 Logic Drive San Jose, CA 95124		STD
Title: HW-Z1-ZCU216 039 Fixed Clocks		
Size: B	Date Modified: Wednesday, October 07, 2020	Document Number: 038-05003-01 Rev A06
Engineer: BF	Sheet 39 of 80	



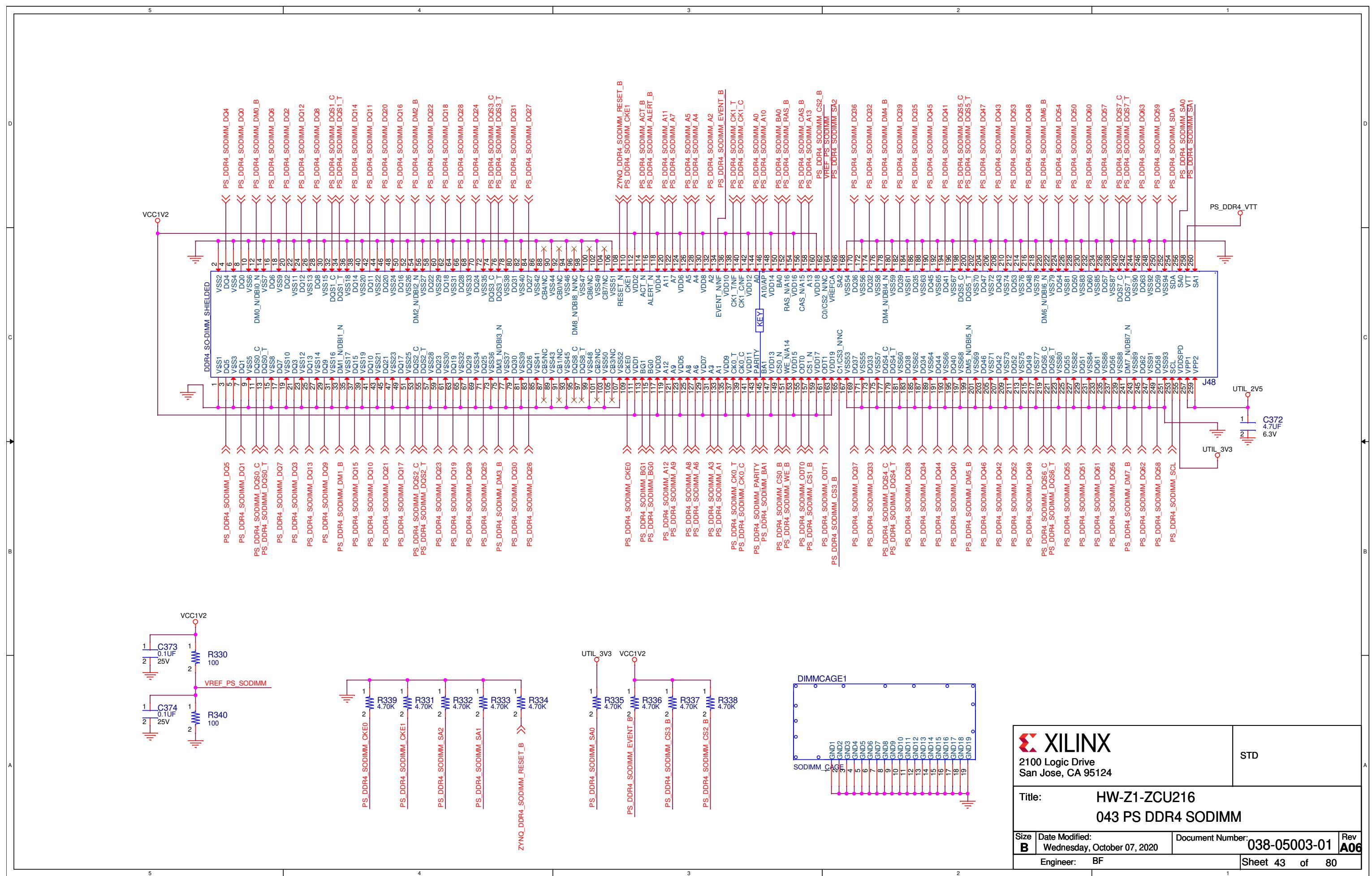




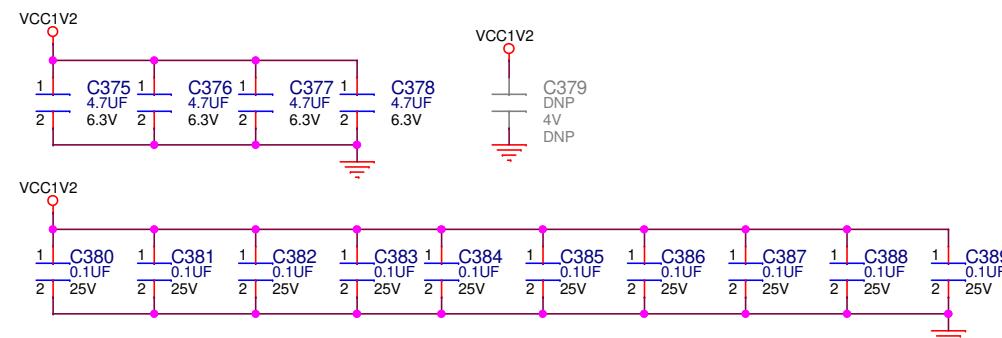
XILINX
2100 Logic Drive
San Jose, CA 95124

Title: HW-Z1-ZCU216
042 PMOD Connectors

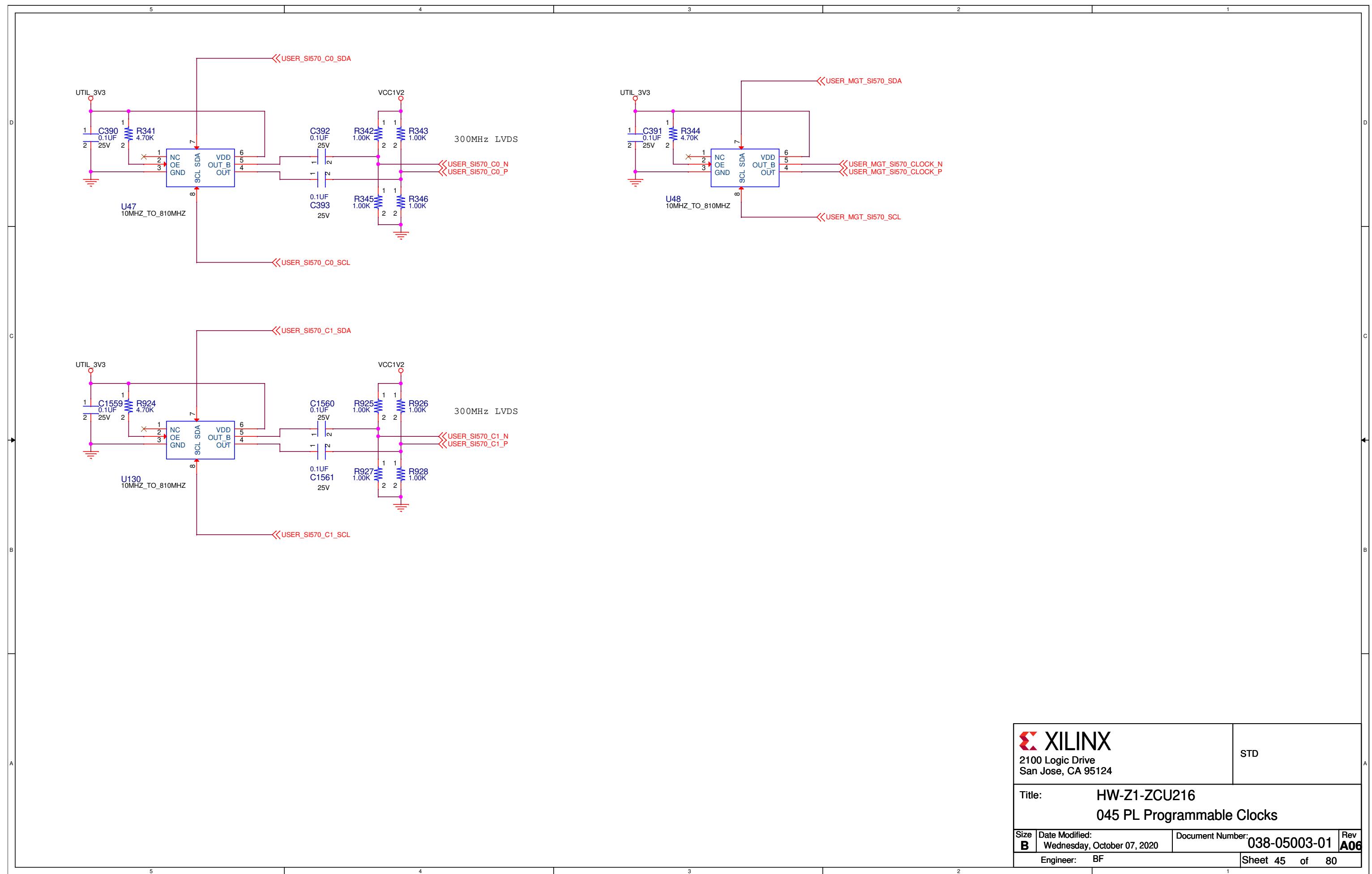
Size	Date Modified:	Document Number:
B	Wednesday, October 07, 2020	038-05003-01 Rev A06
Engineer:	BF	Sheet 42 of 80



PS SODIMM DECOUPLING



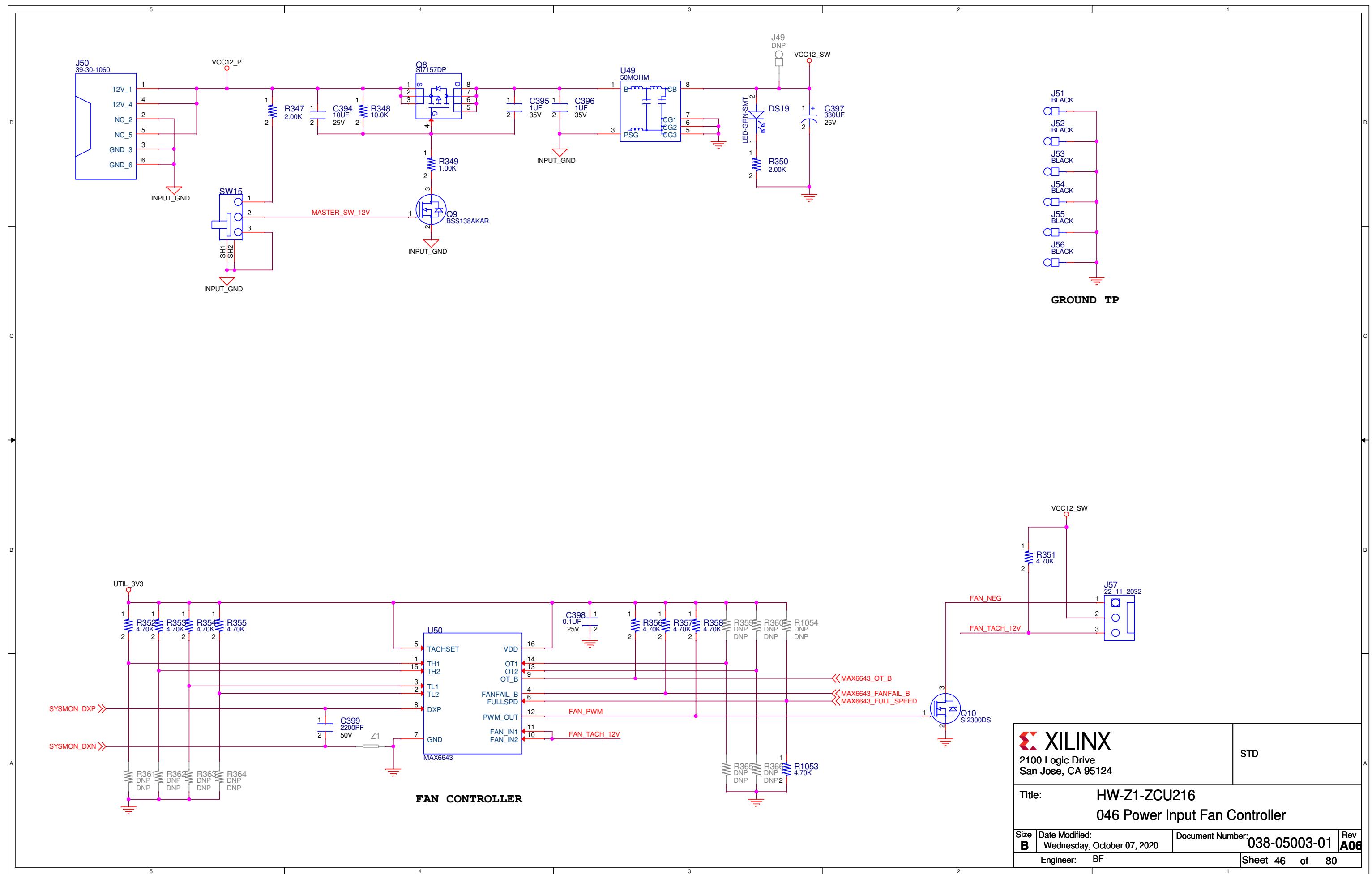
XILINX 2100 Logic Drive San Jose, CA 95124		STD
Title: HW-Z1-ZCU216 044 SODIMM Decoupling		
Size	Date Modified: B Wednesday, October 07, 2020	Document Number: 038-05003-01 A06
Engineer:	BF	Sheet 44 of 80



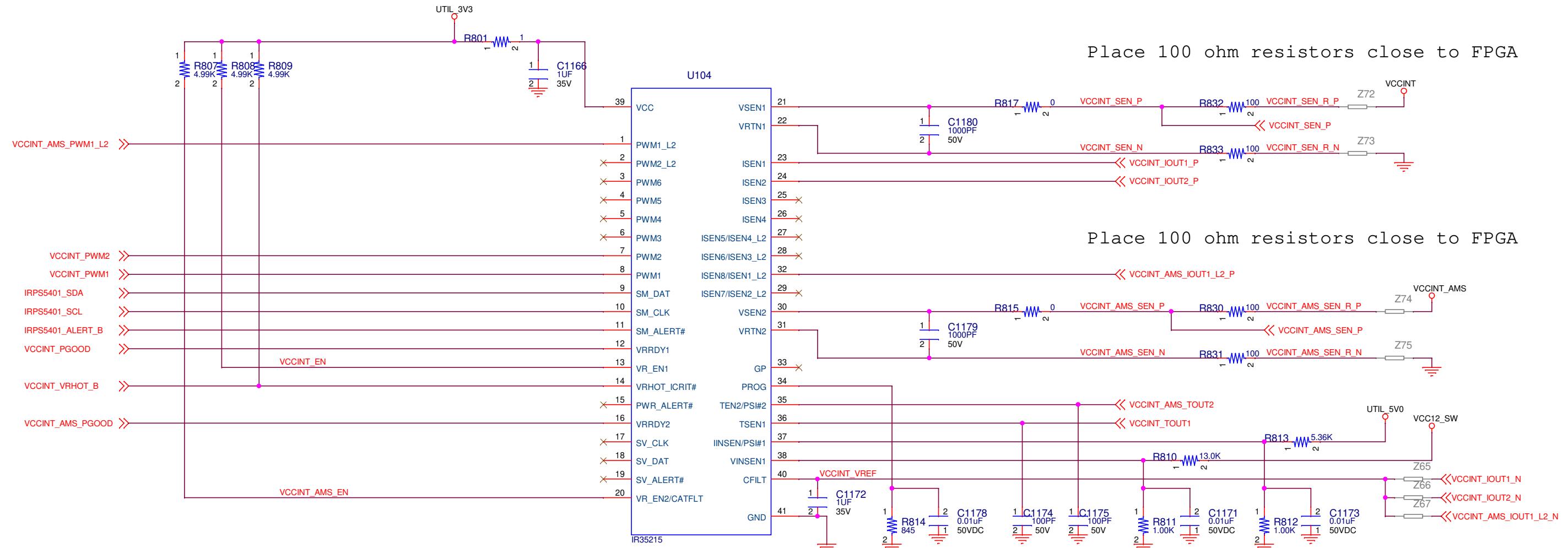
XILINX
2100 Logic Drive
San Jose, CA 95124

Title: **HW-Z1-ZCU216**
045 PL Programmable Clocks

Size	Date Modified:	Document Number:	Rev
B	Wednesday, October 07, 2020	038-05003-01	A06
Engineer: BF	Sheet 45 of 80		



REPLACE IC WITH CORRECT FIRMWARE P/N



ADDR: 0

7-BIT I2C ADDR: 0x10

7-BIT PMBUS ADDR: 0x40

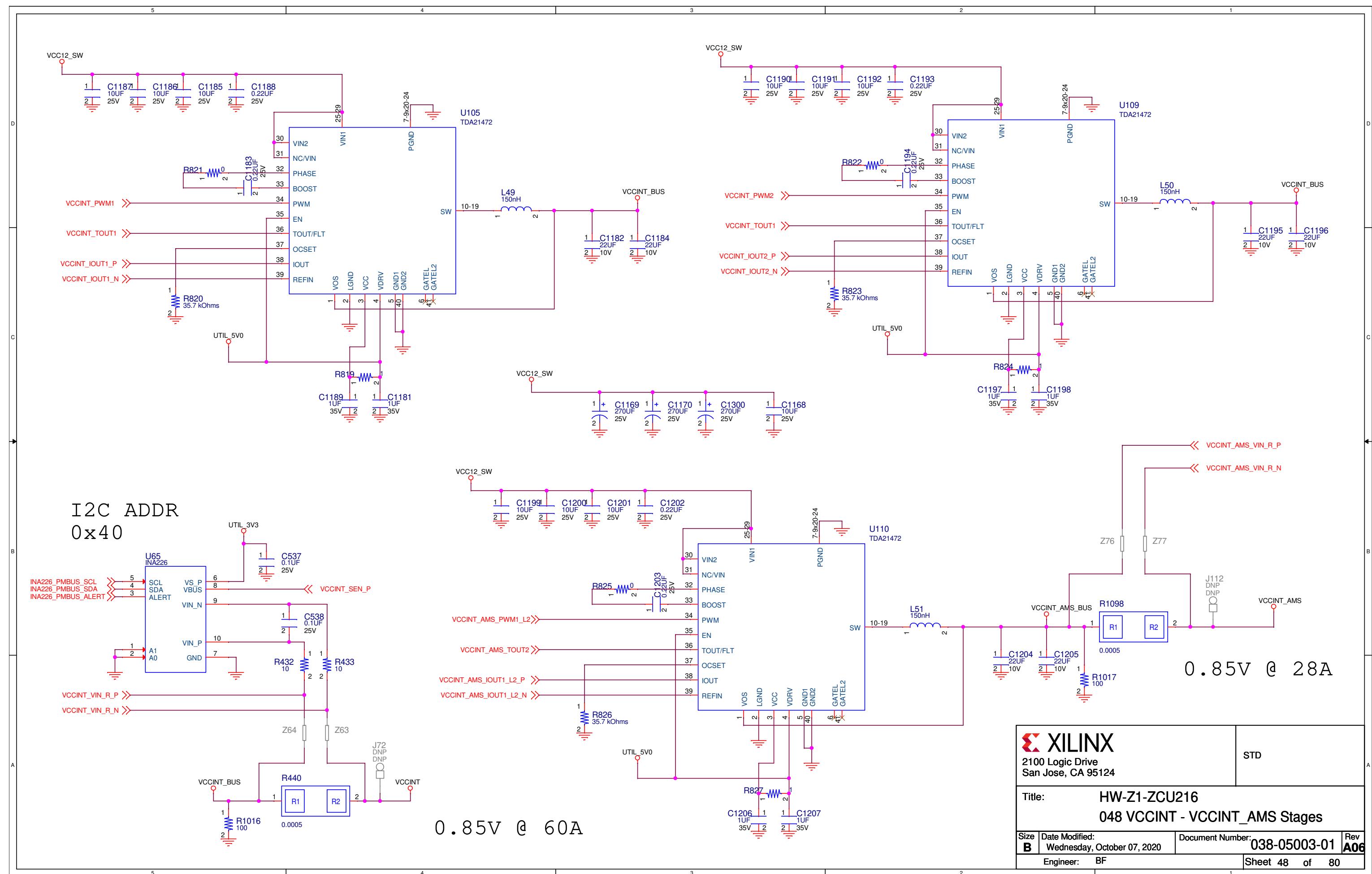
XILINX

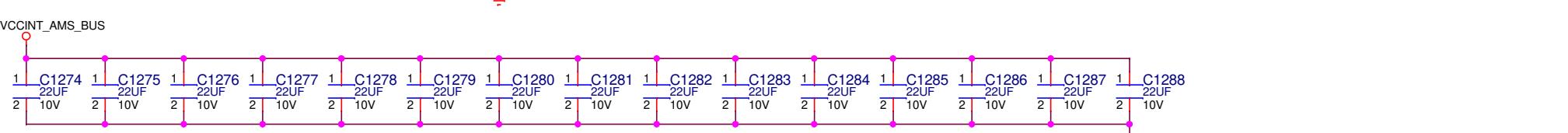
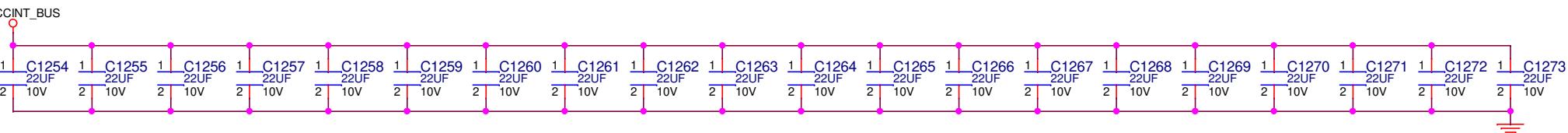
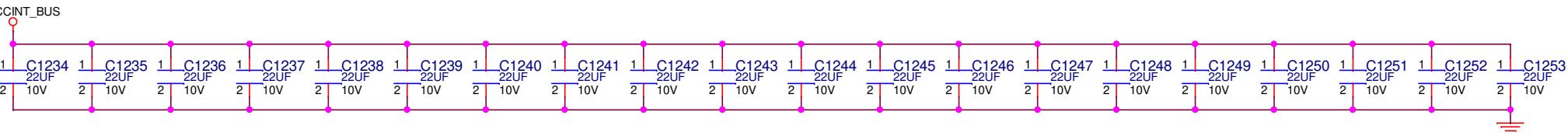
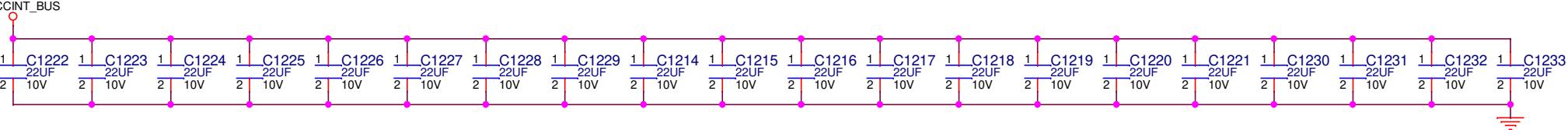
2100 Logic Drive
San Jose, CA 95124

STD

Title: HW-Z1-ZCU216
047 VCCINT - VCCINT_AMS PMIC1

Size: B	Date Modified: Wednesday, October 07, 2020	Document Number: 038-05003-01 Rev A06
Engineer: BF	Sheet 47 of 80	



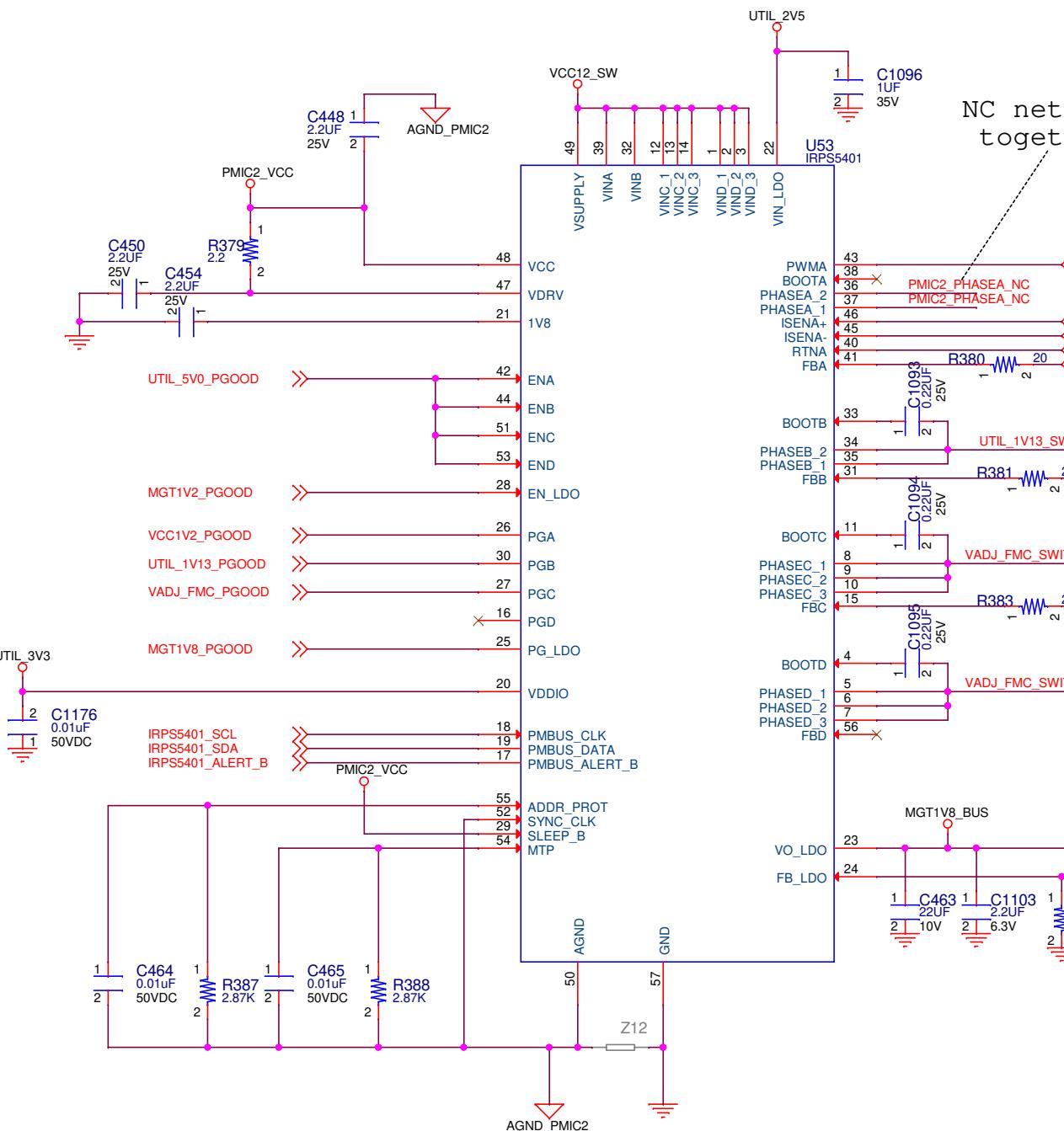
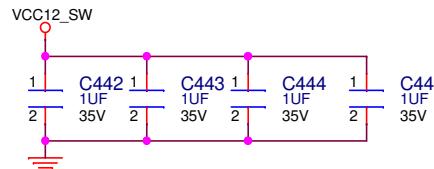
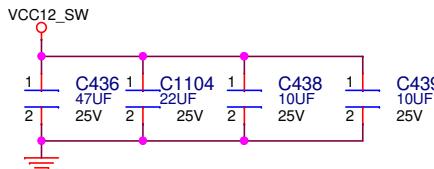


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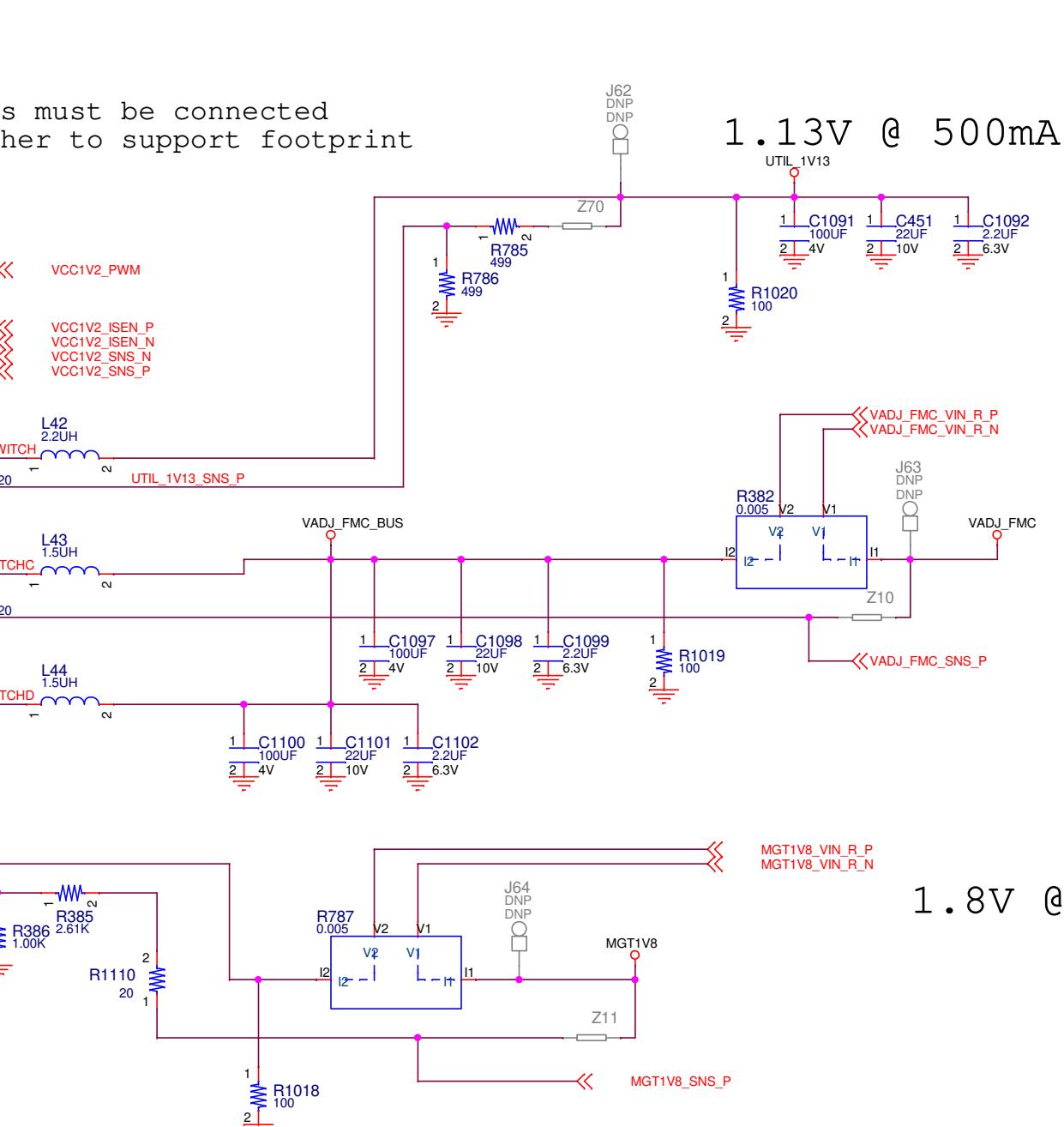
Title: HW-Z1-ZCU216
049 VCCINT - VCCINT_AMS Decap

Size	Date Modified:	Document Number:
B	Wednesday, October 07, 2020	038-05003-01 Rev A06
Engineer: BF		Sheet 49 of 80

REPLACE IC WITH CORRECT FIRMWARE P/N



NC nets must be connected together to support footprint



MTP : +4

7-BIT I2C ADDR: 0x14

7-BIT PMBUS ADDR: 0x44

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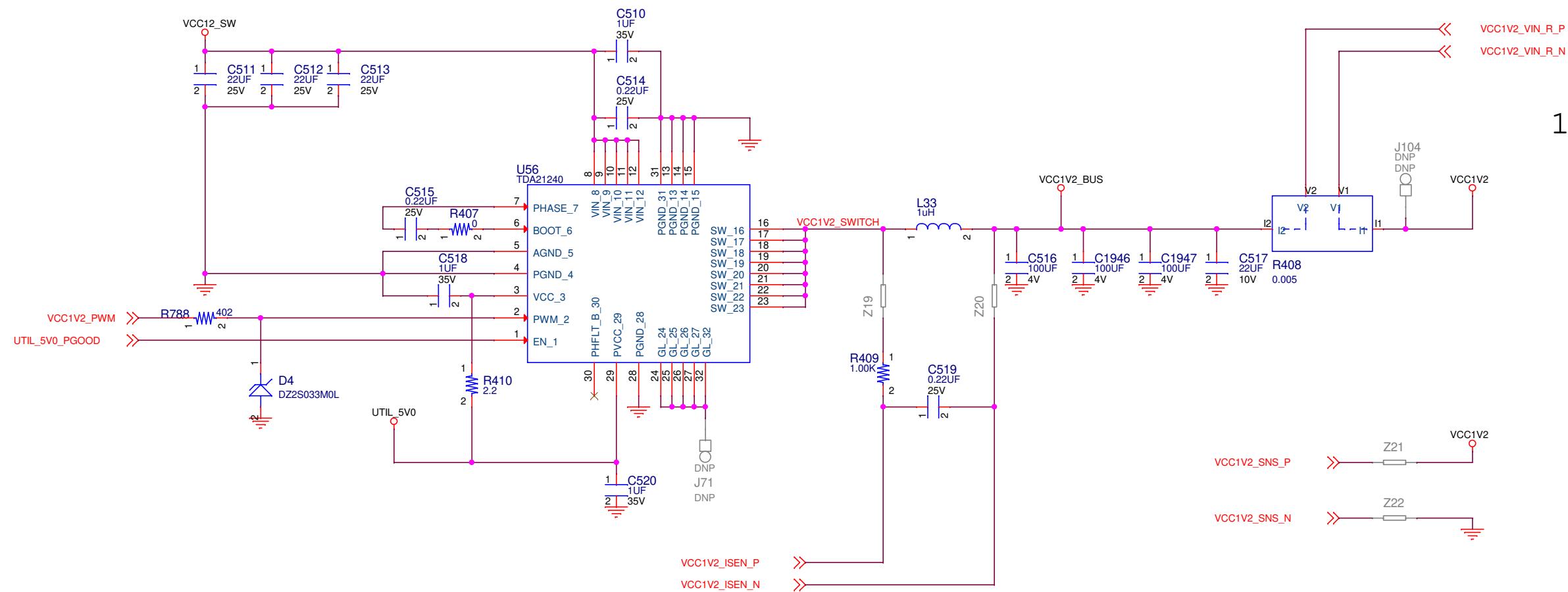
STD

Title: HW-Z1-ZCU216
050 PMIC 2

Size Date Modified: Document Number: Rev

B Wednesday, October 07, 2020 038-05003-01 A06

Engineer: BF Sheet 50 of 80

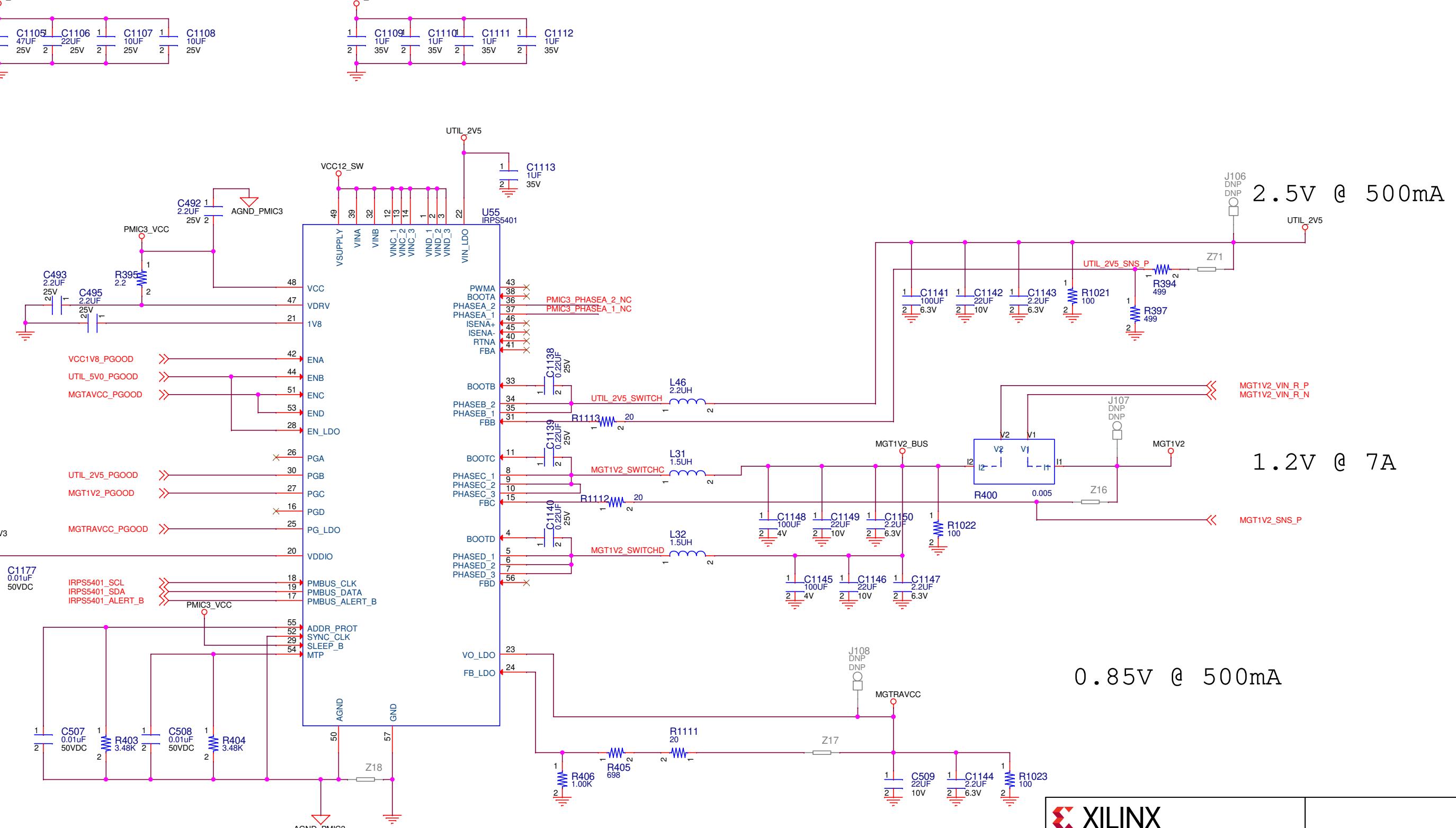


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San Jose, CA 95124

Title: HW-Z1-ZCU216
051 PMIC 2 Power Stage

Size	Date Modified:	Document Number:
B	Wednesday, October 07, 2020	038-05003-01 Rev A06
Engineer: BF		Sheet 51 of 80

REPLACE IC WITH CORRECT FIRMWARE P/N



MTP : +5

7-BIT I2C ADDR: 0x15

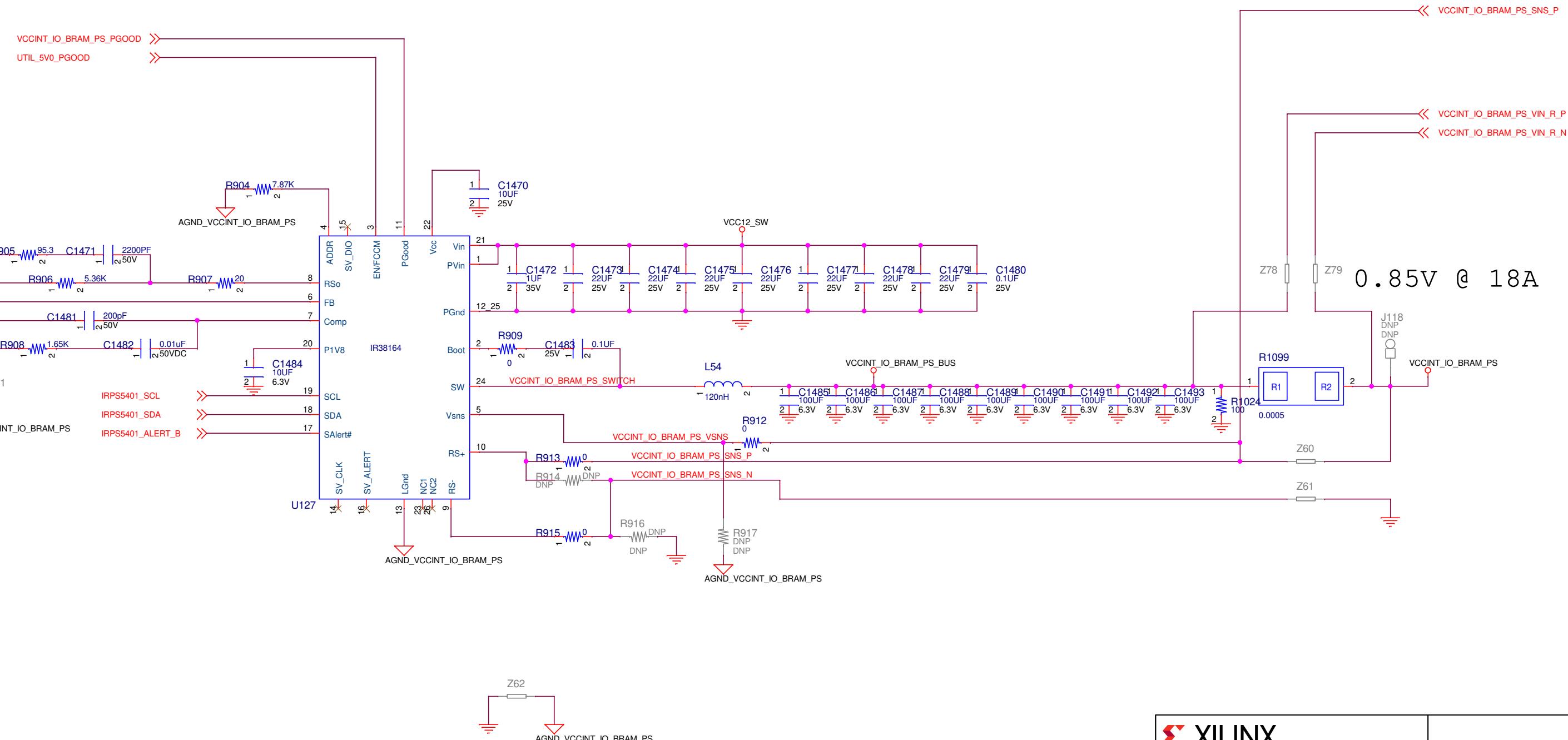
7-BIT PMBUS ADDR: 0x45

The Xilinx logo consists of a stylized red 'X' followed by the word 'XILINX' in a bold, black, sans-serif font. Below the logo, the company's address is listed: '2100 Logic Drive' on one line and 'San Jose, CA 95124' on the line below.

Title: HW-Z1-ZCU216
052 PMIC 3

Size B	Date Modified: Wednesday, October 07, 2020	Document Number: 038-05003-01	Rev A06
Engineer: BF		Sheet 52 of 80	

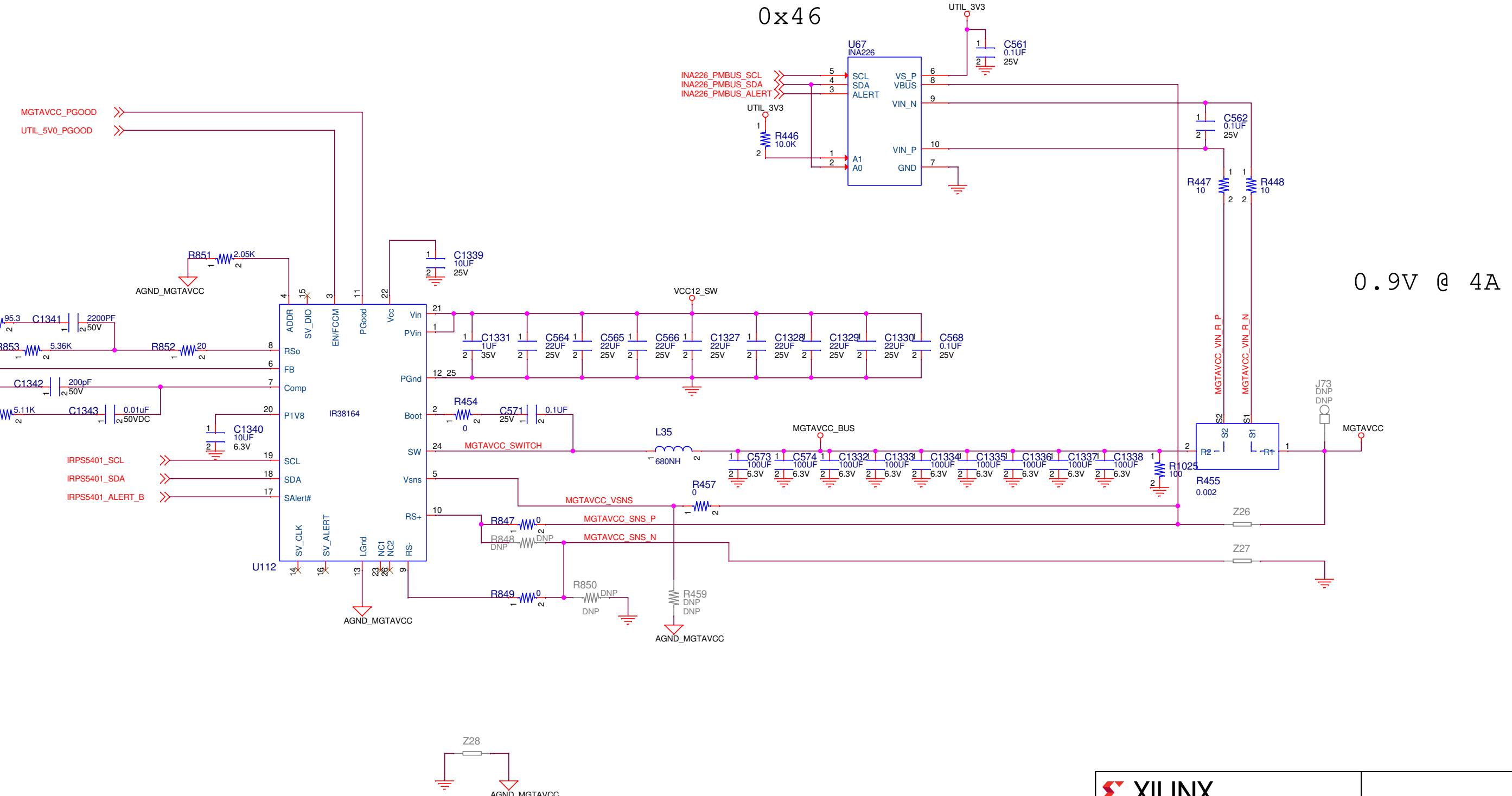
REPLACE IC WITH CORRECT FIRMWARE P/N



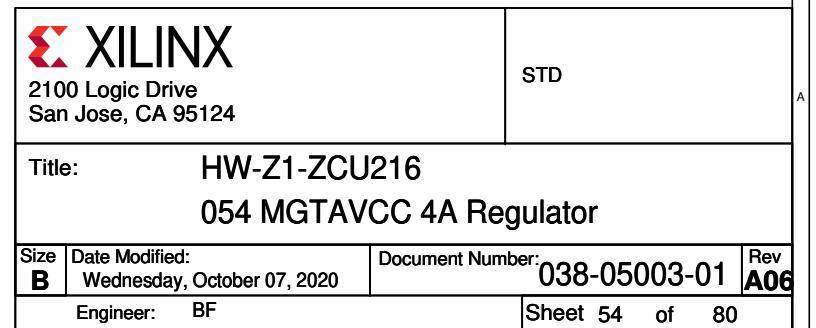
XILINX 2100 Logic Drive San Jose, CA 95124		STD
Title: HW-Z1-ZCU216 053 VCCINT_IO_BRAM_PS 18A Reg		
Size: B	Date Modified: Wednesday, October 07, 2020	Document Number: 038-05003-01 Rev A06
Engineer: BF	Sheet 53 of 80	

REPLACE IC WITH CORRECT FIRMWARE P/N

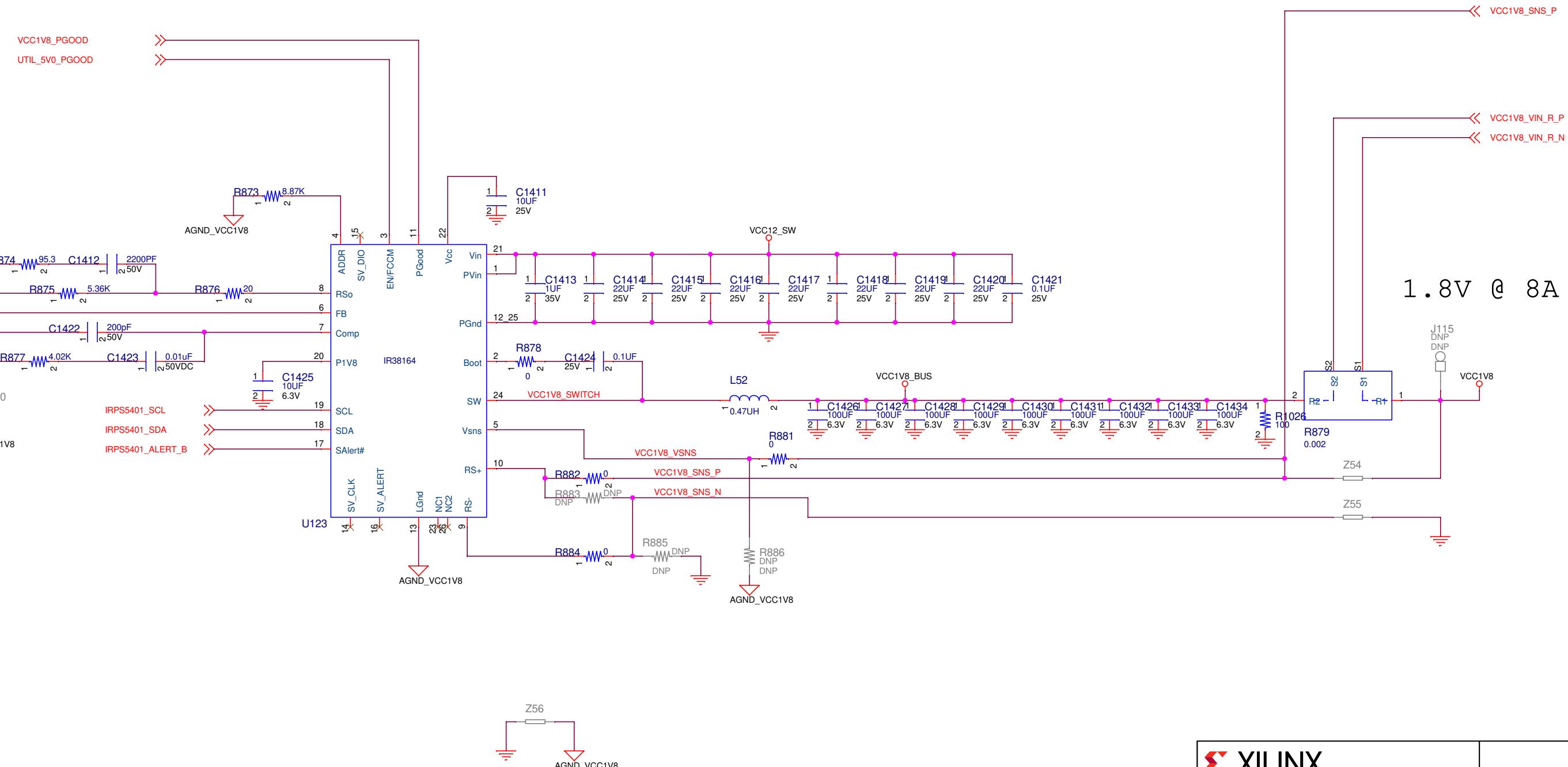
I2C ADDRESSES
0x46



OFFSET: +3
7-BIT I2C ADDR: 0x13
7-BIT PMBUS ADDR: 0x43

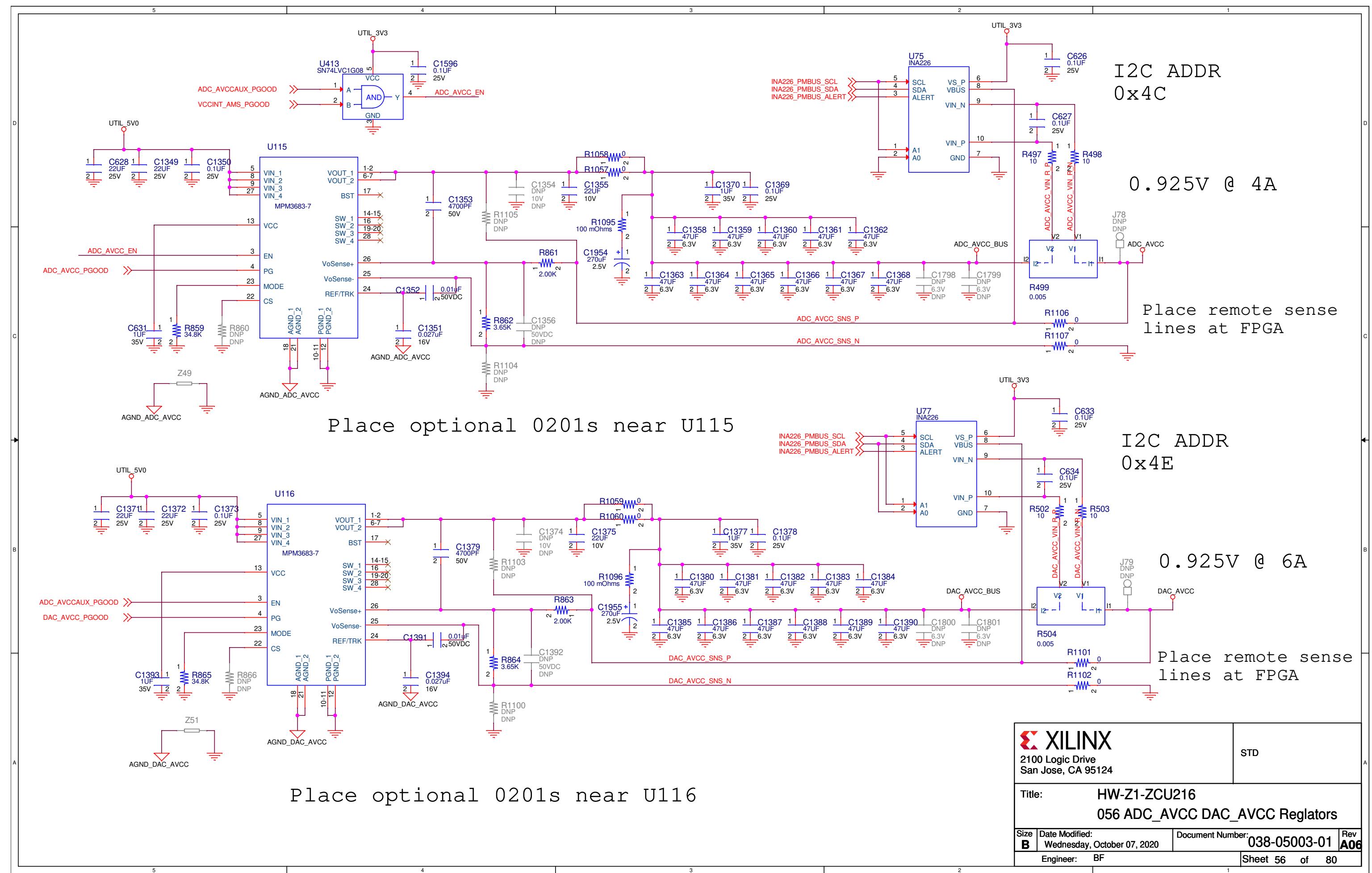


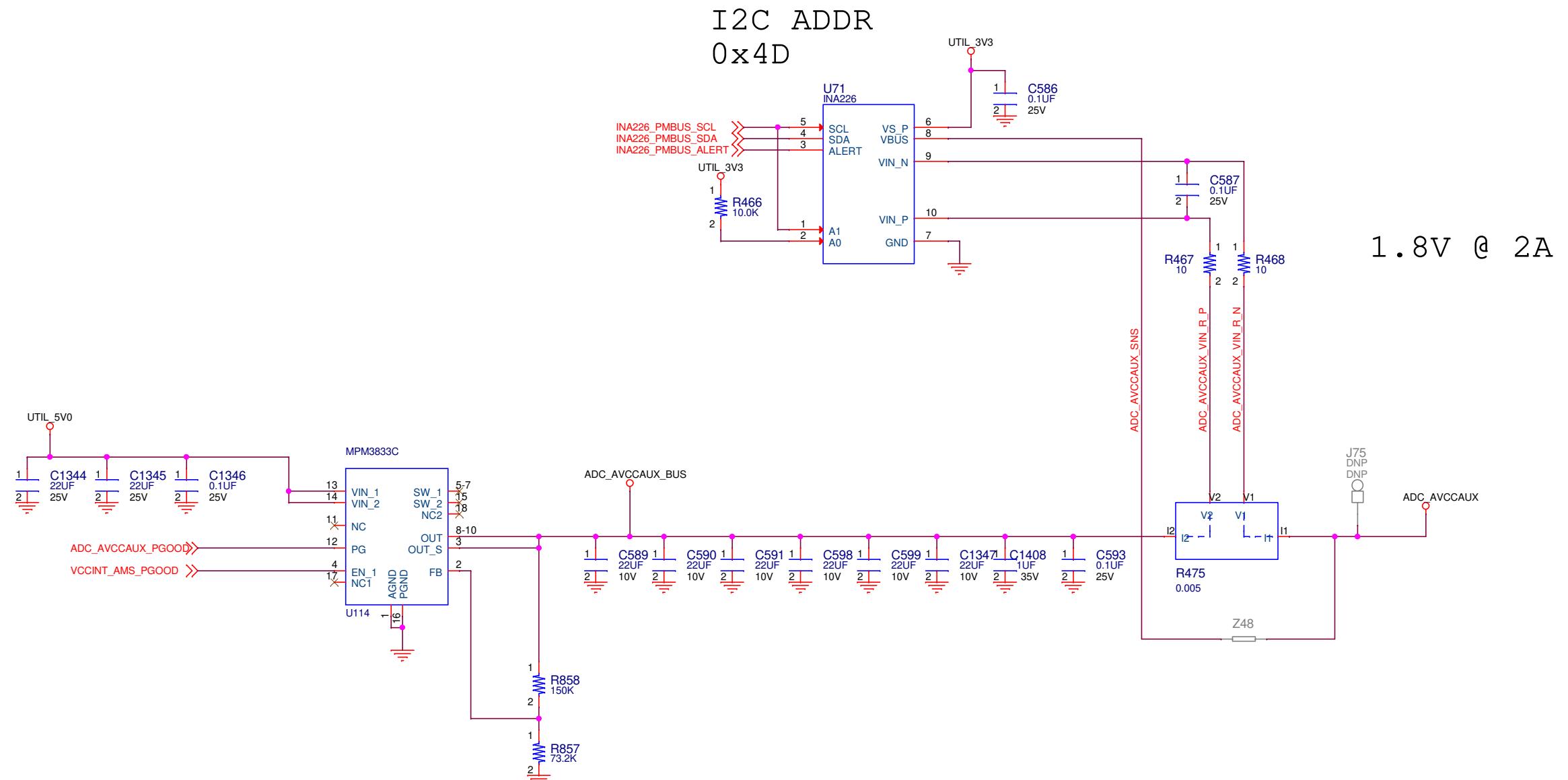
REPLACE IC WITH CORRECT FIRMWARE P/N



OFFSET: +12
 7-BIT I2C ADDR: 0x1C
 7-BIT PMBUS ADDR: 0x4C

XILINX		STD
2100 Logic Drive San Jose, CA 95124		
Title: HW-Z1-ZCU216 055 VCC1V8 8A Reg		
Size: B	Date Modified: Wednesday, October 07, 2020	Document Number: 038-05003-01 Rev A06
Engineer: BF	Sheet 55 of 80	





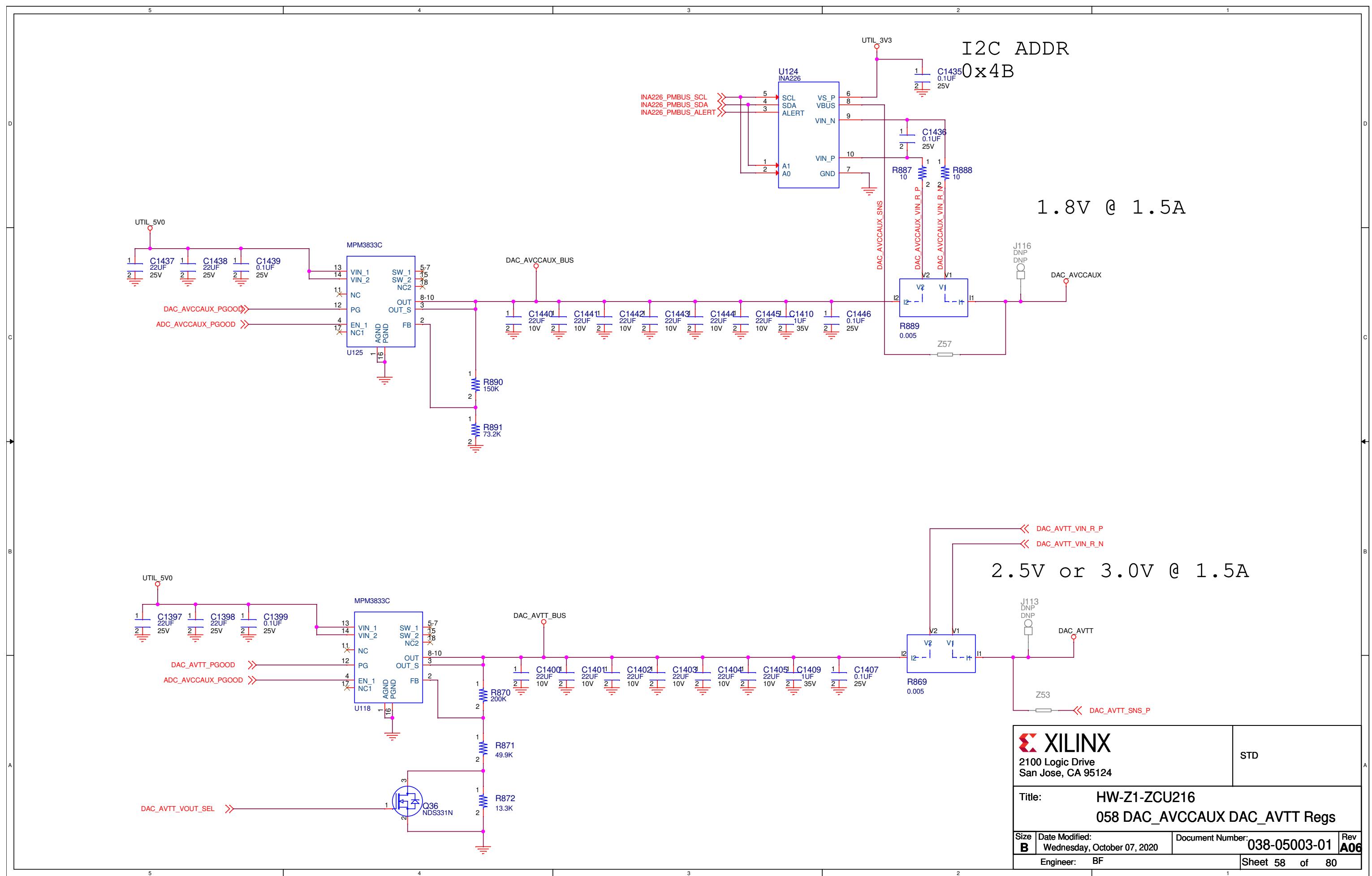
XILINX

2100 Logic Drive
San Jose, CA 95124

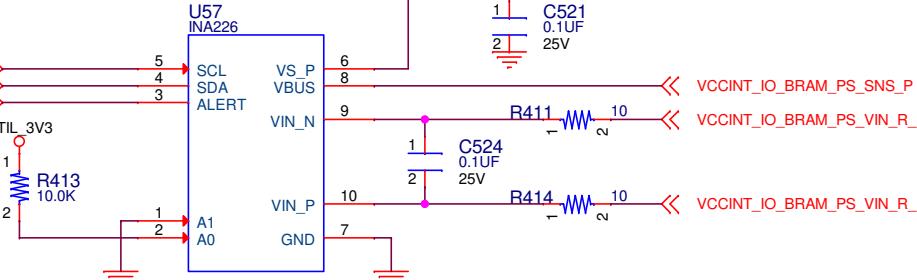
STD

Title: HW-Z1-ZCU216
057 ADC_AVCCAUX 2A Regulator

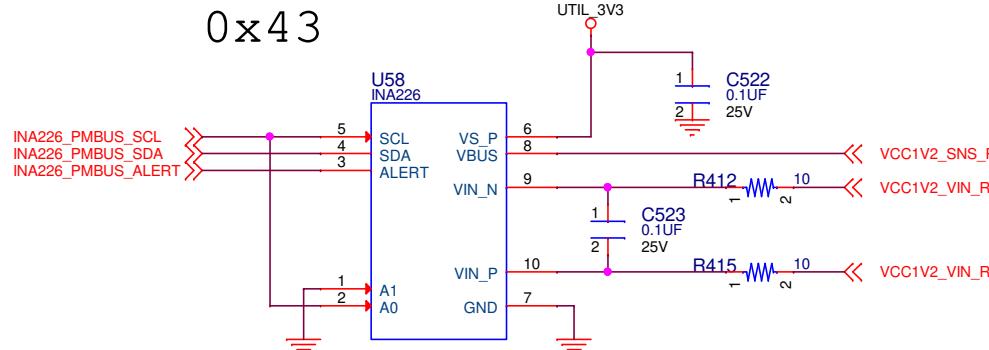
Size	Date Modified:	Document Number:	Rev
B	Wednesday, October 07, 2020	038-05003-01	A06
Engineer:	BF	Sheet 57 of 80	



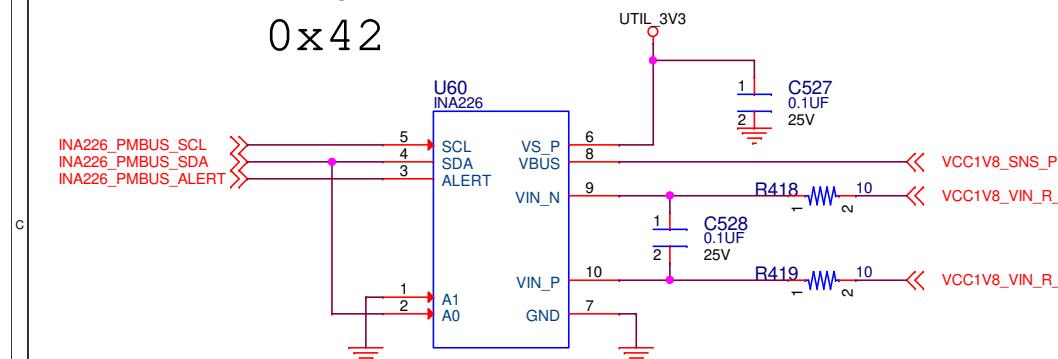
I₂C ADDR
0x41



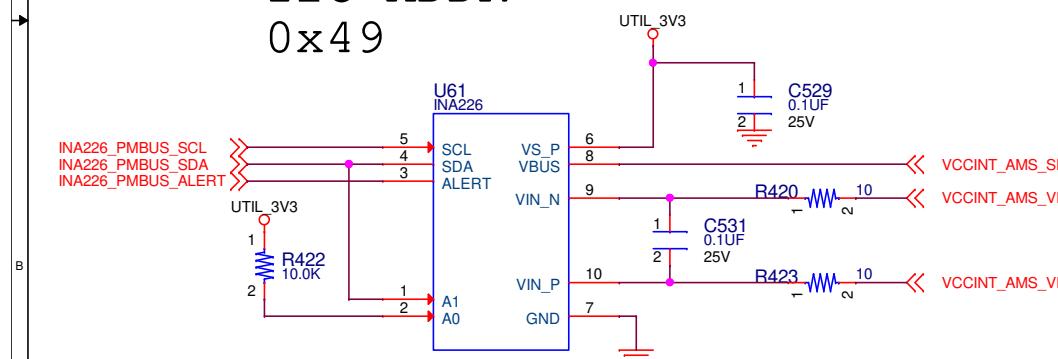
I₂C ADDR
0x43



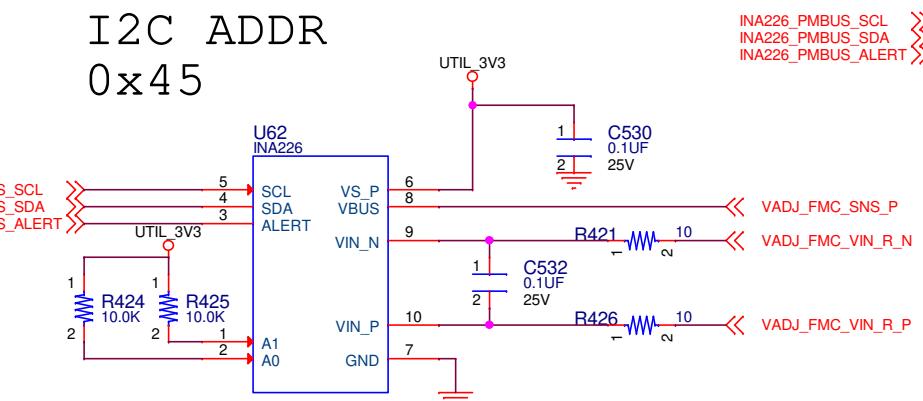
I₂C ADDR
0x42



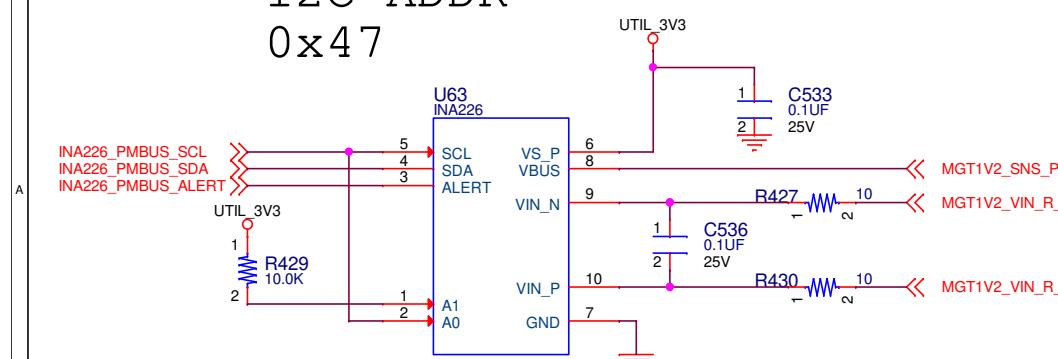
I₂C ADDR
0x49



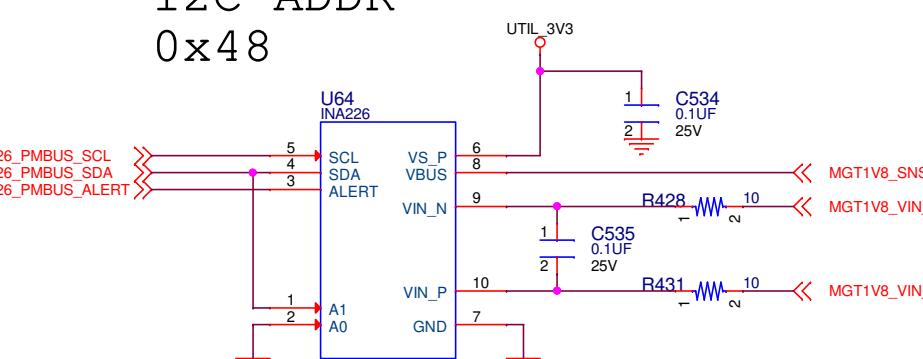
I₂C ADDR
0x45



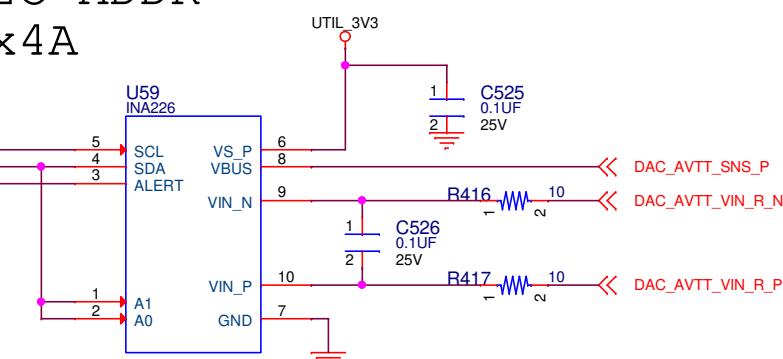
I₂C ADDR
0x47



I₂C ADDR
0x48



I₂C ADDR
0x4A

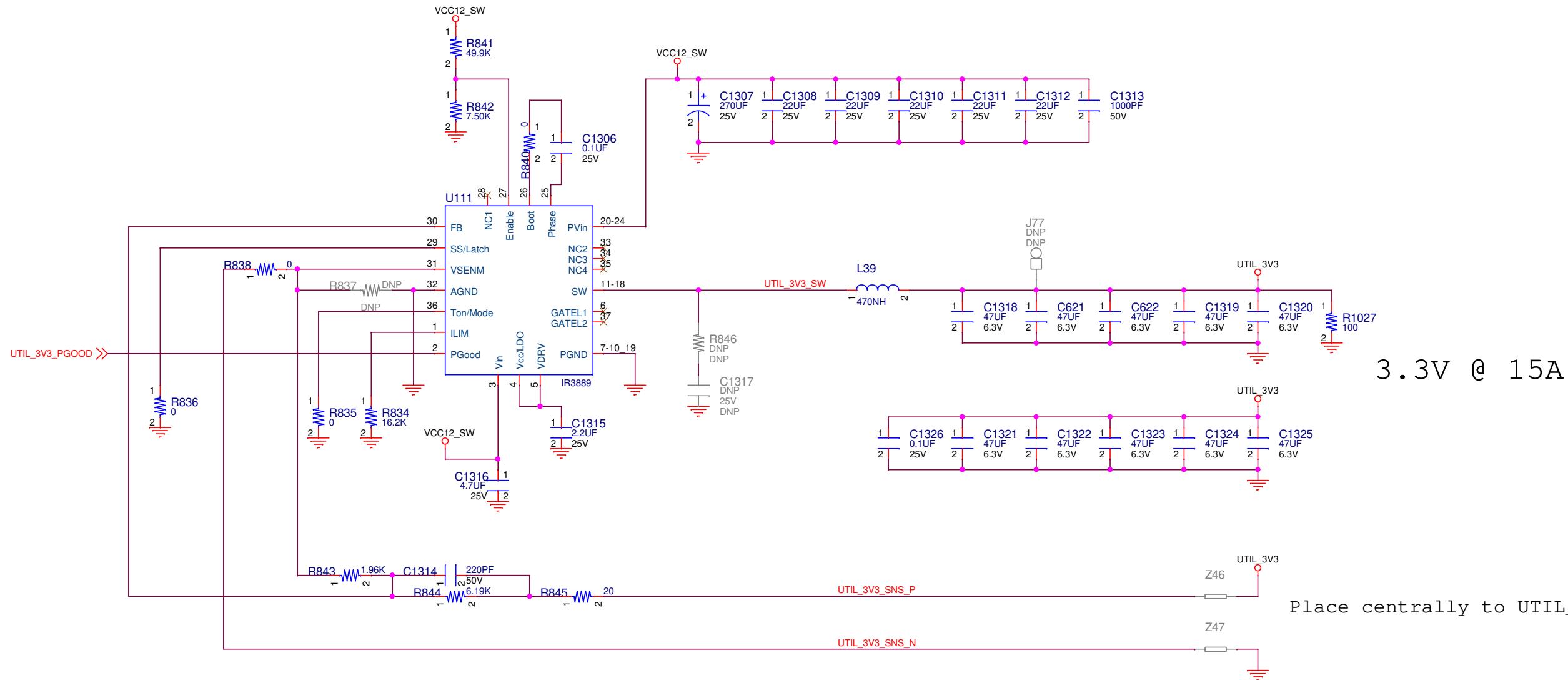


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Title: HW-Z1-ZCU216
059 PMIC Current Sense

Size Date Modified: B Wednesday, October 07, 2020 Document Number: 038-05003-01 Rev A06

Engineer: BF Sheet 59 of 80



3.3V @ 15A

Place centrally to UTIL_3V3 Load

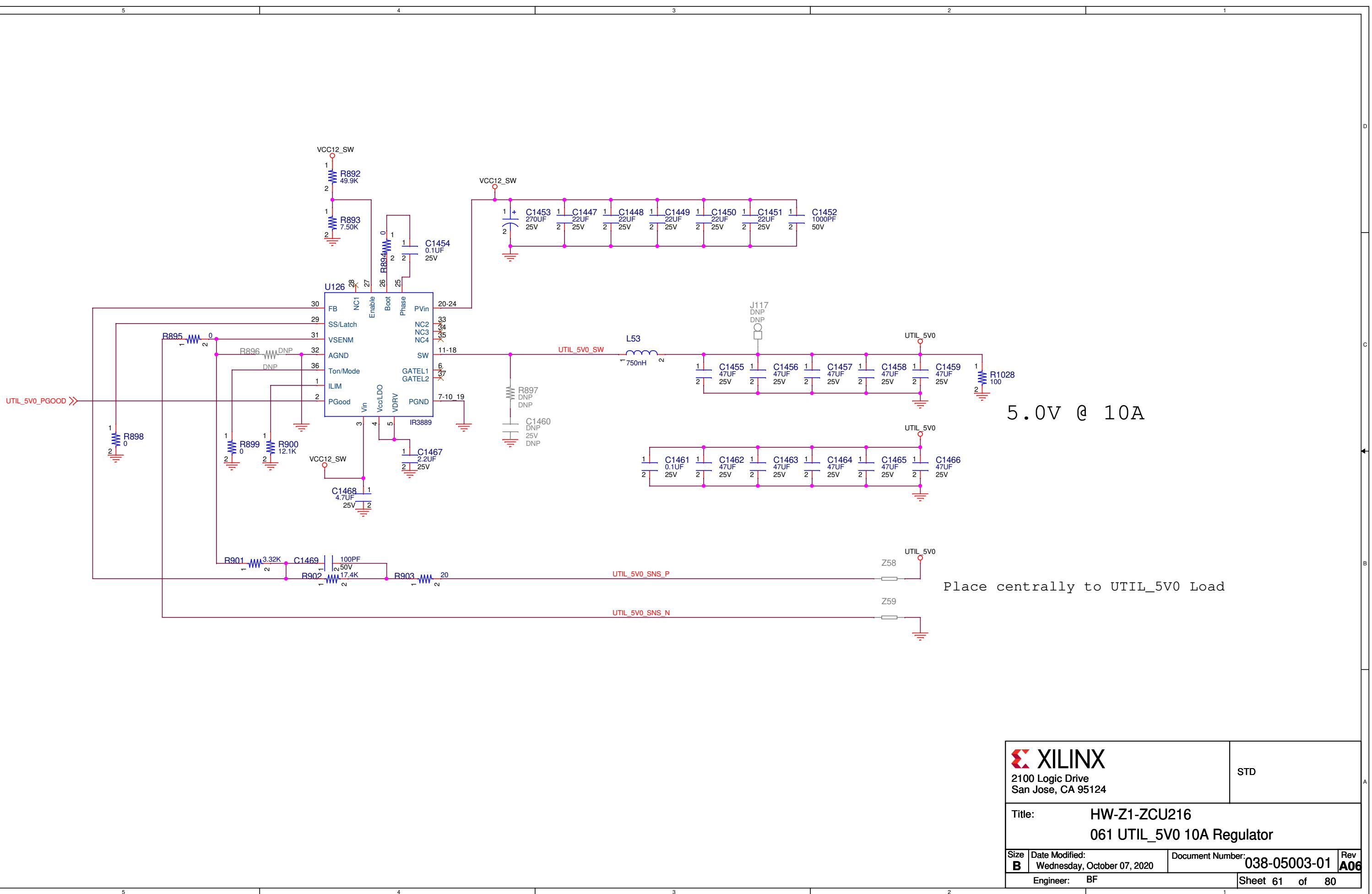


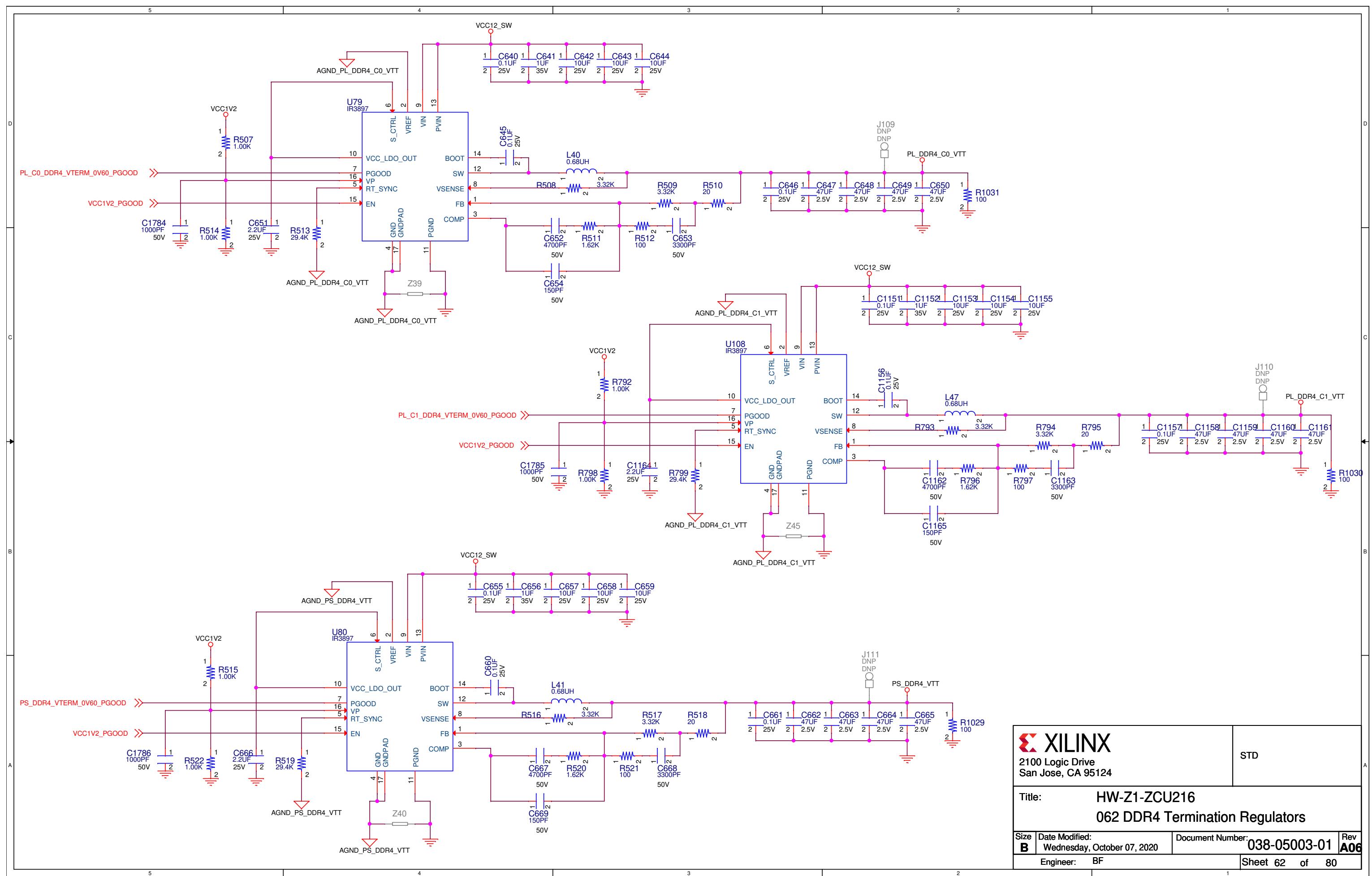
2100 Logic Drive
San Jose, CA 95124

Title: HW-Z1-ZCU216

060 UTIL_3V3 15A Regulator

Size	Date Modified: Wednesday, October 07, 2020	Document Number: 038-05003-01	Rev
B			A06
Engineer: BF		Sheet 60	of 80

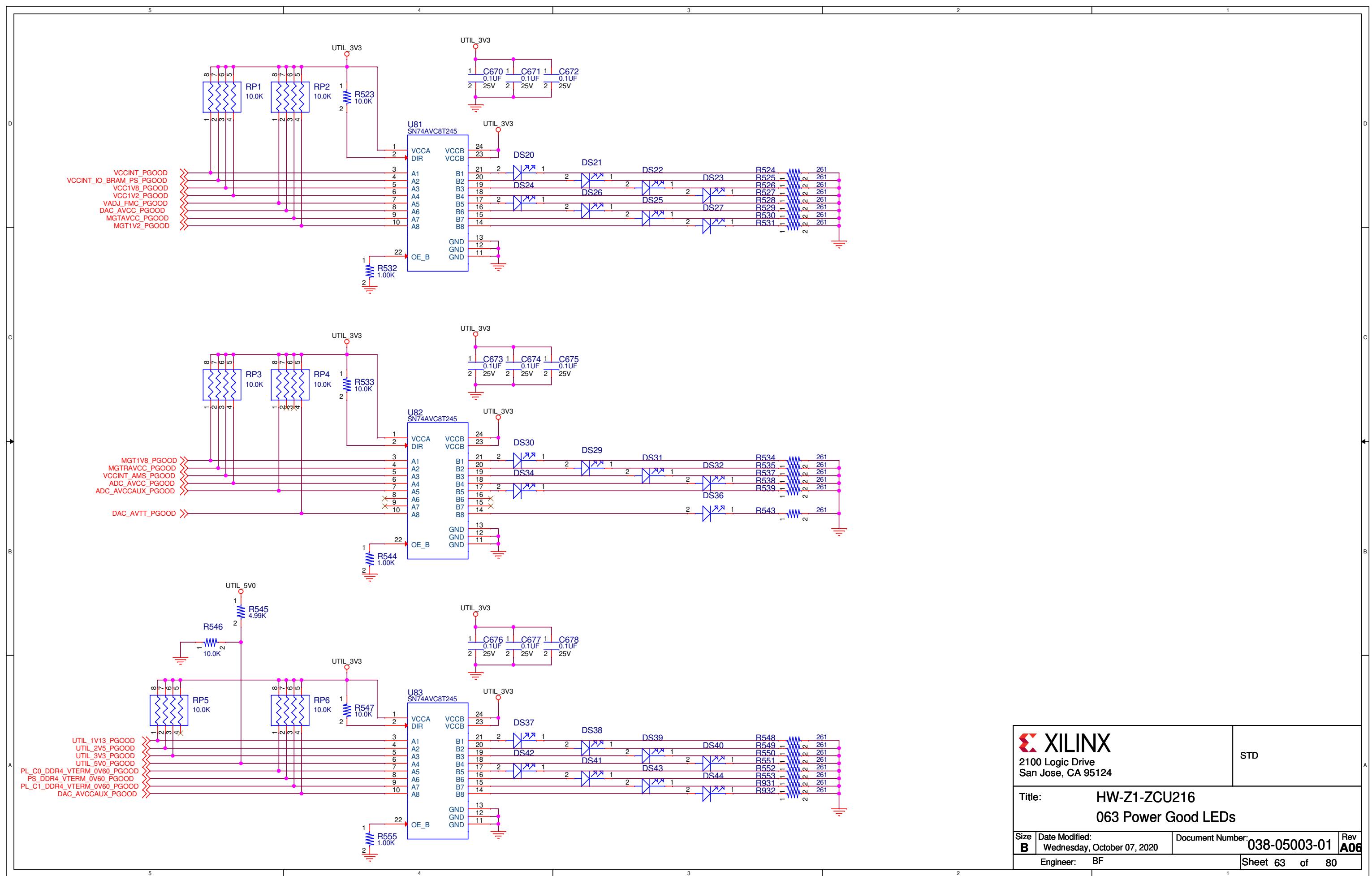




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2100 Logic Drive
San Jose, CA 95124

Title: HW-Z1-ZCU216
062 DDR4 Termination Regulators

Size: B	Date Modified: Wednesday, October 07, 2020	Document Number: 038-05003-01	Rev: A06
Engineer: BF	Sheet 62 of 80		



XILINX

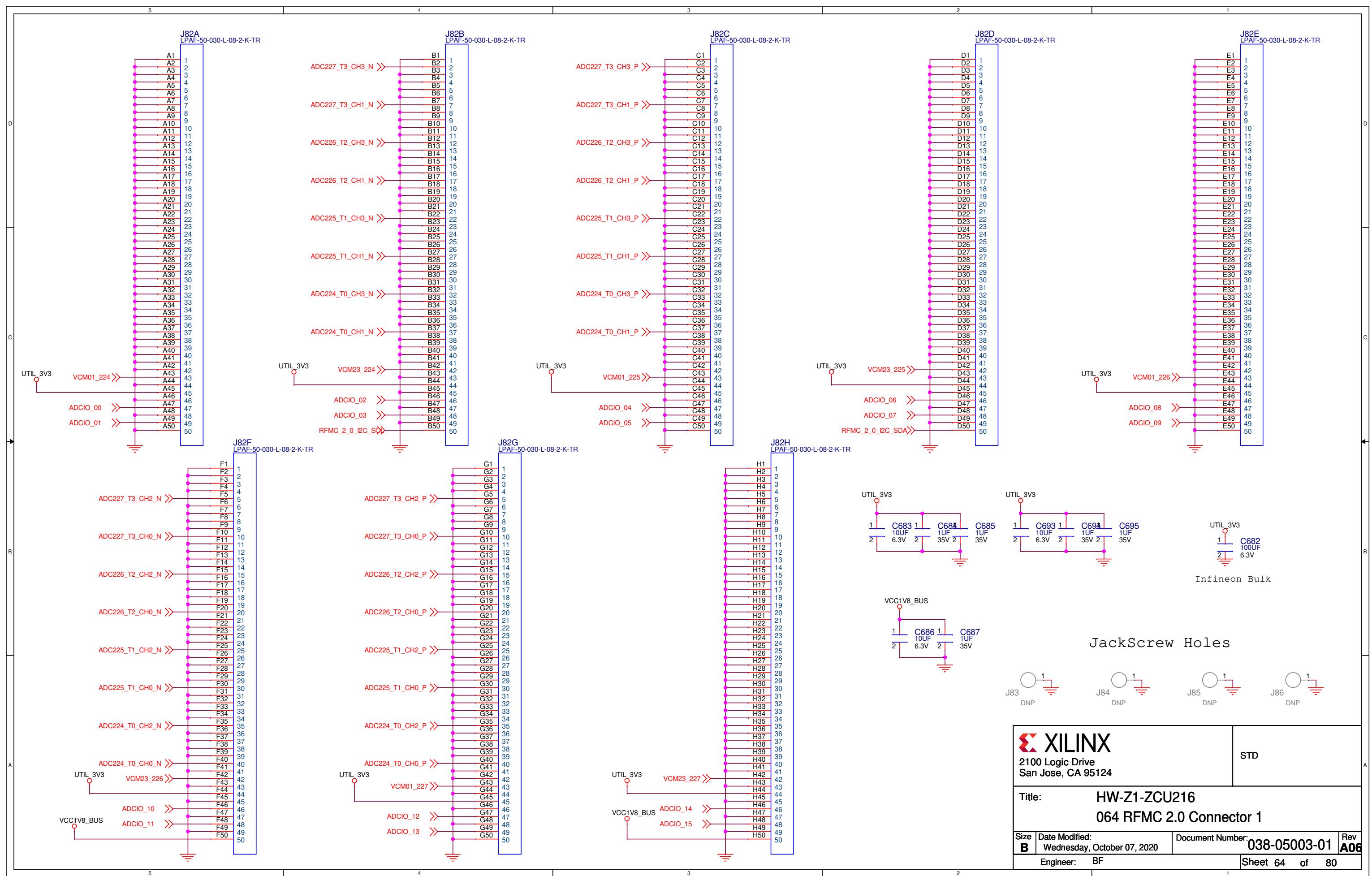
2100 Logic Drive
San Jose, CA 95124

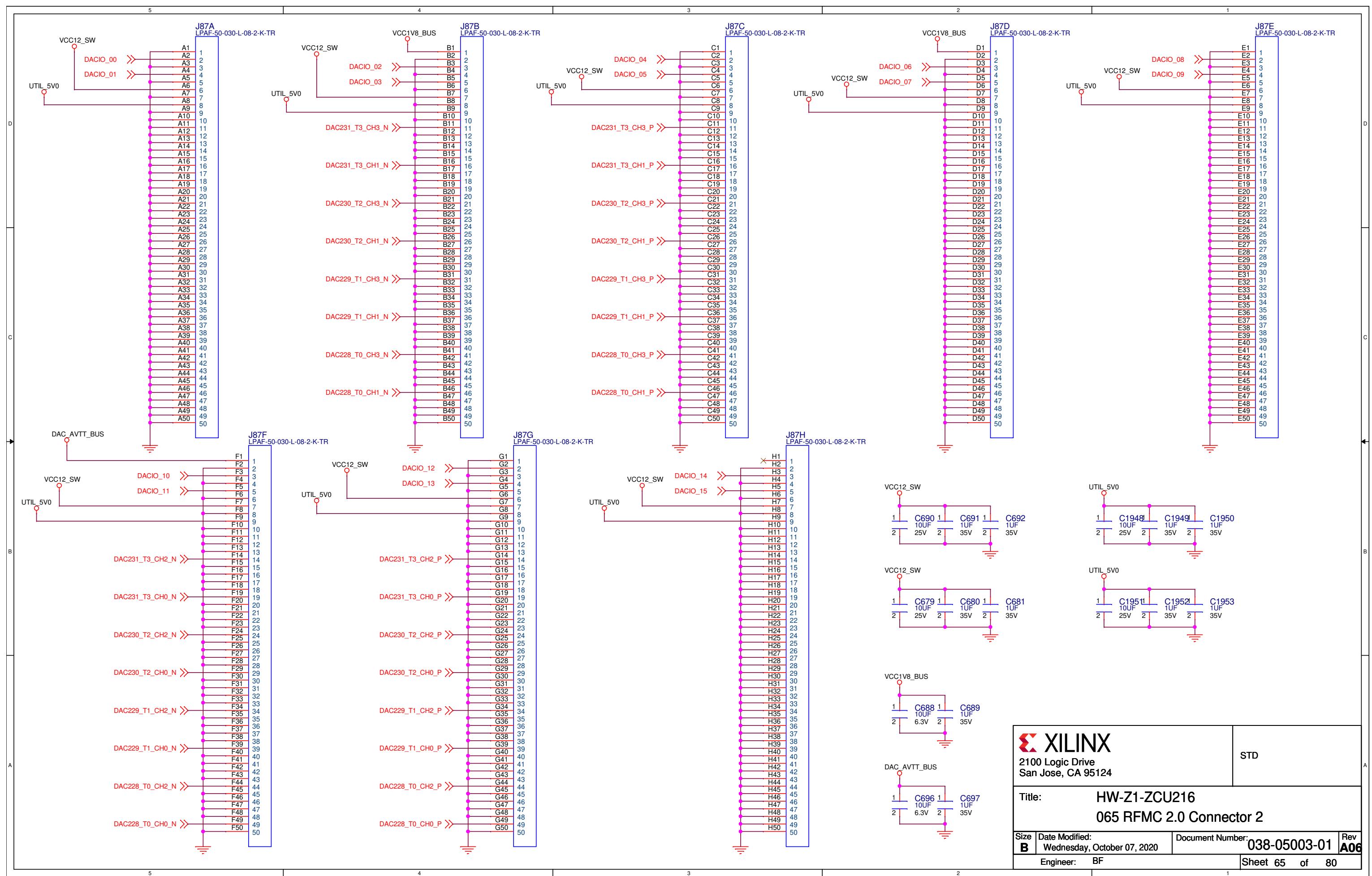
STD

Title: **HW-Z1-ZCU216**
063 Power Good LEDs

Size Date Modified: Document Number: **038-05003-01** Rev **A06**
B Wednesday, October 07, 2020

Engineer: BF Sheet 63 of 80





XILINX

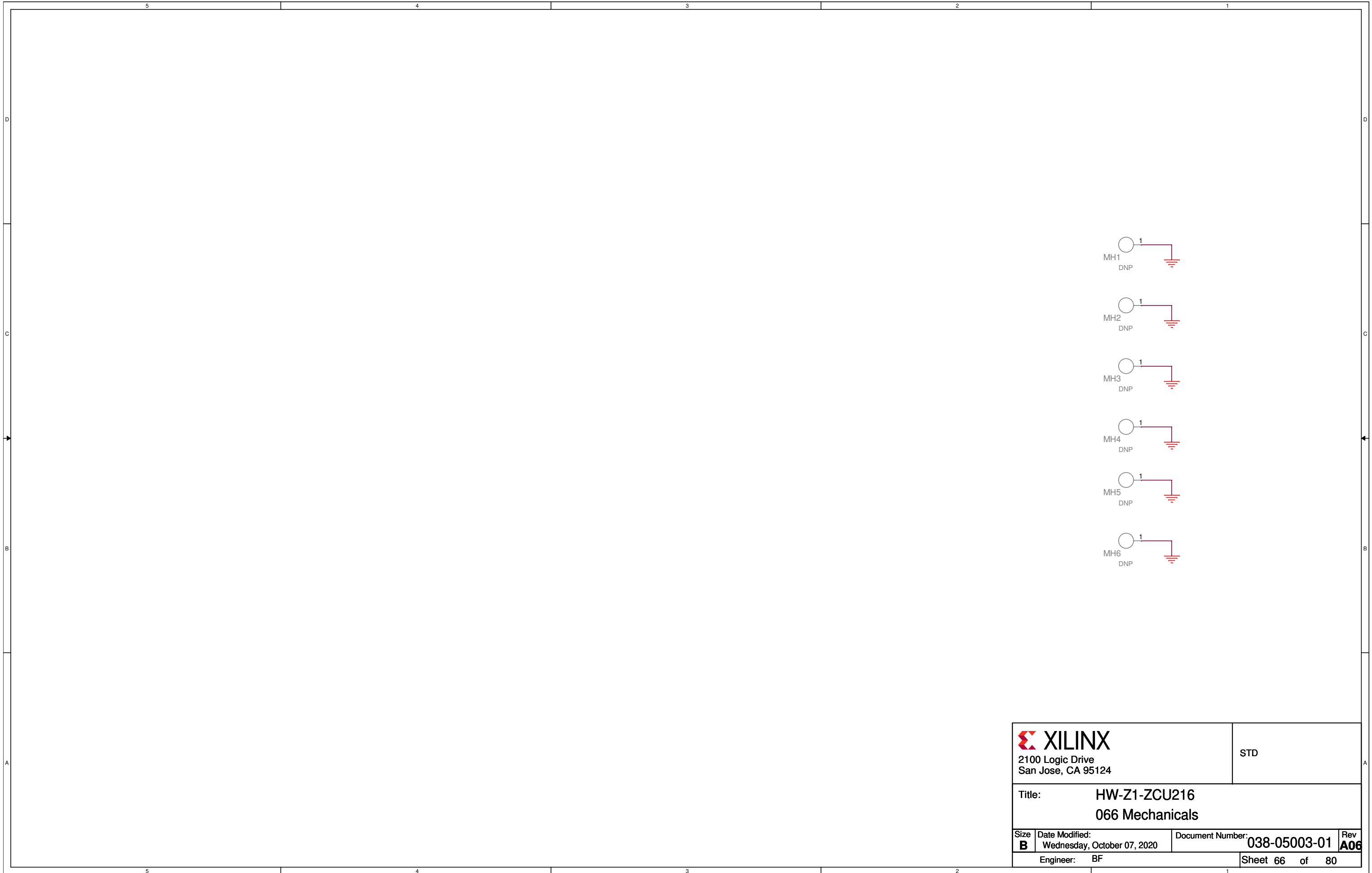
2100 Logic Drive
San Jose, CA 95124

STD

Title: **HW-Z1-ZCU216**
065 RFMC 2.0 Connector 2

Size Date Modified: **B** Wednesday, October 07, 2020 Document Number: **038-05003-01** Rev **A06**

Engineer: **BF** Sheet 65 of 80

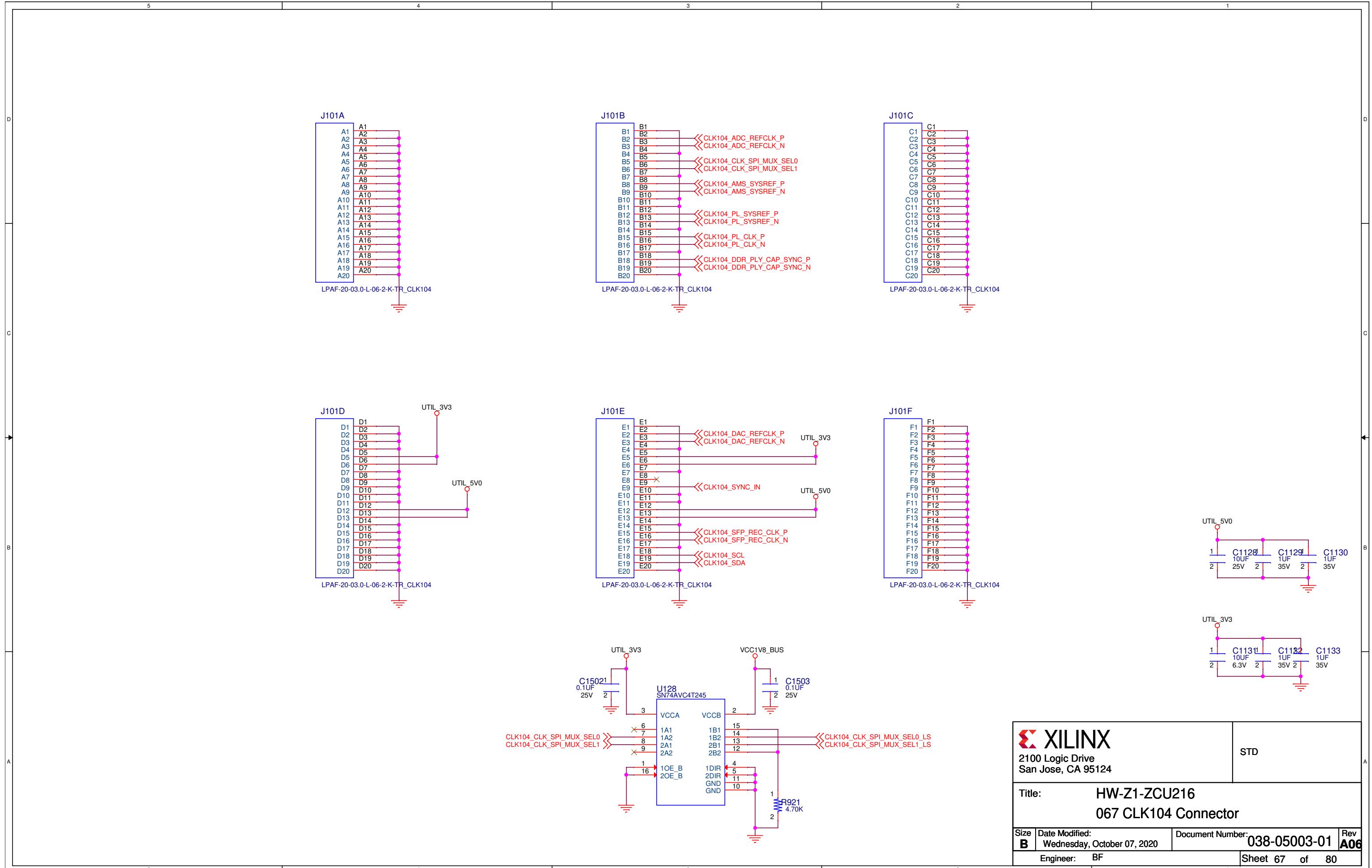


 XILINX
2100 Logic Drive
San Jose, CA 95124

STD

Title: HW-Z1-ZCU216
066 Mechanicals

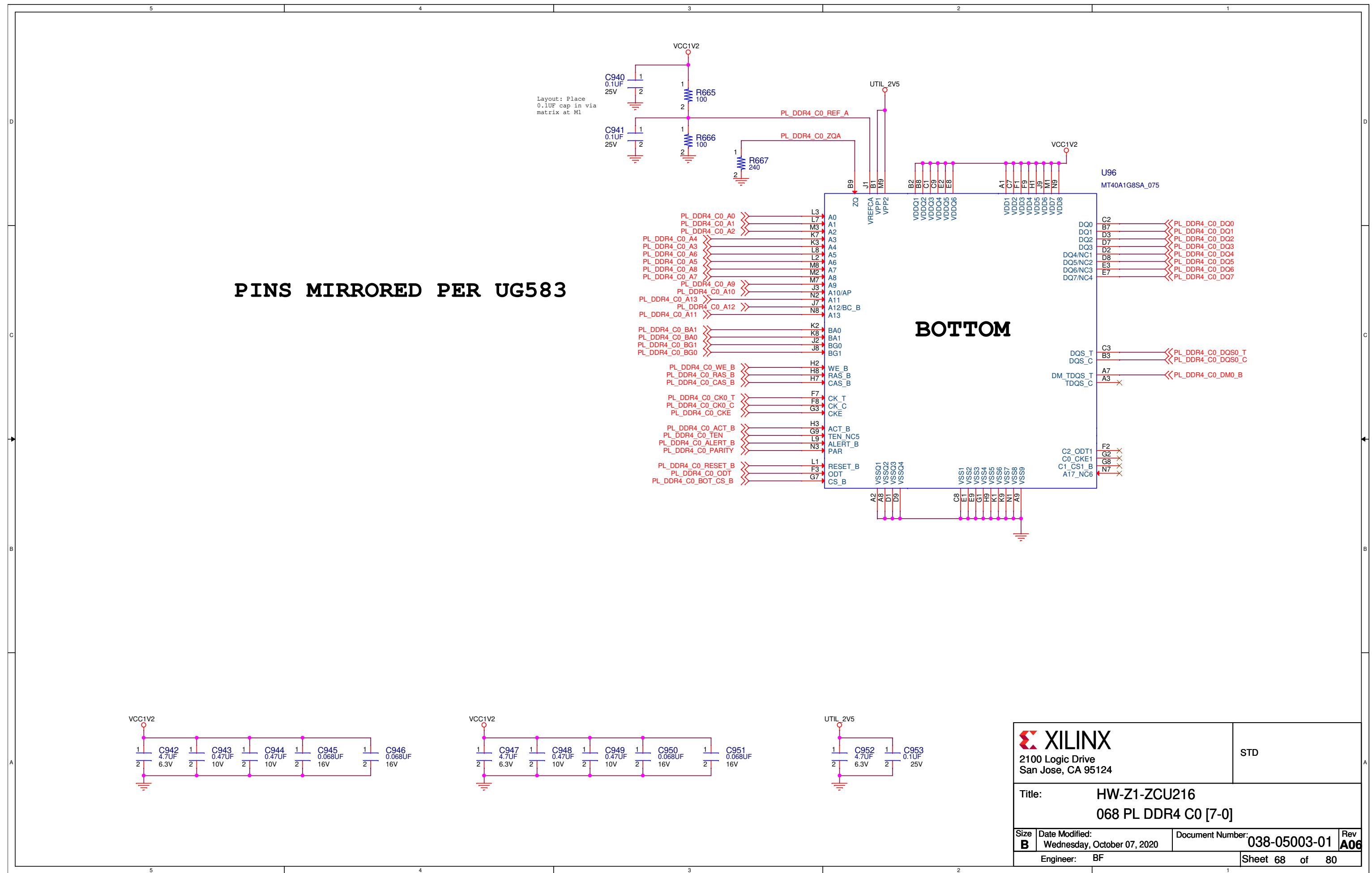
Size	Date Modified:	Document Number:
B	Wednesday, October 07, 2020	038-05003-01 Rev A06
Engineer: BF		Sheet 66 of 80

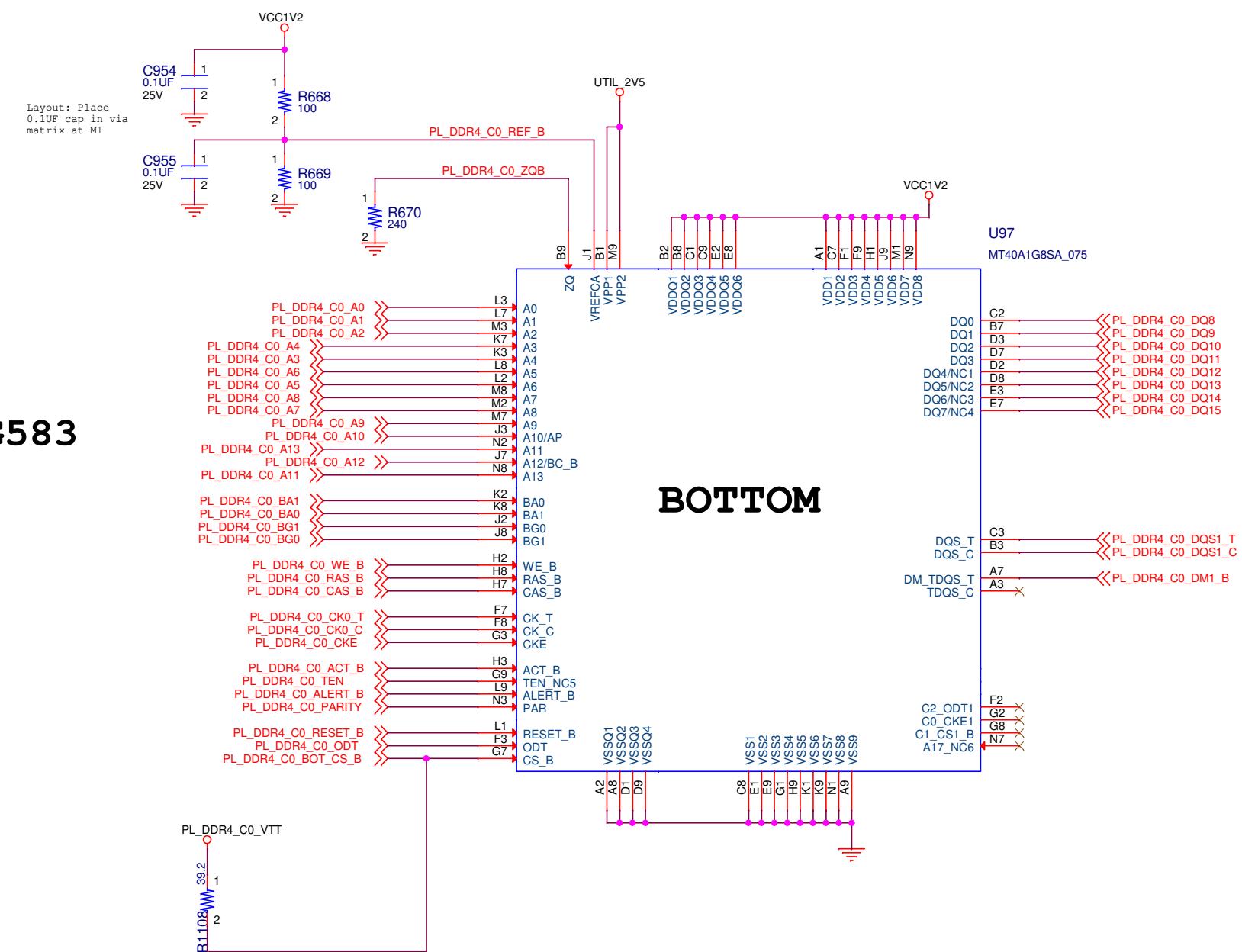
**XILINX**2100 Logic Drive
San Jose, CA 95124

STD

Title: HW-Z1-ZCU216
067 CLK104 ConnectorSize Date Modified: Document Number: Rev
B Wednesday, October 07, 2020 038-05003-01 **A06**

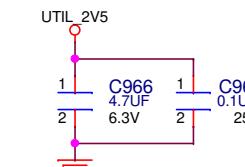
Engineer: BF Sheet 67 of 80



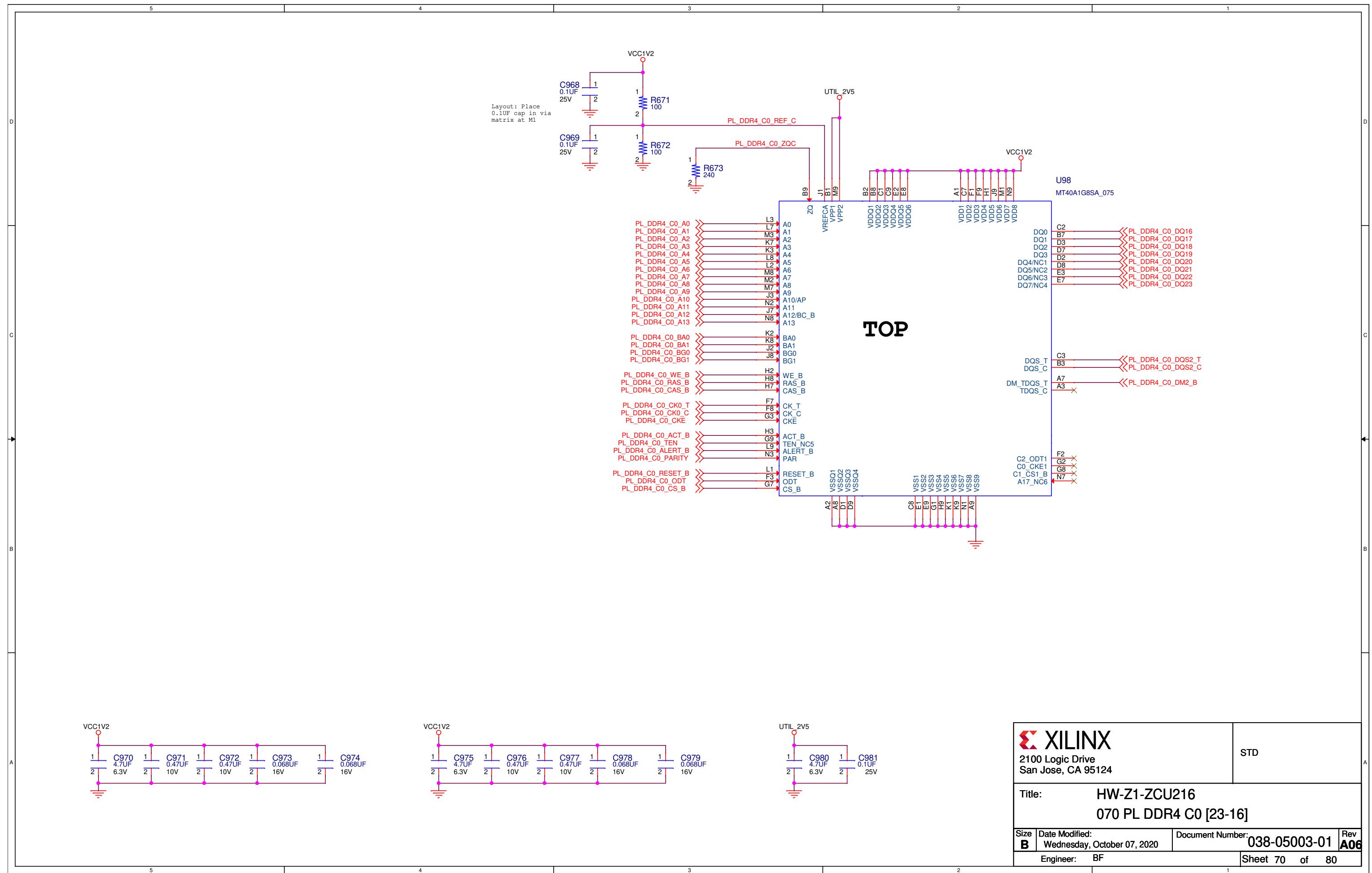


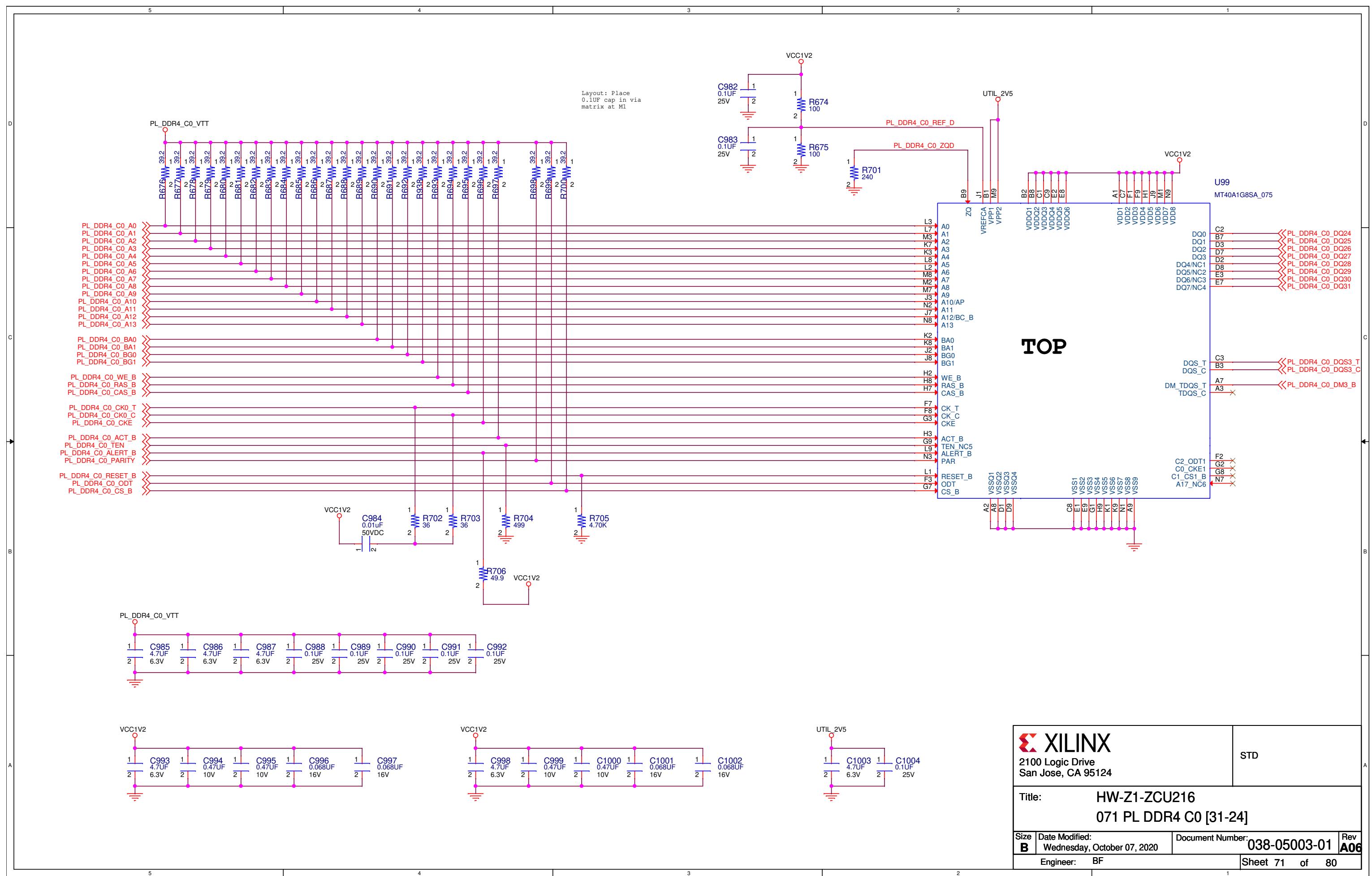
PINS MIRRORED PER UG583

BOTTOM

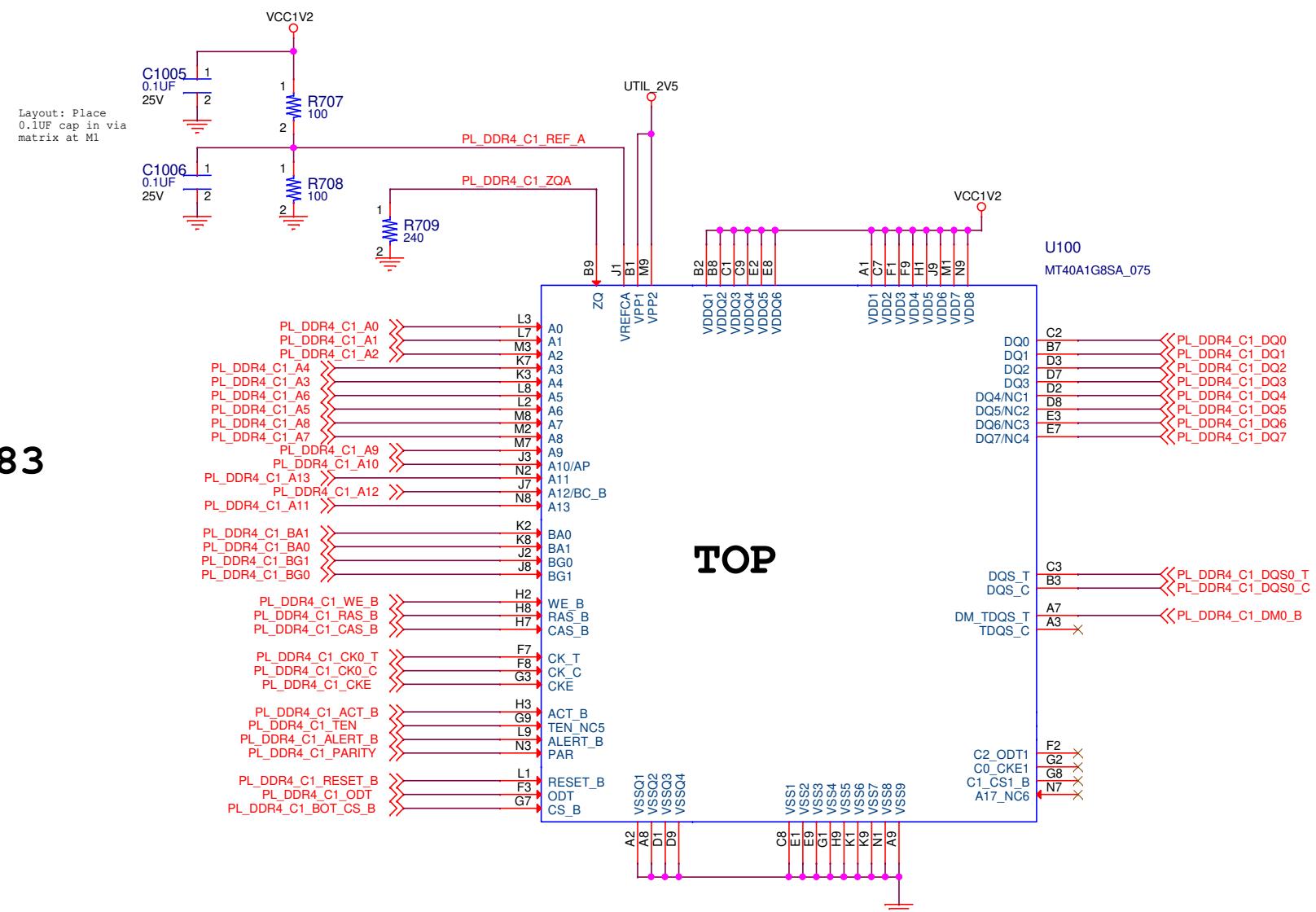


 XILINX 2100 Logic Drive San Jose, CA 95124	STD		
Title: HW-Z1-ZCU216 069 PL DDR4 C0 [15-8]			
Size B	Date Modified: Wednesday, October 07, 2020	Document Number: 038-05003-01	Rev A06
Engineer: BF		Sheet 69	of 80

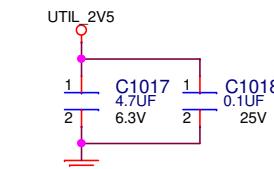
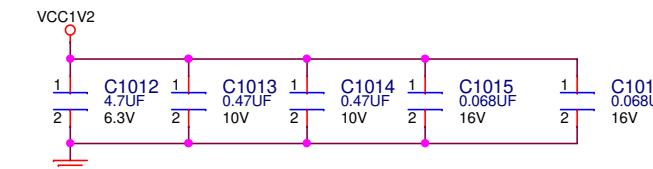
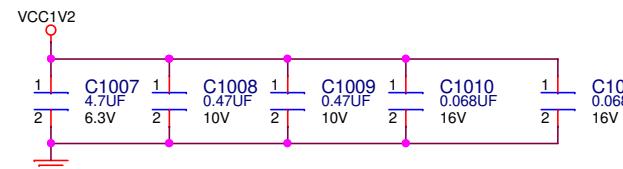
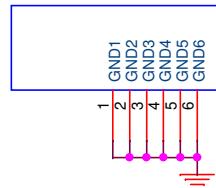




PINS MIRRORED PER UG583



C1_TOPCAGE1

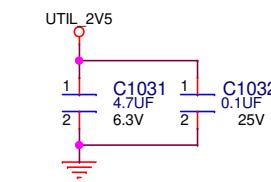
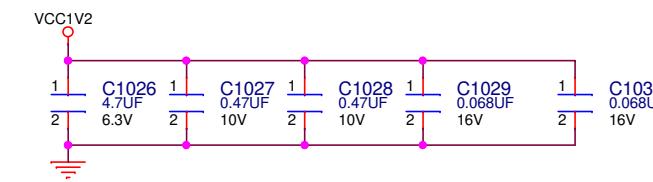
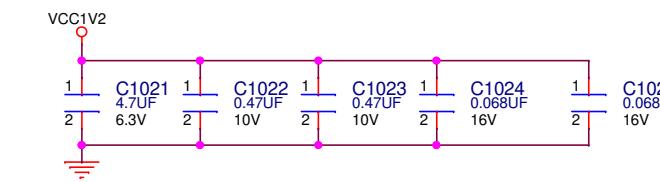


XILINX
2100 Logic Drive
San Jose, CA 95124

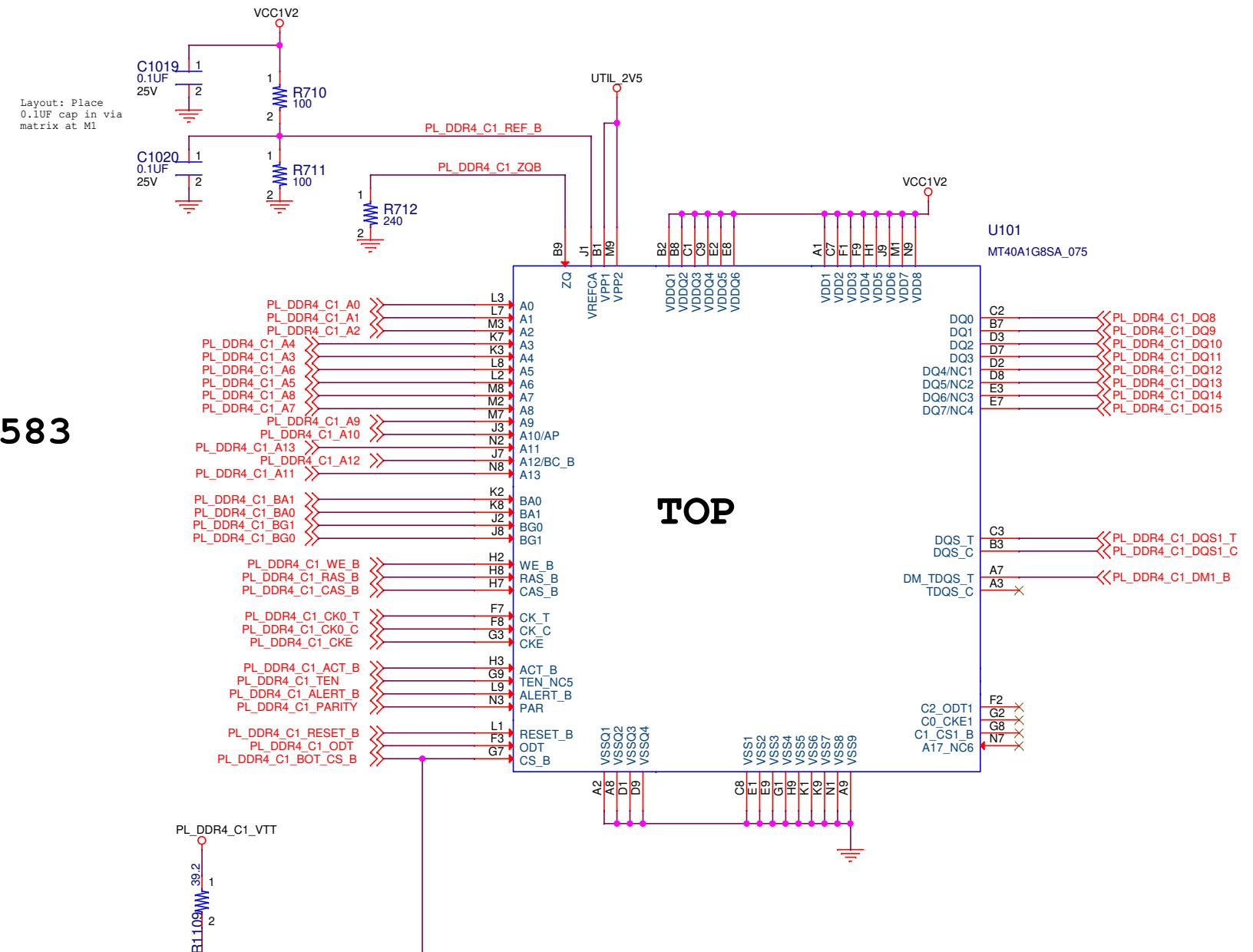
STD

Title: HW-Z1-ZCU216
072 PL DDR4 C1 [7-0]

Size	Date Modified:	Document Number:
B	Wednesday, October 07, 2020	038-05003-01 Rev A06
Engineer: BF	Sheet 72 of 80	

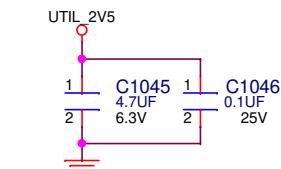
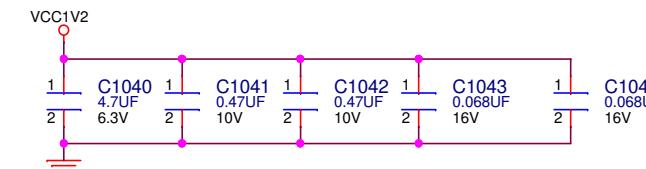
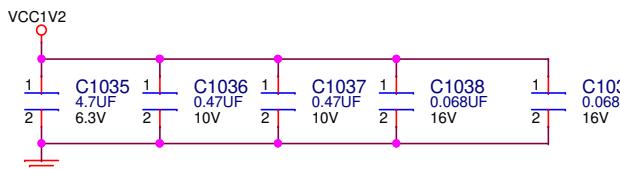
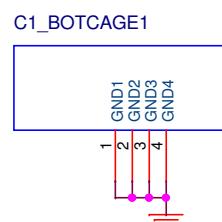
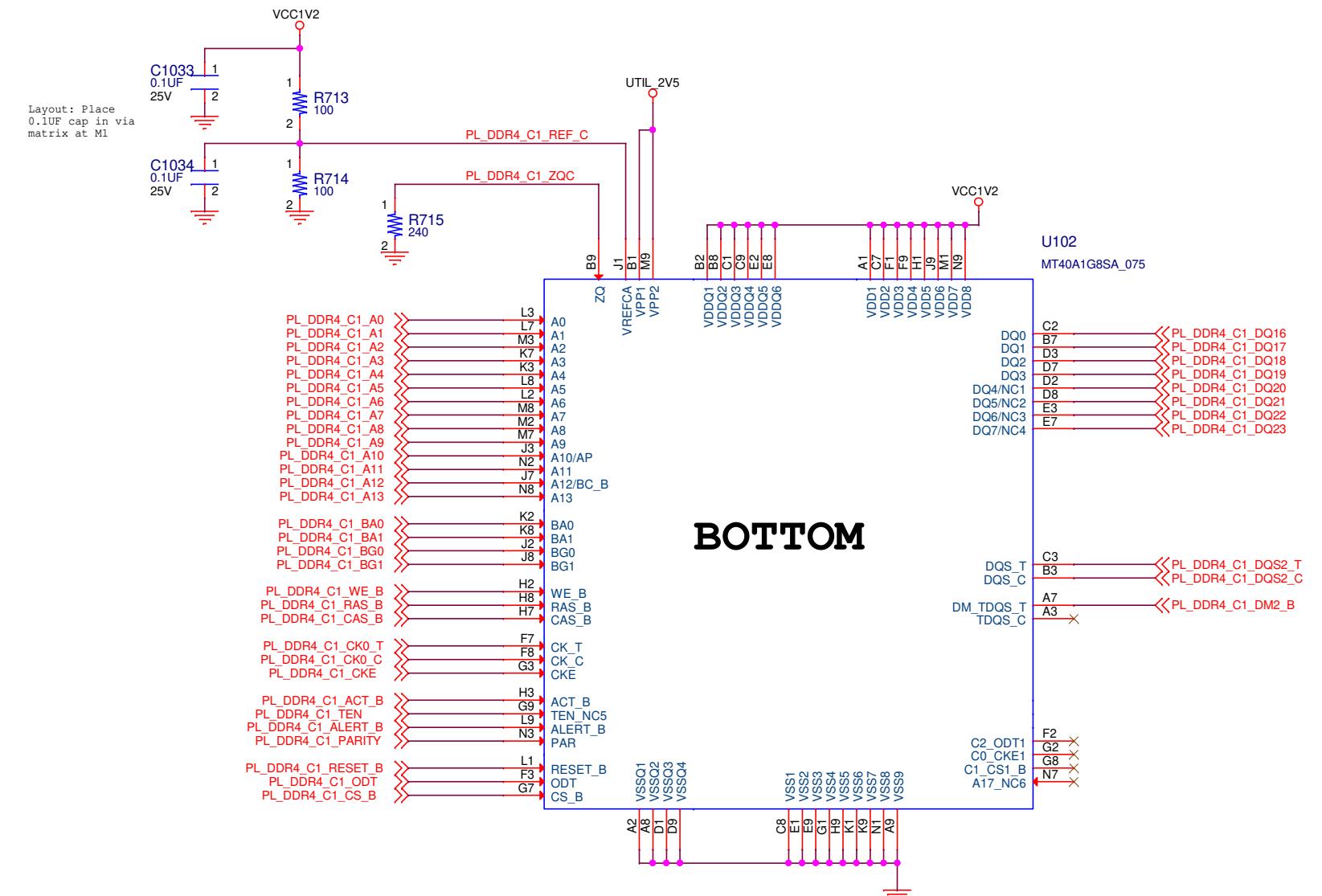


PINS MIRRORED PER UG583



TOP

XILINX 2100 Logic Drive San Jose, CA 95124		STD
Title: HW-Z1-ZCU216 073 PL DDR4 C1 [15-8]		
Size: B	Date Modified: Wednesday, October 07, 2020	Document Number: 038-05003-01 Rev A06
Engineer: BF		Sheet 73 of 80

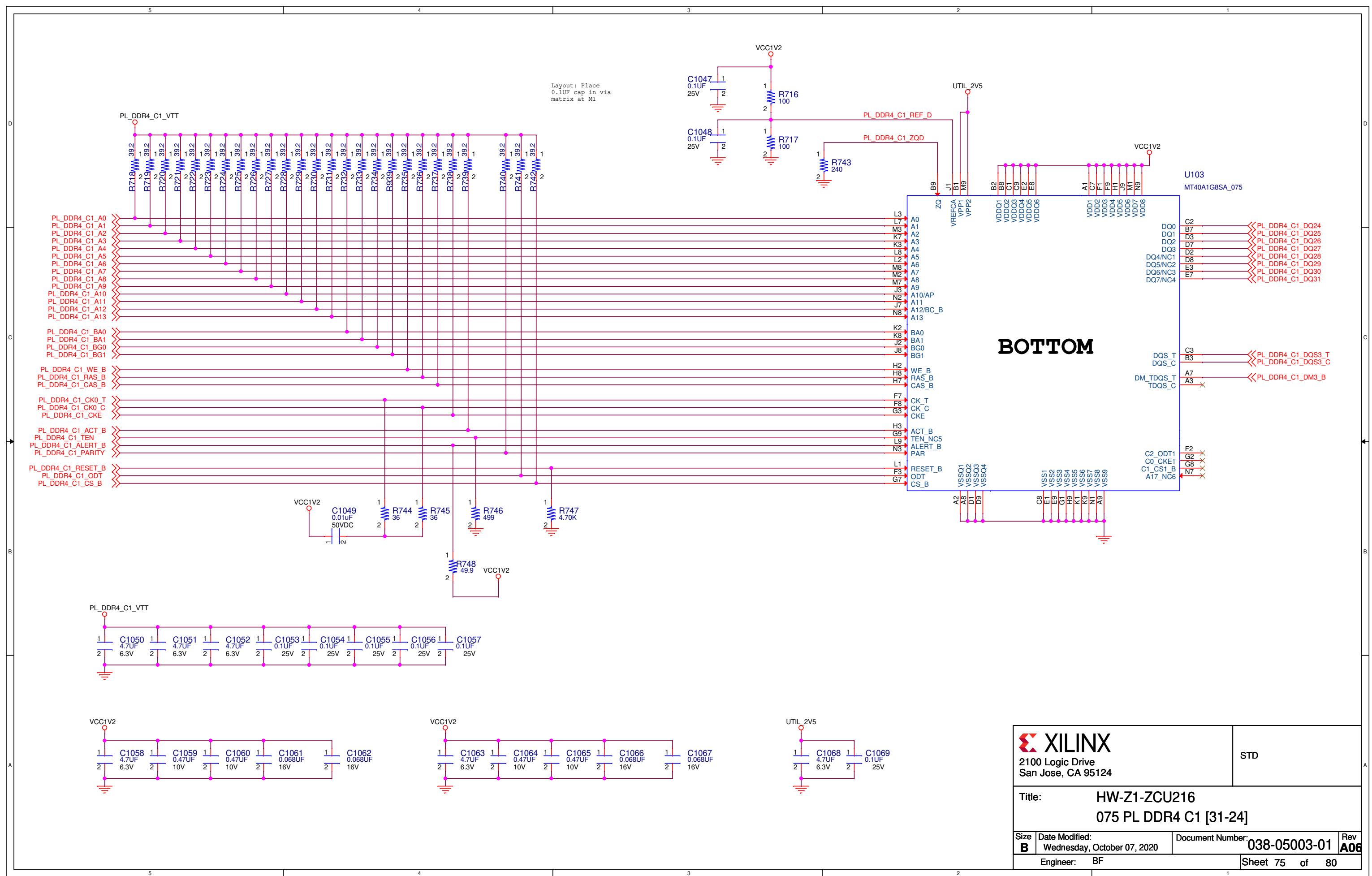


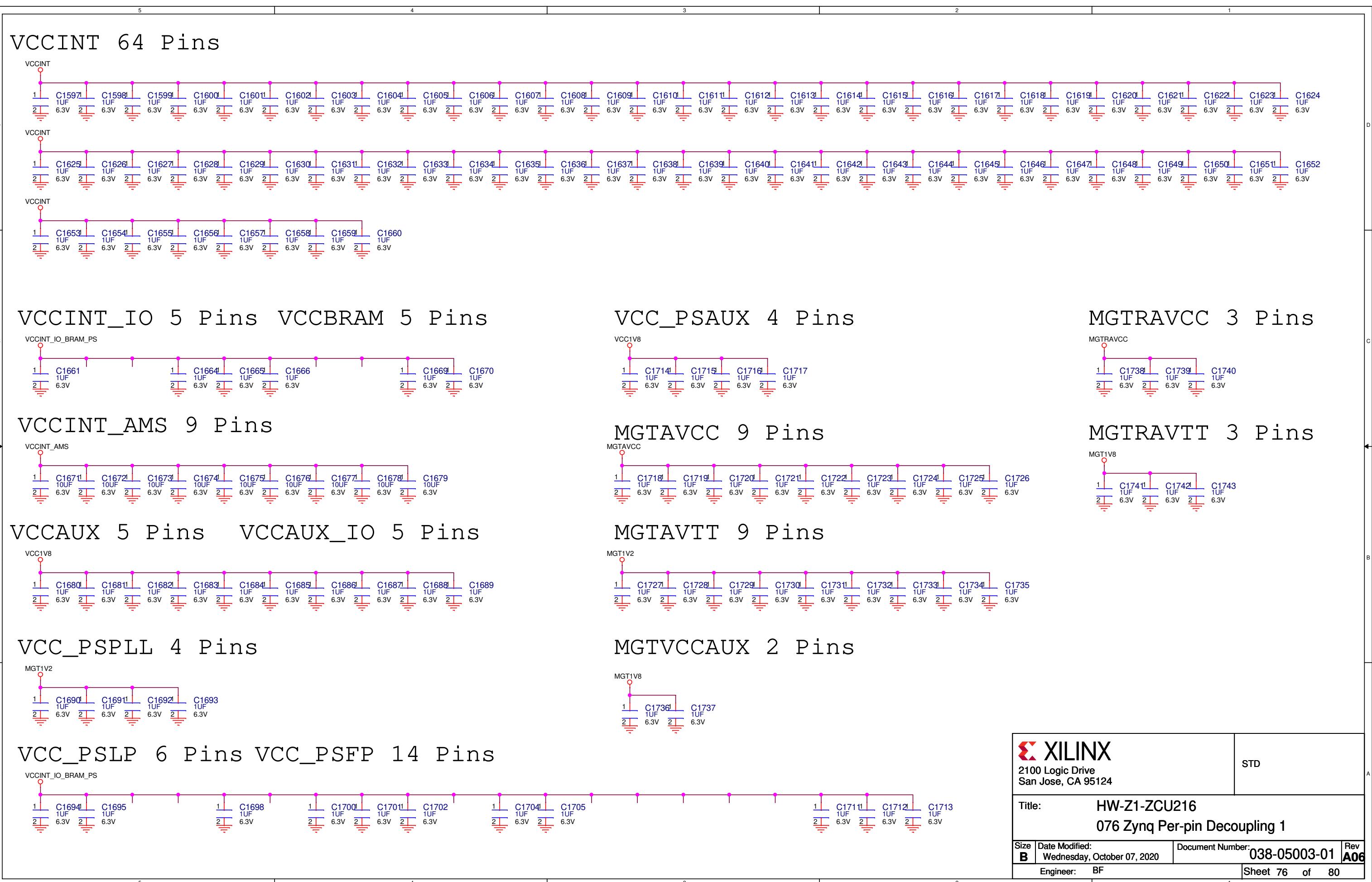
The Xilinx logo consists of a stylized red 'X' followed by the word "XILINX" in a bold, black, sans-serif font. Below the logo, the company's address is listed: "2100 Logic Drive" on one line and "San Jose, CA 95124" on the line below.

STD

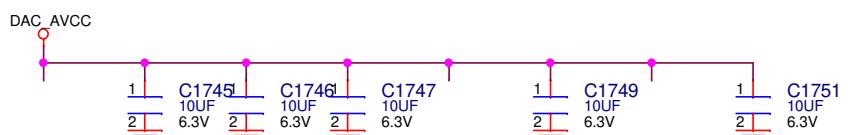
Title: HW-Z1-ZCU216
074 PL DDR4 C1 [23-16]

Size	Date Modified: Wednesday, October 07, 2020	Document Number: 038-05003-01	Rev A06
Engineer:	BF	Sheet 74 of 80	

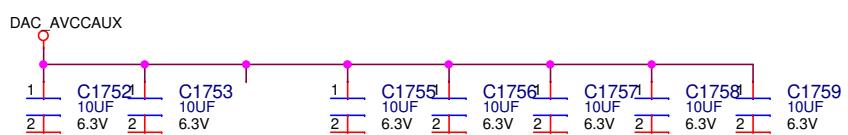




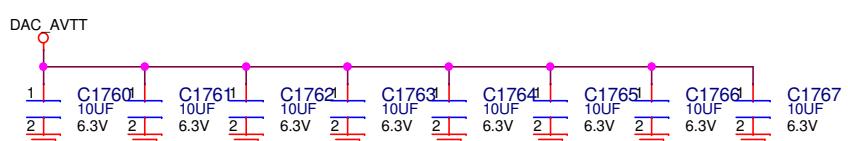
DAC_AVCC 8 Pins



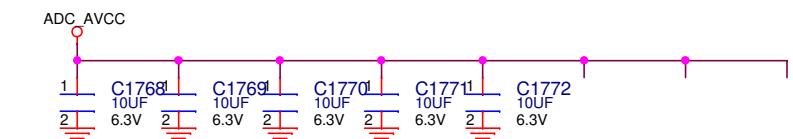
DAC_AVCCAUX 8 Pins



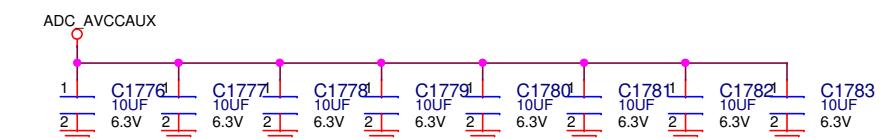
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ADC_AVCC 8 Pins



ADC_AVCCAUX 8 Pins



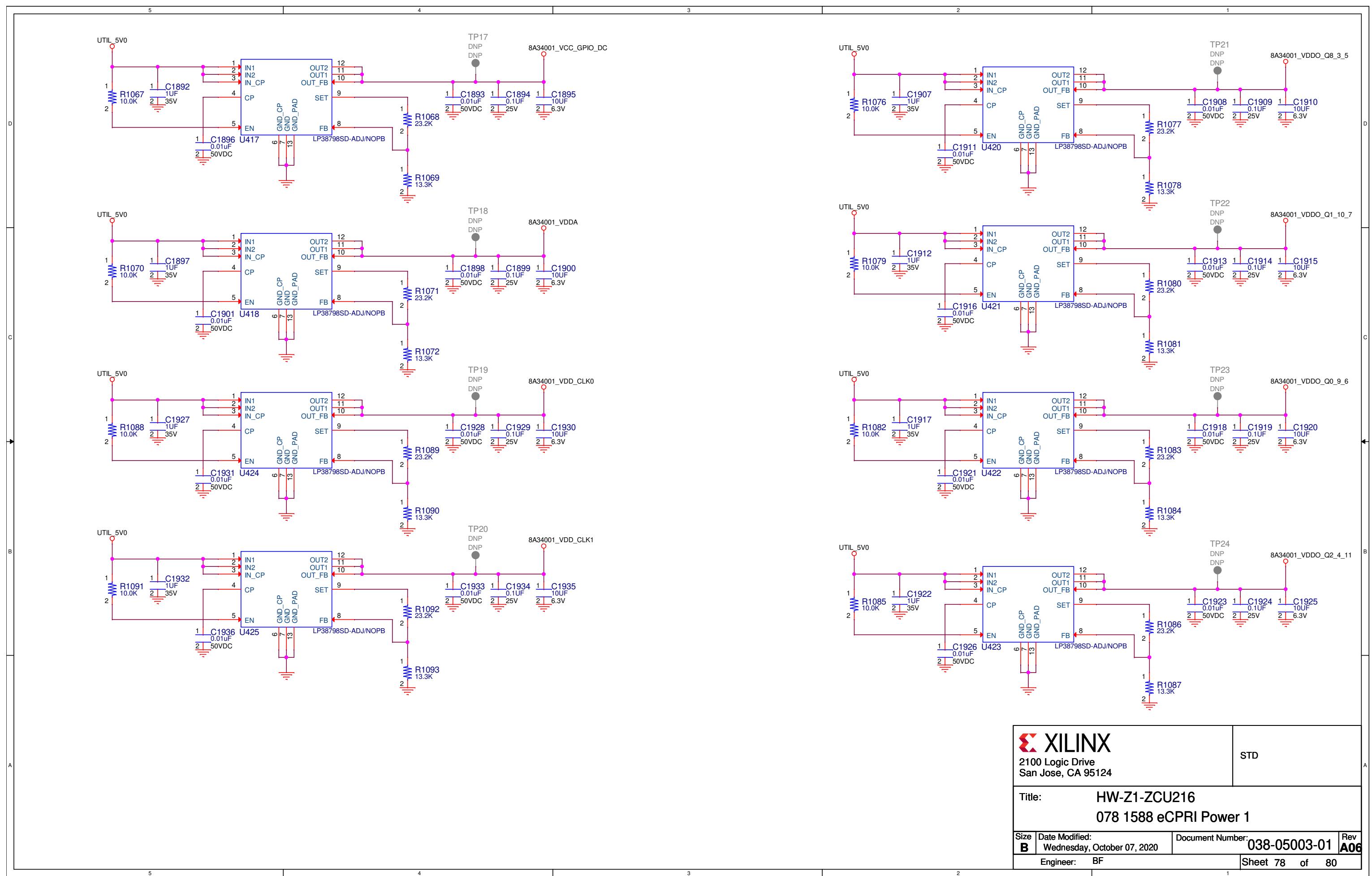
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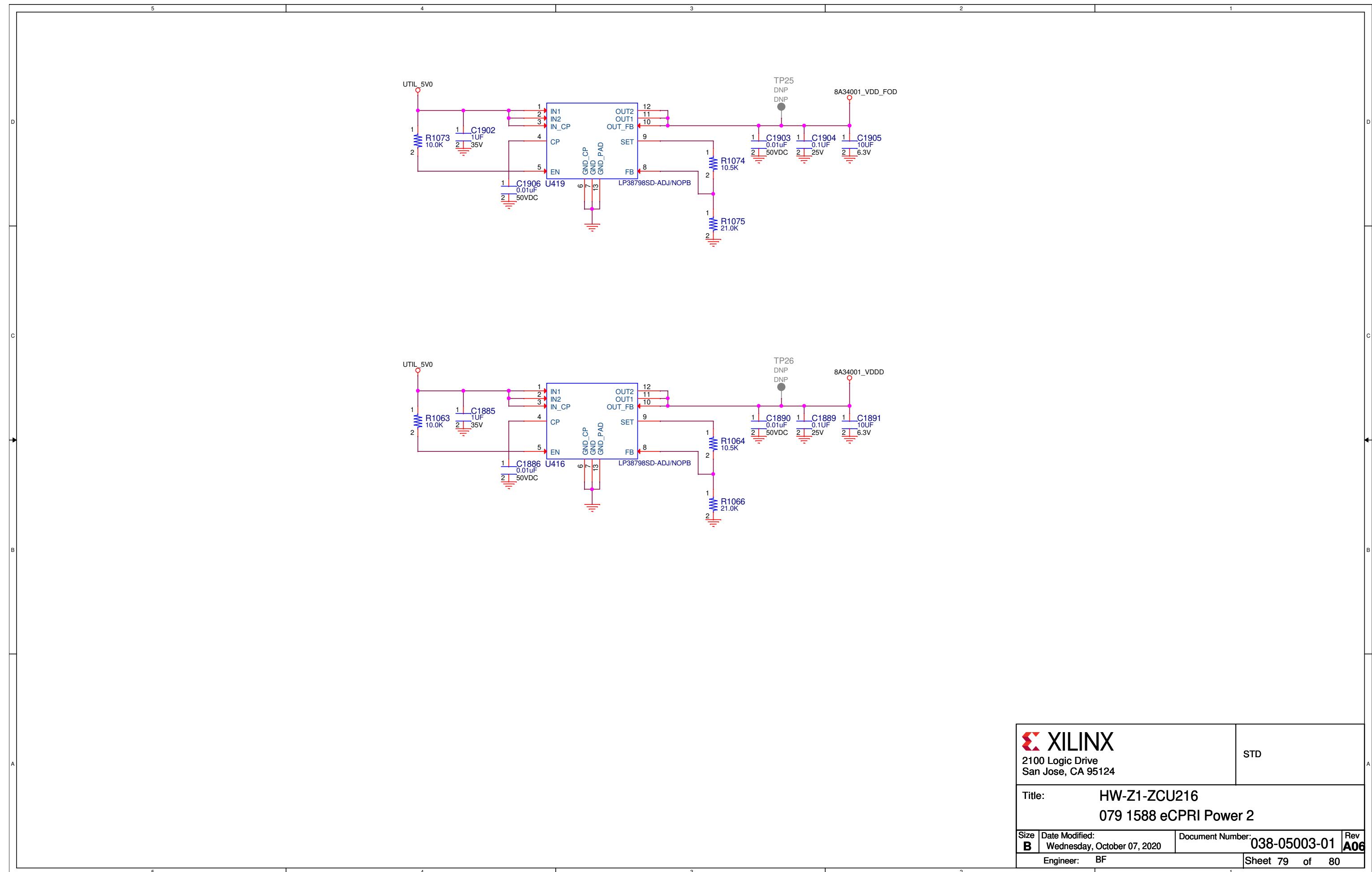
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STD

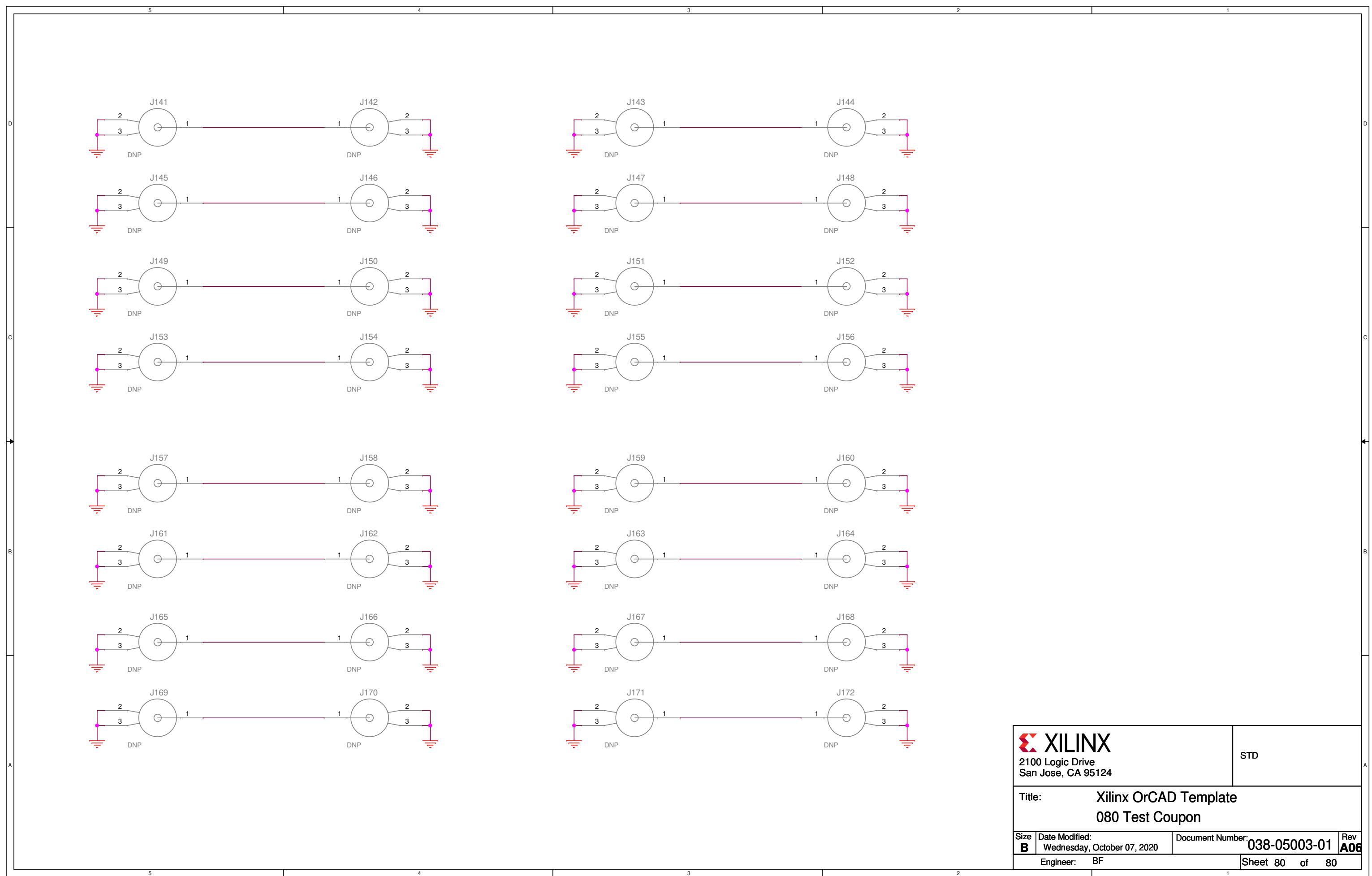
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B	Wednesday, October 07, 2020	038-05003-01 Rev A06
Engineer: BF		Sheet 77 of 80





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Sheet 80 of 80