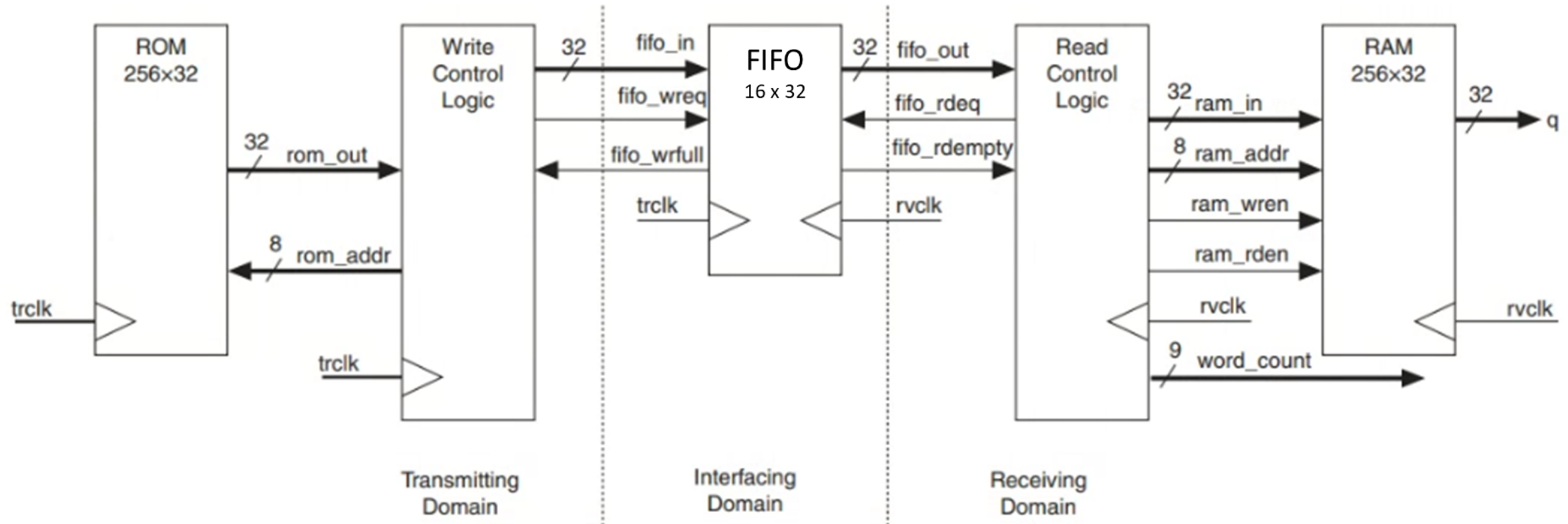


Reading & Writing Control of ROM to FIFO to RAM

Agenda

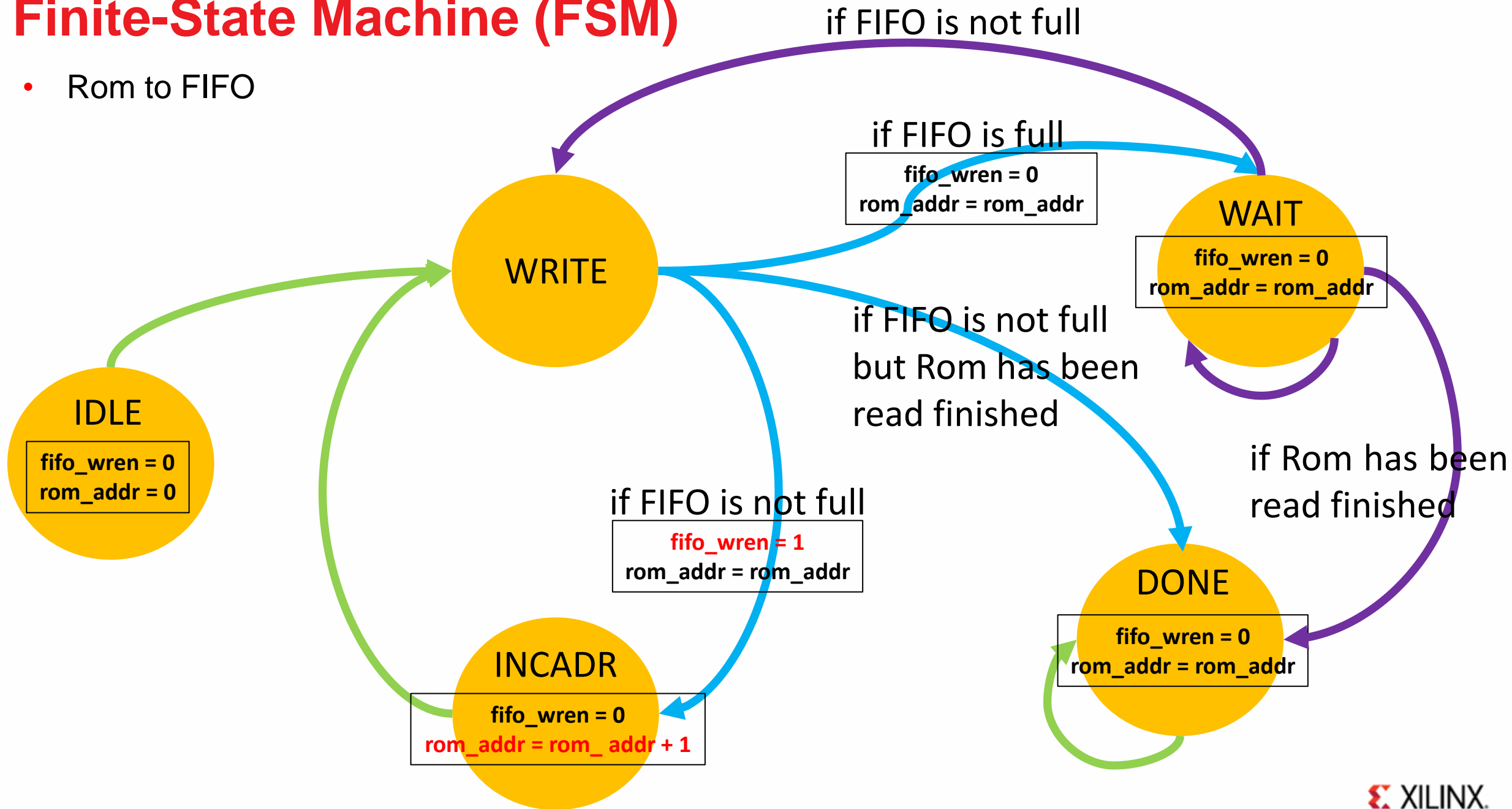
- Structure of Circuit
- Finite-State Machine
- Results of Simulation
- Timing Constraints
- Results of Synthesis

Structure of Circuit



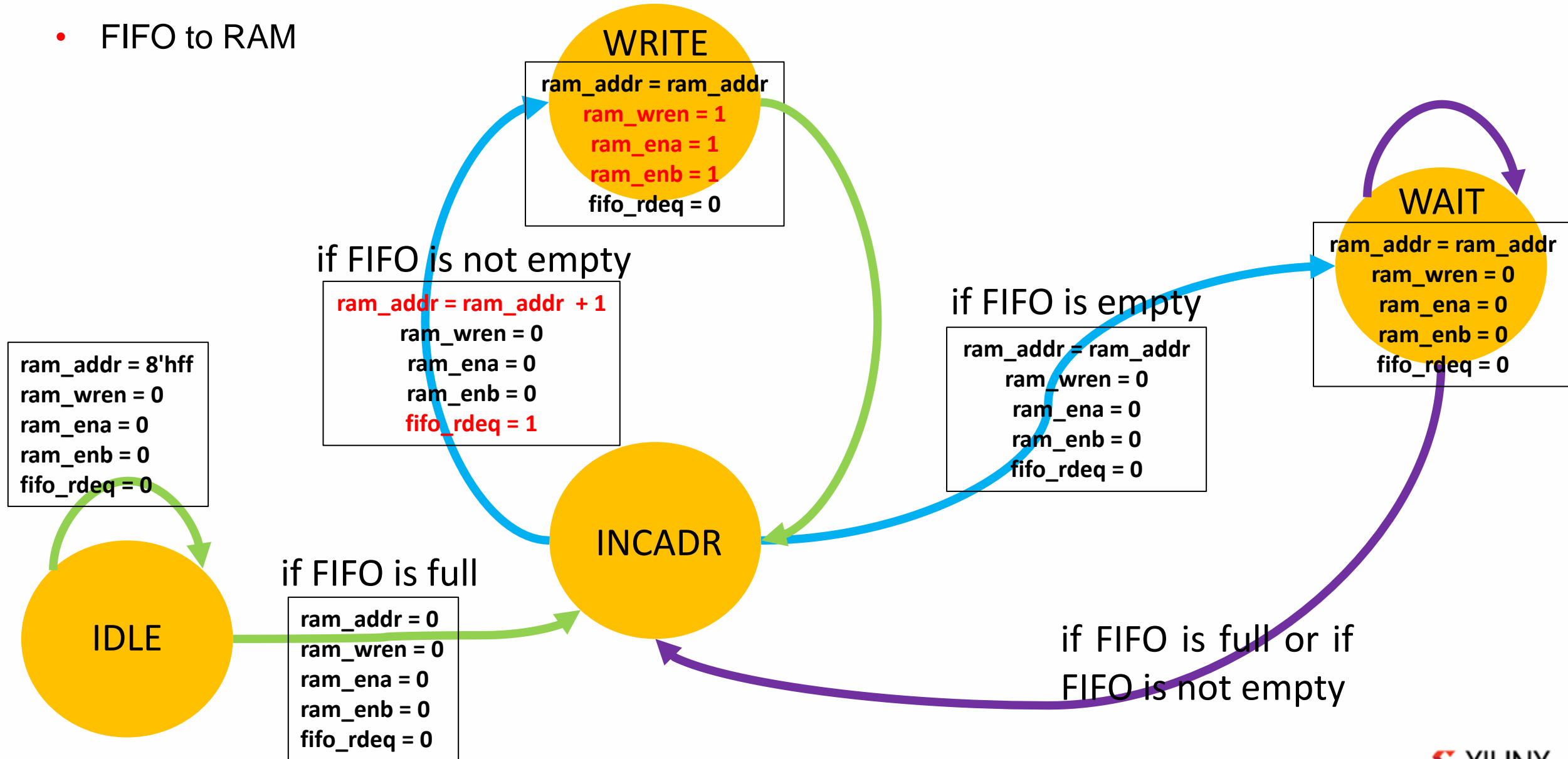
Finite-State Machine (FSM)

- Rom to FIFO

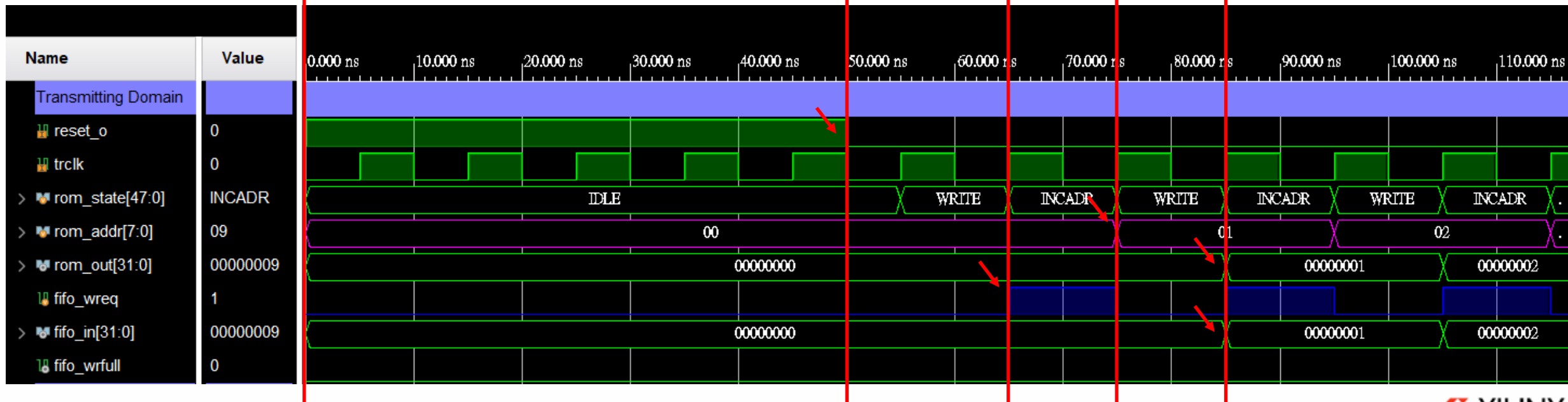
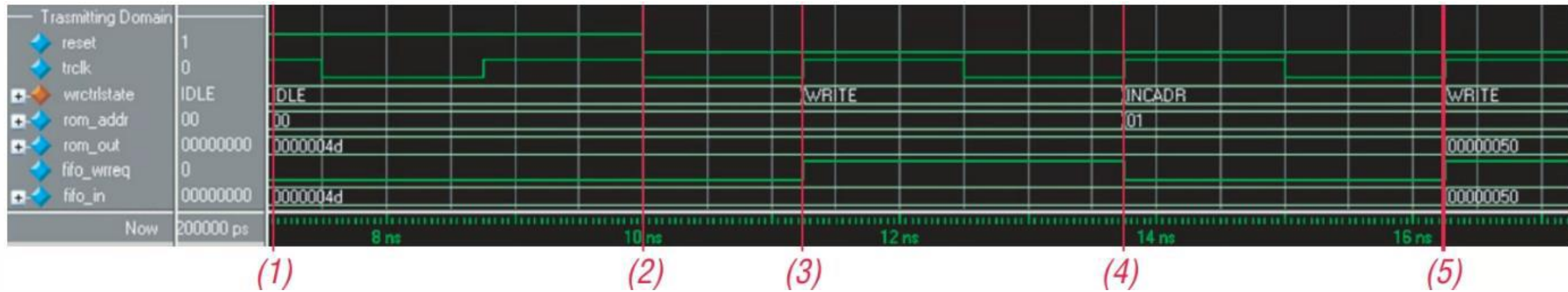


Finite-State Machine (FSM)

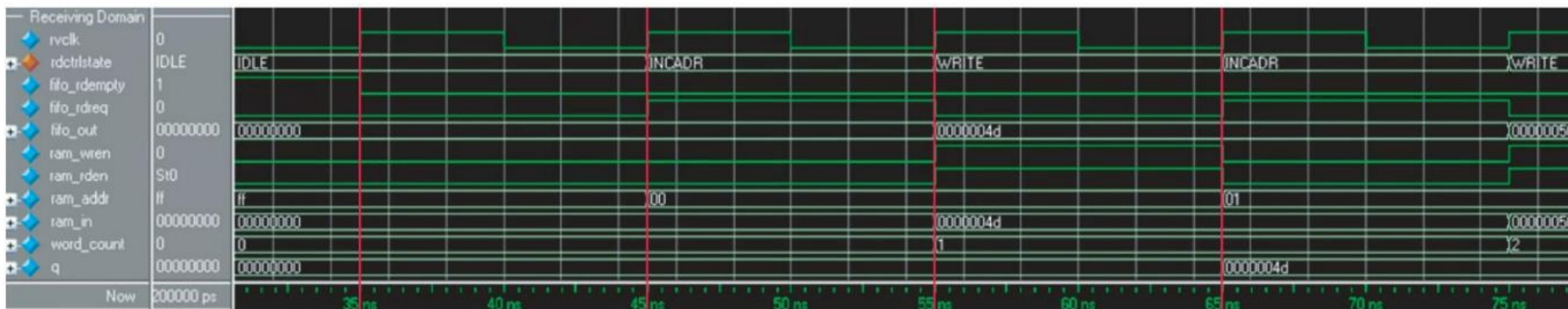
- FIFO to RAM



Results of Simulation – Transmitting Domain



Results of Simulation – Receiving Domain

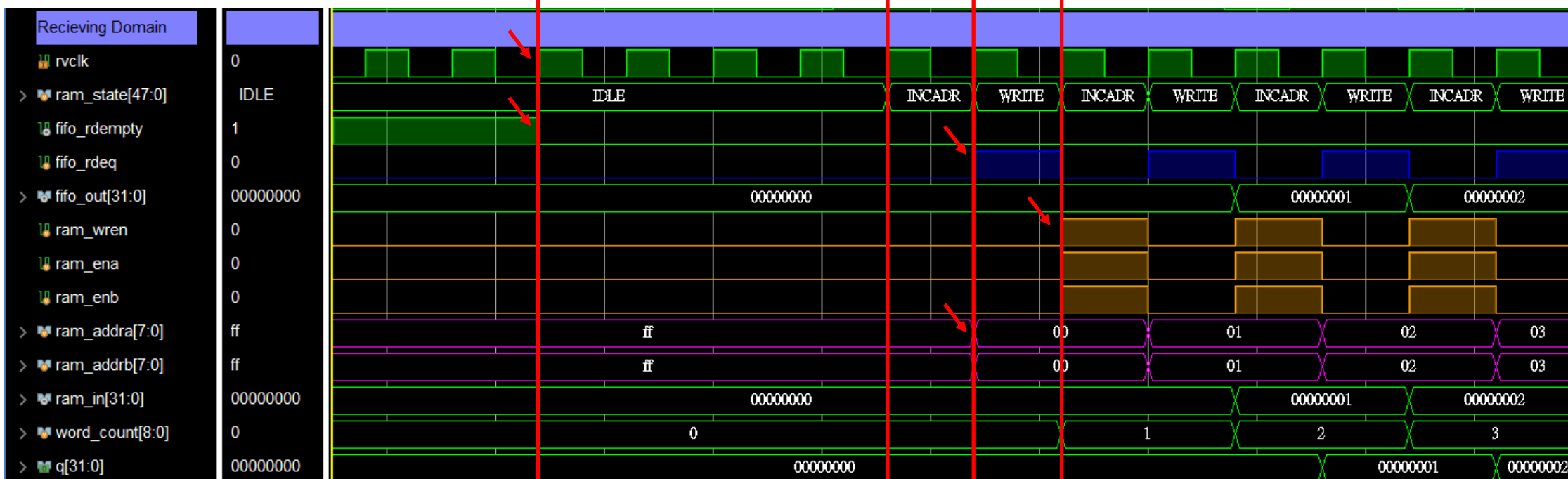


(1)

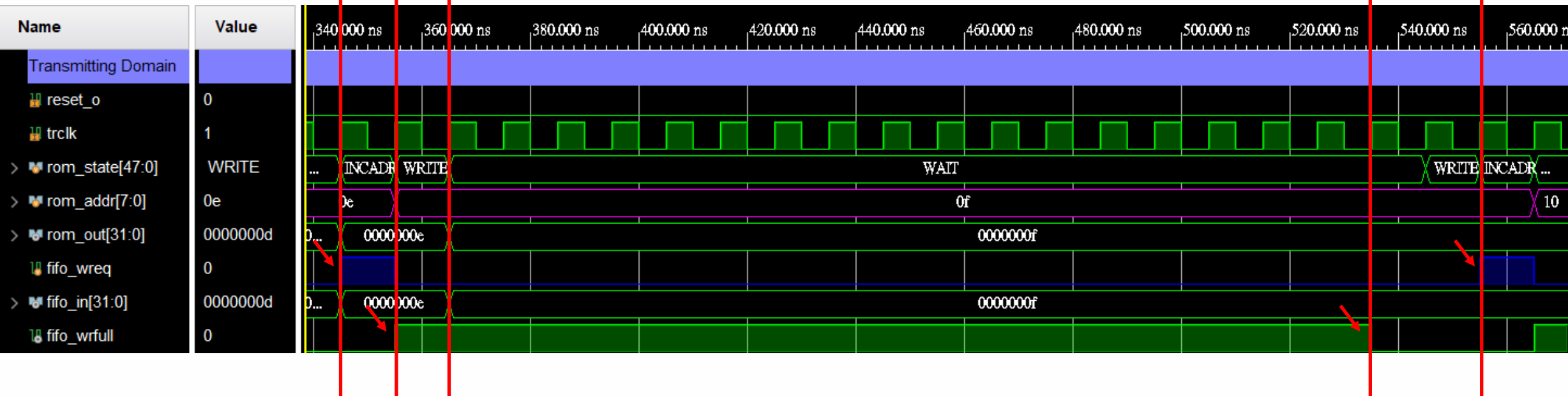
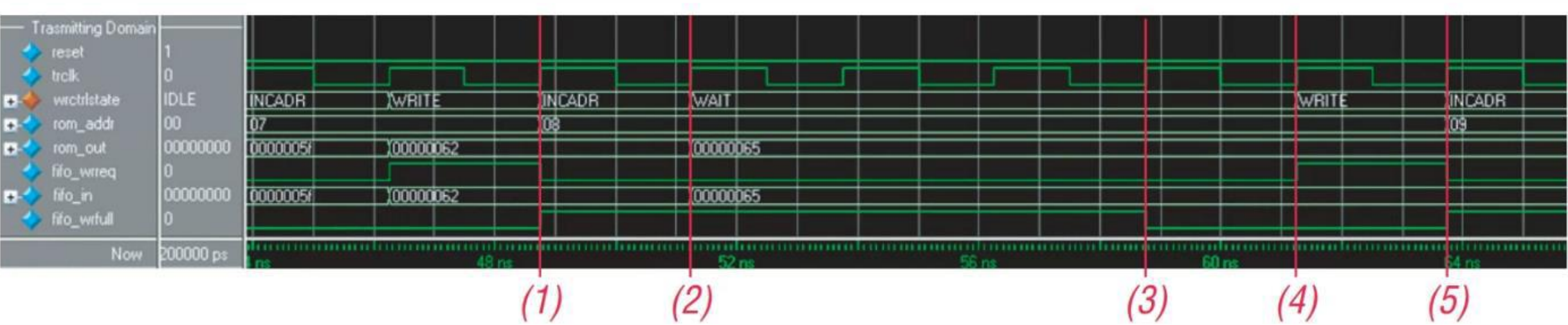
(2)

(3)

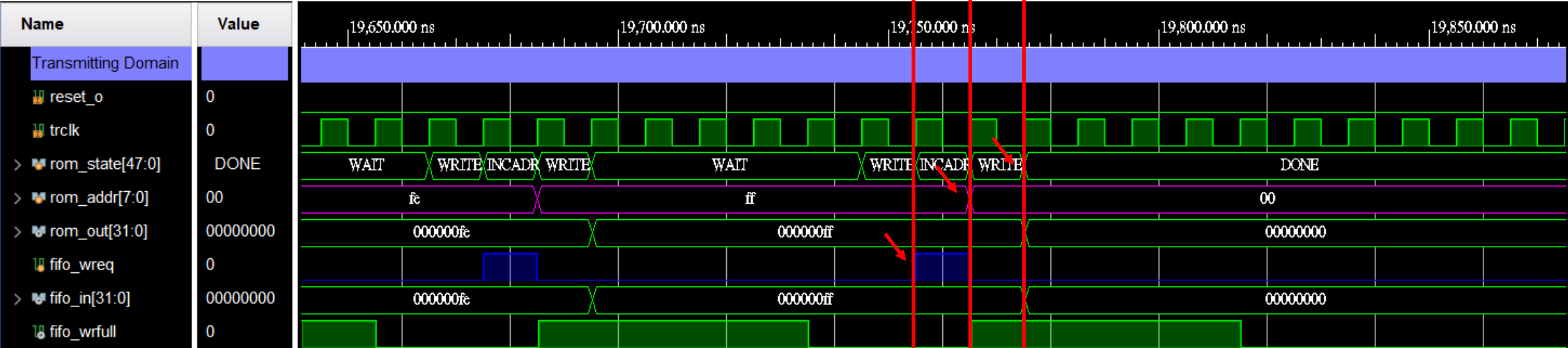
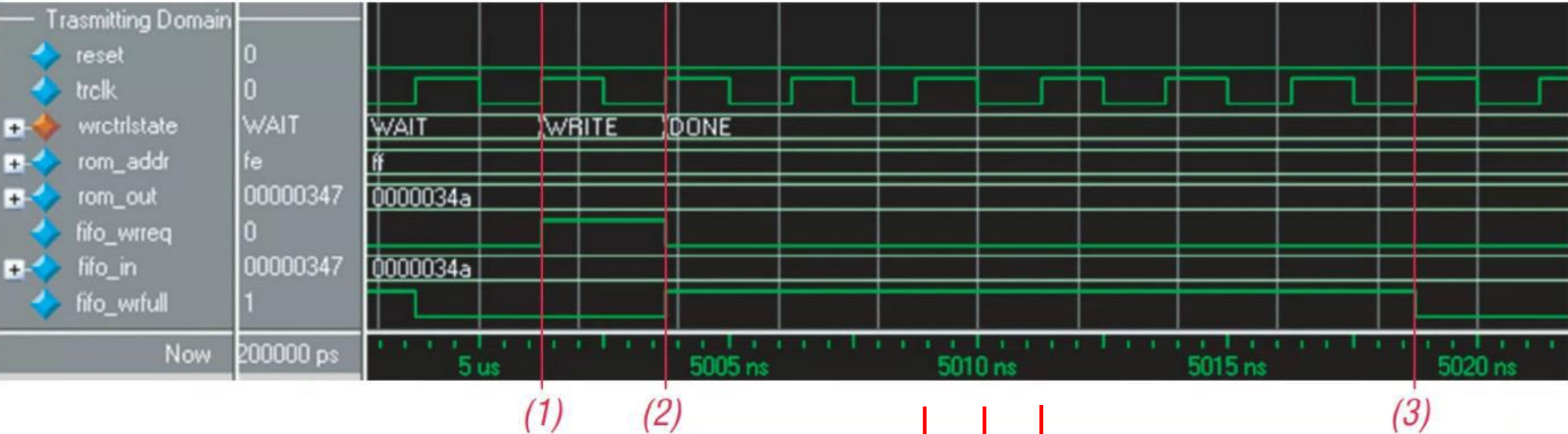
(4)



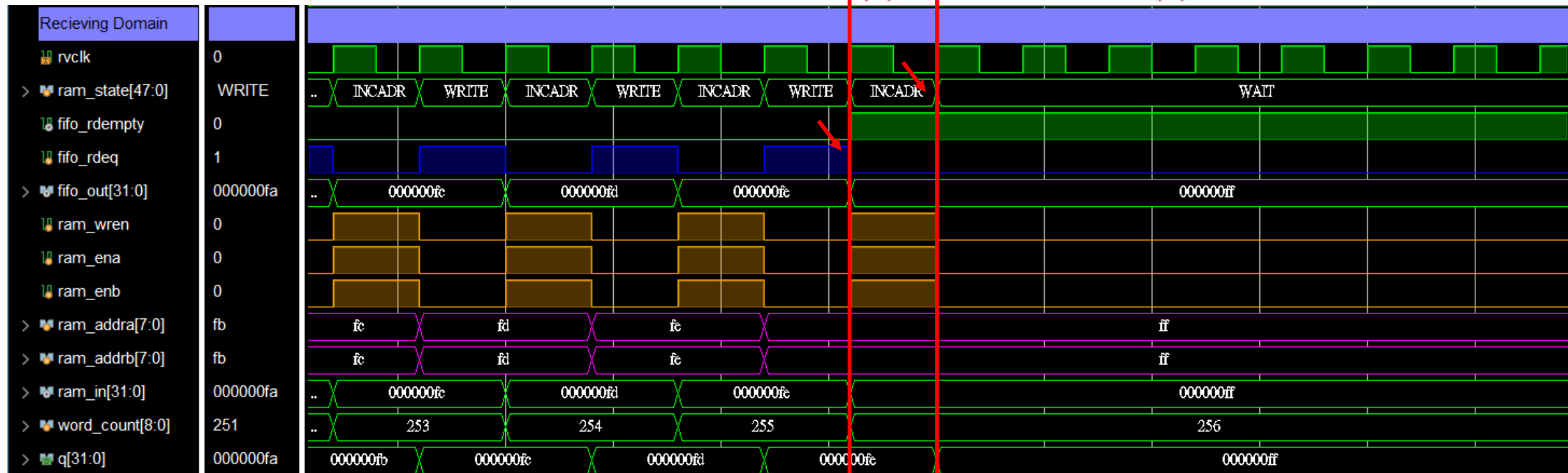
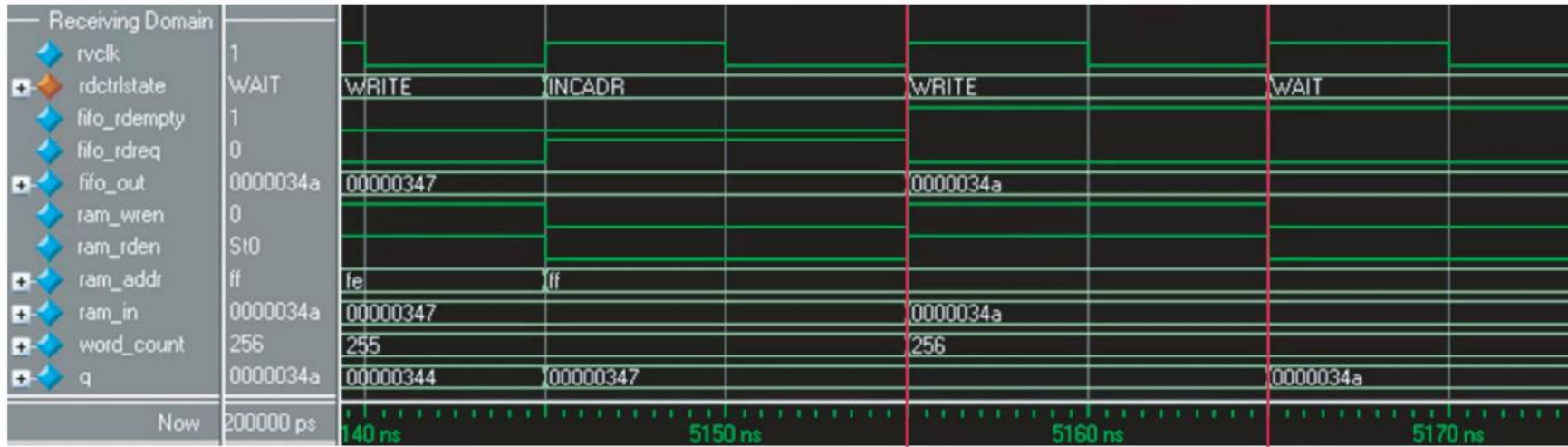
Results of Simulation – When FIFO is full



Results of Simulation – completion of ROM to FIFO



Results of Simulation – completion of FIFO to RAM



Timing Constraints

- trclk is 200MHz, and rvclk is 50MHz

Project Summary

Device

ROM2FIFO.v

Timing Constraints

≡

⬇

✦

+

+

-

✎

Create Clock

▼ Clocks (2)

Create Clock (2)

Create Generated Clock (0)

Rename Auto-Derived Clock (0)

Set Clock Latency (0)

Set Clock Uncertainty (0)

Set Clock Groups (0)

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Current Instance
1	ram_clk	20.000	0.000	10.000	<input type="checkbox"/>	[get_ports rvclk]	timing.xdc		
2	rom_clk	5.000	0.000	2.500	<input type="checkbox"/>	[get_ports trclk]	timing.xdc		

Double click to create a Create Clock constraint

Results of Synthesis

- fsm_extraction: auto

The screenshot displays the Vivado IDE interface. The top window is the 'Settings' dialog, specifically the 'Strategies > Run Strategies' tab. It shows the 'Flow' set to 'Vivado Synthesis 2021' and the 'Name' as 'Vivado Synthesis Defaults'. A red box highlights the 'Options' section, where '-fsm_extraction' is set to 'auto'. Below this, a description for '-fsm_extraction' reads 'FSM Extraction Encoding.'.

The bottom window is the 'Timing' tab, showing the 'Design Timing Summary'. A red arrow points from the text 'WNS = 0.380 ns' to the 'Worst Negative Slack (WNS)' value of '0.380 ns' in the 'Setup' column. The summary table is as follows:

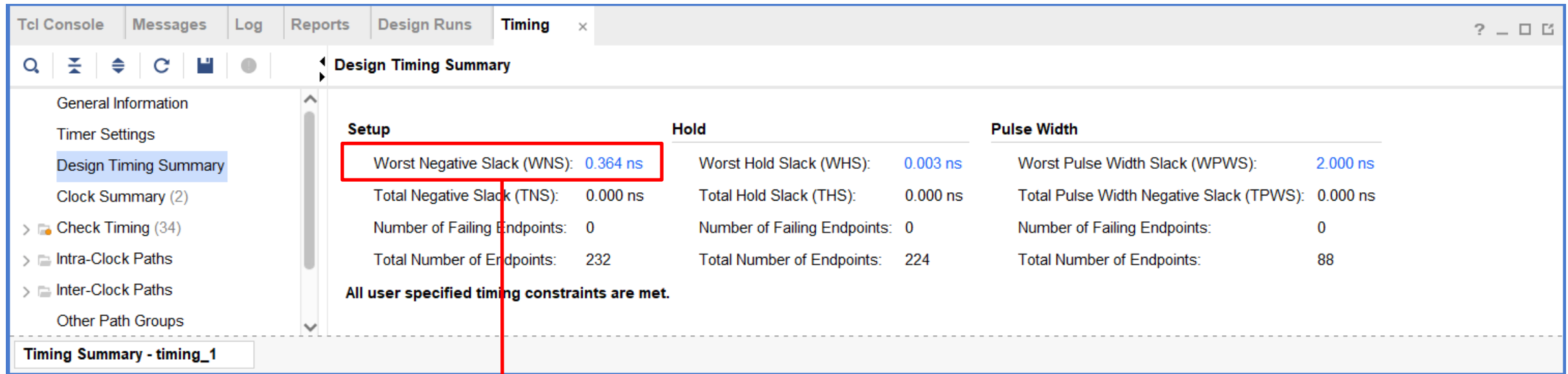
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.380 ns	Worst Hold Slack (WHS): -0.046 ns	Worst Pulse Width Slack (WPWS): 2.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): -0.046 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 1	Number of Failing Endpoints: 0
Total Number of Endpoints: 232	Total Number of Endpoints: 224	Total Number of Endpoints: 89

Below the table, it states 'Timing constraints are not met.' The left sidebar of the Timing window shows a tree view with 'Design Timing Summary' selected.

WNS = 0.380 ns

Results of Synthesis

- fsm_extraction: gray



Timing			
Design Timing Summary			
General Information	Setup	Hold	Pulse Width
Timer Settings	Worst Negative Slack (WNS): 0.364 ns	Worst Hold Slack (WHS): 0.003 ns	Worst Pulse Width Slack (WPWS): 2.000 ns
Design Timing Summary	Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Clock Summary (2)	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
> Check Timing (34)	Total Number of Endpoints: 232	Total Number of Endpoints: 224	Total Number of Endpoints: 88
> Intra-Clock Paths	All user specified timing constraints are met.		
> Inter-Clock Paths			
Other Path Groups			

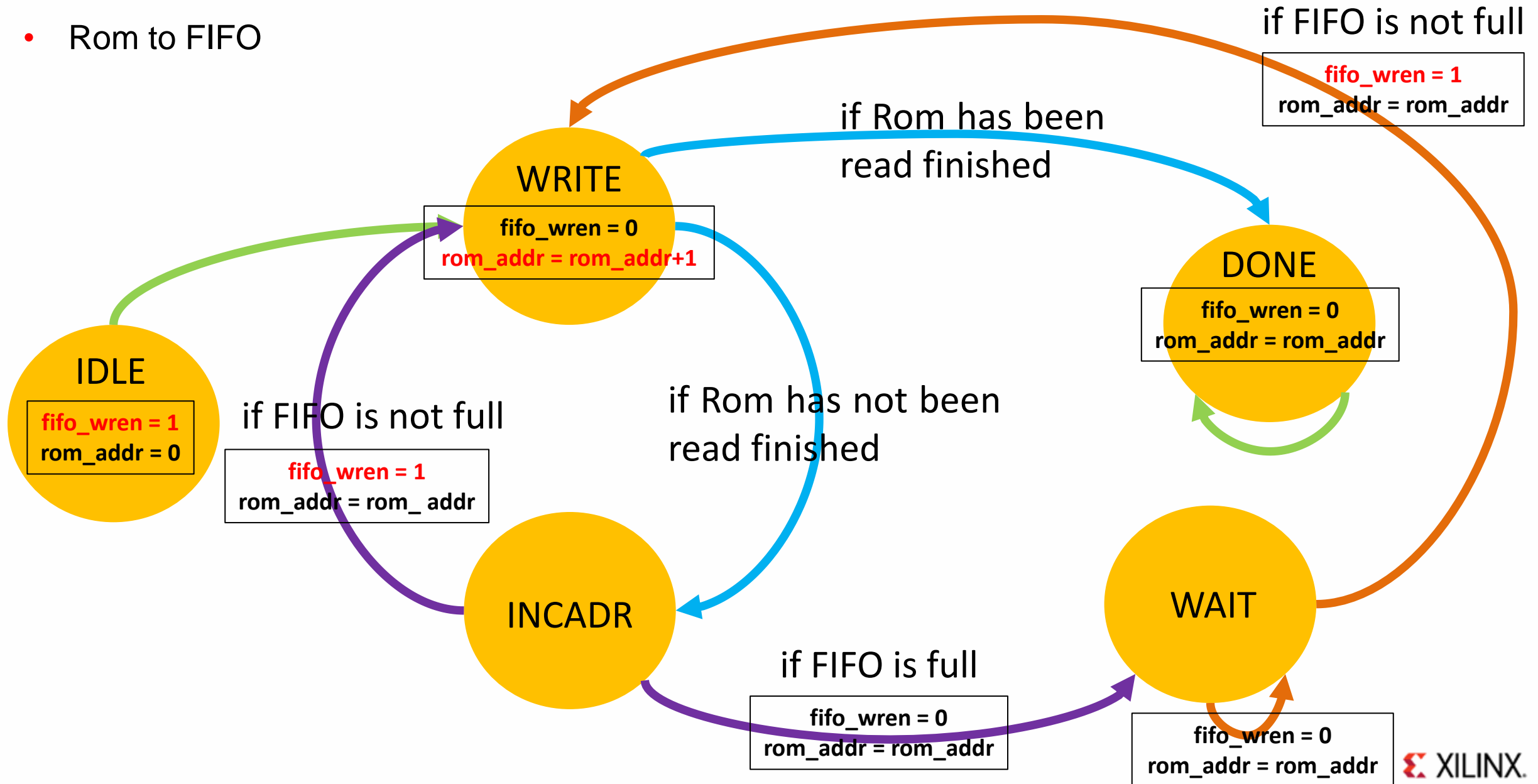
WNS = 0.364 ns

Thank you very much for your attention!

Appendix

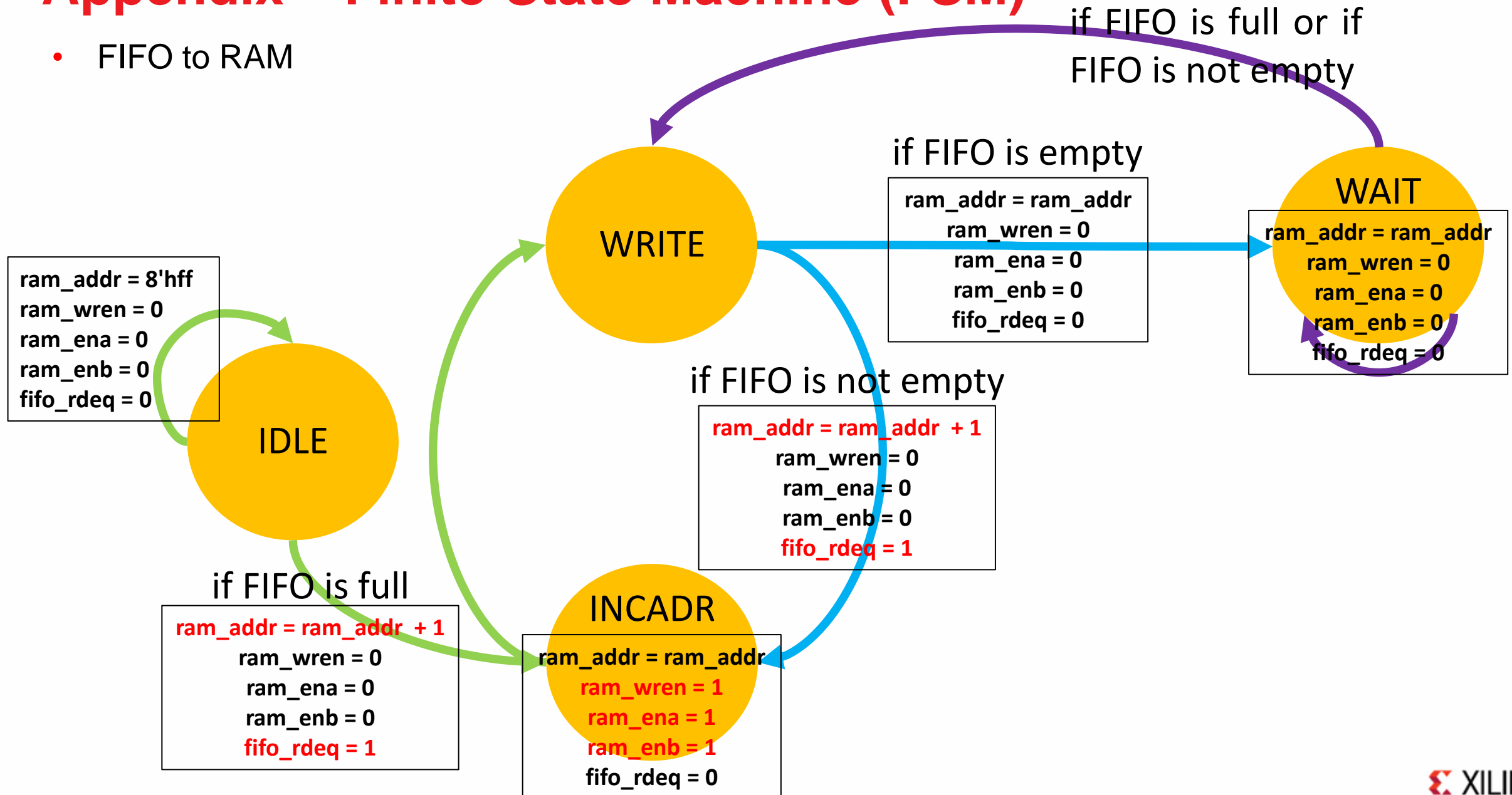
Appendix – Finite-State Machine (FSM)

- Rom to FIFO

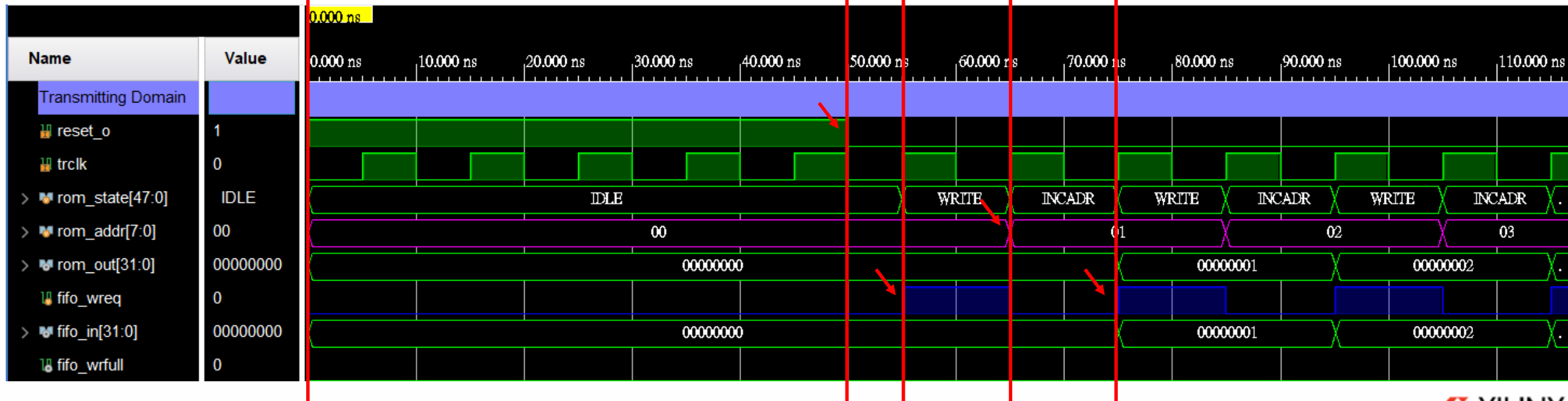
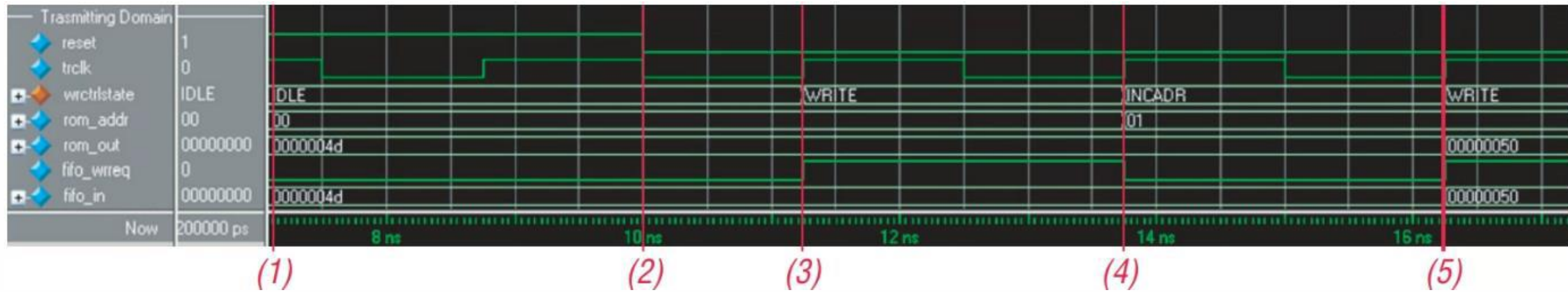


Appendix – Finite-State Machine (FSM)

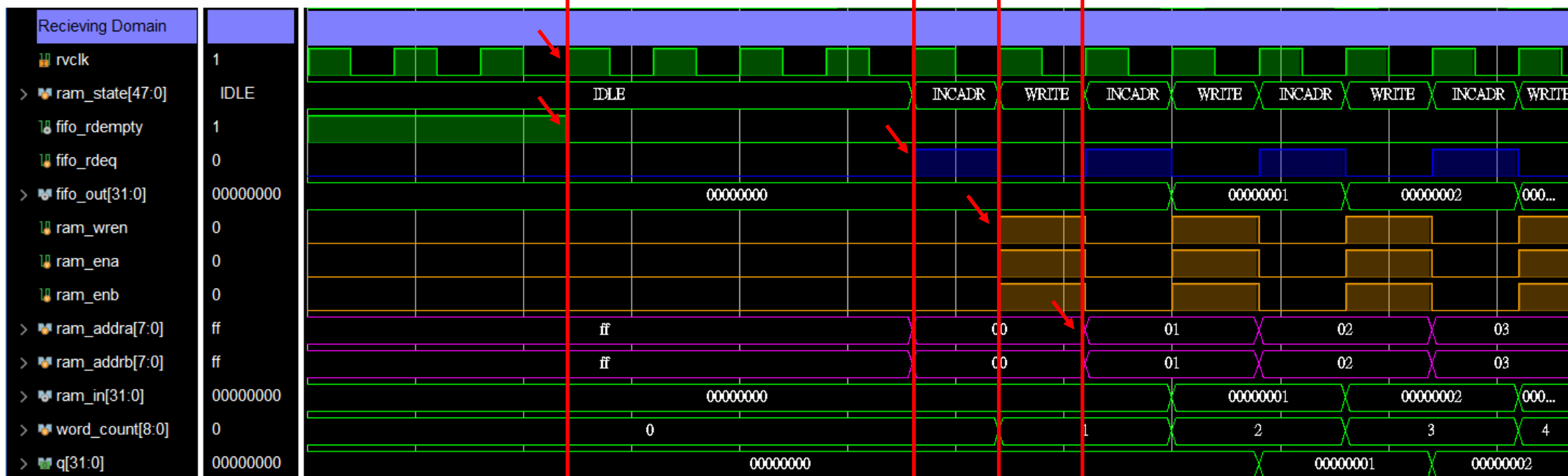
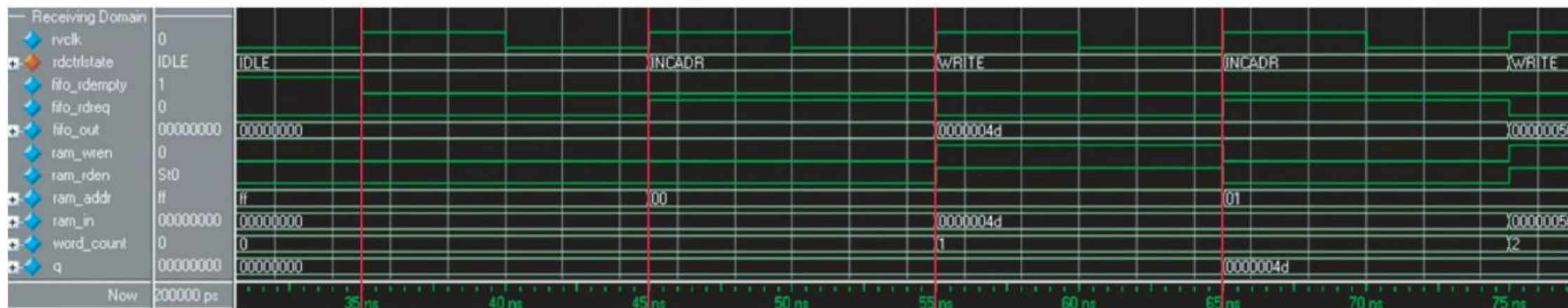
- FIFO to RAM



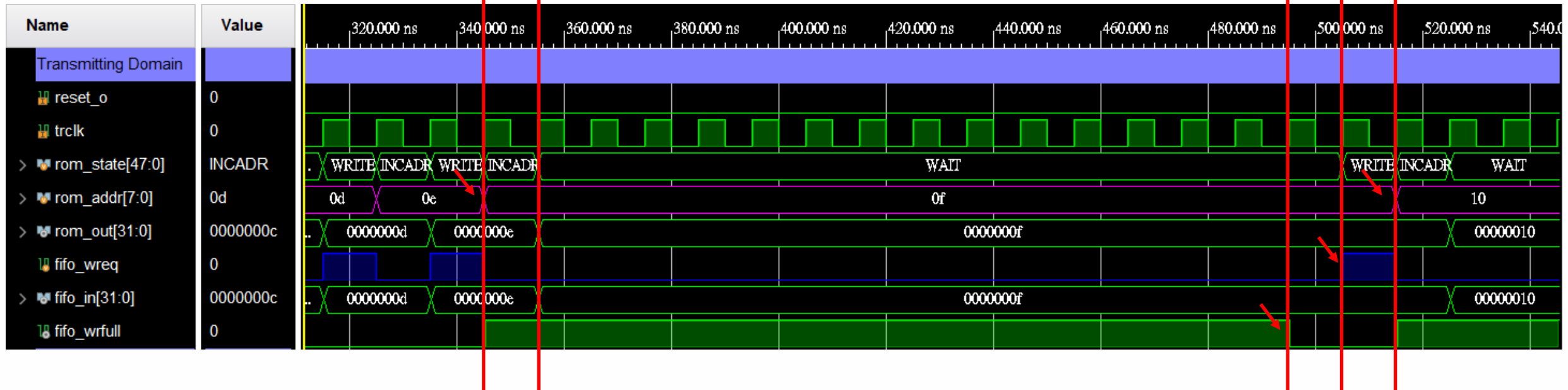
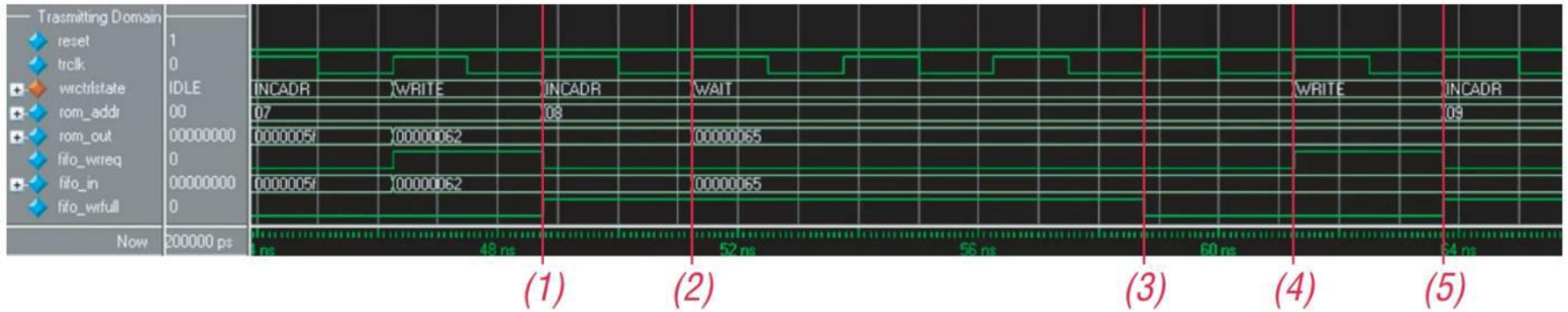
Appendix – Transmitting Domain



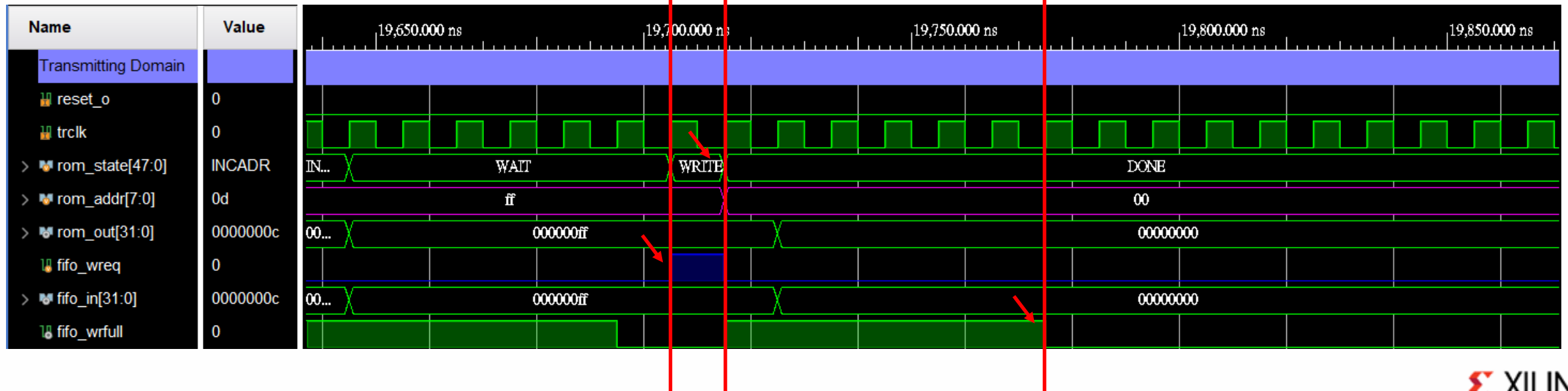
Appendix – Receiving Domain



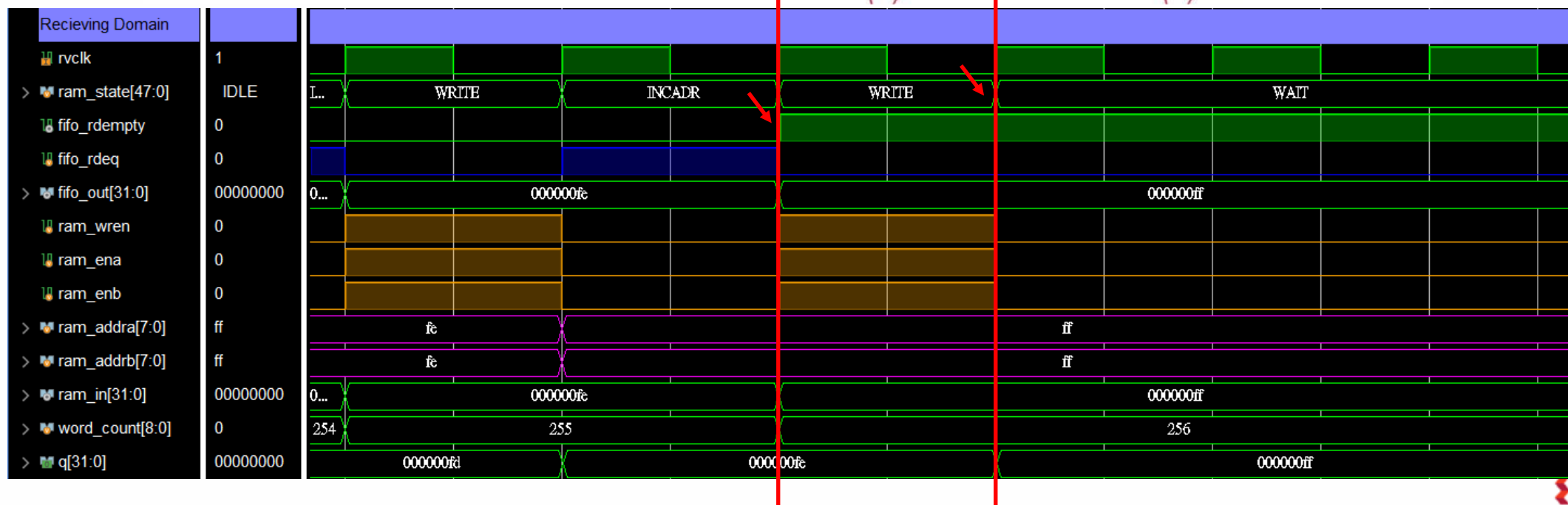
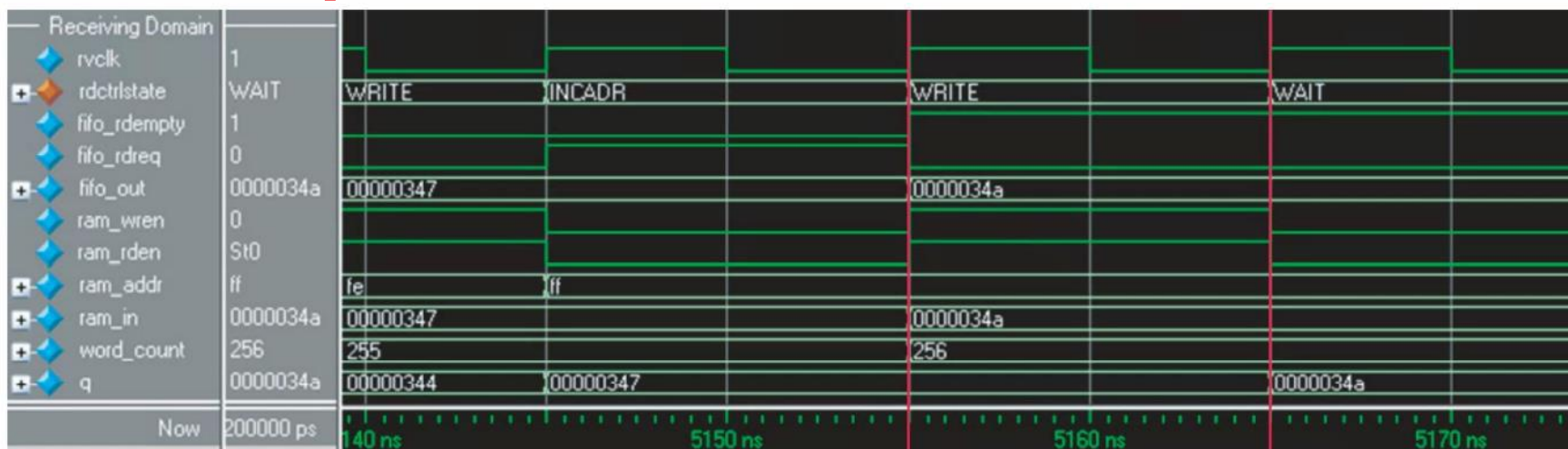
Appendix – When FIFO is full



Appendix – completion of ROM to FIFO



Appendix – completion of FIFO to RAM



Results of Synthesis

- fsm_extraction: auto

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 0.364 ns	Worst Hold Slack (WHS): -0.101 ns	Worst Pulse Width Slack (WPWS): 2.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): -0.101 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 1	Number of Failing Endpoints: 0
Total Number of Endpoints: 232	Total Number of Endpoints: 224	Total Number of Endpoints: 88

Timing constraints are not met.

WNS = 0.364 ns

Results of Synthesis

- fsm_extraction: gray

Design Timing Summary			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): 0.341 ns	Worst Hold Slack (WHS): 0.003 ns	Worst Pulse Width Slack (WPWS):	2.000 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints:	0
Total Number of Endpoints: 232	Total Number of Endpoints: 224	Total Number of Endpoints:	88
All user specified timing constraints are met.			

WNS = 0.341 ns